

Robust to PVT enhanced DC gain amplifier using no Miller capacitor feedforward compensation

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Abstract This paper presents an operational transconductance amplifier compensated in frequency with a feedforward path implemented with current mirrors. This concept eliminates the need of Miller capacitor and improves performance compared to traditional feedforward topologies in regard to DC gain. Gain enhancement is achieved because of the use of current mirrors which reduces the number of the conductances that are connected to the output and increasing output impedance. Moreover, common mode range is improved by the PMOS differential pair used in the feedforward stage. Simulations results for the designed circuit on the typical UMC 180 nm CMOS process, show a DC gain above 60 dB with a unity gain frequency of 511 MHz, a phase margin (PM) of 49°, a slew rate (SR) of 205 V/ μ s and a power consumption of 5.1 mW maintaining low variations in regard to process, voltage and temperature variations.

Keywords Feedforward-compensation · Amplifier · Current mirror · Enhanced gain · PVT

1 Introduction

Amplifiers are important analog blocks in analog signal processing systems. Nowadays, several research is done in order to face the challenges imposed to analog designers by technology scaling and system requirements. For example, for an amplifier intended for communication systems, designer must take into account the degradation caused by power supply and

dimension scaling in characteristics such as input-output dynamic range and DC gain. Additionally, designer must consider the strong requirements in bandwidth, resolution, linearity and power efficiency imposed by the system.

Specification achievement with the amplifiers is not only restricted by technology, also physical and environmental factors must be taken into account. The first ones are essentially permanent and occur in the fabrication process. The second ones are temporal and happen during circuit operation like power supply and temperature variations [1]. Therefore, amplifiers not only must achieve specification but also must be robust to process, voltage and temperature variations (PVT).

In the literature, several topologies of amplifiers are proposed. However, for submicron technologies not all alternatives of conventional CMOS amplifier design are valid. For example, cascode amplifiers is a common concept to improve DC gain, but supply reduction limits their use, leading to the use of cascade amplifiers which are difficult to compensate in frequency. Cascade amplifiers with Miller frequency compensation are commonly used but have limitations in bandwidth because of the large compensation capacitor needed, also its connection between output and gain stages that creates a right-hand-plane zero [2]. A reliable approach to have relatively high DC gain and wide bandwidth is the use of cascade amplifiers with feedforward frequency compensation.

This paper presents the design of a robust to PVT variations operational transconductance amplifier with feedforward frequency compensation which is an extended version of the work in [3]. The proposed amplifier avoids the connection of the feedforward path directly to the output by using current mirrors which enhances output impedance. Also, amplifier output stage provides wide voltage excursion and reduces PVT variations by adding NMOS and PMOS transconductance stages.

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This paper is organized as follows: a review of the feedforward compensation technique is made in the Sect. 2. In the Sect. 3 the proposed circuit is explained and simulations and PVT results are presented in the Sect. 4, along with a comparison between discussed architectures in the previous sections and a summary of performance to compare with amplifiers found in the literature. Finally, some conclusions are drawn in the Sect. 5.

2 No-capacitor feedforward frequency (NCFF) compensation technique

Usually, frequency compensation is implemented with capacitors. The main idea of this compensation type is to do pole-splitting in order to ensure a required PM. However, the use of capacitors limits amplifier bandwidth and slew rate. As feedforward compensation does not use these capacitors, it is an architecture to avoid these limitations.

The feedforward compensation scheme is shown in Fig. 1. The proposed scheme uses two gain stages and a feedforward path which creates a left-half-plane (LHP) zero and a positive phase shift that helps to compensate the negative phase shift of the poles [4]. This conclusion can be explained with the small signal analysis of the scheme of Fig. 1; assuming that $A_{v1} = \frac{g_{m1}}{g_{o1}}$, $A_{v2} = \frac{g_{m2}}{g_{o2}}$ and $A_{v3} = \frac{g_{m3}}{g_{o2}}$ are the DC gain of the three transconductance stages; Feedforward path is implemented by g_{m3} and the first and second poles are located at $\omega_{p1} = \frac{g_{o1}}{C_{o1}}$ and $\omega_{p2} = \frac{g_{o2}}{C_{o2}}$ respectively, the transfer function can be expressed by equation (1) taken from [4].

$$H(s) \cong -\frac{A_{v1}A_{v2} + A_{v3}\left(1 + \frac{s}{\omega_{p1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (1)$$

$$= -\frac{(A_{v1}A_{v2} + A_{v3})\left(1 + \frac{A_{v3}s}{(A_{v1}A_{v2} + A_{v3})\omega_{p1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

The dominant pole of $H(s)$ is located at ω_{p1} , the DC gain is given by $A_{v1}A_{v2} + A_{v3}$ and the LHP zero can be expressed by

$$z_1 = -\omega_{p1}\left(1 + \frac{A_{v1}A_{v2}}{A_{v3}}\right) \cong -\frac{g_{m1}g_{m2}}{C_{o1}g_{m3}} \quad (2)$$

From Eq. (2), the location of the LHP zero is proportional to the gain-bandwidth product (GBW) of the first stage where the proportional factor is $k = \frac{g_{m2}}{g_{m3}}$. To obtain the required PM, g_{m2} and g_{m3} can be sized in such a way that the negative phase shift due to ω_{p2} is compensated by the positive phase shift of the LHP zero. In particular when PM is set to 90° , the frequencies of ω_{p2} and the LHP zero are

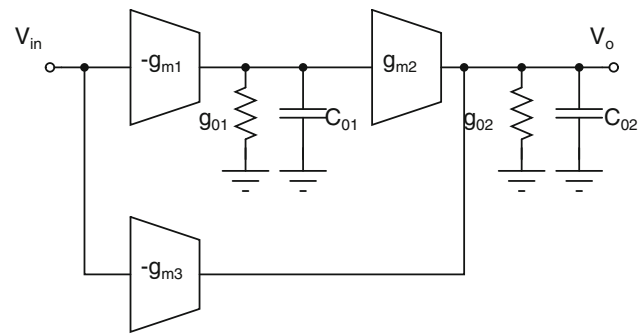


Fig. 1 NCFF compensation scheme [4]

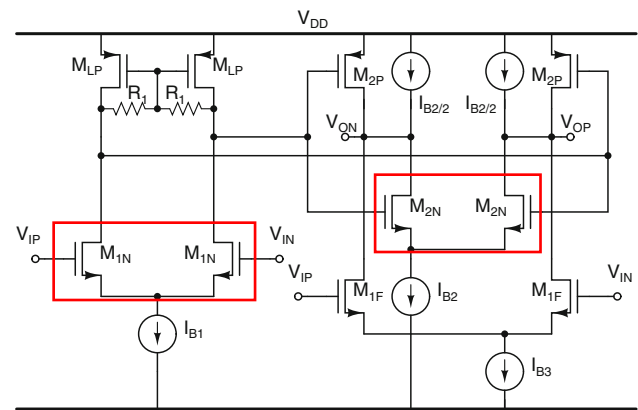


Fig. 2 NCFF amplifier (FFA) [5]

the same and the unity-gain frequency is given by $\omega_{GBW} = A_{v2} \frac{g_{m1}}{C_{o1}}$.

2.1 Circuit level implementation

In [5], an operational transconductance amplifier that uses feedforward compensation is proposed (Fig. 2). The circuit is composed by two gain stages and a feedforward stage (transistors M_{1F}). The first gain stage (transistors M_{1N} and M_{1P}) is resistively loaded to control common mode output. The second stage is composed by a PMOS transconductance stage (M_{2P}) and a NMOS transconductance stage (M_{2N}) with active load. The feedforward stage is implemented by a NMOS differential pair and is applied directly to the output node. Therefore, the output node is charged by four output conductances (hence by four $g_{ds,s}$) which results in a strong reduction of the second stage gain. Besides the problem of reduced gain, the frequency compensation is efficiently implemented achieving a high bandwidth. In the next section it is proposed a circuit modification in order to improve output impedance maintaining the benefits of the frequency compensation. For simplicity, the circuit presented in Fig. 2 will be call FFA in next sections.

3 Proposed circuit realization

The drawbacks mentioned in the previous section can be alleviated with the use of the scheme showed in Fig. 3. The main difference with the scheme showed by Fig. 1 is the use of current mirrors $S_{1,2}$. The main idea is to avoid a direct connection of the output conductance of each stage to the output. The use of current mirrors to drive the output reduces output load (number of $g_{ds,s}$) and allows wide output voltage excursion while the compensation is not significantly affected. This can be explained in a similar way that in the original proposal. To obtain the transfer function of the new scheme, it can be used the same assumptions as in (1), but it must be considered the additional poles of the current mirrors. If it is considered that the poles of $S_{1,2}$ are equal, mathematically the effect of this poles cancel out. However, in a real circuit implementation this condition may be not true. Therefore, the next analysis considers that the poles of the current mirrors are different but the current copy factor is one.

To obtain an idea of how the transfer function of the scheme is modified, it is assumed that $\omega_{S1} = \frac{g_{ms1}}{C_{s1}}$ and $\omega_{S2} = \frac{g_{ms2}}{C_{s2}}$ are the non-dominant poles of the current mirrors. The other terms can be maintained without change, so the transfer function can be expressed as in (3). Here, it can be seen, as it was expected, that there are four poles and two zeros, however in this analysis the LHP zero of higher frequency is neglected. The poles of the current mirrors do not affect the LHP zero approach but these may influence other specifications of the amplifier like GBW, PM and settling time [6], then these poles should be carefully located to avoid degradation of PM and settling time.

$$H(s) \cong - \frac{A_{v1}A_{v2} \left(1 + \frac{s}{\omega_{S1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) \left(1 + \frac{s}{\omega_{S1}}\right) \left(1 + \frac{s}{\omega_{S2}}\right)} - \frac{A_{v3} \left(1 + \frac{s}{\omega_{p1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) \left(1 + \frac{s}{\omega_{S1}}\right) \left(1 + \frac{s}{\omega_{S2}}\right)} \quad (3)$$

Now, it is analysed the effect of the proposed scheme in the LHP zero approach. In (4), it is shown approximately the

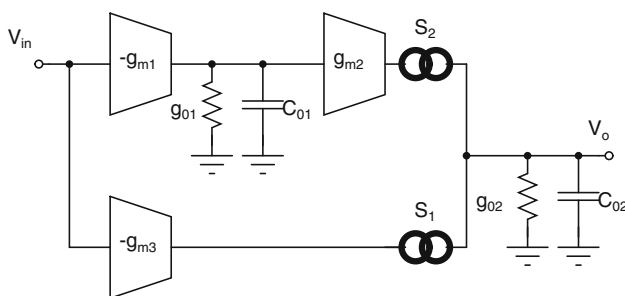


Fig. 3 Proposed NCF compensation scheme

expression for LHP zero. Here, it can be seen that it has the same factor as in (2), but with an additional factor that depends on ω_{S1} where its influence may be reduced if the product $g_{m3}g_{ms1}$ is greater than $g_{m1}g_{m2}$.

Finally, in regard to DC gain the additional poles do not have any negative effect but considering that the connection of each stage to the output is avoided, the output conductance g_{o2} is reduced increasing DC gain. Therefore, the proposed scheme can achieve a higher DC gain with reasonable high GBW and a PM greater than 50° but less than 90° .

$$z_1 = - \frac{\omega_{p1}\omega_{S1}(A_{v1}A_{v2} + A_{v3})}{A_{v3}\omega_{S1} + A_{v1}A_{v2}\omega_{p1}} \cong - \frac{g_{m1}g_{m2}g_{ms1}}{g_{m3}g_{ms1}C_{o1} + g_{m1}g_{m2}C_{s1}} \quad (4)$$

The circuit realization is shown in the Fig. 4 which can be explained as follows: The first gain stage is a differential pair resistively loaded (transistors M_{IN} and M_{LP}) in order to compare with the circuit in [5]. The second stage is composed by the transistors M_{2P} and a NMOS differential pair (M_{2N}) that used current mirrors as charge. Feedforward stage is implemented by PMOS differential pair with current mirrors as charge (transistors M_{IF} and M_{CF}). Finally, the output stage is composed by transistors M_{OSP} and M_{OSN} which allow wide output voltage excursion and the output load (number of $g_{ds,s}$) is reduced because only three transistor's drains are connected to the output.

For the design, non-dominant poles must be taken into account. For properly operation, the frequency of one non-dominant pole is separated twice from the another one and both frequencies are set larger than GBW. The values of the transconductance stages are $g_{m1} = 219 \mu A/V$, $g_{m2} = 1.81 \text{ mA/V}$, $g_{m3} = 3.24 \text{ mA/V}$; for the transconductance of the current mirrors the values are $g_{ms1} = 3.24 \text{ mA/V}$ and $g_{ms2} = 1.81 \text{ mA/V}$.

In next section, simulations results are presented. Henceforth, the circuit presented in 4 will be call PFFA. In [5] it mentioned that the amplifier maintains low gain variations despite PVT variations; therefore, a comparison between proposed amplifier and the proposed in [5] are made by using PVT simulations in order to prove the gain enhancement while maintaining the same or even less gain variations.

4 Simulations and comparison

The technology used to develop the design was the typical UMC 180 nm CMOS process and simulations were carried out in Hspice. Power supply was set to 1.8 V and the used load capacitance was 1 pF. The amplifiers were designed to deliver the same output current maintaining a similar

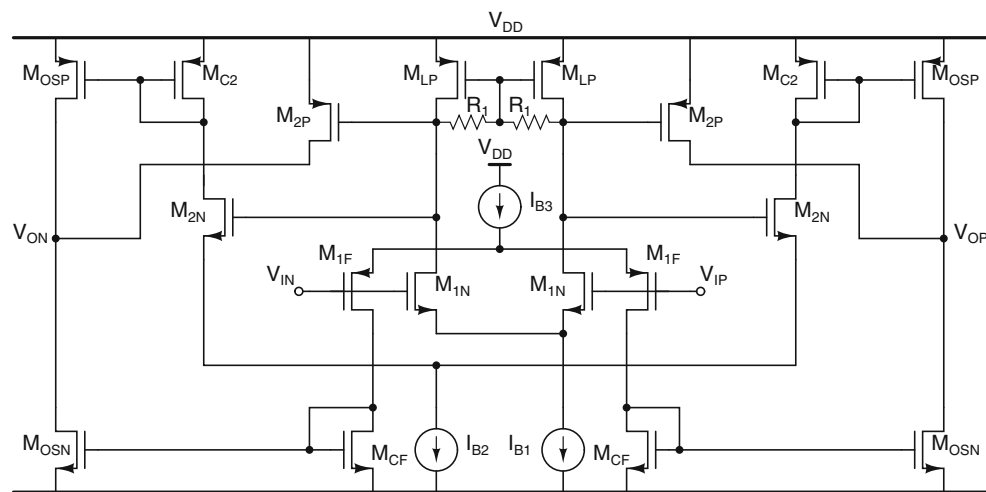


Fig. 4 Proposed NCCF amplifier (PFFA)

power consumption in order to make a performance comparison related to DC gain, GBW and PM and only pre-layout simulations are considered in Sects. 4.1, 4.2 and 4.3. The main idea is to show that the PFFA amplifier has a similar performance compared to circuit proposed in [5] while improving the DC gain. Also, PVT simulations are made for both the PFFA and the FFA topologies. Finally, post-layout results of the proposed circuit are presented in Sect. 4.4. Design parameters for the proposed circuit are shown in Table 1.

4.1 Frequency response

The frequency response of the two amplifiers is shown in the Fig. 5. It can be seen that the proposed amplifier achieve above 63 dB of the DC gain while the FFA achieve around 58 dB (Fig. 5(a)). The difference is because the output impedance of the PFFA is around 12.8 K Ω and the output impedance of the FFA is around 6.6 K Ω which is equivalent to a gain improvement above 5 dB. Therefore, the DC gain is improved as it was expected. On the other hand, GBW of the PFFA is 548 MHz while GBW of the FFA is 595 MHz for a similar power consumption, 4.83 and 4.65 mW respectively. In regard to phase margin, the PFFA has around 52° and for the FFA is close to 90° (Fig. 5(b)).

Table 1 Design parameters of the PFFA

$L : 0.54 \mu\text{m}$	$R_1 : 600 \text{ k}\Omega$
$W_{IN} : 3.24 \mu\text{m}$	$W_{LP} : 10.44 \mu\text{m}$
$W_{IF} : 178.56 \mu\text{m}$	$W_{CF} : 37.44 \mu\text{m}$
$W_{2N} : 25.92 \mu\text{m}$	$W_{C2} : 83.52 \mu\text{m}$
$W_{OSP} = W_{2P} : 167.04 \mu\text{m}$	$W_{OSN} : 74.88 \mu\text{m}$

4.2 Transient response

The output stage of the proposed amplifier allows wide voltage excursion as can be seen in the Fig. 6. Here, the simulations for both amplifiers were made by using an input frequency of 10 KHz and a similar amplitude of the input signal ensuring a total harmonic distortion around 1 %. In the Fig. 6, output voltage of the FFA is also shown and has a differential amplitude of 300 mV while the PFFA has 800 mV of voltage excursion.

To validate the PM and GBW of both amplifiers, the step response was simulated for unity gain configuration and an input step of 200 mV with a rise time of 0.1 ns. The differential output of both amplifiers is shown in Fig. 7. As expected, for the PFFA amplifier the output waveform shows the influence of the non-dominant poles, i.e., the behavior of the response shows a high order transfer function, not a first order transfer function as it can be achieved for the FFA amplifier. Therefore, the PFFA amplifier shows a significantly overshoot of 20 mV but the behavior is similar to the FFA, in regard to slew rate (SR) and settling time. SR for FFA is 150 V/ μs while for the PFFA is 210 V/ μs with a 0.1 % settling time of 50 and 40 ns respectively. This improvement is achieved because the SR is directly related to the load capacitance and as the proposed circuit reduces the number of transistor connected to the output, the number of parasitic capacitances are less, and the effective load capacitance is reduced. Despite having better SR, the PFFA amplifier has a similar settling time because the influence of the non-dominant poles; as it was mentioned, a high order transfer function increases the settling time specification by adding more time constants to the responses. On the other hand, the FFA amplifier has a high settling time because of the high PM.

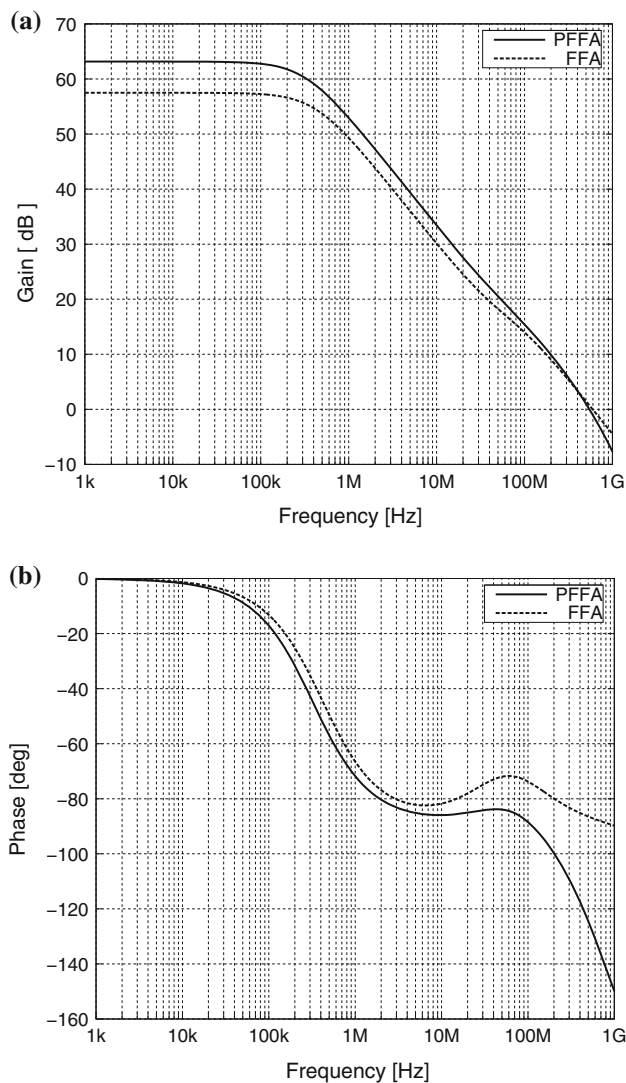


Fig. 5 Frequency response, **a** magnitude and **b** phase of amplifiers

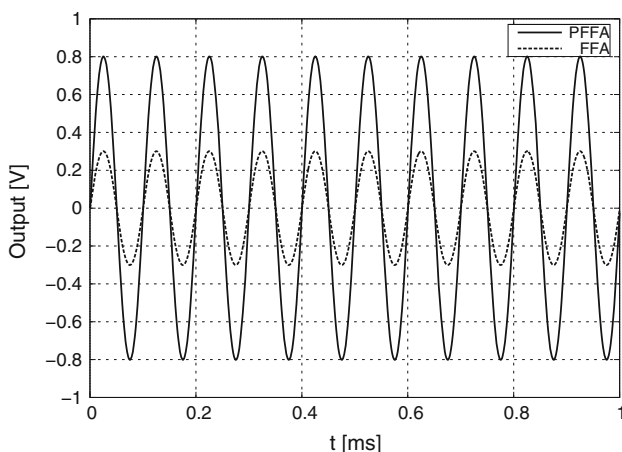


Fig. 6 Sinusoidal response of both amplifiers

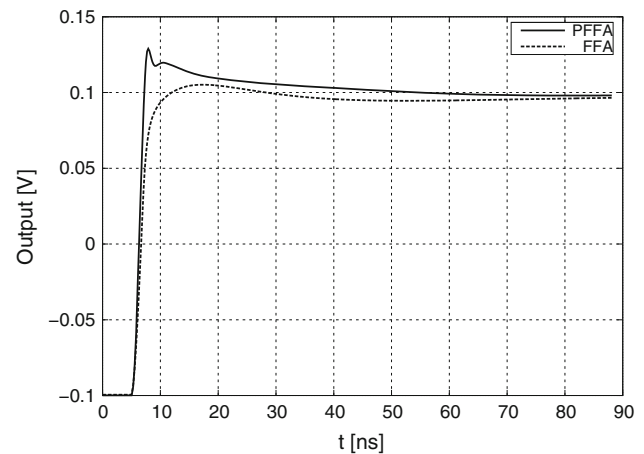


Fig. 7 Step response of both amplifiers

An additional interesting behavior of the PFFA amplifier is the common mode operation. Because of the use of a PMOS differential pair in the circuit input, the gain of the amplifier can be maintained high despite having low common mode values while both amplifiers have similar V_{DSat} . The Fig. 8 shows the transient behavior of both amplifiers with the same simulation setup of the step response. Here, the input of the amplifiers is varied from 0 to 1.8 V and it is observed how the output follows the input. The Fig. 8(a) correspond to the FFA and Fig. 8(b) to the PFFA. In this figures, it can be observed that the PFFA output follows the input for values from 0.3 to 1.4 V while for the FFA the minimum value is 0.5 with a maximum of 1.4 V, thus, the PFFA can operate to lower values of common mode.

4.3 PVT simulations

Table 2 shows the simulation setup for PVT variations. The technology used allows simulations in five process corners, to the power supply is used $\pm 10\%$ and temperature varies from -20 to 100°C . Both amplifiers are simulated under same conditions and only frequency response was studied in order to observe variations in DC gain, GBW and PM. The proposed amplifier shows a better performance to process variations compared to the FFA as it can be seen in the Fig. 9, where only the five corners process are considered; this magnitude response shows that for the FFA (Fig. 9(a)) the SS and FF corners has variations that are appreciable while for the PFFA (Fig. 9(b)) the values of all five corners are pretty similar. While the PFFA has a maximum gain variation of 2.3 % and GBW changes about 6 % maintaining a PM variation less than 0.1 %, the FFA has variations of 8.3 % in DC gain and 7 % in GBW

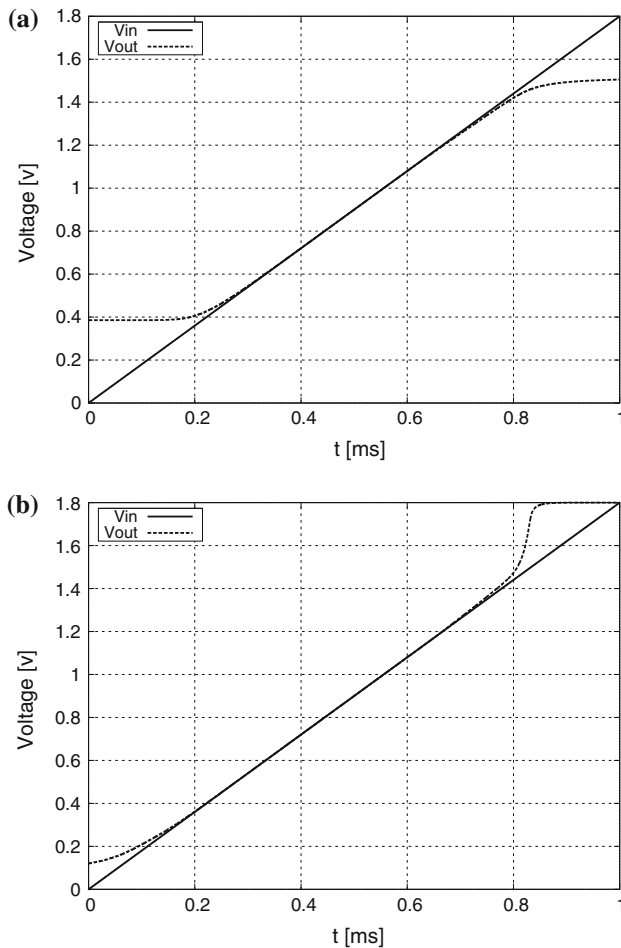


Fig. 8 Common mode variation for FFA (a) and PFFA (b)

Table 2 Simulation corners

Process	SS	SF	TT	FS	FF
Voltage	$V_{DD} - 10\%$	-	V_{DD}	-	$V_{DD} + 10\%$
Temperature	$-20\text{ }^{\circ}\text{C}$	-	$60\text{ }^{\circ}\text{C}$	-	$100\text{ }^{\circ}\text{C}$

maintaining a PM variation less than 0.1 %. So, the proposed amplifier shows similar robustness in the frequency compensation and reduced process variations because reducing the number of transistor in the output not only improve DC gain, besides increasing output impedance and reducing output capacitance, also the sources of variations connected to the output are reduced. Additionally, as the output impedance of proposed circuit is higher than the FFA amplifier, the percentage variations in the impedance are more significant in the FFA than in the PFFA.

The Fig. 10 presents overall PVT simulations results for both amplifiers regard to gain magnitude. As expected, the PFFA (Fig. 10(a)) shows better performance having a

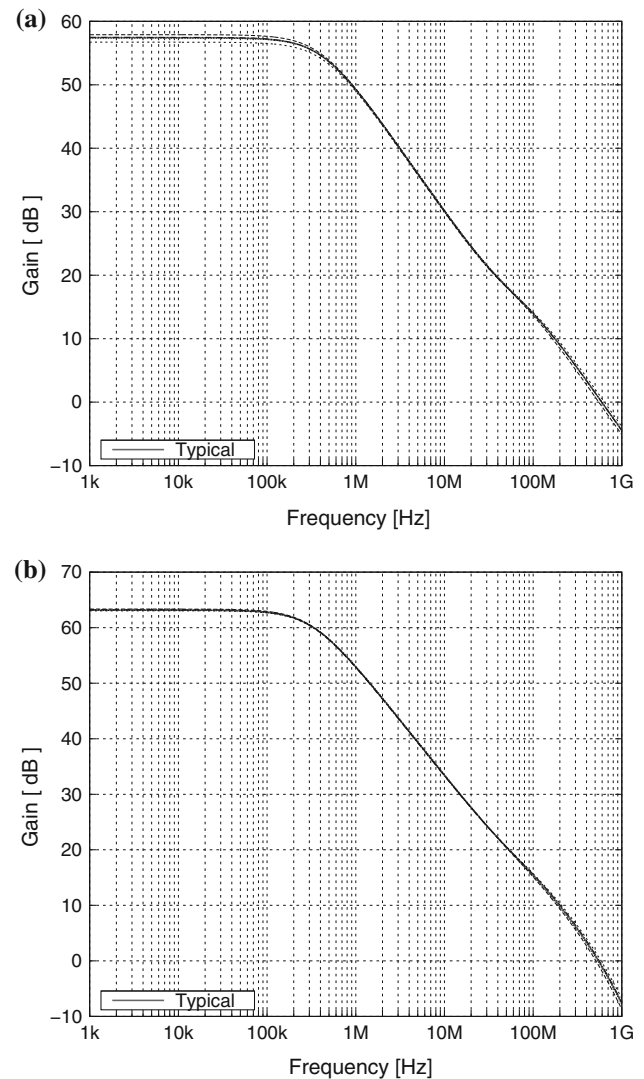


Fig. 9 Process variations: **a** magnitude variations of the FFA and **b** magnitude variations of the PFFA

minimum and maximum gain of 61.7 and 65.3 dB while the FFA (Fig. 10(b)) has 53.3 and 60.2 dB of minimum and maximum gain respectively. Also, GBW variations are reduced by proposed circuit which its minimum and maximum are 481 and 676 MHz; to the FFA, the values are 477 and 814 MHz respectively.

Table 3 summarizes amplifiers PVT performance with respect to frequency response. Here, it can be seen that the PFFA enhances not only DC gain but also robustness to PVT variations. PM of the proposed amplifier has similar changes compared to the FFA despite of having lower values.

4.4 Post-layout simulations

Layout implementation of PFFA circuit is presented in Fig. 11. For better matching, common centroid respect to

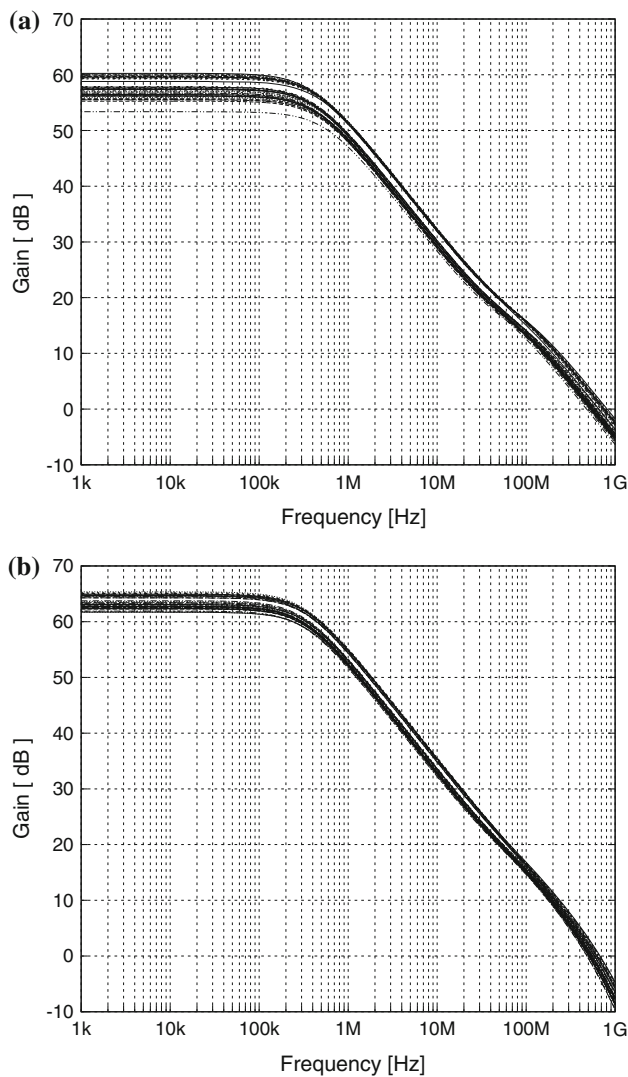


Fig. 10 PVT variations: **a** magnitude variations of the FFA and **b** magnitude variations of the PFFA

Table 3 Circuit specification

Specification	Typ.	Min.	Max.
FFA			
Gain	57.4 dB	53.3 dB	60.2 dB
GBW	595 MHz	477 MHz	814 MHz
PM	92.6°	91.8°	94.2°
PFFA			
Gain	63.1 dB	61.7 dB	65.3 dB
GBW	547 MHz	481 MHz	676 MHz
PM	52.3°	51.8°	53.6°

the NMOS input differential pair has been used. Post layout simulations for PVT variations was obtained, and the results are presented in Fig. 12. The Fig. 12(a) shows the magnitude response which has similar characteristics as

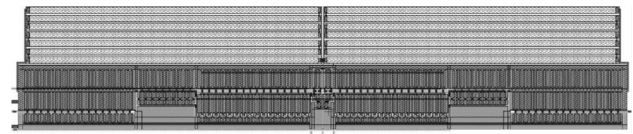


Fig. 11 Layout of PFFA amplifier

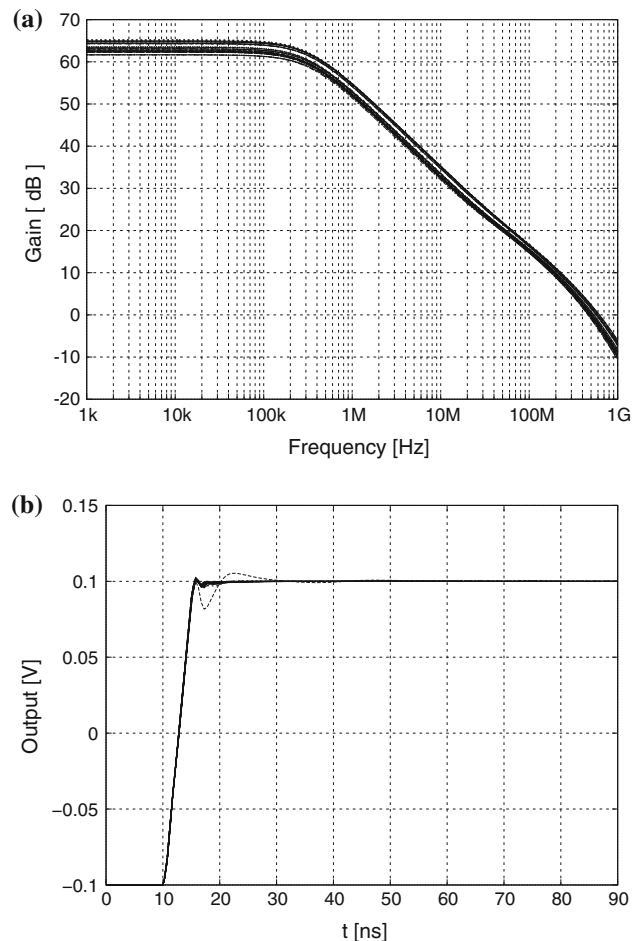


Fig. 12 Post-layout frequency response (a) and step response (b) of PFFA

pre-layout simulations. DC gain of the amplifier is always over 61 dB and despite the GBW is reduced to 511 MHz, the variations are even less than pre-layout simulations. PM is higher than 47° for all simulations corners. To validate the stability of the amplifier, transient response was obtained. Fig. 12(b) shows the step response where it can be seen amplifier is stable for all corners and in the worse case the settling time of 1 % is 60 ns. The power consumption was around 5.1 mW.

Finally, based in the Figures of merits (FoM) proposed in [7] [defined as (5) and (6)], the Table 4 shows a comparison with other amplifiers found in the literature which present only simulation results. With the exception of [8]

Table 4 Comparison of different amplifiers

Ref. (year)	SR (V/ μ s)	Power (mW)	DC gain (dB)	PM ($^{\circ}$)	GBW (MHz)	Technology CMOS (nm)	FoM1 $\left(\frac{V}{\mu s} \frac{pF}{mW}\right)$	FoM2 $\left(\frac{MHz \cdot pF}{mW}\right)$
[9] 2011	-	3.24	90.3	63.8	700($C_L = 0.5$ pF)	180	-	108
[8] 2012	-	9	91.5	62	714($C_L = 7.5$ pF)	130	-	595
[10] 2013	150	1	63	65	500($C_L = 0.3$ pF)	45(SOI)	45	150
[5] FFA	150	4.65	58	92	595($C_L = 1$ pF)	180	32.2	127.9
PFFA	205	5.1	63	49	511($C_L = 1$ pF)	180	40.2	100.2

Post-layout results

the PFFA amplifier presents a similar performance to other amplifiers. The power consumption can be optimized to improve the FoM2.

$$FoM1 = \frac{SR \cdot C_L}{Power} \quad (5)$$

$$FoM2 = \frac{GBW \cdot C_L}{Power} \quad (6)$$

5 Conclusion

An operational transconductance amplifier that uses NCFF compensation is proposed. The proposed circuit uses current mirrors to add second gain stage and feedforward stage to the output increasing output impedance. As a result, DC gain is enhanced and also wide output voltage excursion is allowed. Also, the input common mode range is improved for PFFA by the use of PMOS differential pair in the feedforward stage. Simulations performed with Hspice on the typical CMOS 180 nm UMC process shows that the amplifier has a DC gain of 63 dB, GBW product of 511 MHz, a phase margin of 49 $^{\circ}$, a SR of 205 V/ μ s and a power consumption of 5.1 mW. The comparison made shows a similar performance for both amplifiers despite of the proposed circuit has lower phase margin. PVT simulations of the amplifiers proves that the PFFA improve robustness maintaining DC gain above 60 dB even for post-layout simulations.

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