- BCD technologies for 80 V -200 V and 700 V

BCD technology classification

High Voltage BCD (HV BCD)

: DMOS Voltage Capability from 500V/1200V
: Medium Market Size
: Medium – Low complexity (LSI)

Medium Voltage BCD

: DMOS Voltage Capability from 80V/300V
: Large arket Size
: Medium complexity (LSI)

High Power BCD (HP BCD)

: DMOS Voltage Capability from 30V to 120V
: Large Market Size
: Medium Complexity (LSI)

High Density BCD (HD BCD)

: DMOS Voltage Capability from 5V to 80V
: Small Market Size
: Large Complexity (VLSI)
: Follows the VLSI roadmap in terms of scaling (typically 3 generations behind)

BCD technology classification

- ❑ HV and Medium Voltage BCD (medium-low complexity)
  - From JI Resurf substrate to SOI + STI and DTI (Trench etch isolations)
  - Single gate oxide
  - DMOS Lateral Structure
  - DMOS voltage capability from 80V/300V to 500V/1200V
  - * Emerging LIGBT
- ❑ HP BCD (high power, medium complexity)
  - Conventional JI substrate, simple process architecture
  - Single gate oxide
  - DMOS Lateral(low voltage) and Vertical(high voltage)
  - DMOS voltage capability from 30V to 120V
  - * Emerging Vertical and Lateral Superjunctions and LIGBTs
- ❑ HD BCD (high density, large complexity)
  - CMOS like substrate and process architecture
  - Dual gate oxide for CMOS and DMOS
  - DMOS Lateral Structure
  - DMOS voltage capability from 5V to 80V
  - NVM compatibility
  - RF capability
  - High degree of Modularity

80 -200 V BCD Features for different generations

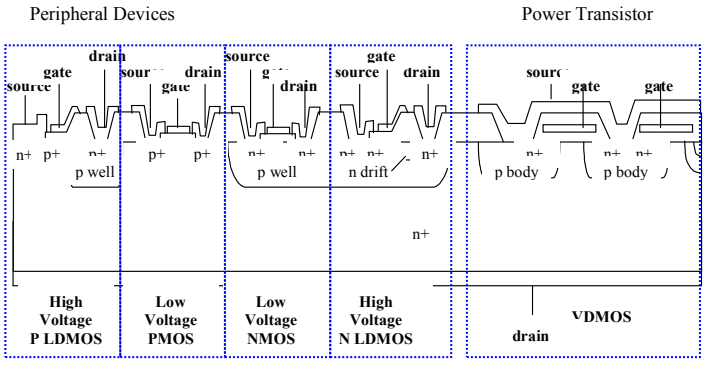
	BCD-SOI	BCD-SOI (ABCD 9)	BCD3s	BCD4	BCD5	BCD6	BCD8	BCD9
Litho (um)	1.0	0.13	1.0	0.8	0.6	0.35	0.18	0.13
Dual Gate Oxide	N	Y	Y	N	Y	Y	Y	Y
CMOS L-gate (um)	1.0	0.13	1.0	0.8	0.6	0.35	0.18	0.13
CMOS(V)	5	1.2/3.3	5	5	5	3.3/5	1.8/3.3	1.2/3.3
DMOS Structure (Lateral/Vertical)	L	L	L&V	L&V	L	L	L	L
Complementary Power DMOS	Y	N	N	N	Y	Y	Y	Y
DMOS(V)	12.0/170/200	100	16/45 /65/80/90	30/45 /65/80/90	16/20/30/45 /65/90	5/12/20 /30/45/65	5/12/20/45	5/12/20
NVM Compatibility	-	-	Y	-	Y	Y	Y	Y
Metal Levels (last one thick)	2-3	3	2~3	2~3	2~3	3~4~5	4~5~6	4~5~6
Cu metal *(optional)	N	Y	N	Y*(thick)	Y*(thick)	Y*(thick)	Y*(thick)	Y* (thin/thick)

Reference : ST roadmap

Gate Oxide Considerations

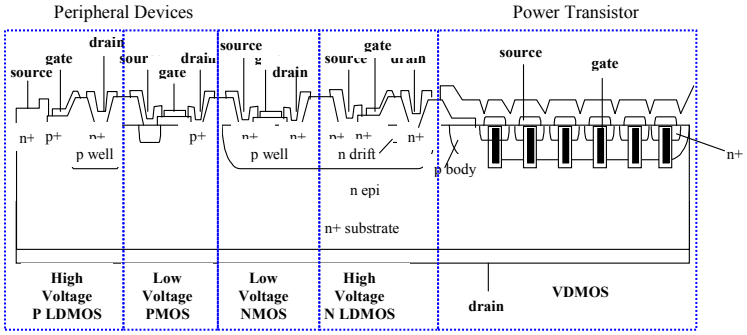
- **Double Poly - Dual Gate Oxide**
  - High Performance CMOS Logic
  - Suitable for High bias DMOS gate voltage
  - Process Complexity
- **Single poly – Mono gate Oxide**
  - High Power DMOS and Low performance CMOS Logic
  - Low cost Process
  - Process Simplicity

BCD with a vertical power MOSFET and some LDD MOSFETs



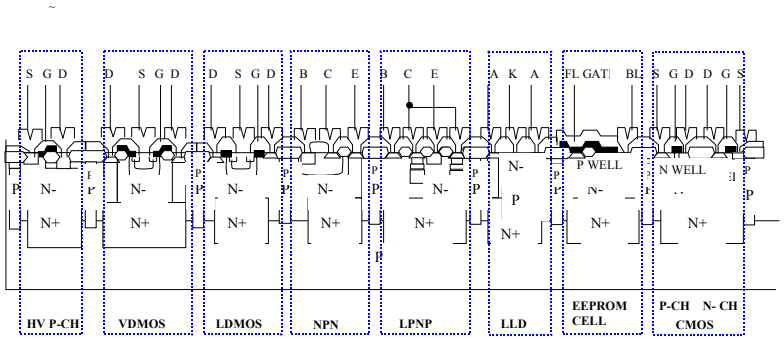
A BCD type process employing a pure vertical high voltage device (Power MOSFET), CMOS cells and high voltage lateral devices

BCD with a vertical power Trench MOSFET and some LDD MOSFETs



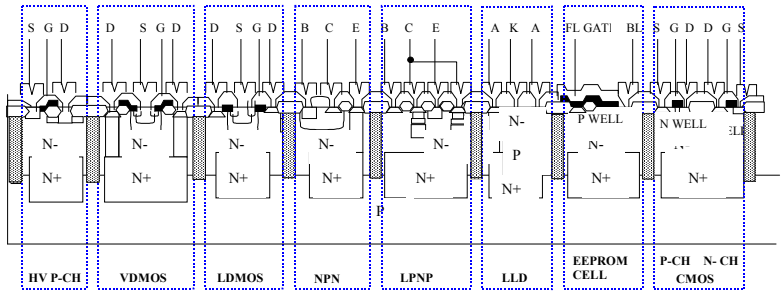
A BCD type process employing a pure high voltage vertical device (in the case a Trench Power MOSFET), CMOS cells and high voltage lateral transistors

Multipower BCD process BCD with quasi-vertical VDMOS, LDMOS, EEPROM and bipolar transistors



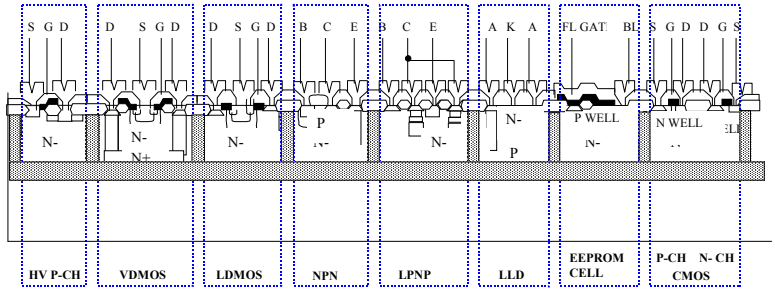
Cross-section of BCD-III process in bulk silicon featuring p+ isolations and n+ buried layers

Multipower BCD process BCD with quasi-vertical VDMOS, LDMOS, EEPROM and bipolar transistors and trench isolation



Cross-section of Multipower BCD process in bulk silicon featuring trench isolations and n+ buried layers

Multipower BCD process in SOI technology



Cross-section of SOI BCD process featuring svereal power components, C<OS cells, bipolar transistors, EEPROM cell

- SOI technology and prospects

The case for SOI in power ICs !

SOI = Silicon On Insulator

SOI: an active semiconductor layer that is separated from the passive semiconductor substrate through a buried insulating material

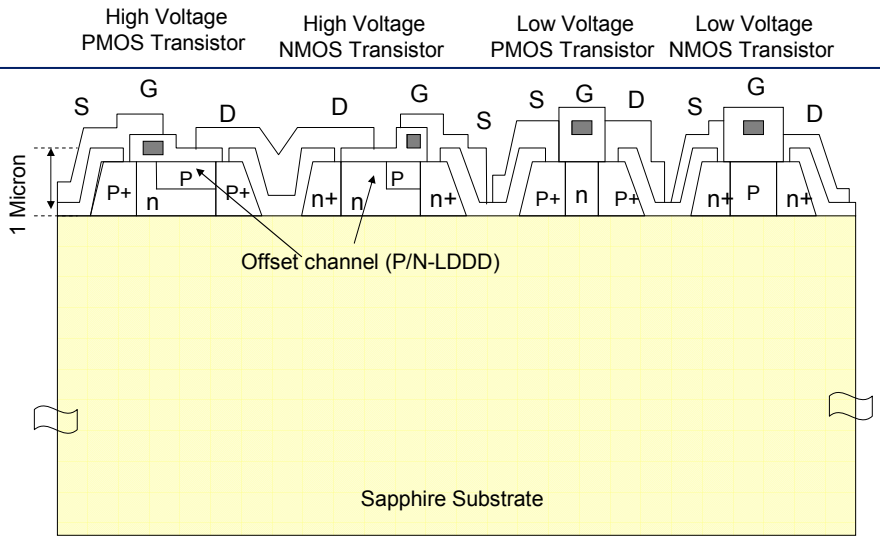
SOI for Power ICs

+

- vertical isolation is achieved via a buried insulated layer
- very low interference between adjacent devices
- high speed (for bipolar devices such as Diodes & LIGBT)
- low area consumption
- Fast reverse recovery for diodes
- Flexible to integrate a variety of high voltage devices (LIGBT, diodes, thyristors, high voltage BJT).
- Allows integration of more than one HV switch in the IC.
- Less affected by high side or bellow handle wafer operation
- No latch-up
- Substrate and BOX can form a back field plate that allows significant reduction in Ron..

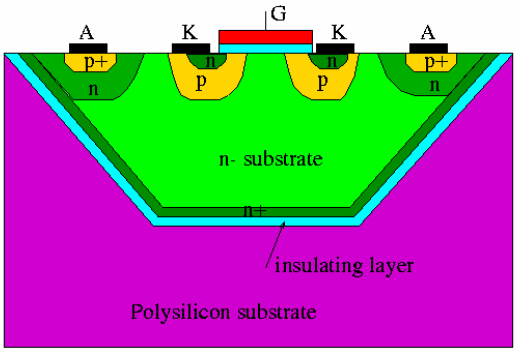
-

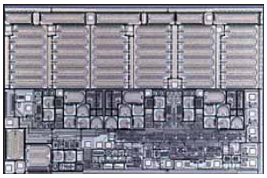
- self-heating
- the substrate is relatively expensive
- Breakdown limited by the BOX thickness



Cross-section of a Silicon on Sapphire (SOS) high voltage IC (30 V-60 V). SOS has been largely abandoned in favour of SOI.

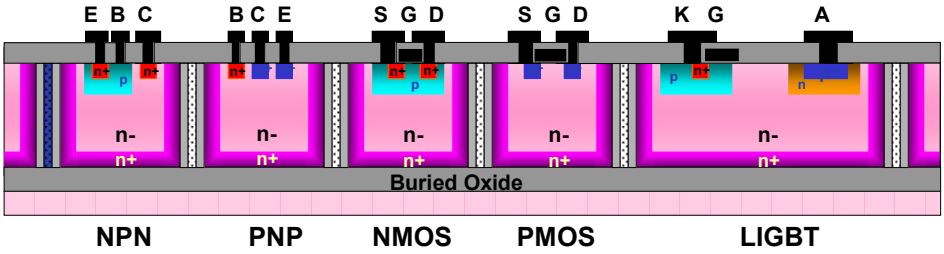
An IGBT structure in the DI -tub technology



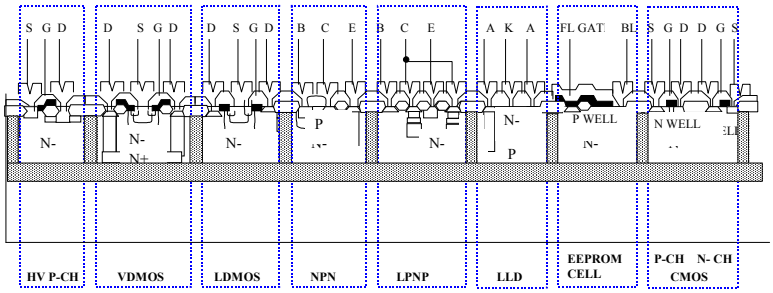


Cross-section of a Dielectric Isolation (DI) high voltage vertical IGBT (500 V) developed by Hitachi. The technology has been very successful but it is reaching its limit.

An LIGBT structure in thick SOI technology

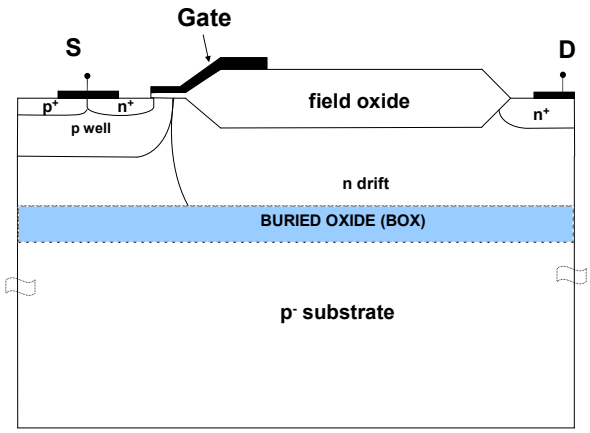


Multipower BCD process in SOI technology

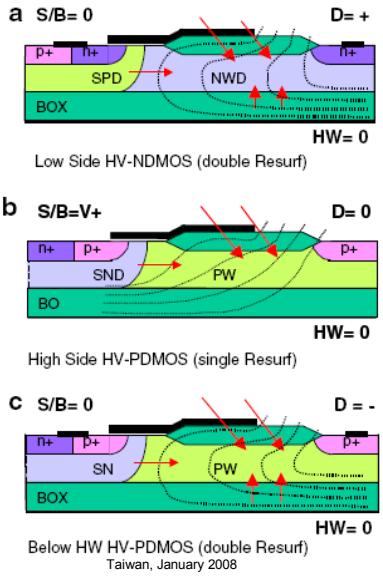


Cross-section of SOI BCD process featuring svereal power components, C<OS cells, bipolar transistors, EEPROM cell

LDMOSFET in thick SOI technology



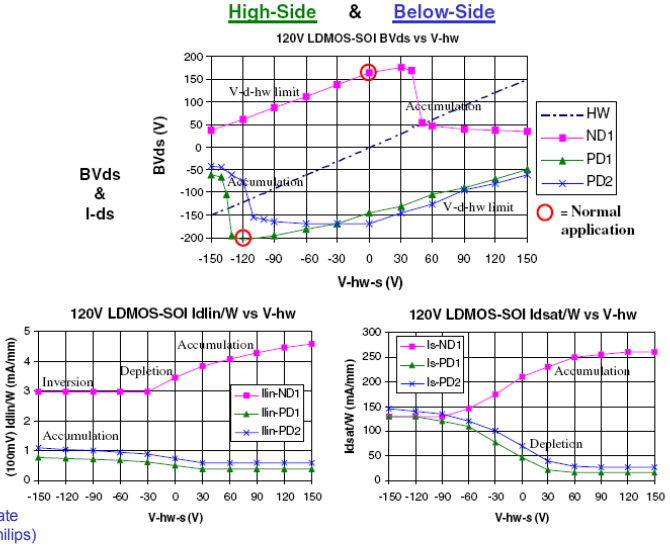
Low side and High Side LDMOSFETs in SOI



P. Wessels, Solid State Electronics 2007, (Philips)

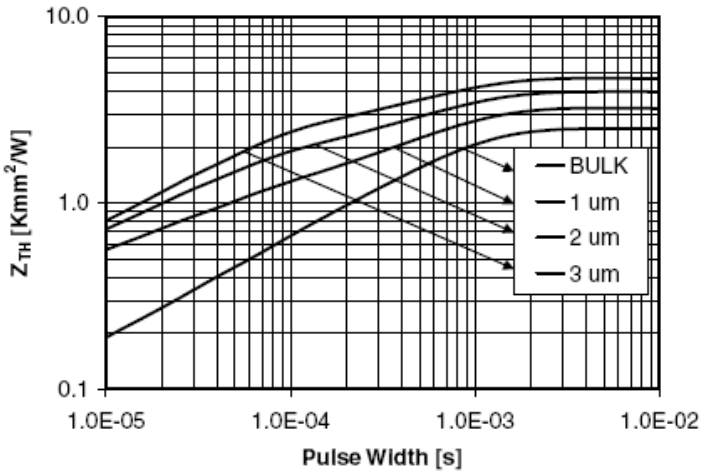
Effects of substrate bias on electrical performance of SOI LDMOSFETs

High-Side & Below-Side



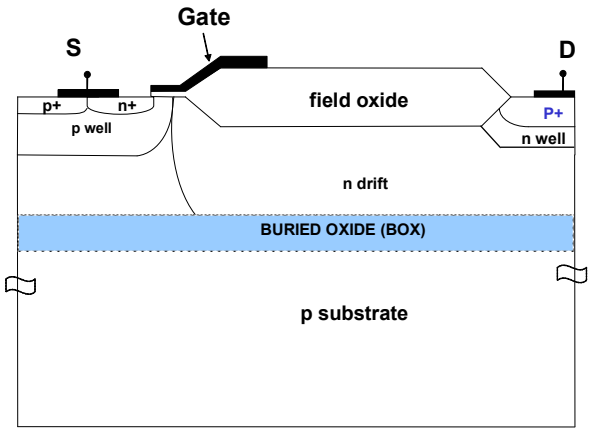
P. Wessels, Solid State Electronics 2007, (Philips)

Thermal impedance of SOI vs Bulk

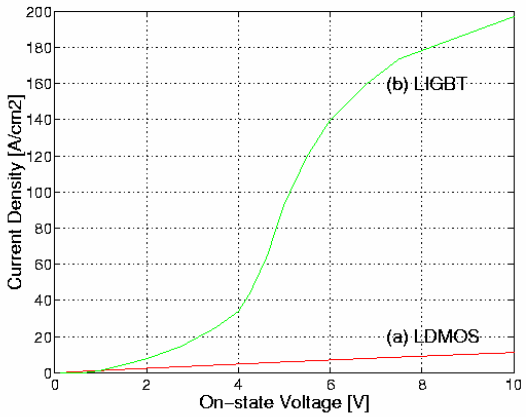


P. Wessels, Solid State Electronics 2007, (Philips)

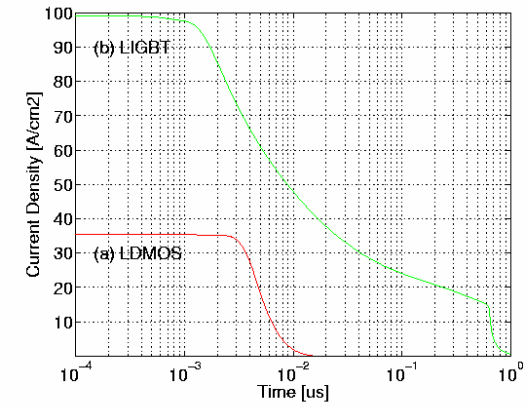
LIGBT in thick SOI



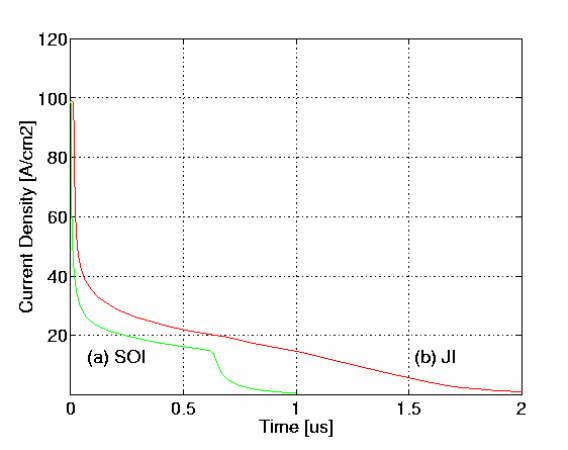
Typical On-state characteristics for an SOI LDMOSFET and an SOI LIGBT



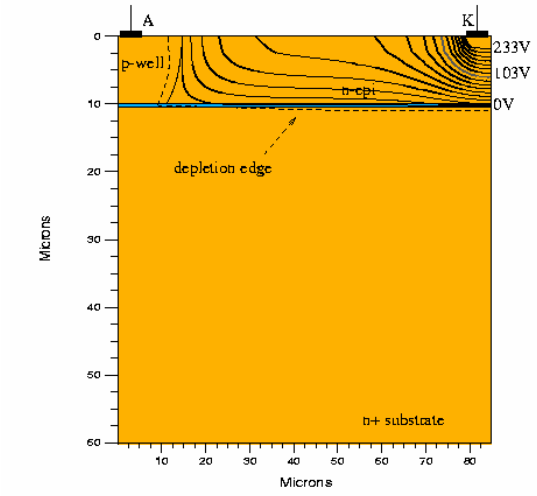
Typical turn-off characteristics for an SOI LDMOSFET and an SOI LIGBT



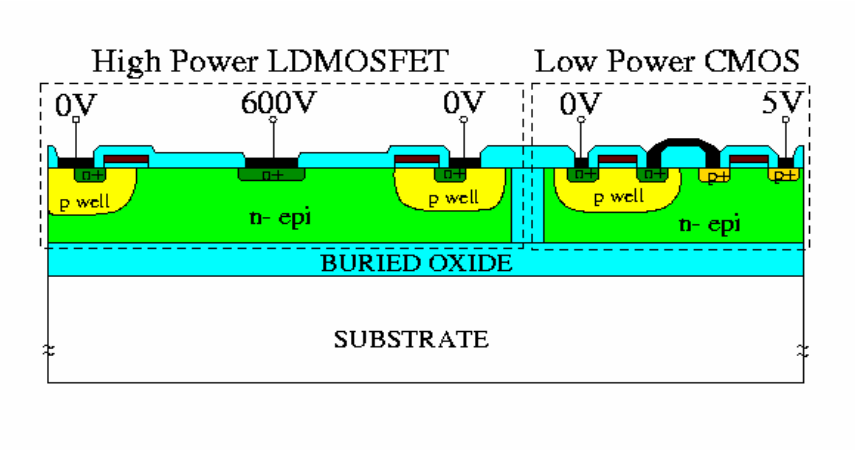
Comparison between the turn-off characteristics for an SOI LIGBT and a JI LIGBT



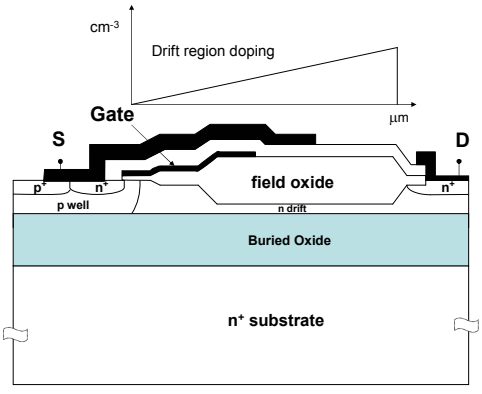
Potential Contour in SOI devices



SOI HVIC cell containing an LDMOSFET switch



Philips Ultra-thin SOI LDMOSFET with linearly doped drift region



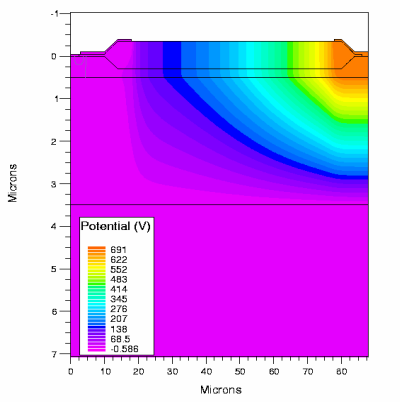
- The device features:

(1) ultra thin SOI layer 0.3-0.5 microns

(2) linearly graded doping profile with the concentration at the source (10^{15} cm^{-3}) much lower than at the drain end (10^{16} cm^{-3}).

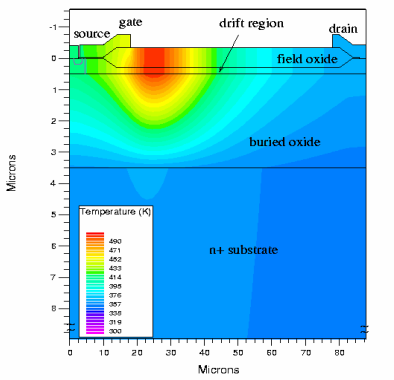
(3) The drift length for 600V is approx. 40 microns and the source extends above the field oxide (25 microns in the drift layer) to allow the formation of an accumulation layer which in the on-state helps to reduce the resistance of the drift layer. Further extension of the gate towards the drain may however degrade the breakdown capability.

Off-state Potential lines & On-state temperature profile in Philips LDMOSFET

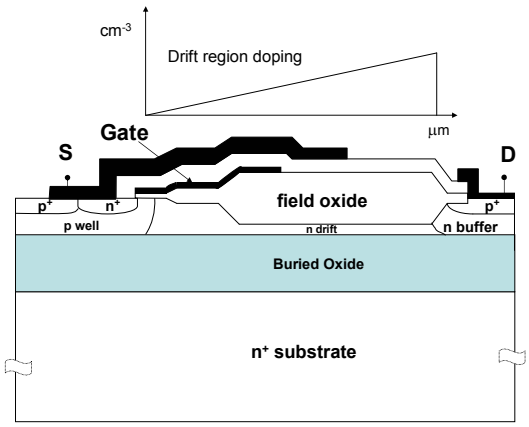


Potential distribution at breakdown

Temperature profile in the on-state

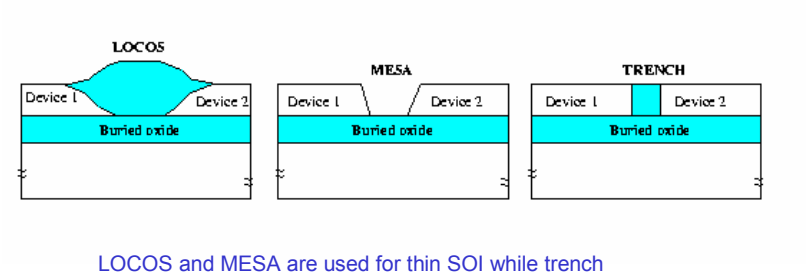


Philips LIGBT with linearly graded profile



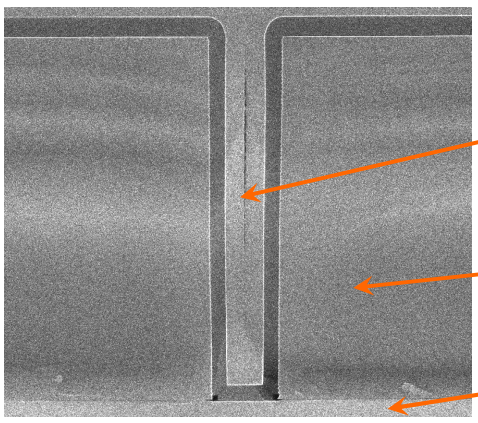
The LIGBT can offer up to 3X increase in the current density compared to a MOSFET and suffers less in the temperature. In the case of Philips linearly graded structure, the n drift region is very thin and therefore there is limited plasma built init. This ensures that the device will switch off considerably faster than a standard IGBT.

Typical Isolations in SOI PICs

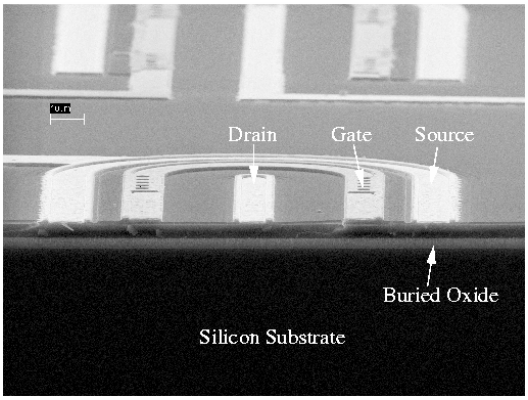


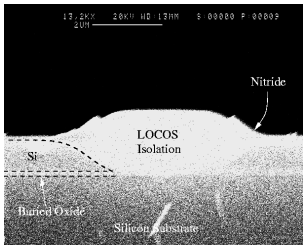
LOCOS and MESA are used for thin SOI while trench isolation is generally used for thicker SOI

Vertical and lateral isolation



SEM photograph of a circular LDMOSFET fabricated at Southampton Microelectronics center

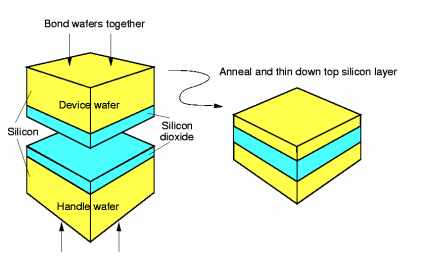




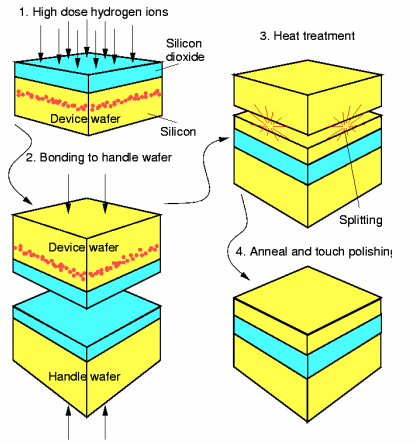
SOI technologies for Power ICs

- Wafer bonding (bonding of two silicon wafers, one with a top oxide)
- SMARTCUT(uses implantation of He and wafer bonding)

SOI - Wafer bonding & SMARTCUT (SOITEC)



Wafer bonding (bonding of tw0 silicon wafers, one with a top oxide)



SMARTCUT

Partial SOI power devices and ICs

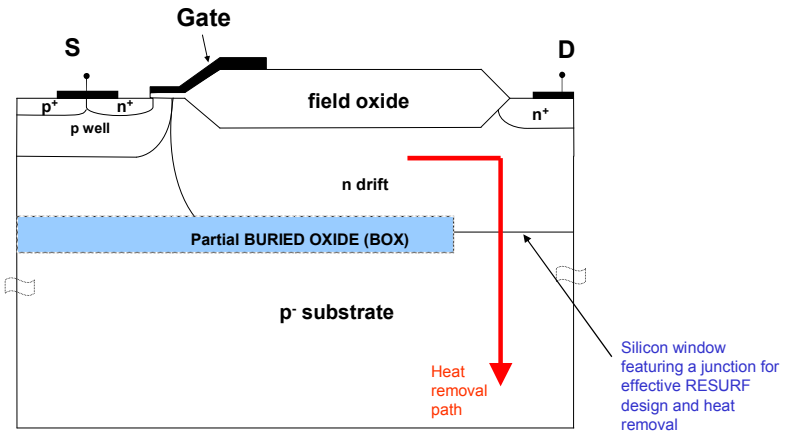
+

- vertical isolation is achieved via buried insulated islands and reverse-biased junctions
- high breakdown voltage (Resurf effect)
- low interference between adjacent devices
- high speed (for both unipolar and bipolar devices)
- reduced self-heating

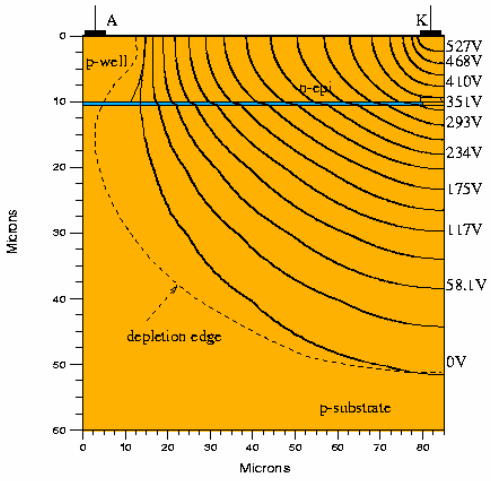
-

- complex fabrication process
- very expensive

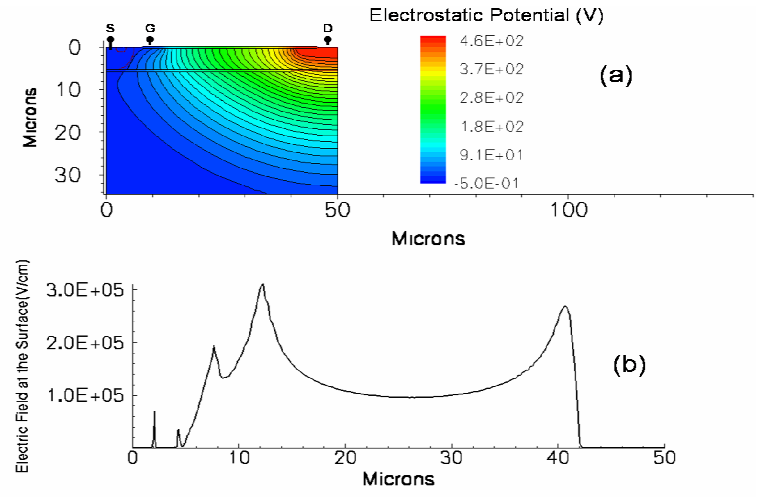
LDMOSFET in partial SOI technology



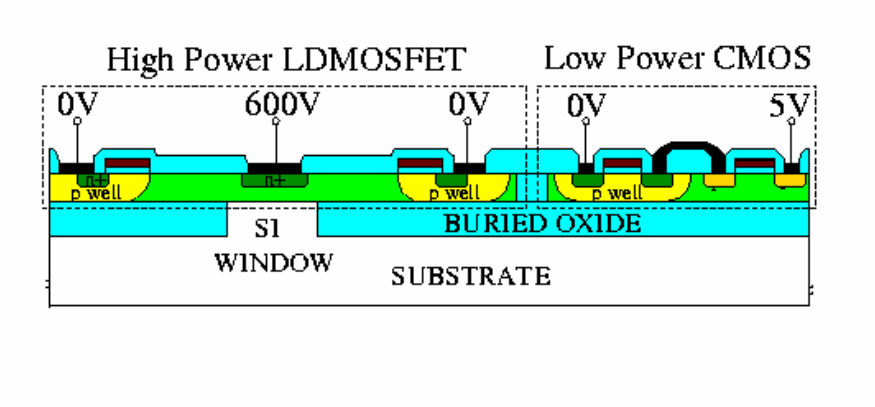
Potential Contour in Partial SOI devices



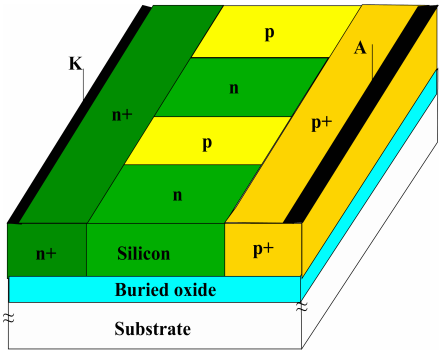
PSOI Potential LINE and RESURF distribution



Partial SOI PIC cell containing an LDMOSFET switch

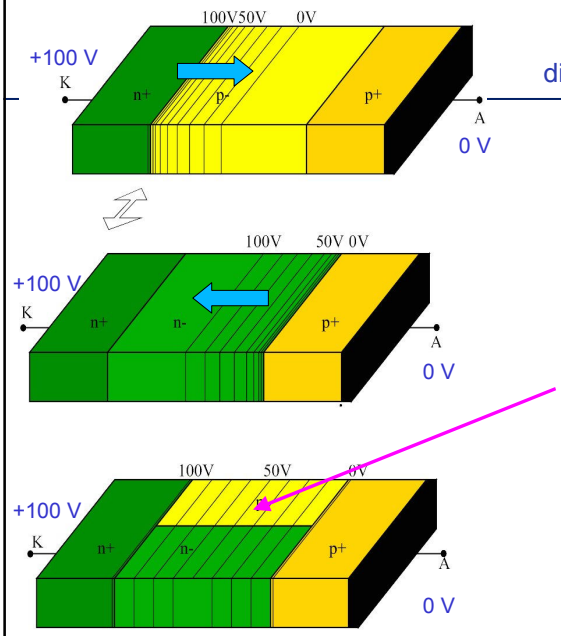


The 3D Resurf junction
(lateral Super-Junction)



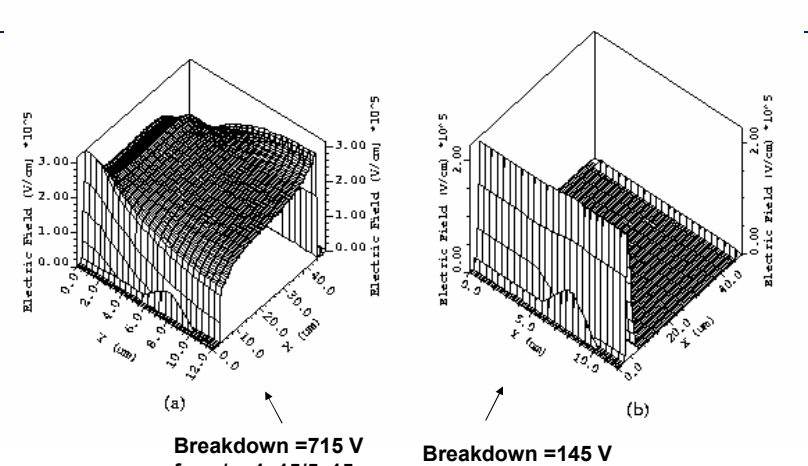
- Enhanced breakdown/on-state trade-off.
- Voltage supported/length of the drift layer : 20V/micron
- simple fabrication process (CMOS compatible)
- can be used in both JI and SOI technologies

Potential distribution in PIN diodes and the 3D Resurf diode



Uniform field/potential distribution

Surface Electric Field distribution



Breakdown =715 V for n/p=1e15/5e15

2D Electric field distribution in the 3D Resurf junction

Breakdown =145 V for n= 1e15

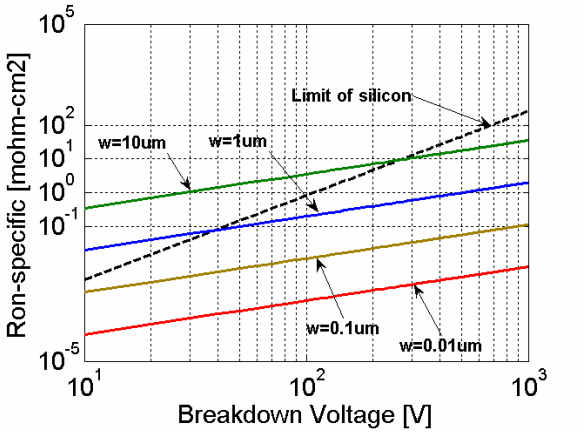
2D Electric field distribution in the classical n+/n/p+ diode

Comparison of Breakdown voltage in the classical diodes and the ideal 3D Resurf (Super-junction) diode

	Doping of drift layer	width of drift layer	lenght of drift layer	Breakdown voltage
Classical p+/n/n+ diode	n=1e15	12 μ m	40 μ m	145 V
Classical p+/p/n+ diode	p=5e15	12 μ m	40 μ m	110 V
3D diode p+/(n,p)/n+	n=1e15 p=5e15	n - 10 μm p - 2 μm	40 μ m	**780 V**

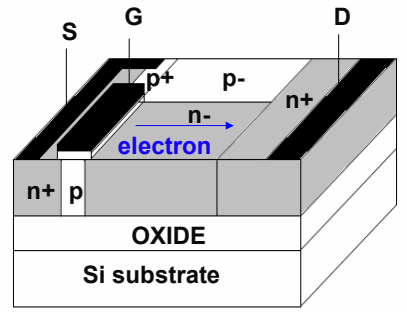
Superjunction – A super-concept for super-low on-state resistance

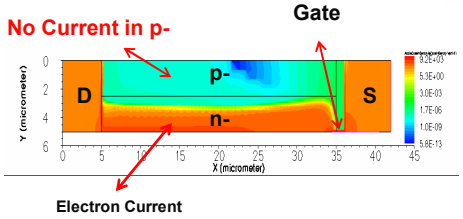
$$R_{specific-drift-superjunction} = \frac{4wV_{BR}}{\mu_n \varepsilon_r \varepsilon_0 \xi_{critical}^2} \approx 1.98 \times 10^{-1} w^{5/4} V_{BR}\Big|_{Silicon-superjunction}$$



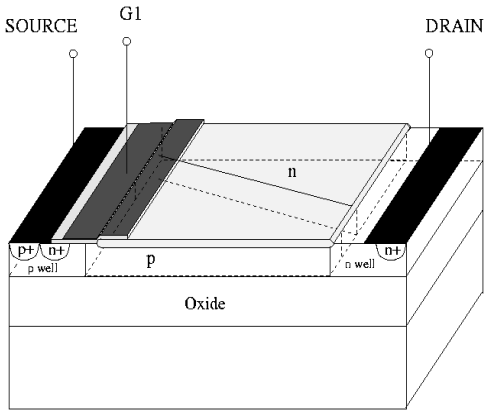
Simulation Results – Single Gate MOSFET

- Unipolar Device
- CMOS compatible
- Can be made in JI or SOI technology
- Easy to fabricate





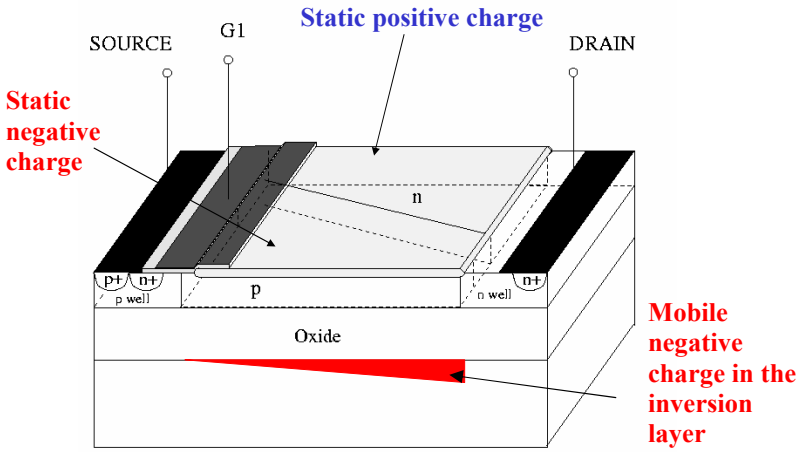
The Unbalanced SuperJunction (Cambridge - Fuji)



The n drift region is uniformly doped but its charge varies linearly from the source end to the drain end to compensate for the charge in the inversion/accumulation layer under the BOX. Thus the doping of the n layer is higher than that of the p layer leading to both enhanced on-state and breakdown performance.

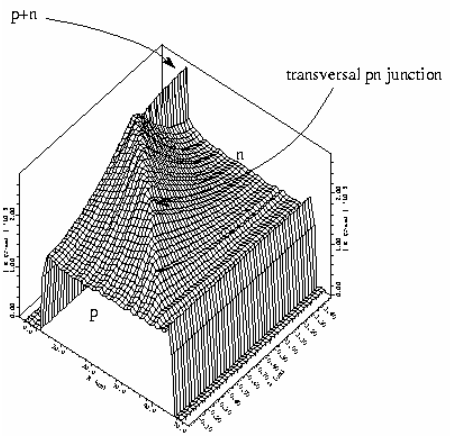
R. Ng, F. Udrea, ISPSD 2001, Japan

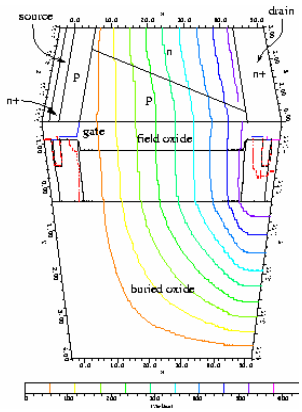
Unbalanced Super-Junction (3D-Resurf) – dynamic Resurf



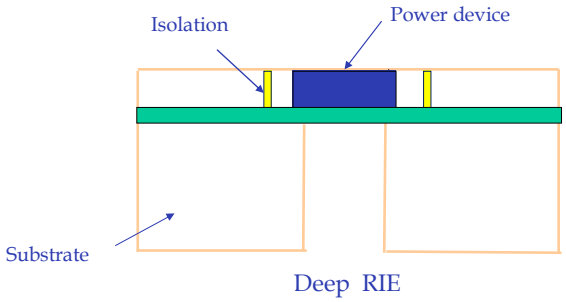
Electric Field and Potential lines

- Electric field and potential distribution ~ 620 volts





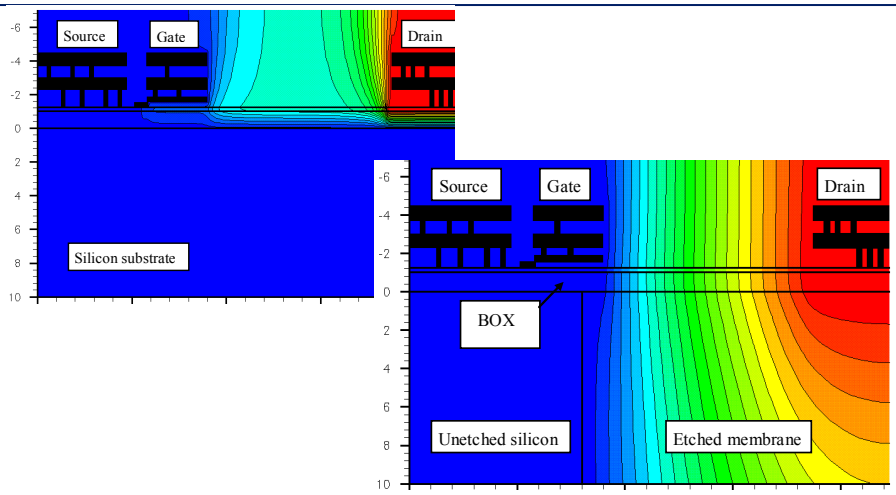
The Membrane Power Device



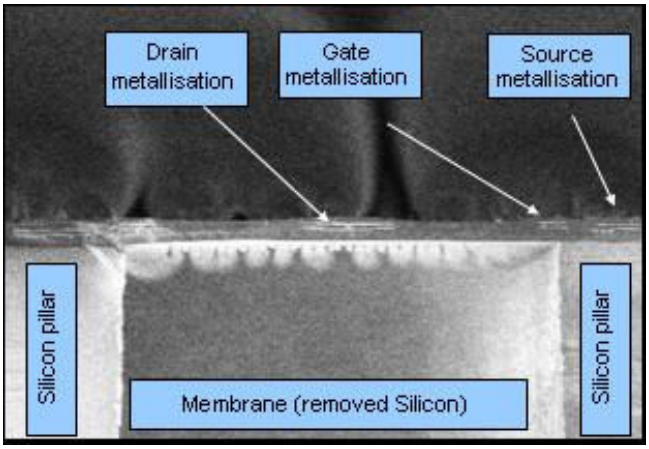
Compared with state-of-the-art power devices for ICs:

- high breakdown ability
- excellent isolation and reduced cross-talk
- very low power losses
- fast switching (increased frequency of operation)

Membrane versus standard SOI

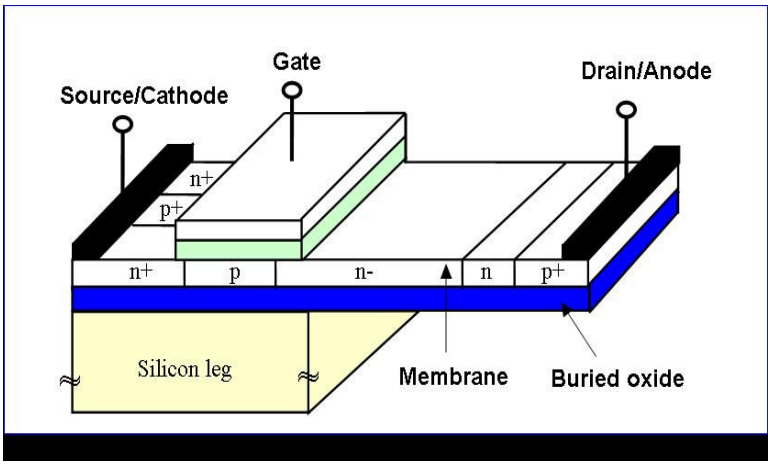


Going to a commercial foundry…

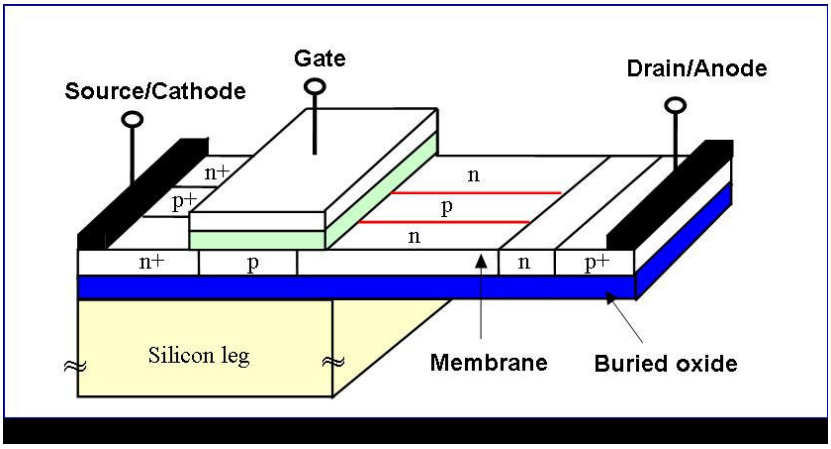


SEM photograph of a CAMSEMI membrane power device.

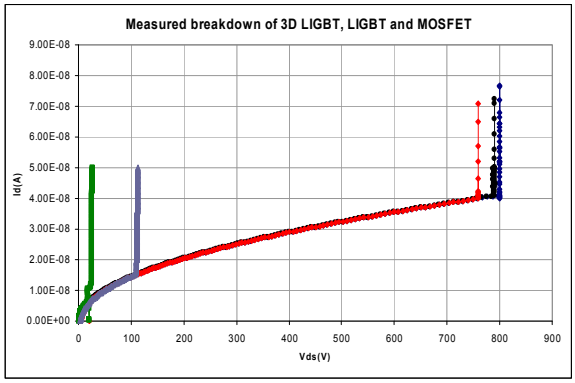
CamSemi LIGBT structure

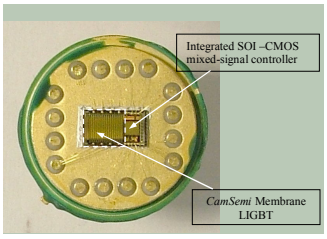


CamSemi superjunction LIGBT structure



Cambridge Semiconductor - CamSemi





LIGBTs vs MOSFET

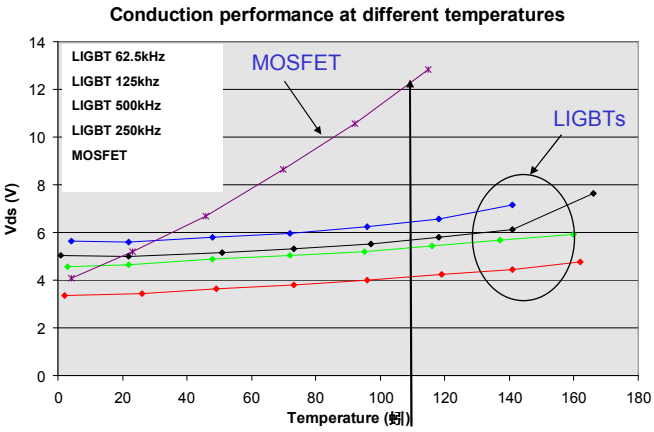
LIGBT can deliver:

-3X current density

-2x reduction in on-state losses

- At 125 C, the on-state resistance of the MOSFET can shoot up by almost 3X

-The LIGBT on-state resistance increases by 20-30%



Typical working temperature

Does this come with a penalty in the switching speed ? – No as Camsemi LIGBT can be faster than a vertical MOS