ISSCC 2018

SESSION 6
Ultra-High-Speed Wireline

A 112Gb/s PAM-4 Transmitter with 3-Tap FFE in 10nm CMOS

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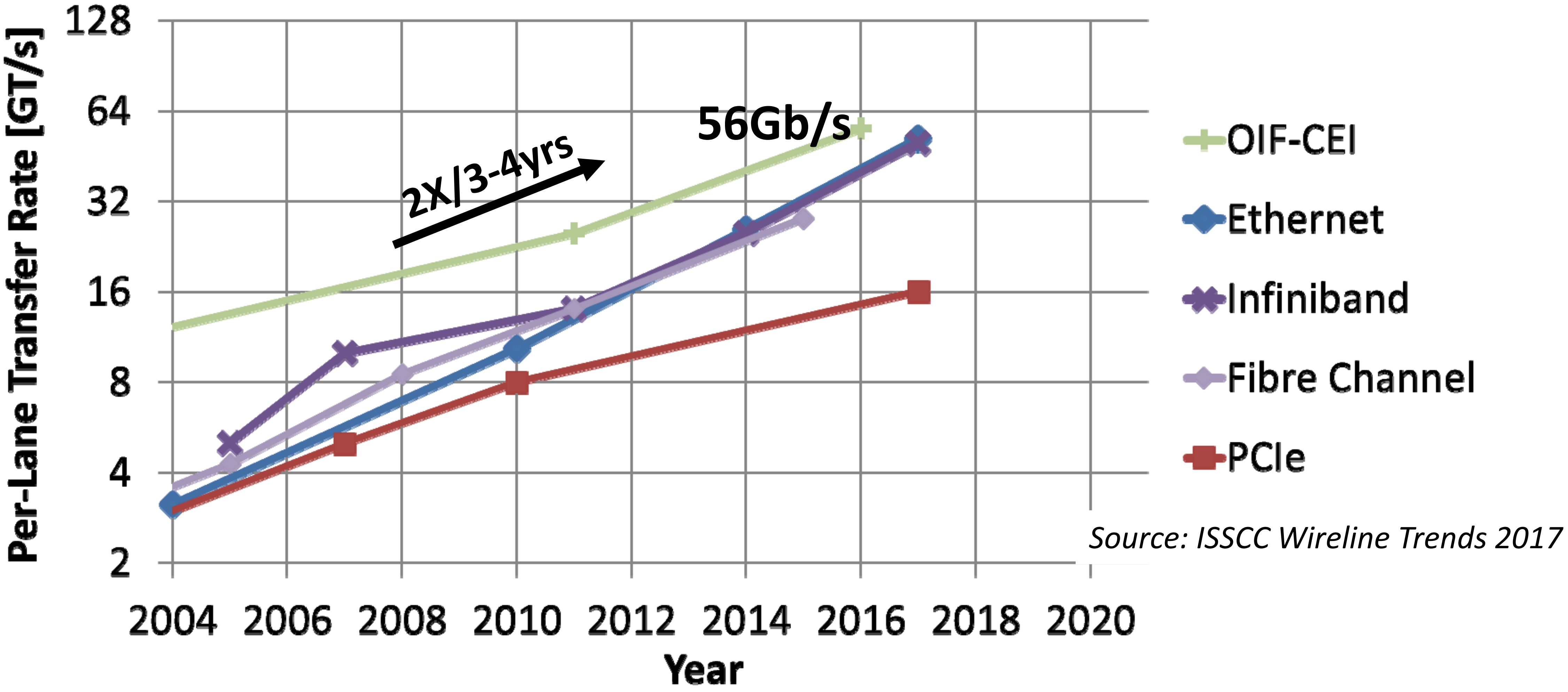
Intel, Hillsboro, OR

Outline

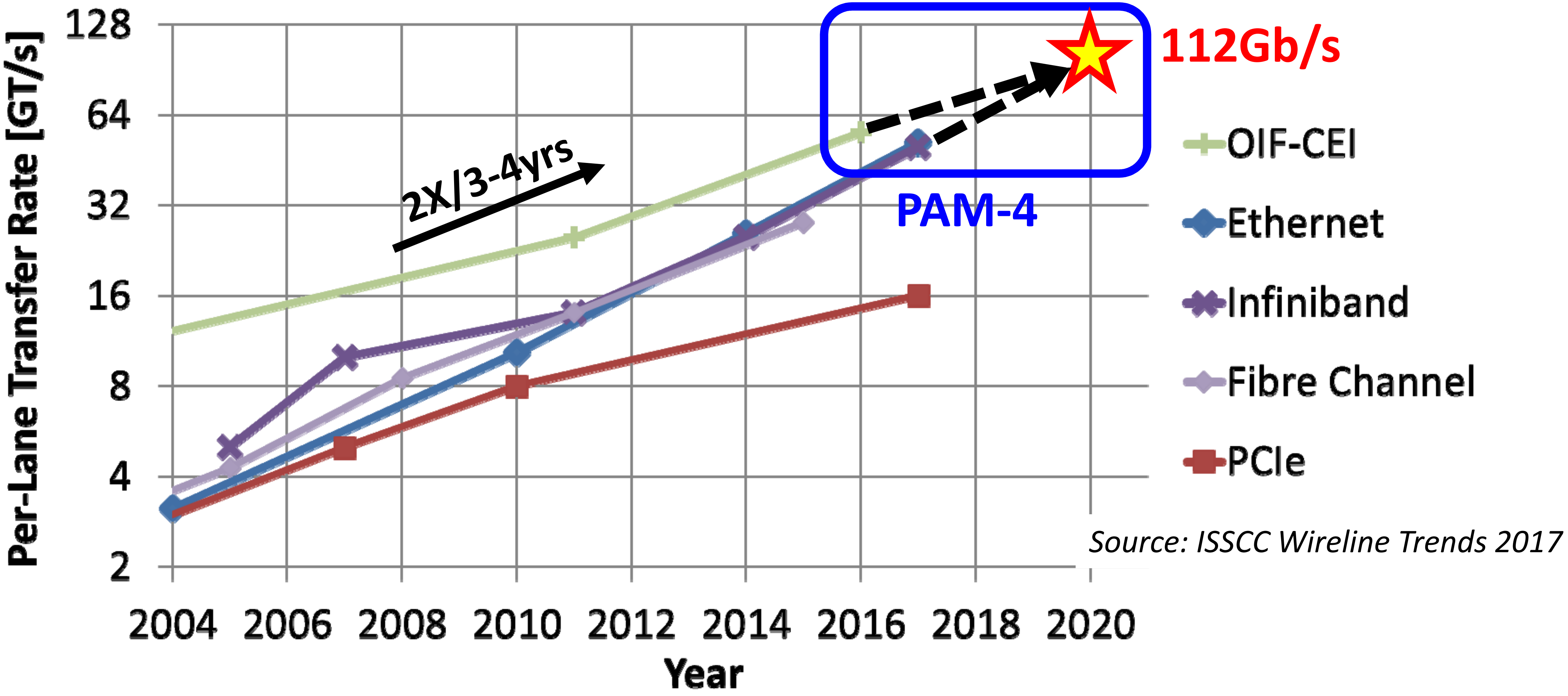
- Background
- TX architecture
- Circuit implementation
- Measurement results
- Summary

Data Rate Scaling for Datacenter



- Per-lane data rate has doubled every 3-4 years

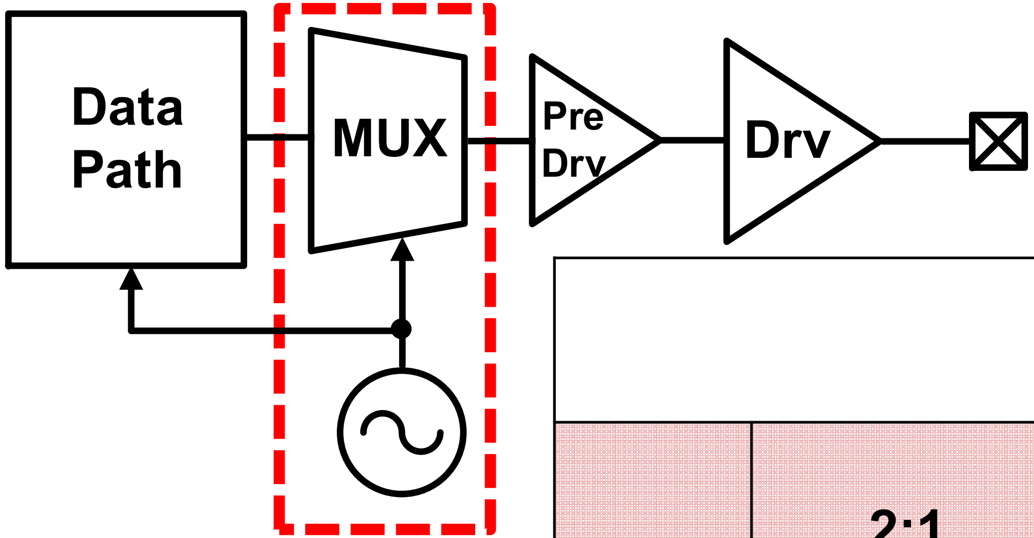
Data Rate Scaling for Datacenter



- Per-lane data rate has doubled every 3-4 years
- PAM-4 has been adopted for long-reach wireline starting at 56Gb/s

TX Architecture Considerations

Clock speed & MUX interleaving rate



PAM-4 112Gb/s (56GS/s)

		Clock Speed	
		14GHz	**28GHz**
MUX Rate	**2:1 Half-rate**	☹ Local clock doubler ☹ Poor timing (1UI window) ☺ Lowest clocking power ☺ Good clock distribution BW	☺ No clock doubler/divider ☹ Poor timing (1UI window) ☹ High clocking power ☹ Clock distribution BW limit
	4:1 Quarter-rate	☹ Quadrature clock gen ☺ Good timing (3UI window) ☺ Low clocking power ☺ Good clock distribution BW	☹ Quadrature divider ☺ Good timing (3UI window) ☹ High clocking power ☹ Clock distribution BW limit

TX Architecture Considerations

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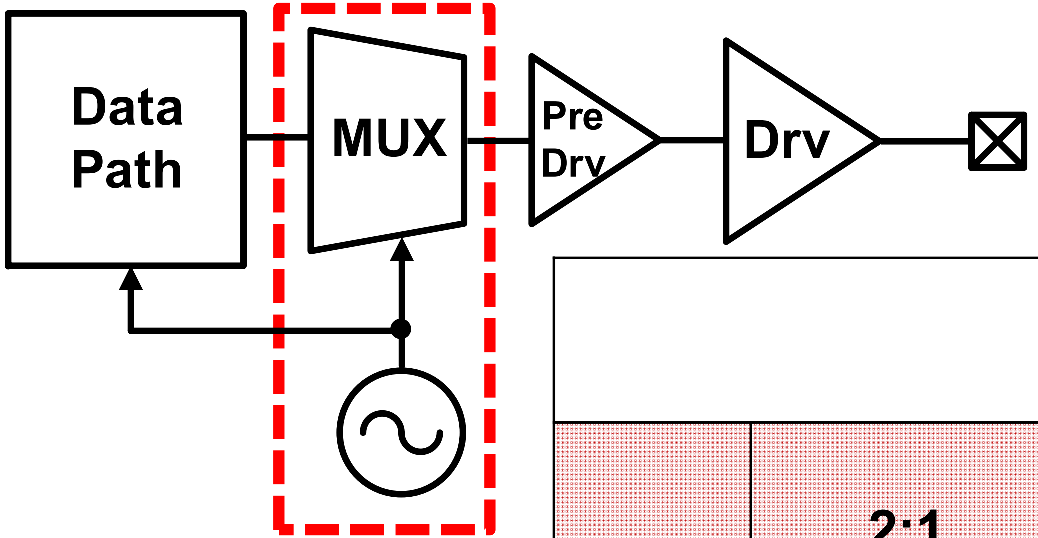

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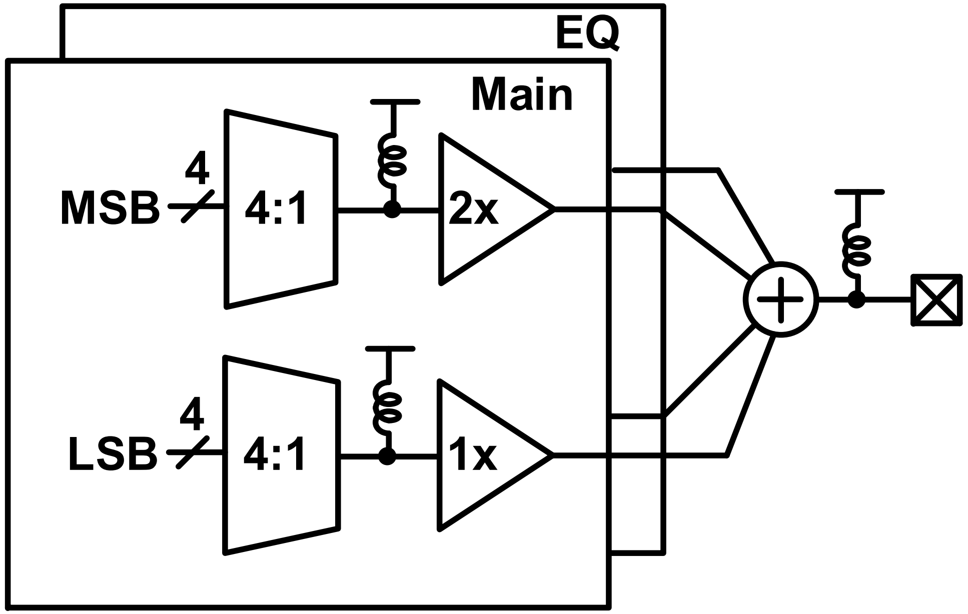
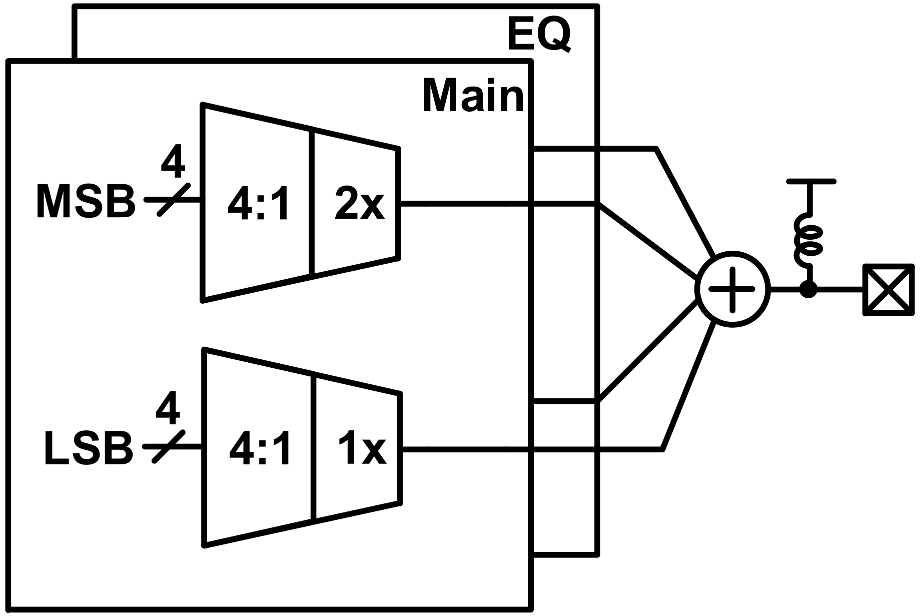
TX Architecture Considerations

At pre-pad ← **Data serialization** → At pad



- ☺ Low clock load
- ☹ Pre-driver power
- ☹ High ISI
- ☹ Large area



- ☹ High clock load
- ☺ No pre-driver power
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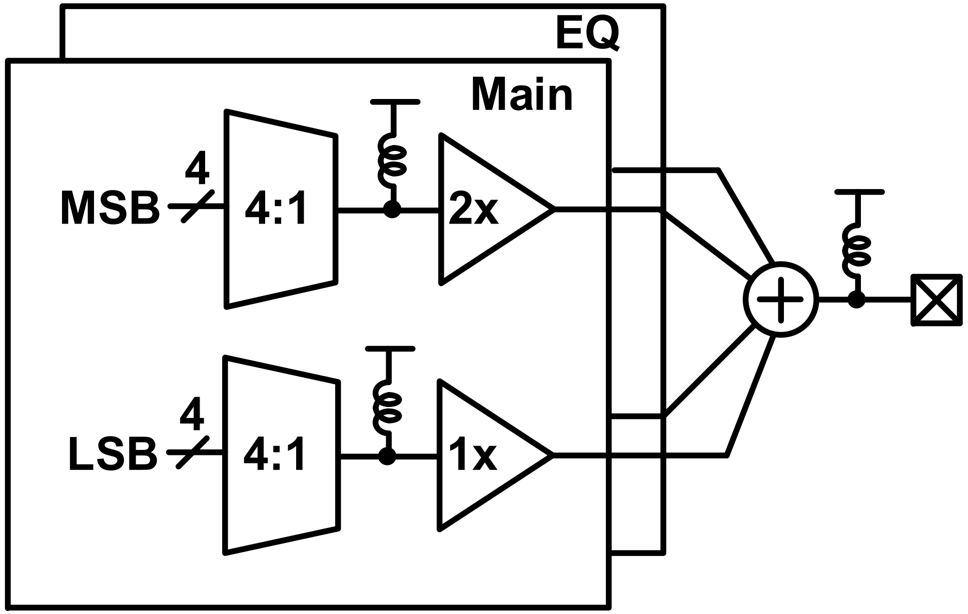
TX Architecture Considerations

At pre-pad ⟵ **Data serialization** ⟶ At pad



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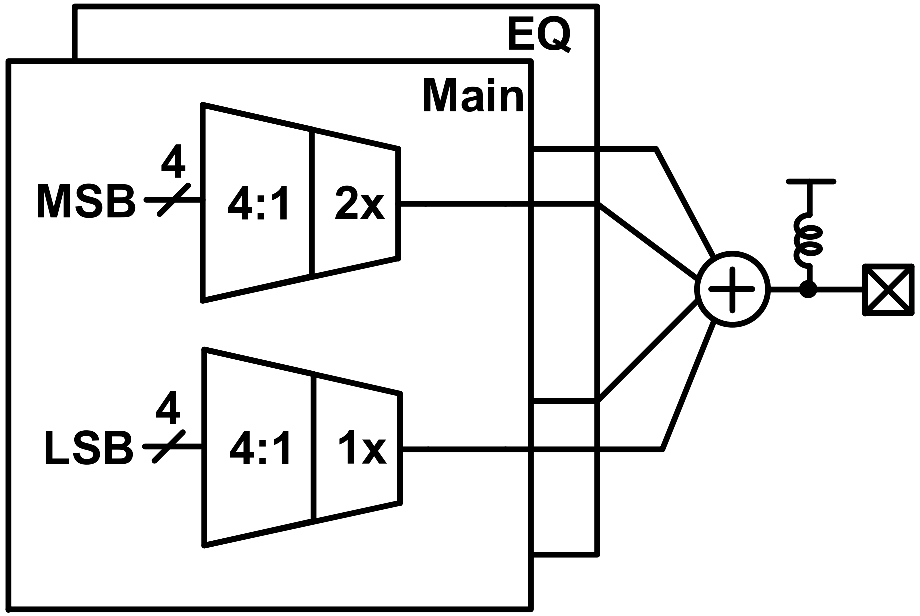

☹ High clock load
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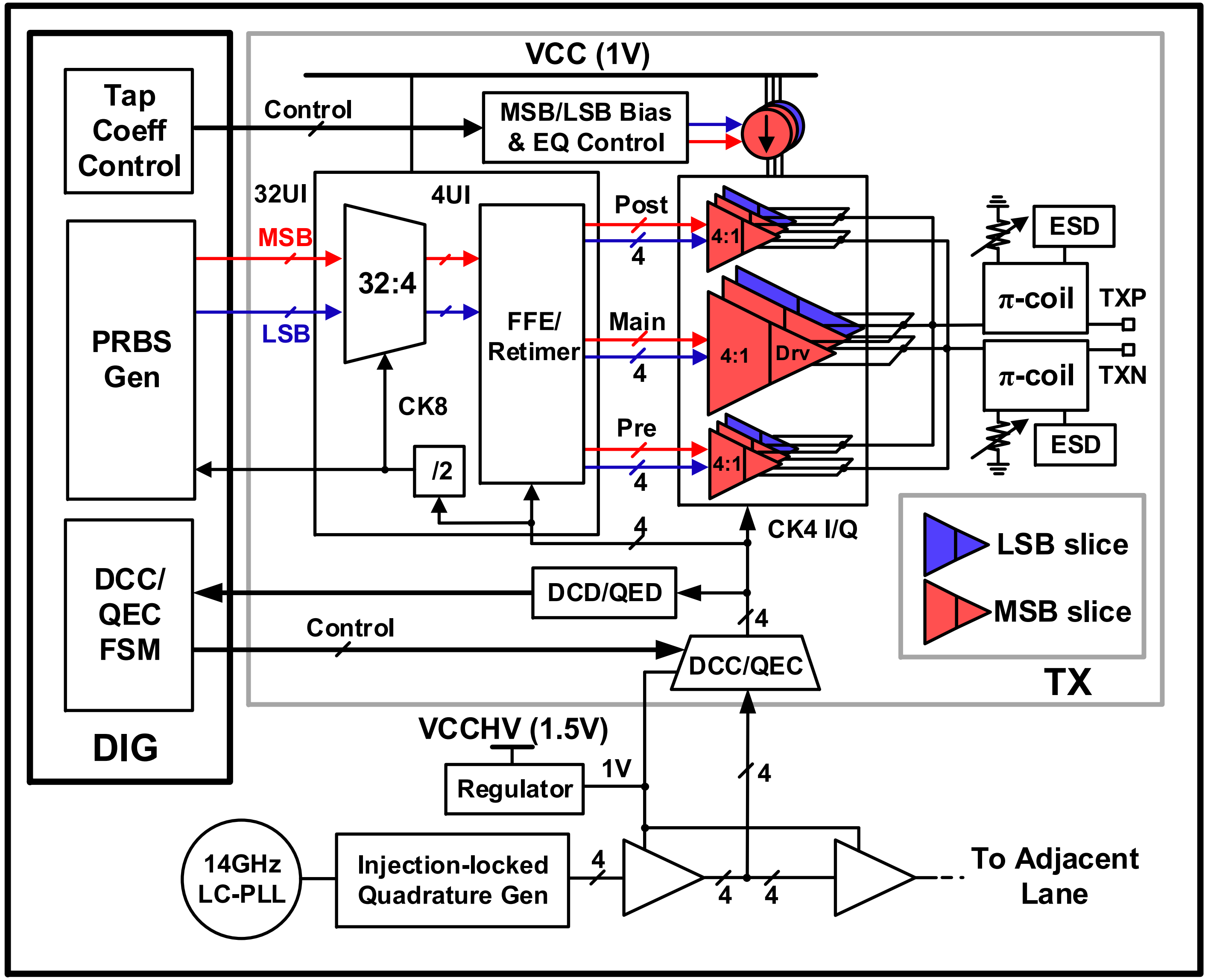
NRZ/PAM-4 Dual-Mode 112Gb/s TX



- Intel 10nm technology
- Quarter-rate architecture
- 3-tap FFE
- Regulated 14GHz clocking
- Merged 4-to-1 MUX/driver
- π-coil for pad BW extension
- 250V-CDM/1kV-HBM ESD
- 2.07pJ/bit energy efficiency (PAM-4 112Gb/s)

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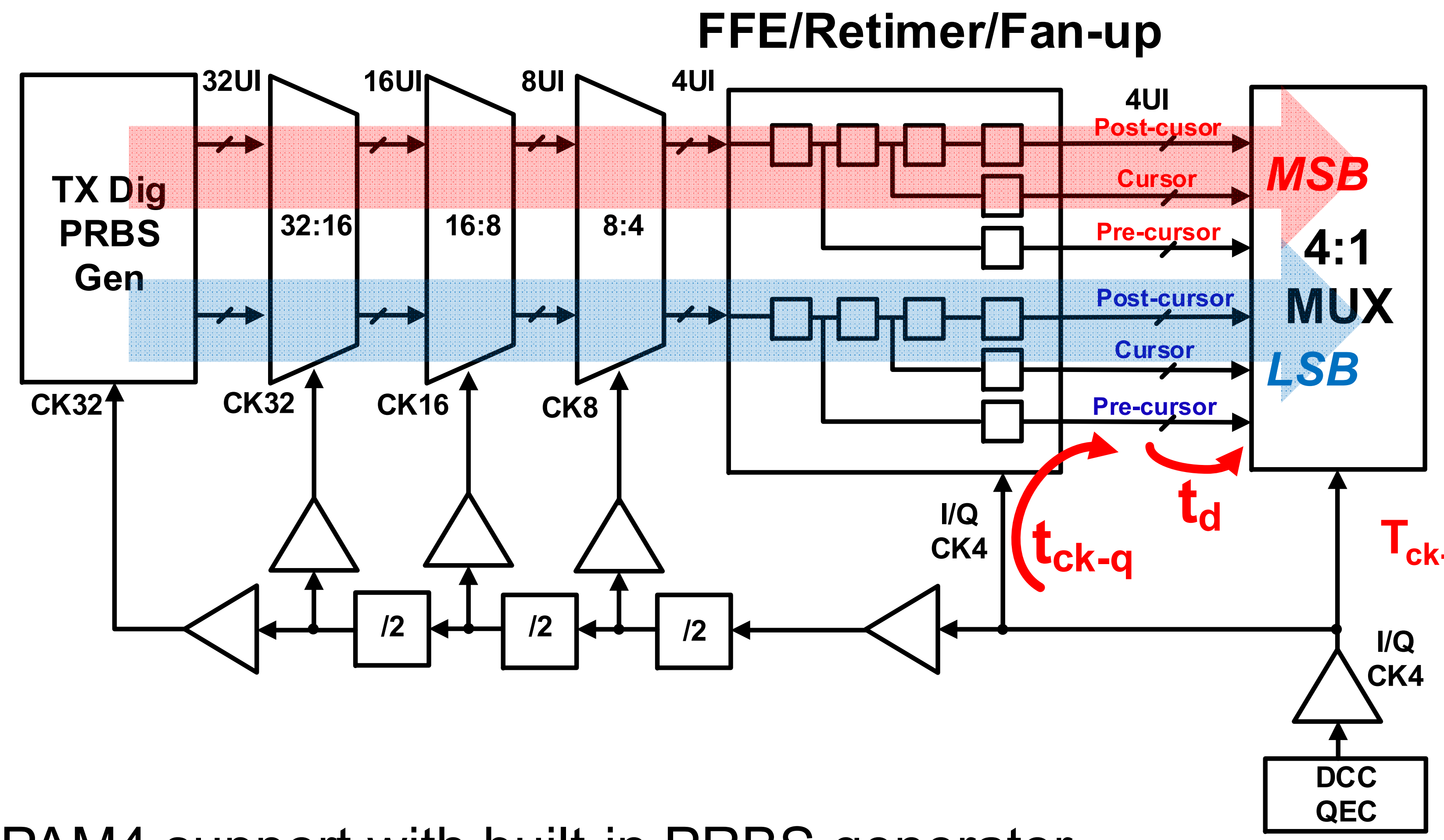
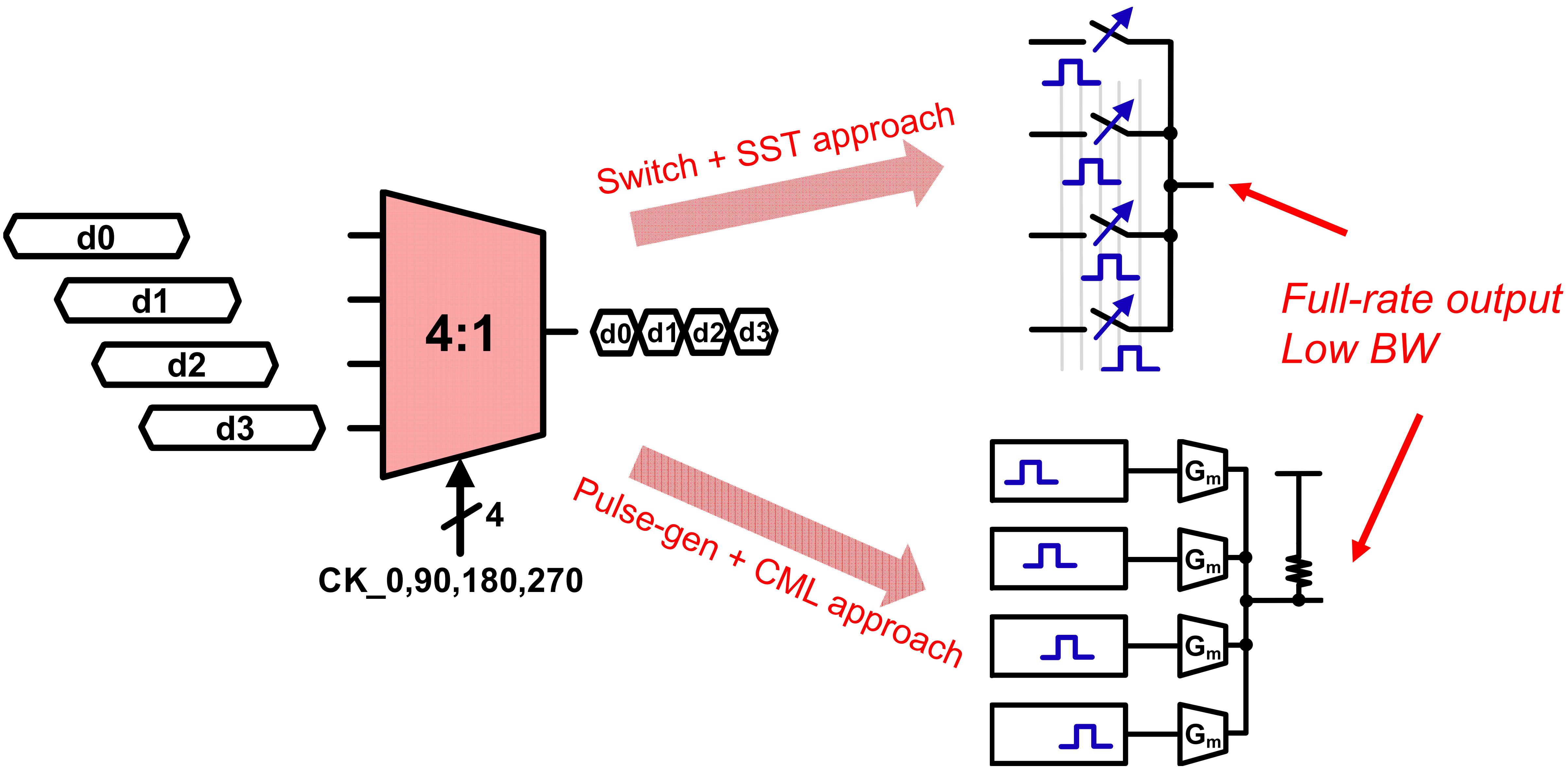
Data-Path



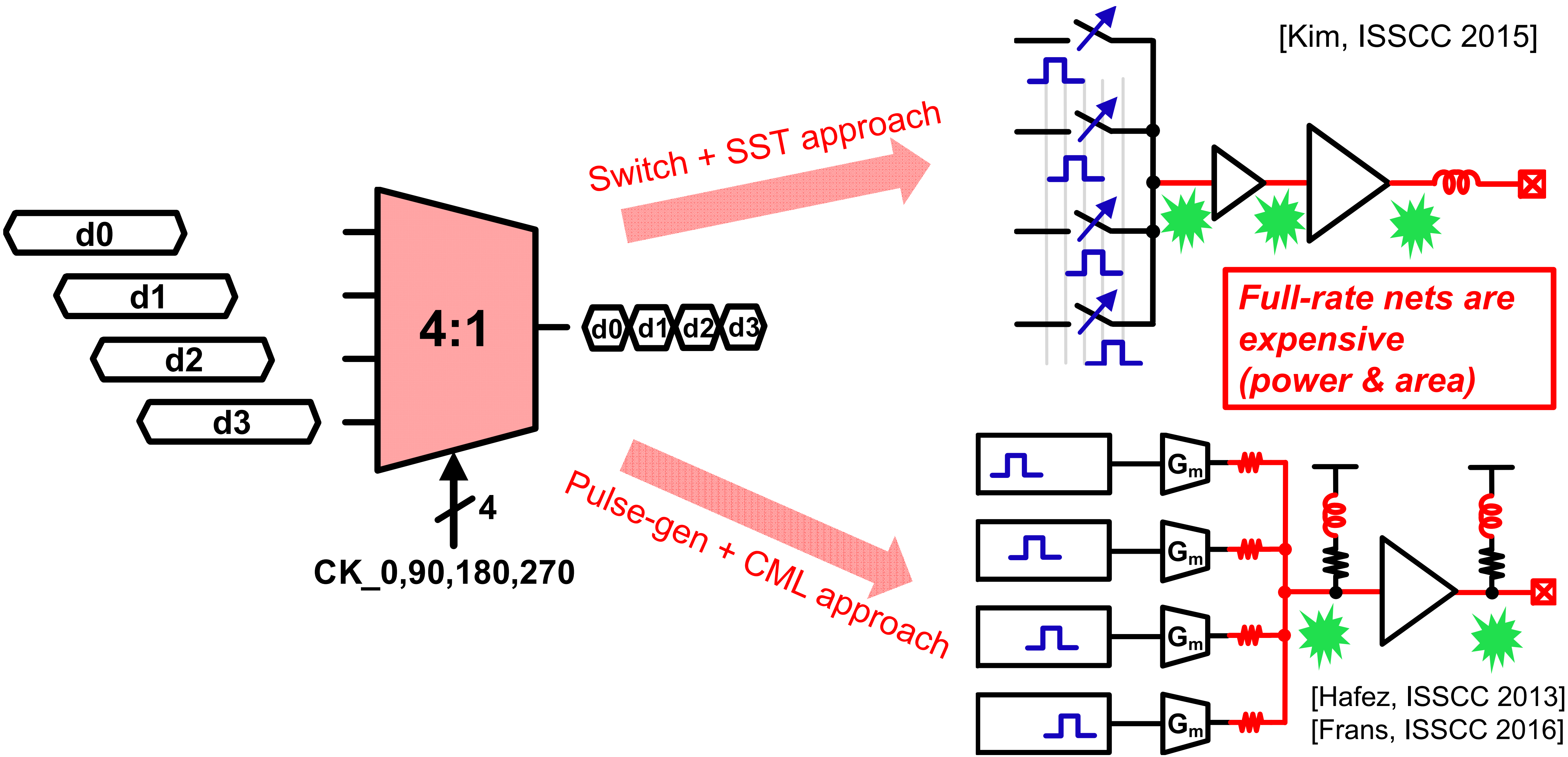
$T_{ck\text{-}q} + t_d + t_{setup} < 3UI$

- NRZ/PAM4 support with built-in PRBS generator
- 32:4 serializer with dedicated MSB/LSB data-paths
- 3-tap FFE and fan-up/retimer

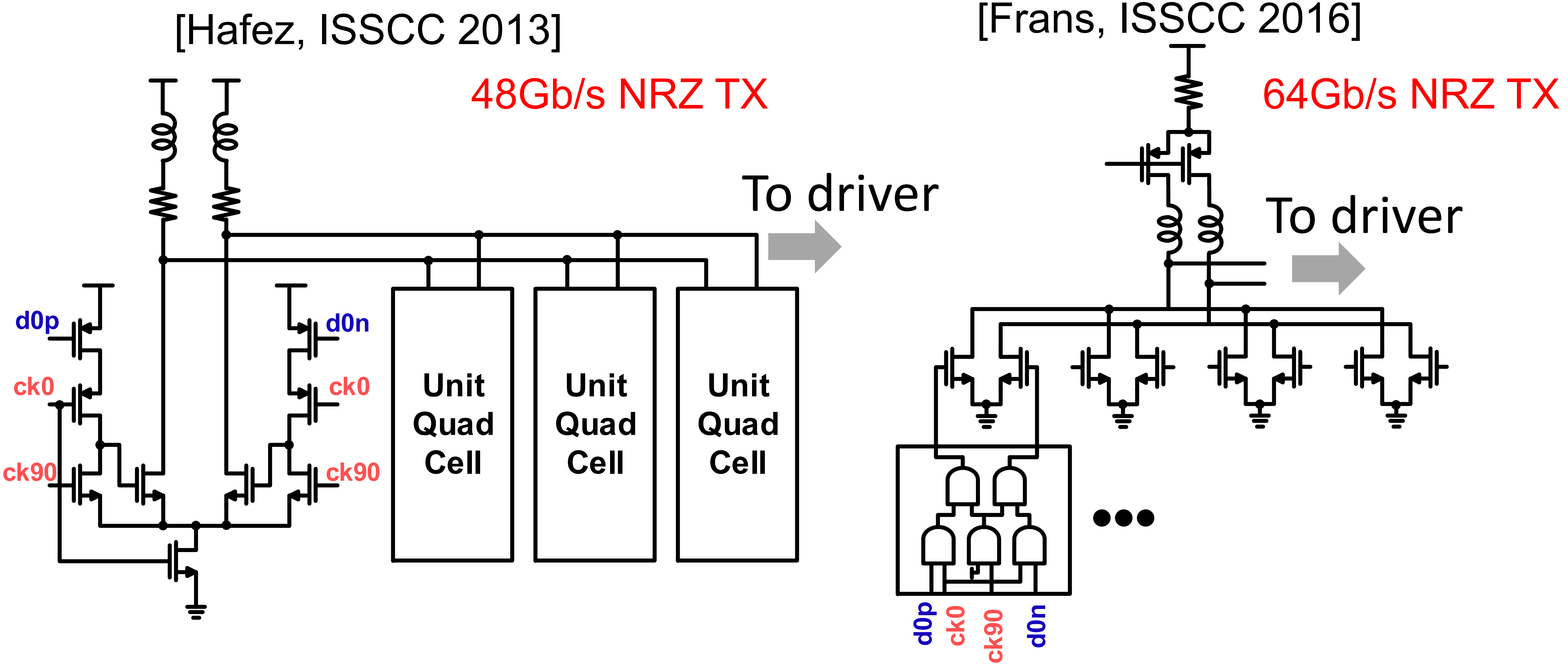
4:1 Data Serialization Approaches



4:1 Data Serialization Approaches

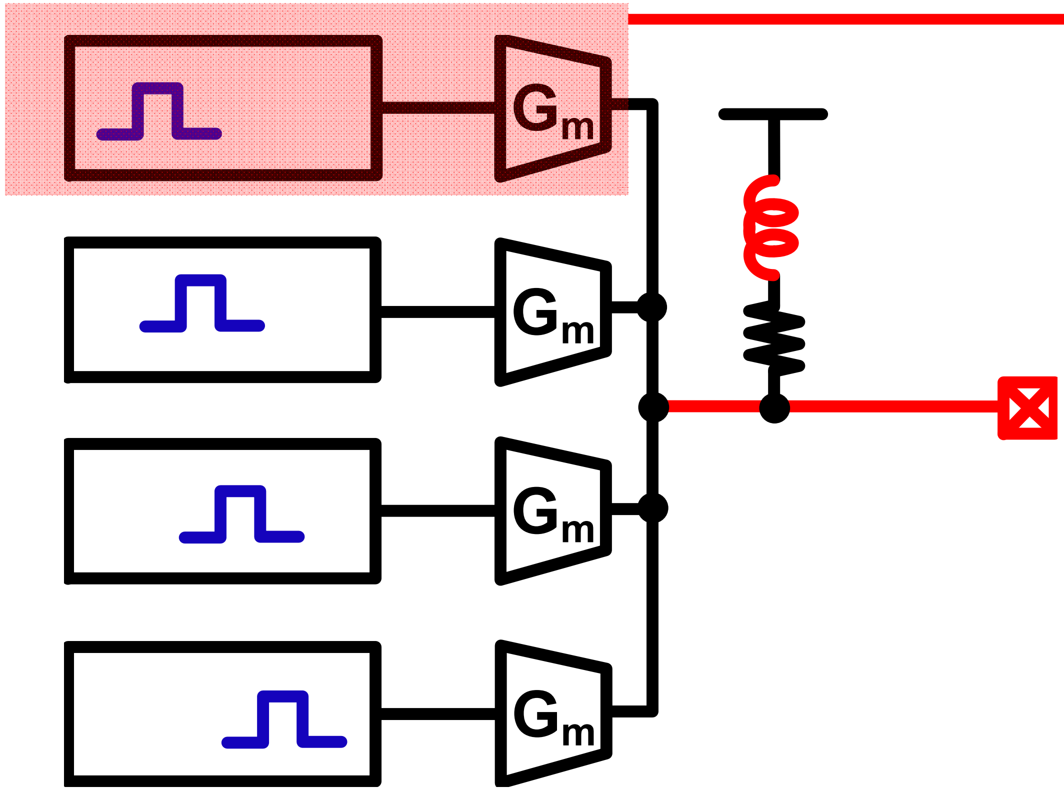


Pulse Generator and CML Summer: Prior Arts



- Good designs as a pre-driver, but not as a output stage

Proposed Approach of 4:1 Data Serialization



- 1-UI pulse gen + CML config
- Simple & compact topology
- Optimized BW & power

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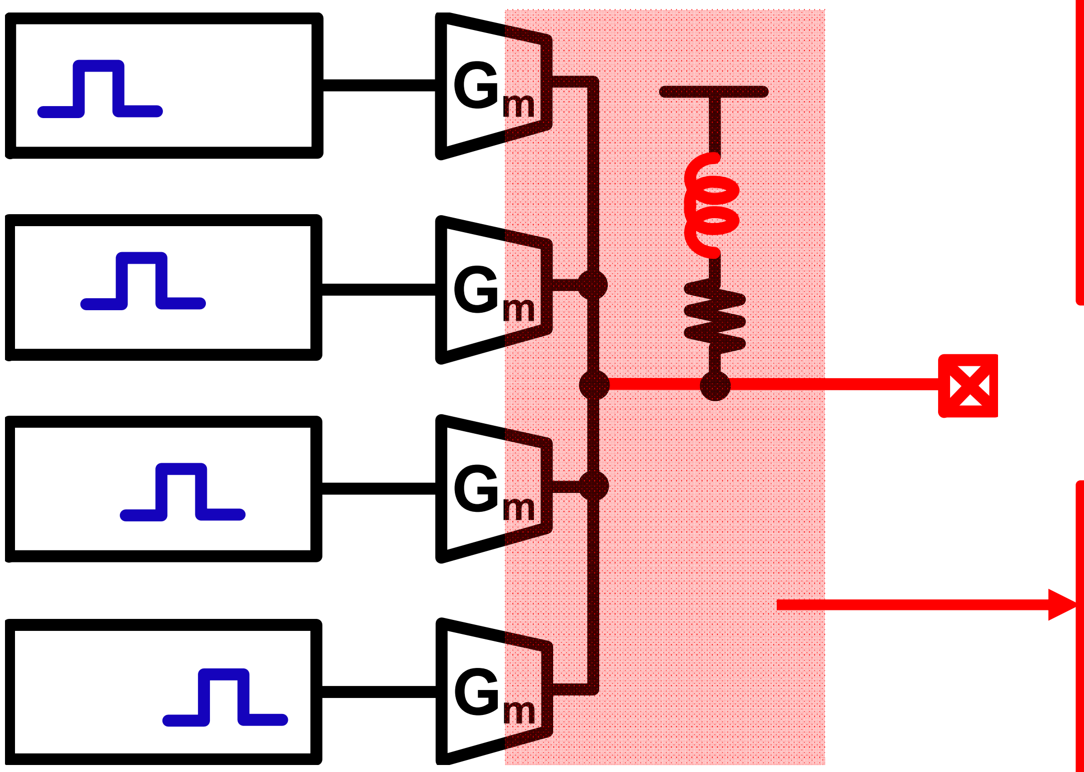
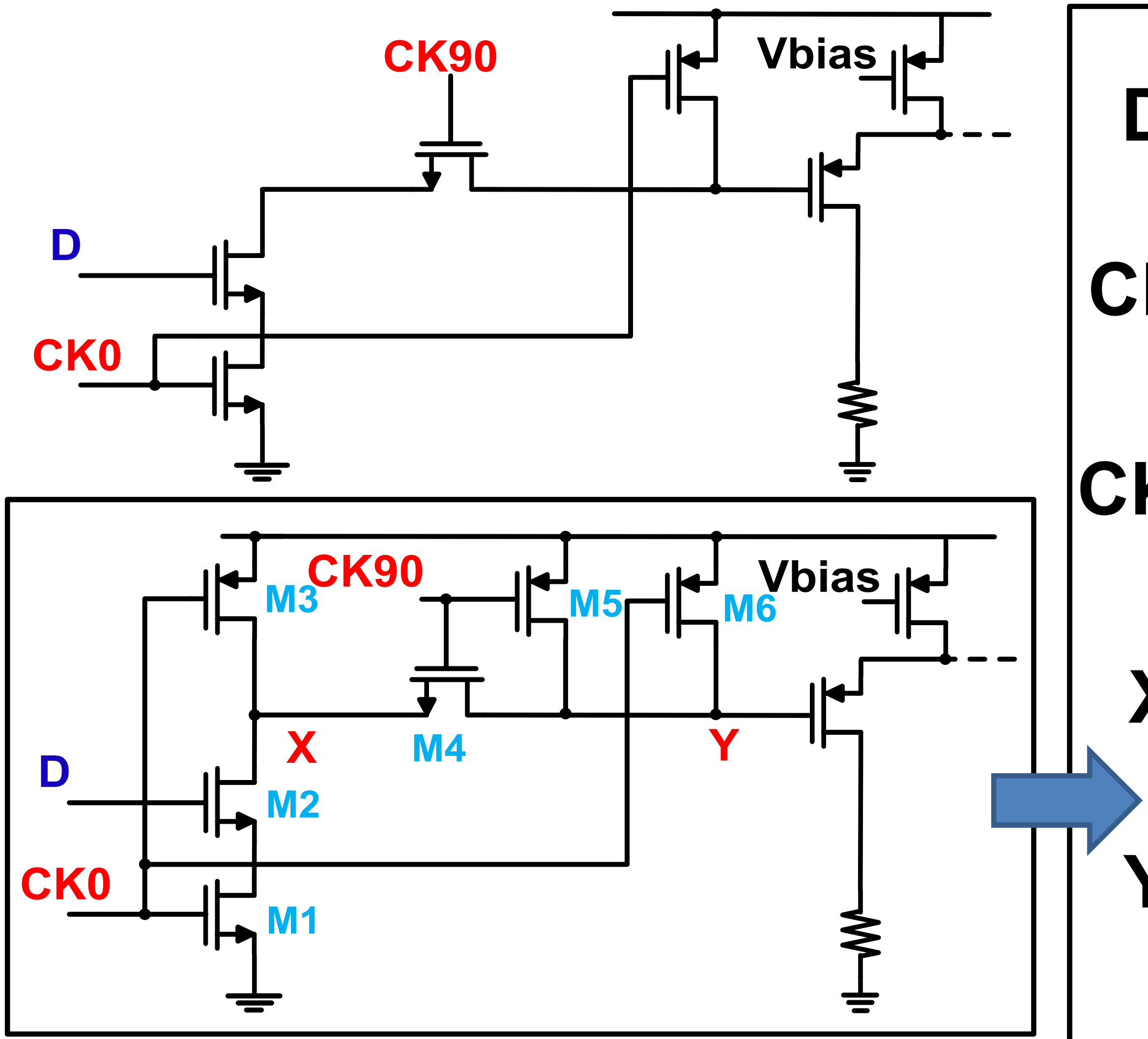
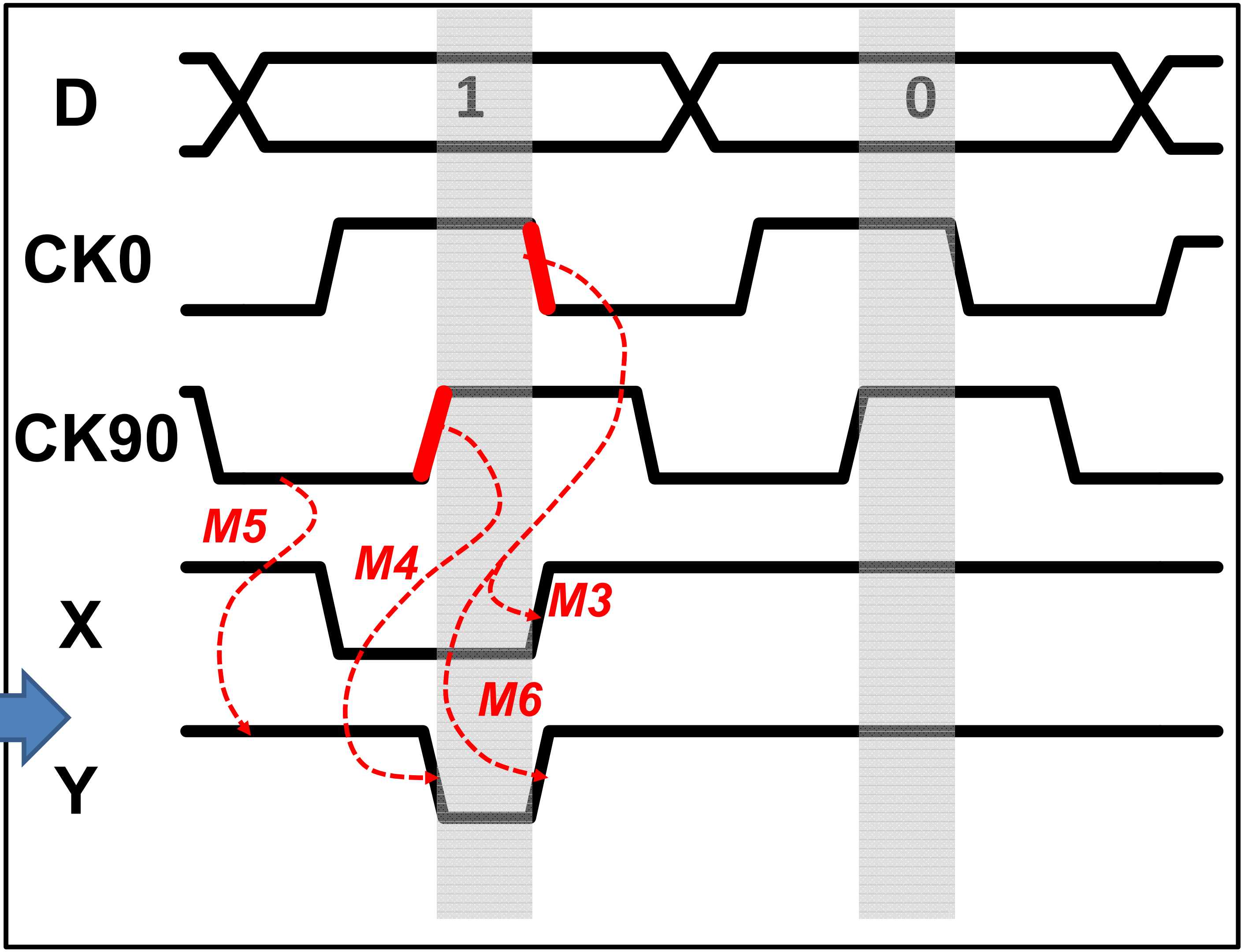


- 1-UI pulse gen + CML config.
- Simple & compact topology
- Optimized BW & power

- No unwanted series R at output
- Strong enough to drive pad
- Only one full-rate net at pad

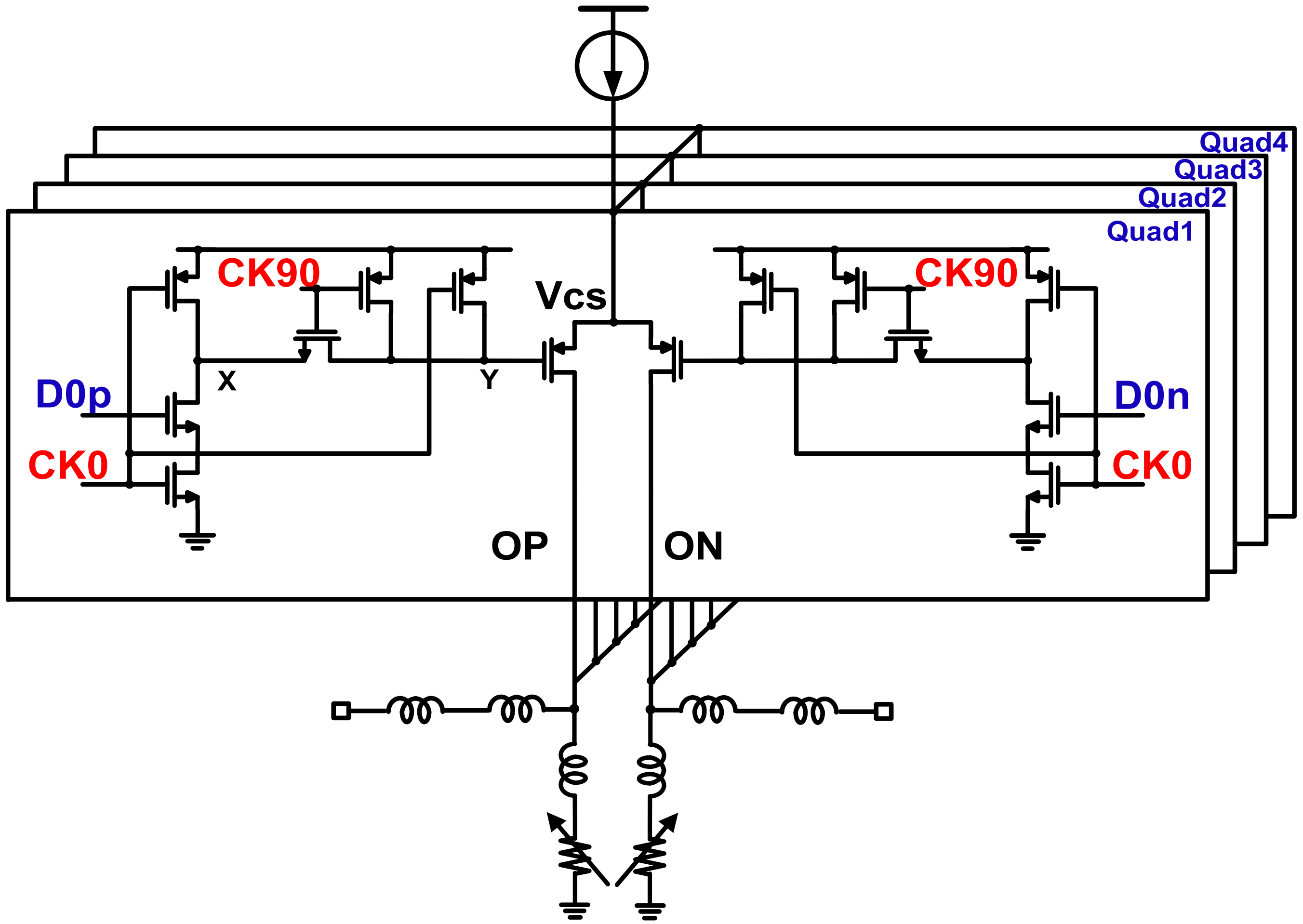
Proposed Pulse Generator and CML Combo

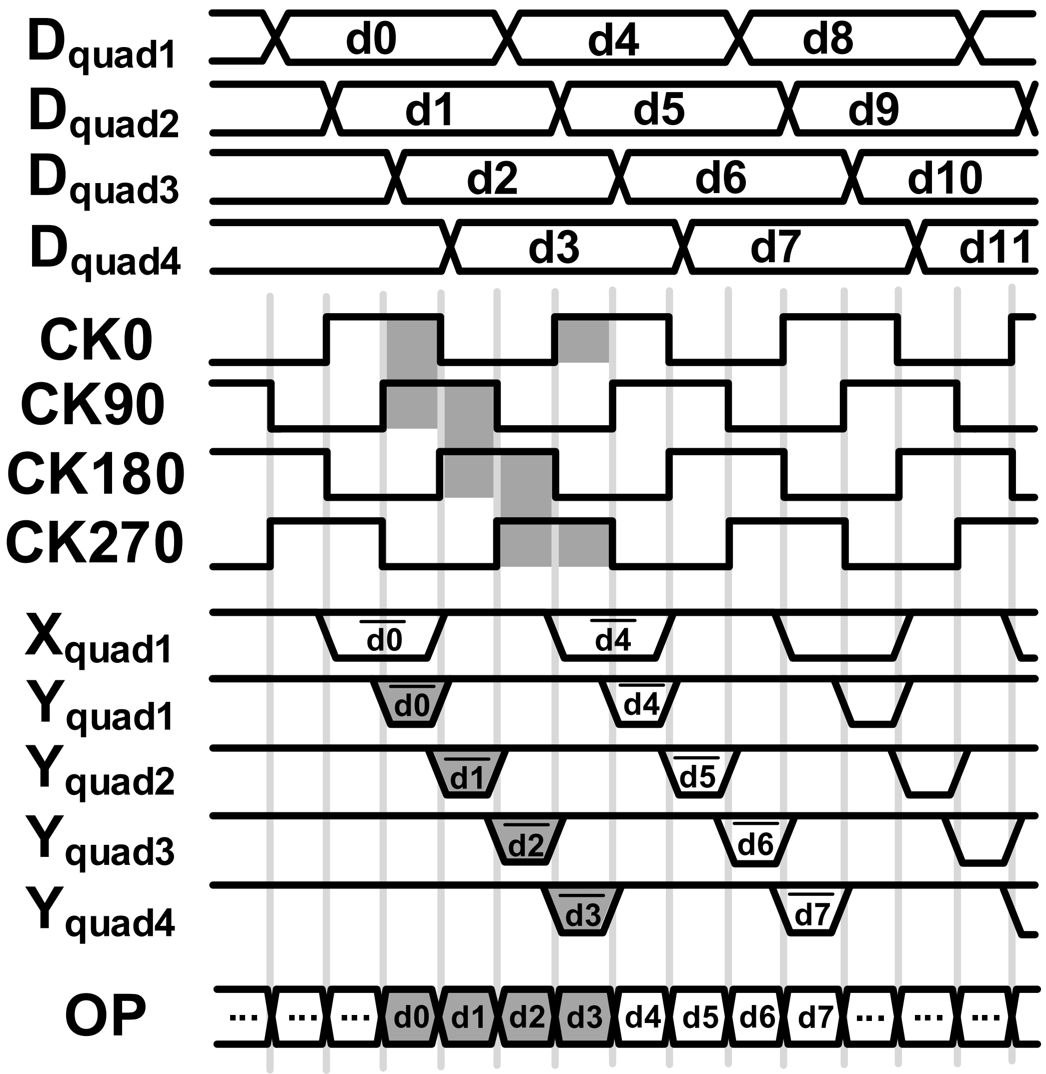




Key devices: M1, M2, M4, M6
M3 & M5 improve ISI

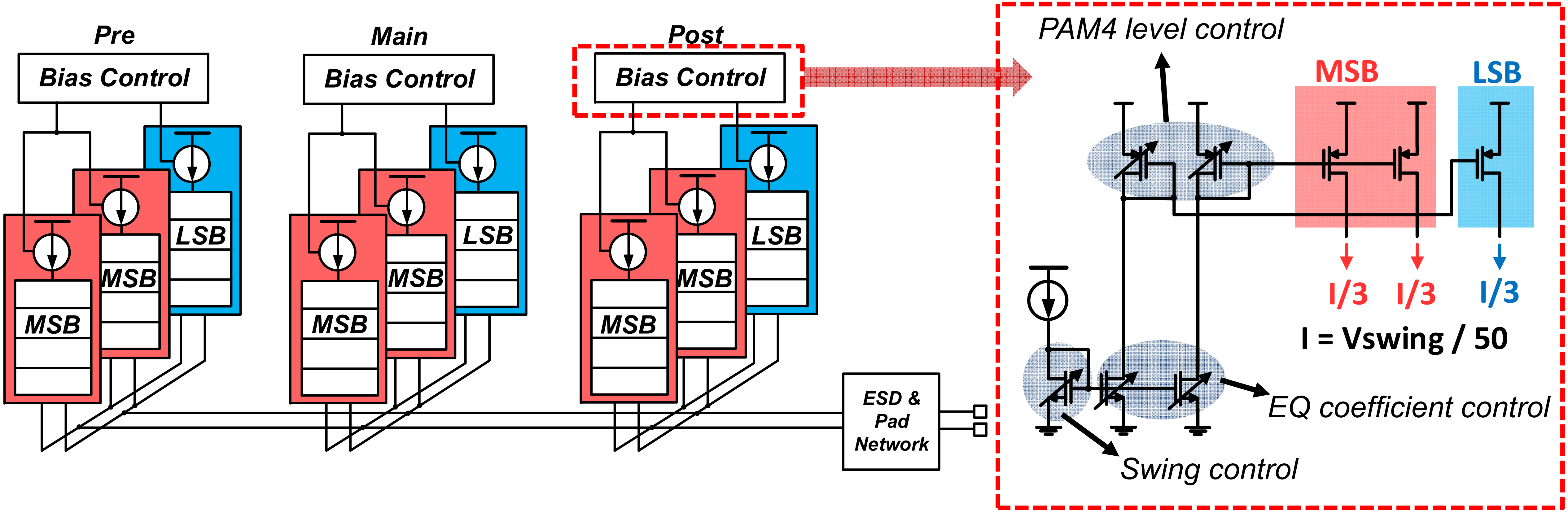
Proposed 4:1 MUX & Driver Combo





- Inductor is used only at output pad
- ISI at pad is 600fs in the worst case simulation

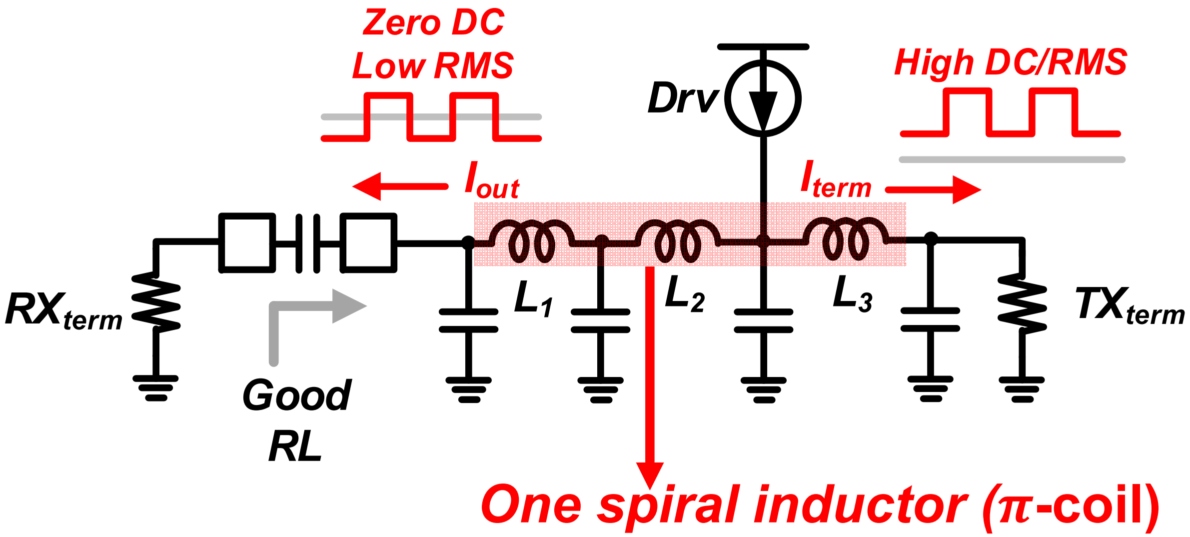
Full Driver and Bias Circuit



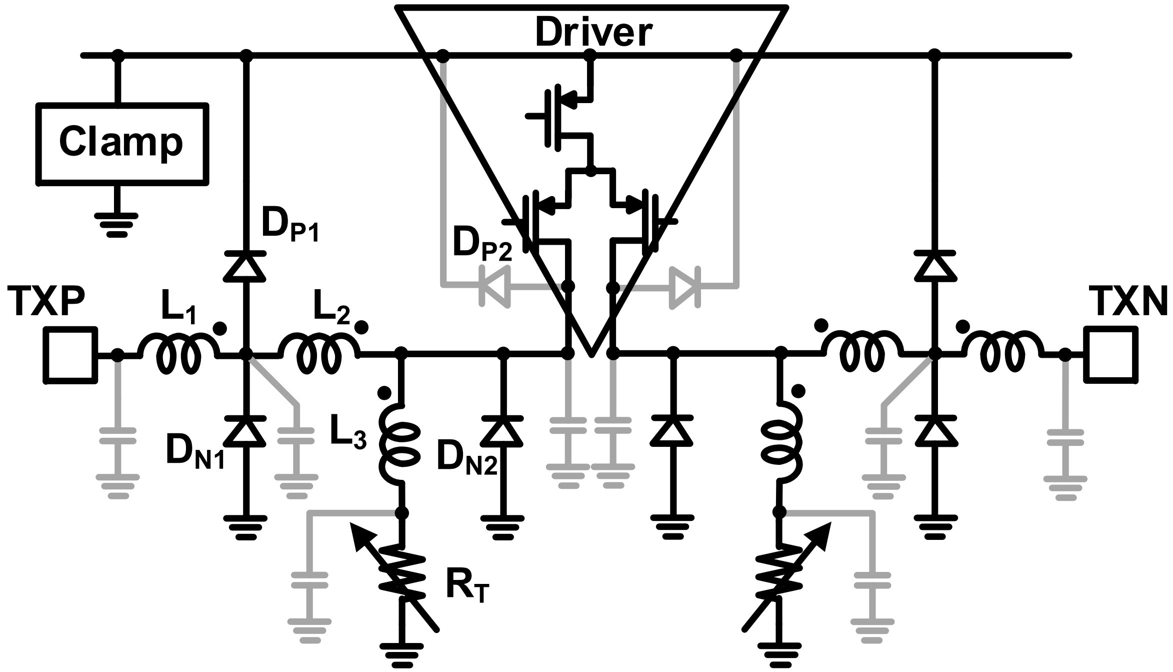
- Driver is segmented to support NRZ and PAM4 modulations
  → Separate input data paths feed driver slices
- IDAC control: driver swing (3b), EQ coefficient (5b), PAM4 level (4b)

Output Pad Network

Proposed π-coil network



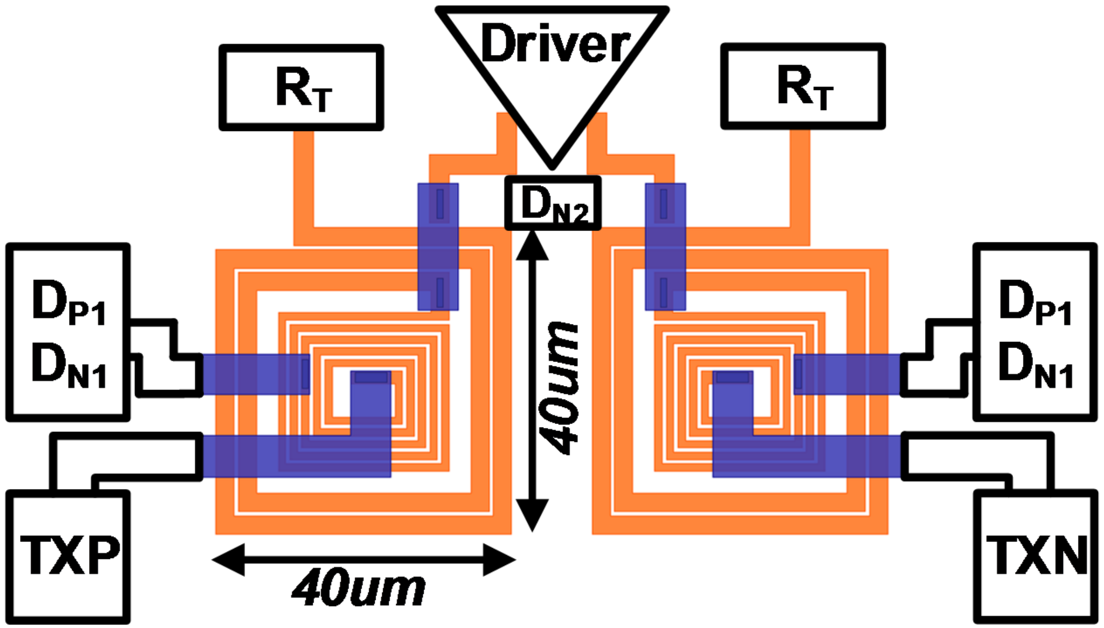
Full output pad network



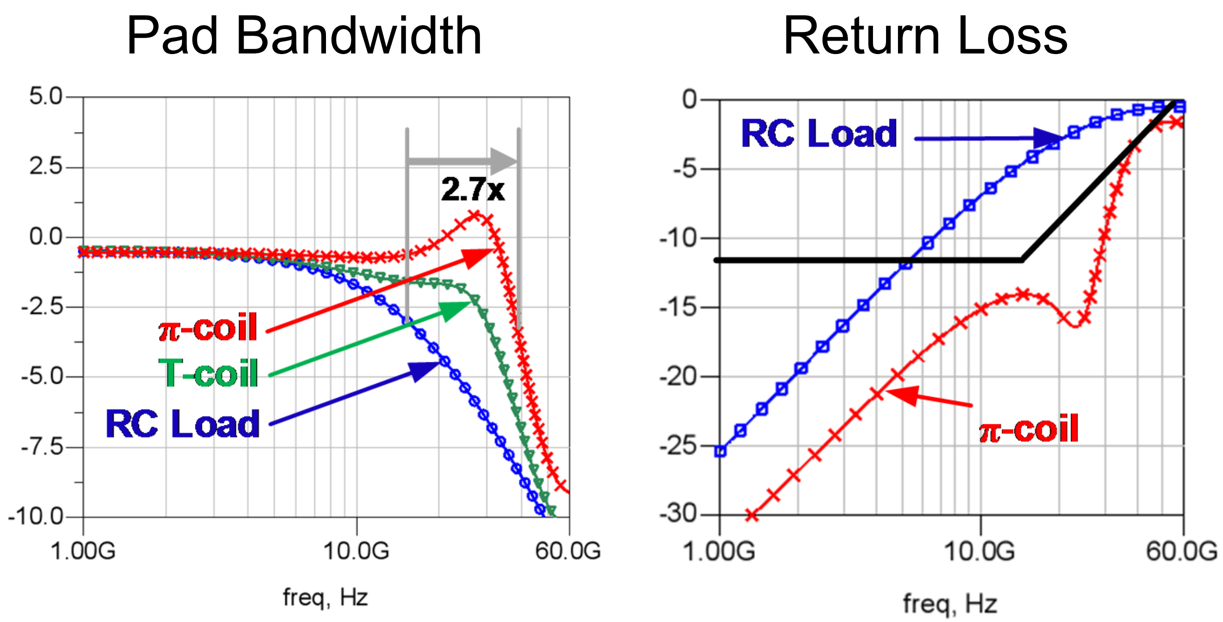
- Large Cpad due to ESD diode (250V-CDM/1kV-HBM), driver junction/metal, termination resistor, C4-bump
- Distributed ESD diodes for size optimization
- **π-coil is used to improve pad bandwidth and meet RL spec**

Output Pad Network

Proposed π-coil network

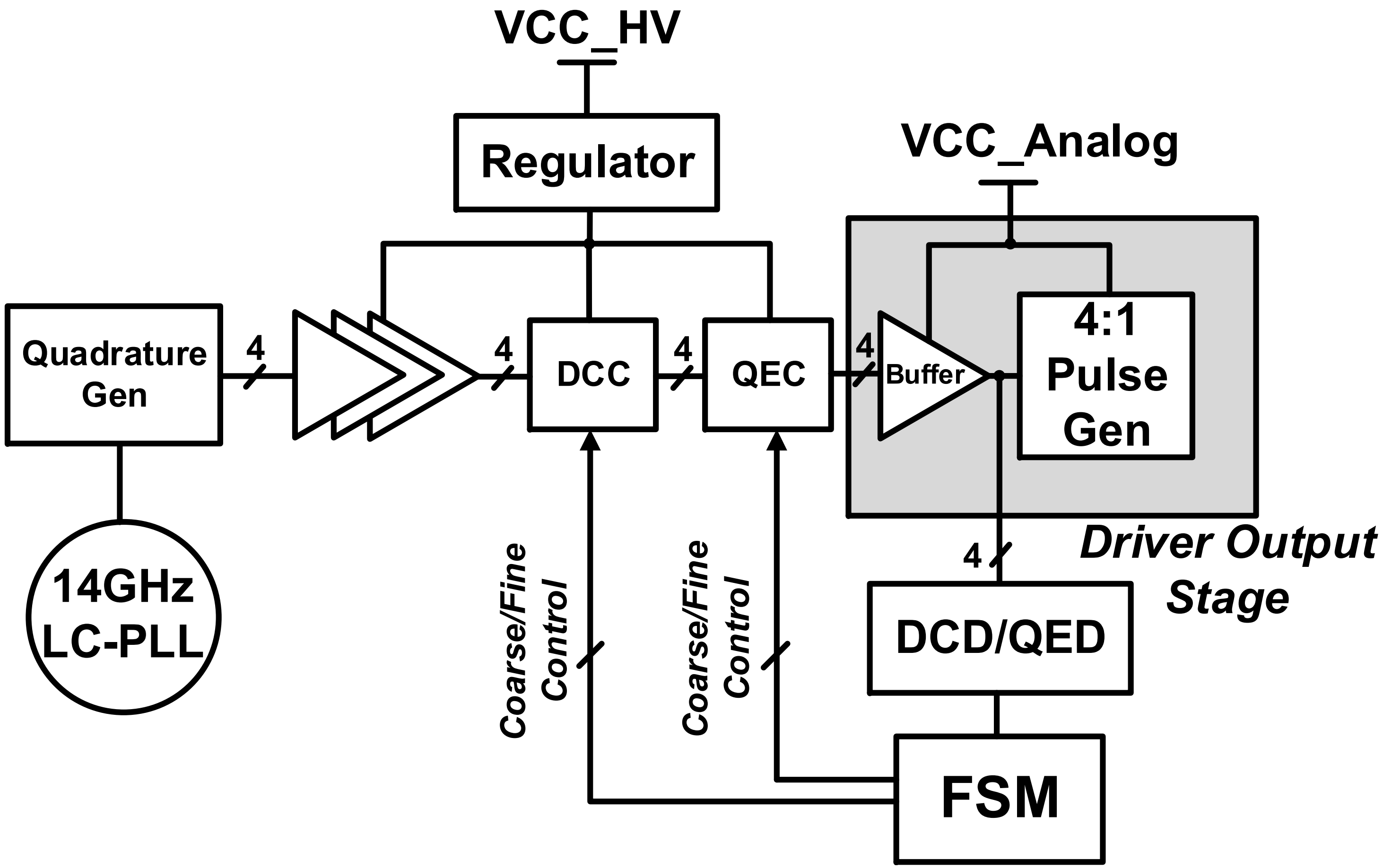


EM simulation results



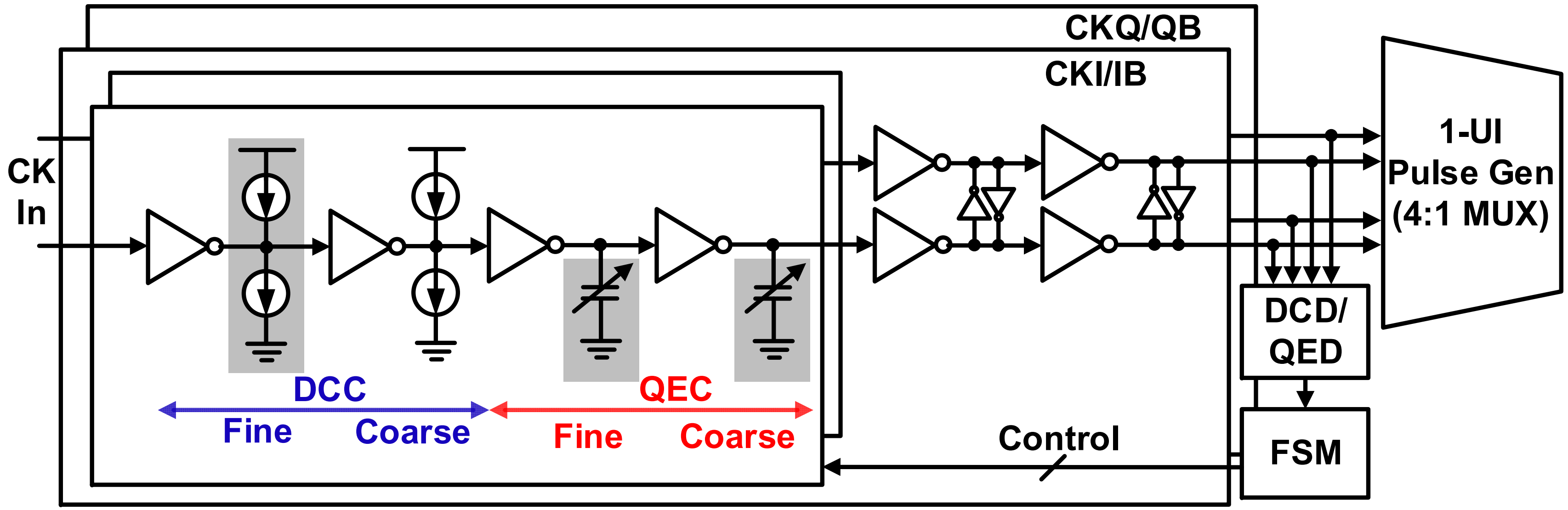
- π-coil improves pad 3-dB bandwidth by 2.7x while meeting RL spec
- Area of π-coil is minimized by leveraging mutual inductance (nested configuration) and optimizing conductor widths to match current densities

Clock Distribution

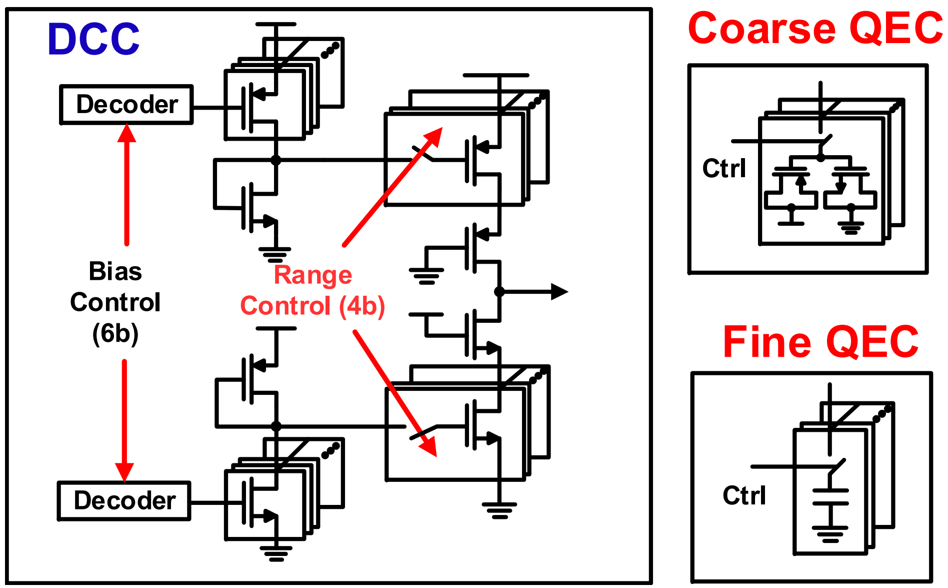


- 10-14GHZ LC-PLL
- Injection-locked I/Q clock gen
- Per-lane DCC/QEC
- Regulated CMOS distribution

Clock Spacing Error Correction (DCC/QEC)



- +/- 8ps coarse correction range
- +/- 1ps fine correction range
- <80fs step size
- Low jitter amplification



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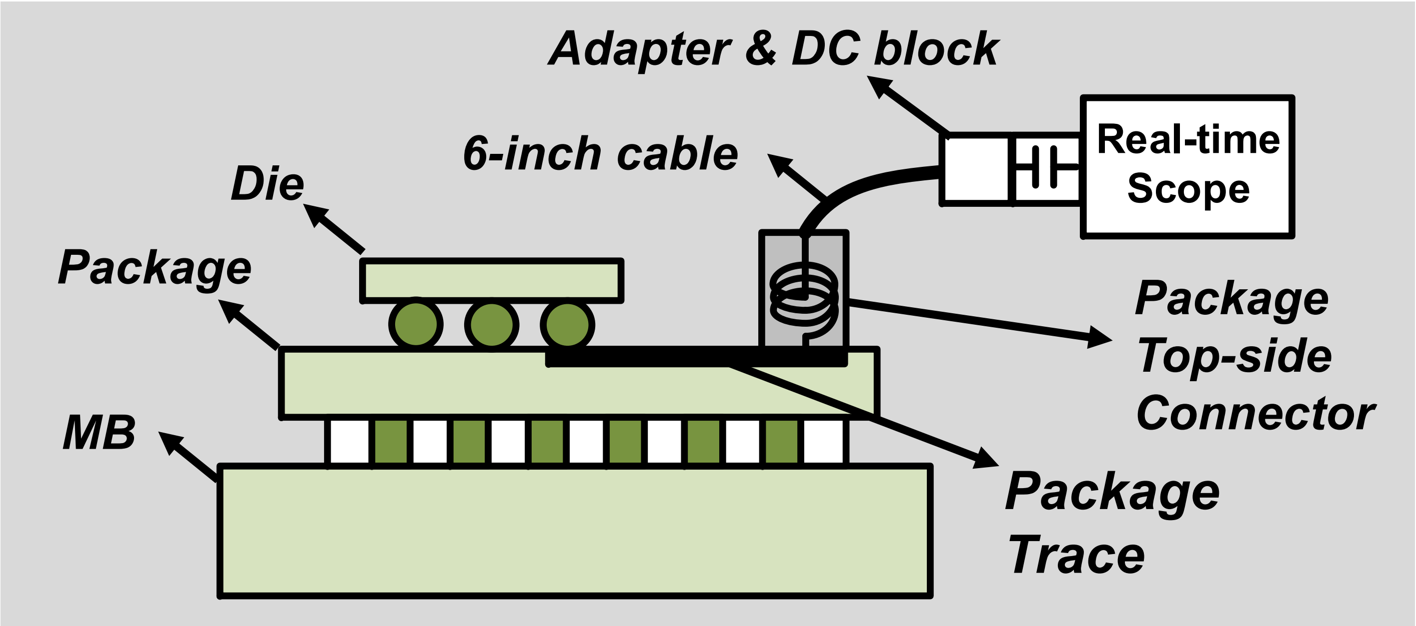
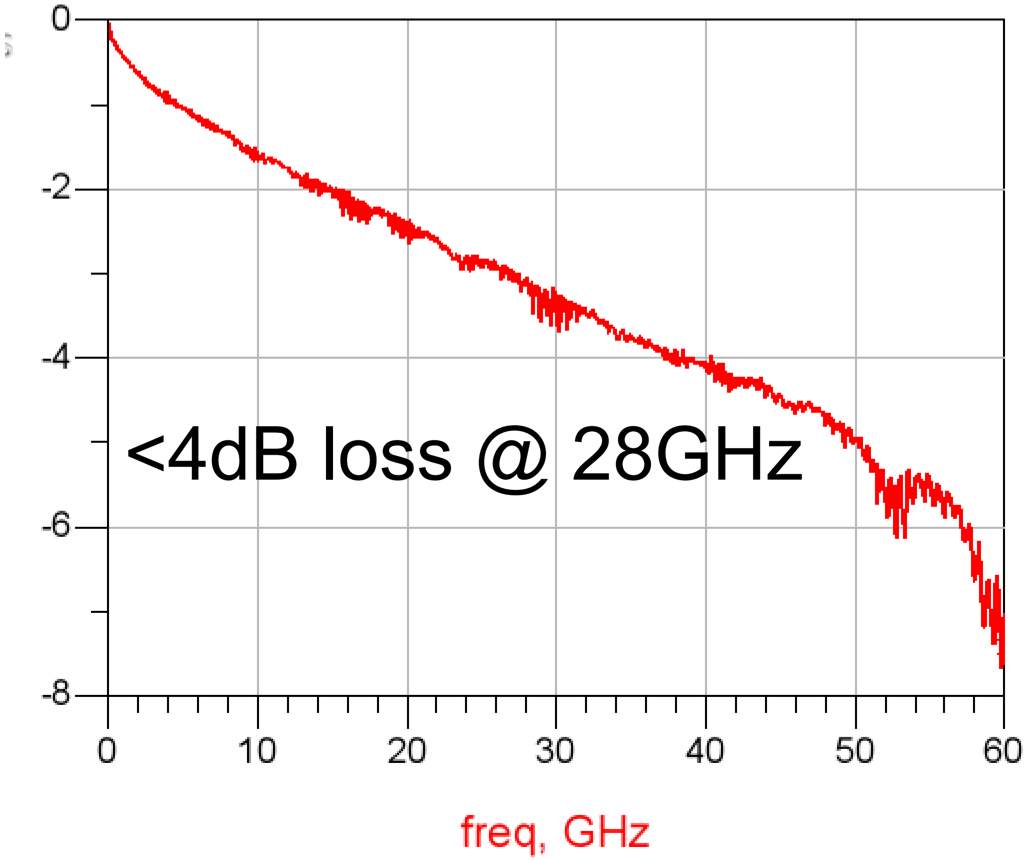
Test Platform

TX test platform configuration

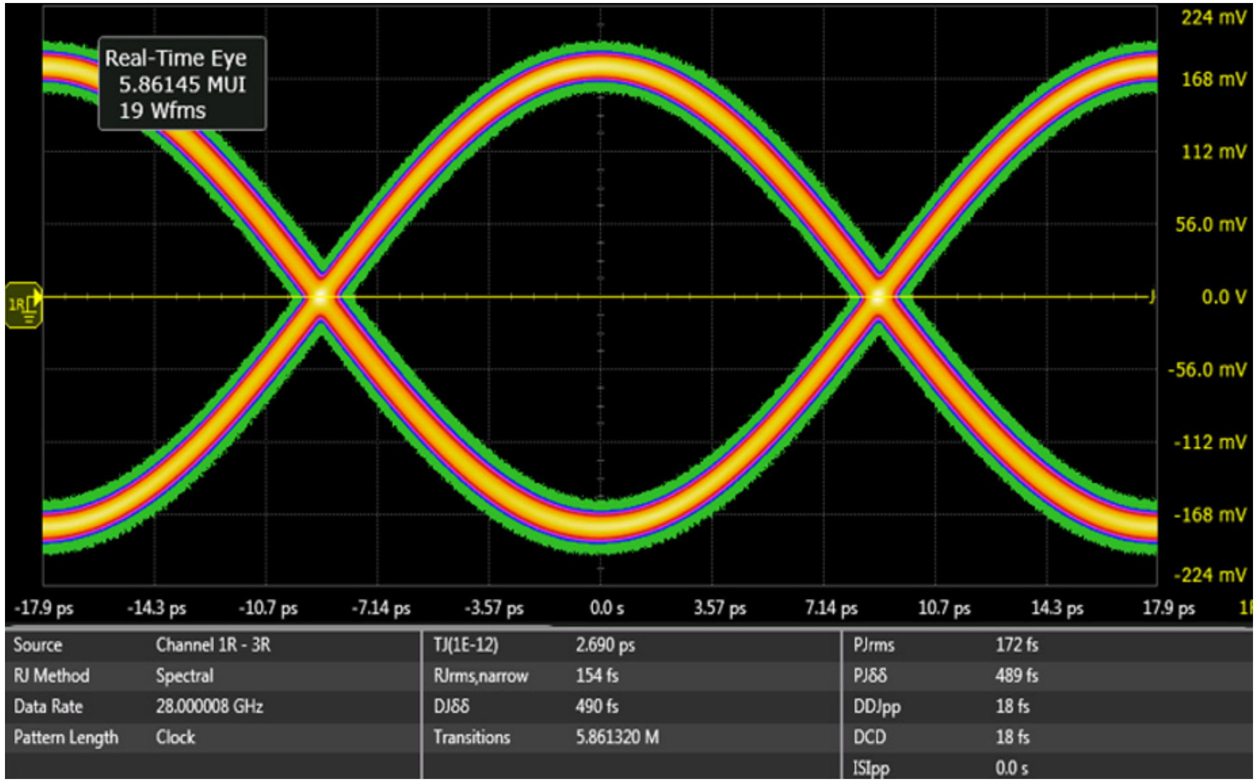


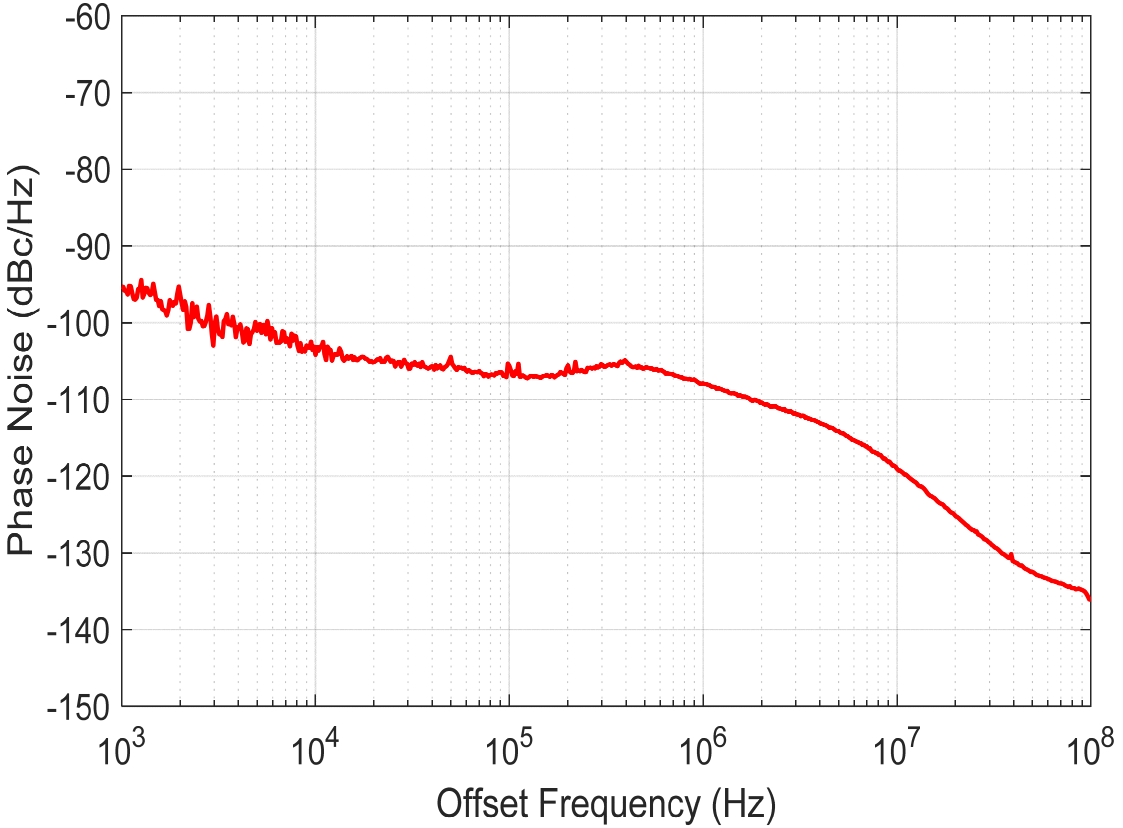
Real-time oscilloscope
- Keysight DSAZ634A

Measure channel IL



28GHz Clock Pattern

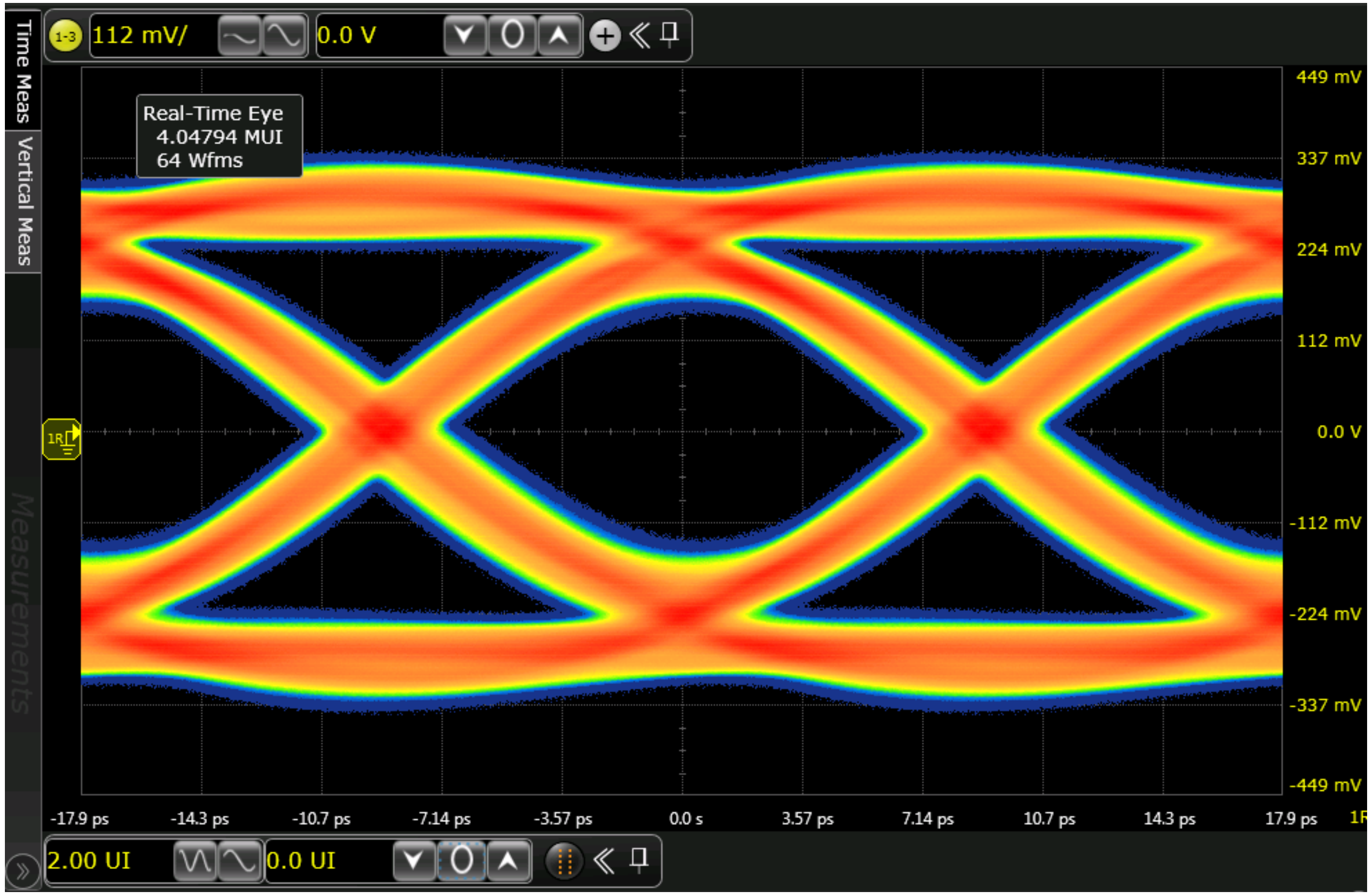




- CDR BW = 10MHz
- RJ=154fs
- DJ=0.49ps
- DCD=18fs

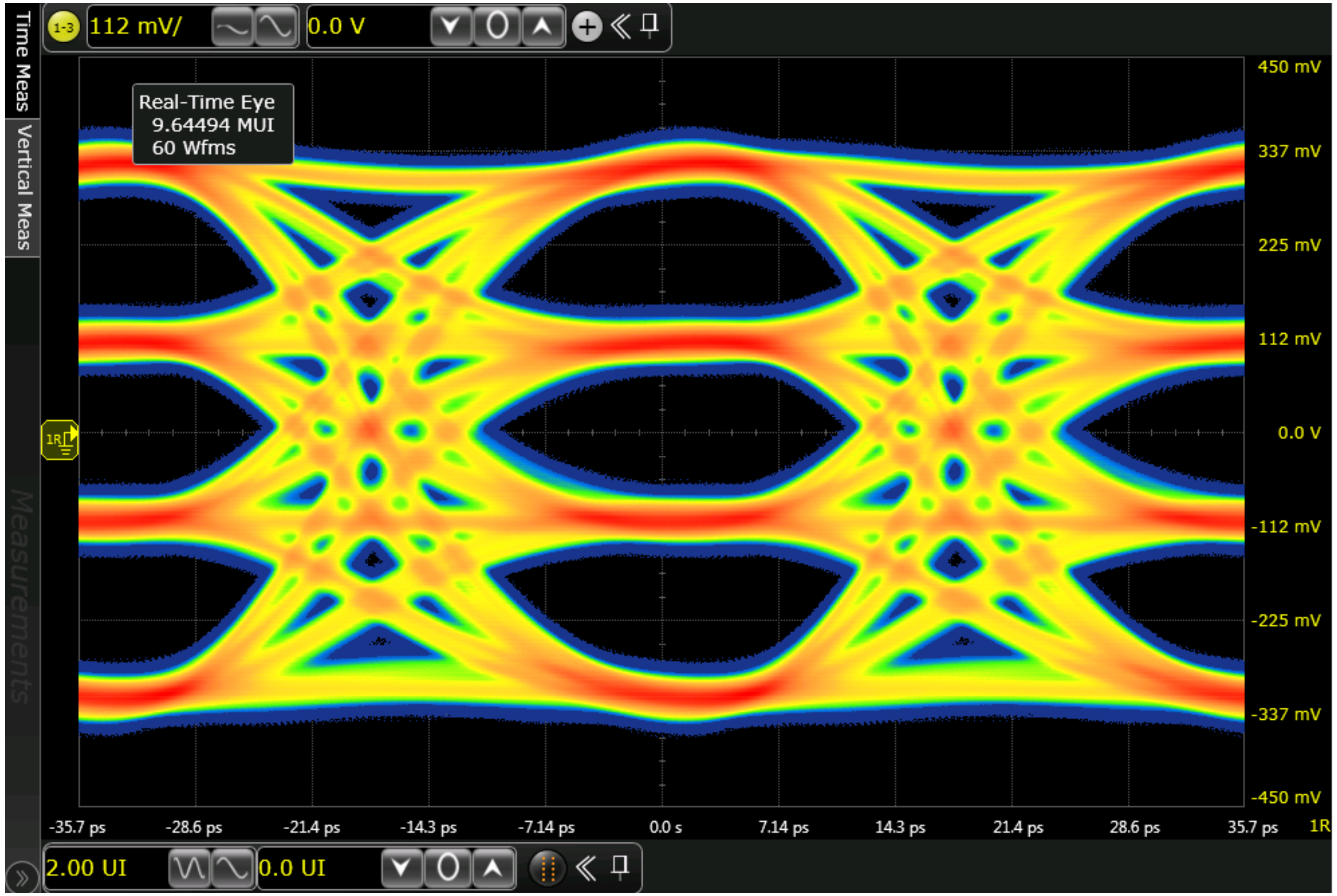
- PLL phase noise
  -108dBc/Hz@1MHz
  -119dBc/Hz@10MHz

56Gb/s NRZ Eye Diagram



- 2.5dB post-cursor EQ
- TJ=7.6ps, ISI=2.5ps @ BER=10^{-12}
- EH=260mV

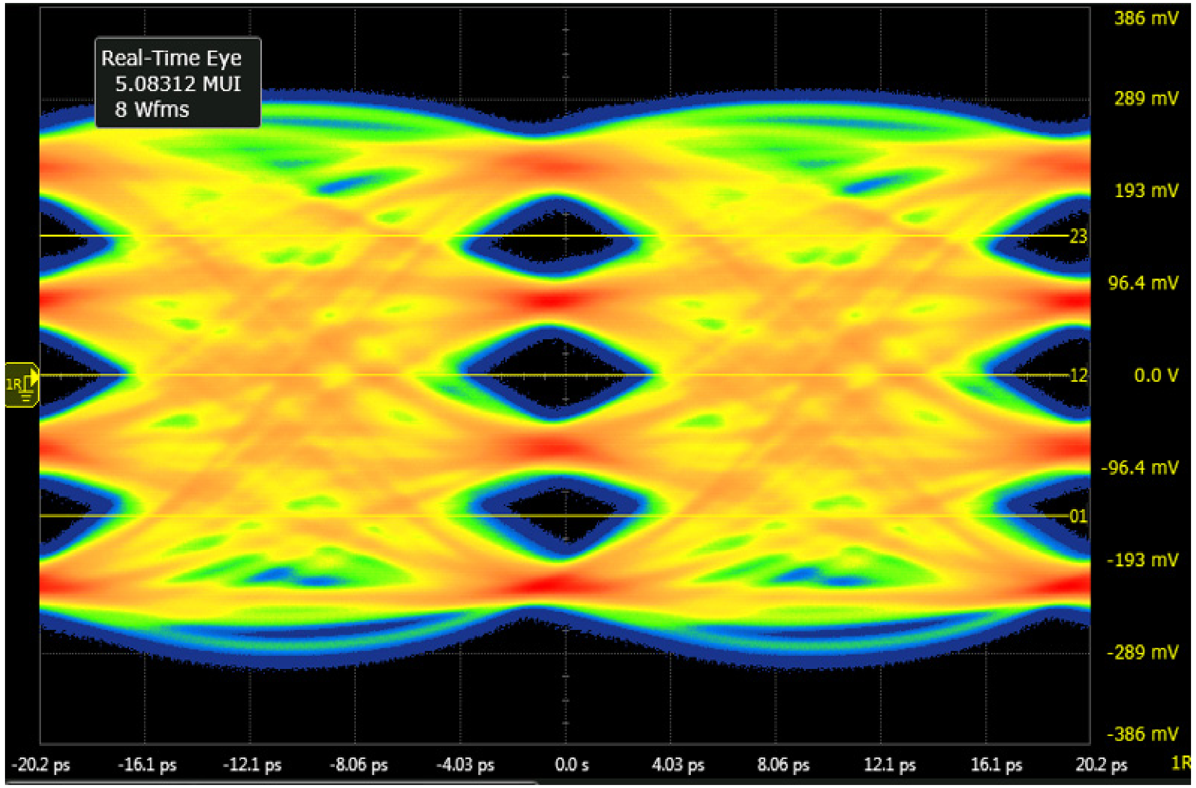
56Gb/s PAM-4 Eye Diagram



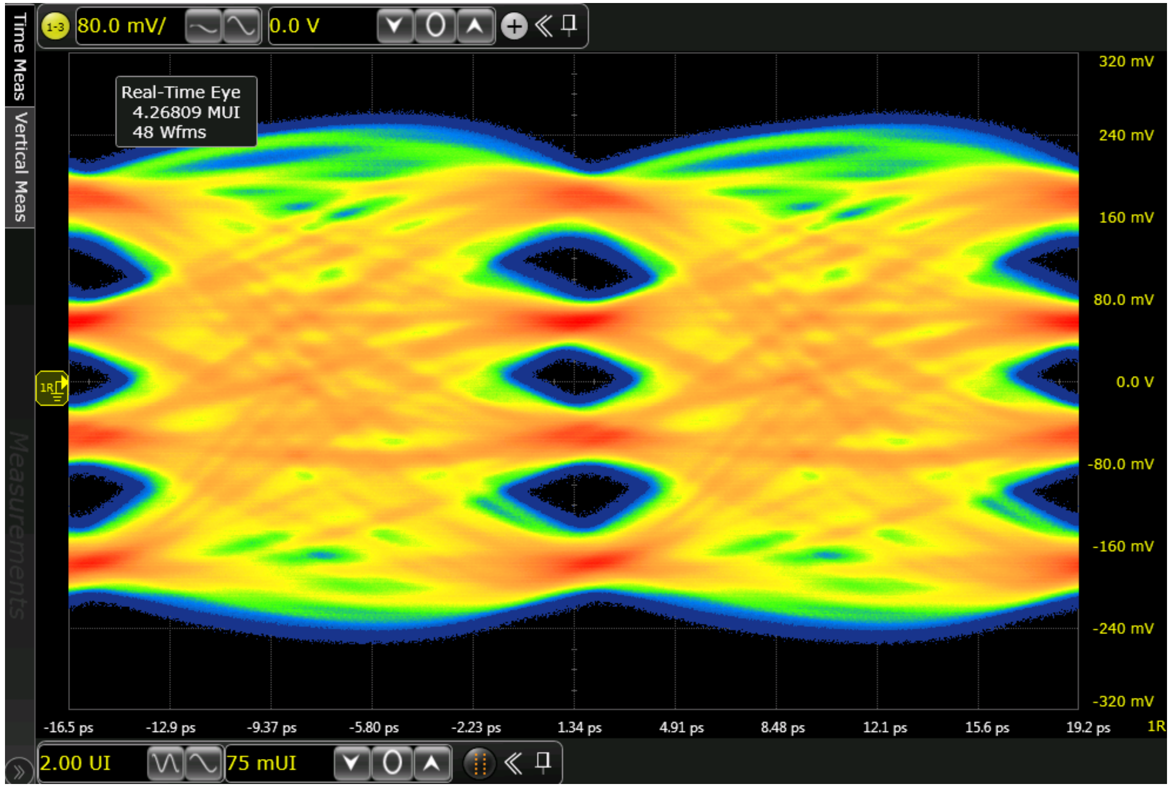
- No EQ
- EH>98mV
- RLM=99.3%

100 & 112Gb/s PAM-4 Eye Diagrams

100Gb/s



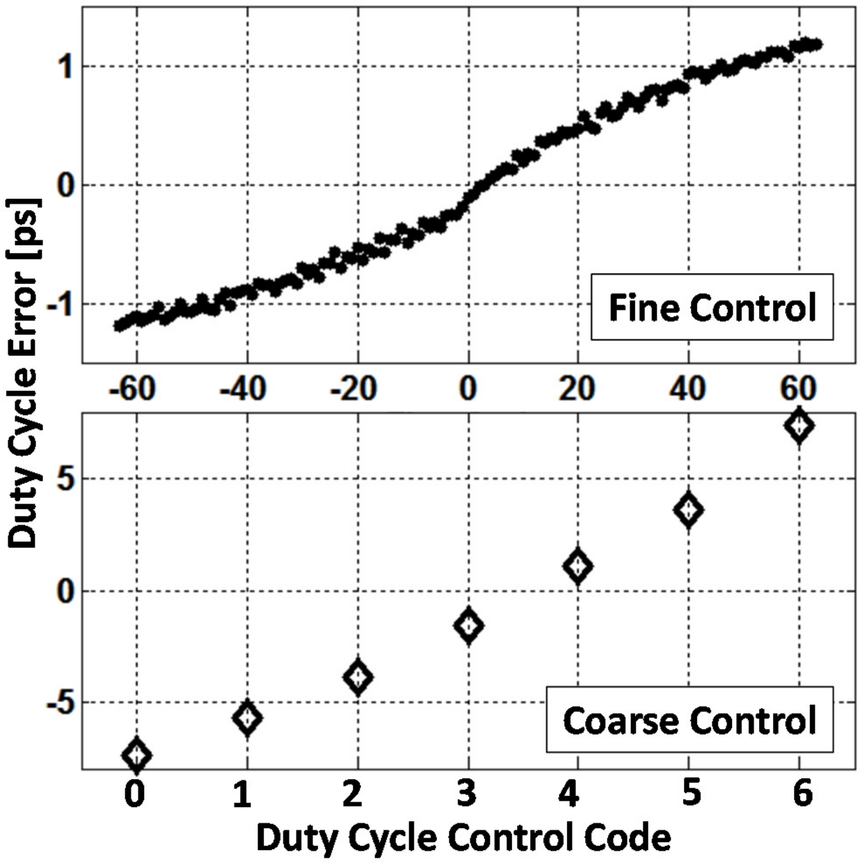
112Gb/s



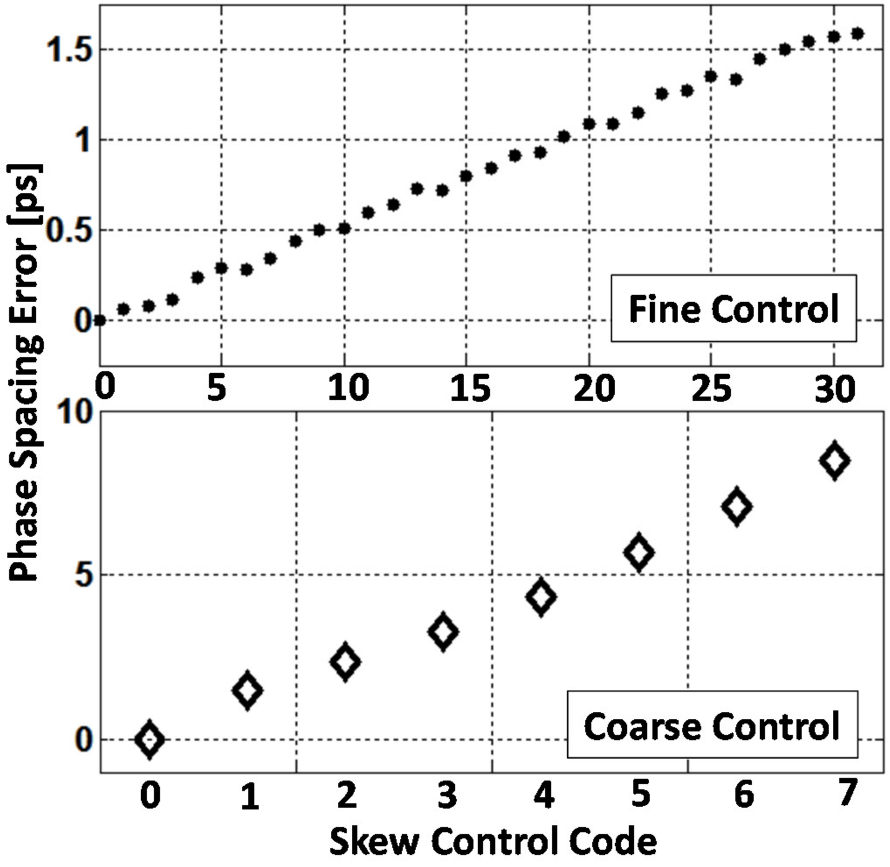
- EH>30mV
- RLM=98.5%

DCC & QEC Measurement

Duty-cycle Correction

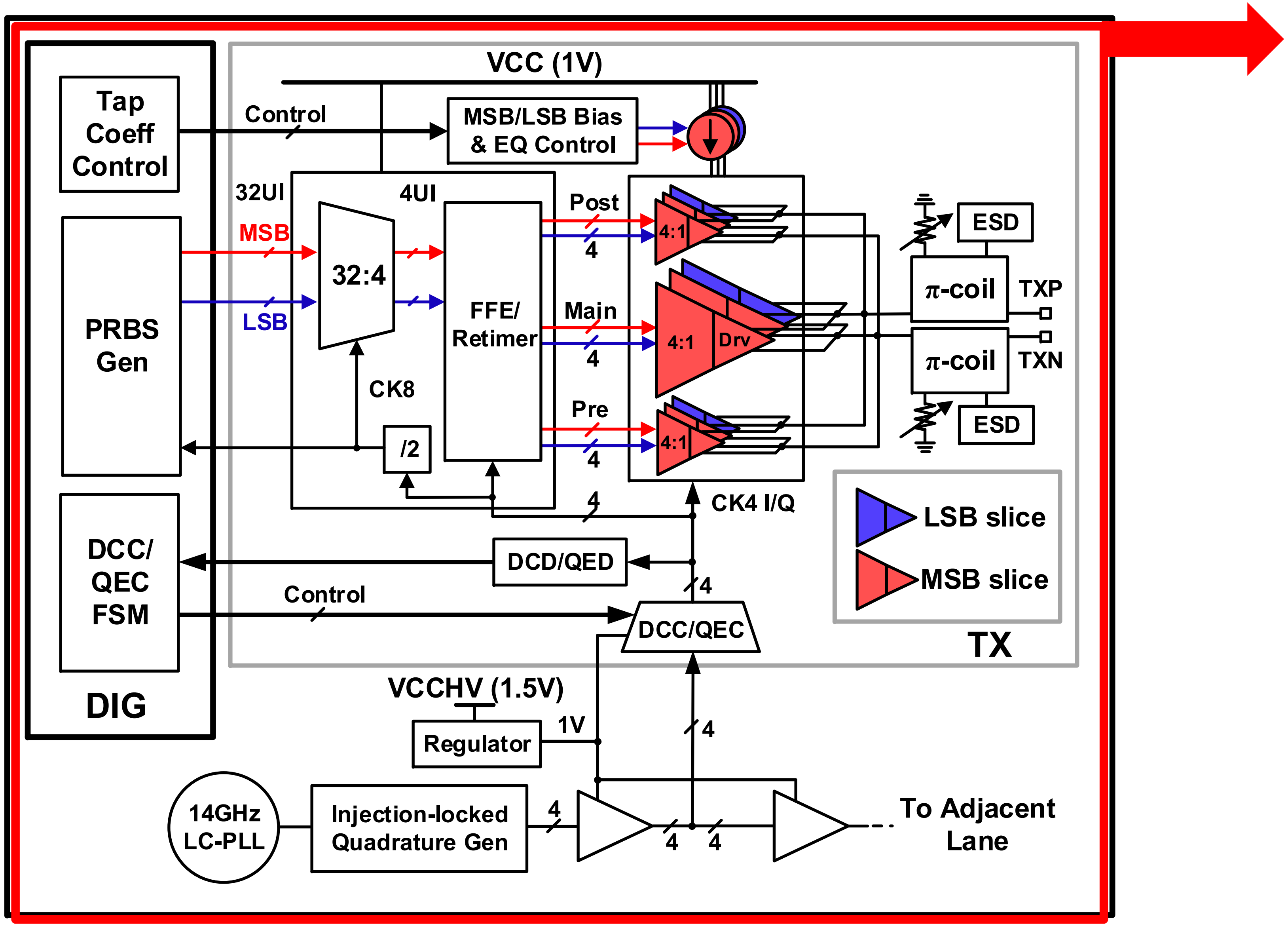


Quadrature-error (skew) Correction



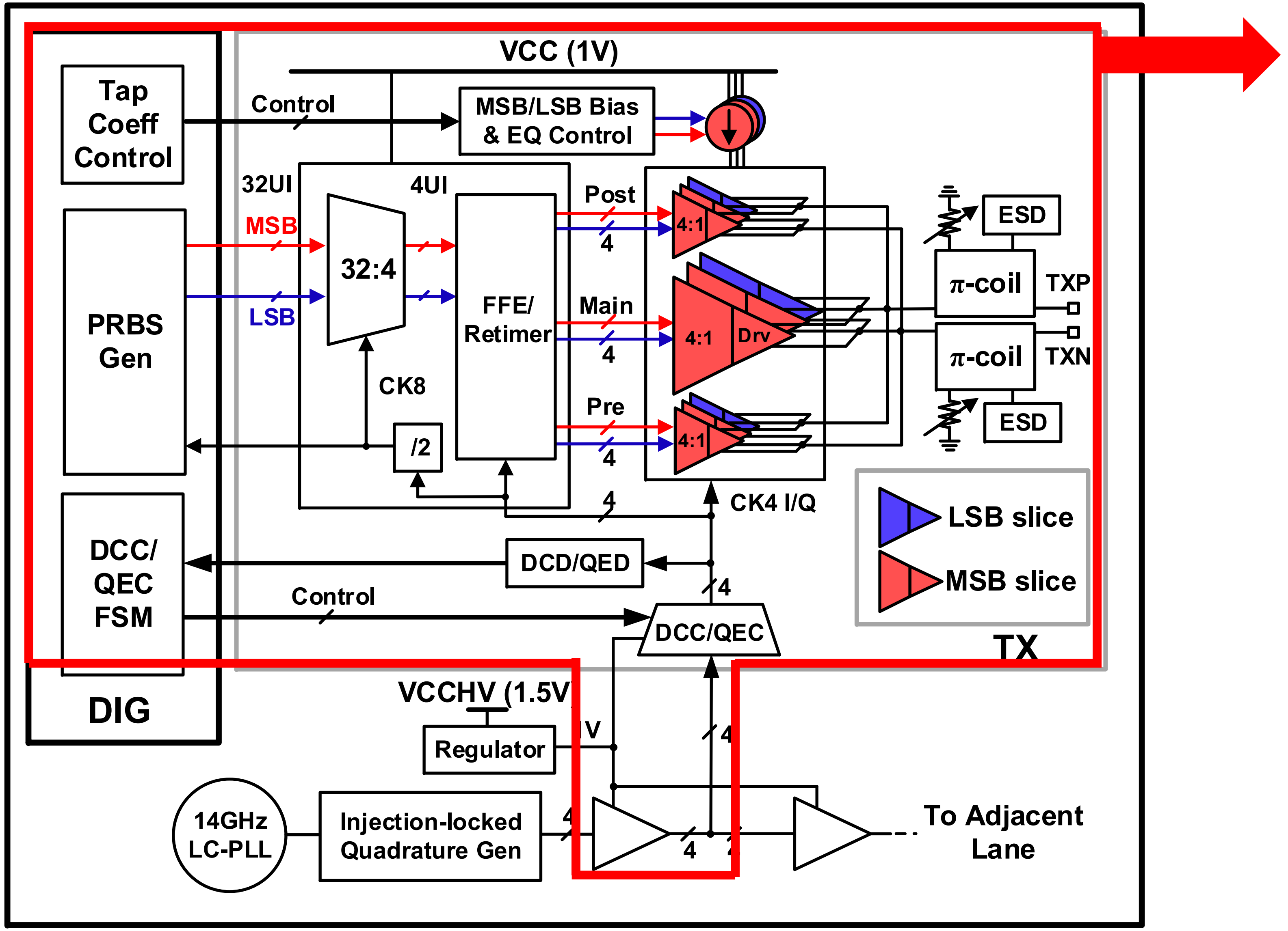
- Correction range > +/- 8ps
- Correction step size < 80fs

Power Consumption



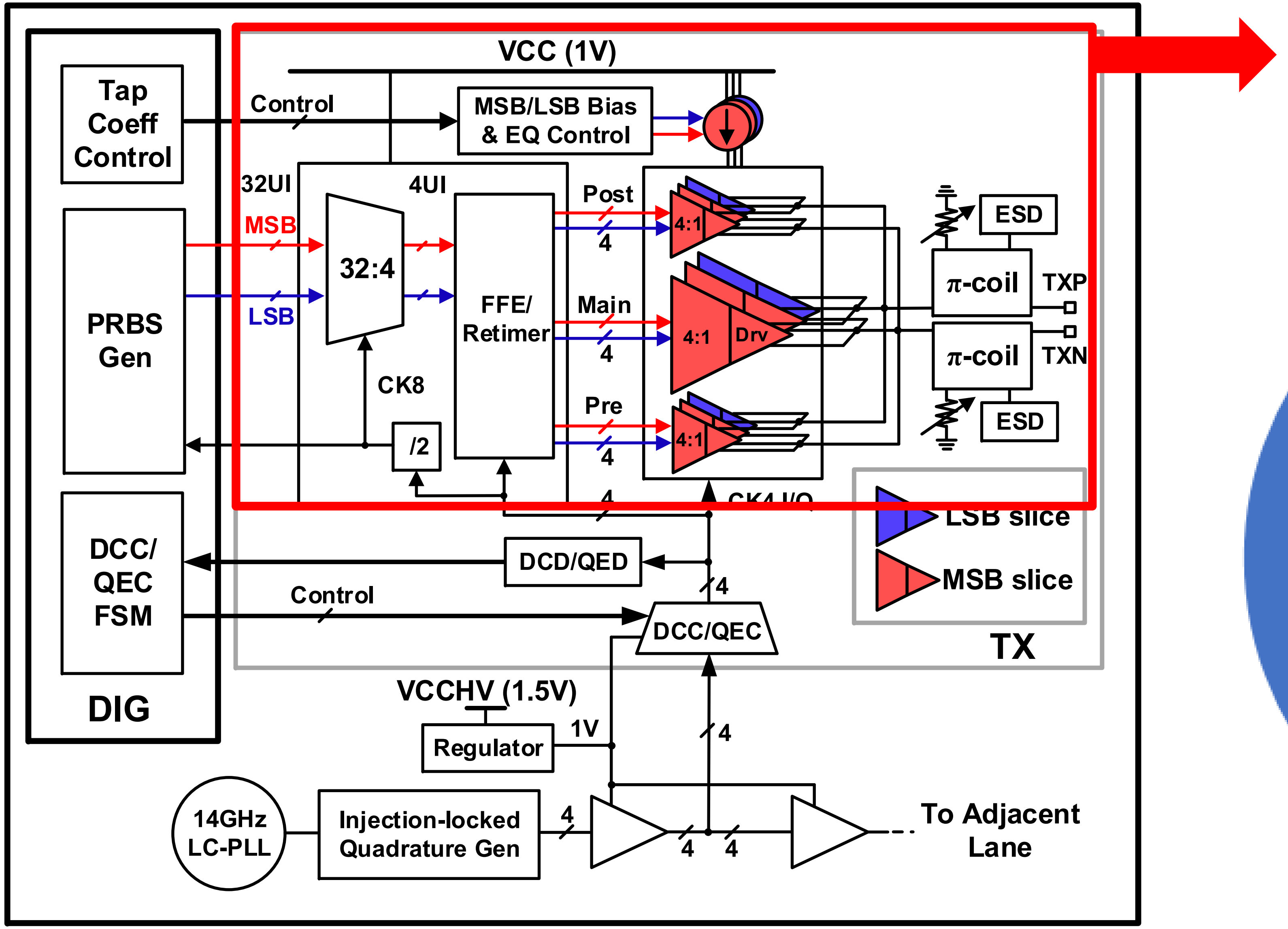
232mW for 112Gb/s PAM4 (2.07pJ/bit)

Power Consumption

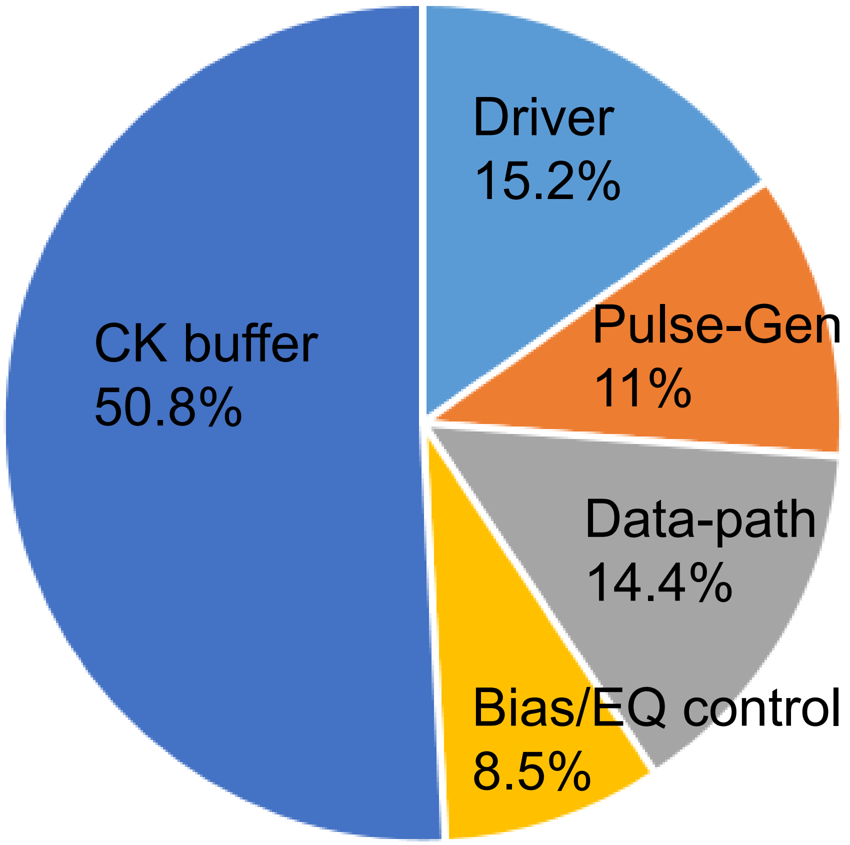


193mW for 112Gb/s PAM4 (1.72pJ/bit)

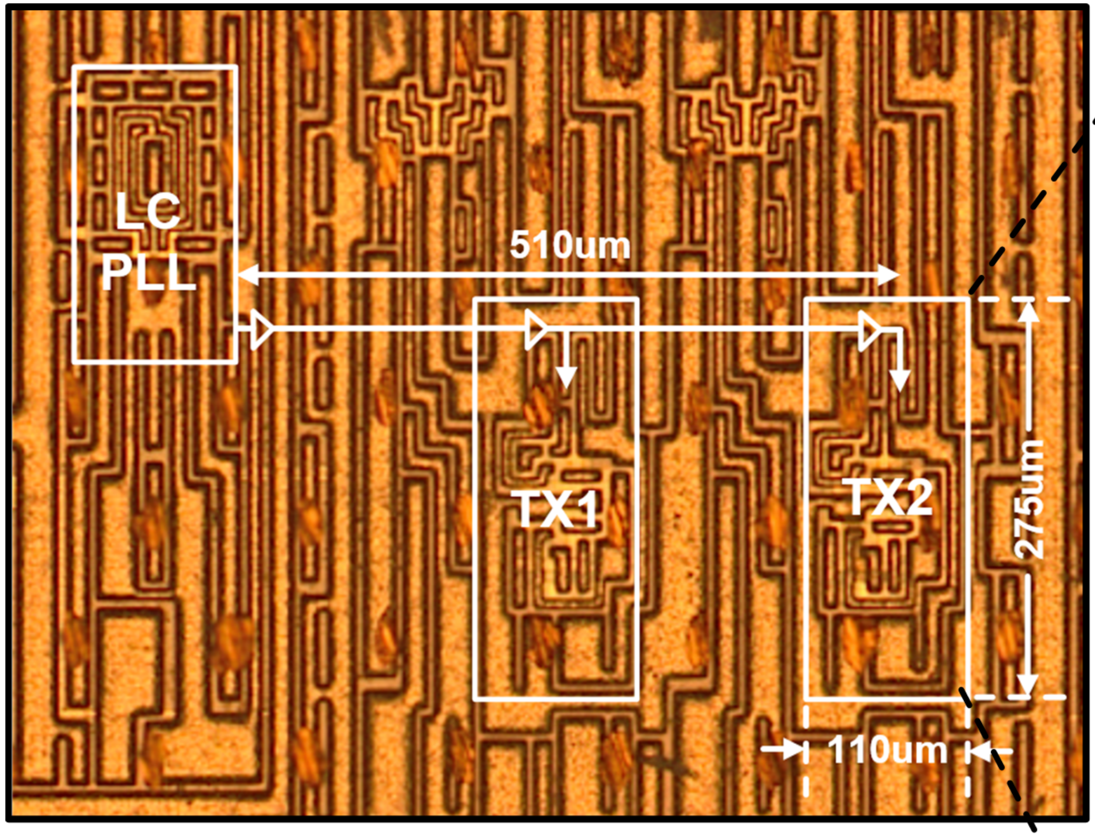
Power Consumption

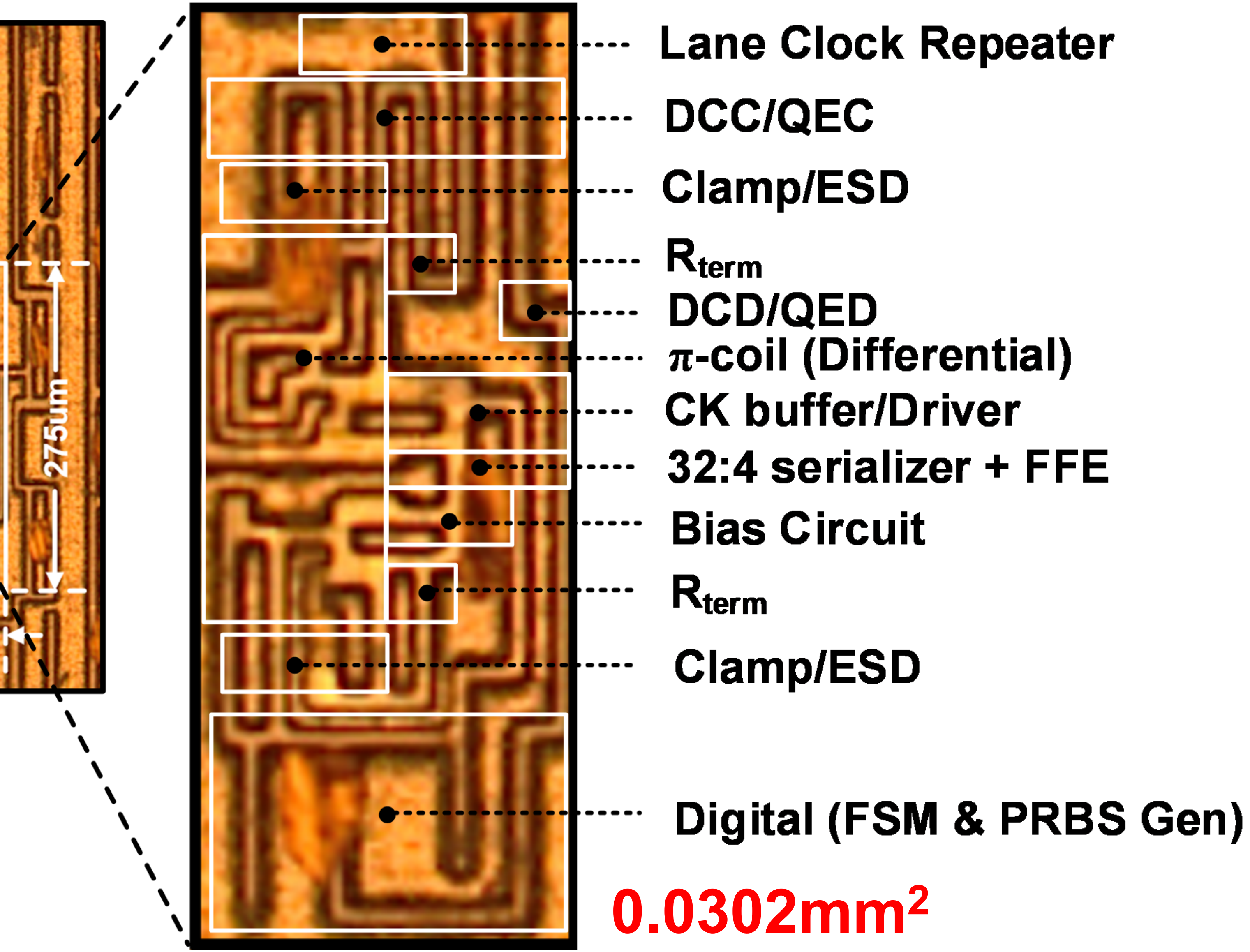


118mW for 112Gb/s PAM4 (1.05pJ/bit)



Die Photo





$0.0302mm^2$

Performance Comparison

	Steffan ISSCC '17	Dickson ISSCC '17	Bassi ISSCC '16	Frans ISSCC '16	This Work		
Technology	28nm FDSOI	14nm FinFET	28nm FDSOI	16nm FinFET	10nm FinFET		
Architecture	Quarter-rate	Half-rate	Half-rate	Quarter-rate	Quarter-rate		
Modulation	PAM-4	PAM-4	PAM-4	NRZ	NRZ	PAM-4	PAM-4
Data Rate	64Gb/s	56Gb/s	45Gb/s	64Gb/s	56Gb/s	56Gb/s	112Gb/s
Clock Source	On-chip PLL	External	External	On-chip PLL	On-chip PLL		
FFE	4-tap	3-tap	4-tap	3-tap	3-tap		
Driver Type	CML	SST	SST-hybrid	CML	CML		
Output Network	Double T-coil	None	T-coil	T-coil	π-coil		
Output Swing w/o FFE	$1.2V_{ppd}$	$0.9V_{ppd}$	$1.3V_{ppd}$	$0.8V_{ppd}$	$0.75V_{ppd}$		
RJ - Clock Pattern	$290fs_{rms}$	$318fs_{rms}$	NA	$150fs_{rms}$	$154fs_{rms}$		
RLM	94%	NA	94%	NA	NA	99.3%	98.5%
SNR	NA	NA	NA	NA	NA	>31dB	31dB
Energy/bit (TX+Clock Distribution)	2.26pJ/bit** (w/o PLL)	1.8pJ/bit (w/o PLL)	NA	5.31pJ/bit	4.14pJ/bit	1.9pJ/bit	2.07pJ/bit
Energy/bit (TX FE only)	NA	NA	2.66pJ/bit	3.51pJ/bit	3.44pJ/bit	1.7pJ/bit	1.72pJ/bit
TX Area (w/o PLL)	NA	$0.035mm^2$	$0.28mm^2$	$0.32mm^2$	$0.0302mm^2$		

Summary

- 56GS/s NRZ/PAM-4 dual-mode TX was implemented in Intel 10nm technology
- TX achieves jitter (RJ/DJ) performance compliant with CEI-56G NRZ LR spec
- TX achieves the lowest area and better energy efficiency at about twice the data-rate of previously published PAM-4 TXs

Acknowledgement

Anabella Jimenez, Pamela Le, Kelan Ren, Dan Shi,
Danny John, Ahmet Durgun, Renee Garcia,
Byron Grossnickle, Joshua Bondie, Dennis Baker

Thank you!

A 112Gb/s 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS

Christian Menolfi[1], Matthias Braendli[1], Pier Andrea Francese[1], Thomas Morf[1], Alessandro Cevrero[1], Marcel Kossel[1], Lukas Kull[1], Danny Luu[2,1], Ilter Ozkaya[1,3], Thomas Toifl[1]

[1]IBM Research, Rüschlikon, Switzerland

[2]ETH, Zurich, Switzerland

[3]EPFL, Lausanne, Switzerland

Motivation

The need for speed …

- I/O data rates growing to 100Gb/s + in the near future
- Standards like OIF CEI working on 112Gb/s
- Higher speed, higher losses → precise equalization
- Multilevel signaling (such as PAM-4) require more associated signal processing (FEC etc.)
- Increasing complexity and digital signal processing

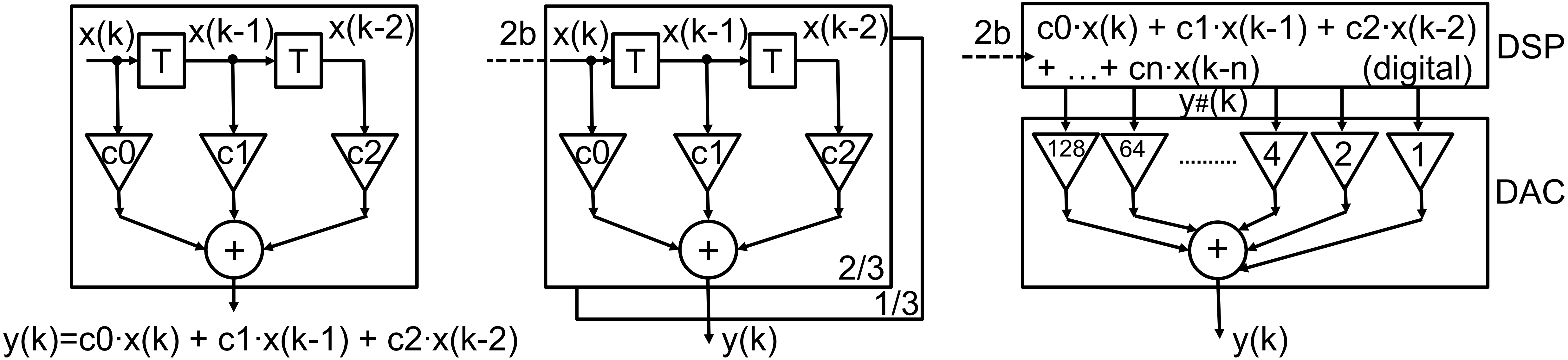
➢ DAC based TX

Outline

- Introduction
- Block Diagram
- Circuit Implementation
  - 4:1 Multiplexer
  - Active Peaking Pre-Driver
  - SST Driver Segment
  - Clock Duty-Cycle Correction
- Experimental results
- Summary/Conclusion

DAC based TX

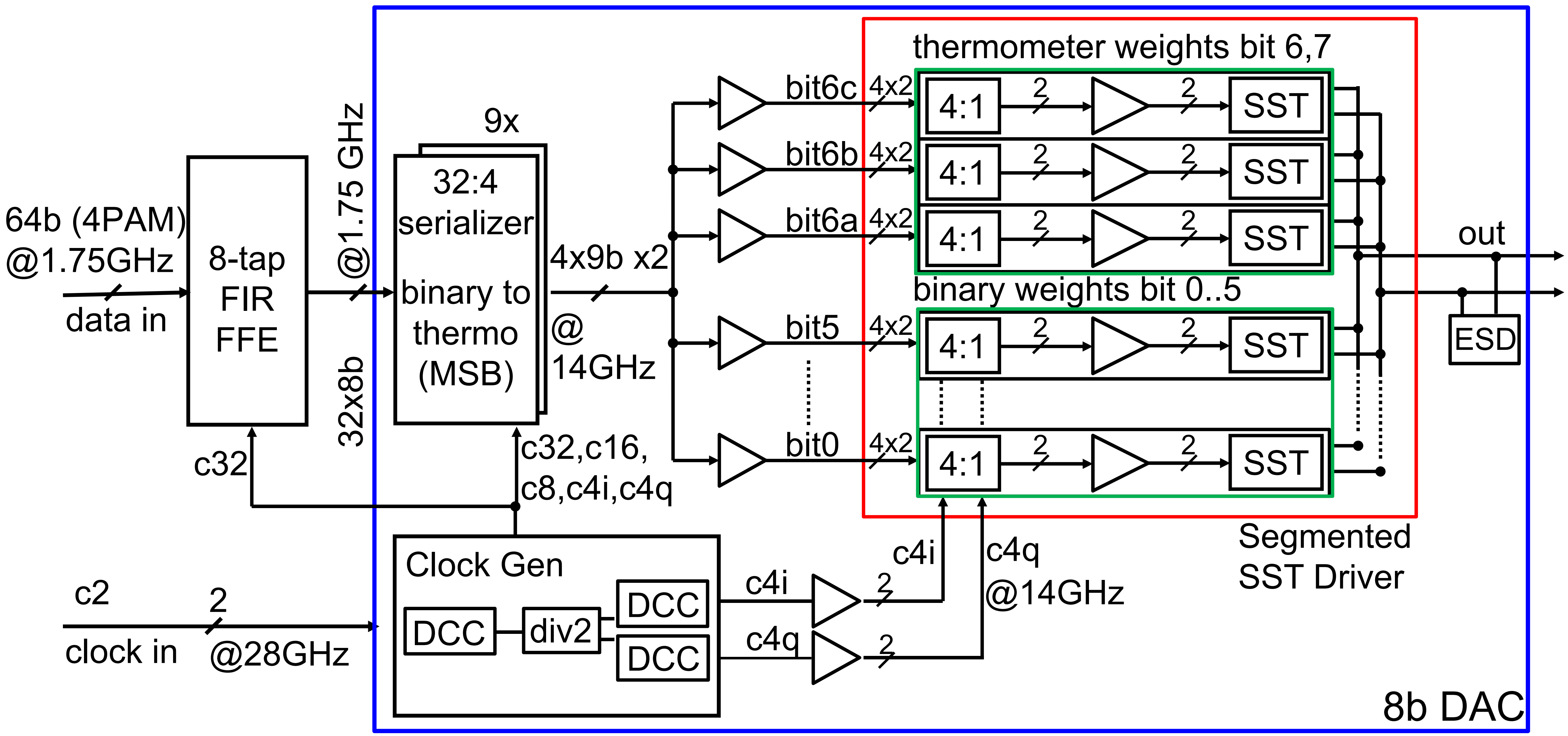
NRZ: 3-tap FFE | PAM-4: 3-tap FFE | PAM-4: N-tap FFE



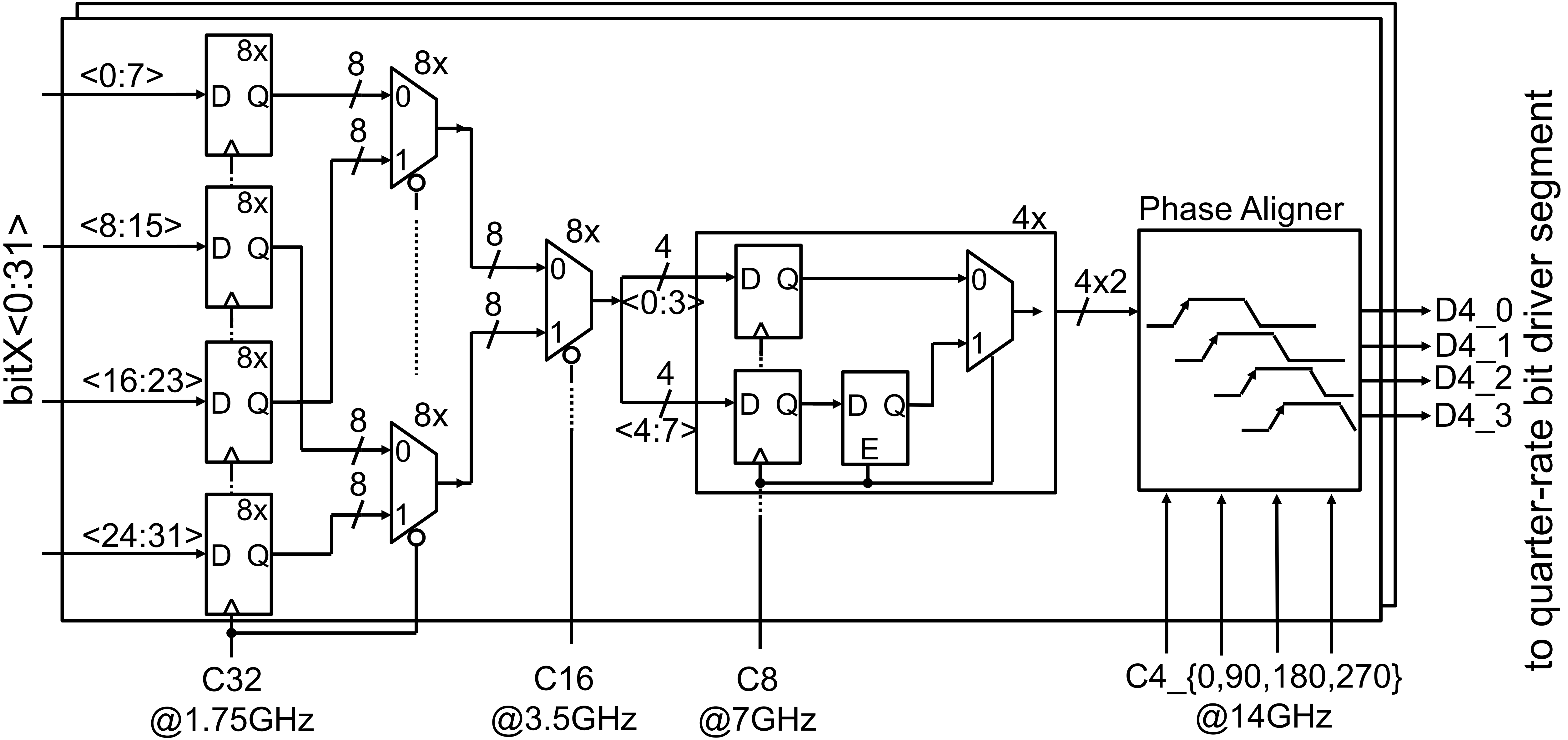
- "Traditional" TX FFE structure
  - time-delayed data streams x[k-n]
  - variable weight sub-drivers with weight cn
  - limited number of taps
- DAC based TX FFE structure
  - digital FFE implementation → digital sample y#(k)
  - sample bit data streams
  - fixed binary weight sub-drivers
  - suitable for larger number of taps

➢ **Maximum flexibilit**y in # taps and weights

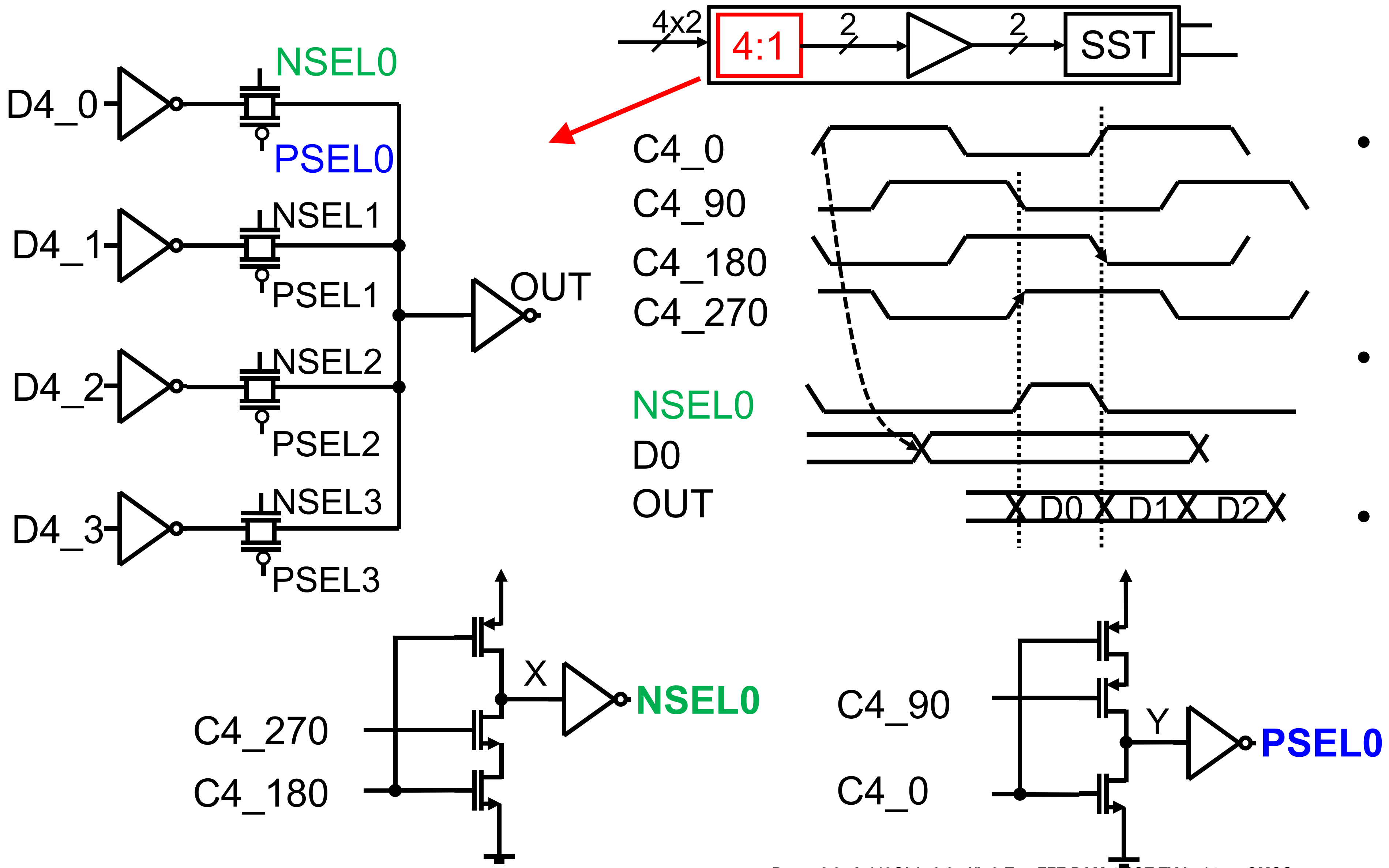
TX Block Diagram



32:4 Serializer

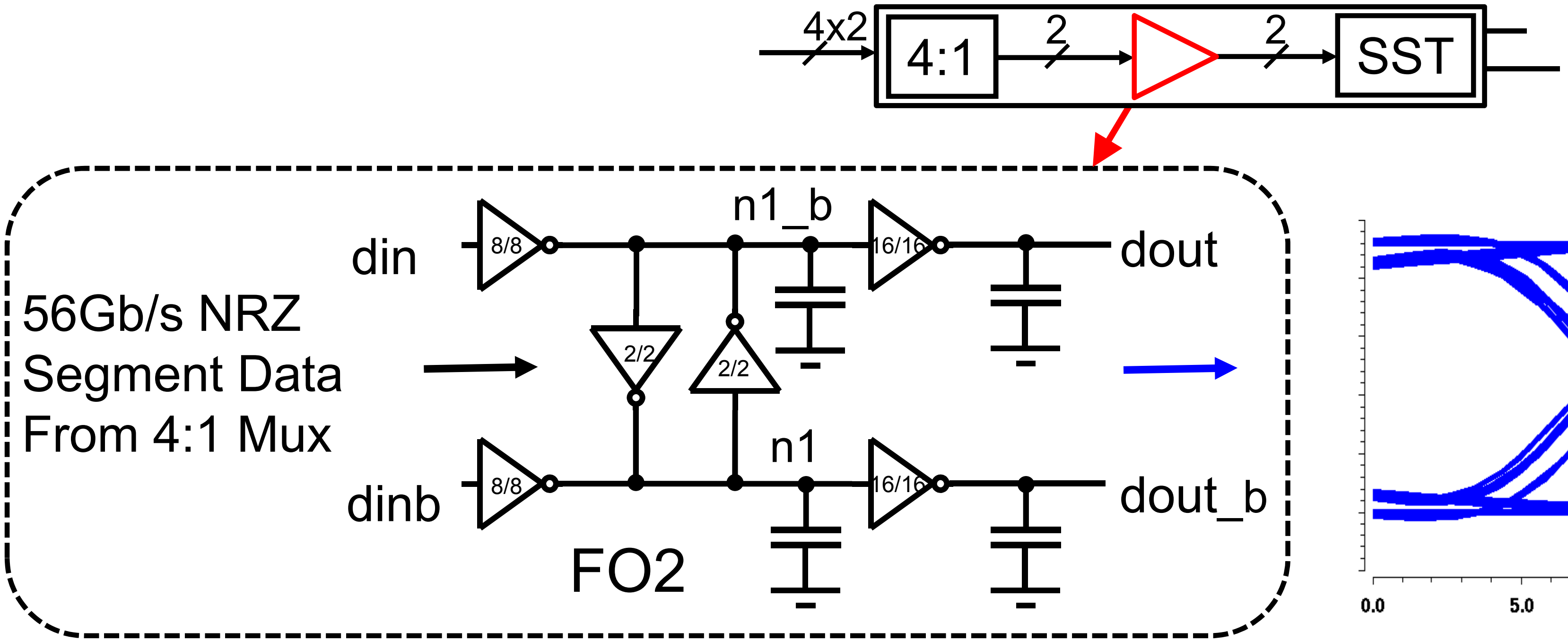


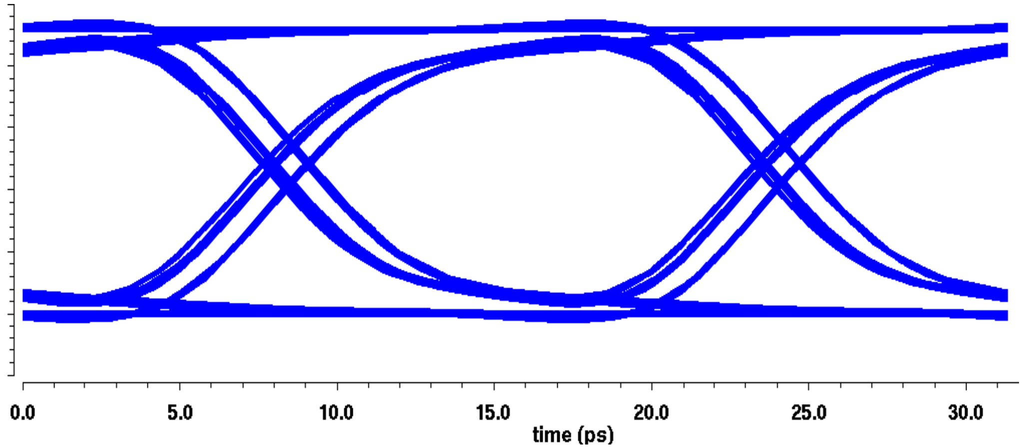
Quarter-Rate 4:1 Multiplexer



- Pulsed pass-gate mux with 25% duty-cycle select pulse
- D4_0 launched on rising edge of CK4_0
- NSEL0 on the last U.I. of quarter-rate period

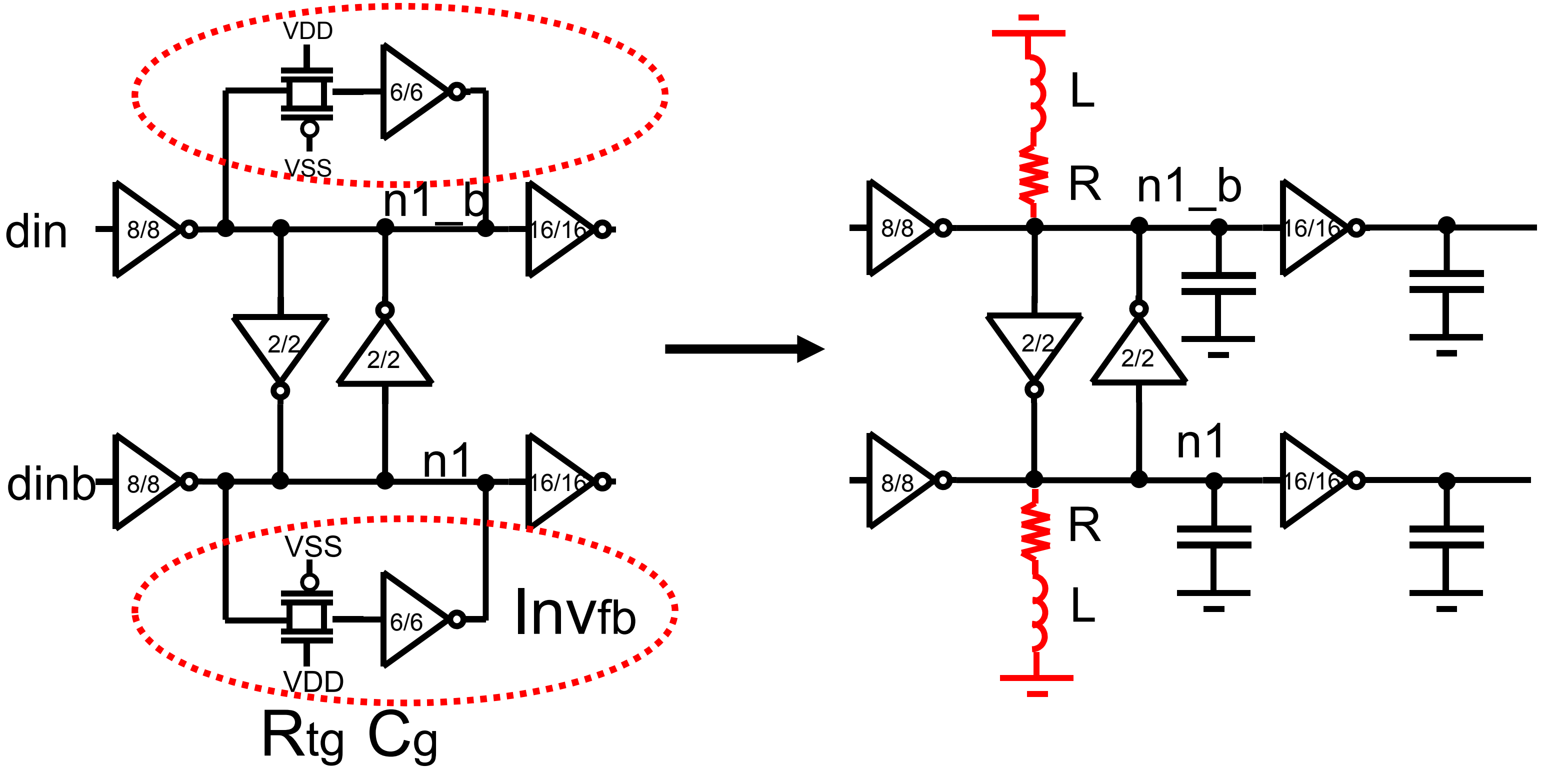
CMOS Pre-Driver

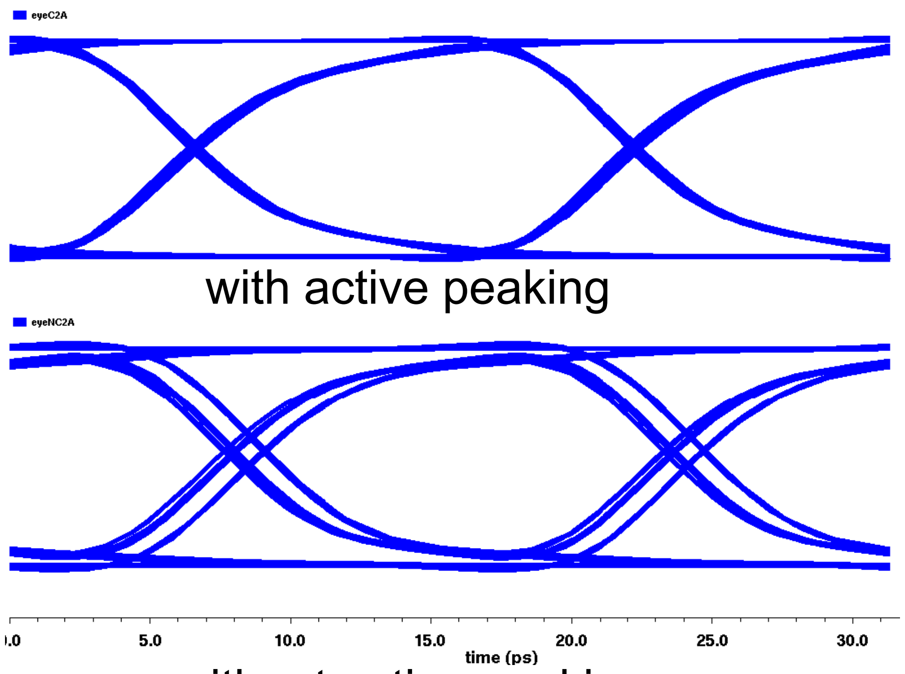




- Pre-driver: Motivation is to save power in the 4:1 mux
- Conventional static CMOS speed performance is limited by technology
- At 56Gb/s data rate the pre-driver no longer settles within 1U.I. in FO2 configuration
- Intersymbol interference

Active Peaking CMOS Pre-Driver





without active peaking

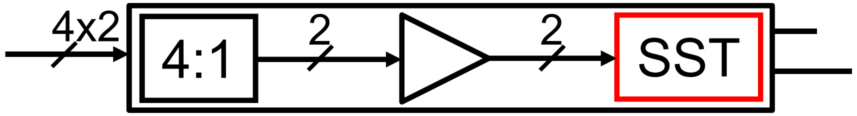
[6] H. W. Lu, et al.,"A Scalable Digitalized Buffer for Gigabit I/O," *Proc. CICC*, pp. 241-244, Sept. 2008.

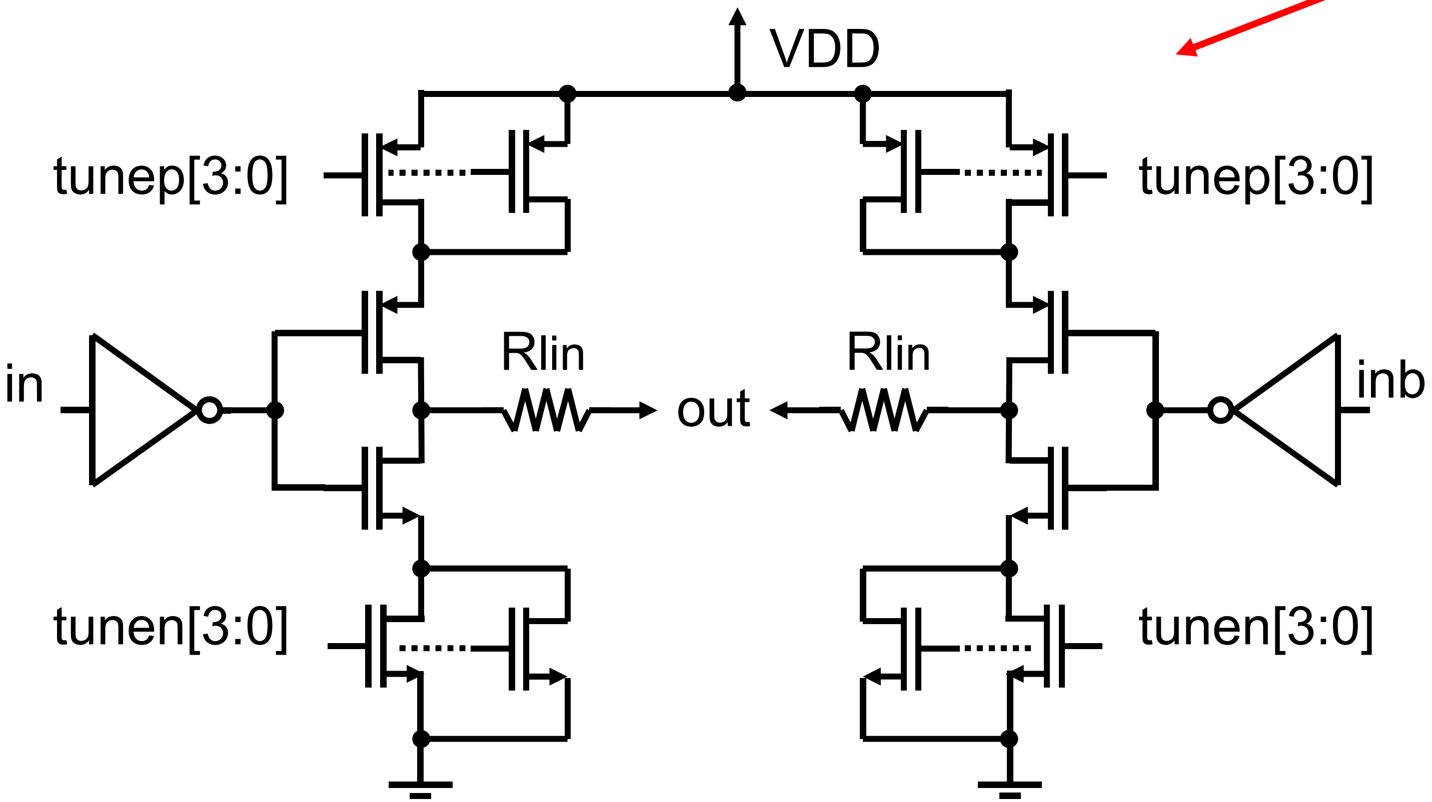
$R \approx 1/g_{mfb}$

$L \approx R_{tg}C_g/g_{mfb}$

- Active peaking enhances performance of static CMOS (at the cost of higher power consumption)

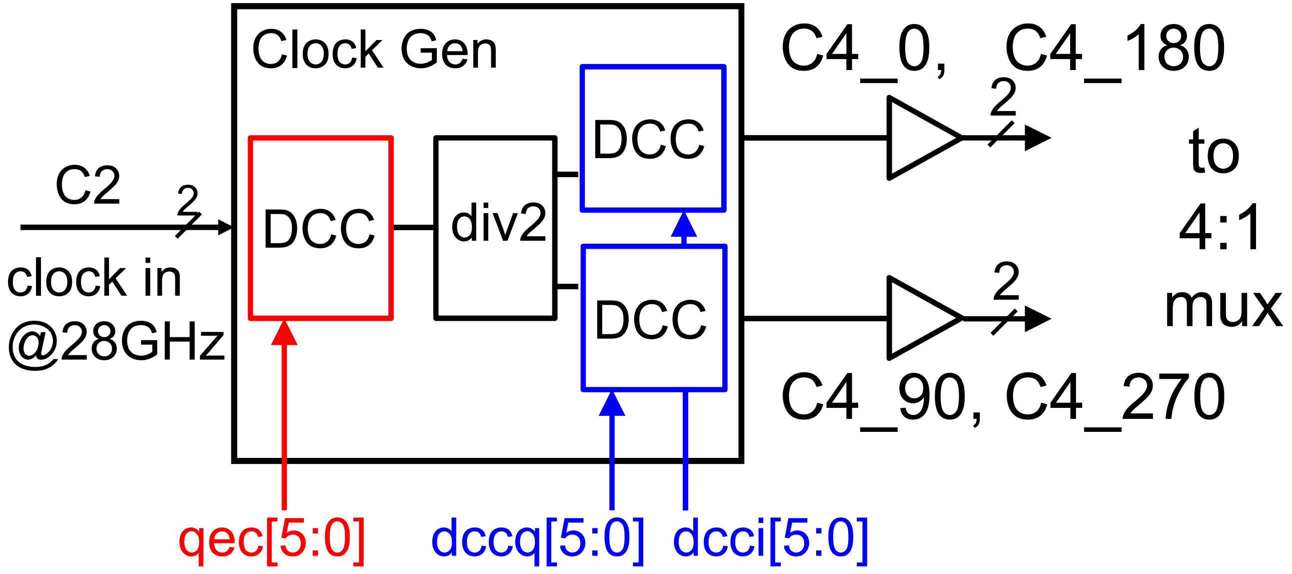
SST Driver Stage

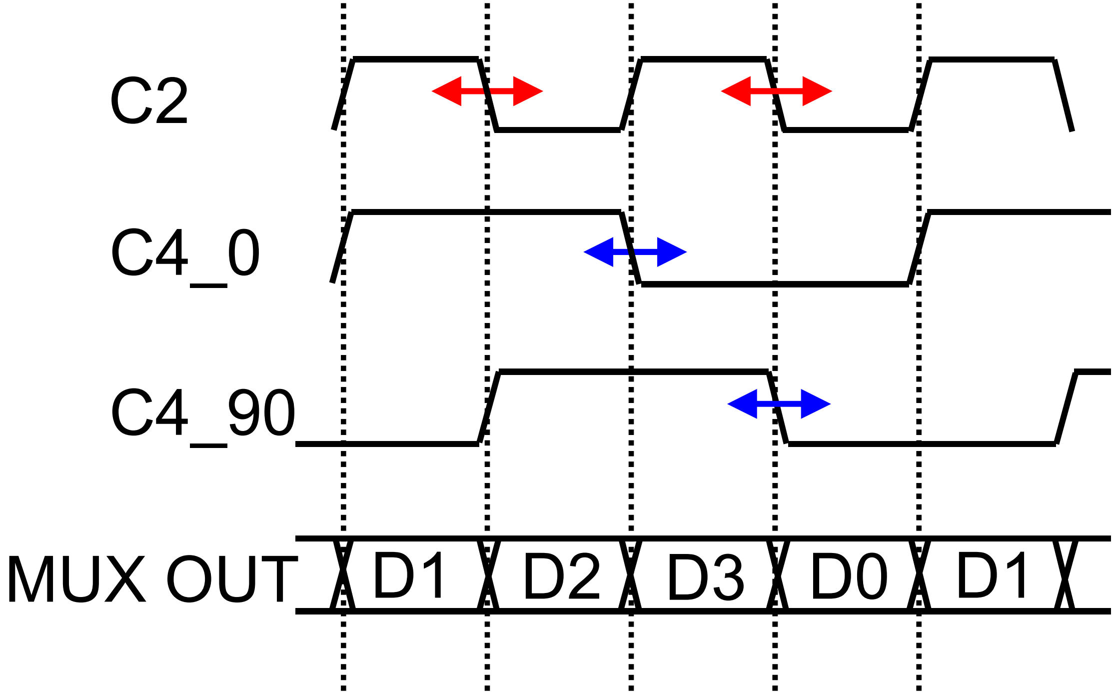




- header & footer devices for impedance fine tuning
- R = Rlin (74%) + Rmos (26%) (linearity)
- unit segment at 1/64R weight (bit 2)
- largest segment 16/64R weight (bit 6)
- custom scaled segments for 1/256 R and 1/128 R (bit 0,1)

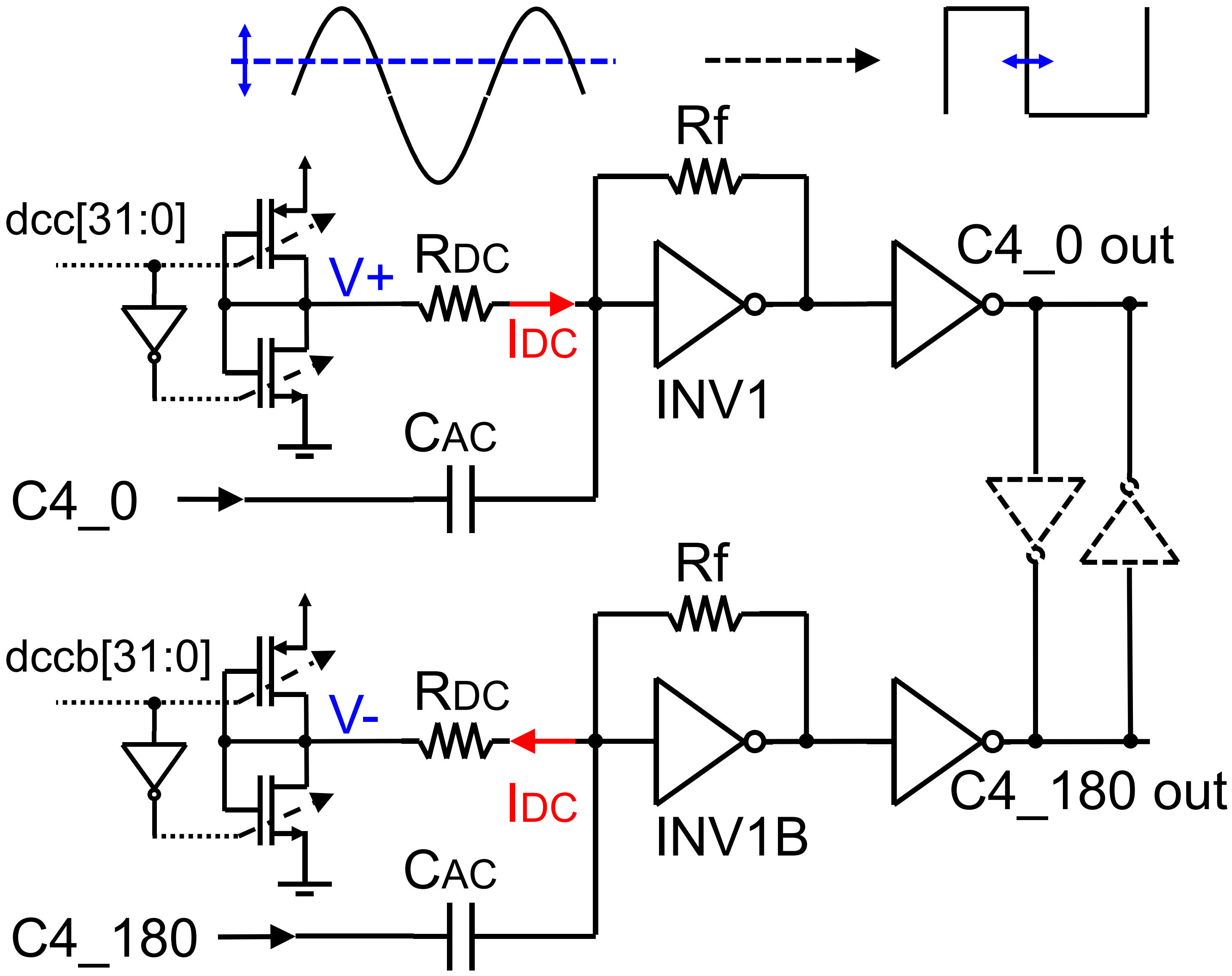
Quarter-Rate Clock I/Q & Duty-Cycle Correction





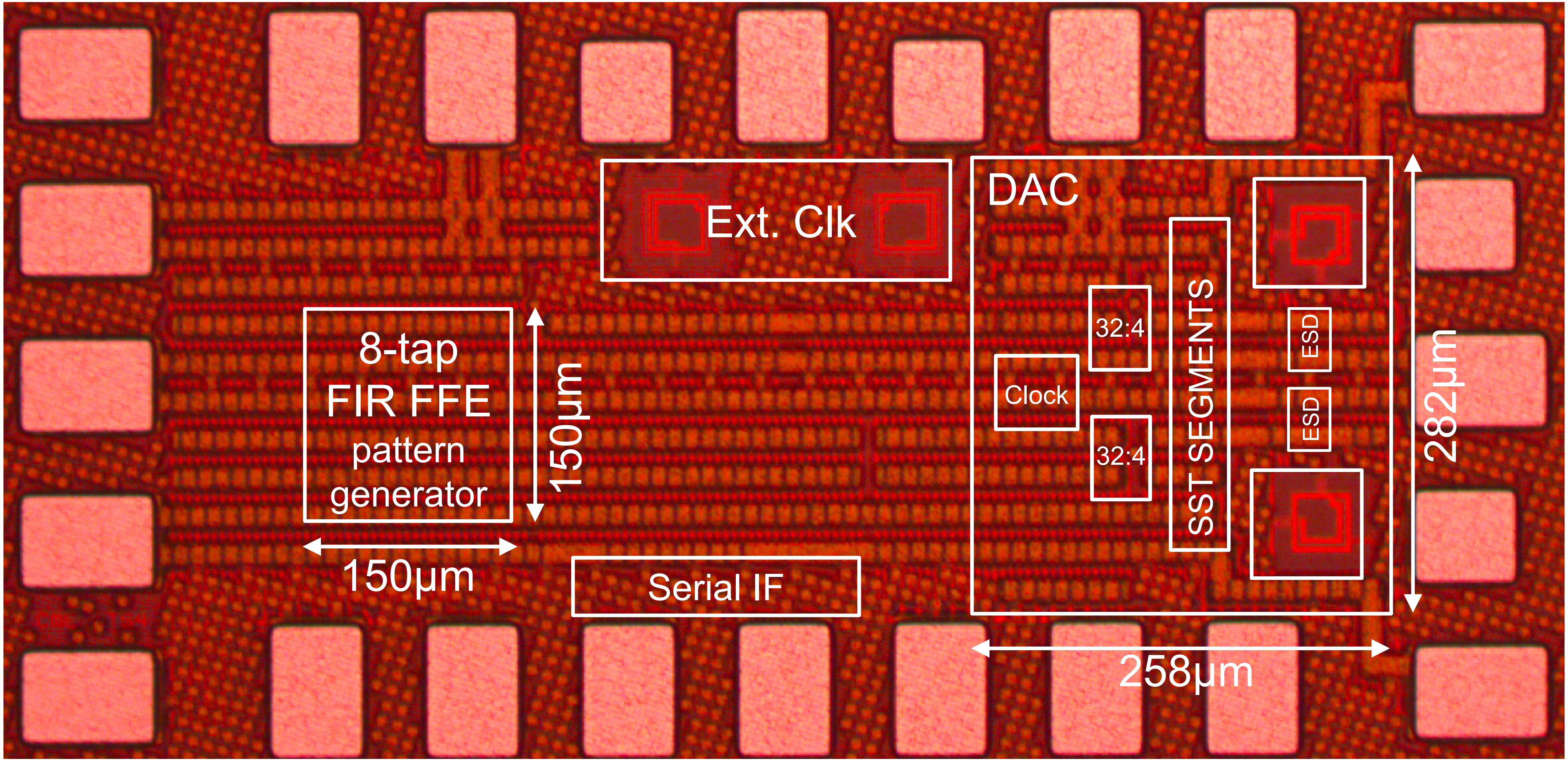
- Duty cycle of input clock C2 defines I/Q mismatch of divided C4 clocks
- 2 separate DCC's in C4_I and C4_Q clock path

Duty-Cycle Correction

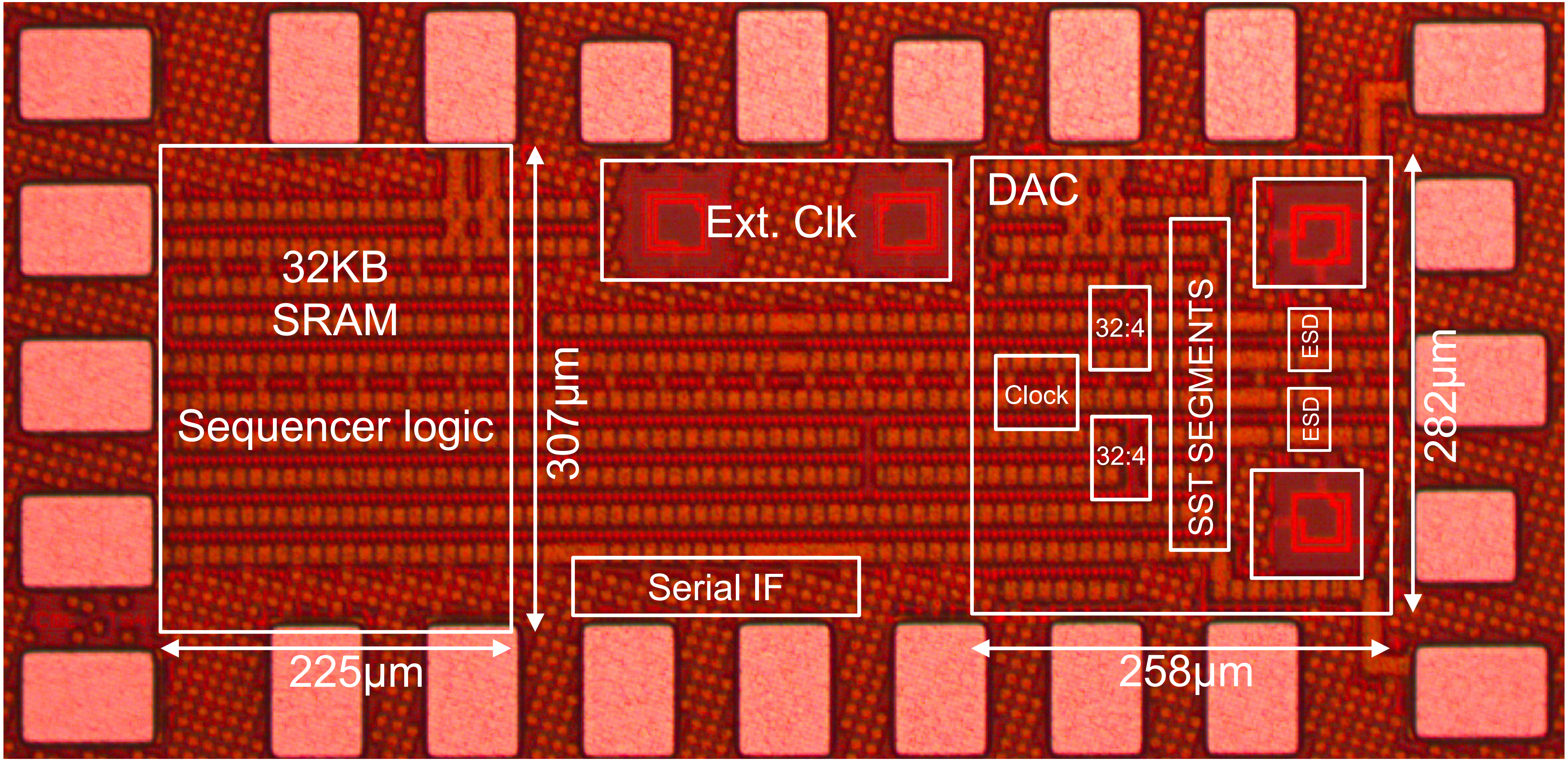


- INV1,INV1B biased at trip point (equal PMOS / NMOS drive strength)
- Clock path AC-coupled to INV1
- IDC injected at INV1shifts trip point and duty-cycle
- VDAC based on pull-up / pull-down MOS diodes (monotonic)
- RDC used to adjust tuning range

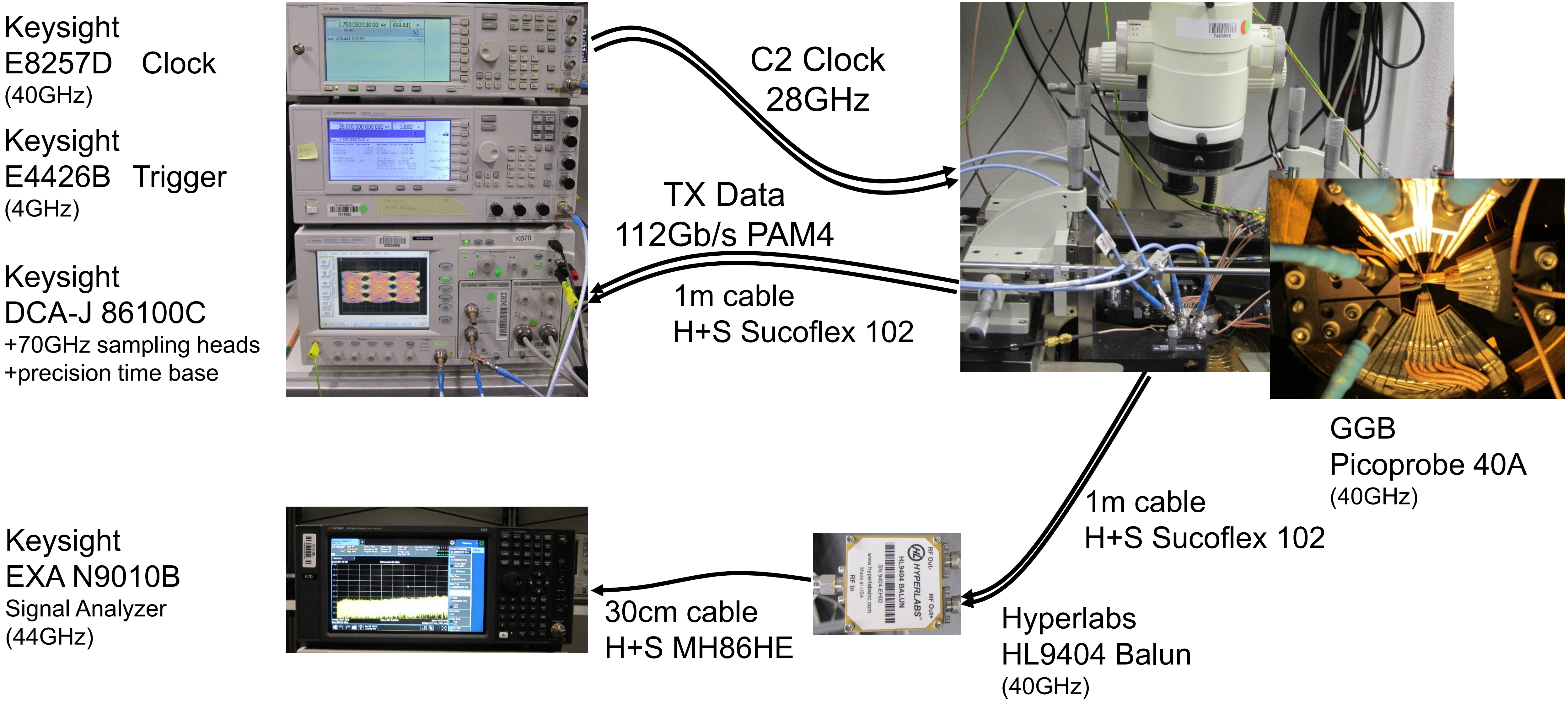
Chip Micrograph TX (1mm x 0.5 mm)



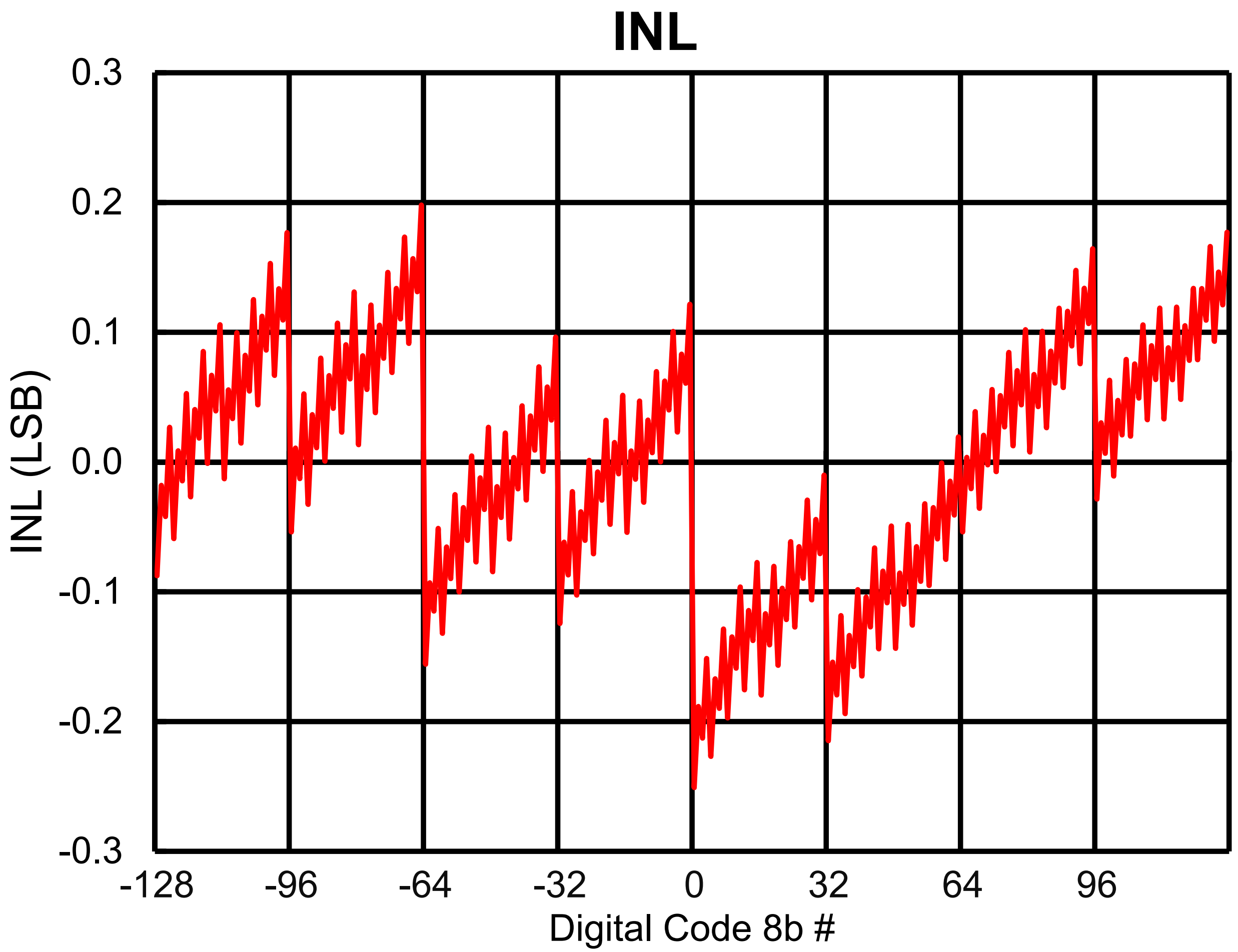
Chip Micrograph DAC Test Chip

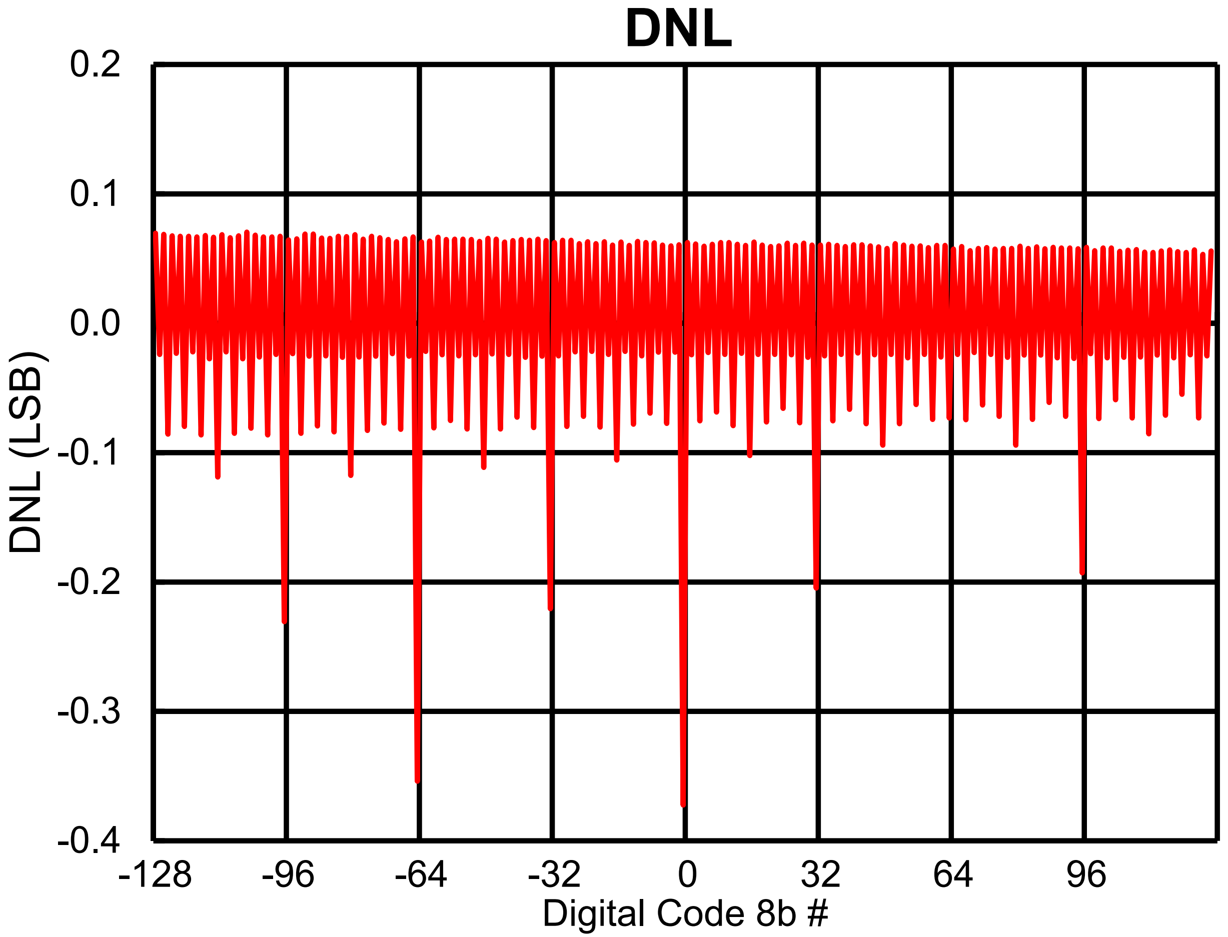


Measurement Setup

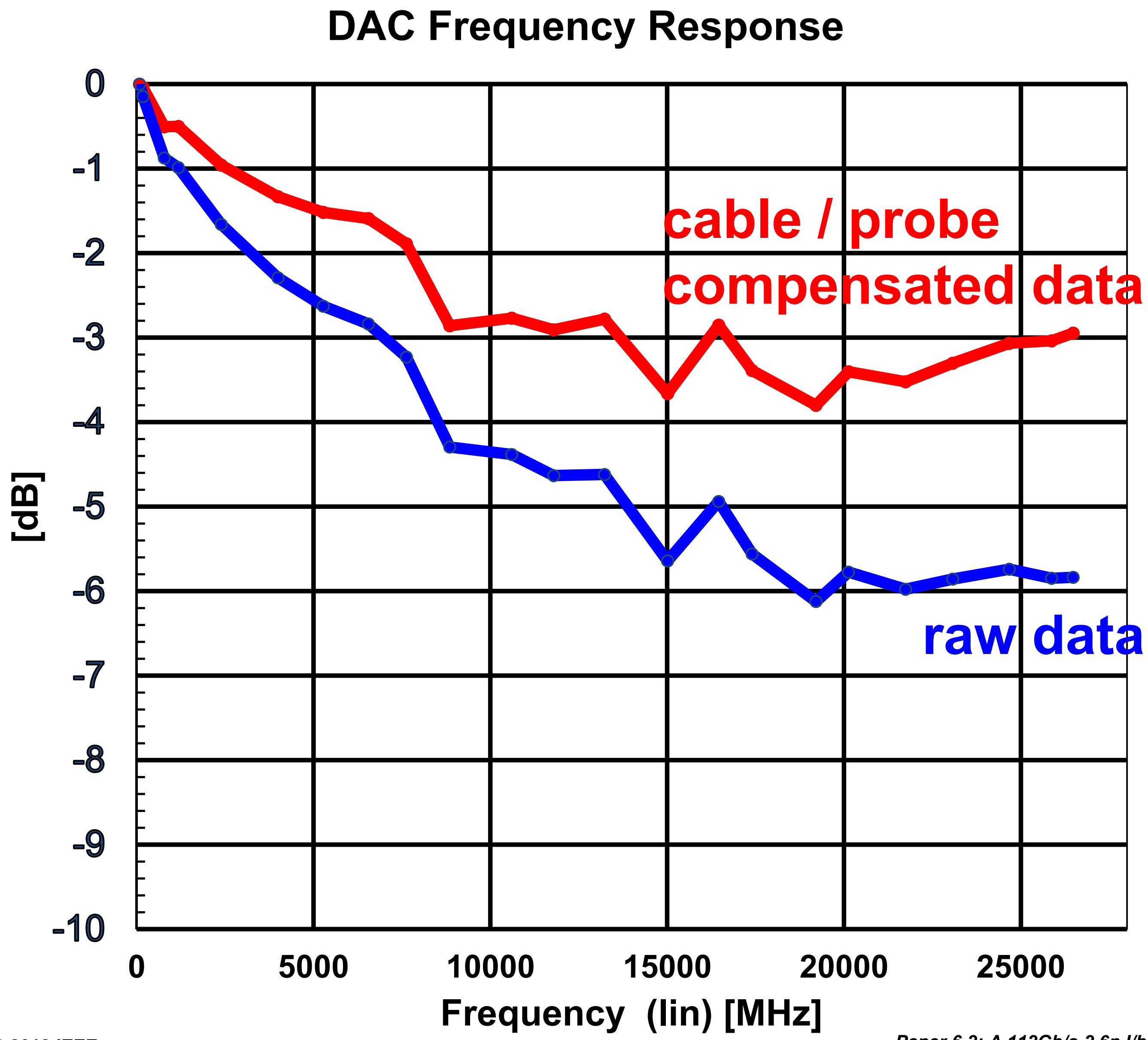


DAC INL/DNL


INL
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
INL (LSB)
-128
-96
-64
-32
0
32
64
96
Digital Code 8b #

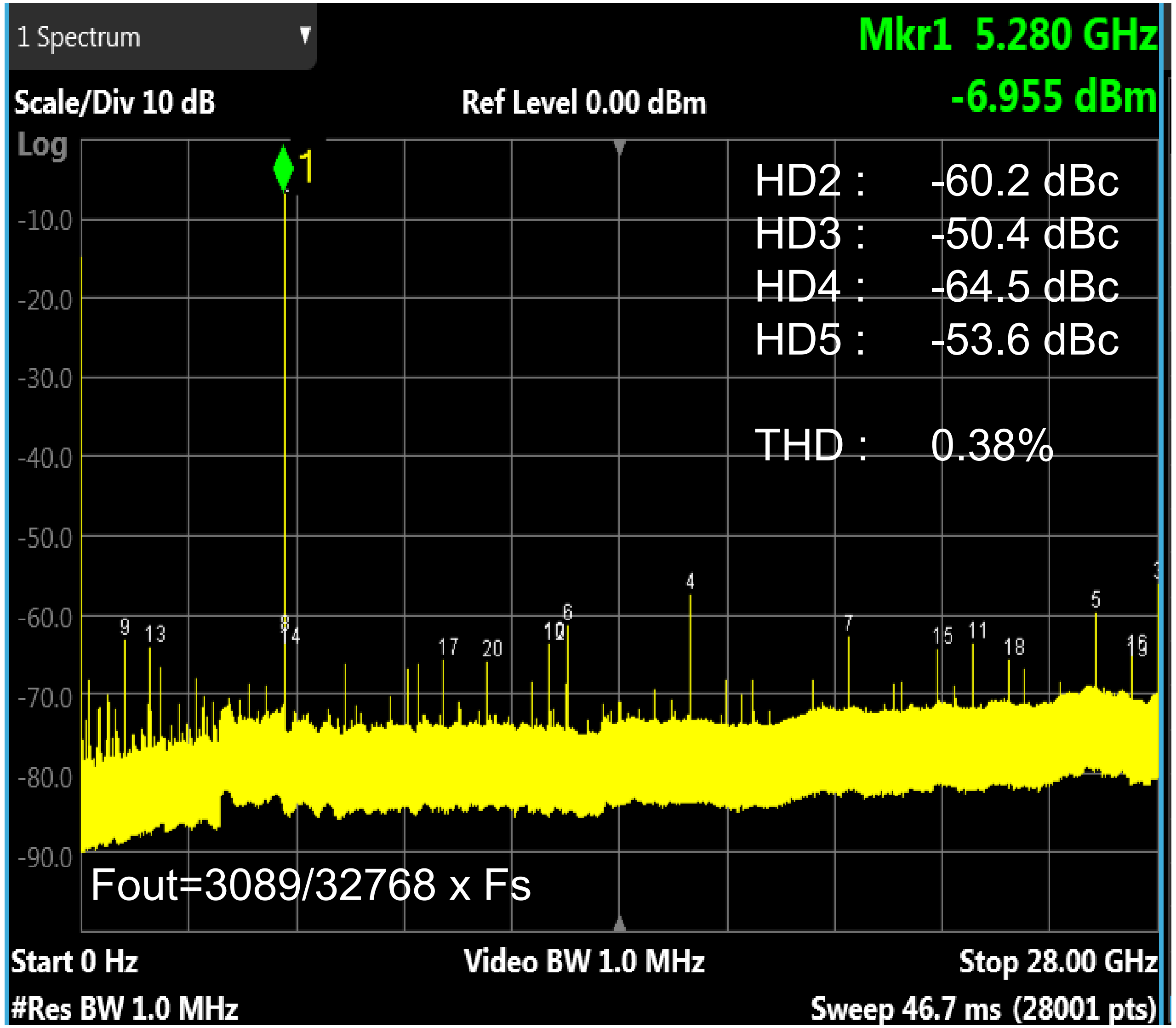

DNL
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
DNL (LSB)
-128
-96
-64
-32
0
32
64
96
Digital Code 8b #

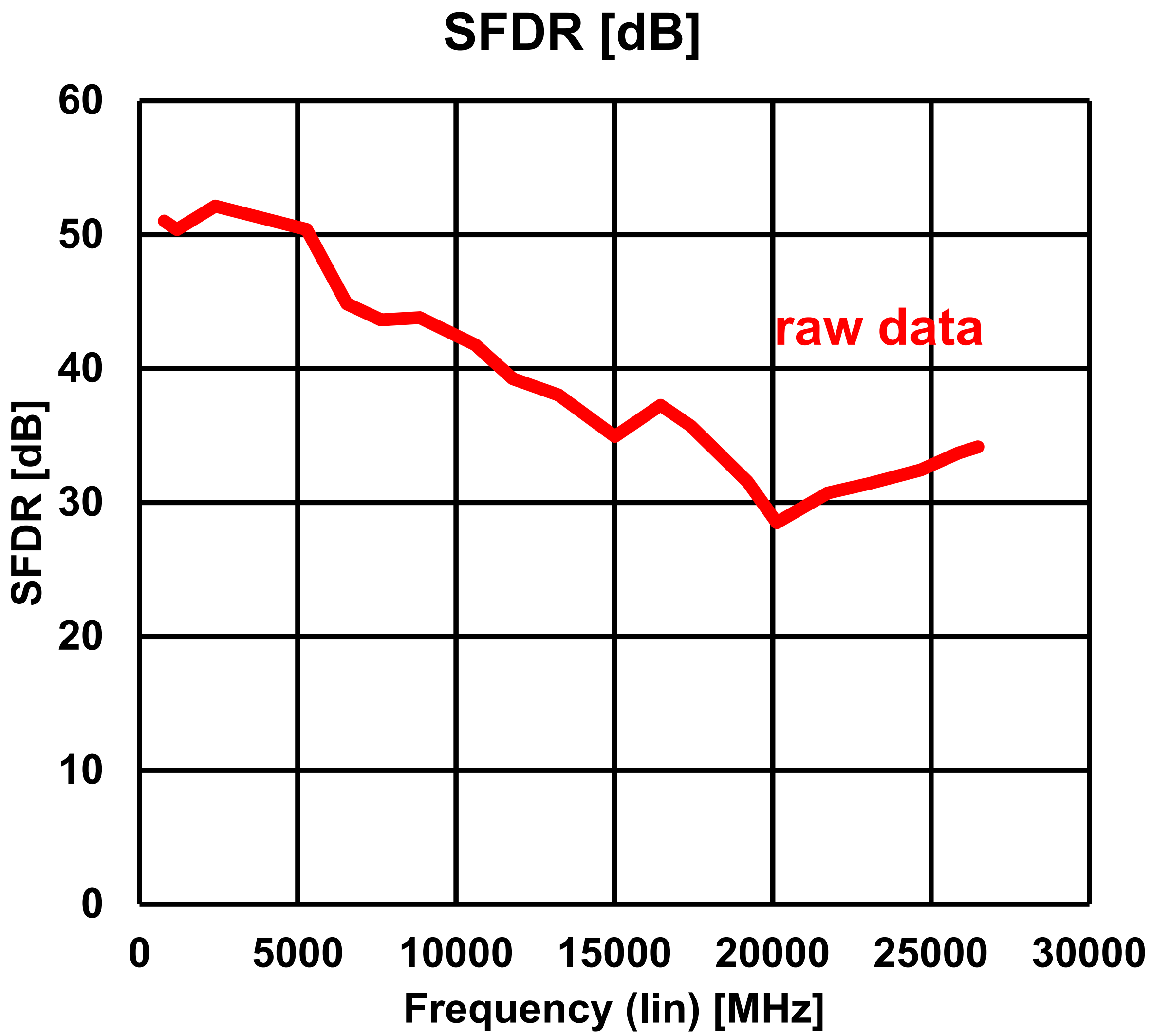
DAC Frequency Response



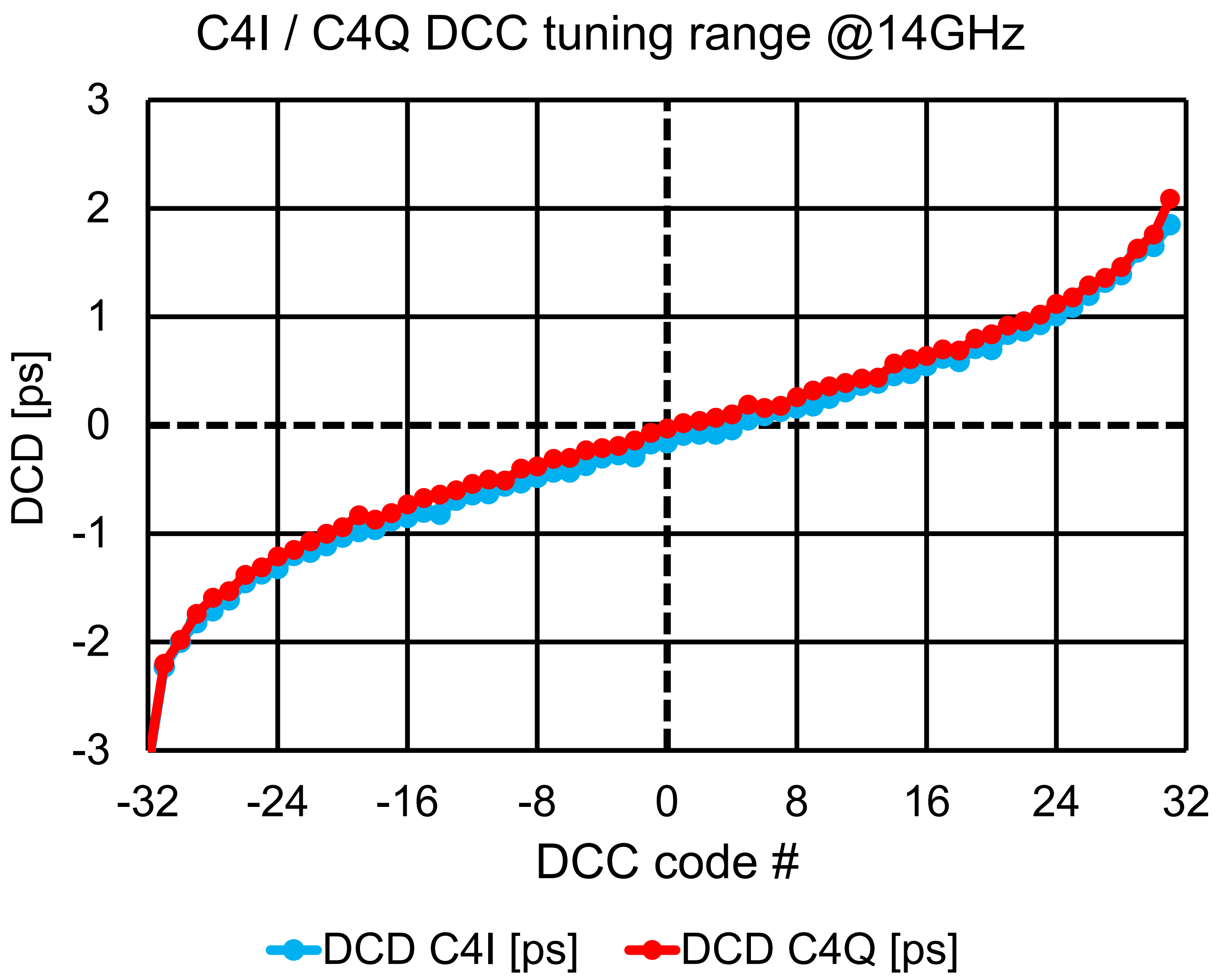
- Response measured with scope using synthesized sine waves at different frequencies (peak-to-peak values)
- 0dB corresponds to 920mVppd
- Compensation:
  - Cable : 1m H+S Sucoflex 102 (-2.2dB @25GHz)
  - Probe: GGB Picoprobe 40A (-0.65dB @25GHz)

DAC Spectrum & SFDR @ 56GS/s





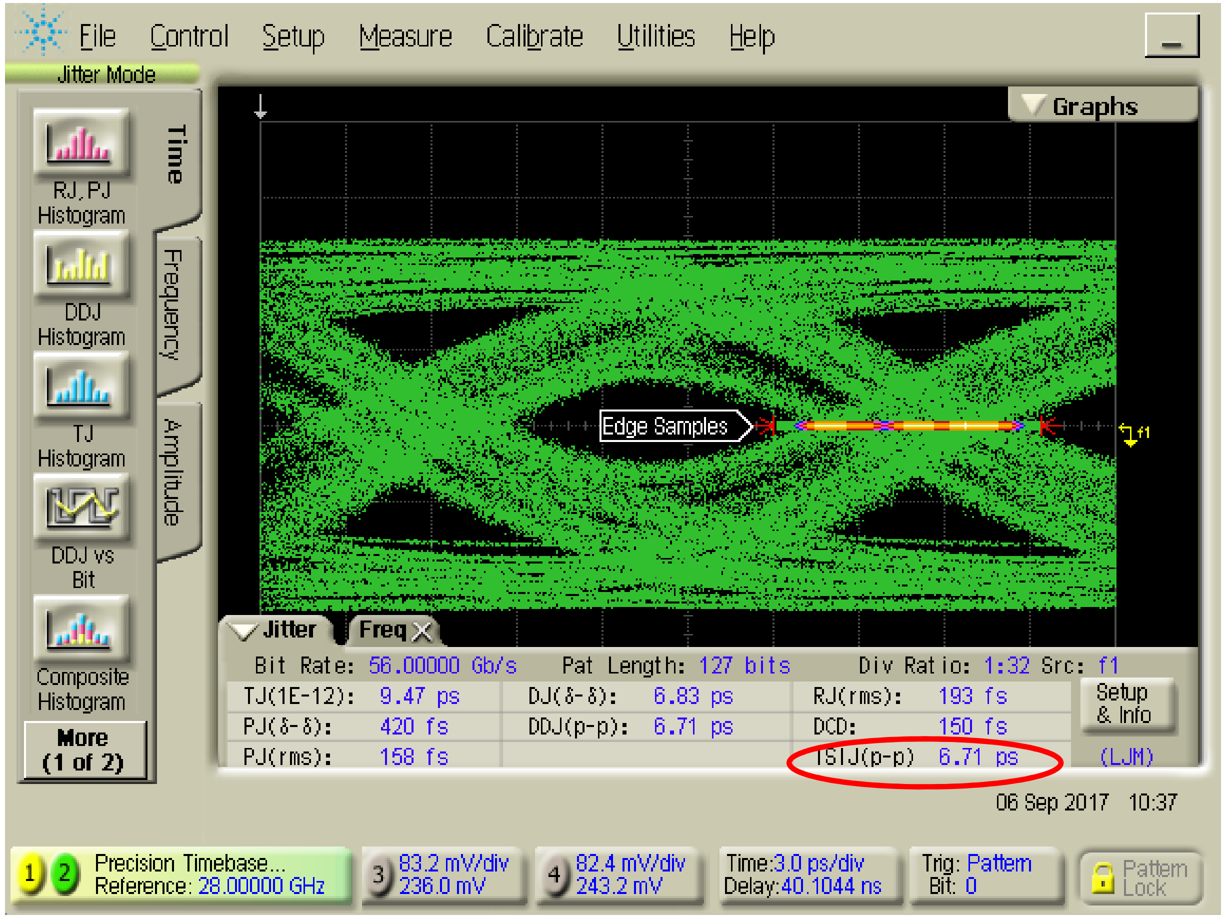
Quarter-Rate Clock DCC Correction



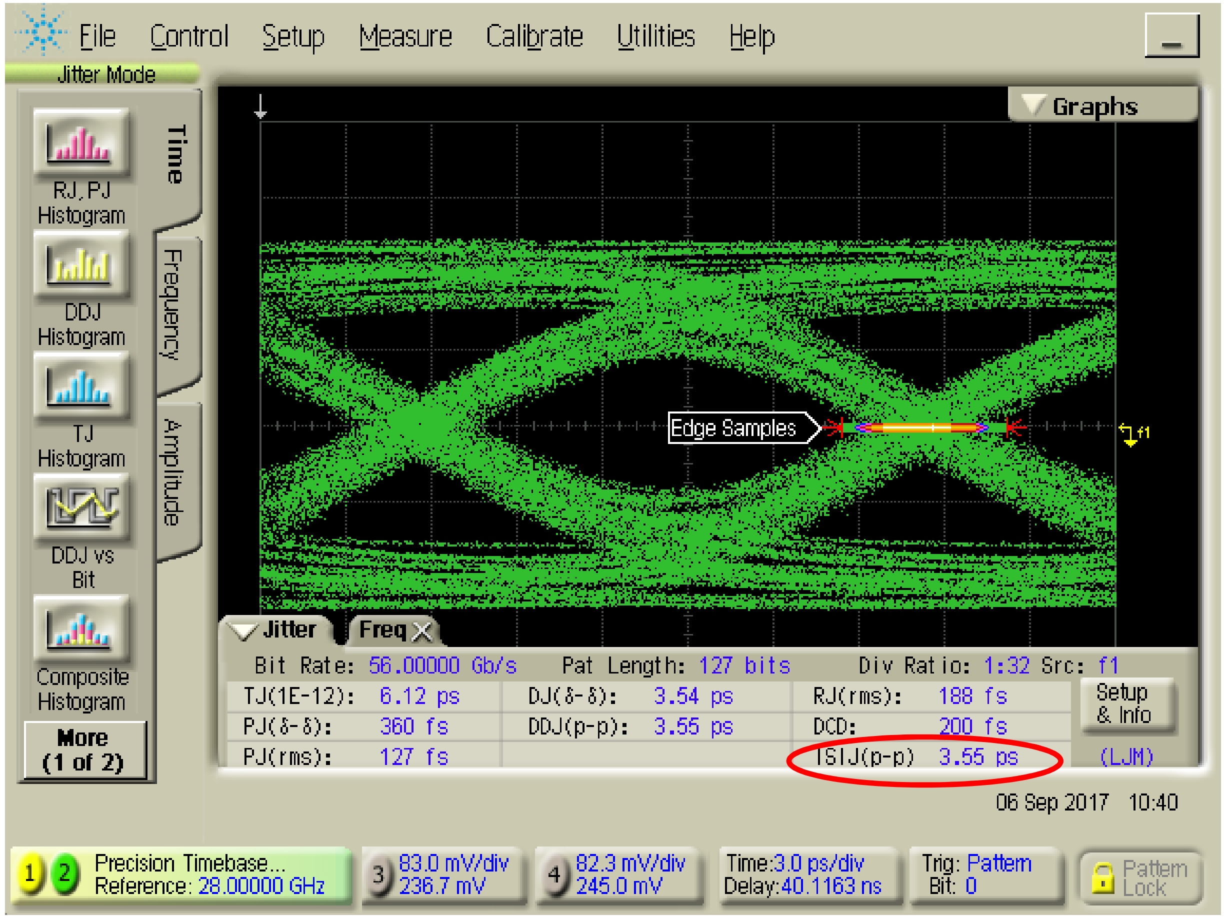
- Quarter-rate clock C4I,C4Q duty-cycle correction range +/- 2ps within 60 steps

Pre-Driver: No Peaking vs. Active Peaking

56Gb/s NRZ, no equalization, **no** peaking

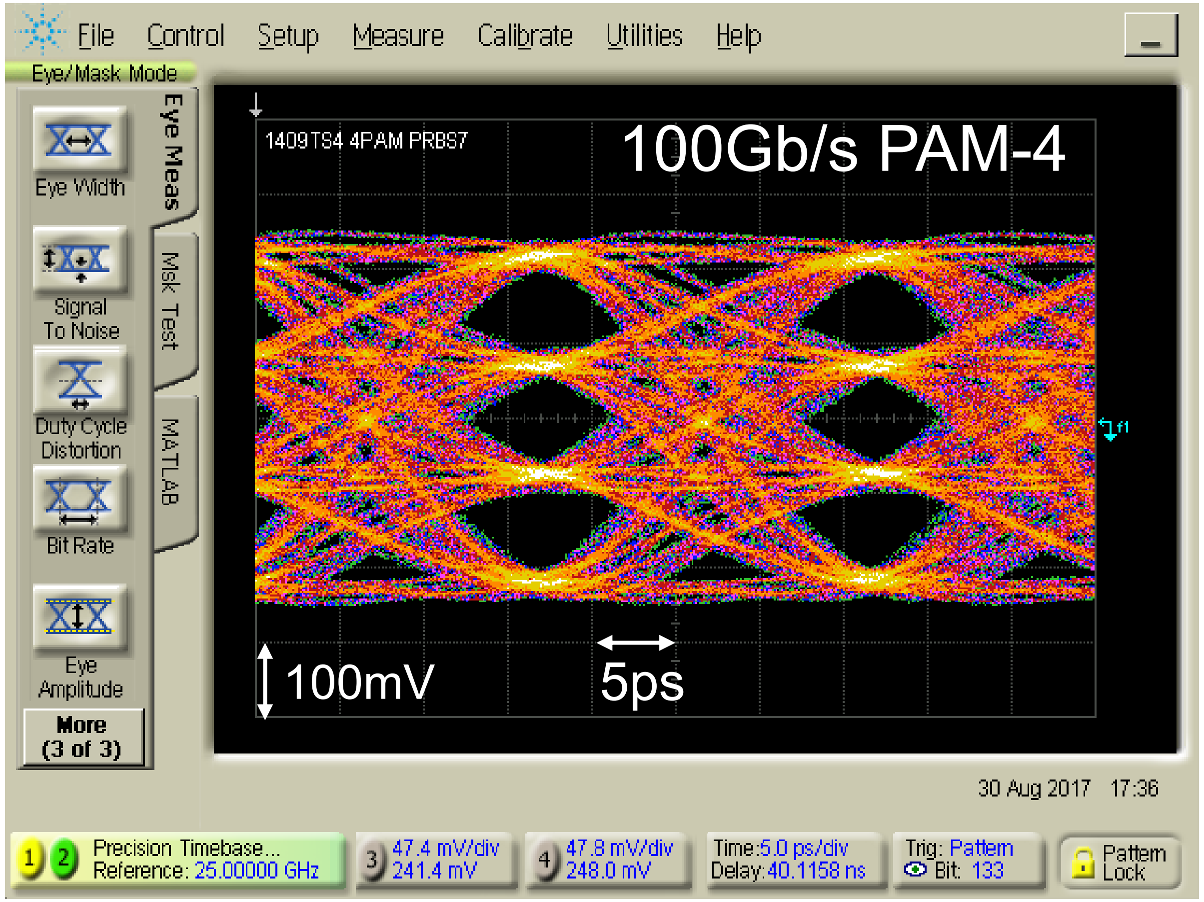


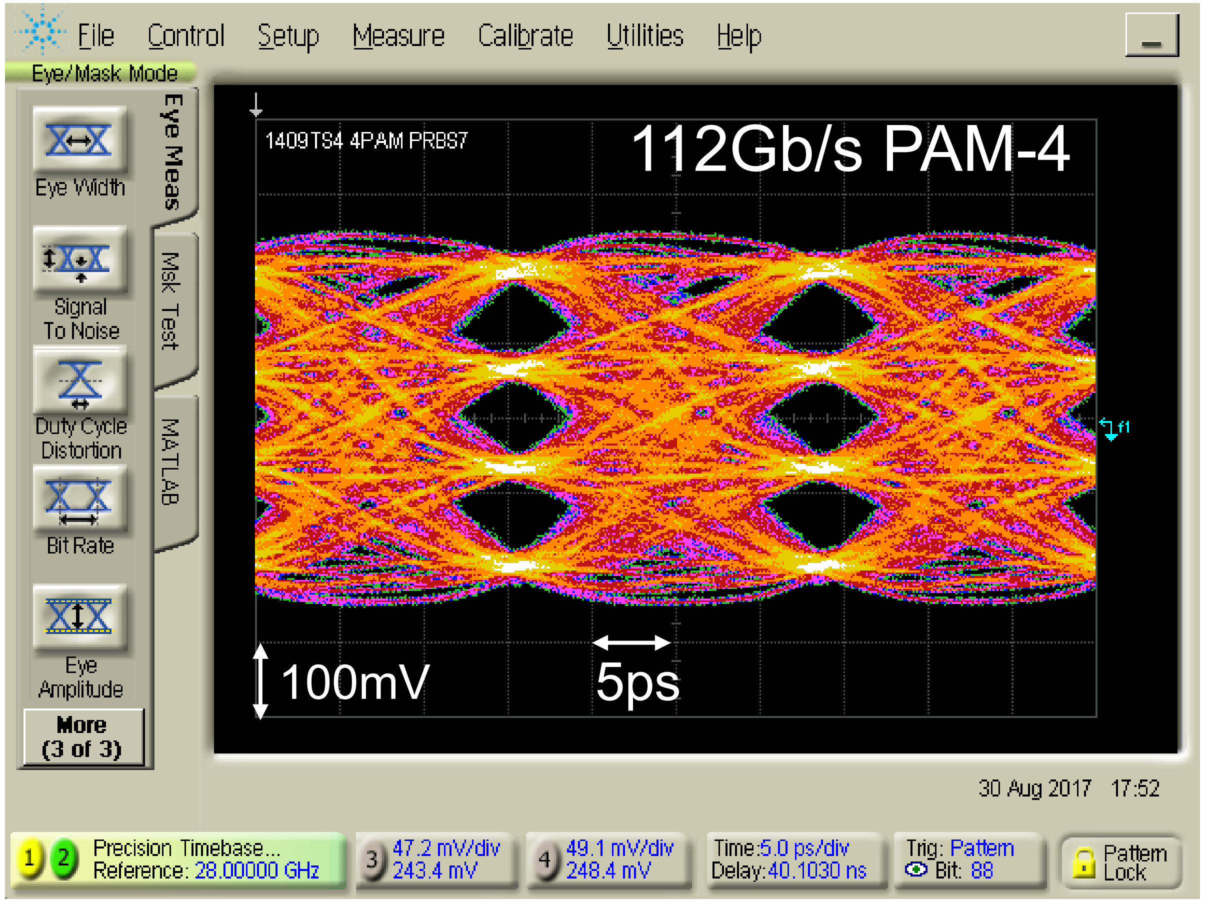
56Gb/s NRZ, no equalization, **with** peaking



- Active peaking in the pre-driver **improves ISI jitter by ~3.2ps**
- Power penalty is 20.9mW @0.95V supply

PAM-4 Data Eyes





Equalization: [0.005, -0.054, **0.733**, -0.118, -0.057, 0.005, -0.020, 0.008]

Equalization: [0.007, -0.072, **0.726**, -0.145, -0.034, -0.008, -0.005, -0.003]