A 35 mW 8 b 8.8 GS/s SAR ADC with Low-Power Capacitive Reference Buffers in 32 nm Digital SOI CMOS

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Abstract

An asynchronous 8× interleaved redundant SAR ADC achieving 8.8 GS/s at 35 mW and 1 V supply is presented. The ADC features pass-gate selection clocking scheme for time-skew minimization and per-channel gain control based on low-power reference voltage buffers. The sub-ADC stacks the capacitive SAR DAC (CDAC) with the reference capacitor to reduce the area and enhance the settling speed. It achieves 38.5 dB SNDR and 58 fJ/conversion-step with a core chip area of 0.025 mm^2 in 32 nm CMOS SOI technology.

Introduction

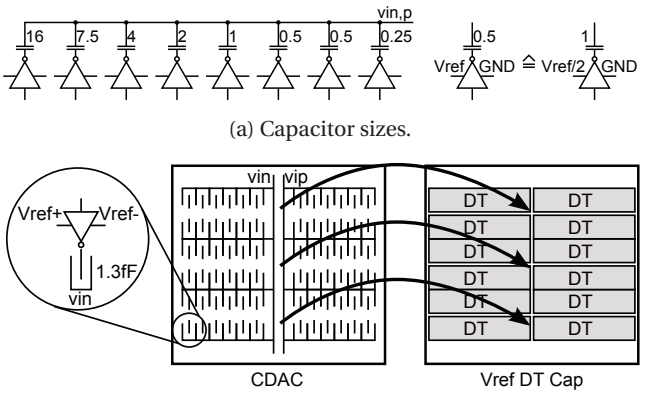
Next-generation high-speed links will require power- and area-optimized ADCs with more resolution than flash ADCs can provide to address higher order signal demodulation. SAR ADCs are very attractive for power-efficient converters and offer an excellent topology for deep submicron digital CMOS processes as no operational amplifiers are required. Only very few designs have explored the range above 4 GS/s.

The design presented here requires no input buffer, features a low-power voltage reference buffer with individual gain-control of each sub-ADC with a fine-grain, robust R-3R ladder [1] and a low-skew clock-generation scheme.

ADC Architecture

The ADC runs at 8.8 GS/s and is based on interleaving 8 SAR ADCs with alternating comparators for enhanced speed [2]. The SAR conversion is redundant with an optimized CDAC as shown in Fig. 1a, which relaxes the settling-time requirement from > 99% to 94%. The CDAC is based on a custom metal structure in the lower metals and placed on top of the reference deep-trench (DT)/DRAM capacitors, *Cref*, to save chip area and optimize settling speed, see Fig. 1b. The high CDAC settling speed is based on the large 80 pF *Cref* and a low-ohmic connection from CDAC to *Cref*.

Each sub-ADC receives its own master reference voltage, which is digitally set by a minimum-size 11 b R-3R ladder, assuring a step size of < 0.1% *Vref* without missing codes, see Fig. 2. The calibration algorithm is external and based on an 11-step binary search from MSB to LSB to set the on-chip R-3R ladders. The master reference voltage *Vmaster* is buffered with a clocked comparator circuit to recharge *Cref*. *Vmaster* is compared with *Vref* in each sub-ADC at the end of the SAR cycle, and charge is added to *Cref* if necessary. Using a simple resistive divider instead of the circuit in Fig. 2 would result in *Vref* being dependent on the input signal and sensitive to temperature variations.



(a) Capacitor sizes.

(b) Layout with underlying DT capacitors.

Fig. 1. CDAC [2].

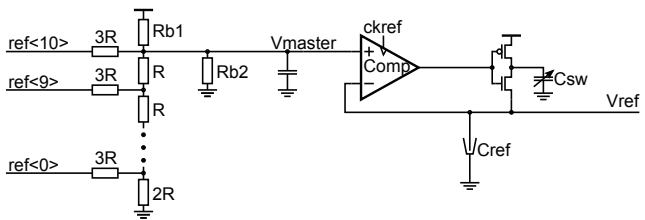


Fig. 2. Reference buffer and R-3R ladder for gain control.

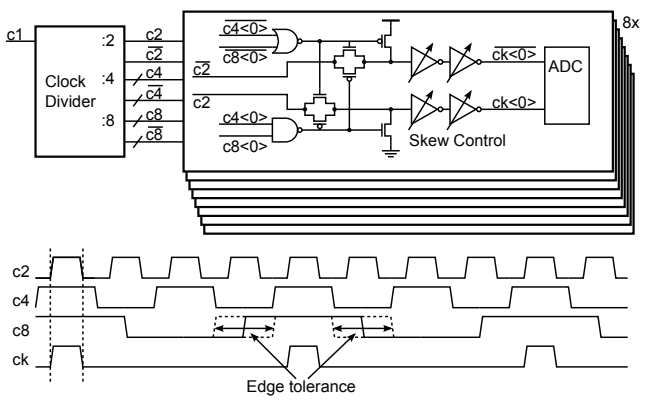


Fig. 3. Clock distribution.

The low input capacitance of 128 fF per side in the sub-SAR ADC, a short tracking window of 1/8 period and a small number of sub-ADCs enable a low input capacitance and therefore render an input buffer unnecessary. In addition, a very small sub-ADC design ensures a short routing distance to keep the parasitic resistance and capacitance small and

wire mismatch in the data and clock lines negligible.

The clocking circuit in Fig. 3 is optimized for low skew by using only one 4.4 GHz clock $c2$ and its inverted signal $\overline{c2}$ to sample the signal. Pass gates controlled by clocks $c4$ and $c8$ are used to enable one ADC at a time. The edge tolerance serves to reduce the number of $c8$ clocks required. Skew control based on current starved inverters allows clocks ck and $\overline{ck}$ to be shifted by up to 3.5 ps in steps of < 250 fs. The layout of the data input and of the $c2$ clocks is strictly symmetrical and shielded to match the capacitance, resistance and inductance of each branch.

Measurement Results and Conclusions

The ADC nominal full-scale input is 500 $mV_{pp,diff}$. The $Vmaster$ tuning range is 250−500 mV and is nominally set to 380 mV. The ADC operates from a single 1 V supply, but tolerates a supply range from 0.8 to 1.2 V. The measured total power consumption of 35 mW at 1 V and 8.8 GS/s consists of 6 mW for clock generation and 29 mW for the 8 sub-ADCs.

Figure 4 plots ENOB vs. input frequency at 8 GS/s sampling frequency. ENOB is limited by thermal noise. The skew compensation was not tuned for flat ENOB. The amplitude vs. input frequency plot in Fig. 4 shows a 3 dB bandwidth of 4.2 GHz. All 3 samples are from a typical process corner.

Figure 5 gives the spectrum of a typical sample at 3.81 GHz input frequency achieving 48.7 dB SFDR with the input amplitude set to reach −1 dBFS.

The measured DNL is below 0.71 LSB and INL below 0.88 LSB, see Fig. 6, i.e. very similar to DNL/INL of a single SAR ADC [2]. INL exhibits a small systematic mismatch resulting from the layout of the CDAC for the MSB and the MSB-1 capacitors. Table I compares the performance of ADCs [3, 4, 5]. A FOM of 58 fJ/conversion-step is found at 1.0 V supply and 8.8 GS/s based on ENOB at low frequency. The sampling frequency is above 10 GS/s at 1.1 V supply for all measured samples. The ADC was manufactured in a 32 nm SOI CMOS process with a core area of 130 μm × 195 μm, see Fig. 7. In summary, the design presented has a 28× smaller FOM, a 12× smaller area and 9× smaller power consumption than previously reported 6 b+, ≥ 4 GS/s CMOS ADCs [6].

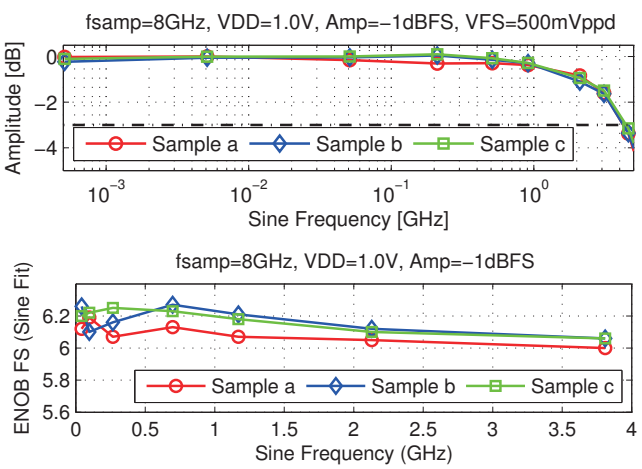


Fig. 4. ENOB vs. input sine frequency. Amplitude at each frequency adjusted to -1dBFS.

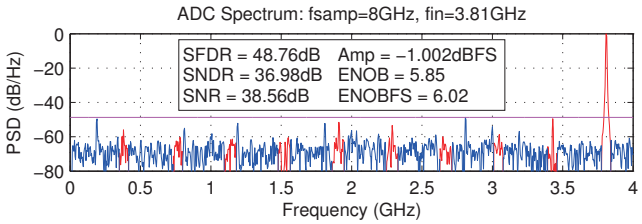


Fig. 5. Power spectral density for a 3.81 GHz input signal.

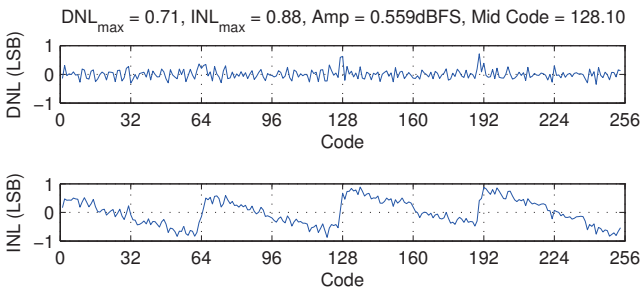


Fig. 6. INL and DNL.

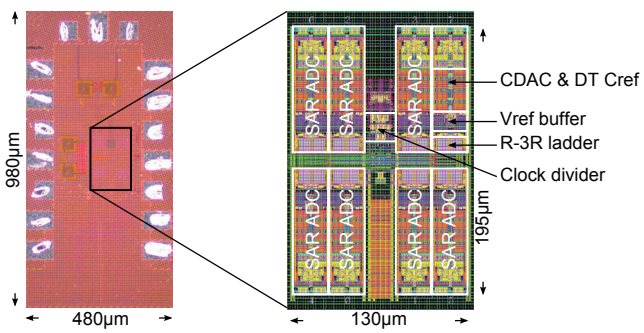


Fig. 7. Chip micrograph and layout view.

Table I. Performance comparison.

Specifications	[3]	[4]	[5]	This work	
Architecture	Flash	Ti-Pipeline	Ti-Flash	Ti-SAR	
CMOS Technology (nm)	65	90	65	32	
Resolution (bits)	6	6	6	8	
Supply Voltage (V)	1.3	-	1.5	1.0	1.1
SNDR (dB)	32	36.6	30.8	38.5	38.5
Sampling Speed (GHz)	5	10.3	16	8.8	10
Number of Channels	1	8	8	8	
Power (mW)	320	1600	435	35	49
FOM (fJ/conv. step)	1970	2790	2600	58	71
Area (mm^2)	0.3	-	1.47	0.025	

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