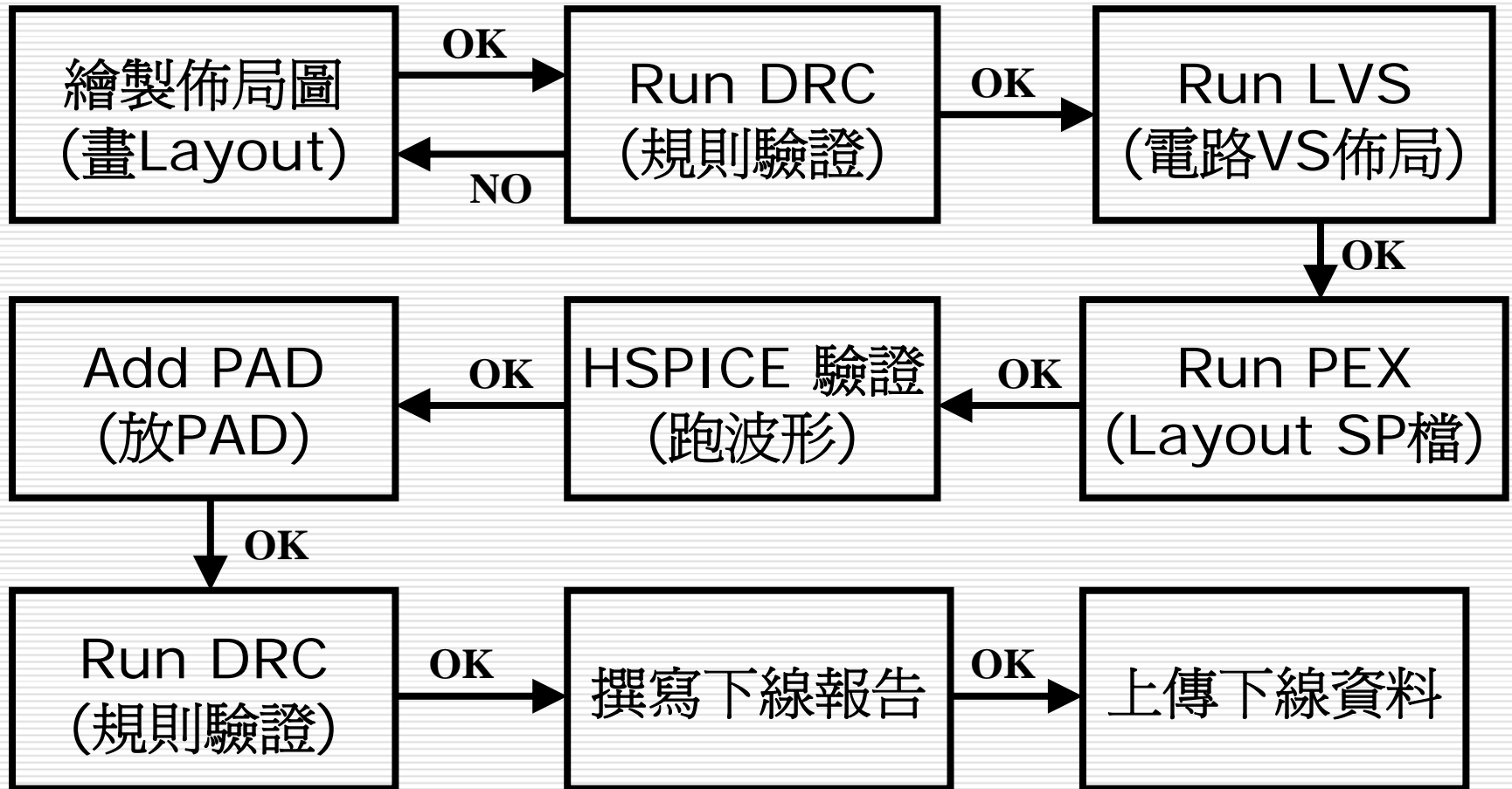


Post-Simulation 教學手冊 (Calibre部分)

目錄

- **Post-Simulation**流程
- **Prepare Files**
- **Layout editor environment setup**
- **DRC**
- **LVS**
- **PEX**

Post-Simulation 流程



Prepare Files

035ms.tf	Technology file for design rule
DRC	Design Rule Check
LVS	Layout vs Schematic
RC_Ex	Post layout extraction
cds.lib	
.cdsinit	
.cshrc	
display.drf	

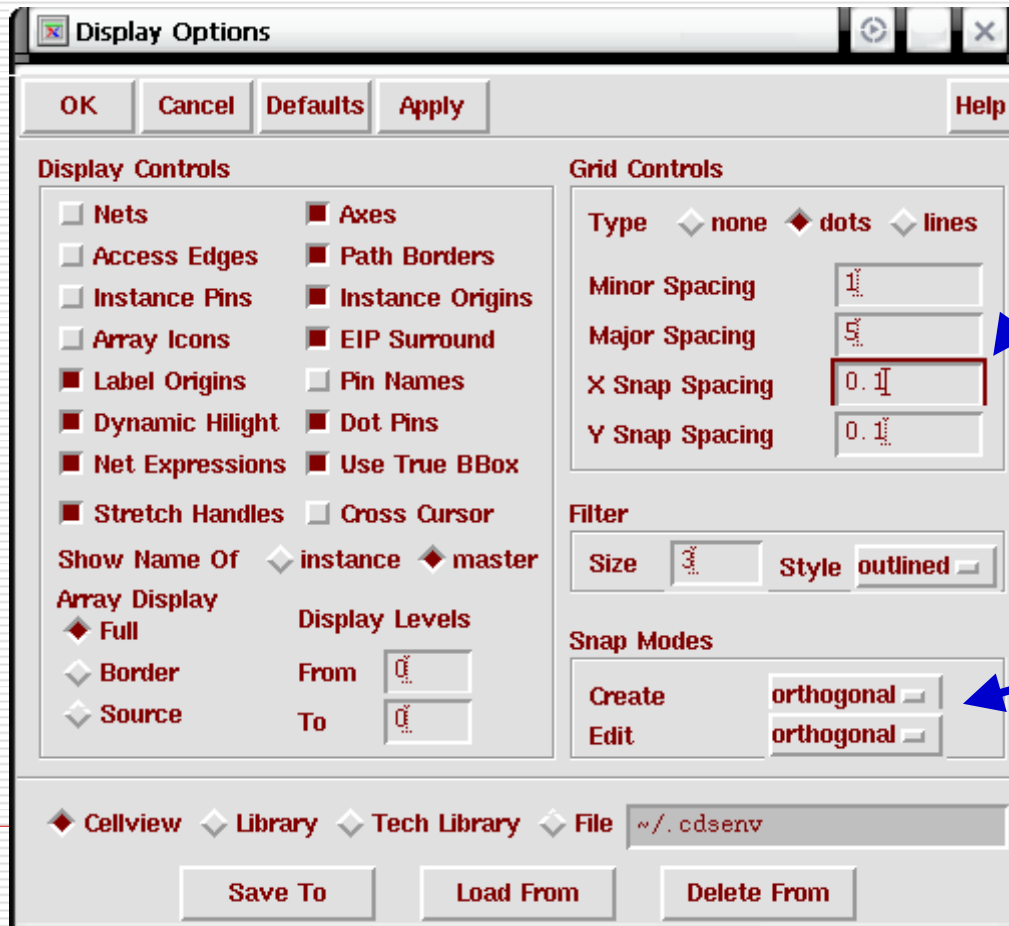
Prepare Files

檢查2p4m資料夾中是否有這些檔案和資料夾

035ms.tf	
cali035pMMSV_2P4M.lvs	For LVS
CM35P5_4M.23a.2	For DRC
display.drf	
mm0355v.l	
TSMC352P4MCalibre.pex2	For PEX

Layout editor environment setup

Options → Display

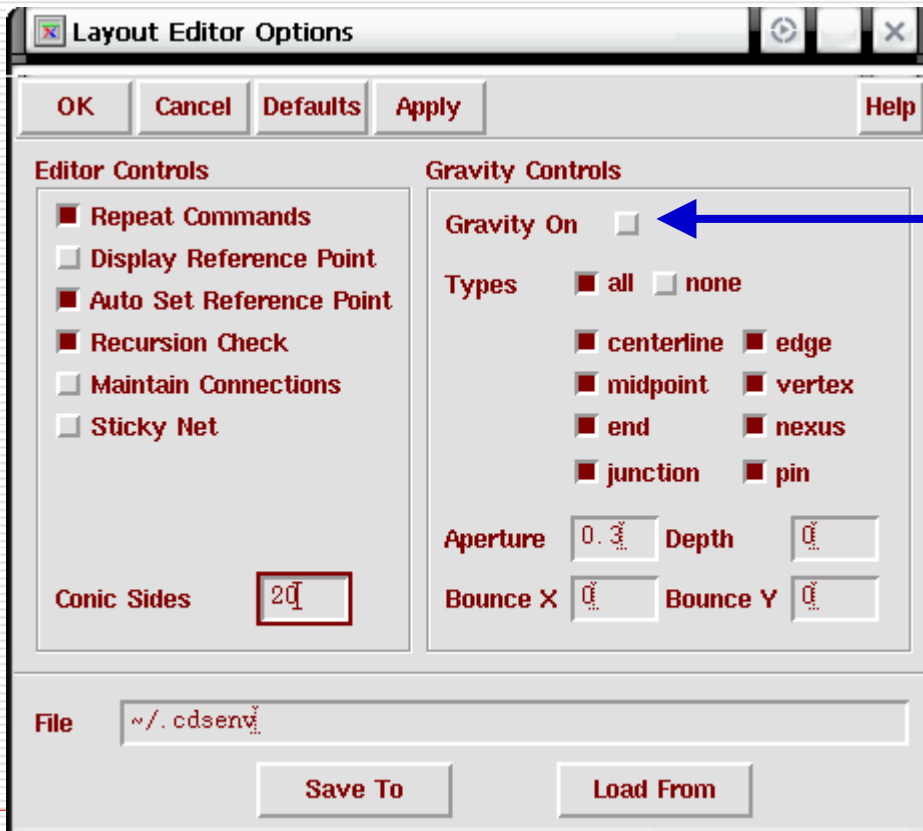


X(Y) Snap Spacing :
X(Y) 軸移動的最小間距，
通常是 **0.05**

Snap Modes
視情況選擇適當設定

Layout editor environment setup

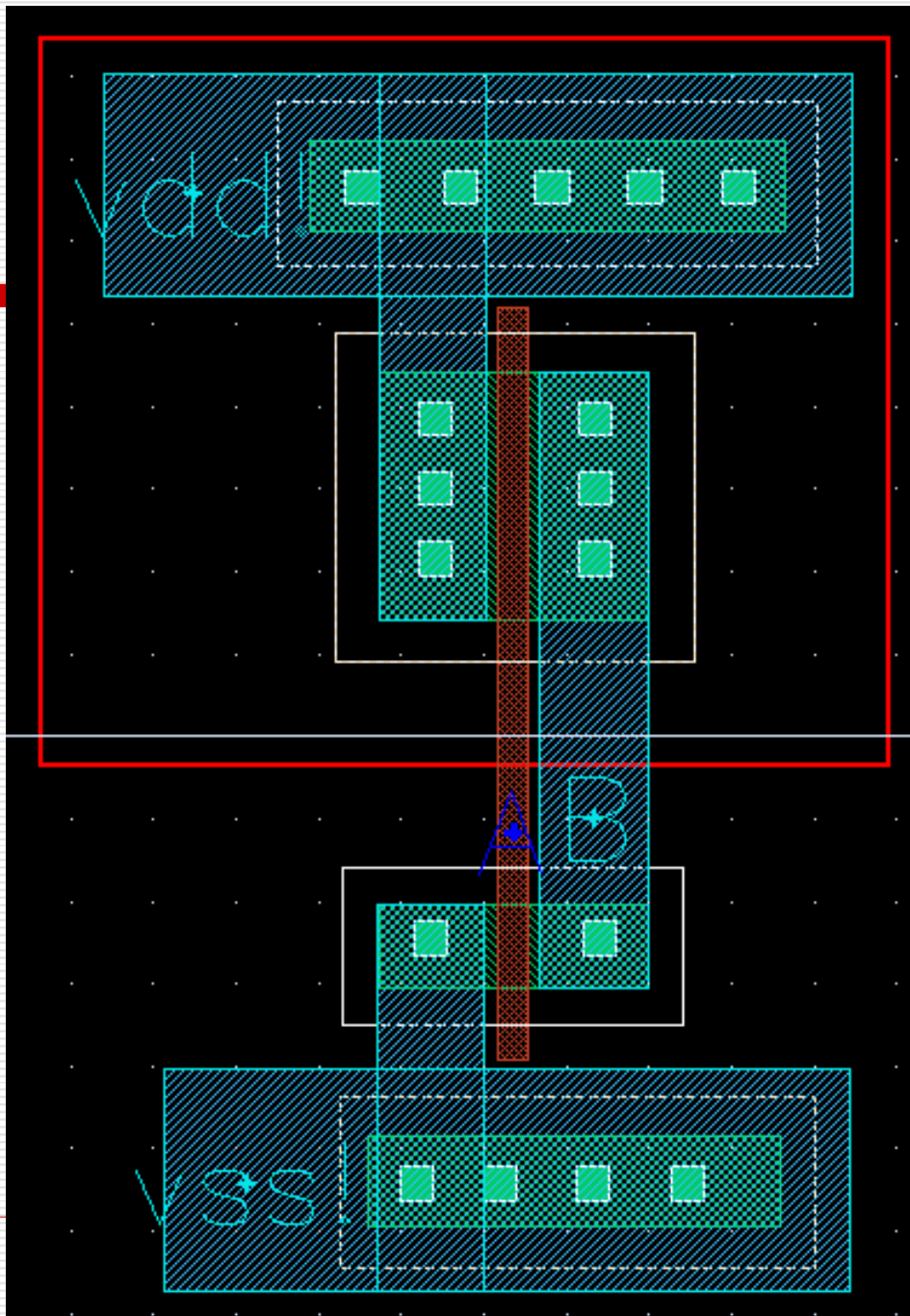
□ Options → Layout Editor



當遊標靠近 **object** 時
即被吸到 **object** 邊緣
(建議取消)

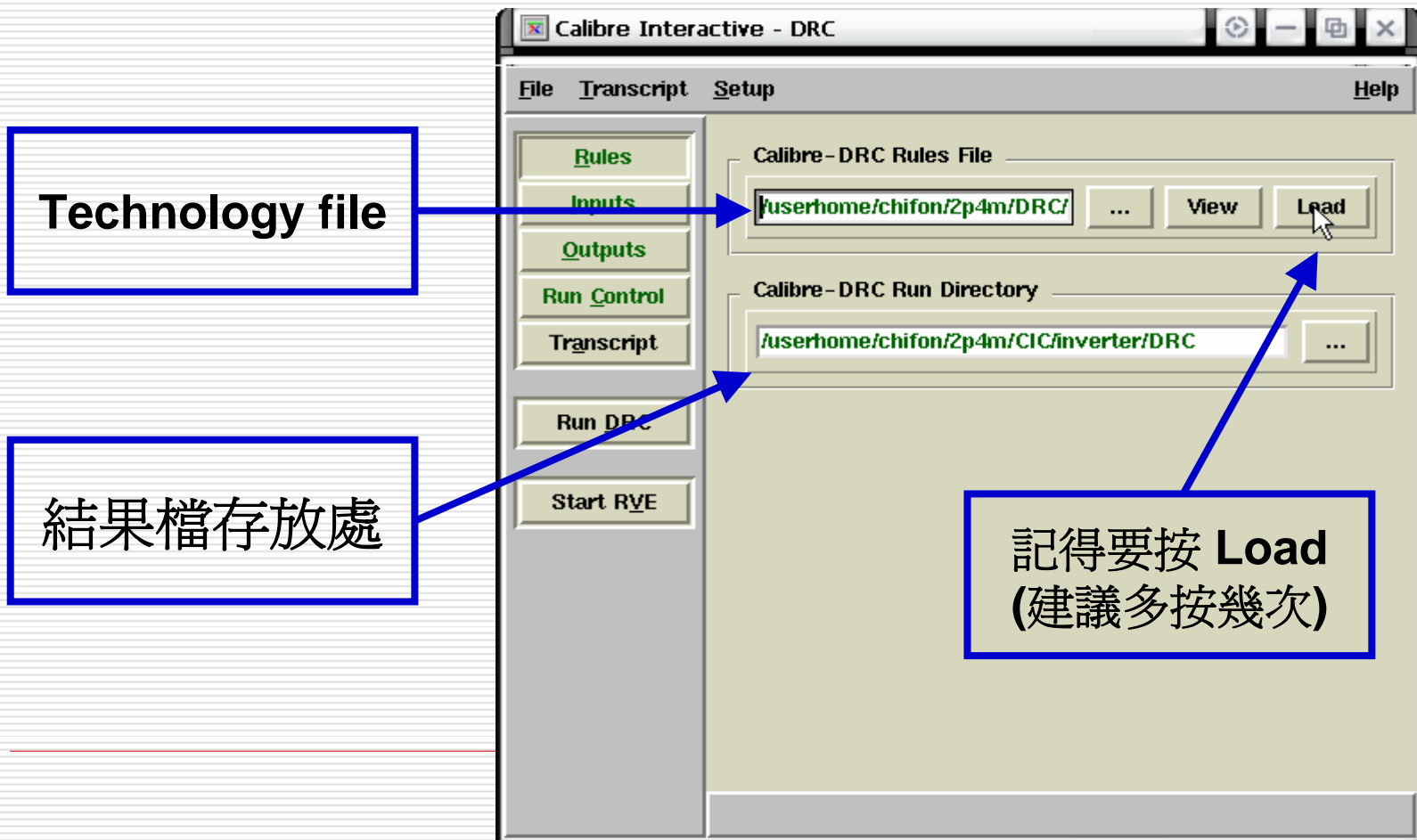
Layout's Hot Key

F2	save	f	fit all
m	move	c	copy
s	stretch	del	delete
u	undo	i	create instance
o	create contact	^p	create symbolic pin
z	zoom	r	rectangle
k/K	ruler/clear all ruler	l	label
q	properties		



DRC (Design Rule Check)

❑ Virtuoso Layout 視窗 → Calibre → Run DRC → Rules

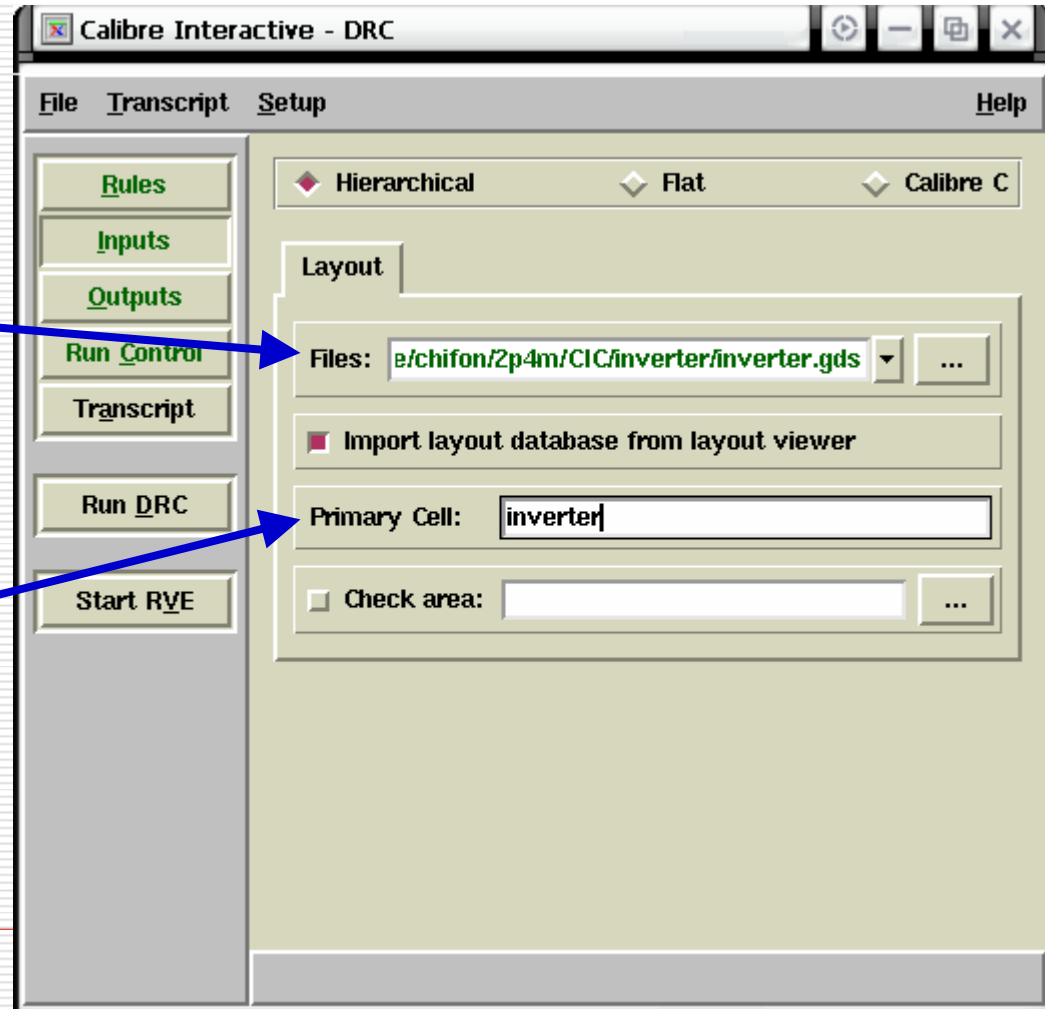


DRC (Design Rule Check)

□ Inputs

Layout gds file

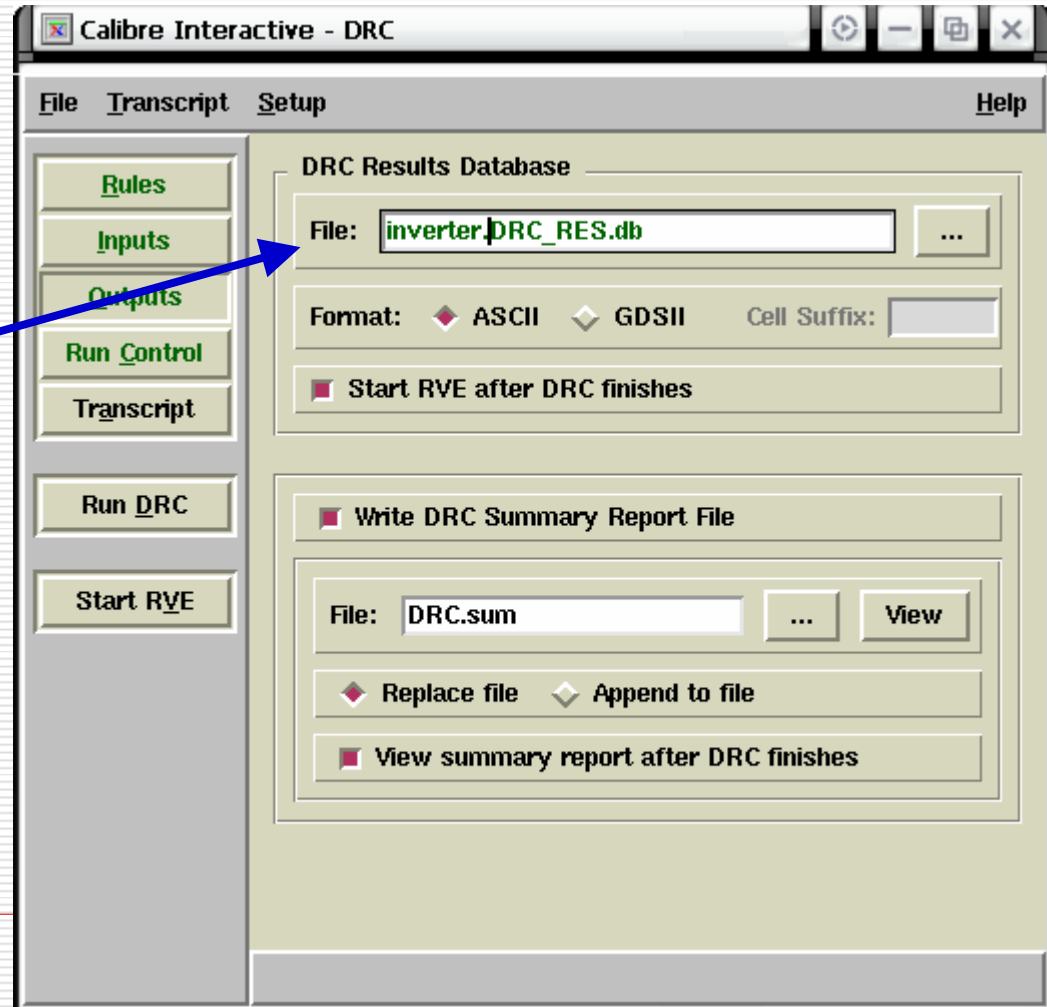
輸入 Cell Name



DRC (Design Rule Check)

□ Outputs

輸入 **Cell Name**
(此步驟可省略)



DRC (Design

□ 按下 Run DRC

The screenshot displays the Calibre DRC interface. The main window, titled "Calibre - DRC RVE : inverter.DRC_RES.db", shows a tree view with a green checkmark and the text "No Errors in 0 Checks" and "Cell inverter". Below this, a "Checktext" field is empty. The status bar at the bottom indicates "Cell inverter : 0 Errors".

An overlaid window titled "DRC Summary Report DRC.sum" displays the following text:

```
=====  
=== CALIBRE::DRC-H SUMMARY REPORT  
===  
Execution Date/Time:   Fri Apr 1 15:33:47 2005  
Calibre Version:      v9.1.7.5   Wed Oct 9 10:08:59 PDT 2002  
Rule File Pathname:   _CM35P5_4M.23a.2_  
-----  
n/2p4m/GIC/inverter/inverter.gds  
n/2p4m/GIC/inverter/DRC  
S.db (ASCII)  
E)  
EW = YES  OFFGRID = YES  
ON = YES  NONSIMPLE PATH = NO  
-----  
e FLAT instantiation.  
e FLAT instantiation.  
e FLAT instantiation.  
e FLAT instantiation.  
e FLAT instantiation.  
e FLAT instantiation.  
e FLAT instantiation.  
e FLAT instantiation.  
-----
```

DRC (Design Rule Check)

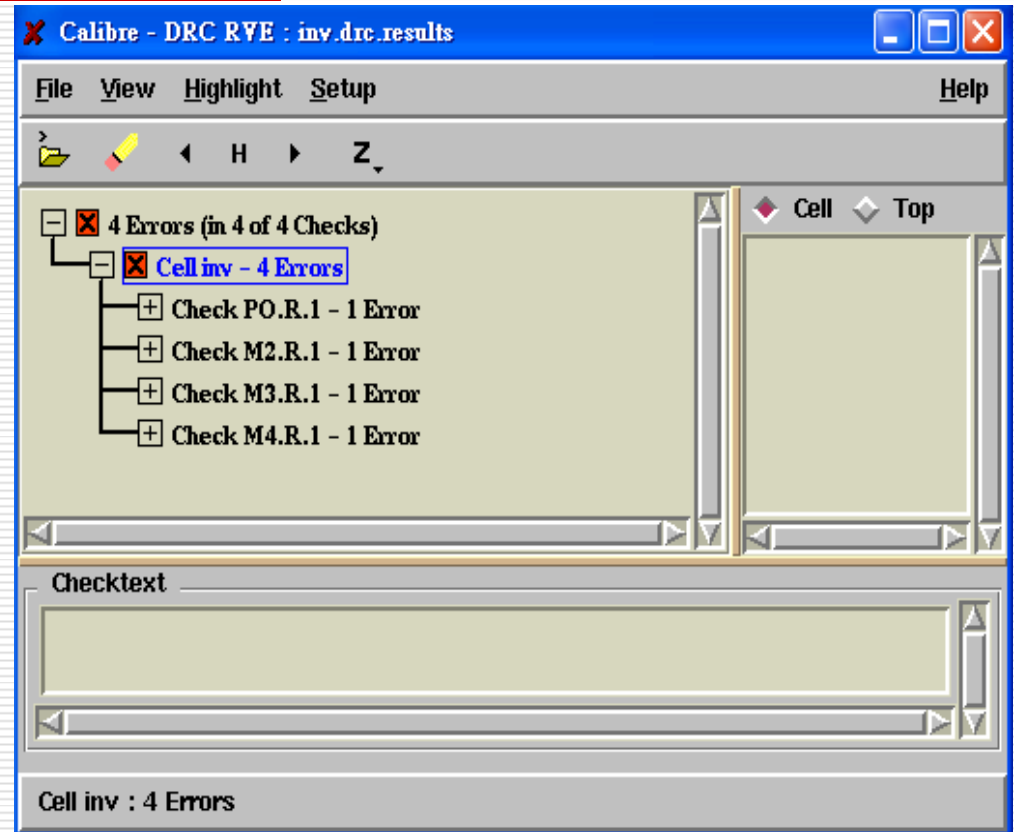
□ 可允許的錯誤

註：

.R 的 **Error** 跟 **Layout** 的材料密度有關不會影響 **DRC** 的正確度

可允許之 **DRC** 錯誤狀況及誤判錯誤列表可參考下列網頁

<http://www2.cic.org.tw/~shuttle/drc/t35ms/index.html>



LVS (Layout vs Schematic)

- 注意：做 **LVS** 前需先完成電路模擬，也就是要有電路的 **SPICE Files**

將在 **Pre-Simulation** 所產生出來的 **SPICE File** 做如下的改變

```
inverter.sp - WordPad
檔案(F) 編輯(E) 檢視(V) 插入(I) 格式(O) 說明(H)
. PARAM
*.GLOBAL vdd!
+ vss!

*.PIN vdd!
*+ vss!

*****
* Library Name: CIC
* Cell Name: inverter
* View Name: schematic
*****

.SUBCKT inverter A B
*.PININFO A:I B:O
M1 B A vss! vss! N w=1u L=350.00n
M0 B A vdd! vdd! P w=1u L=350.00n
.ENDS

如需說明，請按 F1
```

MM1改爲M1
MM0改爲M0

NM改爲N

PM改爲P

LVS (Layout vs Schematic)

- ❑ Virtuoso Layout 視窗 → Calibre → Run LVS → Rules

The screenshot shows the Calibre Interactive - LVS window. On the left is a vertical toolbar with buttons for Rules, Inputs, Outputs, Run Control, Transcript, Run LVS, and Start RVE. The main area contains two input fields: 'Calibre-LVS Rules File' with a path and a 'Load' button, and 'Calibre-LVS Run Directory' with a path and an ellipsis button. Annotations include a box labeled 'Technology file' pointing to the Rules button, a box labeled '結果檔存放處' pointing to the Transcript button, and a box labeled '記得要按 Load (建議多按幾次)' pointing to the Load button.

Technology file

結果檔存放處

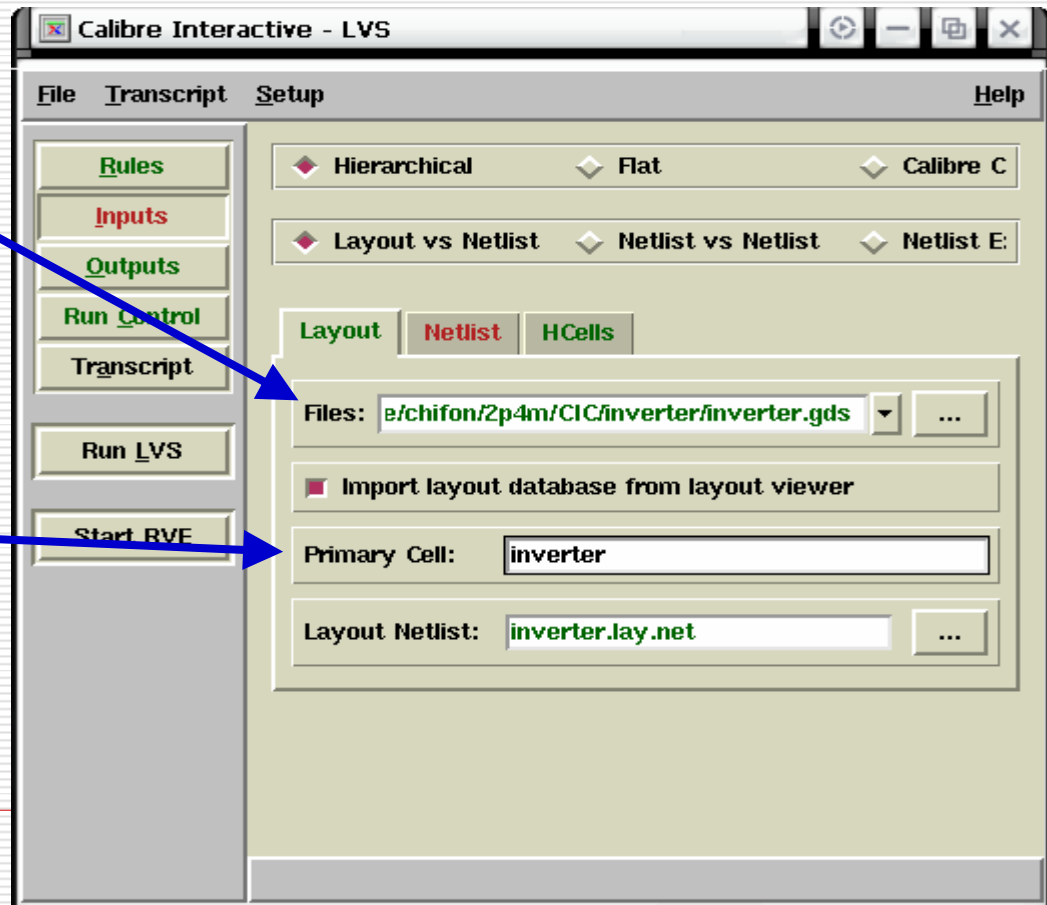
記得要按 Load
(建議多按幾次)

LVS (Layout vs Schematic)

□ Inputs → Layout

Layout gds file

輸入 Cell Name

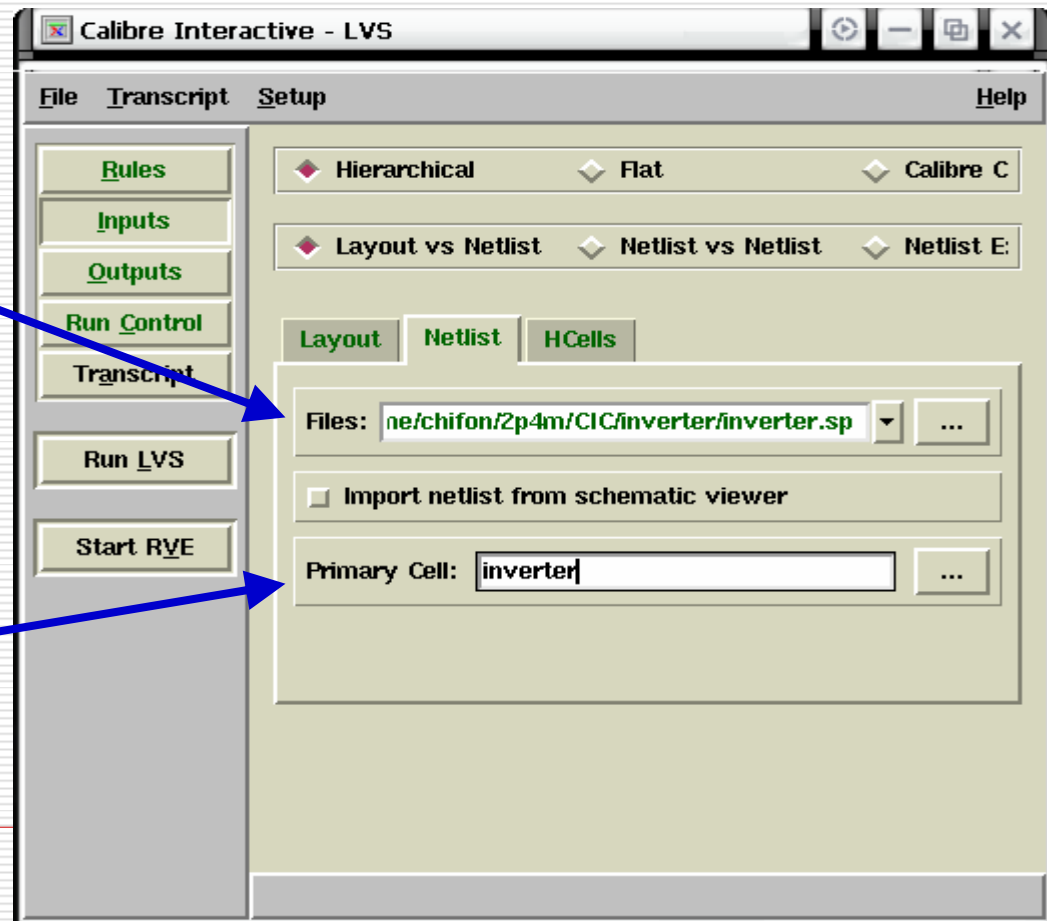


LVS (Layout vs Schematic)

□ Inputs → Netlist

電路 SPICE file

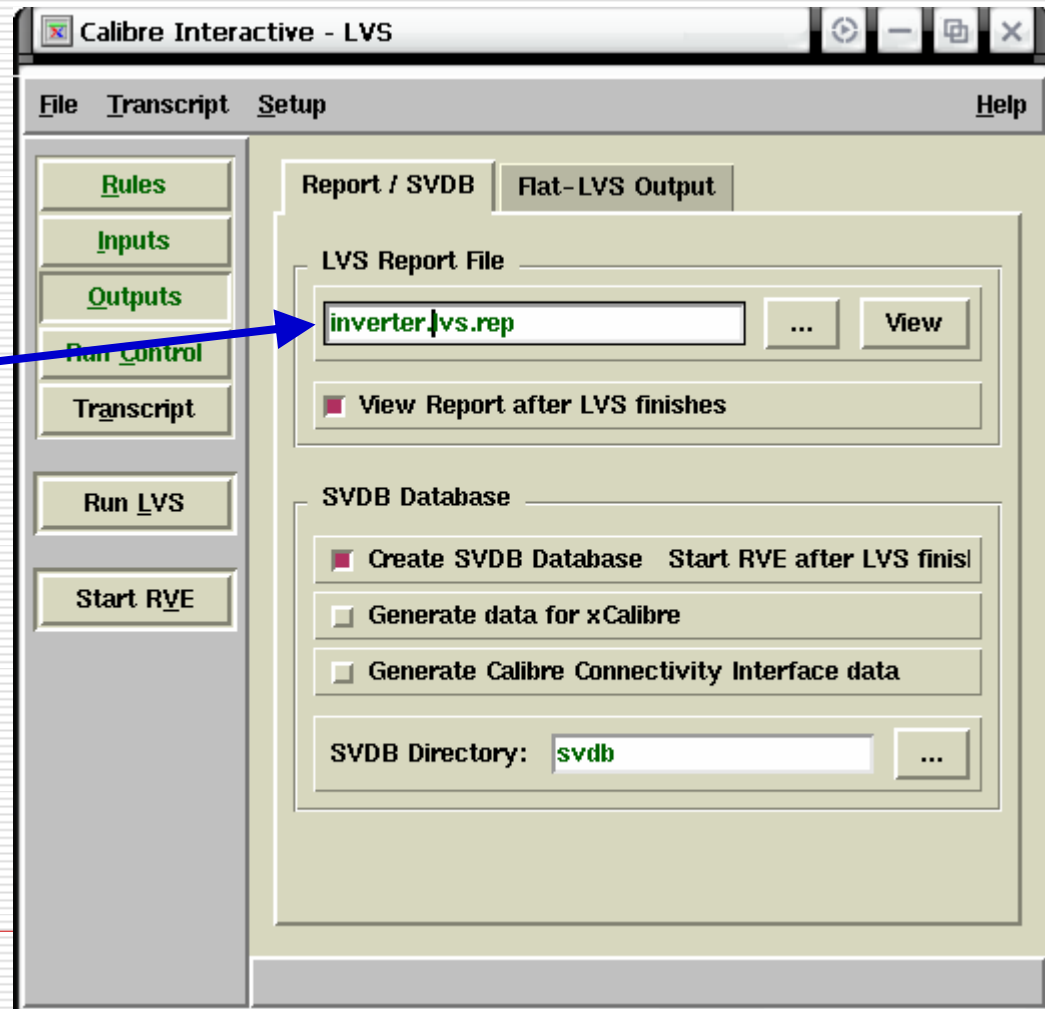
輸入 Cell Name



LVS (Layout vs Schematic)

□ Outputs

輸入Cell Name
(此步驟可省略)

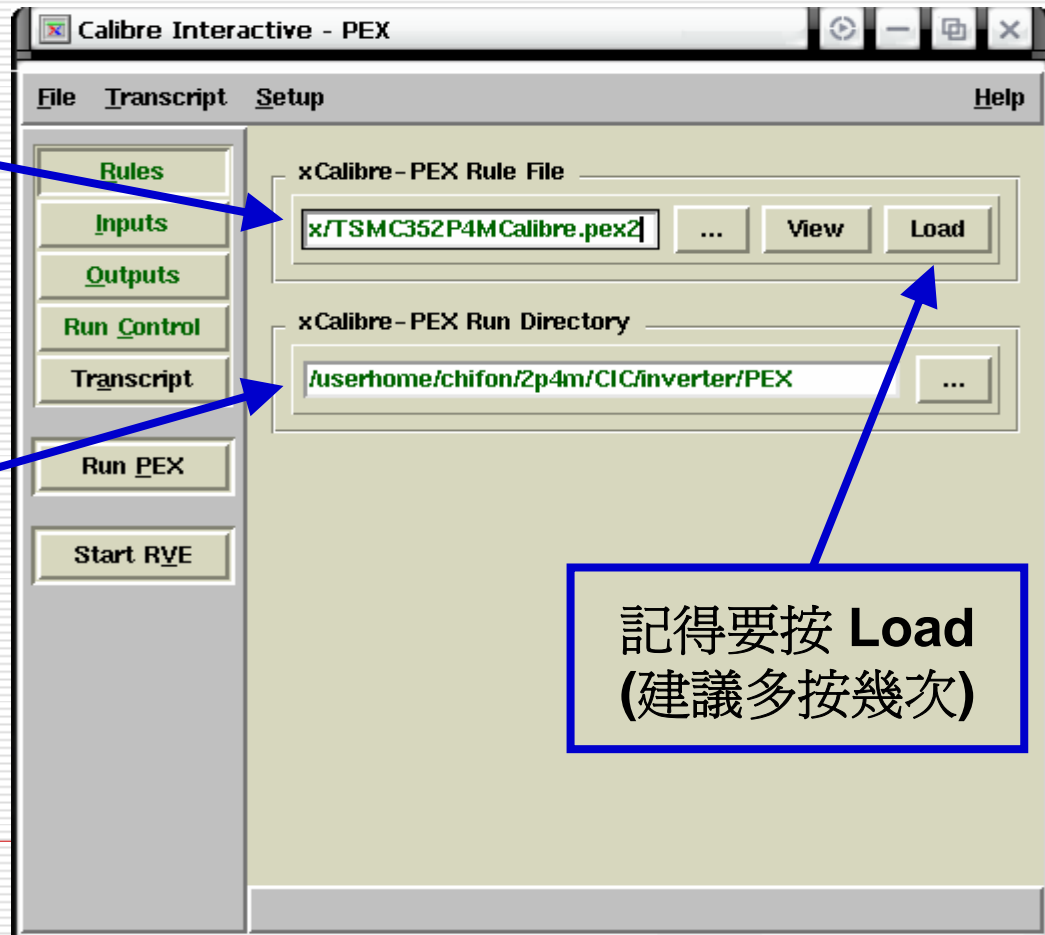


PEX (Post layout extraction)

- ❑ Virtuoso Layout 視窗 → Calibre → Run PEX → Rules

Technology file

結果檔存放處



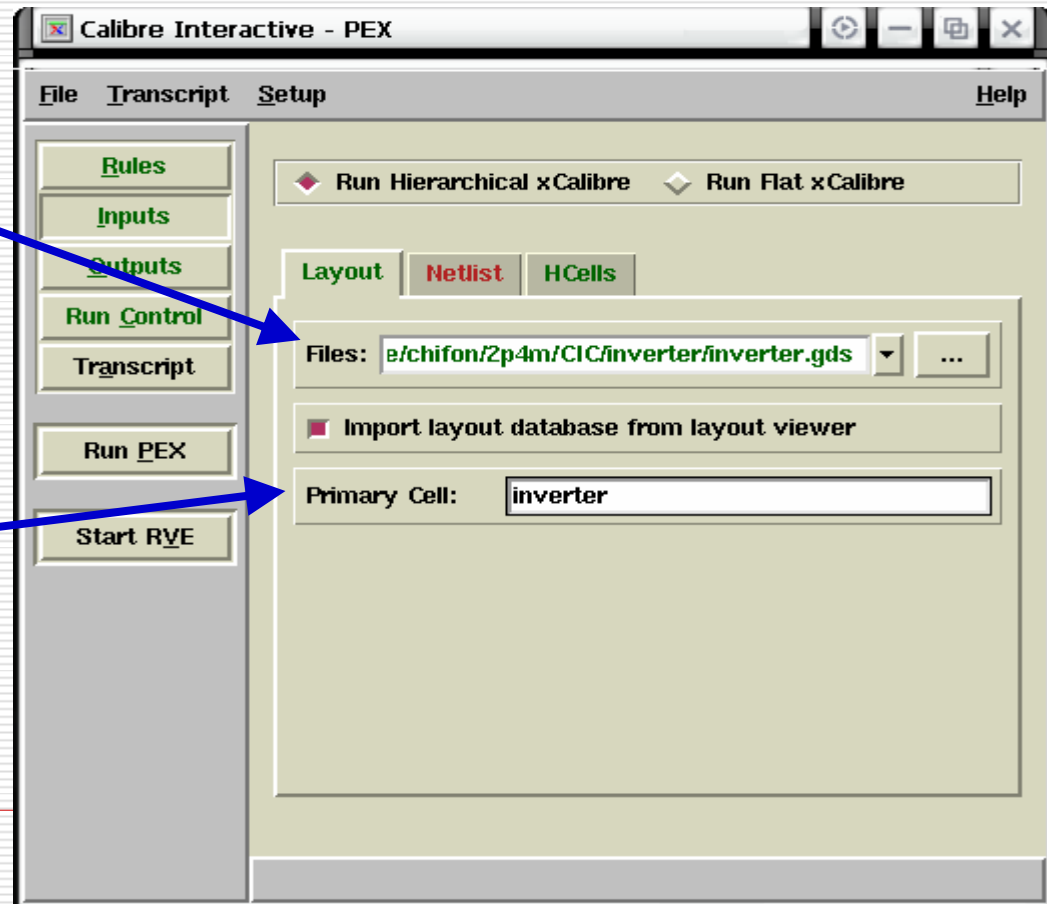
記得要按 Load
(建議多按幾次)

PEX (Post layout extraction)

□ Inputs → Layout

Layout gds file

輸入 Cell Name

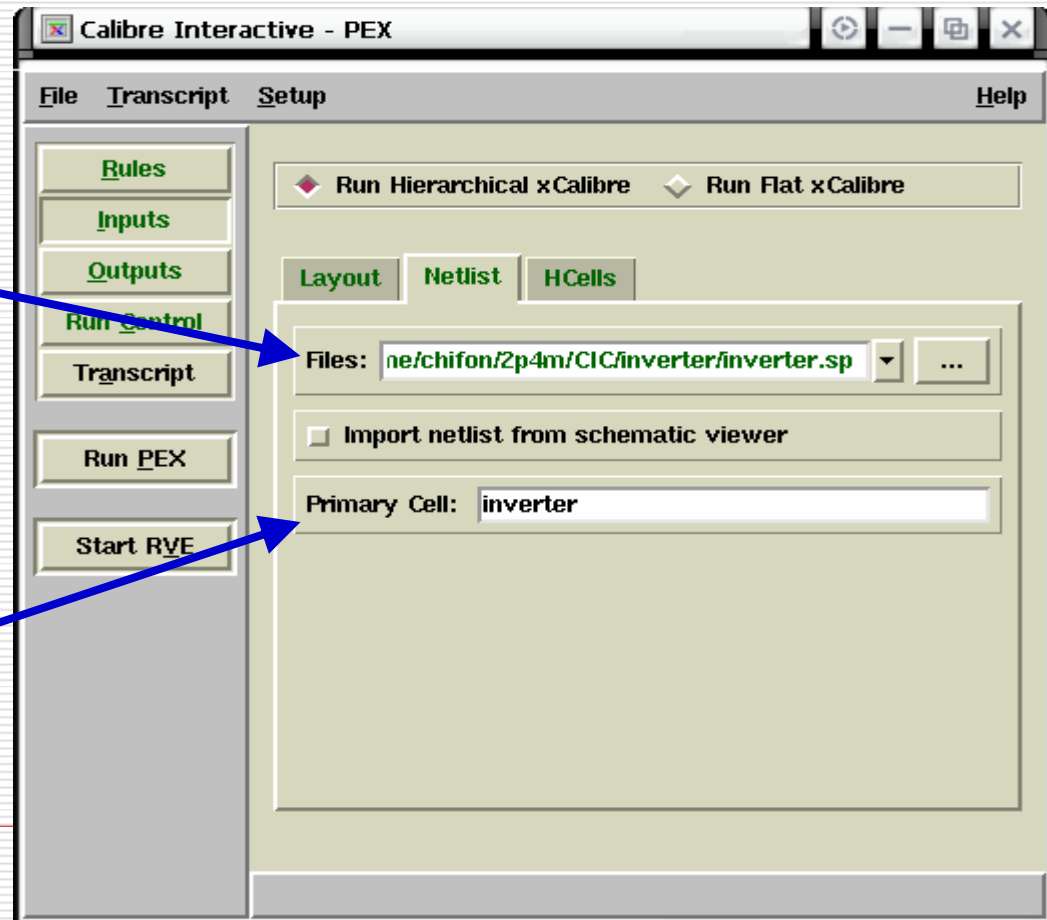


PEX (Post layout extraction)

□ Inputs → Netlist

電路 SPICE file

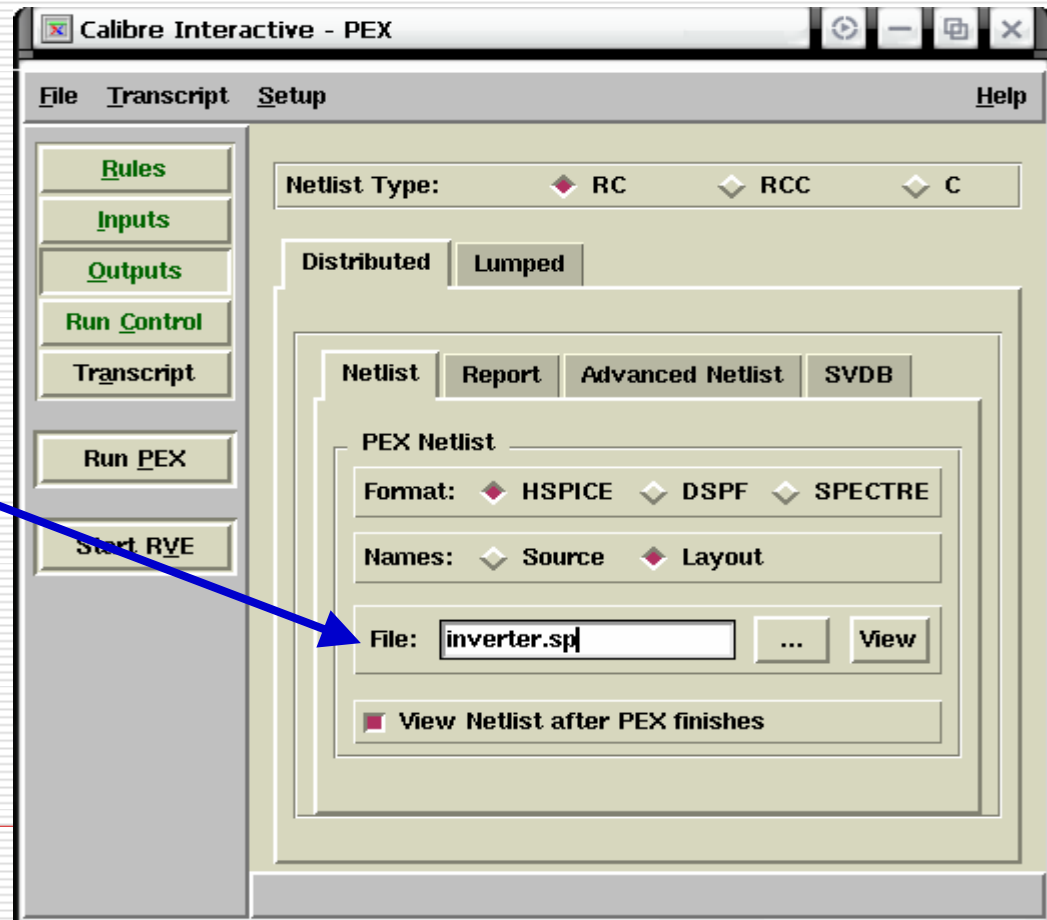
輸入 Cell Name



PEX (Post layout extraction)

□ Outputs → Netlist

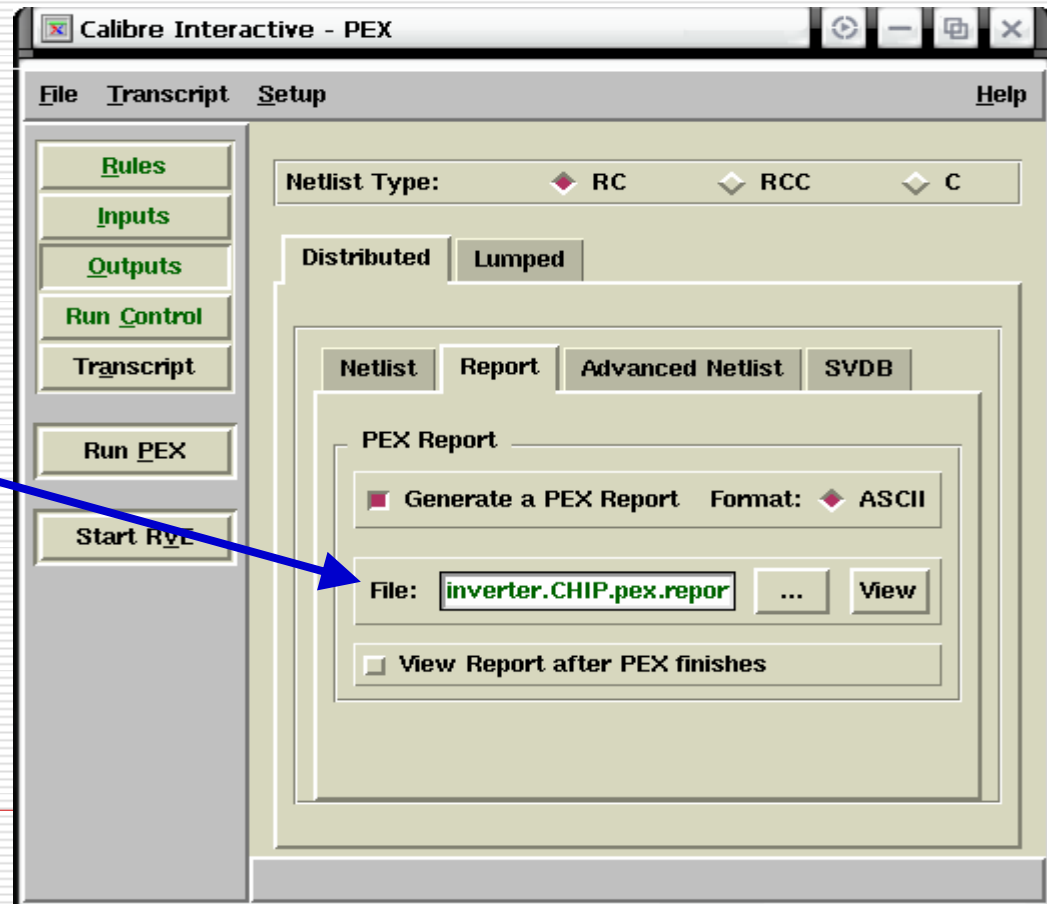
輸入欲輸出的檔名



PEX (Post layout extraction)

□ Outputs → Report

輸入欲輸出的檔名



PEX (Post layout extraction)

□ 按下 Run PEX

則在存放結果資料夾中，將會產生出含有寄生電容電阻的 **SPICE Files**，如下圖所示。

