Post-Simulation 教學手冊 (Calibre部分)

目錄

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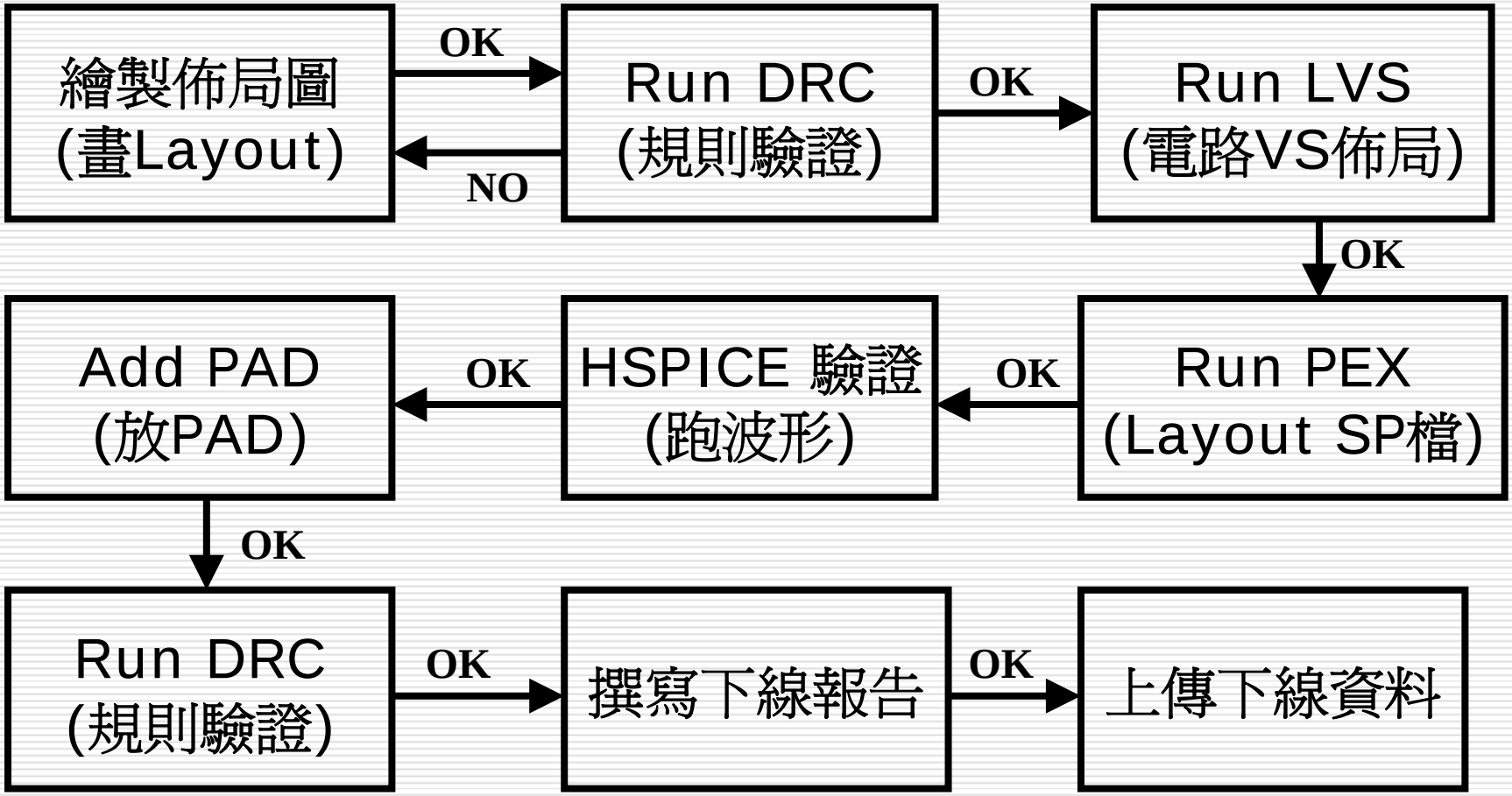
- Prepare Files
- Layout editor environment setup
- DRC
- LVS
- PEX

Post-Simulation流程

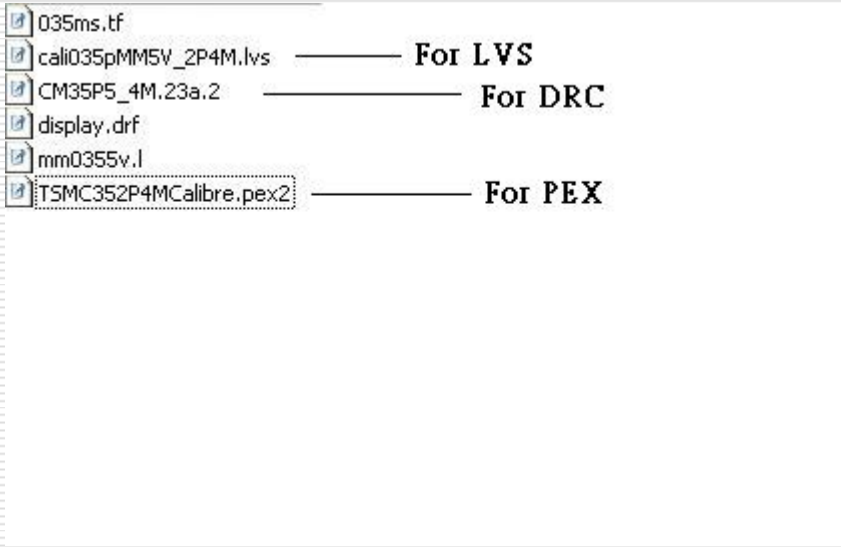


Prepare Files

035ms.tf	Technology file for design rule
DRC	Design Rule Check
LVS	Layout vs Schematic
RC_Ex	Post layout extraction
cds.lib	
.cdsinit	
.cshrc	
display.drf	

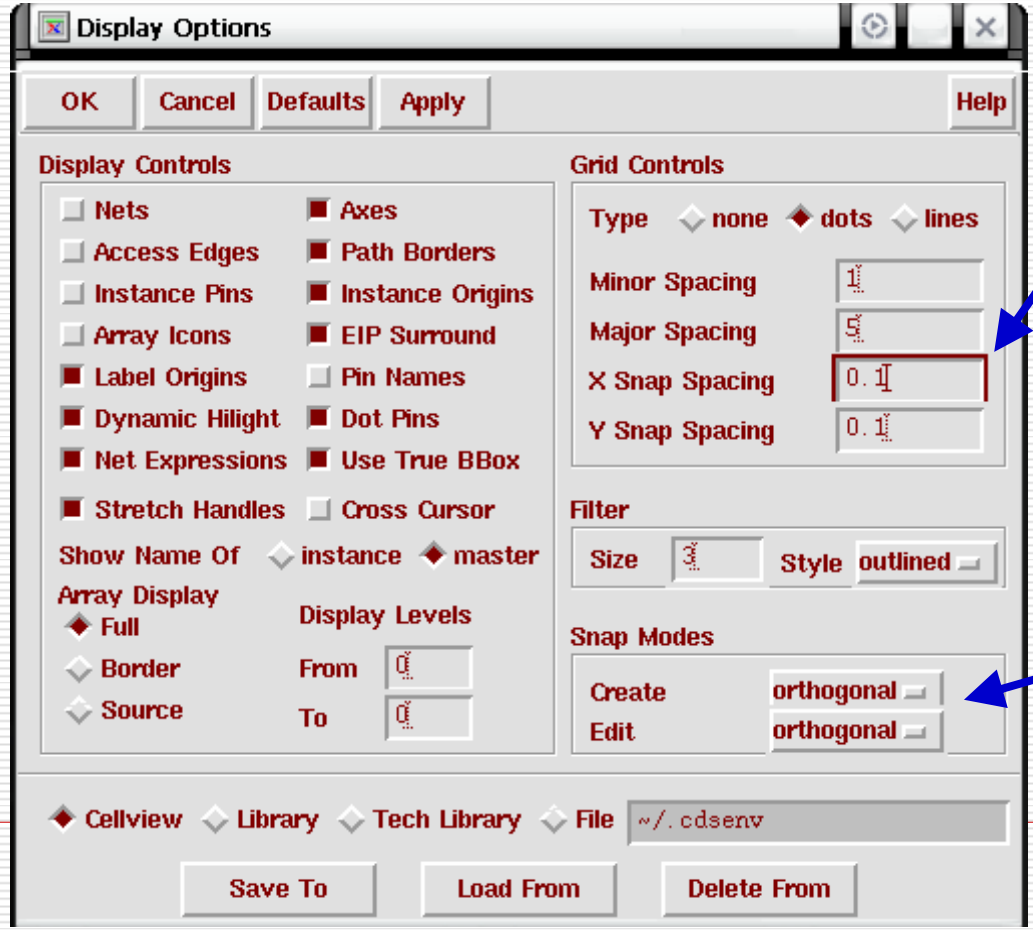
Prepare Files

檢查**2p4m**資料夾中是否有這些檔案和資料夾



Layout editor environment setup

- Options → Display

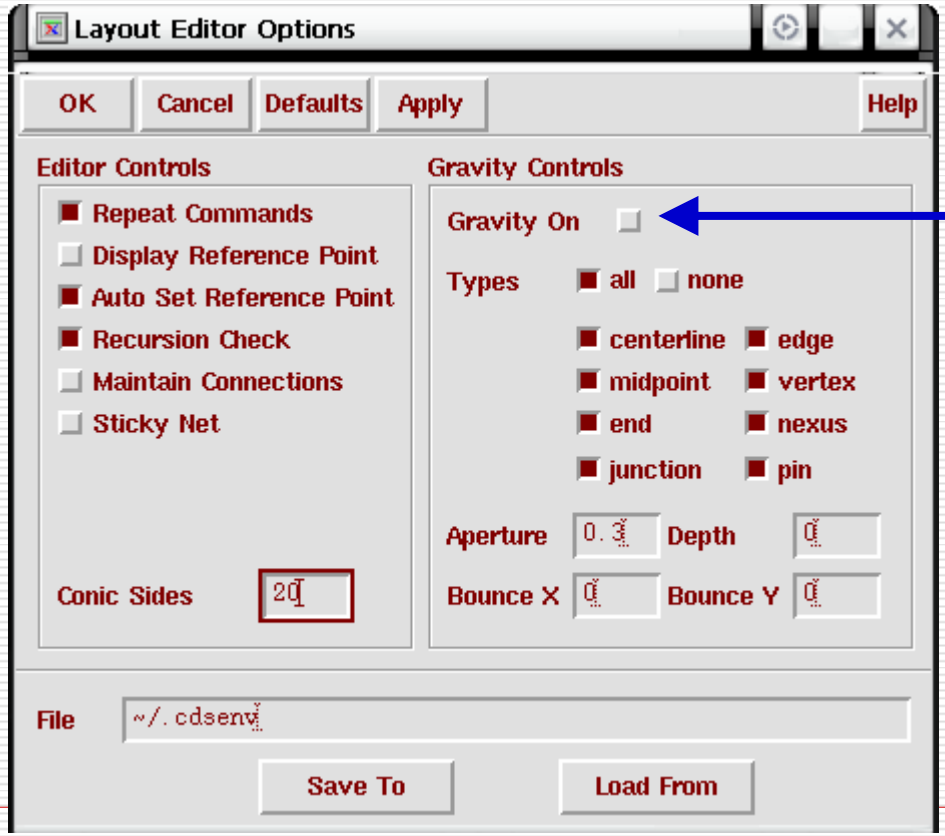


X(Y) Snap Spacing :
X(Y) 軸移動的最小間距，通常是 **0.05**

Snap Modes
視情況選擇適當設定

Layout editor environment setup

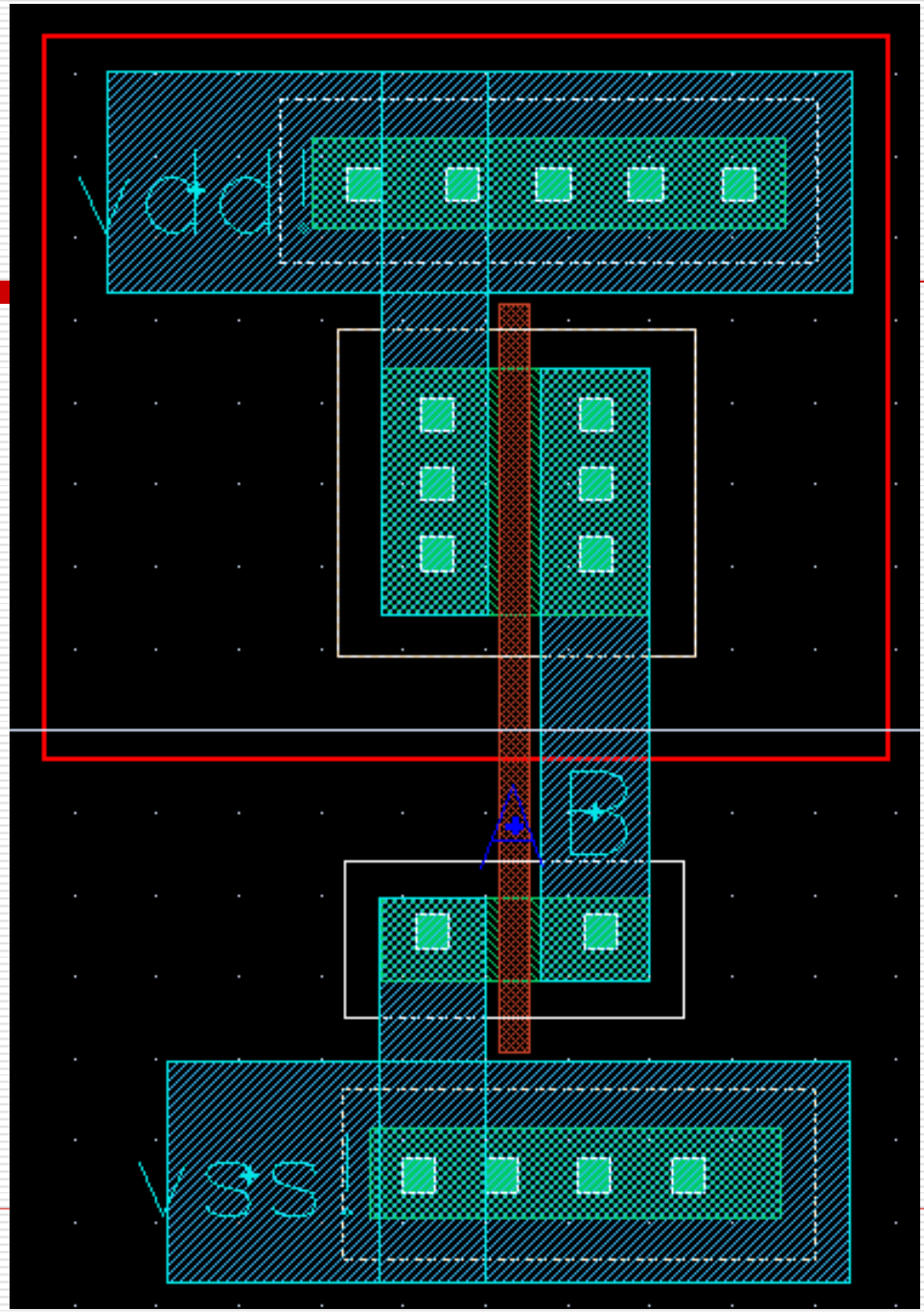
- Options → Layout Editor



當遊標靠近 **object** 時即被吸到 **object** 邊緣 **(建議取消)**

Layout's Hot Key

F2	save	f	fit all
m	move	c	copy
s	stretch	del	delete
u	undo	i	create instance
o	create contact	^p	create symbolic pin
z	zoom	r	rectangle
k/K	ruler/clear all ruler	l	label
q	properties		


vdd
B
A
vss

DRC (Design Rule Check)

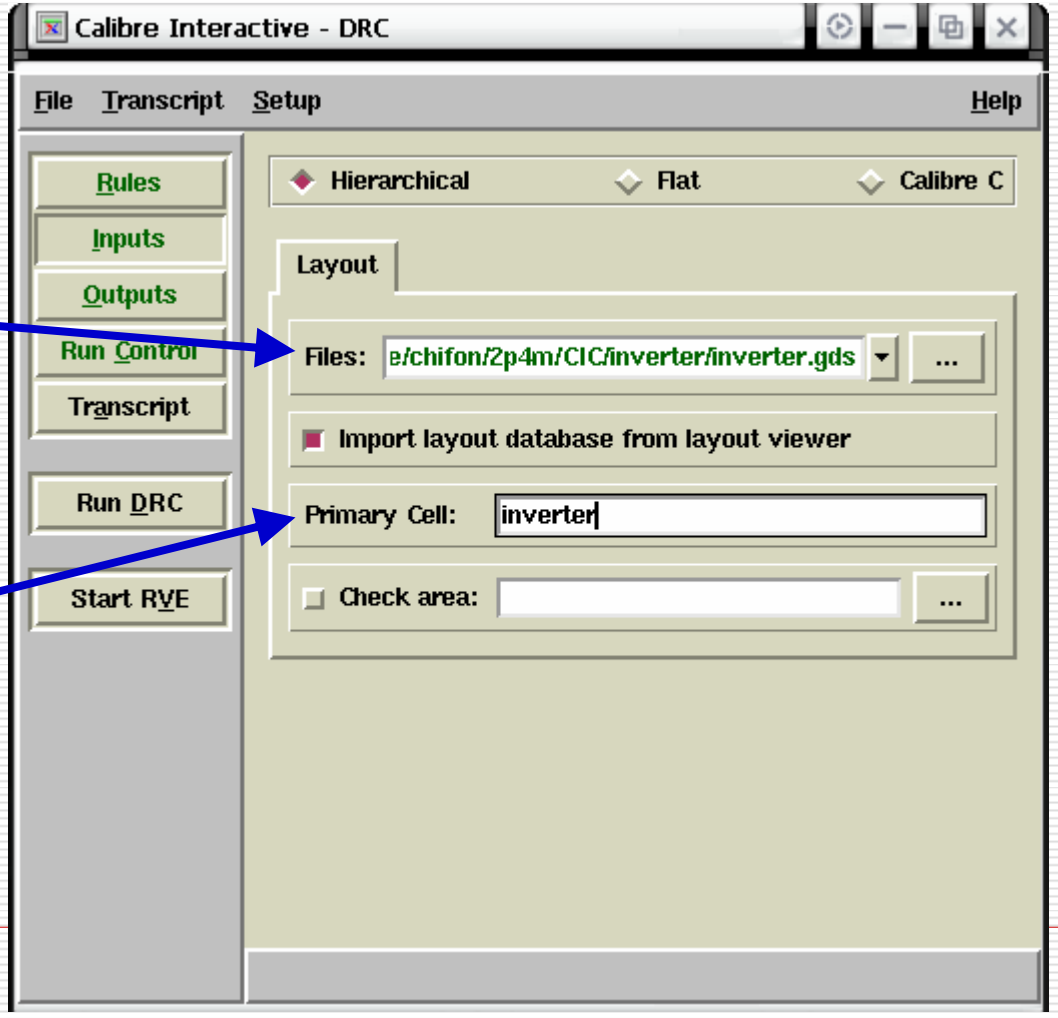
- Virtuoso Layout 視窗 → Calibre → Run DRC → Rules

DRC (Design Rule Check)

- Inputs

Layout gds file

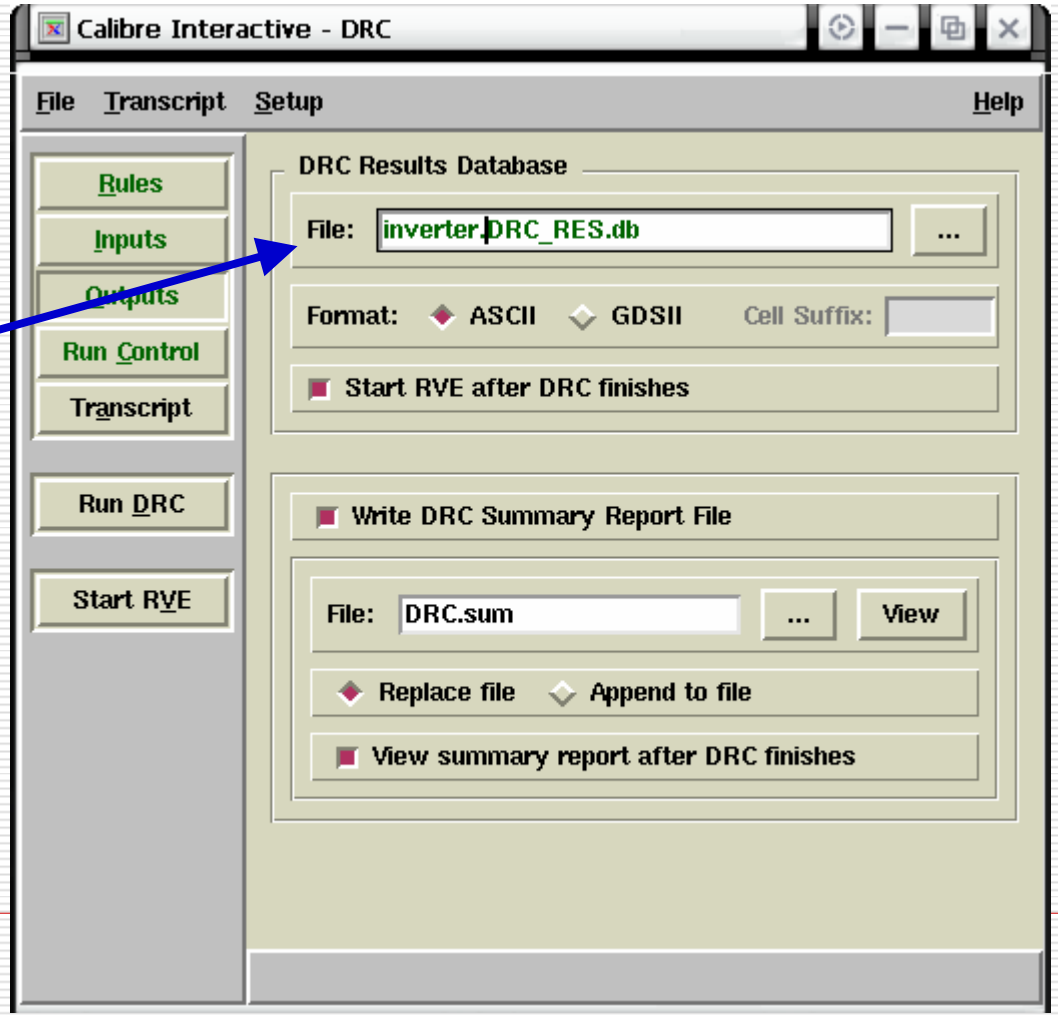
輸入Cell Name



DRC (Design Rule Check)

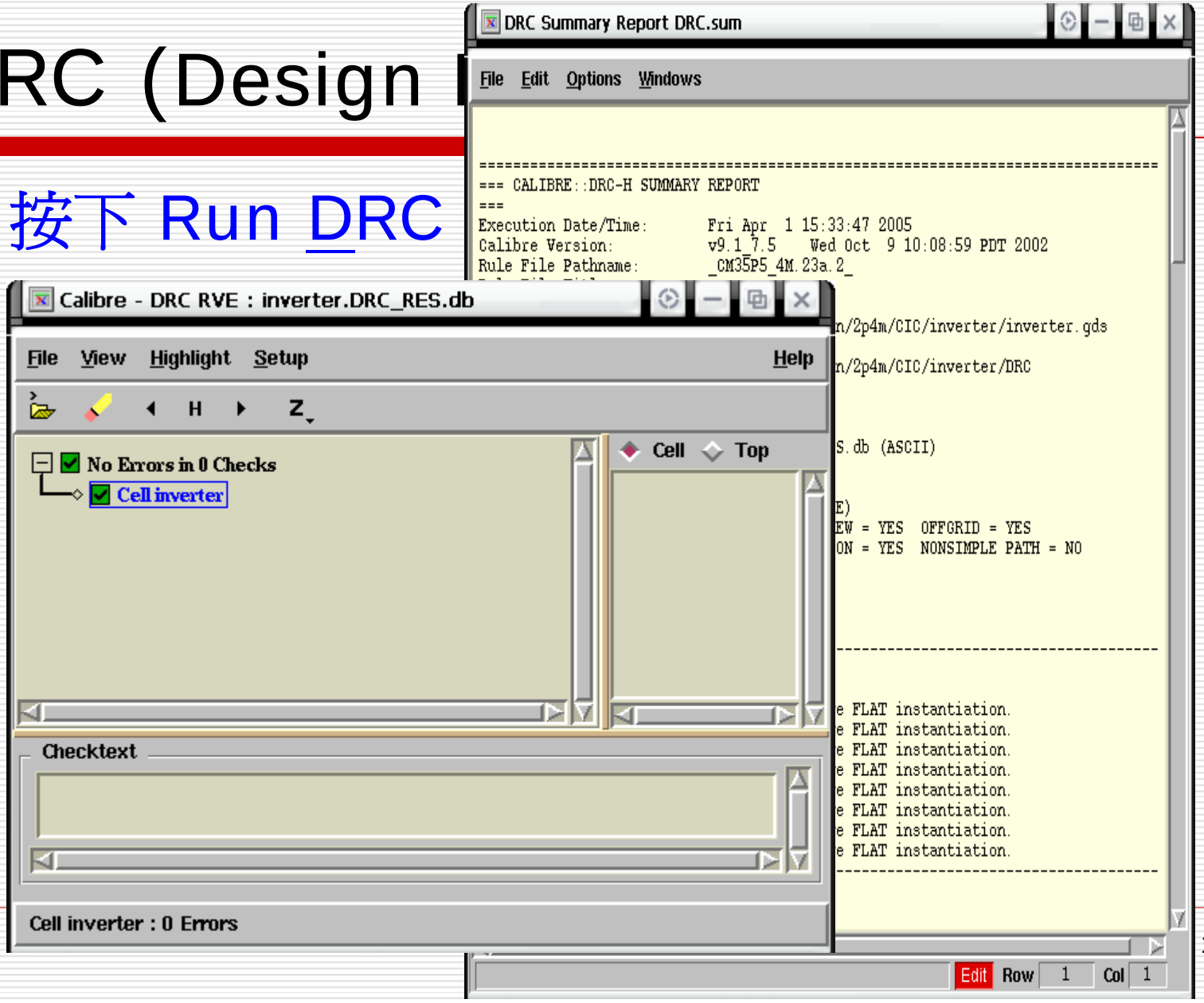
- Outputs

輸入**Cell Name**
(此步驟可省略)



DRC (Design

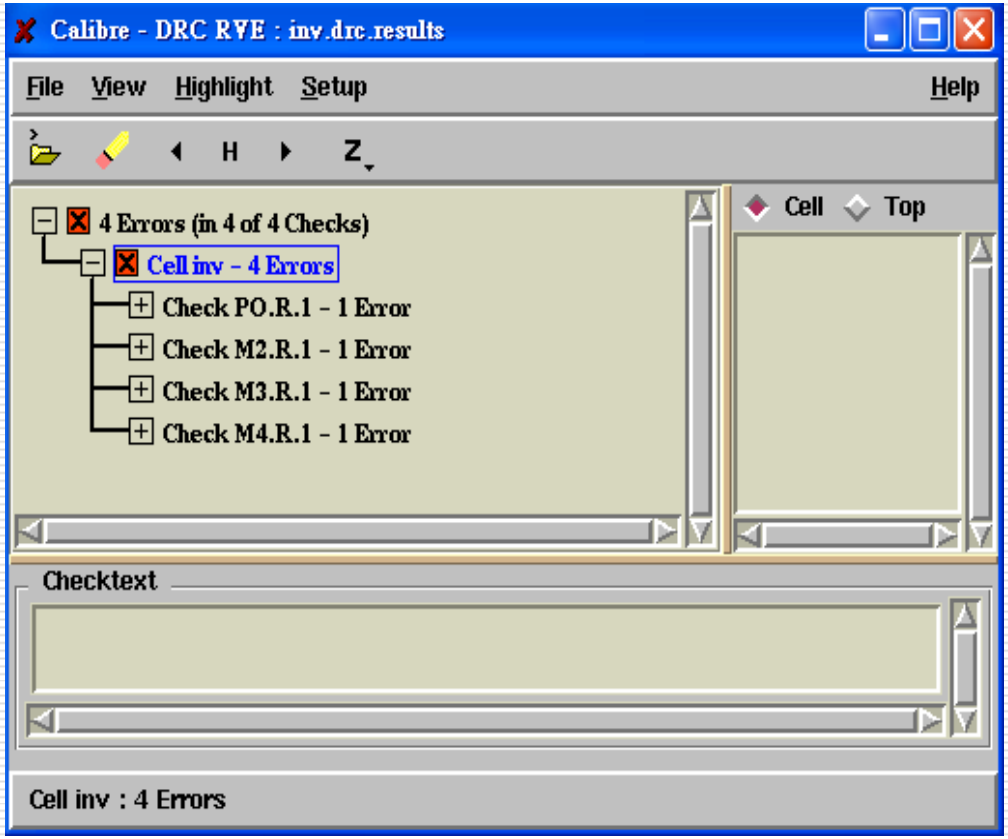
- 按下 Run DRC



DRC (Design Rule Check)

- 可允許的錯誤

註：
.R 的 **Error** 跟 **Layout** 的材料密度有關不會影響 **DRC** 的正確度



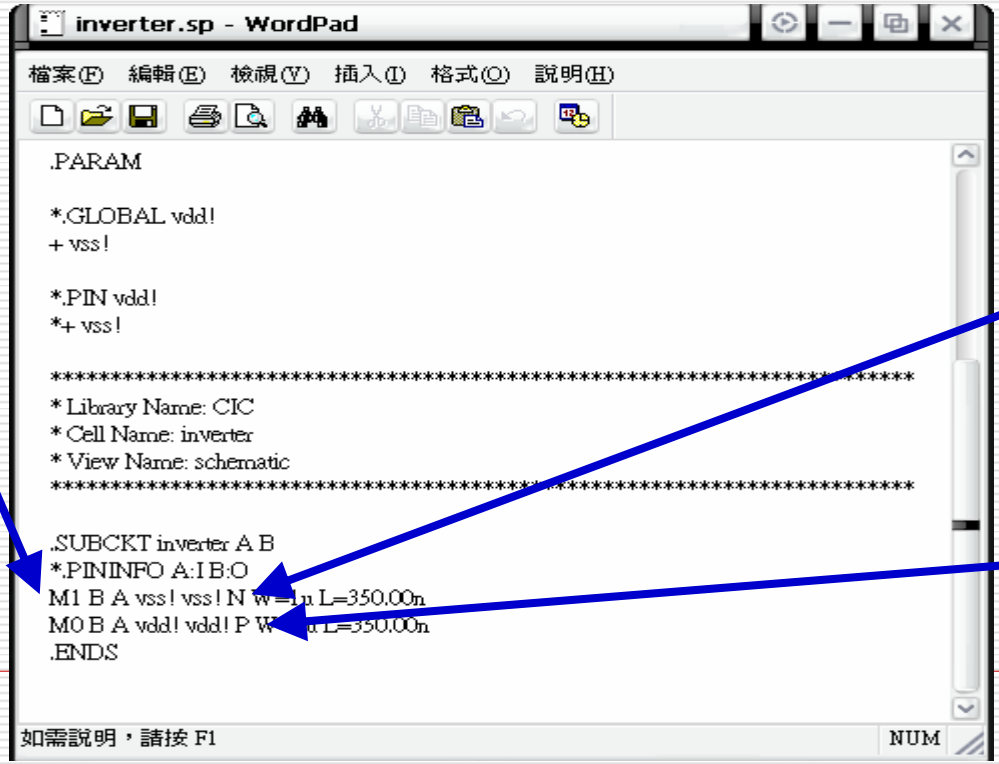
可允許之 **DRC** 錯誤狀況及誤判錯誤列表可參考下列網頁

http://www2.cic.org.tw/~shuttle/drc/t35ms/index.html

LVS (Layout vs Schematic)

- 注意：做 **LVS** 前需先完成電路模擬，也就是要有電路的 **SPICE Files**

將在 **Pre-Simulation** 所產生出來的 **SPICE File** 做如下的改變



MM1改爲M1
MM0改爲M0

NM改爲N

PM改爲P

LVS (Layout vs Schematic)

- Virtuoso Layout 視窗 → Calibre → Run LVS → Rules

Technology file

結果檔存放處

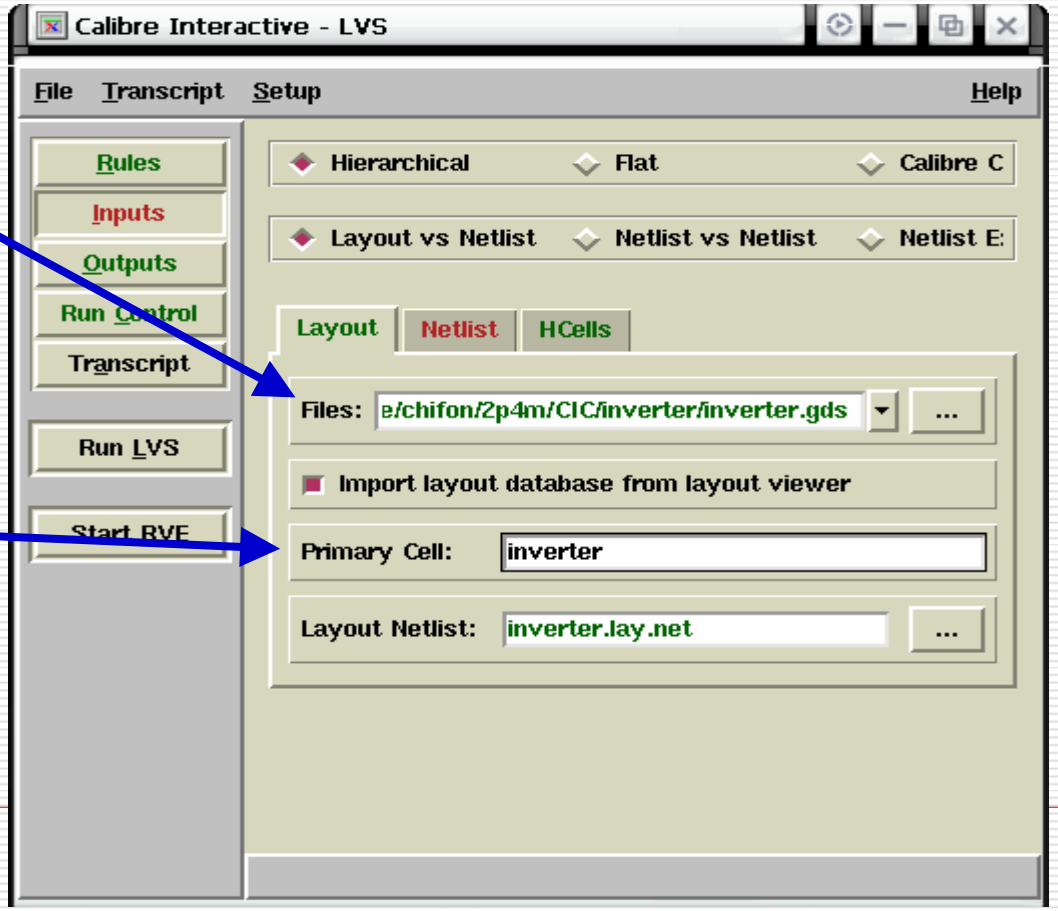
記得要按 **Load**
(建議多按幾次)

LVS (Layout vs Schematic)

- Inputs → Layout

Layout gds file

輸入Cell Name

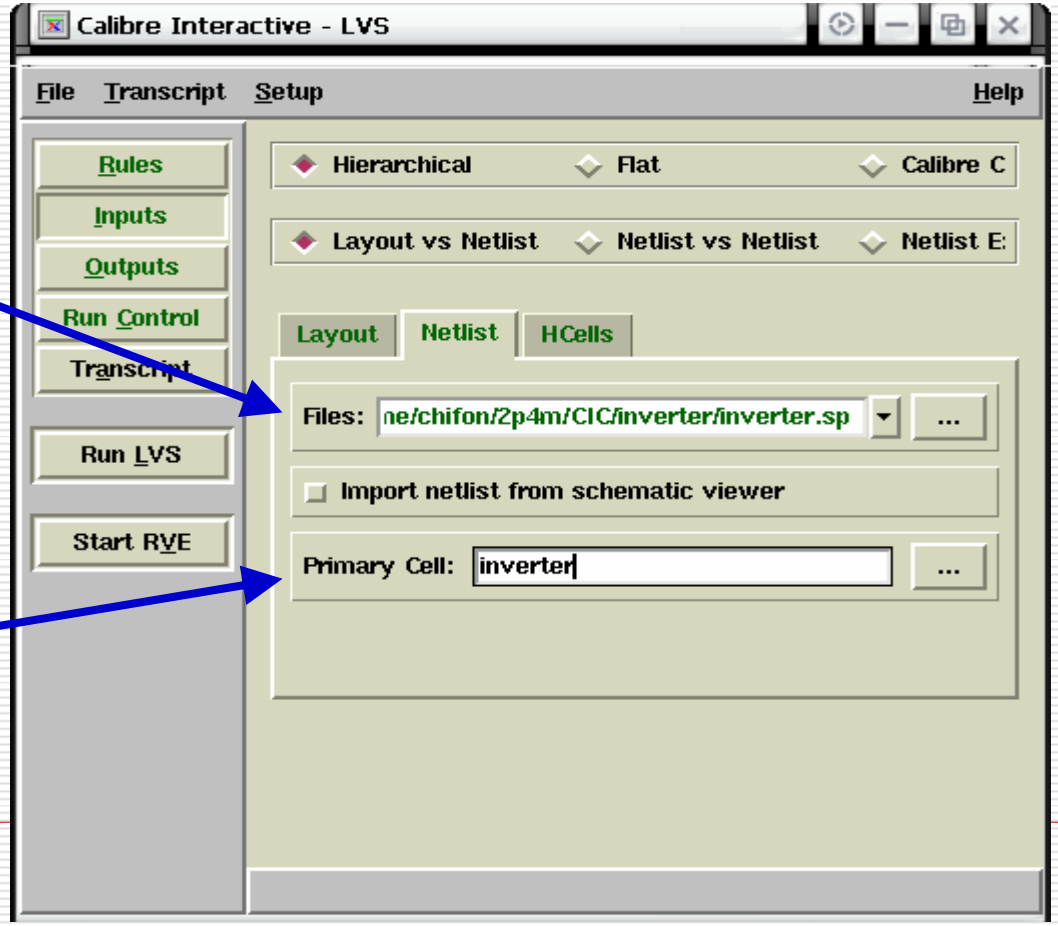


LVS (Layout vs Schematic)

- Inputs → Netlist

電路 **SPICE file**

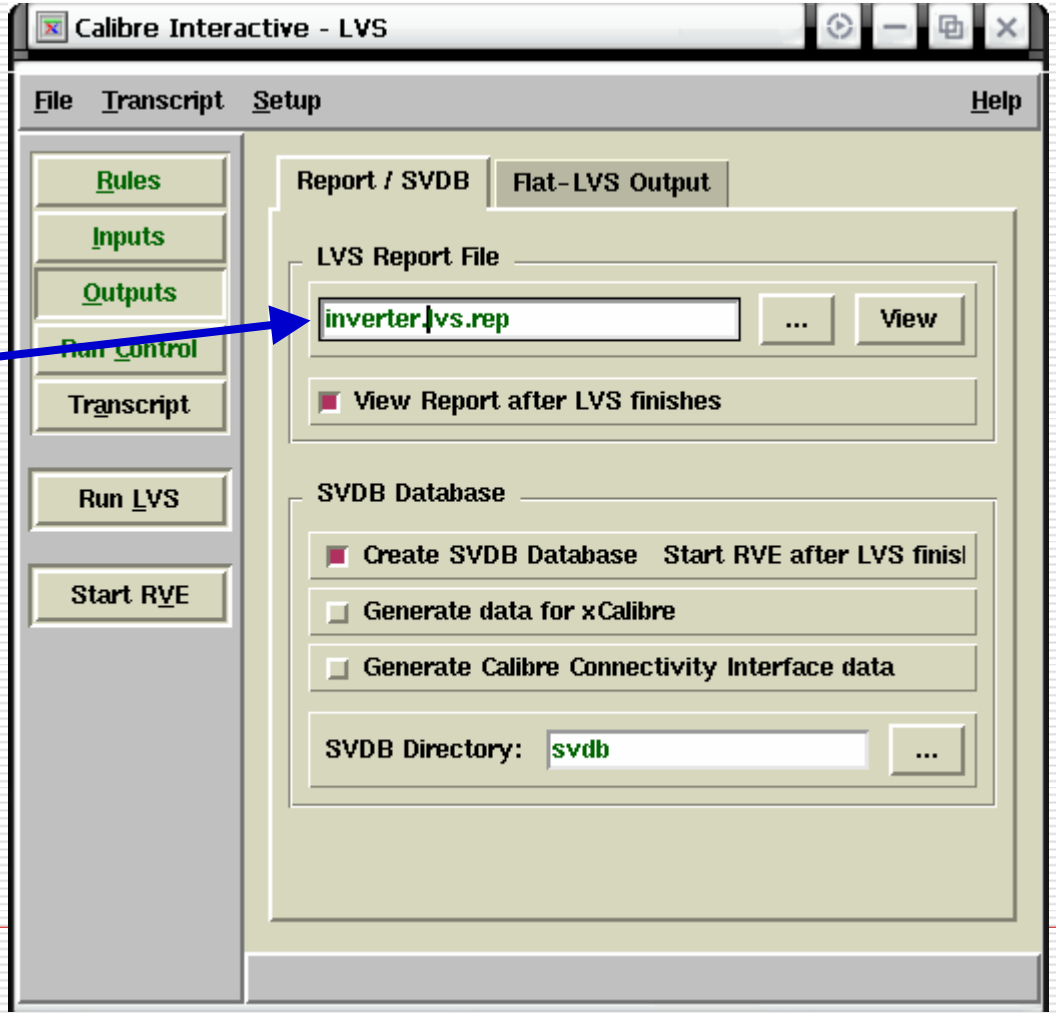
輸入**Cell Name**



LVS (Layout vs Schematic)

- Outputs

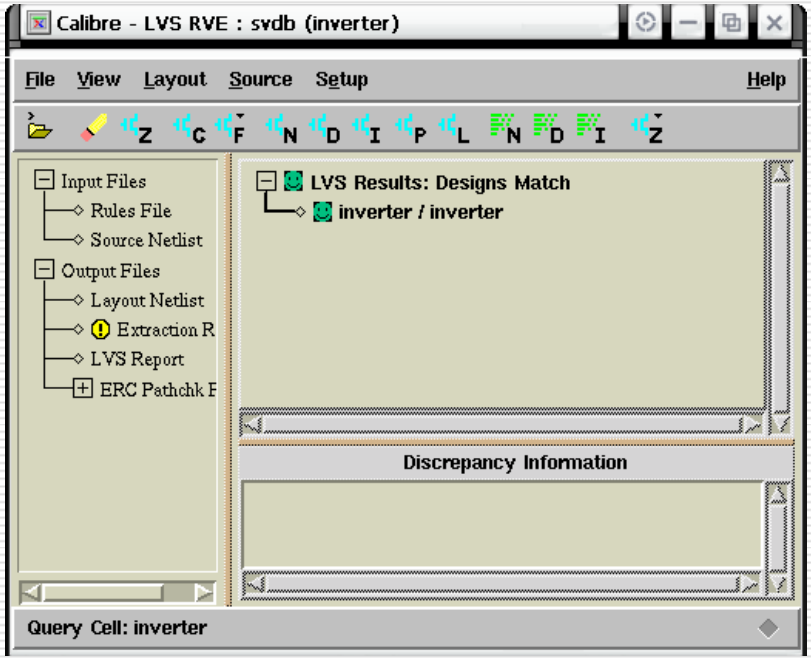
輸入**Cell Name**
(此步驟可省略)



LVS (Layout vs Schematic)

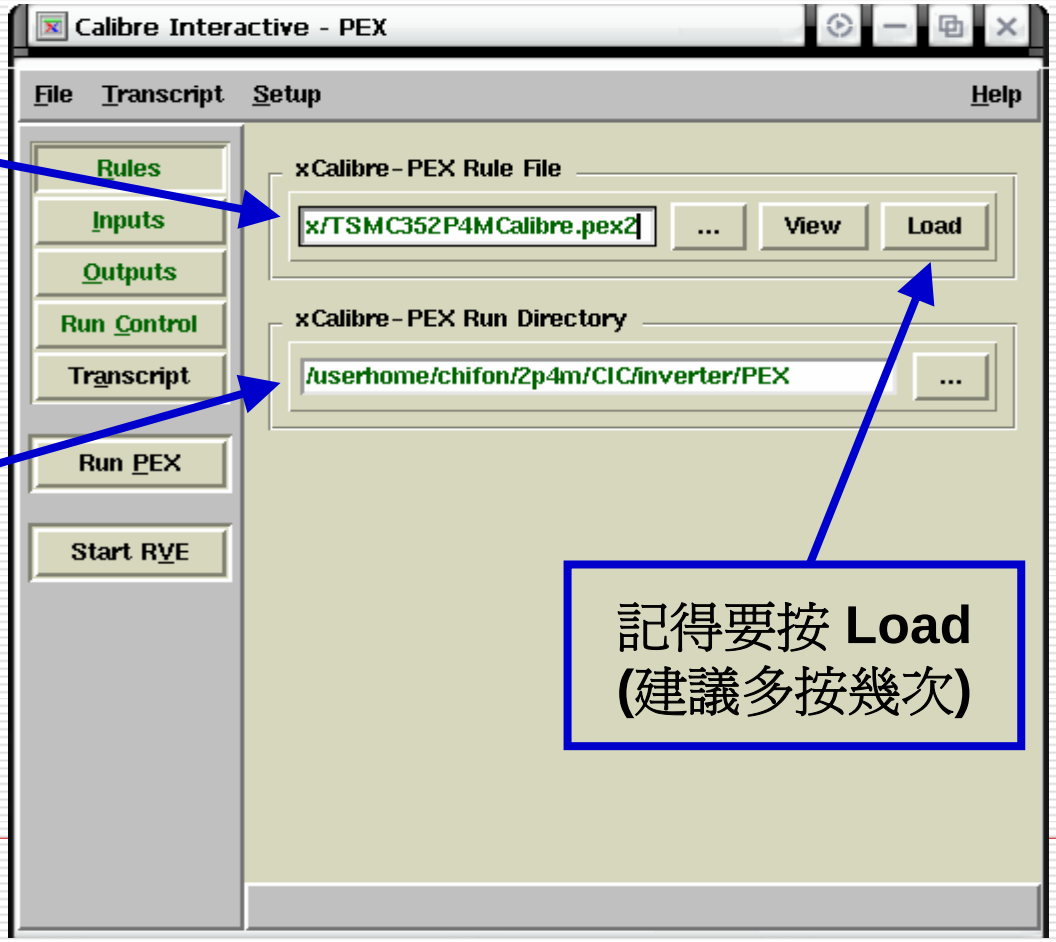
- 按下 Run LVS

  若 **Layout** 和 **Schematic** 比對相同則出現以下結果



PEX (Post layout extraction)

- Virtuoso Layout 視窗 → Calibre → Run PEX → Rules

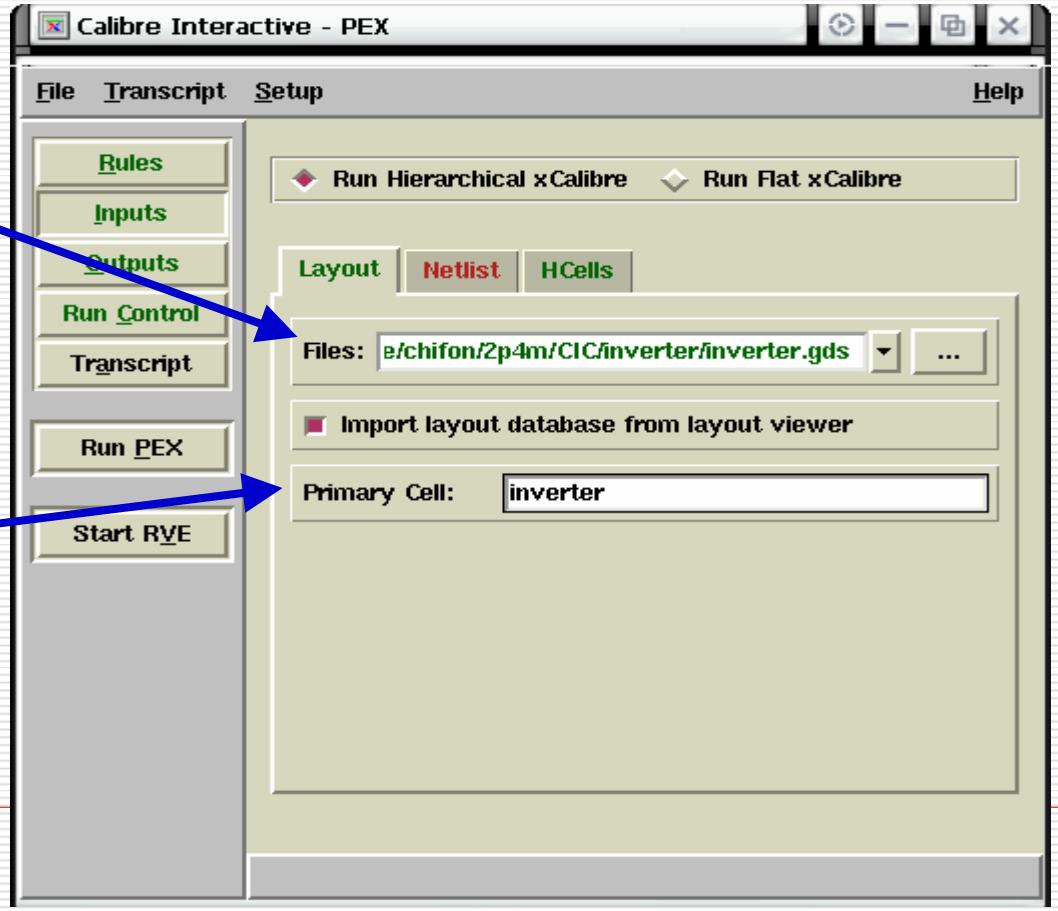


PEX (Post layout extraction)

- Inputs → Layout

Layout gds file

輸入Cell Name

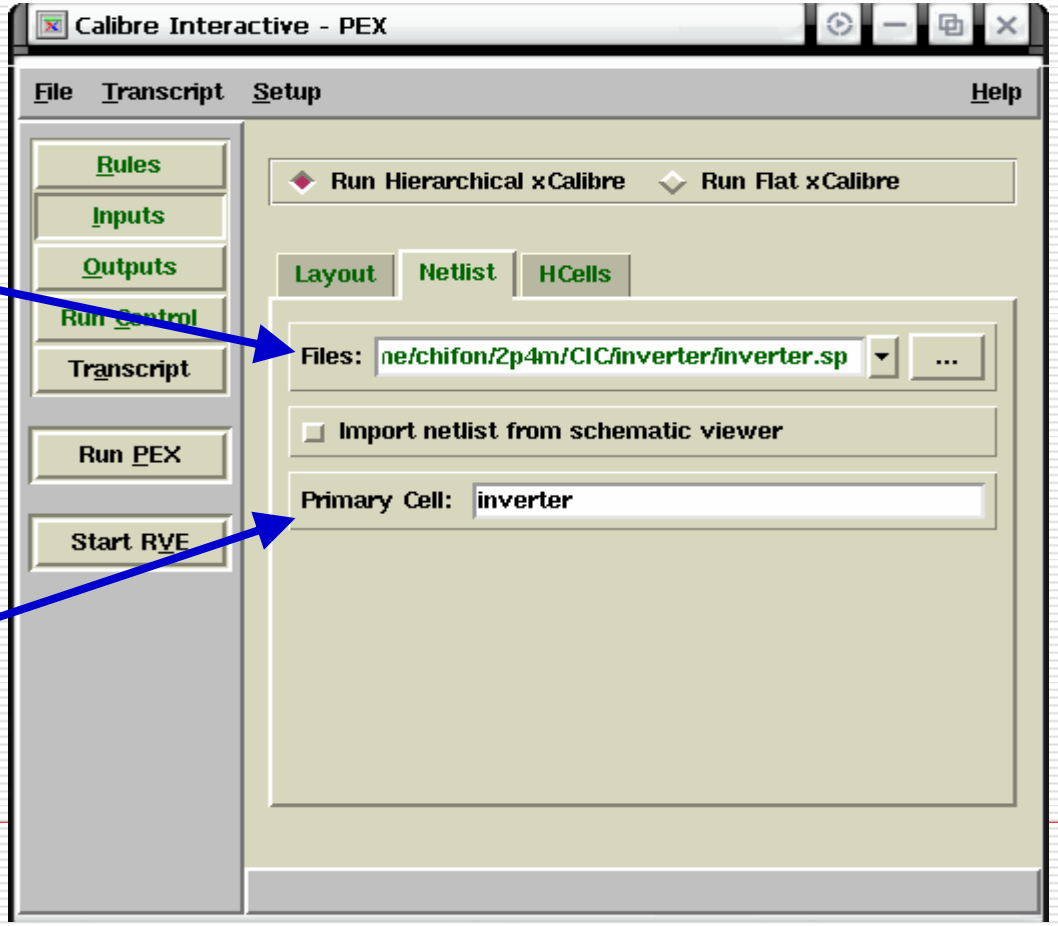


PEX (Post layout extraction)

- Inputs → Netlist

電路 **SPICE file**

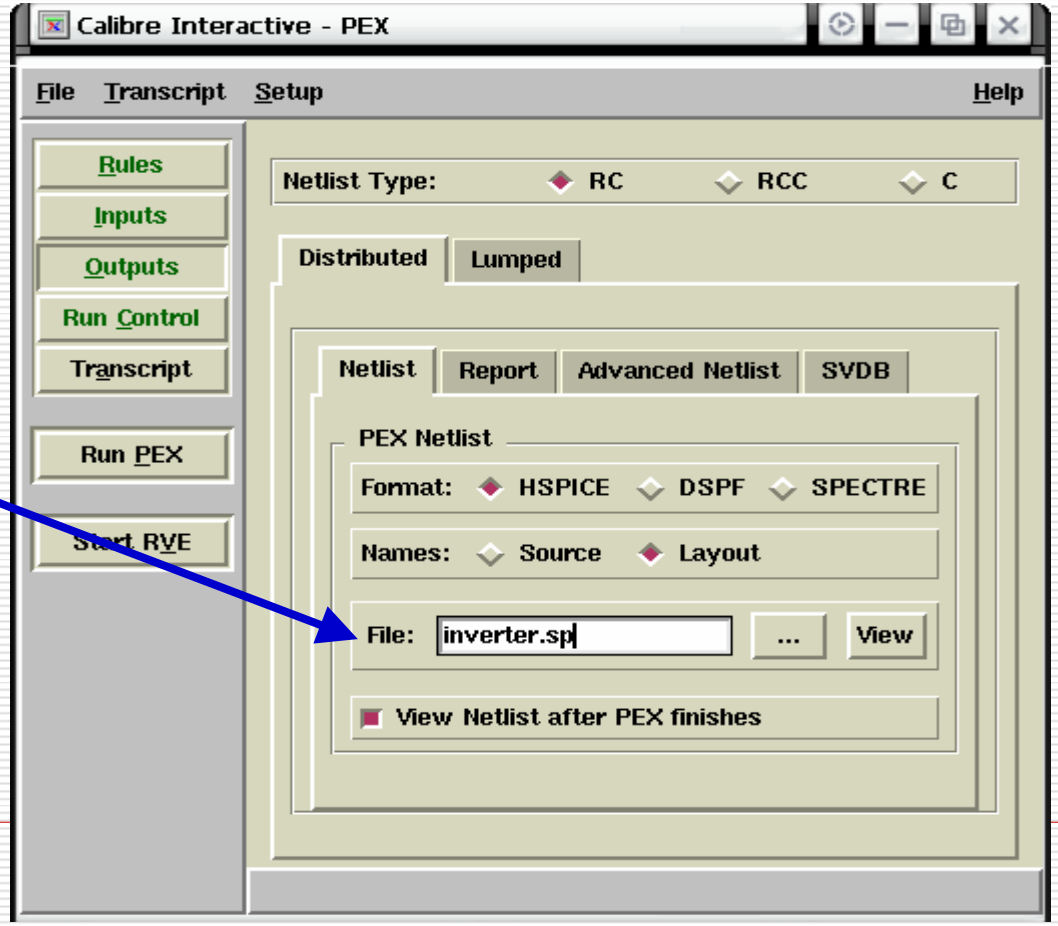
輸入**Cell Name**



PEX (Post layout extraction)

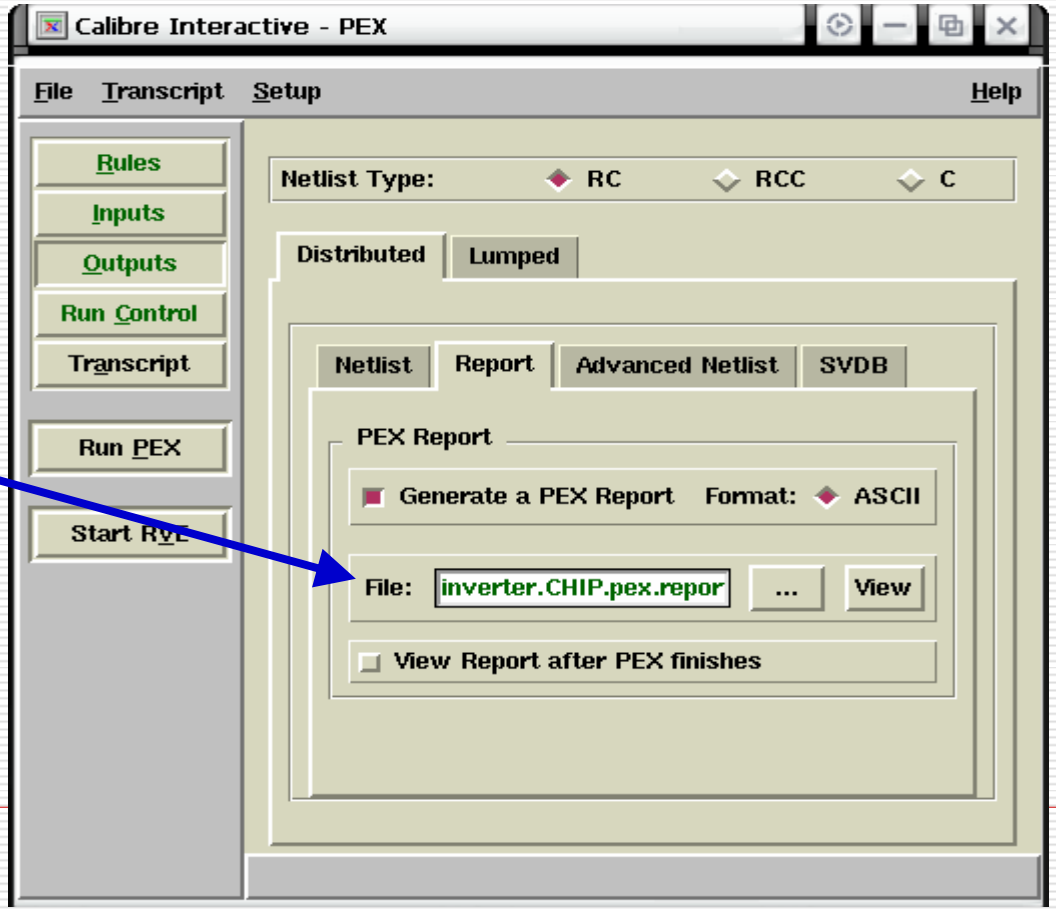
- Outputs → Netlist

輸入欲輸出的檔名



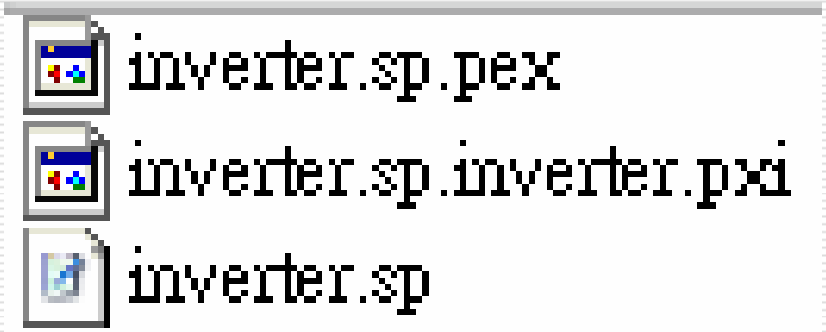
PEX (Post layout extraction)

- Outputs → Report



輸入欲輸出的檔名

PEX (Post layout extraction)

- 按下 Run PEX

則在存放結果資料夾中，將會產生出含有寄生電容電阻的 **SPICE Files**，如下圖所示。