An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing

Luís H. C. Ferreira, *Member, IEEE*, Tales Cleber Pimenta, *Member, IEEE*, and Robson L. Moreno

***Abstract*—An ultra-low-voltage ultra-low-power CMOS Miller operational transconductance amplifier (OTA) with rail-to-rail input/output swing is presented. The topology is based on combining bulk-driven differential pair and dc level shifters, with the transistors work in weak inversion. The improved Miller OTA has been successfully verified in a standard 0.35-μm CMOS process. Experimental results have confirmed that, at a minimum supply voltage of 600 mV, lower than the threshold voltage, the topology presents almost rail-to-rail input and output swings and consumes only 550 nW.**

***Index Terms*—Bulk-driven differential pair, full swing, Miller operational transconductance amplifier (OTA), operational amplifier, rail to rail, ultra-low-voltage and ultra-low-power circuits.**

I. Introduction

THE term low-voltage CMOS was initially coined for circuits working under 3 V, on processes that used to work on a 5 V power supply. Presently, the power supply voltages are 3.3, 2.5, 1.8,and even 1.2 V on the recent 0.13-μm process, thus demanding a reformulation of the meaning of low-voltage CMOS. For the present manufacturing process, it is probably more useful to present a topology that works with 1 V on a 3.3-V process than a topology that works with a 0.8 V on a 1.2-V process, due to the differences of the transistors.

When considering the market trend towards low-voltage and low-power, the frequency response, the power supply voltage and consumption are the main specifications of the analog circuit design [1]–[3]. The speed of digital circuits improves as the power supply voltage is reduced. On the other hand, that is not true for analog circuits where the signal/noise ratio is always reduced. Nevertheless, the main drawback on implementing low-voltage CMOS circuits is the threshold voltage. On a 5- to 1.2-V power supply voltage reduction, the threshold was reduced from 0.8 to 0.35 V; satisfactory for digital circuits but extremely high for analog circuits, even working in weak inversion. Since the threshold voltages do not reduce satisfactorily, there is the need for alternative architectures that minimize their effects.

Unquestionably, the main part of an operational amplifier is the differential input pair, which can be implemented either as gate-driven or bulk-driven. The gate-driven operation of a rail-to-rail differential pair can be implemented using two or more differential pairs in parallel, where they can be in a complementary [4]–[6] or unbalanced configuration [7]. Those techniques require complex circuits to control the transistors bias currents in order to maintain a constant conductance over the entire signal swing range. Another option is the use of a simple differential pair with floating gates [8]–[10], in which the gate voltage is given by the input signal and an internal voltage feedback, thus providing a rail-to-rail operation.

One of the best approaches for low-voltage CMOS circuits is the bulk-driven differential pair, since it allows a large signal swing without cutting off the transistor [11]–[13]. However, the bulk–source transconductance g_{mb} is smaller than the gate–source transconductance g_m, and therefore, the unit gain bandwidth is smaller considering the same current.

In a way, there is a tradeoff between signal swing and frequency response. MOS transistors biased at higher current densities are faster, but require larger $V_{\rm DS}$ drops. Under weak inversion, the signal swing is larger than on strong inversion due to the low $V_{\rm DS}$, but the frequency response is reduced due to the extremely low currents. Since a circuit working on ultra-low-voltage and ultra-low-power is desired, weak inversion was used to implement the circuit presented in this work.

II. Weak Inversion Operation

The drain current $I_{\rm DS}$ of a MOS transistor in weak inversion is based on the channel diffusion current and can be given by (1), when referred to source voltage [14]; where I_S is the characteristic current, T the absolute temperature, n the inclination of the curve in weak inversion, k the Boltzmann constant, q the charge of the electron or hole. This expression is a consensus among the models EKV [3], BSIM3v3 [14] and ACM [15]

$$I_{\rm DS} = I_S \left(\frac{W}{L}\right) \exp\left(q\frac{V_{\rm GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-q\frac{V_{\rm DS}}{kT}\right)\right]. \quad (1)$$

Observe that if $V_{\rm DS} \geq 3$ kT/q, then the transistor will be saturated in weak inversion [3]. The transconductance g_m can be found as presented in (2), which is a function of current $I_{\rm DS}$ and factor n kT/q only

$$g_m = q\frac{I_{\rm DS}}{nkT}. \quad (2)$$

The dc parameters of the MOS transistor in weak inversion operation can easily be found using the minimum square method given by [16]. The transconductance g_{mb} can be found as given in (3), where γ is the body efffect coefficient and Φ_F is the Fermi potential [2]

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_F - V_{SB}}} g_m. \quad (3)$$

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The authors are with the Institute of Information Technology and Engineering Systems, Federal University Itajubá (UNIFEI), Itajuba 37500-903, Brazil (e-mail: luis@unifei.edu.br; tales@unifei.edu.br; moreno@unifei.edu.br).

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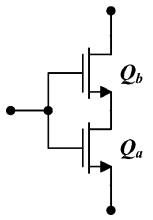

Fig. 1. Composite transistor with common well.

The transconductance g_{mb} varies from 20% to 30% of g_m for the same transistor in a CMOS process [2]. Therefore, it is possible to predict g_{mb} from g_m, and thus obtain the sizes of the transistors working in weak inversion.

An important configuration for MOS transistor in weak inversion is the composite transistor. The structure of an nMOS composite transistor is shown in Fig. 1 [17]. Consider that the transistors are implemented in the same well, since the substrate is common to all nMOS transistors in the CMOS process utilized [18].

The current and voltage expressions of the composite transistor can be derived directly from Fig. 1 and are given by (4), respectively. According to (1) and the conclusions given by [3], it is possible to relate current and voltage of the elements, as it will be explained

$$I_{\mathrm{DS}a} = I_{\mathrm{DS}b} \quad V_{\mathrm{DS}a} = V_{\mathrm{GS}a} - V_{\mathrm{GS}b}. \tag{4}$$

Considering that the drain–source voltage applied is enough to saturate transistor Q_b, then $V_{\mathrm{DS}a}$ is given by (5). This expression is a function of the transistor sizes and the CMOS process parameters, valid for weak inversion only and is independent of the transistor's gate–source voltage [17]. Therefore, a variation in $V_{\mathrm{DS}b}$ does not affect $V_{\mathrm{DS}a}$, so it is kept constant by cascode effect

$$V_{\mathrm{DS}a} = \frac{kT}{q} \ln\left(1 + \frac{\left(\frac{W}{L}\right)_b}{\left(\frac{W}{L}\right)_a}\right). \tag{5}$$

Observe that the drain–source voltage for saturation of transistor Q_a does not depend on the gate–source voltage. This is the basis of the composite transistor, which is valid only for weak inversion operation and not for strong inversion.

III. Improved Miller OTA Circuit

The circuit of an improved Miller operational transconductance amplifier (OTA) is shown in Fig. 2; thus called due to the improvements over the traditional Miller OTA [1]. A bulk-driven differential pair allows low-voltage operation of Miller OTA [2]. This is true because a transistor biased by the bulk and having maximum gate voltage is always active. In the circuit, if the common-mode voltage is close to the positive rail, the circuit is highly linear. On the other hand, if the common-mode voltage is close to the negative rail, the differential pair causes distortion to the signal, since the active load starts switching off. In order to solve this problem, two batteries are placed in series with the active load, to provide a dc shifting on the signal, as indicated in

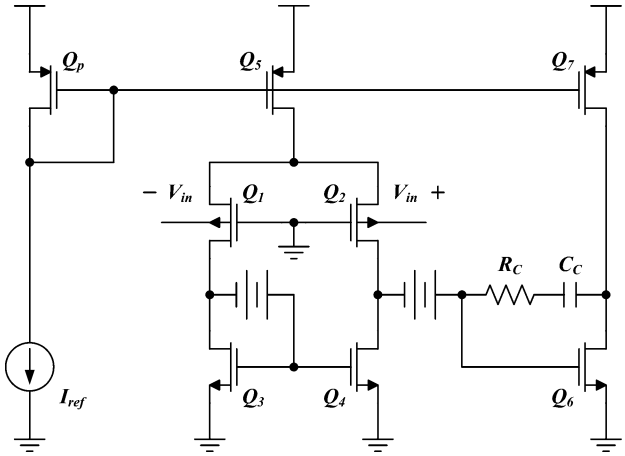

Fig. 2. Concept of the improved Miller OTA circuit.

Fig. 2. In this way, the active load remains operational with constant voltage for lower values of the input signal, thus avoiding non linearity conditions. If the common-mode voltage is close to the negative rail, the p-n junction of well–source of transistors Q_1 and Q_2 could be forwarded biased. Nevertheless, as it was experimentally confirmed by Blalock [11], it poses latch risk to the structure as long as the current in the bulk terminal is small, and should be carefully observed during the implementation of the project.

Obviously, circuits are not capable of generating voltages, but are capable of providing voltage drops, thus emulating batteries. A good option is the replacement of the battery by a common-gate amplifier. In terms of dc analysis, the transistor in diode configuration can be modeled by a resistance whose value is given by the inverse its transconductance, emulating a battery. Nevertheless, in terms of ac analysis, the transistor is an active load, and since the transistor is in saturation, it presents a gain. Therefore, it modifies the frequency response. The improved Miller OTA circuit is redrawn as shown in Fig. 3, in order to easily visualize the level shifters.

Observe that transistor pairs Q_{3a}–Q_{3b} and Q_{4a}–Q_{4b} form composite transistors. They allow the differential pair active load and the common gate amplifier to be biased by the same potential, without the use of additional biasing sources. From the composite transistor equations, it is possible to conclude that $V_{\mathrm{DS}3a}$ is given by (6). An analogous expression is obtained for $V_{\mathrm{DS}4a}$

$$V_{\mathrm{DS}3a} = \frac{kT}{q} \ln\left(1 + 2\frac{\left(\frac{W}{L}\right)_{3b}}{\left(\frac{W}{L}\right)_{3a}}\right). \tag{6}$$

In terms of dc analysis, voltages $V_{\mathrm{DS}3a}$ and $V_{\mathrm{DS}4a}$ are equal and constant. Therefore, voltages $V_{\mathrm{DS}1}$ and $V_{\mathrm{DS}2}$ should be equal and constant, thus optimizing matching of diferential pair Q_1 and Q_2, consequently reducing the differential offset voltage. The dimensions of transistors Q_8 and Q_9 should be carefully matched in order to avoid unbalance in the structure of the differential pair. Additionally, care should be taken in dc bias between stages in order to avoid any systematic offset at the output of the differential amplifier. Therefore, from the expressions of currents as functions of the transistors sizes, it

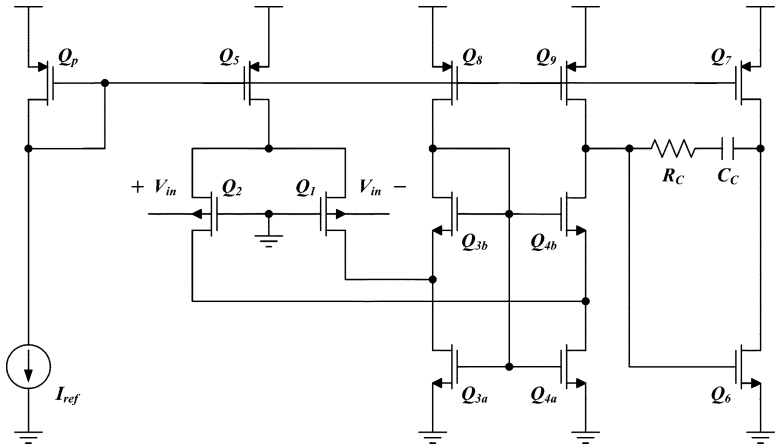

Fig. 3. Improved Miller OTA circuit using common gate as dc shifting.

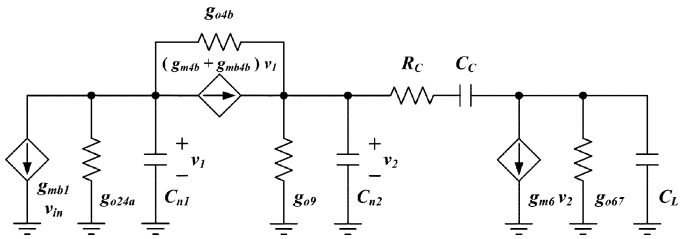

Fig. 4. AC model of the improved Miller OTA.

is possible to conclude that there will be no systematic offset voltage in the improved Miller OTA circuit, as long as (7) is satisfied

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_{4a}} = 2\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5 + 2\left(\frac{W}{L}\right)_9}. \tag{7}$$

Assuming that pMOS threshold voltage is higher than nMOS [18], then the minimum power supply voltage $V_{\rm DD}$ is defined by voltages $V_{\rm GS1}eV_{\rm DS5}$, as given by (8). Since $V_{\rm GS}$ in weak inversion is smaller than the transistor threshold voltage, the power supply voltage can be lower than the pMOS threshold voltage

$$V_{\rm DD}^{\rm MIN} \geq V_{\rm GS1} + V_{\rm DS5}^{\rm SAT}. \tag{8}$$

The ac small-signal model of the amplifier is defined by the elements on the nodes along the signal path. Considering the π model of the transistor, the OTA amplifier can be modeled as given by Fig. 4. g_m, g_{mb}, and g_o are obtained from dc biasing conditions; C_{n1} and C_{n2} are the parasitic capacitances between the source and drain nodes of transistor Q_{4b}, which is responsible for the dc shifing.

Now, applying the Laplace transform, considering pole separation and ignoring the parasitic capacitances at the other nodes, the circuit of Fig. 4 presents a gain, two real poles and one zero. Since A_o is independent of the frequency, it can be obtained directly equating the circuit without the capacitances, the open loop gain is given by

$$A_o = \frac{g_{mb1}g_{m6}}{g_{o67}\left(\frac{g_{oB}+g_{o9}}{g_{m4b}+g_{mb4b}+g_{o4b}}g_{o24a} + g_{o9}\right)}. \tag{9}$$

By equating the nodes of the circuit given in Fig. 4, it is possible to verify that the frequency of the dominant pole f_d is given by (10). The frequencies of the nondominant pole f_n and the zero f_z are given by

$$f_d = -\frac{g_{mb1}}{2\pi A_o C_C\left(1+\frac{g_{o24a}}{g_{m4b}+g_{mb4b}+g_{o4b}}\right)} \approx -\frac{g_{mb1}}{2\pi A_o C_C} \tag{10}$$

$$f_n = -\frac{g_{m6}}{2\pi C_L} \quad f_z = -\frac{1}{2\pi C_C\left(R_C - \frac{1}{g_{m6}}\right)}. \tag{11}$$

These amendments in the ac model do not change the position of the nondominant pole or the zero, when compared to the conventional Miller OTA model [1]. Nevertheless the open loop gain is higher than in the original, thus positioning the dominant pole further from the nondominant pole, thus improving the precision of the model. The value of resistor R_C allows a great flexibility in positioning the zero in the amplifier transfer function. If its value is equal to the inverse of the transconductance g_{m6}, then the zero will be positioned at infinity, thus eliminating its effect on the amplifier transfer function.

Based on the model, the zero and the poles are negative, since the transconductance, capacitance and resistance are defined positive. This characteristic defines the transfer function as minimum phase, a necessary condition to validate the criteria of stability given by the Bode diagrams.

The slew-rate can be obtained using a complex approach. Since neither of the diferential pair transistors is ever cut off, the drain current $I_{\rm DS5}$ never flows in only one of them. Therefore, the internal SR is given by the difference of the currents at these transistors after a sharp transistion at the input. The external SR is obtained similarly. Both slew-rates are given by (12). Those currents are not easily defined on the simplified model, since they take into account the substrate voltage, nevertheless, they can be easily obtained from the analysis of the operation point given by the simulations

$$SR_{\rm in} = \frac{I_{\rm DS1} - I_{\rm DS2}}{C_C}$$
$$SR_{\rm ex} = \frac{I_{\rm DS7} - (I_{\rm DS1} - I_{\rm DS2})}{C_L}. \tag{12}$$

TABLE I
TRANSISTORS AND OTHER ELEMENTS OF THE IMPROVED MILLER OTA

$(W/L)_{Q1}$	250 µm/1 µm	$(W/L)_{Q2}$	250 µm/1 µm
$(W/L)_{Q3a}$	100 µm/1 µm	$(W/L)_{Q3b}$	400 µm/1 µm
$(W/L)_{Q4a}$	100 µm/1 µm	$(W/L)_{Q4b}$	400 µm/1 µm
$(W/L)_{Q5}$	200 µm/9 µm	$(W/L)_{Q6}$	400 µm/1 µm
$(W/L)_{Q7}$	800 µm/9 µm	$(W/L)_{Q8}$	100 µm/9 µm
$(W/L)_{Q9}$	100 µm/9 µm	$(W/L)_{QP}$	200 µm/9 µm
C_C	5 pF	R_C	73.1 kΩ
C_L	15 pF	I_{ref}	130 nA

Unfortunately, a disadvantage of the bulk driven differential pair is its large input capacitance, when compared to the gate-driven approach. Nevertheless, since the main goal is low-voltage and low-frequency, this inconvenience is not a serious problem and can be easily overcome in the design.

The topology for rail-to-rail operation is simple yet efficient approaches for low-voltage design, where the operational amplifiers meet a wide range of applications.

IV. SIMULATIONS AND MEASUREMENTS OF THE IMPROVED MILLER OTA

In a unity gain buffer configuration, the amplifier should be capable of linear operation up to 1 kHz for a capacitive load of 15 pF with full rail-to-rail swing. Laker and Sansen [1] method was used to obtain the size of the transistors for the Miller OTA. By adapting that methodology, it is possible to calculate the dimensions of the transistors and elements as listed in Table I. The minimum expected power supply for the design is just 600 mV.

The weak inversion operation implies large transistor dimensions, which in turn minimizes the influence of noise, mainly the flicker noise that is domminant in a MOS transistor at low frequency [1], [2]. The improved Miller OTA circuit has an area of 300 μm$\times$ 200 μm.

As can be observed from (6), transistors Q_{3a} and Q_{4a} are not saturared in weak inversion. This is not critical in terms of ac model since it does not harm the circuit gain, as it can be seen by (9). Saturation of these transistors would require transistors Q_{3b} and Q_{4b} as being two and half times larger than the values adopted in Table I, thus penalizing circuit area.

The circuit was simulated in HSpice using BSIM3v3 model of a standard 0.35-μm n-well CMOS process from TSMC. The nMOS and pMOS threshold voltages are approximately 490 and 690 mV, respectively [18]. Fig. 5 shows a micrograph of the improved Miller OTA circuit.

The functionality tests show that the circuit closely follows the simulation results, thus demonstrating its functionality and its rail-to-rail swing capability. Fig. 6 presents the input (A1 channel) and output (A2 channel) waveforms of an improved Miller OTA connected as a unit gain buffer for a power supply of just 600 mV. The input is a 1-kHz sinusoidal signal of 300-mV amplitude and offset.

It is possible to verify visually the input/output rail-to-rail swing operation of the improved Miller OTA, at the maximum frequency, which shows distortions. Fig. 7 presents the measured slew-rate at maximum signal swing, for a power supply of 600 mV.

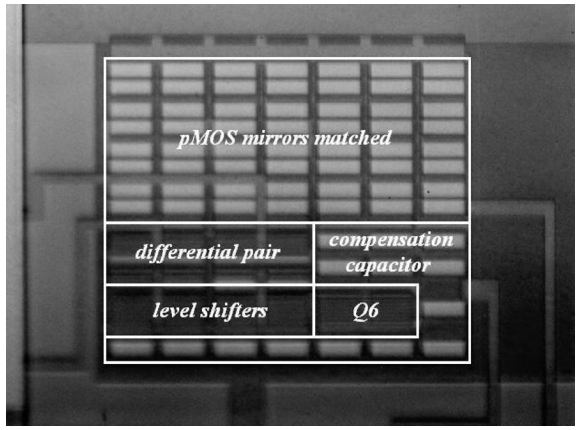

Fig. 5. Micrograph of the improved Miller OTA circuit.

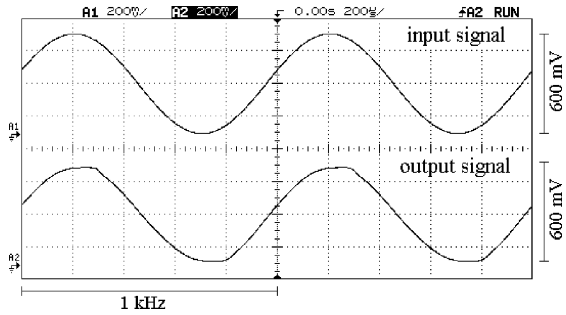

Fig. 6. Amplifier input (A1 channel) and output (A2 channel) waveforms with rail-to-rail at a 600-mV power supply.

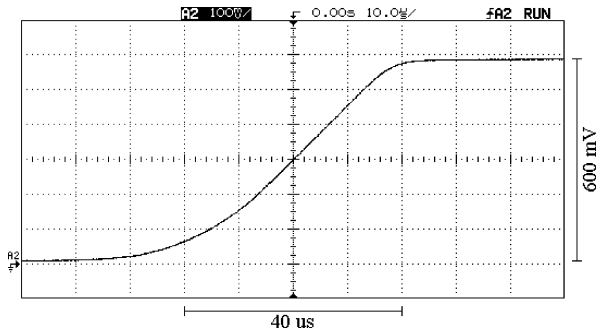

Fig. 7. Slew-rate of the improved Miller OTA at 600-mV supply.

Table II summarizes the comparison results of the simulated and the measured values. Every obtained result is in accordance to the circuit specifications. As can be observed from Fig. 6, the circuit presents distortion when operated with rail-to-rail at maximum frequency. The THD (total harmonic distortion) was obtained from a 260-mV 1-kHz sinus signal of millivolts offset, for a power supply of 600 mV. The signal swing was limited to the linear operation in a unit gain buffer configuration.

The measured results are very close to the simulated ones, thus showing the good approximation given by the BSIM3v3 model, even for operation in weak inversion region. This topology using only weak inversion transistors in a standard 0.35-μm CMOS process is capable of working with just 600 mV and consumes only 550 nW. The threshold voltages are approximately 690 mV for the pMOS devices and 490 mV

TABLE II
SIMULATED VERSUS MEASURED VALUES

	Simulation	Measured
Minimum power supply	600 mV	600 mV
Open loop gain	73.5 dB	69.4 dB
Unit gain frequency	13.02 kHz	11.35 kHz
Phase margin	54.1°	65.1°
Maximum signal swing	0 to 0.60 V	0 to 0.60 V
Linear signal swing	0.04 V to 0.56 V	0.04 V to 0.56 V
Offset voltage	–	3.0 mV
Slew-rate	14.7 V/ms	14.6 V/ms
CMRR @ 100 Hz	67.4 dB	74.5 dB
PSRR @ 100 Hz	58.1 dB	53.7 dB
Power consumption	550 nW	548 nW
THD_3 @ 520 mV_{p-p}	0.13 %	0.08 %
Input voltage noise @ 1 kHz	–	290 nV/√Hz

TABLE III
OPERATIONAL AMPLIFIER PERFORMANCE BENCHMARK INDICATORS

	This work	[12]	[19]
CMOS technology	0.35-µm	2.50-µm	–
Power supply	0.60 V	0.90 V	1.40 V
Unit gain frequency	11.35 kHz	5.60 kHz	14.00 kHz
Open loop gain	69.4 dB	70.0 dB	95.0 dB
Phase margin	65.1°	62.0°	65.0°
Signal swing	0 to 0.60V	0.01V to 0.89V	0.01V to 1.39V
Offset voltage	3.0 mV	2.6 mV	3.0 mV
Slew-rate	14.6 V/ms	–	3.0 V/ms
CMRR	74.5 dB	26.0 dB	60.0 dB
Power consumption	550 nW	450 nW	840 nW

for the nMOS devices, thus showing this topology works fine in weak inversion, since the power supply voltage is just 600 mV.

This circuit implementation is capable of working up to 1.5 V and still maintains the design specifications. At higher power supply voltages, the frequency response starts to degrade, especially the phase margin. The minimum measured power supply voltage is 500 mV, but the frequency response also deteriorates, especially the gain.

Table III shows a list of measured operational amplifier benchmarks used to evaluate this work. Features of the circuit (shown in Fig. 3) are listed in the first column, along with values of other works listed in other columns.

The improved Miller OTA can operate with a power supply voltage lower than 500 mV in a standard 0.25-μm CMOS process or even lower than 400 mV in a standard 0.18-μm CMOS process, due to their lower threshold voltages. These values were obtained using BSIM3v3 model and the typical values listed [18].

V. CONCLUSION

This work presented a simple rail-to-rail CMOS Miller OTA topology for ultra-low-voltage and ultra-low-power applications using dc shifting and bulk-driven differential pair configuration.

Since all transistors work in weak inversion, the presented topology is capable of running on a 600-mV power supply voltage and a power consumption of just 550 nW, in a 0.35-μm n-well CMOS process. The threshold voltages are 690 mV for pMOS transistors and 490 mV for nMOS transistors, thus showing that the architecture works beyond the limit given by the threshold voltages. The presented topology uses only 12 transistors and a few passive elements.

The circuit allows rail-to-rail swing at both input and output, and it is capable of low-voltage and low-power operation. The circuit can be used in ultra-low-power, ultra-low-voltage and high time constant applications, such as bandgap, physical transducers, process controllers and mainly on small battery operated devices.

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