THE DESIGN, MODELING AND OPTIMIZATION OF ON-CHIP INDUCTOR AND TRANSFORMER CIRCUITS

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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December 1999

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Abstract

On-chip inductors and transformers play a crucial role in radio frequency integrated circuits (RFICs). For gigahertz circuitry, these components are usually realized using bond-wires or planar on-chip spirals. Although bond wires exhibit higher quality factors (Q) than on-chip spirals, their use is constrained by the limited range of realizable inductances, large production fluctuations and large parasitic (bondpad) capacitances. On the other hand, spiral inductors exhibit good matching and are therefore attractive for commonly used differential architectures. Furthermore, they permit a large range of inductances to be realized. However, they possess smaller Q values and are more difficult to model.

In this dissertation, we develop a current sheet theory based on fundamental electromagnetic principles that yields simple, accurate inductance expressions for a variety of geometries, including planar spirals that are square, hexagonal, octagonal or circular. When compared to field solver simulations and measurements over a wide design space, these expressions exhibit typical errors of $2-3\%$, making them ideal for use in circuit synthesis and optimization. When combined with a commonly used lumped π model, these expressions allow the engineer to explore trade-offs quickly and easily.

These current sheet based expressions eliminate the need for using segmented summation methods (such as the Greenhouse approach) to evaluate the inductance of spirals. Thus, the design and optimization of on-chip spiral inductors and transformers can now be performed in a standard circuit design environment (such as *SPICE*). Field solvers (which are difficult to integrate into a circuit design environment) are now only needed to verify the final design.

Using these newly developed inductance expressions, this thesis explores how on-chip inductors should be optimized for various circuit applications. In particular, a new design methodology is presented for enhancing the bandwidth of broadband amplifiers using optimized area efficient, on-chip spirals. This method is applied in the implementation of a CMOS gigabit ethernet transimpedance preamplifier to boost the bandwidth by $\approx 40\%$.

This dissertation also develops a general methodology for computing the mutual inductance and mutual coupling coefficient of various on-chip spiral transformers. Furthermore, this work provides lumped, analytical transformer models that show good agreement with measurements.

Acknowledgments

My college years at Stanford have exposed me to a variety of challenging, invigorating and enjoyable experiences and I would like to take this opportunity to thank all the wonderful teachers, colleagues, staff, family and friends whom I have been fortunate to interact with during my lifetime.

I thank Prof. Tom Lee, my Ph.D. advisor, for sharing his passion and love for RF circuit design. He encouraged me to work on a variety of projects and thereby provided me with a well rounded perspective in engineering. His philosophy of researching fundamental issues that limit the availability of low-cost commercial electronics is both compelling and challenging. I am grateful to him for giving me the freedom to work on anything that fit within the above framework and for generating the funds required to build a state-of-the art RF laboratory. Above all, I thank him for his friendship, his natural charisma and great sense of humor.

I also thank Prof. Bruce Wooley and Prof. Stephen Boyd for serving on my oral examination committee and for reading my thesis. Prof. Bruce Wooley was my associate advisor, and I thank him for encouraging me at times when I needed it most. I am indebted to Prof. Stephen Boyd, who has treated me like one of his own students. His energy and enthusiasm for knowledge are boundless. Prof. Butrus Khuri-Yakub served as my undergraduate advisor and as my SURF (Summer Undergraduate Research Fellowship) faculty mentor. Without his whetting my appetite for research, I would not have continued on for Ph.D. I thank him for years of advice and friendship and for chairing the oral examination committee. I am also grateful to Prof. Simon Wong for his encouragement, advice and help on modeling on-chip transformers.

I appreciate my colleagues in CIS for creating a healthy and dynamic environment for conducting research. *SMIRC*, the research group headed by Prof. Tom Lee is certainly a dream team and it was a privilege and pleasure to work along side Tamara Ahrens, Rafael Betancourt, Dave Colleran, Joel Dawson, Ramin Farjad-Rad, Prof. Ali Hajimiri, Mar Hershenson, Hamid Rategh, Hirad Samavati, Dr. Derek Shaeffer, Dr. Arvin Shahani and Kevin Yu. Maria del Mar Hershenson and I have worked together on several projects and publications. In many ways, our strengths and traits complement each other well and I have learned much about time management and efficiency by observing her amazing ability to multi-task. Most importantly, I thank her for her dynamism, friendship and great sense of humor. Dr. C. Patrick Yue and I collaborated on the modeling of on-chip inductors and transformers and I would like to acknowledge him for a productive and enjoyable partnership.

Kevin Yu deserves recognition for building and supporting the computer infrastructure of our research group. Thanks to his zeal, vigilance and energy, our computer network has operated not only operated smoothly, but also has been endowed with several bells and whistles. Kevin also served the de-facto expert on fine dining and thanks to his influence, my appreciation for, and exposure to, haute cuisine has increased by several orders of magnitude.

During my PhD candidacy, I have been fortunate to share an office with Tamara Ahrens. The many compliments that our cubicle has received for its distinct character are all due to her unrelenting efforts and unbridled creativity. I thank her for spearheading the development of the RF design laboratory and for teaching and mentoring undergraduates with unparalleled passion and effervescent zeal.

I would also like to thank members of the GPS receiver project, (*Waldo*), for a memorable and laudable team effort. In particular, Dr. Derek Shaeffer, Dr. Arvin Shahani and I shared many wonderful adventures as we worked together to meet a variety of tapeout deadlines.

I am indebted to Greg Gorton and Ali Tabatabei for coordinating several tapeouts with National Semiconductor Inc., and to Jaeha Kim, Dr. Stefanos Sidiropoulos and Dr. Ken Yang for working selflessly on the CAD tools used to fabricate the chips. These folks (as well as several others) served well beyond the call of duty and

worked selflessly to make life substantially easier for the other students. I also feel very fortunate to have crossed the path of Bendik Kleveland, not only because of his technical expertise, but also because of his keen sense of humor. Robert Drost was another outstanding colleague whom I was lucky to work with on many class projects. I was also privileged to share many discussions on fundamental issues with Dr. Bharadwaj Amrutur and I am grateful to him for always providing a refreshing perspective and being a wonderful friend. I would also like to thank Jim Burnham, Eugene Chow, Dr. Katayoun Falakshahi, Arash Hassibi, Dr. Joe Ingino, Theresa Kramer, Sotirios Limotyrakis, Dr. Alvin Loke, Dr. Adrian Ong, Jeannie Ping-Lee, Won Namgoong, Dr. Sha Rabii, Theerachet Soorapanth, Dwight Thompson, Dan Weinlader, Gu-Yeon Wei for numerous technical (and not so technical) discussions that enriched my life at CIS.

The staff of CIS has been a pleasure to interact with. Ann Guerra deserves special recognition for her extraordinary efforts. Her ability to multi-task and coordinate several events simultaneously is what allows the research groups of Prof. Bruce Wooley and Prof. Tom Lee to operate smoothly. She can organize a space launch with a calm and poise that would make it seem like a routine evening stroll. Thanks, Ann for helping us, for keeping up our spirits, and for looking out for us.

The industry sponsors of CIS deserve special support for giving us the opportunity and funding to work at the frontiers of knowledge. I would like to thank IBM for fellowship support, HP and Tektronix for providing special deals on our test equipment and Rockwell and National Semiconductor for access to sub-micron CMOS processes. I am also indebted to Dr. Mehmet Soyer (IBM), Dr. Chris Hull and Dr. Paramjit Singh (Rockwell) for their support and advice. I would like to thank Dr. Richard Dasher, Carmen Miraflor, Maureen Rochford, Harrianne Mills and Joanna Evans for coordinating and organizing all the events with our industry sponsors.

I have enjoyed serving as a teaching assistant for a variety of undergraduate and graduate courses and laboratory classes. I thank my students for their zeal, commitment and desire for knowledge. I have learned so much from them. I am also grateful to the professors of the classes for which I served as a teaching assistant.

In particular I deeply appreciate the encouraging words and advise of Prof Connie Chang-Hasnain and Prof. Malcom McWhorter. Marianne Marx also deserves a big thank you for giving me the opportunity to serve as a teaching assistant. Additionally, the Stanford Center for Teaching and Learning will always have special place in my heart for sparking my interest in teaching during my undergraduate years.

Stanford is a exciting and invigorating place to learn and live. It brings together outstanding individuals in a variety of fields from many places in the world. My life has been enriched by their perspectives and values.

It was during my graduate years that I was fortunate to discover the joy of dance. I thank the Stanford Dance Division, the Stanford Ballroom Dance Club and the Viennese Ball Committees for introducing and guiding me to a passion that will reign forever. Dance was the biggest reason why my Ph.D. years were the most enjoyable of my college life.

The members of the Stanford Vintage Dance Ensemble deserve special mention: I will dearly miss our intense and fun-filled Tuesday night practices and our energetic performances. I thank you, my dance partners (particularly Laura Hill) for all the invigorating dances and for their their commitment to excellence. I also thank our director and choreographer Richard Powers, our choreographers and instructors (especially Monica and Ryan) and the Friends for Dance at Stanford building an enthusiastic and tightly knit dance family. May the invigorating flames of dance light up the souls of everyone.

During the course of my Ph.D, I have been rewarded with fantastic roommates. I would like to thank the residents of Crothers Memorial Hall (the engineering dorm) for a global, multi-cultural environment that provided delightful and insightful perspectives on life. Maria Meyer has simultaneously served as a surrogate mother, counselor, friend, peace-maker and office coordinator to more than a hundred students every year. My fellow graduate resident assistants (GRAs), Melissa Aczon, Mitch Oslick, and Francis Rotella were a pleasure to work with and I look forward to sharing many moments of laughter with them in the years to come. My good fortune with roommates continued when I moved off campus. Thank you, Arvin, Ashwini, Birdy, Jean-Michel and Vidya for sharing a part of your lives with me.

My friends, family and teachers have always been there for me. I have learned from them, grown up around them and shared many endearing moments with them. I wish I could acknowledge each of them in person, but that would double the size of this thesis.

To Amma (mother) and Appa (father): This dissertation is dedicated to you. You are an eternal source of inspiration, support and love. You have shown me how to find happiness in the small things in life and how to keep perspective. You have taught by example how to live a balanced and well-rounded life. Amma, your strength and courage was what allowed me to complete the Ph.D. Appa, you have guided and taken care of me both from heaven and earth. You taught me the value of optimism and patience, quintessential qualities for a PhD. I am what I am because of both of you you. I pray that I can bring up my children the way you brought me up.

To Krista: Thank you, my love, for coming into my life. You are my dream come true.

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Chapter 1

Introduction

THE explosive growth in commercial wireless and wired communication markets has generated tremendous interest in inexpensive radio-frequency integrated circuits (RFICs). Traditionally, RFICs have been mostly used in military applications and have been fabricated in expensive GaAs and silicon bipolar technologies. However the quest for low cost solutions in the commercial market has spurred a desire to implement RFICs in standard CMOS technology. The performance of standard CMOS technologies, thanks to the impetus of the microprocessor and memory markets, has improved constantly and consistently. In fact, submicron CMOS technologies now exhibit sufficient performance for radio frequency applications in the $1-5$GHz range, making them ideal for commercial applications. An additional advantage of these CMOS processes is that they permit the integration of the analog and digital components, the holy grail for "system-on-chip" solutions.

The advantages of integrating radio frequency circuits are compelling. The fewer the external components, the smaller the size of the circuit board and perhaps the smaller the power consumption. These two advantages are especially significant in the rapidly expanding personal communication services market where portability and long battery life are essential. Furthermore, integration enhances the reliability and robustness of the end product as it minimizes the number of external connections that require soldering. Component matching is also easier thereby offering the designer more flexibility to choose high performance architectures. Finally testing

time and cost, two key issues in the communications area where time to market is paramount, are reduced as the level of integration increases.

Among the common circuit elements, transistors, diodes, capacitors and resistors are easily integrated on chip, thanks to the research done for microprocessor and memory chips over the last thirty years. Although on-chip inductors and transformers have traditionally not been used in microprocessors or memories, they are finding increasing use in radio frequency circuits. All major components in a narrowband front-end system need inductors and transformers. These components include low-noise amplifiers (LNAs), oscillators, filters, baluns, matching networks and mixers. Thus, inductors and transformers account for a large fraction of the area (and cost) of RFICs [1, 2, 3, 4, 5, 6]. Consequently, the past decade has seen increased activity in their design, modeling and optimization.

Most of this modeling work has centered around the development of field solvers to predict the behavior of on-chip inductors and transformers. While accurate, these field solvers are time consuming, computationally intensive and require experience on the part of the user. These field solvers also do not provide any insight into the engineering trade-offs involved in the design of these on-chip inductors and transformers. Although the better field solvers are excellent for verification, they are inconvenient at the initial design and optimization stages.

To facilitate the design of inductor circuits, significant work has been done on modeling on-chip inductors using lumped circuit models [7, 8, 9, 10]. These lumped models are attractive as they are easily incorporated into a standard circuit design environment (such as *SPICE*). Furthermore, most of the parasitic capacitance and resistances in these models have simple, physically intuitive, analytical expressions. However, the inductance itself lacks a simple formula and therefore needs to be computed using a complicated segmented summation method. The lack of a simple, accurate inductance expression remains as a major impediment to using these lumped models for quick design and optimization.

In this thesis, we develop a theory based on fundamental electromagnetic principles that yields simple, accurate inductance expressions for on-chip spiral inductors of various geometries. We also use these expressions and concepts to develop a

lumped circuit model for on-chip spiral transformers. The work presented in this thesis forms a basis for using lumped circuit models to facilitate the design and optimization of inductor and transformer circuits.

1.1 Organization

Chapter 2 reviews the current state-of-the-art in modeling on-chip spiral inductors. After presenting the major modeling approaches, it elaborates on a popular lumped circuit model and highlights the lack of simple, accurate inductance expressions.

Chapter 3 introduces and develops a general theory based on current sheet approximations that permits the self and mutual inductances of a variety of geometries to be quickly calculated. The accuracy of the current sheet approximation is studied for key geometries and appropriate correction terms are presented to improve the accuracy of the inductance expressions. Particular attention is paid to geometries that approximate a square and circular spiral, permitting simple, accurate expressions to be developed for them.

Chapter 4 presents several simple accurate expressions for calculating inductances of on-chip spirals. First, the expressions derived from the theory described in chapter 3 are discussed. Second, special type of data-fitted expressions (called monomials) are described. These monomials can be used in special types of optimization routines called *geometric programs*, for which extremely fast solutions have been developed. Then, a third set of expressions, based on a modification of a simple expression developed by Wheeler are presented. These new expressions, as well as expressions reported previously in the literature, are compared to comprehensive field solver simulations spanning a wide design space. Finally, all these expressions are compared to measurement results. The accuracy of the new expressions show an order of magnitude improvement over previously published expressions, making them ideal for circuit design and optimization.

Chapter 5 treats the design and modeling of on-chip transformers. Several on-chip transformer realizations are described and compared with one another. Then, a general approach for modeling these realizations using a lumped circuit model is

presented. Finally, this approach is illustrated with several examples that show good agreement with measurements.

Chapter 6 illustrates how the simple, analytical inductance expressions can be used within a lumped circuit model of a spiral inductor to easily explore engineering trade-offs and to compare the performance of various geometries. It also investigates how on-chip inductors can be used as shunt-peaking elements to enhance the bandwidth of broadband amplifiers.

Chapter 7 studies how magnetic coupling to the substrate can degrade the performance of on-chip spirals. The current sheet approach discussed in chapter 3 is applied to obtain a simple expression that provides insight into the dominant parameters that degrade performance.

Chapter 8 summarizes the major contributions of this thesis and suggests areas that merit further work.

Chapter 2

Models and Inductance Expressions for On-Chip Spirals

In this chapter, we review on-chip inductor realizations and see how they are modeled. Section 2.1 discusses commonly used spiral geometries and identifies the lateral and vertical parameters that determine performance. Section 2.2 describes the common approaches used to model on-chip spirals. Section 2.3 examines the analytical expressions that exist for the elements in a commonly used lumped circuit model for on-chip inductors. Section 2.4 highlights the insufficient accuracy of previously published inductance expressions and underscores the need for developing simple, accurate inductance expressions that can be incorporated in the lumped circuit model.

2.1 On-chip Inductor Realizations

On-chip inductor implementations entail a myriad of trade-offs. In order to understand these trade-offs, we need to consider both the vertical and lateral geometries of the layout. Figure 2.1 shows a three dimensional view of a square spiral with 1.75 turns. Square spirals are popular because of the ease of their layout. Squares are generated easily even with simple Manhattan-style layout tools (such as MAGIC). However, other polygonal spirals have also been used in circuit design. Some designers prefer polygons with more than four sides to improve performance. Among these,

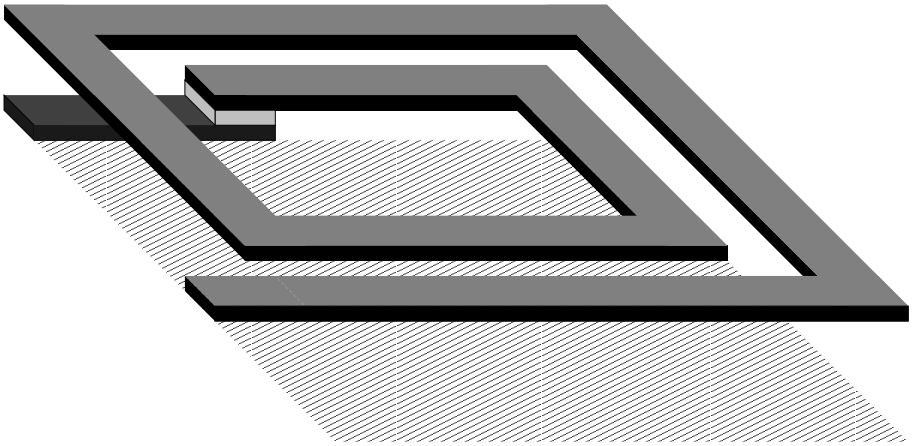


Figure 2.1: 3-D view of square spiral with 1.75 turns.

hexagonal and octagonal inductors are used widely. If desired, a circular spiral may be approximated by polygons with many more sides. Figures 2.2, 2.3, 2.4 and 2.5 show the layout for square, hexagonal, octagonal and circular spirals respectively. Some CAD tools such as *ASITIC* generate such layouts automatically [11].

The lateral parameters of a spiral are completely specified by the following:

1. number of turns, n
2. metal width, w
3. edge-to-edge spacing between adjacent turns, s
4. any one of the following: the outer diameter d_{out}, the inner diameter d_{in}, the average diameter $d_{\text{avg}} = 0.5(d_{\text{out}} + d_{\text{in}})$, or the *fill ratio*, defined as $\rho = (d_{\text{out}} - d_{\text{in}})/(d_{\text{out}} + d_{\text{in}})$. Note that $d_{\text{out}} = d_{\text{avg}} + n(w + s) - s$ and that $\rho = (n(w + s) - s)/d_{\text{avg}}$.
5. number of sides, N

While the inductance of an on-chip spiral is determined primarily by its lateral dimensions, its parasitic capacitances and resistances are determined by both the

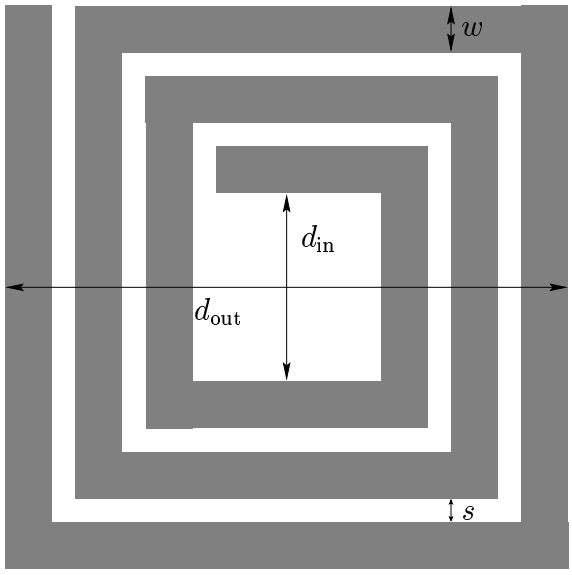


Figure 2.2: Square spiral.

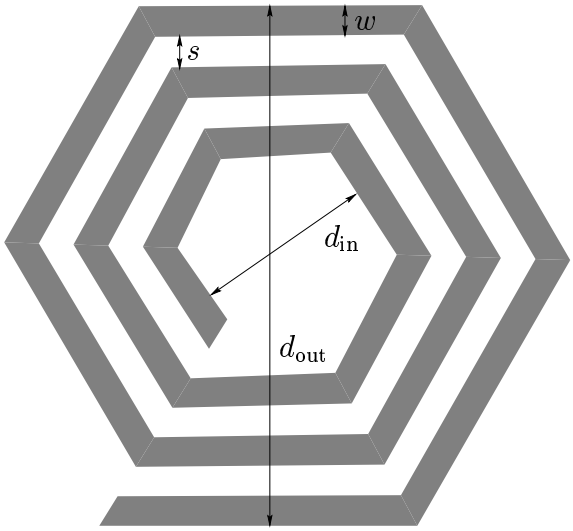


Figure 2.3: Hexagonal spiral.

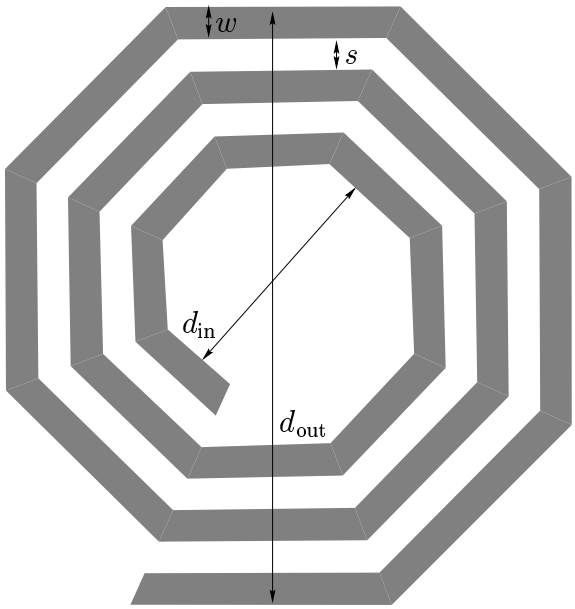


Figure 2.4: Octagonal spiral.

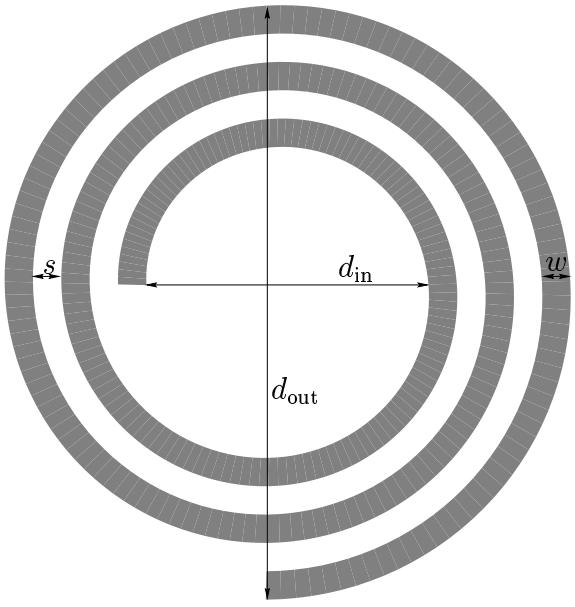


Figure 2.5: Circular spiral.

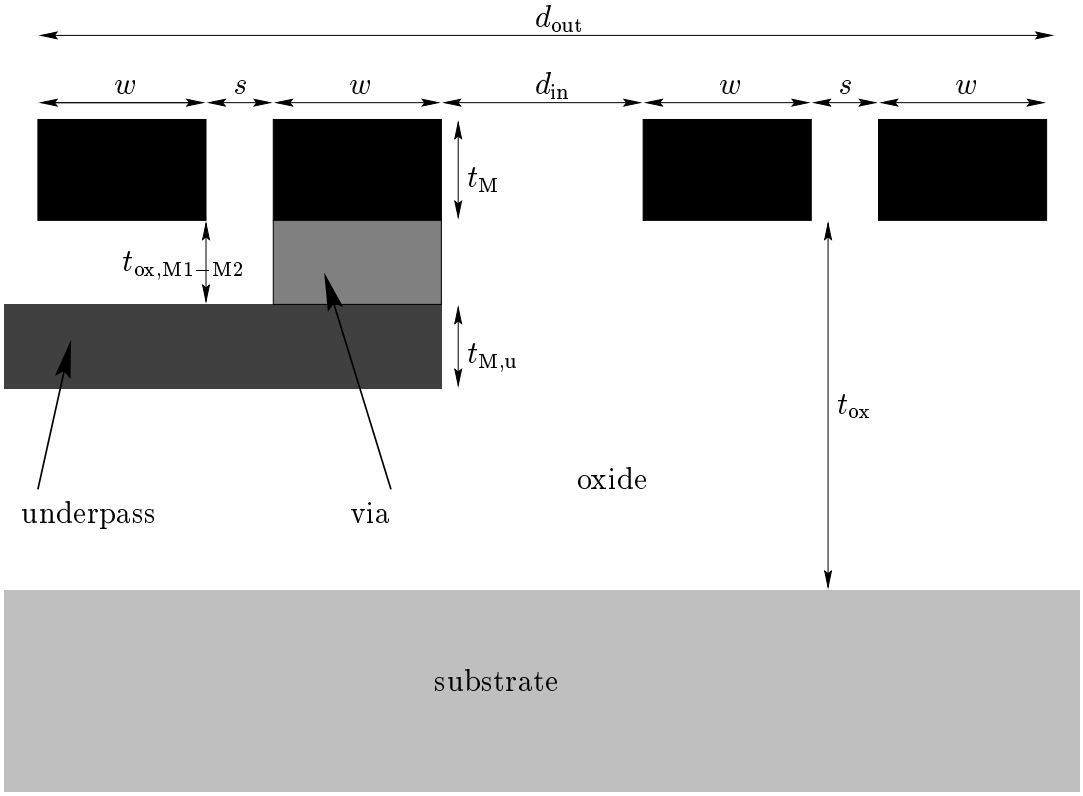


Figure 2.6: Vertical cross section of a square spiral with 1.75 turns.

lateral and vertical dimensions. The vertical cross section of a typical square spiral is illustrated in figure 2.6. Usually, the planar spiral is realized on the top metal layer to reduce the spiral-to-substrate oxide capacitance. In submicron CMOS technologies, the top metal layer has the largest thickness, thereby minimizing the DC series resistance of the inductor. The inner end of the spiral is connected by an underpass on a lower metal layer. Although the inductance and series resistance of this underpass is not significant in practical on-chip realizations, the feedthrough capacitance between the spiral and the underpass has a noticeable, but second order, effect on the overall performance.

Several variations on the spiral geometry exist. The spiral may be realized by strapping two or more metal layers together to reduce its series resistance. However

this reduction in resistance trades off with increased spiral-to-substrate capacitance. Furthermore, for GHz applications, the skin effect reduces the effective thickness of the conductors, thereby limiting the improvement offered by shunting metal layers [12].

Alternatively, multi-level series connected spirals may be used. Such implementations are useful when high inductance densities are desired or when magnetic coupling to the substrate needs to be minimized. The drawback with this approach is the low self resonant frequency stemming from the large feedthrough capacitance between the layers.

The optimal lateral and vertical parameters of a spiral are determined by the specifications of the circuit of which it is a part. The parasitic elements of an on-chip spiral entail important engineering trade-offs. Thus, these spirals need to be modeled properly to permit the designer to choose the optimal inductor for a given application. The next section discusses the relative merits of different modeling approaches.

2.2 On-Chip Inductor Modeling

The modeling of on-chip inductors can be classified into three major groups. In decreasing order of complexity, they are:

1. Field solvers
2. Segmented circuit models
3. Compact, scalable, lumped circuit models

The following subsections will examine these approaches.

2.2.1 Field Solvers

The most accurate approach to modeling any distributed electrical system is to solve Maxwell's equations subject to boundary conditions. Several general purpose

3-D electromagnetic simulators operate by solving Maxwell's equations numerically. *Maxwell*, *EM-Sonnet* and *MagNet* are examples of such tools ([13, 14]). Although accurate, these simulators are slow and are computationally intensive, both in memory and time. Thus, while these field solvers are suitable for accurately simulating simple structures, they are not suitable for simulating large three dimensional structures with multiple segments. On-chip spirals require long simulation times, access to fast processors and availability of substantial memory, factors that are aggravated by commonly encountered situations where the spacing between conductors is small compared to their width. Even the 'much faster' 2-D simulation of spiral inductors takes $10 - 15$ minutes per inductor [4]. Furthermore, since these simulators require both the lateral and vertical geometries to be specified, considerable experience is required on the part of the user to simulate on-chip inductors. For the reasons noted above, full fledged field solvers are not a practical option for on-chip inductor design.

To alleviate some of these issues custom field solvers, geared specifically for the simulation of on-chip spiral inductors and transformers, have been developed. These tools achieve faster simulation speeds by ignoring retardation effects so that magnetostatic and electrostatic approximations may used to quickly solve the field matrices. Some popular spiral inductor and transformer simulators are *SPIRAL* and *ASITIC* [11].

Although faster than the general purpose field solvers, these tools also suffer from several drawbacks. The use of these tools complicates the interface between the inductor model and the circuit simulator (such as *SPICE*). The best way to incorporate these field solvers in the design flow is to use them first to generate a library of inductors that span a wide design space and then link that library to the circuit simulator. Unfortunately, this requires new libraries to be generated for every process or, worse, an existing library to be updated even if only a few process parameters are changed. Another disadvantage is that several iterations (each involving the transfer of simulation data from the field solver to the circuit simulator) may be required to achieve the optimum design. Furthermore, this approach offers no design insight about engineering trade-offs. Thus field solvers are best suited to verify rather than design and optimize inductor circuits.

2.2.2 Segmented Circuit Models

A simpler approach entails the use of separate lumped π models for each segment of an inductor [6]. For example, a square inductor with n turns will have $4n$ segments, each with its own lumped model. Some additional terms are needed to model coupling between the segments and any associated bends.

Figure 2.7 illustrates this approach for a single turn of a square spiral. Each segment contains the conductor's self inductance, series resistance and the associated capacitances. A dependent current source is used to account for the mutual inductance between segments. The values of the resistances and capacitances are determined from process constants and frequency information. The self and mutual inductances are computed using the approach outlined by Greenhouse (in fact, the segment based approach was first proposed by Greenhouse to compute the total inductance of planar spirals) [15]. Although simpler than a field solver, the segmented model is very bulky and complicated. Thus, although it may be integrated into a circuit simulator environment, the complexity of the inductor model could easily surpass that of the remainder of the circuit, thereby compromising the speed of the circuit simulation. Furthermore, since the number of segments is determined by the product of the number of turns and the number of sides per turn, optimization of the complete circuit requires a script that can dynamically add or remove segments to the model. These considerations make the segmented model more cumbersome than a fast spiral inductor simulator such as *ASITIC*.

2.2.3 Compact, Lumped Models

The disadvantages of 3-D simulators and segmented models indicate the need for a compact, lumped inductor model that can be conveniently incorporated into a circuit simulator. Significant work has gone into modeling spiral inductors using such lumped circuit models [7, 8, 9, 10]. In these models, the spiral is represented by an equivalent π circuit with the inductance and series resistance in the series branch and the spiral-to-substrate capacitances and the substrate parasitics in the shunt branches.

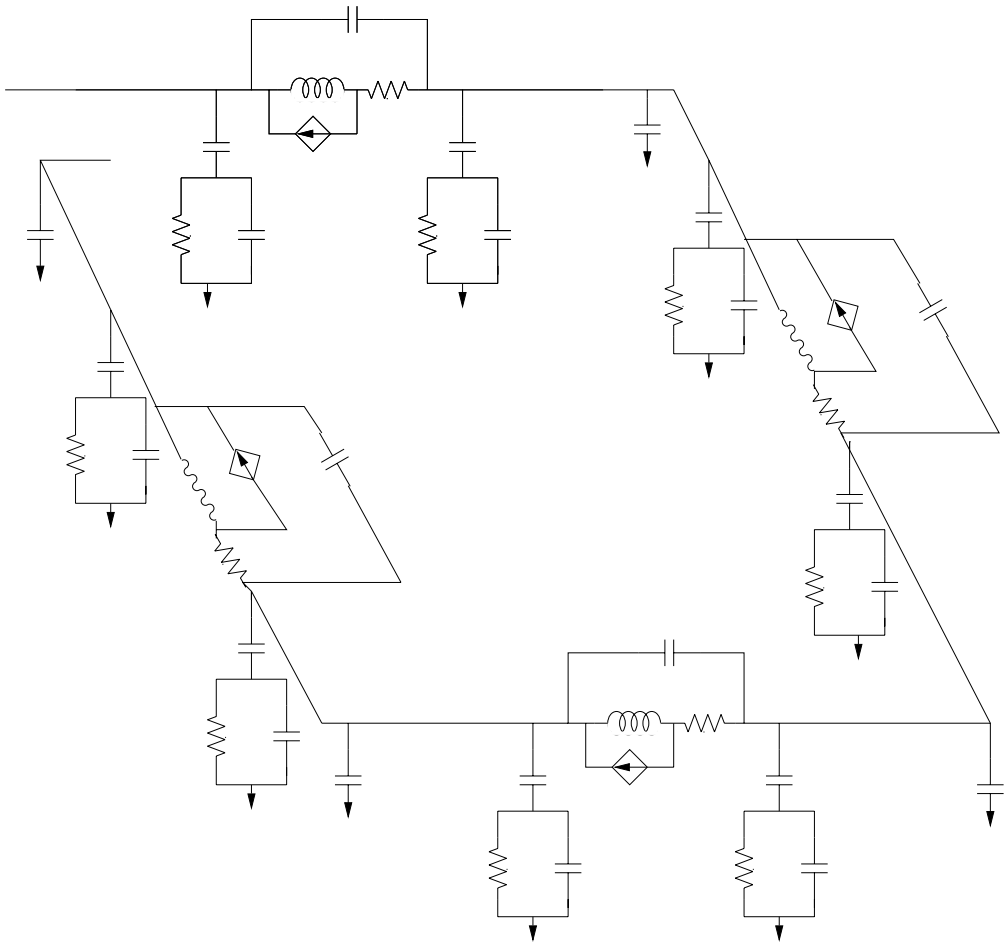


Figure 2.7: Segmented model for one turn of a square spiral.

As in the modeling of any distributed system, the accuracy of the lumped circuit approximation breaks down at higher frequencies [6]. However, the lumped models exhibit sufficient accuracy up to the self-resonant frequency of the spiral, which is the frequency range of interest as it represents the region where the spiral acts as an inductor. The speed, convenience and compactness of these lumped models make them ideal candidates for use in circuit design and optimization. The next section will describe how most elements in a popular lumped model may be represented by simple, analytical expressions.

2.3 Analytical Expressions for Elements in the Lumped Model

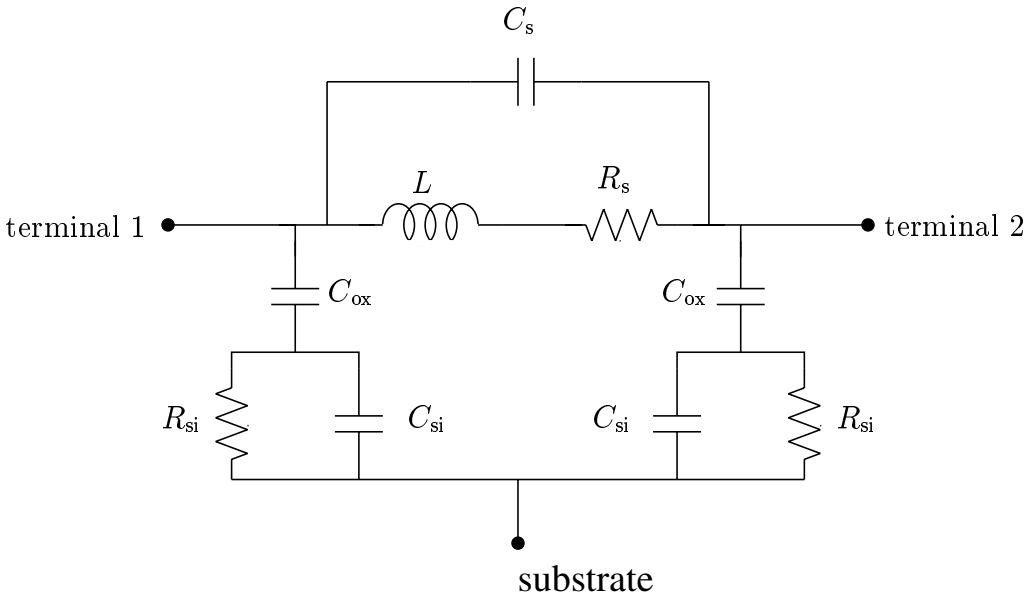


Figure 2.8: π circuit model of a spiral inductor.

A popular lumped model for a spiral inductor is shown in figure 2.8 [7]. The model includes the series inductance (L), the series resistance (R_s), the feedforward

capacitance (C_s), the spiral-substrate oxide capacitance (C_{ox}), the substrate capacitance (C_{si}) and the substrate spreading resistance (R_{si}). Although the parasitic resistors and capacitors in this model have simple, physically intuitive expressions, the inductance value itself lacks an accurate formula. We will now present analytical expressions for the parasitic elements. In these expressions, the term, l, refers to the length of the spiral, which is very well approximated as $l = nd_{\text{avg}}N\tan(\pi/N)$.

- $\boldsymbol{R_{\text{s}}}$**:** The series resistance of the spiral is given by

$$R_{\text{s}} \approx \frac{l}{\sigma w \delta(1 - e^{(\frac{-t}{\delta})})}, \tag{2.1}$$

  where σ is the conductivity, and t is the turn thickness and δ, the skin length, is given by $\delta = \sqrt{\frac{2}{\omega\mu_o\sigma}}$, where ω is the frequency, and μ is the magnetic permeability of free space ($\mu = 4\pi 10^{-7}\text{H/m}$). This expression models the increase in resistance with frequency due to the skin effect.

- $\boldsymbol{C_{\text{ox}}}$**:** The spiral-substrate oxide capacitance accounts for most of the inductor's parasitic capacitance. It is well approximated by:

$$C_{\text{ox}} \approx \frac{1}{2}\frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} lw, \tag{2.2}$$

  where ϵ_{ox} is the oxide permitivity ($\epsilon_{\text{ox}} = 3.4510^{-13}\text{F/cm}$) and t_{ox} is the oxide thickness between the spiral and the substrate.

- $\boldsymbol{C_{\text{s}}}$**:** This capacitance is mainly due to the capacitance between the spiral and the metal underpass required to connect the inner end of the spiral inductor to external circuitry. It is modeled by:

$$C_{\text{s}} \approx \frac{\epsilon_{\text{ox}}}{t_{\text{ox,M1-M2}}} nw^2, \tag{2.3}$$

  where $t_{\text{ox,M1-M2}}$ is the oxide thickness between the the spiral and the underpass.

- $\boldsymbol{C_{si}}$**:** The substrate capacitance is given by,

$$C_{si} \approx \frac{1}{2} C_{sub} lw, \tag{2.4}$$

where C_{sub} is the substrate capacitance per unit area. Since the substrate impedance is difficult to model, C_{sub} is generally treated as a fitting parameter.

- $\boldsymbol{R_{si}}$**:** The substrate resistance can be expressed as

$$R_{si} \approx \frac{2}{G_{sub} lw}, \tag{2.5}$$

where G_{sub} is the substrate conductance per unit area. Since the substrate impedance is difficult to model, R_{sub} is generally treated as a fitting parameter.

2.3.1 Patterned Ground Shield (PGS)

Among the parasitics elements discussed so far, the substrate capacitance and resistance are difficult to evaluate as their computation requires knowledge of the substrate doping. The placement of a patterned ground shield (PGS) beneath the spiral inductor eliminates this modeling uncertainty (except, of course, for the coupled magnetic loss) and may improve the inductor's performance. Figure 2.9 illustrates a typical PGS. The polysilicon ground shield is broken to prevent eddy currents from flowing in it. The outer edges of this broken shield are connected to ground thereby forcing most of the electric field to be terminated at the polysilicon boundary, thereby eliminating C_{si} and R_{si}. The trade-off is an increase in C_{ox} because of the reduction in effective oxide thickness:

$$C_{ox} \approx \frac{1}{2} \frac{\epsilon_{ox}}{t_{ox,po}} lw, \tag{2.6}$$

where $t_{ox,po}$ is the oxide thickness between the spiral and the polysilicon layer. The expressions for L_s,R_s and C_s are not altered by the PGS.

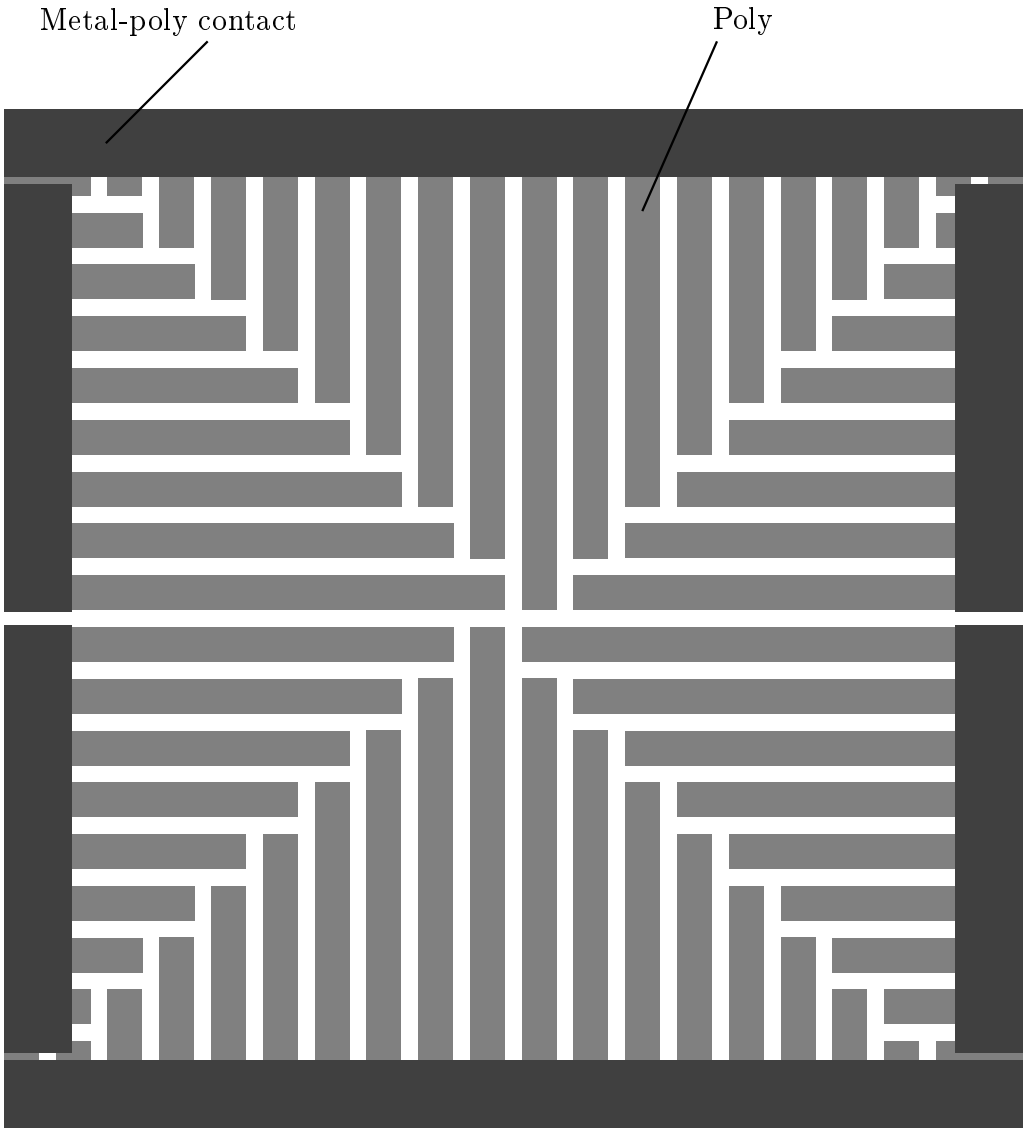


Figure 2.9: Patterned Ground Shield (PGS).

2.3.2 Limitations of the Compact, Lumped Model

Although the compact, lumped model captures the dominant parasitics, it has some drawbacks. The expression for the series resistance does not include the increase in resistance due to the proximity effect. The proximity effect arises because the current distribution within a spiral's conductor is influenced by the magnetic fields from the adjacent conductors. These fields reduce the effective cross sectional area of the conductor thereby increasing the series resistance. For practical spirals, the proximity effect is usually not significant compared to the skin effect and may therefore be ignored.

The lumped model accounts for the resistive and capacitive coupling to the substrate by incorporating the elements R_{si} and C_{si}. Energy in the spiral may also be coupled to the substrate by inductive means. In this case, the current in the spiral causes eddy currents to flow in the substrate, causing a mutual inductance between the spiral and the substrate. This mutual inductance increases with frequency as the skin depth of the substrate reduces and therefore results in increased energy being coupled to the substrate. This energy loss translates to an effective increase in the series resistance of the inductor. Thus, inductive coupling to the substrate can significantly degrade the performance of spiral inductors implemented in CMOS epi processes where the substrate has high conductivity. Chapter 7 treats this topic in more detail.

The biggest limitation of this compact, lumped model is in the calculation of the inductance itself. Unlike the other elements which have simple expressions, the inductance of the spiral is usually calculated using the Greenhouse method [7, 16, 15], which is based on a segmented summation approach. The number of segments in the spiral is determined by the product of the number of sides per turn and the number of turns. The self inductance of each of these segments and the mutual inductance between each of them is then evaluated and summed together to give the total inductance. The complexity of this summation increases as the square of the number of segments and therefore lacks a simple expression. Although the Greenhouse method offers sufficient accuracy and adequate speed, it cannot provide

an inductor design directly from specifications. Thus the absence of a simple accurate expression for the inductance diminishes the versatility of the lumped model and makes it inconvenient for circuit design and optimization.

The next section discusses simple expressions that have been reported in the literature for square spirals.

2.4 Previously Reported Inductance Expressions

In this section we describe some previously published formulas for square planar inductors. The simplest formula was proposed by Voorman [17]:

$$L_{\mathrm{voo}} = 10^{-3} n^2 d_{\mathrm{avg}}, \tag{2.7}$$

where the inductance is in nH, and d_{avg} is in μm. (We will use these units throughout the paper.) H. Dill [18] also published a formula similar to Voorman's formula,

$$L_{\mathrm{dil}} = 8.5 \cdot 10^{-4} n^{5/3} d_{\mathrm{avg}}. \tag{2.8}$$

These simple formulas use only the average diameter and the number of turns, and so not surprisingly exhibit typical errors of 40%, and in some cases errors as large as 80%.

H. Bryan [19] published an empirical formula for printed-circuit square inductors,

$$L_{\mathrm{bry}} = 2.41 \cdot 10^{-3} n^{5/3} d_{\mathrm{avg}} \log(4/\rho), \tag{2.9}$$

where ρ is the fill ratio defined as $\rho = (d_{\mathrm{out}} - d_{\mathrm{in}})/(d_{\mathrm{out}} + d_{\mathrm{in}})$. This formula gives a small improvement over Voorman's formula. Another formula with a similar improvement was obtained by H. Ronkanien *et. al* [20], who proposed a semi-empirical expression for the inductance,

$$L_{\mathrm{ron}} = 1.5 \mu_0 n^2 e^{-3.7(n-1)(w+s)/d_{\mathrm{out}}} \left(d_{\mathrm{out}}/w\right)^{0.1}. \tag{2.10}$$

Recently, J. Crols [8] published another empirical formula:

$$L_{\text{cro}} = 1.3 \cdot 10^{-4} (d_{\text{out}}^3 / w^2) \eta_a^{5/3} \eta_w^{1/4}$$

where η_a is the ratio of wire area to total area, and η_w is the ratio of wire width to turns pitch, *i.e.*, $\eta_w = w/(w+s)$. In terms of our previously defined variables we can express Crols' formula as

$$L_{\text{cro}} = 1.3 \cdot 10^{-3} d_{\text{avg}}^{1.67} d_{\text{out}}^{-0.33} w^{-0.083} n^{1.67} (w+s)^{-0.25}. \tag{2.11}$$

All of the expressions described above have significant systematic offset errors, *i.e.*, they tend to over- or underestimate inductance on average. However, even if the expressions are scaled to zero mean error (by multiplying each by a constant correction factor or adding a fixed offset) the errors are still typically around 15–20%, and in some cases larger. Therefore none of these expressions is good enough for use in a lumped circuit model that may be used for circuit design and optimization.

2.5 Summary

Although a compact, lumped model exists for spiral inductors, the absence of a simple, accurate expression for the inductance remains a major obstacle to its use in quick circuit optimization. The thrust of this thesis is to generate simple, accurate expressions for on-chip spirals. Chapter 3 develops a current sheet based theory that yields accurate expressions for a variety of spiral geometries. When combined with the lumped, circuit model discussed in this chapter, these new expressions provide a basis for optimizing inductor circuits quickly and easily.

Chapter 3

The Current Sheet Approach to Calculating Inductances

3.1 Introduction

Chapter 2 emphasized the lack of simple accurate expressions for spiral inductors as the major impediment to the optimization of circuits with on-chip inductors. In this chapter, we introduce a current sheet based approach that provides simple expressions for a variety of geometries. The purpose of this chapter is to generate accurate expressions for geometries that approximate square and circular spirals. The expressions developed here will be used in chapter 4 to calculate the inductance of on-chip spirals with an acceptable degree of accuracy.

In section 3.2 we consider line filaments. The treatment begins with the derivation of the mutual inductance between straight, parallel line filaments using the Neumann integral. We then present approximate expressions for some special cases that are valuable for engineers. Particular attention is paid to an approximate expression for the mutual inductance between two parallel lines of equal length (placed so that a line through their centers is orthogonal to the lines). This approximate expression contains a constant factor and three terms which are functions of the distance of separation between the two lines. The first term is proportional to the natural logarithm of this distance, the second is a proportional to this distance and

the third is proportional to the square of this distance. In section 3.3, we will see how a well defined transformation of this expression provides the basis for deriving simple (and accurate) expressions for the self and mutual inductances of conductors with uniform finite cross sections. This transformation is achieved by replacing the terms involving the distance of separation by functions of the mean distances of the finite cross sections. In particular, the natural logarithm term now becomes a function of the geometric mean distance (GMD); the linear term becomes a function of the arithmetic mean distance (AMD); and the quadratic term becomes a function of the arithmetic mean square distance (AMSD).

In section 3.4 we use the GMD, AMD and AMSD concepts to derive the self and mutual inductance of current sheets of various geometries. In keeping with the theme of obtaining expressions for on-chip spirals, the geometries considered serve as good approximations to the sides of a square spiral. Rectangular current sheets are considered first because of their simplicity. Then, trapezoidal current sheets are considered as they serve as more realistic approximation. In section 3.5 we expand our treatment to conductors with rectangular cross sections. Once again the GMD, AMD and AMSD serve as the bases for generating expressions for self and mutual inductances.

In section 3.6 we explore how the total inductance of a system of conductors can be computed by summation of the individual segments. Noting that the sides of on-chip spirals are made up of parallel (horizontal) conductors with identical cross sections and uniform spacing, we pay special attention to the computation of the total inductance of such an arrangement. In section 3.7 we use a current sheet approximation to obtain a simple expression for the total inductance of identical parallel conductors. We compare the more exact summation based method to our simple expression over a broad design space and identify the major correction terms that are needed to provide more accurate expressions. We do this by considering the GMD, AMD and AMSD segments of the expression and obtaining the most significant corrections in each of these segments for non-zero spacing and finite conductor thickness. We then compare our corrected expression to both the summation

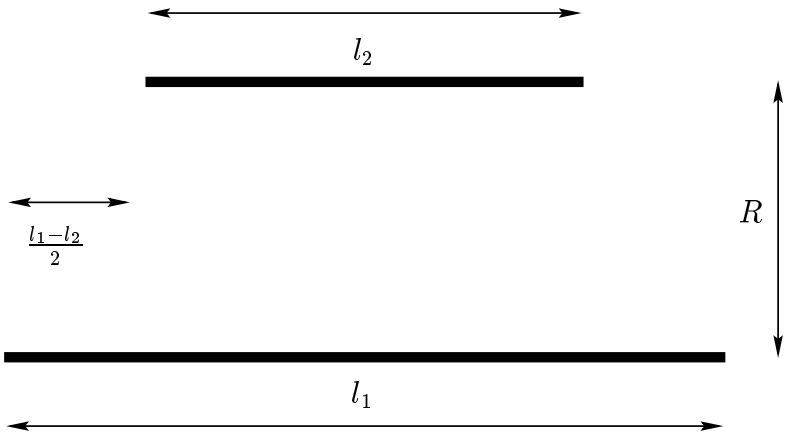


Figure 3.1: Two parallel lines

method and current sheet based approximation. In section 3.8 we extend our treatment to a system of parallel conductors with identical cross sections but unequal length. This configuration is chosen as it serves as an excellent representation of one side of a square spiral. In section 3.9, we consider a system of concentric, parallel, four-sided conductors that approximates all four sides of a square spiral.

In section 3.10, we complete our treatment by examining circular geometries. We start by considering concentric circular filaments and proceed to circular current sheets before looking at a system of concentric circular conductors with rectangular cross sections. The simple expressions that we obtain are useful in bounding the inductances of spirals made up of polygons with a large number of sides.

In section 3.11 we summarize our findings.

3.2 Line Filaments

For line filaments, the mutual inductance terms are evaluated using the Neumann double integral [21]:

$$M = \frac{\mu}{4\pi} \oint\oint \frac{1}{R} \mathbf{dl_1} . \mathbf{dl_2}, \tag{3.1}$$

where $\mathbf{dl_1}$ and $\mathbf{dl_2}$ are the vector current elements and R is the distance between the elements. Thus, the mutual inductance is proportional to the inner product of the vector current elements and is inversely proportional to the distance between them. The vector dot product quantifies the well known observation that the mutual inductance between two elements is a maximum when the current elements are parallel to one another and the current flow is in the same direction. When the current flow is in opposite directions, the mutual inductance is a minimum (and negative). When the current elements are in orthogonal directions, the mutual inductance is zero.

Equation 3.1 has analytical solutions for many cases of interest. Our treatment is limited to parallel lines that exhibit one or more axes of symmetry.

3.2.1 Parallel Line Filaments

We wish to compute the mutual inductance between two parallel lines for the case illustrated in figure 3.1. The lines are unequal in length and positioned so that a line through their centers is orthogonal to the two lines. For this case, the integral in equation 3.1 has a closed form solution. The expression for the mutual inductance evaluates to:

$$M_{line} = \frac{\mu}{2\pi}\left[\left(\frac{l_1+l_2}{2}\right)\ln\left(\sqrt{\left(\frac{l_1+l_2}{2R}\right)^2+1}+\left(\frac{l_1+l_2}{2R}\right)\right)-\sqrt{\left(\frac{l_1+l_2}{2}\right)^2+R^2}\right]$$
$$-\frac{\mu}{2\pi}\left[\left|\frac{l_1-l_2}{2}\right|\ln\left(\sqrt{\left(\frac{l_1-l_2}{2R}\right)^2+1}+\left|\frac{l_1-l_2}{2R}\right|\right)-\sqrt{\left(\frac{l_1-l_2}{2}\right)^2+R^2}\right]. \tag{3.2}$$

For lines of equal length, l, this expression simplifies to:

$$M_{line} = \frac{\mu}{2\pi}\left[l\ln\left(\sqrt{\left(\left(\frac{l}{R}\right)^2+1\right)}+\frac{l}{R}\right)-\sqrt{(l^2+R^2)}+R\right]. \tag{3.3}$$

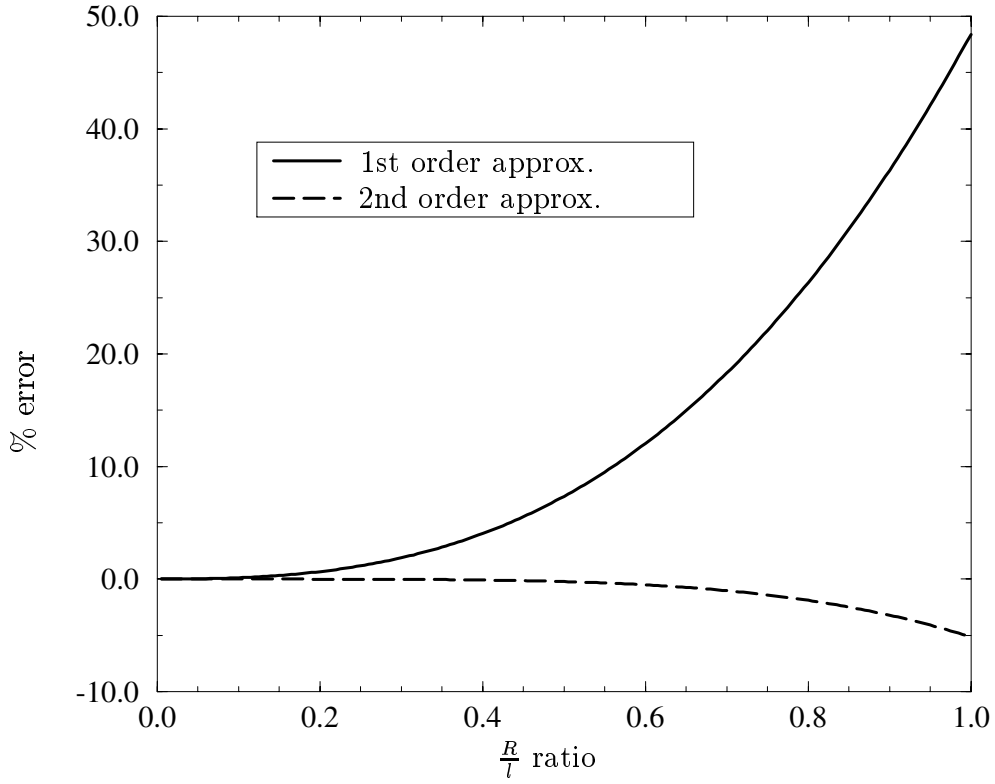


Figure 3.2: Accuracy of approximate mutual inductance expression for parallel line segments of equal length

As one may expect, the mutual inductance increases as the length increases and the distance of separation decreases. When $R \gg l$, we may simplify this expression by using a series expansion in terms of the quantity $(\frac{R}{l})$. For our purposes, only terms up to the quadratic one are needed:

$$M_{line} \approx \frac{\mu l}{2\pi}\left[\ln(2l) - \ln(R) - 1 + \frac{R}{l} - \frac{R^2}{4l^2}\right]. \tag{3.4}$$

Figure 3.2 compares equation 3.4 to the exact one for $\frac{R}{l} < 1$. The solid line is a first

order approximation which omits the quadratic term in equation 3.4. The dashed line represents equation 3.4. While the first order approximation is good to within 5% for $\frac{R}{l} < 0.4$, the second order approximation exhibits much better accuracy with errors within 5% for $\frac{R}{l} < 1$.

3.3 Extension to Conductors with Finite Cross Sections

Although valid strictly only for parallel line filaments, equation 3.4 forms the basis for deriving simple expressions for the self and mutual inductances of systems of conductors with finite cross sections.

We begin by noting that equation 3.4 contains three terms that are functions of the distance between the two lines, R. Among these three terms, the dominant one is proportional to $\ln R$. This term is followed in order of importance by first the linear term and then the quadratic one. In the case of parallel line filaments, the distance R is a constant. When equation 3.4 is extended to cases of finite conductor cross sections, the total inductance is now the weighted average of the mutual inductance between parallel line filaments separated by a distance R, where R is now a continuous variable that spans distances between all possible combination of points in the cross section [22]. Therefore, each of the three terms involving R is transformed to a mean distance that represents the weighted average of that term over all possible values of R.

By definition, the mean of the $\ln R$ term is replaced by the natural logarithm of the geometric mean distance (GMD), while R and R^2 terms are replaced by the arithmetic mean distance (AMD) and the arithmetic mean square distance (AMSD), yielding the following general approximate expression [22]:

$$M_{\text{gen}} \approx \frac{\mu l}{2\pi}\left[\ln(2l) - \ln(\text{GMD}) - 1 + \frac{\text{AMD}}{l} - \frac{\text{AMSD}^2}{4l^2}\right]. \tag{3.5}$$

Since equation 3.5 is a weighted average of equation 3.4, its accuracy is also determined by the ratio of the separation distance to the conductor length. Since equation 3.4 is accurate to within 5% for $\frac{R}{l} < 1$, equation 3.5 will also be accurate to within 5% as long as the maximum distance between two points on a cross section is smaller than the conductor's length.

The following subsections will examine the GMD, AMD and AMSD definitions in detail.

3.3.1 GMD

The geometric mean distance (GMD) of distances, d_1 and d_2 is given by the well known expression:

$$\text{GMD} = \sqrt{d_1 d_2}. \tag{3.6}$$

An equivalent representation is obtained by taking the natural logarithm of both sides so that

$$\ln(\text{GMD}) = \frac{1}{2}\left[\ln(d_1) + \ln(d_2)\right]. \tag{3.7}$$

An extension of this concept to n distances is straightforward and is given by:

$$\ln(\text{GMD}) = \frac{1}{n}\left[\ln(d_1) + \ln(d_2) \cdots + \ln(d_{\text{n}})\right]. \tag{3.8}$$

The GMD may also be used for multiple variables. Thus the GMD between p points on one set and q points on another set is:

$$\ln(\text{GMD}) = \frac{1}{pq}\left[\sum_{i=1}^{p}\sum_{j=1}^{q}\ln(d_{\text{i,j}})\right], \tag{3.9}$$

where $d_{\text{i,j}}$ refers to the distance between point i (on the first set) and point j (on the second set). Note that the base of the logarithm is irrelevant; we use the natural logarithm for consistency with earlier work.

The GMD may also be defined for distances involving continuous variables. As before, the logarithm of the GMD is simply the mean of the logarithm of the variable distances. The summations now become integrals. In fact, for purposes of calculating self and mutual inductances, the GMD is most useful in the integral form because practical cross sections are continuous rather than discrete.

The continous equivalent of equation 3.9 was first introduced as an aid in inductance calculations by Maxwell (see article 691 of [23]). Maxwell discussed the value of the GMD for cross sections that span two dimensions as well as one dimension. In particular, he highlighted that the sensible observations that the GMD of straight lines is useful in determining inductances of current sheets, whereas the GMD of rectangles is useful in determining inductances of conductors with rectangular cross sections.

He defined the GMD between two conductors with fixed cross sections of areas A_1 and A_2 as that value that satisfies the following relation:

$$A_1 A_2 \ln(\text{GMD}) = \iiiint \ln(r)\, dx\, dy\, dx'\, dy', \tag{3.10}$$

where "$dxdy$ is the element of area of the first conductor's cross- section, $dx'dy'$ is the element of area of the second conductor's cross-section, r is the distance between these elements, the integration being extended first over every element of the first section and then over every element of the second." In article 692, Maxwell goes on to list the values of GMD for several geometries and points out that the GMD definition is also valid for a single conductor: "It is not necessary that the two figures should be different, for we may find the geometrical mean of the distance between every pair of points in the same figure." Similarly, in [22], Rosa defined the GMD of a line from itself as the "n^{th} root of the product of the n distances between all the various pairs of points in the line, n being increased to infinity." For line filaments, the area integrals become line integrals and the quadruple integrals reduce to double integrals:

$$l_1 l_2 \ln(\text{GMD}) = \iint \ln(r)\, dx\, dx'. \tag{3.11}$$

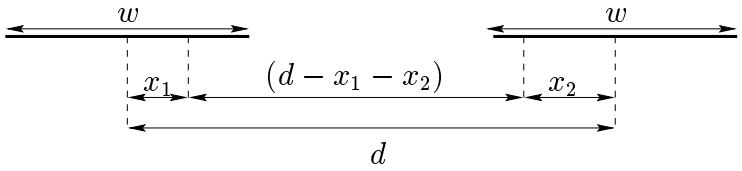


Figure 3.3: Two equal length straight lines on the same axis

Here l_1 and l_2 are the lengths of the two lines and dx and dx' are the elements of line of the first and second lines.

In general, the evaluation of the multiple integrals can be tedious! Even when closed form solutions exist, the results can be bulky and inconvenient. Fortunately, the GMD of geometries common to practical inductance calculations have simple forms. Maxwell, Rosa and Grover have already provided many useful relations for the GMDs of rectangular and circular geometries. In this section, we will illustrate the computation of the GMD for some very simple cases. We will consider the GMD between two equal, parallel straight lines as well as the GMD of a straight line from itself. We will then describe how these results may be extended using very good approximations to rectangular cross sections. All of these results will be used in the derivation of simple inductance expressions for spiral geometries.

Figure 3.3 illustrates two equal straight line segments of length, w, that lie on the same line and are separated by center to center distance, d. The GMD is given by appropriate substitution into equation 3.11:

$$\ln(\text{GMD}) = \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} \ln|d - x_1 - x_2| dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2}. \tag{3.12}$$

Although this integral has a closed form solution, the result does not provide much insight (see [24] for details). Instead, a series expansion of the result in terms of $\frac{w}{d}$ yields a more useful result:

$$\ln(\text{GMD}_{\text{2lines}}) \approx \ln(d) - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} \ldots \tag{3.13}$$

This result is widely used in calculations of the mutual inductance between straight parallel conductors. As expected, the GMD is smaller than the center-to-center distance, d. The difference between the natural logarithms of the GMD and d becomes more negative as w/d increases, implying that the ratio GMD$/d$ decreases as w/d approaches its maximum value of one. For most cases, only the quadratic correction term is needed. Even when $w/d = 1$, the exact value of GMD$/d$ deviates from the estimate using only the quadratic correction term by less than 3%.

In the same manner that the GMD between two distinct cross sections is used in mutual inductance calculations, the GMD of a single cross section is used in self inductance calculations. For example, the GMD of a straight line of length, w, is used in the calculation of the self inductance of current sheets. The result is:

$$\begin{aligned} \ln(\mathrm{GMD}_{1\mathrm{line}}) &= \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} \ln|x_1 + x_2| dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2} \\ &= \ln(w) - 1.5. \end{aligned} \tag{3.14}$$

The procedure for calculating the GMD of a rectangular cross section of width, w, and thickness, t, is more tedious. Although a closed form expression does exist [23], the exact result does not provide any insight. Fortunately, this expression may be approximated to an accuracy better than 0.5% by replacing w in 3.14 by $(w+t)$ [22]:

$$\ln(\mathrm{GMD}_{1\mathrm{rect}}) \cong \ln(w + t) - 1.5 \tag{3.15}$$

An accurate evaluation of the inductance requires the use of the AMD and AMSD in addition to GMD. In the two subsections we will examine the AMD and AMSD.

3.3.2 AMD

As we did for the GMD, we will first define the AMD for a single discrete variable and then extend the concept to multiple continuous variables. The arithmetic mean distance (AMD) of n distances is simply the mean of those distances:

$$\mathrm{AMD} = \frac{1}{n}\left[d_1 + d_2 \cdots + d_{\mathrm{n}}\right]. \tag{3.16}$$

The AMD may also be defined for multiple variables. Thus the AMD between p points on one set and q points on another set is:

$$\mathrm{AMD} = \frac{1}{pq}\left[\sum_{i=1}^{p}\sum_{j=1}^{q} d_{\mathrm{i,j}}\right], \tag{3.17}$$

where $d_{\mathrm{i,j}}$ refers to the distance between point i (on the first set) and point j (on the second set). This idea may be extended to cases where the distances involve continuous variables. Once again, the AMD is the mean of the variable distances.

The AMD between two conductors with fixed cross sections of areas A_1 and A_2 is that value which satisfies the following relation:

$$A_1 A_2 \mathrm{AMD} = \iiiint r\, dx\, dy\, dx'\, dy', \tag{3.18}$$

where $dxdy$ is the element of area of the first conductor's cross- section, $dx'dy'$ is the element of area of the second conductor's cross-section and r is the distance between these elements, the integration being carried out over all the elements of each cross section. For geometries involving lines, the area integrals become line integrals and the quadruple integrals reduce to double integrals:

$$l_1 l_2 \mathrm{AMD} = \iint r\, dx\, dx'. \tag{3.19}$$

Lengths l_1 and l_2 are those of the two lines and dx and dx' are the elements of line of the first and second lines.

The AMD of a straight line often arises in many inductance calculations. The AMD of a straight line of length, w, is::

$$\begin{aligned} \text{AMD} &= \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w}|x_1+x_2|dx_1dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w}dx_1dx_2} \\ &= \frac{w}{3}. \end{aligned} \tag{3.20}$$

The calculation of the AMD of a rectangle of length, w, and thickness, t is more complicated, leading to a complex closed form expression. However, an approximation (good to 2%) is given by:

$$\text{AMD}_{1\text{rect}} \cong \frac{\sqrt{w^2+t^2+0.46tw}}{3}. \tag{3.21}$$

As expected the expression is symmetric in w and t. For $w \gg t$, the AMD converges to $\frac{w}{3}$ and for $w \ll t$, the result converges to $\frac{t}{3}$, both of which are consistent with the observation that the AMD for a rectangle should approach that of a line as one of the dimensions vanishes.

3.3.3 AMSD

The arithmetic mean square distance, AMSD, between two conductors with fixed cross sectional areas A_1 and A_2 is the value that satisfies the following relation:

$$A_1A_2\text{AMSD}^2 = \iiiint r^2\,dx\,dy\,dx'\,dy', \tag{3.22}$$

where $dxdy$ is the element of area of the first conductor's cross- section, $dx'dy'$ is the element of area of the second conductor's cross-section and r is the distance between these elements, the integration being carried out over all the elements of each cross section. For geometries involving lines, the area integrals become line integrals and the quadruple integrals reduce to double integrals:

$$l_1l_2\text{AMSD}^2 = \iint r^2\,dx\,dx'. \tag{3.23}$$

Lengths l_1 and l_2 are those of the two lines and dx and dx' are the elements of the two lines.

The AMSD of a straight line is used in several inductance calculations. The AMSD of a straight line of length, w, is:

$$\begin{aligned} \text{AMSD}^2 &= \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} |x_1 + x_2|^2 dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2} \\ \text{AMSD} &= \frac{w}{\sqrt{6}}. \end{aligned} \tag{3.24}$$

Similarly, the result for the AMSD of a rectangle of length, w, and thickness, t, is:

$$\text{AMSD} = \frac{\sqrt{w^2 + t^2}}{\sqrt{6}} \tag{3.25}$$

3.3.4 Applications of GMD, AMD and AMSD

In the previous subsections, we obtained simple expressions for the GMD, AMD and AMSD of straight lines and rectangles. For some simple self inductance calculations, the GMD, AMD and AMSD of these cross sections may be substituted directly in equation 3.5 to obtain a simple accurate expression for the inductance. However, for mutual inductance calculations and for conductors with nonuniform cross sections, some variable transformation may be needed to elicit a simple expression. In particular, while the GMD between two cross sections will be used in many mutual inductance calculations, the corresponding AMD and AMSD will rarely be needed. The variable transformation usually results in the terms being condensed to some constants plus or minus the AMD and AMSD of a single cross section.

Greenhouse, in his often cited paper [15], defines the GMD between two conductors as "the distance between two infinitely thin imaginary filaments whose mutual inductance is equal to the mutual inductance between the two original conductors." Furthermore, he defines the GMD of a conductor's cross section as "the distance between two imaginary filaments normal to the cross section, whose mutual inductance is equal to the self inductance of the conductor." However, in an earlier paragraph

in the same paper, he presents the expression for the self inductance of a straight conductor in terms of *both* the GMD *and* the AMD! Clearly, these definitions are *inconsistent*. These definitions do not match the general mathematical definition of GMD, which was the form in which Maxwell introduced it in inductance calculations. The GMD is useful in calculating the mutual inductances between conductors only because computing the mean of the natural logarithm of the distances is *part* of the total solution.

In the following sections, we will use these results to derive inductance expressions for various current sheets and conductors with rectangular cross sections.

3.4 Current Sheets

The term current sheet refers to a conductive sheet with finite width and infinitesimal thickness. Although not realisable in practice, the current sheet concept serves as an adequate approximation for geometries where the conductor thickness is dwarfed by the length and width. The inductance of current sheets was first investigated by Rosa and Nagaoka in the early 1900s and was studied by various authors up to 1950 [22, 25]. However, as computers and numerical electromagnetic field solvers were developed, less attention was paid to current sheet based approximations.

In this section, we revisit current sheets and explore how current sheet approximations of various geometries can substantially simplify the computation of their inductance and yield simple, accurate expressions. First, we derive simple expressions for the self and mutual inductance of current sheets of various geometries. We illustrate the use of GMD, AMD and AMSD in inductance calculations by considering rectangular current sheets. We then consider self and mutual inductances involving trapezoidally shaped current sheets that approximate the sides of a square spiral. Later, we consider a four sided square current sheet that approximates an entire square spiral. We also study circular current sheets which serve as excellent approximations for polygonal spirals with more than four sides.

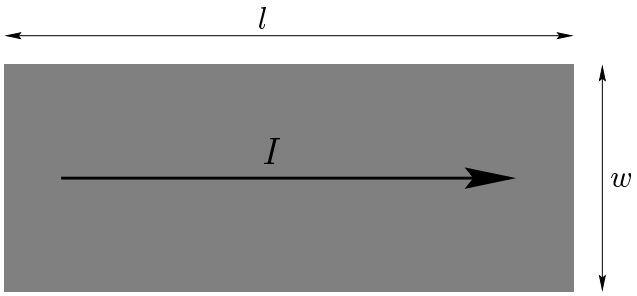


Figure 3.4: Rectangular current sheet

3.4.1 Self Inductance of a Rectangular Current Sheet

Figure 3.4 shows a rectangular current sheet of length, l, and width, w with $w < l$. The self inductance of this current sheet is obtained by substituting the GMD, AMD and the AMSD of the conductor's cross section in equation 3.5 [22] (see appendix A for a detailed derivation). In this case, the conductor cross section is a straight line of length, w. Hence:

$$\text{GMD} = we^{-1.5}, \tag{3.26}$$

$$\text{AMD} = \frac{w}{3}, \tag{3.27}$$

and

$$\text{AMSD} = \frac{w}{\sqrt{6}}. \tag{3.28}$$

Thus the self inductance of a current sheet is:

$$L_{\text{rectsheet}} = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{w}\right) + 0.5 + \frac{w}{3l} - \frac{w^2}{24l^2}\right]. \tag{3.29}$$

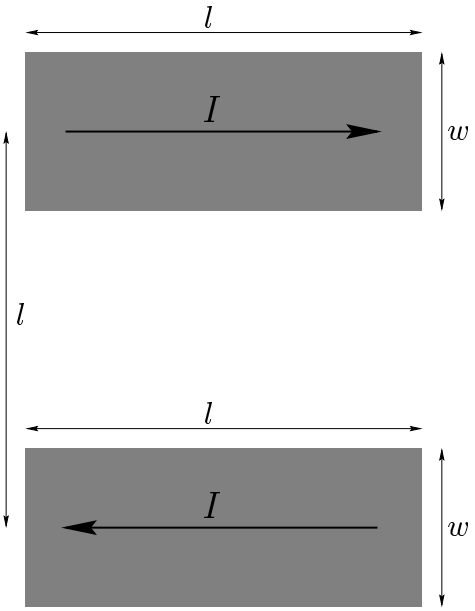


Figure 3.5: Parallel rectangular current sheets

3.4.2 Parallel Rectangular Current Sheets

Next, we compute the mutual inductance between two identical, parallel rectangular sheets of length, l, and width, w. The geometry is illustrated in figure 3.5. The sheets are separated by a center-to-center distance that is equal to the length of each sheet, l. This geometry provides a quick estimate of the mutual inductance between opposite sides of a square spiral. Thus the figure shows the two sheets carrying the same current in opposite directions. Since the center-to-center distance is equal to the length, $w < l$, we carry out a series expansion in terms of $\frac{w}{l}$. The calculation entails the GMD between two straight lines (of length, w) and the AMSD of a straight line (also of length, w). Details of the derivation are presented in appendix A. As the currents in the two sheets flow in opposite directions, the mutual inductance is negative:

$$M_{2\text{rectsheets}} \approx -\frac{\mu l}{2\pi}\left[\ln(1+\sqrt{2}) + 1 - \sqrt{2} + \frac{w^2\sqrt{2}}{24l^2}\right] \tag{3.30}$$

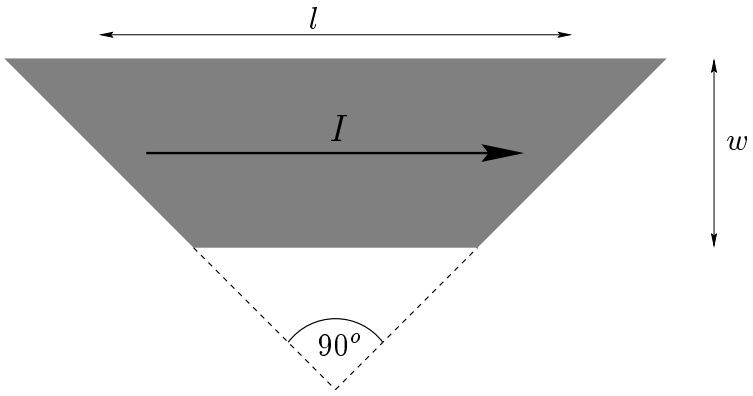


Figure 3.6: Trapezoidal current sheet

3.4.3 Self Inductance of a Trapezoidal Current Sheet

We now turn our attention to current sheets that approximate the sides of a square spiral. First we consider the self inductance of one side. To do so, we study the geometry illustrated in figure 3.6. Note that each of the non-parallel sides is at $\pi/4$ radians to the two parallel sides. This trapezoidal current sheet is fully characterized by its average length, l, and width, w so that the shorter of the parallel sides is of length $l - w$ and the longer $l + w$.

Once again, $w < l$, permitting an accurate series expansion in terms of $\frac{w}{l}$. Once again, the GMD, AMD and AMSD of a straight line are used. However, the computation is modified by correction terms that account for the variation in length. Details of the derivation are presented in appendix A. The result is:

$$L_{\text{trapsheet}} \approx \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{w}\right) + 0.5 + \frac{w}{3l}\left(\sqrt{2} - \ln(1+\sqrt{2})\right) + \frac{w^2}{24l^2}\right]. \tag{3.31}$$

Note that the first two terms are identical to the corresponding ones for a rectangular current sheet. The latter two (less significant) terms are similar in flavor.

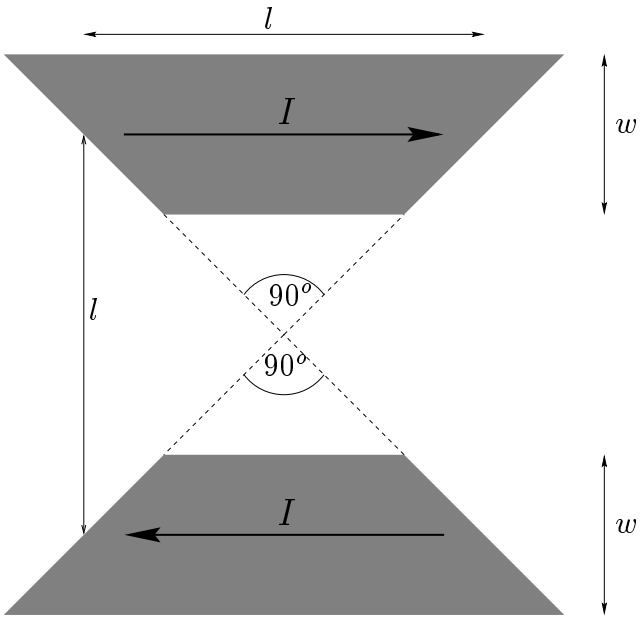


Figure 3.7: Parallel rectangular current sheets

3.4.4 Parallel Trapezoidal Current Sheets

We now consider a geometry that approximates the mutual inductance between two opposite sides of a square spiral. As one may expect, the geometry now entails two of the trapezoidal current sheets considered in the previous subsection. As illustrated in figure 3.7, the two parallel trapezoidal current sheets are identical and are fully characterized by the average length, l, and width, w. They are separated by a center-to-center distance that is equal to the average length, l. Note that the currents are equal and opposite. Once again, $w < l$, permitting an accurate series expansion in terms of $\frac{w}{l}$. Although the variation in length complicates the derivation (see appendix A for full details), the result is similar to the one derived for two parallel rectangular current sheets:

$$M_{\text{trapsheet}} \approx -\frac{\mu l}{2\pi}\left[\ln(1+\sqrt{2}) + 1 - \sqrt{2} - \frac{w^2}{12l^2}\right]. \tag{3.32}$$

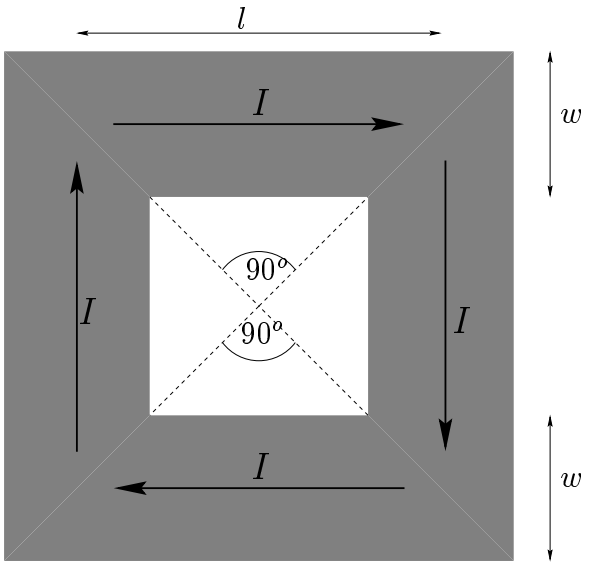


Figure 3.8: Four-sided square current sheet

The constant term is the same for both cases but the quadratic term has different signs. For the parallel rectangular current sheets, the mutual inductance increases as w/l increases because the distance between the inner edges of the sheets decreases. However, for trapezoidal sheets, the length of the inner edges decreases, while the length of the outer edges increases, causing a reduction in mutual inductance.

3.4.5 Four-Sided Square Current Sheet

Figure 3.18 shows a four sided current sheet. Each side is a trapezoidal current sheet similar to the ones considered in the previous two subsections, and is characterized by the average length, l, and width, w. Each side is perpendicular to its adjacent sides so that the mutual inductance between adjacent sides is zero. The total inductance of this geometry is easily calculated using the results for the self inductance of a trapezoidal current sheet and the mutual inductance between parallel trapezoidal current sheets. By symmetry, the total inductance is:

$$L_{\text{sq}} \approx 4(L_{\text{trapsheet}} + M_{\text{trapsheet}}). \tag{3.33}$$

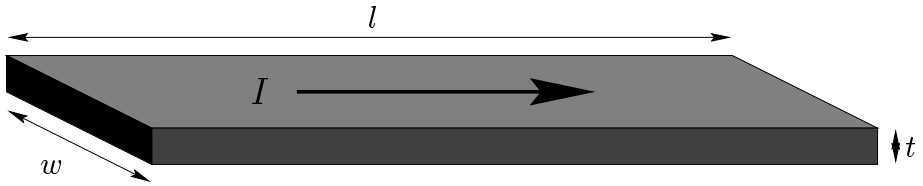


Figure 3.9: Rectangular conductor

Substituting from equations 3.31 and 3.32 we obtain:

$$L_{\text{sq}} = \frac{\mu l}{\pi}\left[2\ln\left(\frac{2.067l}{w}\right) + 0.36\frac{w}{l} + 0.25\frac{w^2}{l^2}\right] \tag{3.34}$$

This expression will be used to generate a simple expression for the inductance of on-chip square, planar spirals in chapter 4.

3.5 Straight Conductors with Rectangular Cross Sections

On-chip spiral inductors are made up of several straight conductors with rectangular cross sections, and thus calculating their values requires a good understanding of such conductors. In this section we develop expressions for the self and mutual inductance of conductors with rectangular cross sections. Once again the GMD, AMD and AMSD concepts serve as the basis for the inductance expressions.

3.5.1 Straight Conductor with Rectangular Cross Section

Figure 3.9 shows a straight conductor of length, l, with rectangular cross section of width, w, and thickness, t. We assume that the length exceeds the maximum distance of the cross section so that $l > \sqrt{w^2 + t^2}$. The self inductance of this

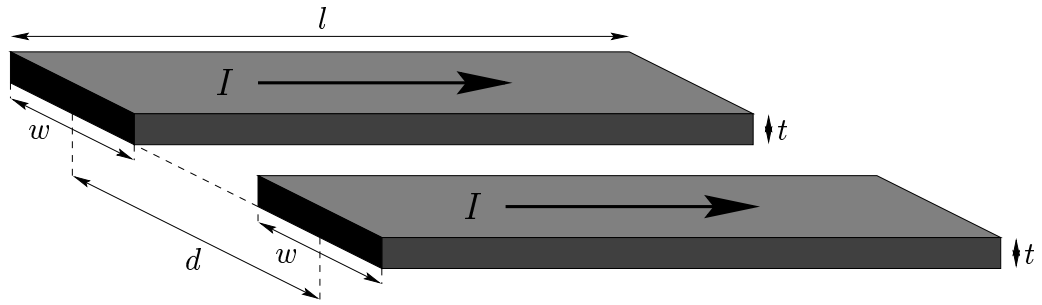


Figure 3.10: Parallel rectangular conductors

conductor is obtained by substituting the GMD, AMD and AMSD of a rectangle in equation 3.5. We use the results from section 3.3 :

$$GMD_{\text{rect}} = (w+t)\exp^{-1.5}, \tag{3.35}$$

$$AMD_{\text{rect}} \cong \frac{\sqrt{w^2+t^2+0.46tw}}{3}, \tag{3.36}$$

and

$$AMSD_{\text{rect}} = \frac{\sqrt{w^2+t^2}}{\sqrt{6}}. \tag{3.37}$$

Hence, the self inductance of this straight rectangular conductor is:

$$L_{\text{rect}} = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 + \left(\frac{\sqrt{w^2+t^2+0.46tw}}{3l}\right) - \left(\frac{w^2+t^2}{24l^2}\right)\right]. \tag{3.38}$$

3.5.2 Mutual Inductance between Two Identical Straight, Parallel Conductors of Rectangular Cross Section

We wish to compute the mutual inductance for the geometry illustrated in Figure 3.10. Two identical conductors of length, l, and rectangular cross section of width, w, and thickness, t, are placed parallel to one another. They are separated

by a center-to-center distance d. The edge-to-edge spacing is s so that $d = w + s$. In this case, the exact computation of the mutual inductance is tedious. However, by noting that $w < d$ and by assuming that $t < d$, we can obtain a very accurate expression:

$$\begin{aligned} M_{2\text{rects}} \approx & \frac{\mu l}{2\pi}\left[\ln\left(\frac{\sqrt{(l^2+d^2)}+l}{d}\right) - \frac{\sqrt{(l^2+d^2)}}{l} + \frac{d}{l}\right] \\ & + \frac{\mu l}{2\pi}\left[\frac{w^2 l}{12d^2\sqrt{l^2+d^2}} - \frac{t^2 l}{12d^2(d+\sqrt{l^2+d^2})}\right]. \end{aligned} \tag{3.39}$$

The first line of this expression is simply the mutual inductance between two line filaments that are placed at the center of each conductor. The second line includes the correction terms for the finite width and thickness. As one may expect, these terms are most important when w/d and t/d approach one. Note that when $t = 0$, the expression reduces to the one describing the mutual inductance between two identical, parallel current sheets (equation 3.30).

Equation 3.39 differs from the corresponding expression given by Greenhouse:

$$M_{2\text{rects}} = \frac{\mu}{2\pi}\left[l\ln\left(\frac{l+\sqrt{l^2+\text{GMD}^2}}{\text{GMD}}\right) - \sqrt{l^2+\text{GMD}^2} + \text{GMD}\right]. \tag{3.40}$$

Greenhouse obtains his expression by replacing the distance of separation parameter in the expression for the mutual inductance between equal length, parallel line filaments by the GMD. Greenhouse assumes that the thicknesses are negligible and uses the GMD between two lines:

$$\ln(\text{GMD}_{2\text{lines}}) = \ln(d) - \frac{w^2}{12d^2} - \frac{w^4}{60d^4}\ldots \tag{3.41}$$

Although the Greenhouse approach violates the definition of GMD, the final result is good enough for most engineering purposes. However the computation is unnecessarily complicated and lacks insight. Furthermore the use of more terms in the series expansion for the GMD is useless as the accuracy of equation 3.40 is limited by the incorrect use of the GMD. On the other hand, our approach is more accurate,

less complex and clearly shows the effect of the conductor's width and thickness on the mutual inductance.

3.6 Total Inductance of a System of Conductors

In this section, we examine a system of conductors and understand how the total inductance of the system may be evaluated. We consider the general problem of n conductors, each carrying the same current. The total inductance is given by:

$$L_T = \Sigma L_i + \Sigma M \tag{3.42}$$

where ΣL_i denotes the sum of self inductances of the conductors and ΣM denotes the sum of all the mutual inductances. Hence, the problem boils down to computing n self inductance terms and $(n^2 - n)$ mutual inductance terms:

$$L_{\mathrm{T}} = \sum_{i=1}^{n} L_i + \sum_{i=1}^{n} \sum_{j=1, j\neq i}^{n} M_{i,j}, \tag{3.43}$$

where L_i denotes the self inductance terms, and $M_{+,ij}$ denotes the mutual inductance terms. A matrix representation allows one to visualize the terms better. Since reciprocity holds ($M_{i,j} = M_{j,i}$), we obtain a symmetric matrix implying that we only need to compute half of the $(n^2 - n)$ mutual inductance terms:

$$\mathcal{M}_{gen,i,j} = \begin{bmatrix} L_1 & M_{1,2} & \dots & M_{1,(n-1)} & M_{1,n} \\ M_{1,2} & L_2 & \dots & M_{2,(n-1)} & M_{2,n} \\ \dots & \dots & \dots & \dots & \dots \\ M_{1,(n-1)} & M_{2,(n-1)} & \dots & L_{(n-1)} & M_{n,(n-1)} \\ M_{1,n} & M_{2,n} & \dots & M_{n,(n-1)} & L_n. \end{bmatrix} \tag{3.44}$$

The general problem of computing these self and mutual inductance terms can be very difficult. Even if one were to assume n straight, parallel conductors with uniform cross sections and uniform current densities, the overall computation has complexity

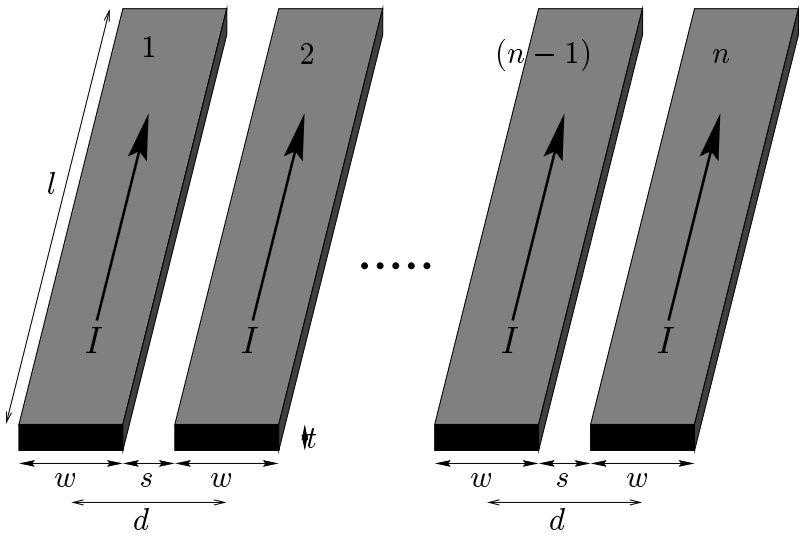


Figure 3.11: Equally spaced parallel rectangular conductors

of order n^2. In the next section, we will consider a simplified version of this problem that is more relevant to the evaluation of inductances of on-chip spirals. The simplifications will yield a system with complexity of order n and enable us to gain an appreciation for the issues at hand.

3.6.1 Parallel Conductors with Identical Dimensions

We simplify the general problem by assuming that all n conductors are identical, with length, l, and rectangular cross section of width, w, and thickness, t. We will also assume that the conductors are parallel to one another and that they are uniformly spaced with edge-to-edge spacing, s. This configuration is illustrated in figure 3.11. We assume that each conductor carries the same current and that this current is uniformly distributed over the entire cross section. Since the conductors are identical, their self inductances are all equal. Furthermore, the uniform spacing of the conductors indicates that only $(n-1)$ different spacings exist, implying that

only $(n-1)$ mutual inductance terms need to be computed. The inductance matrix may be simplified accordingly:

$$\mathcal{M}_{eq,i,j} = \begin{bmatrix} L_1 & M_{1,2} & \dots & M_{1,(n-1)} & M_{1,n} \\ M_{1,2} & L_1 & \dots & M_{1,(n-2)} & M_{1,(n-1)} \\ \dots & \dots & \dots & \dots & \dots \\ M_{1,(n-1)} & M_{1,(n-2)} & \dots & L_1 & M_{1,2} \\ M_{1,n} & M_{1,(n-1)} & \dots & M_{1,2} & L_1 \end{bmatrix} \tag{3.45}$$

The self inductance of one conductor can be calculated using equation 3.38. The mutual inductance between two conductors can be evaluated using equation 3.39 There are n self inductances, each of value L_1, $2(n-1)$ mutual inductances with $d = (w+s)$, $2(n-2)$ mutual inductances with $d = 2(w+s)$, and so on up to 2 mutual inductances with $d = (n-1)(w+s)$. The total inductance reduces to:

$$L_{\mathrm{T}} = nL_1 + 2\sum_{i=1}^{n-1}(n-i)M_{i,j}(d = i(w+s)). \tag{3.46}$$

Despite the simplifications made to reduce the complexity to order n, we still lack a simple expression for the total inductance. In the next section we will see how a current sheet approximation of this problem leads to a simple solution.

3.7 Current Sheet Approximation

Figure 3.12 shows how we convert a problem with n identical parallel, uniformly spaced straight conductors into one of a single equivalent current sheet. In order to obtain a simple expression for the equivalent current sheet we must assume that its total width, $(nw + (n-1)s)$, is less than its length, l. This assumption, which is valid in the context of on-chip spirals, allows us to use equation 3.29 to evaluate the

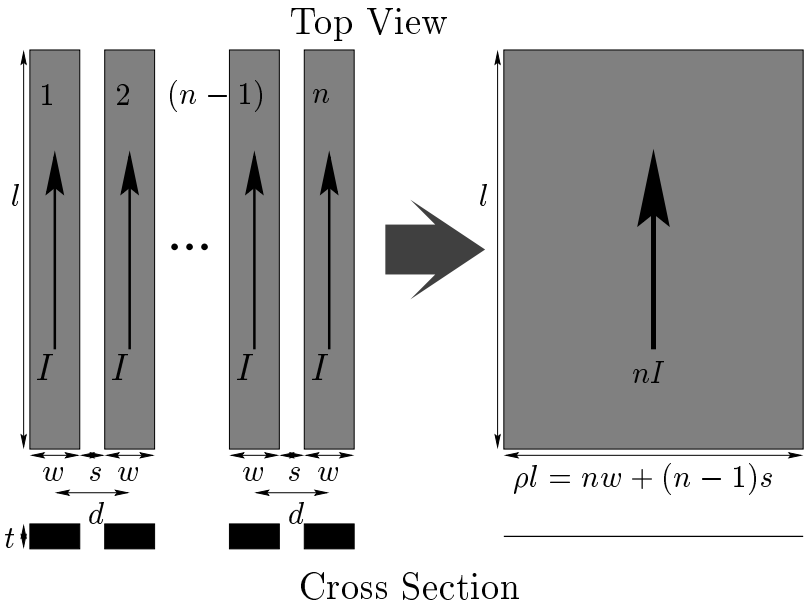


Figure 3.12: Equivalent current sheet representation

total inductance. First, we simplify notation by introducing the variable ρ, which is the ratio of the width of the current sheet to its length:

$$\rho = \frac{nw + (n-1)s}{l}. \tag{3.47}$$

The resulting current sheet expression is:

$$L_{\text{nrectsheet}} \approx \frac{\mu n^2 l}{2\pi}\left[\ln\left(\frac{2}{\rho}\right) + 0.5 + \frac{\rho}{3} - \frac{\rho^2}{24}.\right] \tag{3.48}$$

This result is identical to equation 3.29 except for the n^2 factor in the numerator. This n^2 factor arises because the equivalent current sheet approximates n parallel conductors, each carrying an equal current. Note that the equivalent current sheet representation is exact only when the edge-to-edge spacing between the conductors, s, is zero and the conductor thickness is negligible. In the next subsection, we will compare the accuracy of this approximate expression to the more accurate summation method discussed in subsection 3.6.1.

3.7.1 Comparison to Summation Method

In order to compare the approximate expression to the more accurate summation method, we first generate systems of conductors that span a wide design space. We impose the following constraints on the design space:

- $0.1 < \rho < 0.9$
- $0.01l < s < 0.8\rho l$
- $(w+s)_{\min} = \max[0.01l, (0.04\rho l + s)]$
- $n_{\max} = \frac{\text{floor}(\rho l + s)}{(w+s)_{\min}}$
- $1 < n < n_{\max}$
- $0.02l < t < 0.01l$

Since the approximate expressions as well as the summation method expressions scale with conductor length, the constraints are defined in units normalized to the length. We begin an evaluation of these expressions by first generating over $30,000$ distinct conductor systems that span the design space defined by these constraints.

Of the $30,000$ systems, we choose ones consistent with the overall goal of using our results for the evaluation of the inductance of spirals. This is done by limiting the maximum permissible s/w ratio. We consider only systems with s/w ratios less than 3. Although most on-chip inductors use s/w ratios less than 1, we choose 3 as the maximum to accommodate inductor geometries used in interleaved transformers (see chapter 5). Approximately $27,000$ systems have s/w less than 3, of which $\approx 20,000$ have s/w less than 1. In the remainder of this chapter, we will consider the accuracy of the approximate expressions over both these sets.

We compute the total inductance for each of these systems using both the computationally intensive summation method and our equivalent current sheet expression. Figure 3.13 summarizes the results of these simulations. We plot the percentage error of the approximate expression (when compared to the summation method) vs the s/w ratio. We can see that the errors worsen as s/w increases. However, even

the worst case errors are within -13% and $+5\%$. Note that for $s/w < 1$, the worst case errors are within 5%. As expected, the worst errors are obtained when $n = 2$

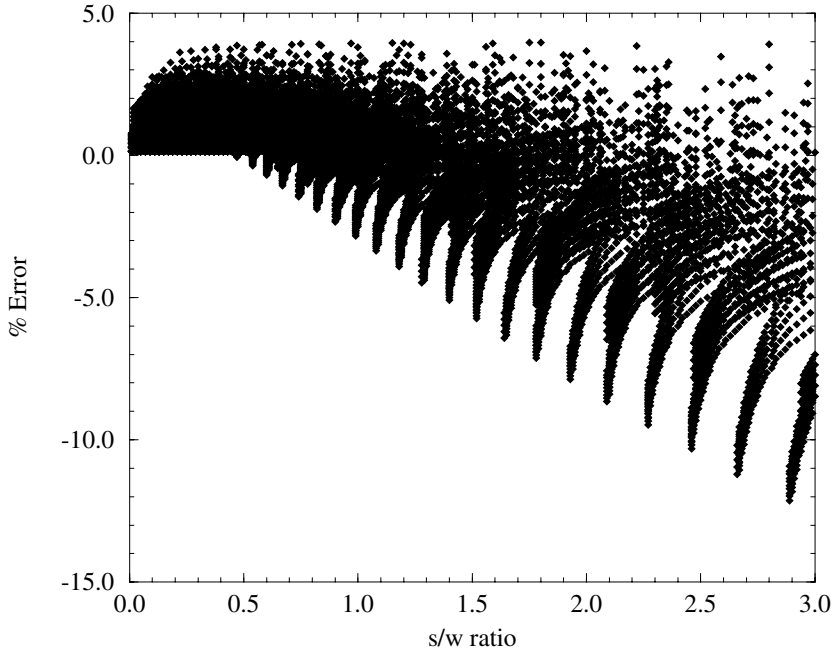


Figure 3.13: Error distribution for the current sheet approximation versus $\frac{s}{w}$ ratio.

for large values of s/w. Such a geometry exhibits a lot of free space between the conductors. Thus, a (continuous) current sheet approximation is poor.

Another source of error for conductors with small widths is the nonzero conductor thickness. This becomes more significant as t/w becomes larger. In practice, this ratio rarely exceeds 1 and in most cases is less than 0.02. Thus, nonzero conductor thickness is not as significant as nonzero spacing.

In the next subsections, we will explore how correction terms may be included in the current sheet approximation to account for nonzero spacing and finite conductor thickness. We will see that the corrected current sheet expression exhibits substantially improved accuracy.

3.7.2 Correction for Nonzero Spacing

A thorough examination of the terms involving the spacing shows three correction terms. In order of importance, these terms are corrections to the GMD, AMD and AMSD of the equivalent current sheet.

The GMD correction term is obtained by comparing the current sheet expression's $n^2 * \ln(nw + (n-1)s)$ term to the corresponding terms obtained in the summation method (i.e. the addition of the self inductance terms $(n * \ln w)$ and the mutual inductance terms $((n^2 - n) * \ln(w + s))$. A series expansion with terms normalized to $(nw + (n-1)s)$ indicates that the first order terms cancel, leaving a second order term that is dominant:

$$L_{\text{scor,GMD}} \approx \frac{\mu n^2 l}{2\pi} \left[\frac{0.5(n-1)s^2}{(nw + (n-1)s)^2} \right] \tag{3.49}$$

This term is most important when $n = 2$ and when s/w is large.

The AMD correction term comes from a comparison of the the AMD components of the current sheet expression and those of the summation method. This comparison is straightforward and yields:

$$L_{\text{scor,AMD}} \approx \frac{\mu n^2 l}{2\pi} \left[\frac{(n-1)s}{3nl} \right] \tag{3.50}$$

Like the GMD correction term, this term is most important when $n = 2$ and when s/w is large.

The corresponding AMSD correction term is insignificant compared to the GMD and AMD correction terms. For completeness, we include it here:

$$L_{\text{scor,AMSD}} \approx -\frac{\mu n^2 l}{2\pi} \left[\frac{(n-1)s(s+w)}{12l^2} \right] \tag{3.51}$$

3.7.3 Correction for Nonzero Conductor Thickness

A careful examination of the terms involving the thickness shows that the GMD correction term dominates the rest. This correction term is easily obtained by noting

that the current sheet expression approximates the natural logarithm terms of the self inductances of the n conductors as $n\ln(w)$ instead of $n\ln(w+t)$. The introduction of this correction term substantially reduces the error attributable to finite conductor thickness:

$$L_{\text{tcor,GMD}} \approx -\frac{\mu n l}{2\pi}\left[\ln\left(\frac{w+t}{w}\right)\right]. \tag{3.52}$$

This term becomes important only when the conductor thickness is comparable to the width. In modern semiconductor processes, the metal thickness rarely exceeds $3\mu m$, implying that this term will only be important for inductors with conductor widths less than $\approx 5\mu m$, a rare case in monolithic inductor design. Also, the effect of conductor thickness becomes less important as the number of turns increases. This is because the thickness has a significant impact only on the self inductance, and as n increases, the mutual inductance terms go up as $n^2 - n$, whereas the self inductance terms go up only as n.

3.7.4 Corrected Current Sheet Expressions

We combine the correction terms (from equations 3.49, 3.50, and 3.52) with the original current sheet equation(3.48) to arrive at our final corrected expression:

$$\begin{aligned} L_{\text{nrect,cor}} =& \frac{\mu n^2 l}{2\pi}\left[\ln\left(\frac{2}{\rho}\right) + 0.5 + \frac{\rho}{3} - \frac{\rho^2}{24}\right] \\ &+ \frac{\mu n^2 l}{2\pi}\left[\frac{0.5(n-1)s^2}{(\rho l)^2} + \frac{(n-1)s}{3nl} - \frac{1}{n}\ln\left(\frac{w+t}{w}\right)\right] \end{aligned} \tag{3.53}$$

We now compare the corrected and original current sheet expressions with the more exact summation method over the two design spaces defined in subsection 3.7.1. The results are summarized in Table 3.1 and Table 3.2 for maximum s/w ratios of one and three respectively. For comparison, we have also included the inductance computed by summing the self inductances and mutual inductances according to the Greenhouse expressions. As one expects, the Greenhouse method, with its full blown segmented summation approach, achieves the best accuracy. The worst case

error of the Greenhouse method is $\approx 2\%$ and is due mainly to its incorrect use of the GMD discussed earlier. For s/w ratios less than one, the simple current sheet expression, although not as good as the Greenhouse method, exhibits worst case errors less than 4%, indicating that it is good enough over this limited (but practical) design space. In fact, over this range, the simple current sheet expression has a smaller deviation than the corrected expression. This is not surprising as the correction terms introduced in the previous section are chosen to reduce the worst case percentage error and not the standard deviation. Thus, the corrected expression does exhibit a smaller worst case error than the simple expression. The utility of the corrected current sheet expression becomes obvious when one considers a broader design space (with s/w ratios up to three), where its worst case errors are less than 4% (compared to 12% for the simple current sheet expression). We also note that the worst case errors of the corrected expression and Greenhouse's method are comparable over this range, suggesting that the corrected expression is good enough for most purposes.

Computation Method	Min	Max	Mean	Median	StD
Greenhouse summation	-0.17	2.33	0.33	0.04	0.58
Current sheet approximation	-2.83	3.93	0.88	0.83	0.67
Current sheet with corrections	-0.05	3.47	0.78	0.73	0.82

Table 3.1: Error statistics (in %) for the total inductance of identical parallel conductors with rectangular cross section with max s/w ratio of 1 (19526 simulations)

Computation Method	Min	Max	Mean	Median	StD
Greenhouse summation	-0.17	2.33	0.24	0.02	0.52
Current sheet approximation	-12.14	3.96	0.08	0.64	2.05
Current sheet with corrections	-0.36	3.56	0.93	0.88	0.86

Table 3.2: Error statistics (in %) for the total inductance of identical parallel conductors with rectangular cross section with max s/w ratio of 3 (27001 simulations)

Figure 3.14 shows the error distributions of these expressions. The horizontal axis is the absolute percentage error of these expressions referenced to the summation method. The vertical axis shows the fraction of simulations (out of our family

of 27,001) with errors exceeding the specified level. We define the absolute percentage error of the approximation $\hat{L}$ of an inductance L as $100|\hat{L} - L|/L$. Roughly speaking, the closer the error distribution curve to the y-axis, the more accurate the expression. We can determine several important statistics from the curves. By following the horizontal line at the 50% level, we can read off the median error for each approximation. By following a vertical line at some level of error we can find the fraction of inductors for which the approximation was at least that accurate. The maximum error is given by the point where the curve hits the x-axis. Clearly, the maximum error of the corrected expression is much smaller than the maximum error of the current sheet approximation. However, we note that the current sheet approximation exhibits errors less than 2% for 80% of the inductors, indicating that even this simple expression may be good enough for most cases.

3.8 Approximation for One Side of a Square Spiral

Section 3.7 focused on identical parallel conductors with uniform spacing. While this case was convenient for highlighting our approach, it is not useful for evaluating the inductance of on-chip spirals. In this section, we will consider a system of parallel conductors of unequal, but systematically varying lengths that approximate one side of a square spiral. All conductors still have identical rectangular cross sections and are uniformly spaced. As before, we assume a uniform current distribution within each conductor.

The geometry is depicted in figure 3.15 along with the equivalent current sheet approximation. The parameters that define this geometry are the number of conductors, n, the average length, l, the width, w, the edge-to-edge spacing, s, and thickness, t. The corresponding current sheet expression is obtained using equation 3.31. Once again we introduce the variable $\rho = \frac{nw+(n-1)s}{l}$, which is now the

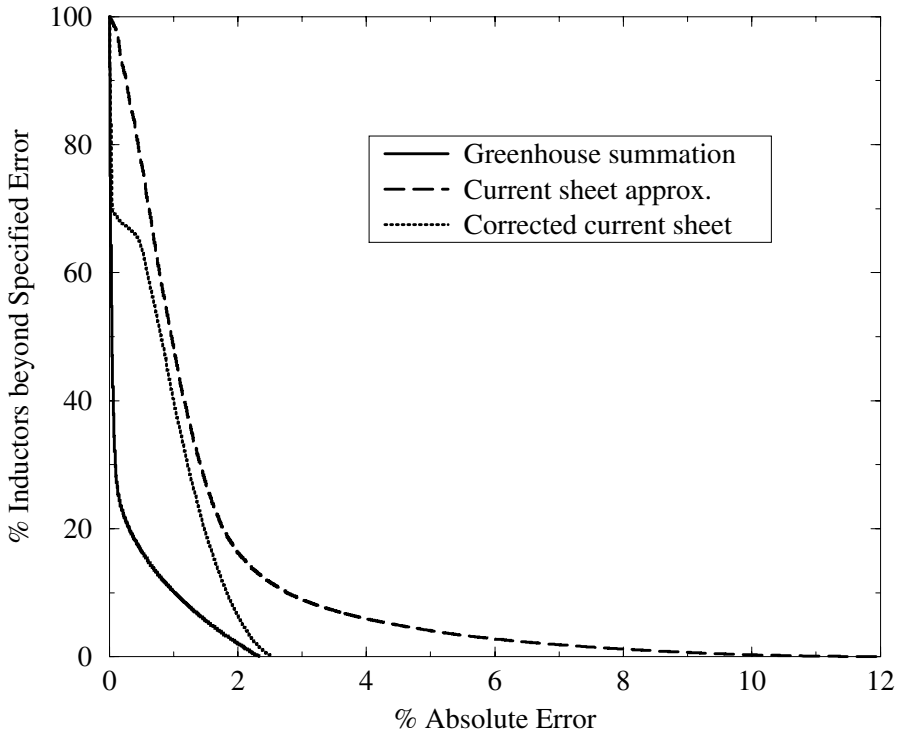


Figure 3.14: Error distribution for the current sheet approximation versus $\frac{s}{w}$ ratio.

ratio of the width of the current sheet to its average length. The simple current sheet approximation is:

$$\begin{aligned} L_{\text{ntrapsheet}} &\approx \frac{\mu n^2 l}{2\pi}\left[\ln\left(\frac{2}{\rho}\right) + 0.5 + \frac{\rho}{3}\left(\sqrt{2} - \ln(1+\sqrt{2})\right) + \frac{\rho^2}{24}\right] \\ &\approx \frac{\mu n^2 l}{2\pi}\left[\ln\left(\frac{2}{\rho}\right) + 0.5 + 0.178\rho + 0.0416\rho^2\right]. \end{aligned} \tag{3.54}$$

The correction terms are obtained by considering the effects of finite spacing and finite thickness on the GMD, AMD and AMSD terms. Once again, the GMD correction terms dominate the rest. The AMSD terms are not significant and may be

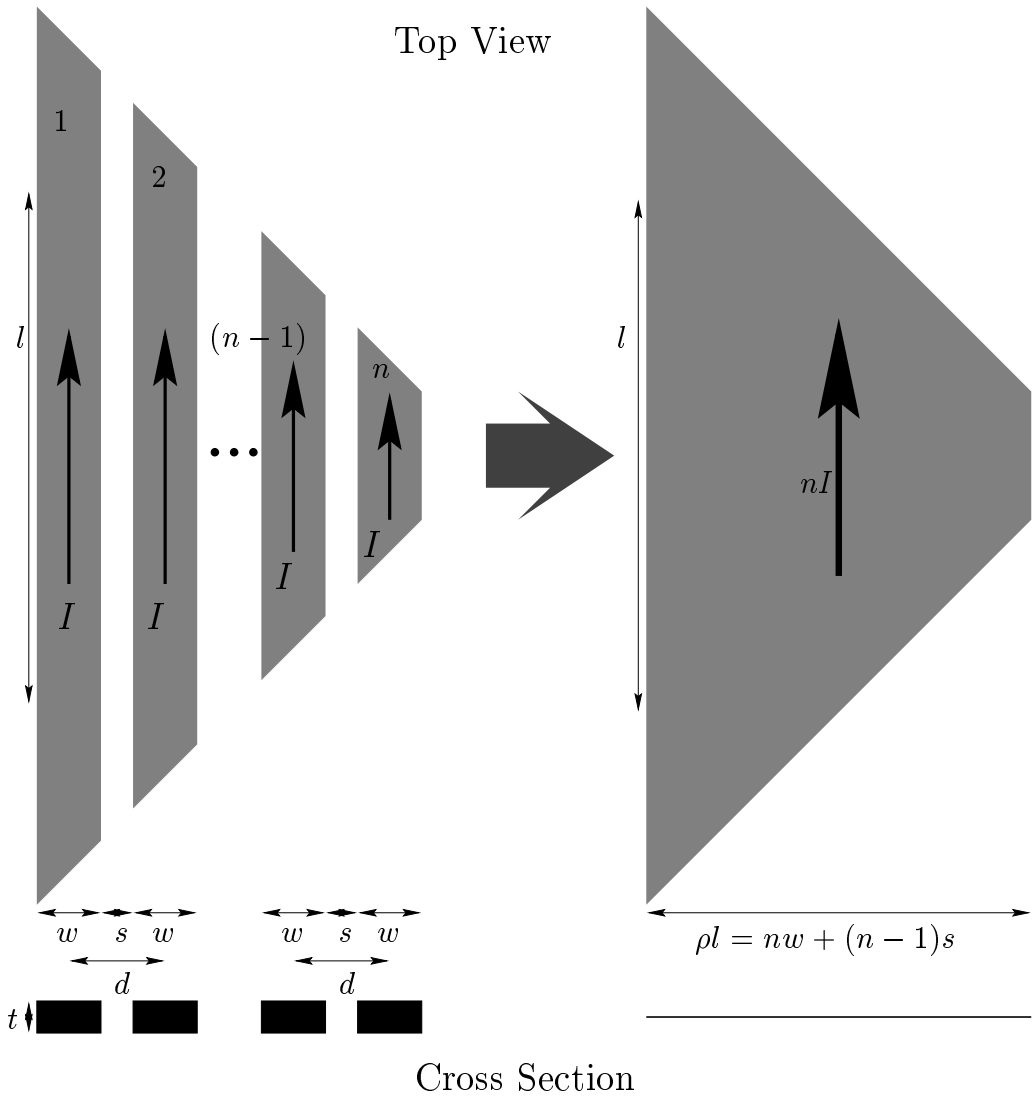


Figure 3.15: Rectangular conductors with trapezoidal variation in length and the equivalent current sheet representation

ignored. Among the AMD correction terms, only the one for finite spacing needs to be included. The complete expression including the significant correction terms is:

$$\begin{aligned} L_{\text{ntrap,cor}} =& \frac{\mu n^2 l}{2\pi}\left[\ln\left(\frac{2}{\rho}\right) + 0.5 + \frac{\rho}{3}\left(\sqrt{2} - \ln(1+\sqrt{2})\right) + \frac{\rho^2}{24}\right] \\ &+ \frac{\mu n^2 l}{2\pi}\left[0.5\frac{(n-1)s^2}{(\rho l)^2} + \frac{(n-1)s}{3nl}\left(\sqrt{2} - \ln(1+\sqrt{2})\right) - \frac{1}{n}\ln\left(\frac{w+t}{w}\right)\right] \\ L_{\text{ntrap,cor}} =& \frac{\mu n^2 l}{2\pi}\left[\ln\left(\frac{2}{\rho}\right) + 0.5 + 0.178\rho + 0.0416\rho^2\right] \\ &+ \frac{\mu n^2 l}{2\pi}\left[0.5\frac{(n-1)s^2}{(\rho l)^2} + 0.178\frac{(n-1)s}{n} - \frac{1}{n}\ln\left(\frac{w+t}{w}\right)\right]. \end{aligned} \tag{3.55}$$

The corrected and original current sheet expressions are compared with the more exact summation method over a design space identical to the one described in subsection 3.7.1. Thus, we perform $\approx 27,000$ simulations in which the s/w ratio varies from $0-3$. The results are summarized in Table 3.3 and Table 3.4 for maximum s/w ratios of 1 and 3 respectively. Once again, we have included the inductance calculated using the Greenhouse method for comparison. While the simple current sheet expression exhibits errors within 4% for s/w ratios less than one, its worst case error approaches -15% for s/w values close to 3. However, the corrected current sheet expression exhibits errors within 3% over this entire range. It is interesting to note that the Greenhouse method also exhibits errors as large as 7%. Such a large error is the result of the Greenhouse method not accounting for the tapered nature of trapezoidally shaped conductors. Consequently, a large discrepancy occurs while computing the self inductance of such conductors when their width becomes comparable to the length. In fact, the corrected current sheet expression's error exhibits a smaller standard deviation than that of the inductance computed using the Greenhouse method. These observations are confirmed by Figure 3.16.

Computation Method	Min	Max	Mean	Median	StD
Greenhouse summation	0.01	7.38	1.63	0.45	2.16
Current sheet approximation	-3.65	4.00	0.92	0.88	0.71
Current sheet with corrections	-0.03	1.95	0.67	0.68	0.66

Table 3.3: Error statistics (in %) for conductors with rectangular cross section and trapezoidally varying length with max s/w ratio of 1 ($\approx 20,000$ simulations)

Computation Method	Min	Max	Mean	Median	StD
Greenhouse summation	0.01	7.38	1.24	0.23	1.95
Current sheet approximation	-14.30	4.02	0.09	0.69	2.19
Current sheet with corrections	-2.25	1.95	0.68	0.70	0.67

Table 3.4: Error statistics (in %) for conductors with rectangular cross section and trapezoidally varying length with max s/w ratio of 3 (≈ 2700 simulations)

3.9 Approximation for a Square Spiral

We are now ready to examine a regular, symmetric geometry that approximates all four sides of a planar square spiral. Figure 3.17 illustrates the system under consideration. There are n parallel, concentric, four-sided conductors with identical rectangular cross section of width, w, and thickness, t. The average length of each side of the square shaped system is l. The conductors are separated by an edge-to-edge spacing s so that the total width of one side of the system is $nw+(n-1)s = \rho l$, where ρ is the ratio of the width of one side to the average conductor length. Thus, the system's outer diameter is $(1+\rho)l$ and the inner diameter is $(1-\rho)l$ where $\rho < 1$.

3.9.1 Summation Method

The total inductance of this system may be calculated using the summation method outlined in section 3.6,

$$L_T = \Sigma L_i + \Sigma M, \tag{3.56}$$

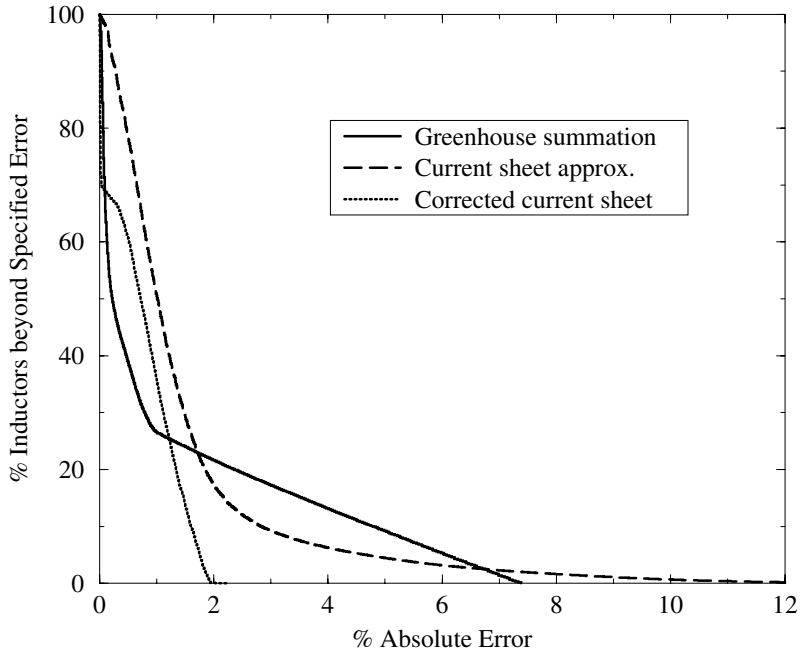


Figure 3.16: Comparison of error distribution of inductances evaluated for parallel inductors with trapezoidally varying length

where ΣL_i denotes the sum of self inductances of the segments and ΣM denotes the sum of all the mutual inductances. Each conductor contains 4 straight line segments. Thus our square system of n conductors has $4n$ segments, $2n$ of which are orthogonal to the other $2n$ segments. Of the $2n$ parallel segments, n have current flow in the opposite direction to the other n. Using symmetry and noting that segments perpendicular to one another have zero mutual inductance, we may write the total inductance as [15]:

$$L_{\mathrm{T}} = 4\left(\sum_{i=1}^{n} L_i + \sum_{i=1}^{n}\sum_{j=1,j\neq i}^{n} M_{+,ij} - \sum_{i=1}^{n}\sum_{j=n+1}^{2n} M_{-,ij}\right) \tag{3.57}$$

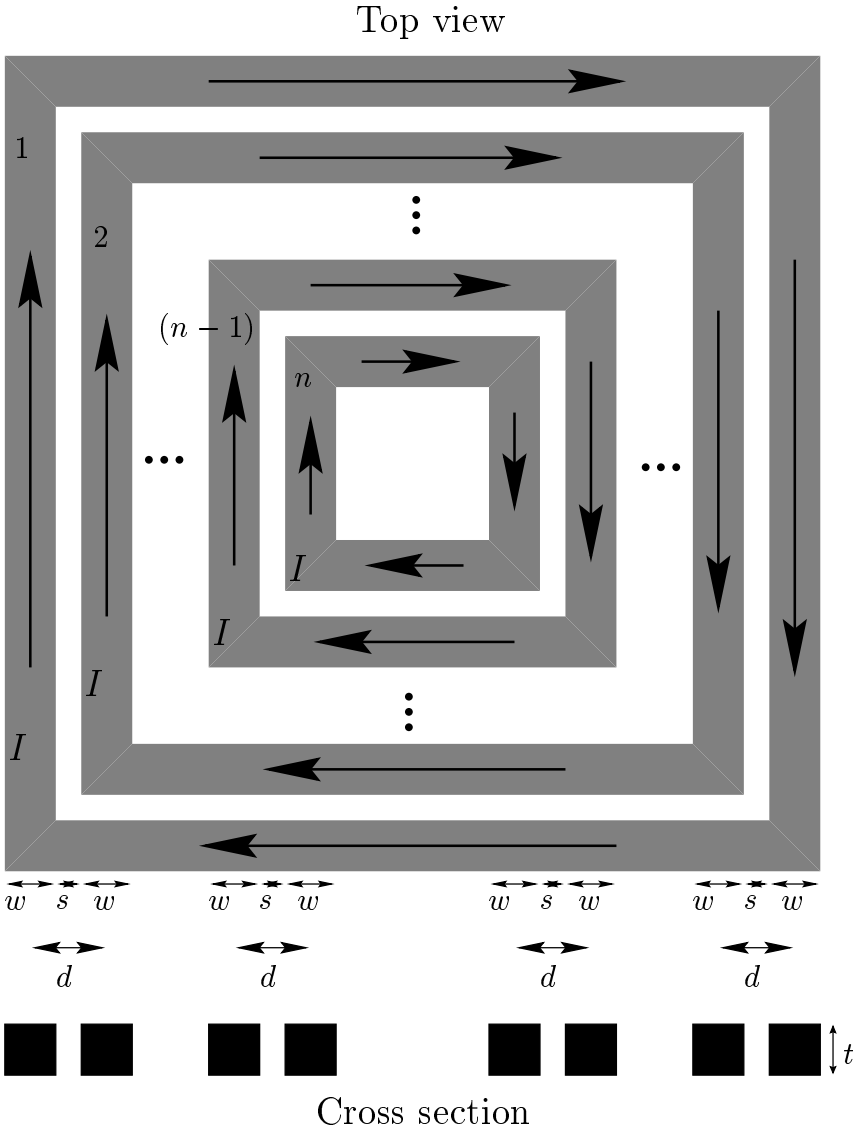


Figure 3.17: System of parallel, concentric, square conductors

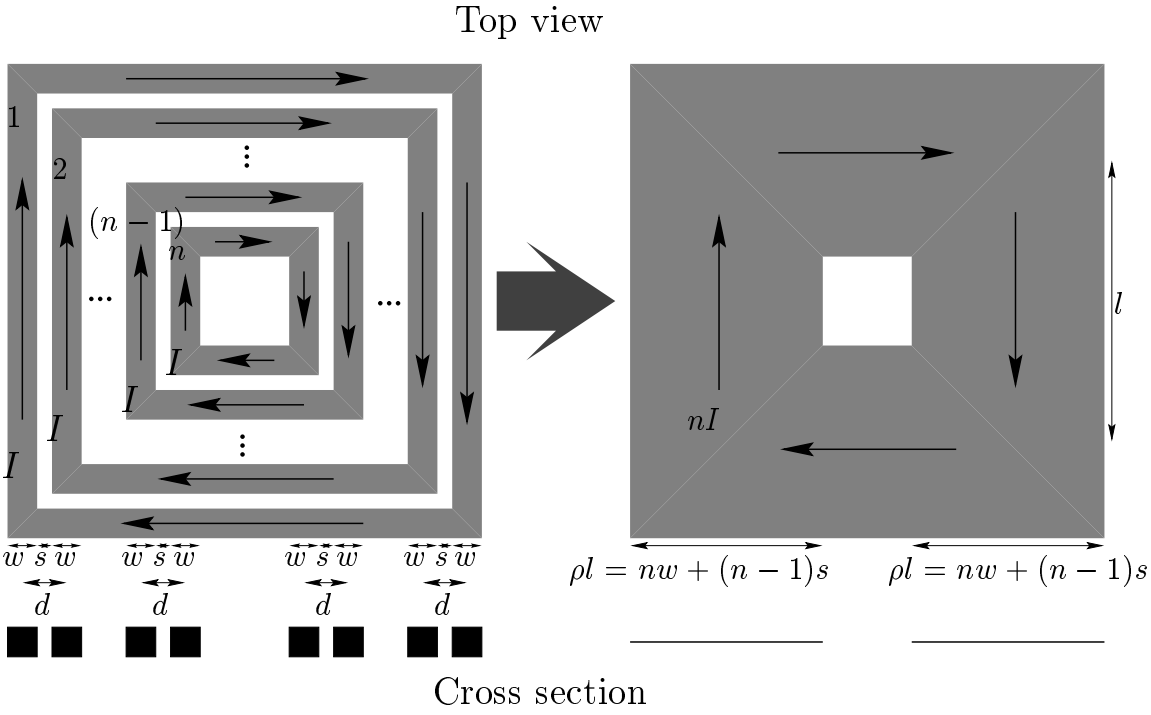


Figure 3.18: Square geometry and equivalent current sheet

where L_i denotes the self inductance terms, $M_{+,ij}$ denotes the positive mutual inductance terms and $M_{-,ij}$ denotes the negative mutual inductance terms. The self and mutual inductances may be calculated using the expressions that we derived in section 3.5, or by using the Greenhouse equations [15]. However, the complexity of the system has order n^2, making such an approach unacceptable for obtaining a simple, accurate inductance expression. Thus, we will pursue an approach similar to that outlined in sections 3.7 and 3.8 and explore how a current sheet approximation combined with the dominant correction terms can render an expression that exhibits very good accuracy.

3.9.2 Current Sheet Approximation of Concentric, Parallel Conductors with Four Sides

Once again we introduce the variable $\rho = \frac{nw+(n-1)s}{l}$, which is now the ratio of the width of the current sheet to the average length of one side of the current sheet. The simple current sheet approximation is obtained from equation 3.34:

$$L_{\text{nsqsheet}} = \frac{2\mu n^2 l}{\pi}\left[\ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2\right]. \tag{3.58}$$

The correction terms are obtained by considering the effect on finite spacing and finite thickness on the GMD, AMD and AMSD terms. Once again, the GMD correction terms dominate. Among the AMD correction terms, only the one associated with finite spacing is significant. The AMSD terms associated with the positive mutual inductance terms may be ignored, although the correction terms involving the negative mutual inductance terms must be included. The complete expression including the significant correction terms is:

$$\begin{aligned} L_{\text{nsq,cor}} =& \frac{2\mu n^2 l}{\pi}\left[\ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2 + 0.5\frac{(n-1)s^2}{(\rho l)^2}\right] \\ &+ \frac{2\mu n^2 l}{\pi}\left[0.178\frac{(n-1)s}{nl} + 0.0833\frac{(n-1)s(s+w)}{l^2} - \frac{1}{n}\ln\left(\frac{w+t}{w}\right)\right]. \end{aligned} \tag{3.59}$$

The corrected and original current sheet expressions are compared with the more exact summation method over a design space identical to the one used in the previous sections. The results are summarized in Table 3.5 and Table 3.6 for maximum s/w ratios of 1 and 3 respectively. Once again, we have included the inductance calculated using the Greenhouse method for comparison. While the simple current sheet expression exhibits errors as large as -7% for s/w ratios less than 1, the corrected current sheet expression exhibits errors only within 3% for s/w ratios up to 3. Note that the corrected current sheet expression's error exhibits a smaller standard deviation (but a somewhat larger mean error) than that computed using the Greenhouse

method. Figure 3.19 compares the absolute error of the three expressions. Table 3.5 Table 3.6 Figure 3.19

Computation Method	Min	Max	Mean	Median	StD
Greenhouse summation	-1.81	2.76	0.76	0.17	1.06
Current sheet approximation	-7.59	4.63	0.95	0.99	1.10
Current sheet with corrections	-0.04	2.50	0.81	0.78	0.81

Table 3.5: Error statistics (in %) for conductors with rectangular cross section making a square inductor with max s/w ratio of 1 ($\approx 20,000$ simulations)

Computation Method	Min	Max	Mean	Median	StD
Greenhouse summation	-1.81	2.76	0.58	0.11	0.95
Current sheet approximation	-22.36	4.65	-0.29	0.74	3.32
Current sheet with corrections	-3.44	2.50	0.80	0.82	0.85

Table 3.6: Error statistics (in %) for conductors with rectangular cross section making a square inductor with max s/w ratio of 3 ($\approx 27,000$ simulations)

3.10 Circular Geometries

In this section, we will look at the self and mutual inductances of some circular geometries. Although not often used in practice, the results of circular geometries are useful for bounding the inductances of polygonal spirals possessing a large number of sides. Such bounds are of particular interest for on-chip spiral inductors, where hexagonal, octagonal and other polygonal spirals are candidates for replacing square spirals. In the previous sections, we have provided a comprehensive treatment of straight, trapezoidal and square geometries. Now, we will provide a similar treatment for circular geometries. We will see that these two extremes yield inductance expressions that are similar in form. In many cases, the terms have the same flavor and retain the same order of importance.

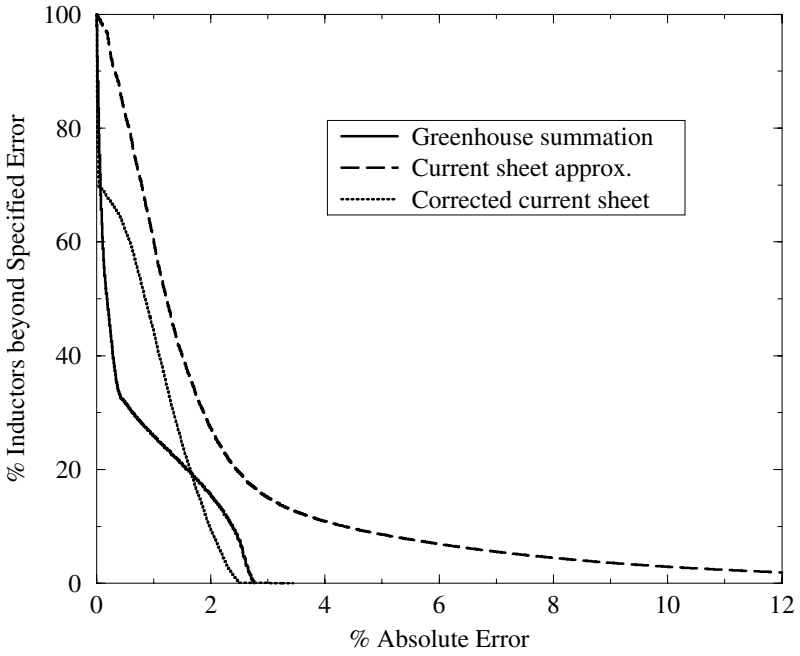


Figure 3.19: Comparison of error distribution of inductances evaluated for a four-sided square sheet

3.10.1 Concentric Circular Filaments

First, we consider the mutual inductance between two concentric circular filaments of radii r_1 and r_1 as illustrated in figure 3.20. An approach similar to the one adopted for straight parallel lines yields an expression that involves elliptic integrals. We use the average diameter, $d = (r_1 + r_2)$, and the ratio of the separation to the average diameter, $\rho = \frac{(r_1 - r_2)}{d}$, as the two variables to obtain the following exact expression: (see appendix B for details):

$$M_{\text{circfil}} = \frac{\mu d}{2} \left[(2 - m)K(m) - 2E(m) \right]. \tag{3.60}$$

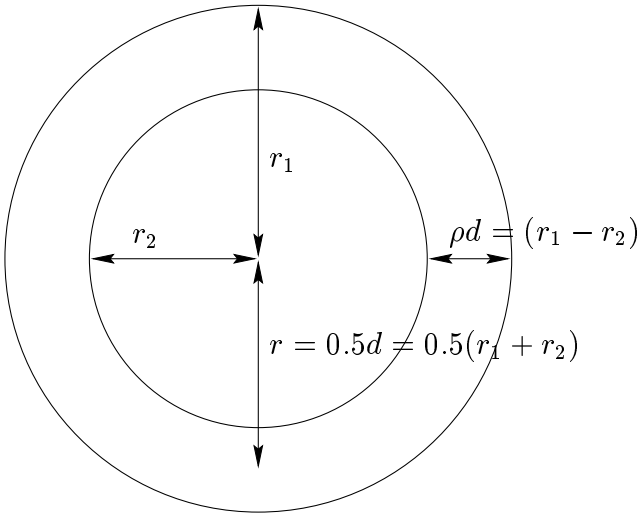


Figure 3.20: Mutual inductance between concentric planar circular filaments

In this equation, $K(m)$ is the complete elliptic integral of the first kind and $E(m)$ is the complete elliptic integral of the second kind, with argument $m = (1 - \rho^2)$. A simpler expression may be obtained via series expansion in terms of ρ. This approach yields an expression that resembles the approximate expression obtained for the mutual inductance between two straight, parallel lines:

$$M_{\text{circfil}} \approx \frac{\mu d}{2}\left[\ln\left(\frac{1}{\rho}\right) - 0.6 + 0.7\rho^2\right]. \tag{3.61}$$

This expression is accurate to within 5% for $\rho < 0.6$ and is good enough for most practical cases.

3.10.2 Self Inductance of a Circular Sheet

Figure 3.21 shows a circular current sheet of average diameter, d, and width, w. The self inductance of this sheet may be obtained by using equation 3.61 and then taking the mean value of the terms. Once again, the GMD and AMSD concepts are used

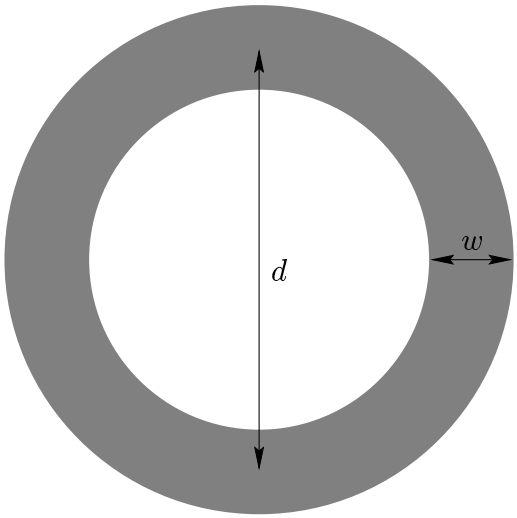


Figure 3.21: Circular current sheet

(note that the AMD is not needed because the series expansion does not contain a term linear in ρ). The result is (see appendix B for details): :

$$L_{\text{circsheet}} \approx \frac{\mu d}{2}\left[\ln\left(\frac{d}{w}\right) + 0.9 + 0.2\frac{w^2}{d^2}\right]. \tag{3.62}$$

3.10.3 Mutual Inductance between Two Concentric Circular Current Sheets

Figure B.3 shows two circular concentric current sheets of average diameters d_1 and d_2. The sheets have equal width, w, and are separated by a center to center distance, ρd, where d is the mean of the two average diameters ($d = 0.5(d_1 + d_2)$). Note that $\rho d = w + s$. The mutual inductance between the sheets is given by (see appendix B for details):

$$M_{\text{circ2sheets}} = \frac{\mu d}{2}\left[(2-m)K(m) - 2E(m) + \left(0.2 + \frac{1}{12\rho^2}\right)\frac{w^2}{d^2}\right], \tag{3.63}$$

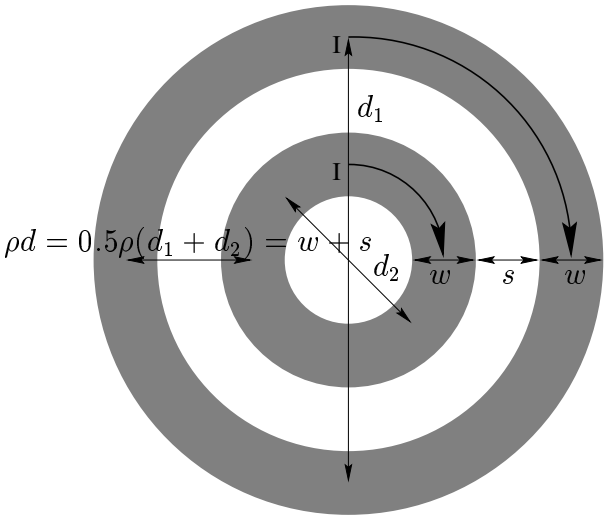


Figure 3.22: Mutual inductance between circular filaments

where the argument for the complete elliptic integrals is again given by $m = (1-\rho^2)$. An approximate series expansion of this expression, using techniques similar to the ones used in straight and square geometries, yields:

$$M_{\text{circ2sheets}} \approx \frac{\mu d}{2}\left[\ln\left(\frac{1}{\rho}\right) - 0.6 + 0.7\rho^2 + \left(0.2 + \frac{1}{12\rho^2}\right)\frac{w^2}{d^2}\right]. \tag{3.64}$$

3.10.4 Parallel Concentric Circular Conductors

Figure 3.23 shows n circular concentric conductors each of width, w, and thickness, t. The edge-to-edge spacing is s. The equivalent current sheet approximation is also shown in the figure. This equivalent current sheet has the same average diameter, d, as the system of n conductors. The width of the current sheet is $\rho d = nw + (n-1)s$. The current sheet expression for the system is simply the self inductance of the equivalent current sheet:

$$L_{\text{ncircsheet}} \approx \frac{\mu n^2 d}{2}\left[\ln\left(\frac{d}{w}\right) + 0.9 + 0.2\frac{w^2}{d^2}\right]. \tag{3.65}$$

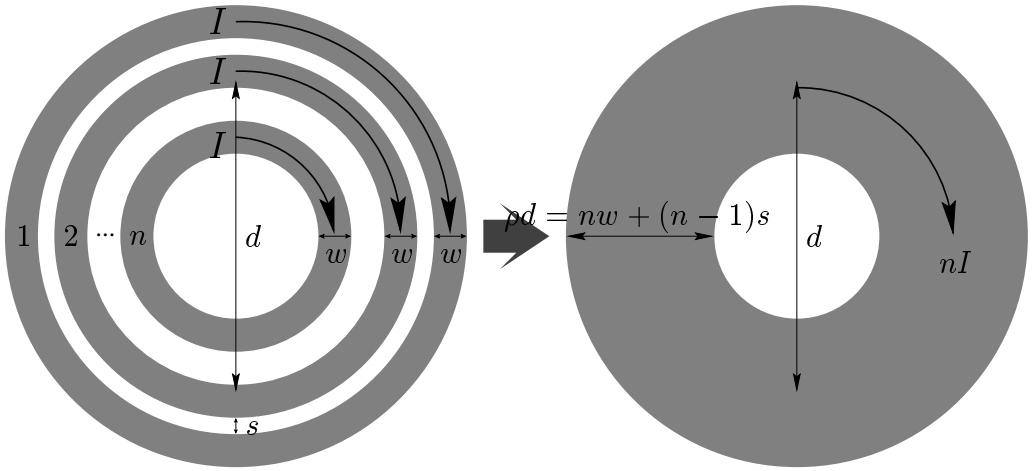


Figure 3.23: Concentric circular conductors with rectangular cross sections

A more accurate expression may be obtained by considering the finite spacing between the conductors as well as the thickness of the conductors. Just as in the case of the straight, parallel conductors, the dominant correction terms are the GMD ones. No AMD correction term is needed as there is no AMD term in the approximate expression. Among the AMSD correction terms, only the one for finite spacing is significant. The corrected expression is:

$$\begin{aligned} L_{\text{ncirc,cor}} \approx & \frac{\mu n^2 d}{2}\left[\ln\left(\frac{d}{w}\right) + 0.9 + 0.2\frac{w^2}{d^2}\right] \\ & + \frac{\mu n^2 d}{2}\left[\frac{0.5(n-1)s^2}{(\rho d)^2} + \frac{0.4(n-1)s(w+s)}{d^2} - \frac{1}{n}\ln\left(\frac{w+t}{w}\right)\right] \end{aligned} \tag{3.66}$$

Table 3.7 and Table 3.8 summarize the accuracy of these expressions for s/w ratios up to 1 and 3 respectively. While the simple current sheet approximation is good enough for s/w ratios up to 1, the corrected current sheet expression is more appropriate for a larger design space. The corrected expression exhibits errors within 3% for s/w ratios up to 3. Figure 3.24 compares the absolute errors of the two expressions.

Computation Method	Min	Max	Mean	Median	StD
Current sheet approximation	-7.94	3.78	0.08	0.37	1.28
Current sheet with corrections	-3.35	2.00	-0.06	- 0.00	0.75

Table 3.7: Error statistics (in %) for circular concentric conductors with rectangular cross section with max s/w ratio of 1 ($\approx 20,000$ simulations)

Computation Method	Min	Max	Mean	Median	StD
Current sheet approximation	-21.90	3.94	-0.92	0.11	3.04
Current sheet with corrections	-3.35	2.08	0.13	-0.00	0.82

Table 3.8: Error statistics (in %) for circular concentric conductors with rectangular cross section with max s/w ratio of 3 ($27,000$ simulations)

3.11 Summary

In this chapter, we have shown how a current sheet based approach can provide simple, accurate expressions for the self and mutual inductances of a variety of geometries. These approximate expressions have been compared to those obtained from more exact (but more complicated) summation methods. The errors of the approximate expressions are within $\approx 4\%$ for s/w ratios less than 1. We have shown how the inclusion of some correction terms can enhance the accuracy of these expressions over a wide design space, yielding errors within $\approx 4\%$ of the more accurate summation method for s/w ratios as large as 3.

As emphasized in chapter 2, the expressions that we derived here are intended for exploring trade-offs, obtaining design insight and optimizing circuits with on-chip inductors. In chapter 4, we will see how the approach developed in this chapter can be easily extended to obtain simple accurate expressions for square, hexagonal and octagonal spiral inductors.

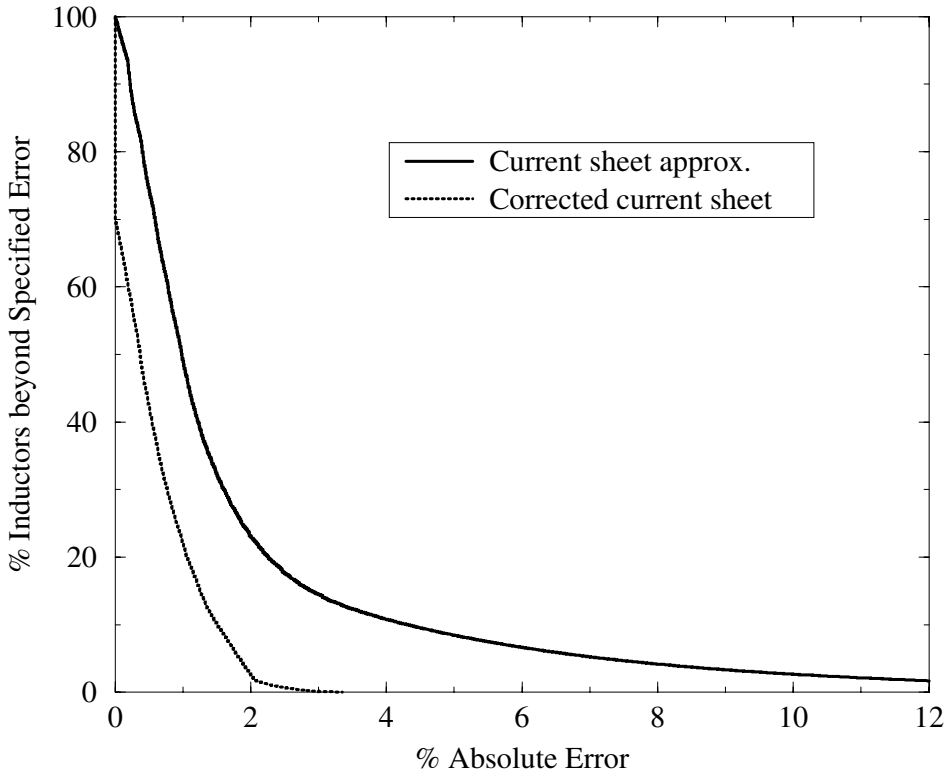


Figure 3.24: Comparison of error distribution of expressions for the total inductance of concentric circular conductors with rectangular cross sections

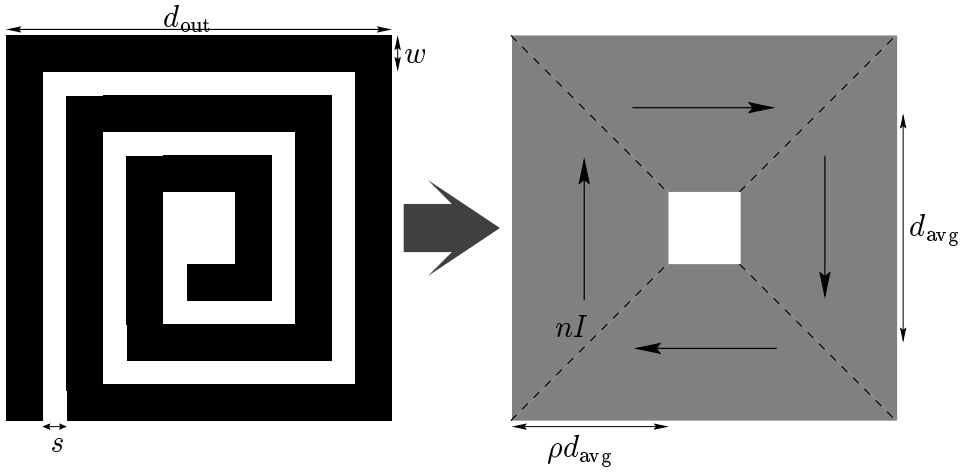
Chapter 4

Simple Accurate Expressions for the Inductance of Planar Spirals

IN this chapter, we describe three new simple expressions for the inductance of square, hexagonal, octagonal and circular planar inductors. The first expression is obtained from the current sheet approach described in chapter 3; the second is a *monomial* expression derived from fitting to a large database of inductors generated by a field solver; and the third is based on a modification of an expression developed by Wheeler [26]. These expressions are presented in section 4.1. The accuracy of these new expressions (as well as the previously published expressions reported in chapter 2) are compared to field solver simulations over a wide design space (spanning more than 19,000 inductors) in section 4.2 and then compared to measurement results in section 4.3. All three expressions are accurate, with typical errors of 2–3%, about an order of magnitude better than the previously published expressions, which have typical errors around 20% (or more). Furthermore, these new expressions are simple and are therefore excellent candidates for use in design and optimization.

4.1 Simple, Accurate Expressions

This section presents several accurate expressions for the inductance of square, hexagonal, octagonal and circular spirals.



4.1.1 Expressions Based on Current Sheet Approximations

Simple and accurate expressions for the inductance of a planar spirals can be obtained by approximating the sides of the spirals by symmetrical current sheets of equivalent current densities. For example, as illustrated in figure 4.1.1, in the case of the square, we obtain four identical current sheets: the current sheets on opposite sides are parallel to one another, whereas the adjacent ones are orthogonal. Using symmetry and the fact that sheets with orthogonal current sheets have zero mutual inductance, the computation of the inductance is now reduced to evaluating the self inductance of one sheet and the mutual inductance between opposite current sheets. These self and mutual inductances are evaluated using the concepts of GMD, AMD and AMSD. The resulting expression is:

$$L_{\text{cursh}} = \frac{\mu n^2 d_{\text{avg}} c_1}{2} \left[\ln(c_2/\rho) + c_3 \rho + c_4 \rho^2 \right], \tag{4.1}$$

where the coefficients c_i are layout dependent and are shown in Table 4.1. The derivations of the expressions for a square and circular spiral were discussed in detail in the previous chapter. The expressions for the hexagonal and octagonal spirals (and for that matter a polygonal spiral with an arbitrary number of sides) are also obtained using the same concepts, but require more work. In general, an N sided

Layout	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Table 4.1: Coefficients for current sheet expression.

polygonal spiral can be approximated by an N sided regular polygonal current sheet. The calculation of the inductance of this regular polygonal current sheet involves the calculation of $\frac{N}{2}$ distinct terms. Thus, as N becomes large, the computation of the coefficients c_i becomes increasingly tedious, albeit significantly less complex than calculating the inductance of a spiral using a segmented summation method (such as the one proposed by Greenhouse).

For sufficiently large values N, the polygonal current sheet is well approximated by a circular sheet, significantly simplifying the inductance calculation. For practical spiral geometries, the circular sheet approximation is within 3% of the polygonal current sheet approximation for $N > 12$. In fact, most of the coefficients tabulated in 4.1 can be well approximated by those obtained from corrections to an equivalent circular current sheet. For example, c_1 is roughly the ratio of the area of a polygon to that of a circle for a fixed diameter so that:

$$c_1 \approx \frac{N}{\pi} \tan\left(\frac{\pi}{N}\right). \tag{4.2}$$

It can be easily verified that c_1 approaches unity as N becomes large. Similarly, the GMD and ASMD coefficients c_2 and c_4 also exhibit monotonic transitions from the square to the circular current sheet. One would expect a similar transition for the AMD coefficent c_3. However, the magnitude of c_3 decays rapidly as a function of N and is significant only for the square case. The reason for this rapid decay can be attributed to the fact that the AMD term only appears in the self inductance calculation of one side of a spiral: as N increases (while keeping the average diameter d_{avg} fixed), not only does the length of a side decrease, but also the relative weight of self inductance terms goes down as $\frac{1}{N}$.

4.1.2 Data Fitted Monomial Expression

Our second expression is based on a data fitting technique, and has the form:

$$L_{\text{mon}} = \beta d_{\text{out}}^{\alpha_1} w^{\alpha_2} d_{\text{avg}}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{4.3}$$

where the coefficients β and α_i are layout dependent, and given in Table 4.2. The

Layout	β	α_1 (d_{out})	α_2 (w)	α_3 (d_{avg})	α_4 (n)	α_5 (s)
Square	$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	$1.28 \cdot 10^{-3}$	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	$1.33 \cdot 10^{-3}$	-1.21	-0.163	2.43	1.75	-0.049

Table 4.2: Coefficients for data-fitted monomial expression.

expression in (4.3) is called a *monomial* in the variables d_{out}, w, d_{avg}, n, and s. The coefficients are obtained as follows. We first change variables to use the logarithms of the variables:

$$x_1 = \log d_{\text{out}}, \quad x_2 = \log w, \quad x_3 = \log d_{\text{avg}}, \quad x_4 = \log n, \quad x_5 = \log s.$$

Taking the logarithm of the inductance as well we can express the monomial relation (4.3) as

$$y = \log L = \alpha_0 + \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4 + \alpha_5 x_5$$

where $\alpha_0 = \log \beta$. This is a linear-plus-constant model of y as as function of x, and is easily fit by various regression or data-fitting techniques. To develop our models we use a simple least-squares fit: we chose α_i to minimize

$$\sum_{k=1}^{N} \left(y^{(k)} - \alpha_0 - \alpha_1 x_1^{(k)} - \alpha_2 x_2^{(k)} - \alpha_3 x_3^{(k)} - \alpha_4 x_4^{(k)} - \alpha_5 x_5^{(k)} \right)^2,$$

where the sum is over our family of inductors (so $N \approx 19,000$). It is also possible to use more sophisticated data-fitting techniques, *e.g.*, one which minimizes the maximum error of the fit, or one in which the coefficients must satisfy given inequalities or bounds.

For all three cases tabulated in table 4.2, the exponents of the variables with the dimension of length (d_{out}, w, d_{avg} and s) sum to unity, which is consistent with the expectation that the inductance scales linearly with the size of a spiral.

Since the monomial expression L_{mon} is developed from our library of inductors, it is important to check that it has predictive ability as well, by checking its error on inductors not in the library. Such tests reveal that the fit for such inductors is as good as the fit for the ones in the family from which the model was developed. This is hardly surprising since the fitting method compresses $19,000$ numbers (*i.e.*, the inductances) to 6 (*i.e.*, the monomial coefficients), and so is not prone to 'overfitting'.

The monomial expression is useful since, like the other expressions, it is very accurate and very simple. Its real use, however, is that it can be used for optimal design of inductors and circuits containing inductors, using *geometric programming*, which is a type of optimization method that uses monomial models [27, 28, 29].

4.1.3 Modified Wheeler formula

H. Wheeler [26] presented several formulas for planar spiral inductors, which were intended for discrete inductors. We have found that a simple modification of the original Wheeler formula allows us to obtain an expression that is valid for planar spiral integrated inductors:

$$L_{\text{mw}} = K_1 \mu_0 \frac{n^2 d_{\text{avg}}}{1 + K_2 \rho} \tag{4.4}$$

where ρ is the fill ratio defined previously. The coefficients K_1 and K_2 are layout dependent and are shown in Table 4.3. The ratio ρ represents how hollow the inductor is: for small ρ we have a hollow inductor ($d_{\text{out}} \approx d_{\text{in}}$) and for a large ρ we

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Table 4.3: Coefficients for modified Wheeler expression.

have a full inductor ($d_{\text{out}} \gg d_{\text{in}}$). Two inductors with the same average diameter but different fill ratios will, of course, have different inductance values: The full one has a smaller inductance because its inner turns are closer to the center of the spiral, and so contribute less positive mutual inductance and more negative mutual inductance.

4.2 Comparison to field solvers

In this section we analyze the error distributions of previously published expressions as well as our expressions by comparing them to the inductance computed using the field solver *ASITIC*.

Figure 4.1 shows the absolute error distributions of previously published expressions for square inductors presented in chapter 2. Figure 4.2 shows the absolute error distributions of our expressions for the same set of square inductors. The comparison is carried out for $\approx 19,000$ inductors spanning a wide design space. Table 4.4 summarizes the extent of the design space.

While the previously published expressions do predict the correct order of magnitude of the inductance, typical errors are 20% or more, which is unacceptable for circuit design and optimization. On the other hand all of the new expressions exhibit substantially better accuracies, with typical errors of $\approx 2-3\%$.

Table 4.5 summarizes the error statistics of our expressions for this design space. The current sheet expression exhibits the best performance with worst case errors less than 9%. The monomial expression exhibits a worst case error of 12% whereas the modified Wheeler expression has errors as large as 22% for a few inductors. The mean errors of all the expressions are less than 1% and the standard deviations are $\approx 2-3\%$ indicating that all three expressions give good accuracy for most inductors.

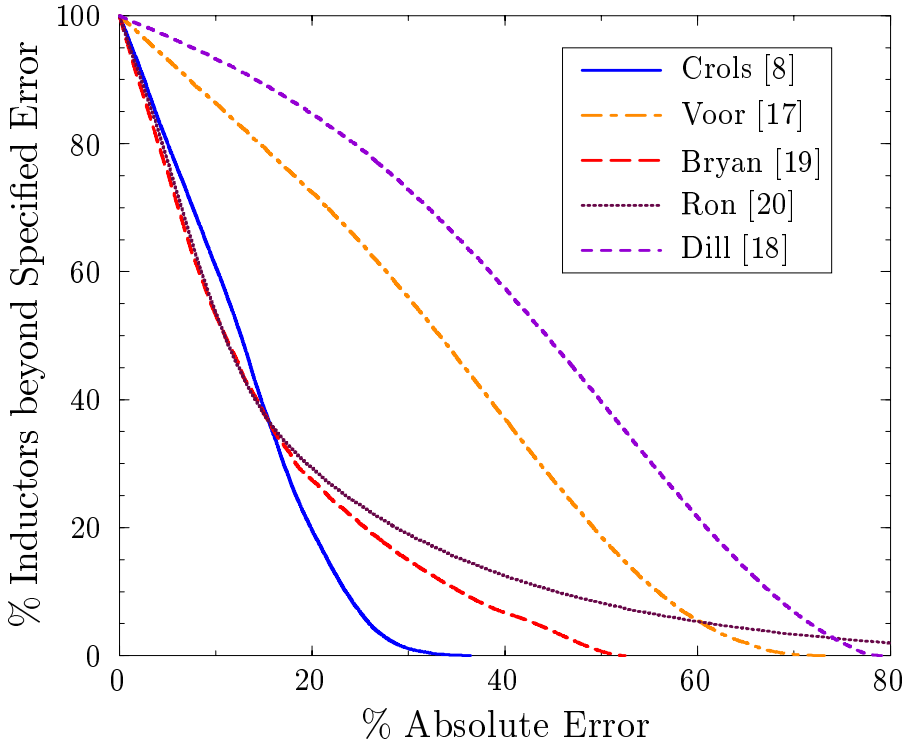


Figure 4.1: Error distribution for previously published expressions for square inductors, compared to field solver simulations.

	Min	Max
L(nH)	0.1	71
OD(μm)	100	400
n	1	20
s/w	0.02	3
ρ	0.03	0.95

Table 4.4: Design space used for simulating square inductors

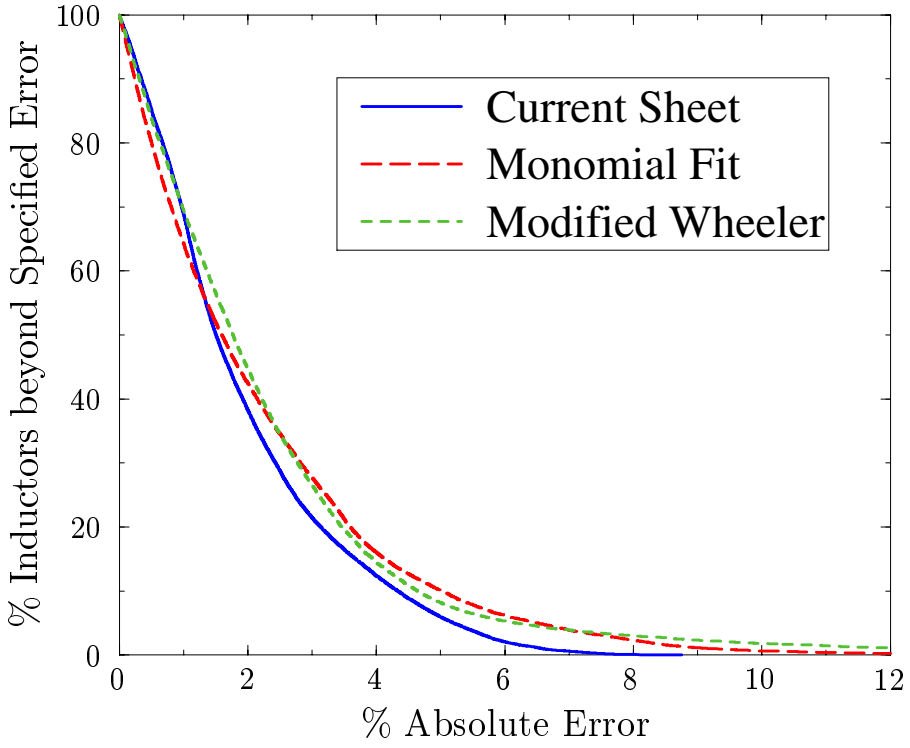


Figure 4.2: Error distribution for the new expressions for square inductors, compared to field solver simulations (Note change of x-axis scale relative to figure 4.1).

Computation Method	Min	Max	Mean	Median	StD
Current sheet	-8.75	5.84	-0.85	-0.47	2.35
Monomial fit	-12.46	14.34	-0.16	-0.01	3.04
Modified wheeler	-22.90	7.21	-0.33	0.14	3.25

Table 4.5: Error statistics (in %) of expressions for square inductors ($\approx 19,000$ simulations)

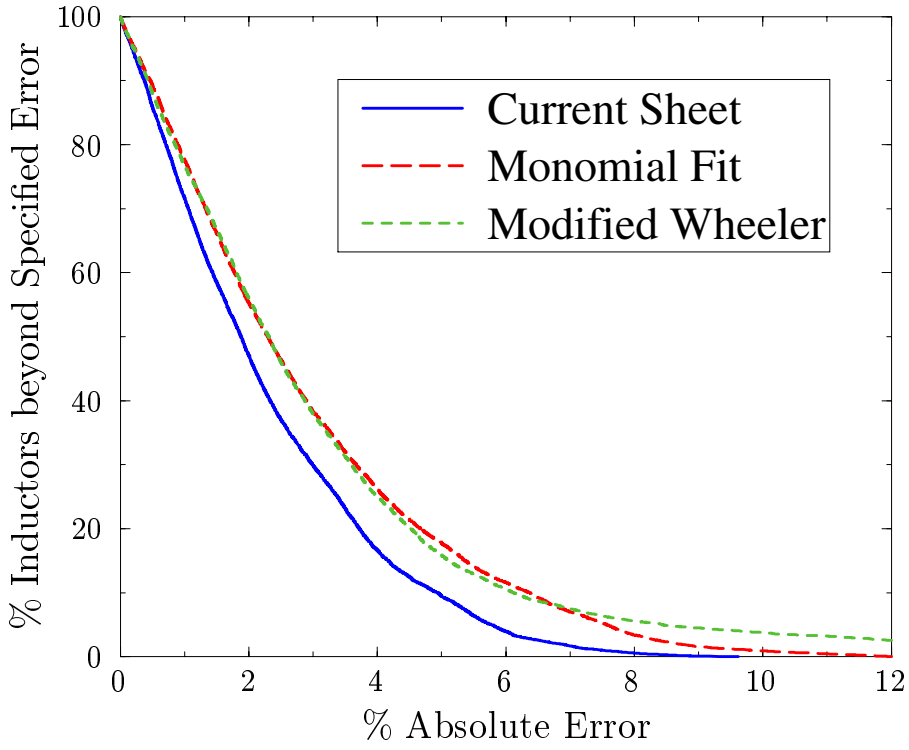


Figure 4.3: Error distribution for the new expressions for hexagonal inductors, compared to field solver simulations ($\approx 8,000$).

Figure 4.3 shows the absolute error distributions of our expressions for hexagonal inductors. The comparison is carried out for $\approx 8,000$ inductors spanning a wide design space. Table 4.6 summarizes the extent of the design space. Table 4.7 summarizes the error statistics of our expressions for this design space. Once again, the current sheet expression exhibits the best performance with worst case errors less than 9%.

Figure 4.4 shows the absolute error distributions of our expressions for octagonal inductors. The comparison is carried out for $\approx 12,000$ inductors spanning a wide design space. Table 4.8 summarizes the extent of the design space. Table 4.9

	Min	Max
L(nH)	0.1	48
OD(μm)	90	350
n	1	20
s/w	0.03	3
ρ	0.01	0.90

Table 4.6: Design space used for simulating hexagonal inductors

Computation Method	Min	Max	Mean	Median	StD
Current sheet	-9.62	7.25	-0.28	-0.26	2.88
Monomial fit	-11.38	12.08	0.24	0.71	3.68
Modified wheeler	-29.84	8.11	-0.39	0.44	4.43

Table 4.7: Error statistics (in %) of expressions for hexagonal inductors ($\approx 8,000$ simulations)

summarizes the error statistics of our expressions for this design space. The current sheet expression exhibits the best performance with worst case errors less than 9%.

4.3 Measurement Results

In this section, we compare the inductance values predicted by previously published expressions as well as new expressions to measurement results. We use both our own measurements as well as previously published measurements.

Figure 4.5 shows the measurement setup. The raw S parameters of the device under test (DUT) are used to extract the low frequency inductance, L, as follows:

	Min	Max
L(nH)	0.1	57
OD(μm)	100	360
n	1	20
s/w	0.03	3
ρ	0.01	0.90

Table 4.8: Design space used for simulating octagonal inductors

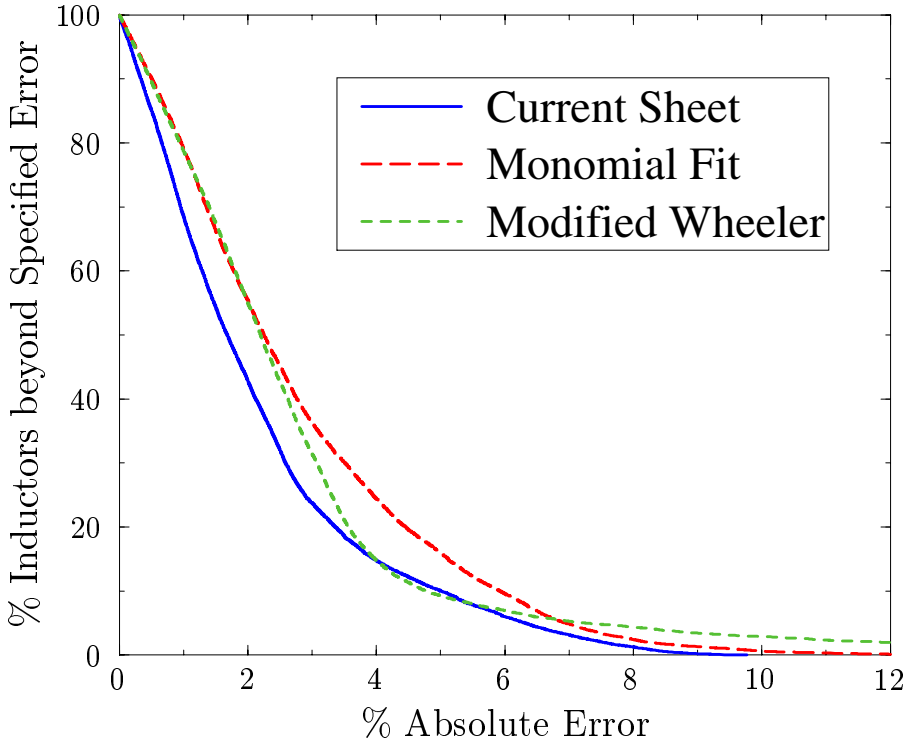


Figure 4.4: Error distribution for the new expressions for octagonal inductors, compared to field solver simulations ($\approx 12,000$).

Computation Method	Min	Max	Mean	Median	StD
Current sheet	-9.77	4.98	-0.72	-0.09	2.78
Monomial fit	-12.88	10.18	-0.00	0.60	3.51
Modified wheeler	-28.59	6.84	-0.28	0.76	3.87

Table 4.9: Error statistics (in %) of expressions for octagonal inductors ($\approx 12,000$ simulations)

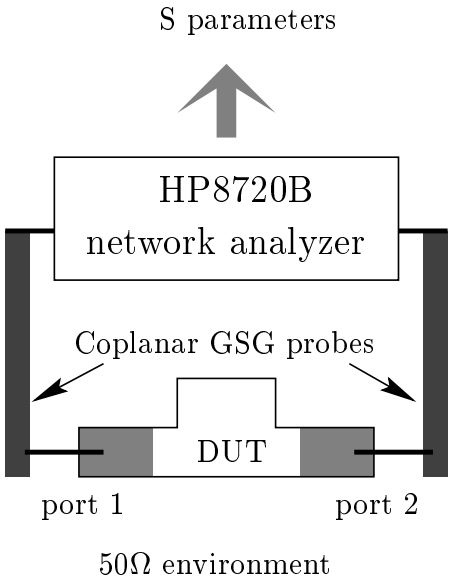


Figure 4.5: Experimental set up for measuring inductance

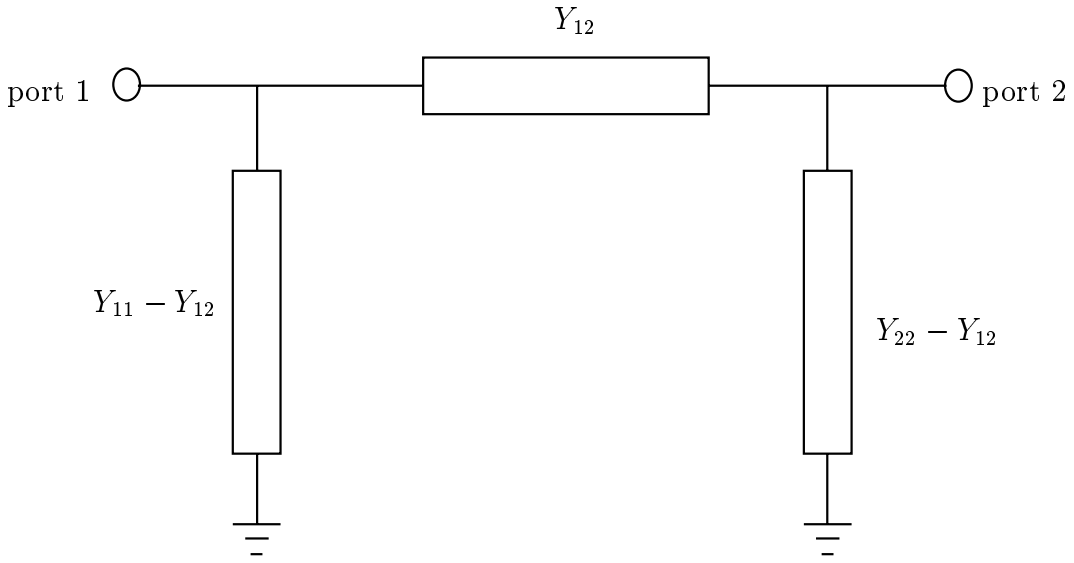


Figure 4.6: Y parameter extraction

1. DUT : S-to-Y ($\mathrm{Y_{DUT}}$)
2. Open calibration: S-to-Y ($\mathrm{Y_O}$)
3. $\mathrm{Y_{Cor}} = \mathrm{Y_{DUT}} - \mathrm{Y_O}$
4. $\mathrm{Y_{Cor}}$ to equivalent π model as illustrated in figure 4.6
5. $L = \frac{1}{\omega}\mathrm{IMAG}(\frac{1}{\mathrm{Y_{12}}})$

Figure 4.7 compares the experimental values to the inductances predicted by previously published expressions, while Figure 4.8 compares the experimental values to the inductance predicted by our formulas as well as *ASITIC*. Once again, it is clear that our expressions exhibit much smaller errors compared to the previous ones. It is also interesting to note how well the predictions of *ASITIC* compare to our expressions. This is particularly of interest in those few cases where the errors between experiment and our expressions approach 20%, which suggests substantial measurement errors, either in calibration or parameter extraction. More important, it is clear that our expressions perform as well as a field solver.

In Table 4.10 we compare the measured inductance values with those predicted by the various expressions. The first fifteen inductors shown in Table 4.10 were fabricated using the top metal level (of thickness 0.9μm) of a 0.35μm CMOS process. The data for the remaining inductors were obtained from previously published work. The first column in Table 4.10 gives the inductor number; the second column shows the source of the inductor data; the third column shows the number of sides; the fourth is the number of turns (n); the fifth, sixth and seventh columns are the outer diameter (d_{out})turn width (w) and spacing (s) in μm; the eighth column shows the measured or reported value of the inductance (L_{meas}) in nH. In the ninth column we give the percent relative error between L_{meas} and (L_{asi} predicted by *ASITIC*), which we define as $e_{\mathrm{meas}} = 100\,(L_{\mathrm{meas}} - L_{\mathrm{asi}})\,/L_{\mathrm{meas}}$. In the final three columns we give the corresponding relative errors e_{whe}, e_{gmd} and e_{mon} for our inductance expressions (4.4), (4.1) and (4.3) respectively.

We observe close agreement between our expressions and the measured data, with larger errors for the smaller inductors. The reason, as explained in [5], is that

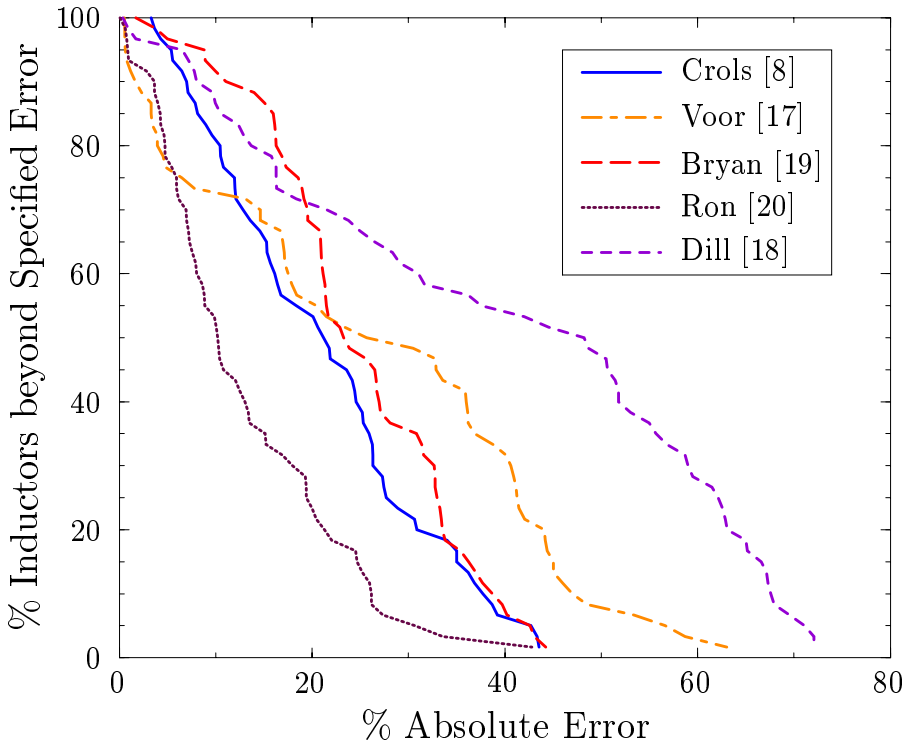


Figure 4.7: Error distribution of previous formulas, compared to measurements.

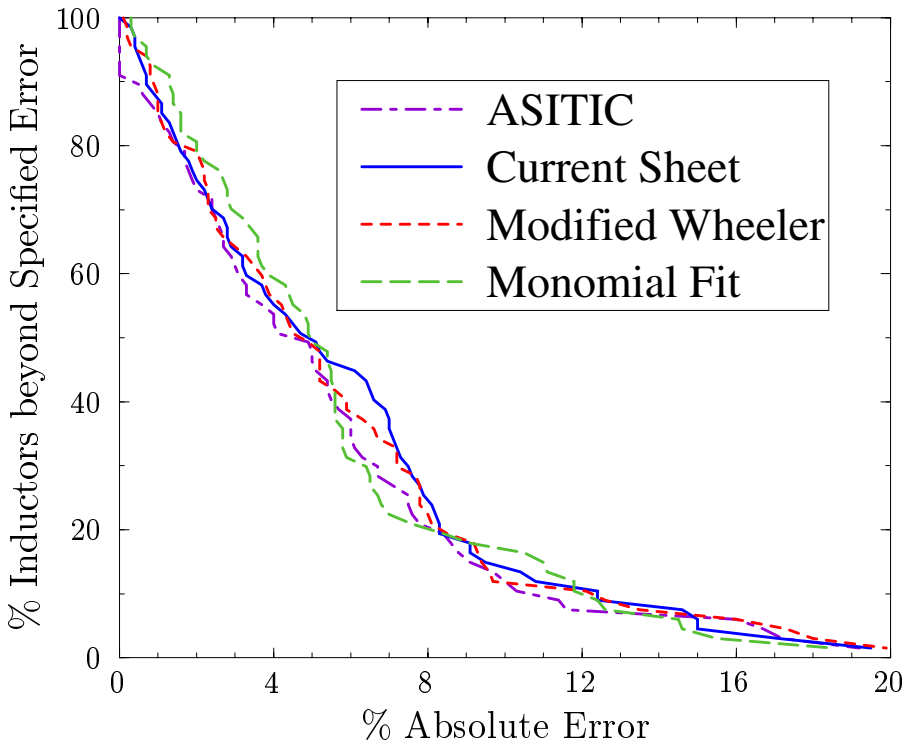


Figure 4.8: Error distribution of new expressions, compared to measurements.

the parasitic inductance inherent in the measurement setup results in large apparent relative errors for low inductance values.

We can also put the accuracy of our formulas in the context of other variations and uncertainties in a spiral inductor. A major limitation in the design, modeling and simulation of spirals is the uncertainty in the oxide thickness due to process variations. Process variations can cause the parasitic capacitances in the inductor model to vary by around 5–10%. These variations translate to an uncertainty in the impedance of the spiral that is of the same order of magnitude as the errors introduced by our expressions. This limitation suggests that inductance expressions with better accuracies than what we have achieved are not necessary and that our expressions are acceptable for use in circuit design and optimization.

4.4 Summary

In this chapter, we have presented three simple, approximate expressions for spiral inductors of square, hexagonal and octagonal geometries. The first expression is derived from electromagnetic principles by approximating the sides of the spiral by current sheets with uniform current distribution. This expression is intuitive and similar in form to inductance expressions for more conventional elements such as coaxial transmission lines and parallel wire transmission lines. The second expression is obtained by data-fitting the coefficients with a monomial expression. Although it lacks the physically intuitive derivation of the first expression, it is very well suited for optimization of circuits using geometric programming. The final expression, called the modified Wheeler expression, is obtained by modifying an expression that Wheeler obtained for discrete inductors.

All three expressions match field solver simulations well, with typical errors of 2–3%, and most errors smaller than around 8%. This represents a great improvement over previously published expressions, which have typical errors of around 20% or more. When compared to experimental data, the errors of our three expressions are comparable to those of a field solver, which suggests that the errors may be due, at least in part, to measurement error. The simplicity, versatility and robustness of our

Inductor #	Source	sides	n	d_{out}	w	s	L_{meas}	e_{asi}	e_{whe}	e_{gmd}	e_{mon}
1	1	4	2.75	344	29.7	1.9	3.20	3.1	5.2	6.4	3.6
2	1	4	3.75	292	13.0	1.9	6.00	-1.7	-1.2	-0.7	-0.4
3	1	4	6.50	217	5.4	1.9	12.50	2.4	1.4	2.3	4.9
4	1	4	2.75	279	18.3	1.9	3.10	0.0	2.1	2.8	1.4
5	1	4	4.75	206	7.8	1.9	6.10	0.0	-0.7	0.3	2.0
6	1	4	7.50	166	3.2	1.9	12.40	4.0	2.2	3.2	5.5
7	1	4	9.50	153	1.8	1.9	18.20	2.7	0.8	1.9	2.7
8	1	4	2.75	277	18.3	0.8	3.10	0.0	0.8	1.3	-2.0
9	1	4	2.75	307	18.3	18.0	2.90	10.3	13.5	14.6	12.4
10	1	4	3.75	321	16.5	1.9	6.10	0.0	0.2	1.1	0.7
11	1	4	7.75	225	4.4	1.9	18.10	0.6	-0.9	0.0	2.9
12	1	4	3.75	193	9.1	1.9	4.00	7.5	6.6	7.5	8.4
13	1	4	5.00	171	5.4	1.9	6.10	4.9	3.0	3.8	5.8
14	1	4	3.25	400	31.6	1.9	4.90	4.1	7.2	8.3	5.9
15	1	4	5.75	339	10.0	1.9	16.20	3.7	2.0	2.7	4.5
16	1	4	12.00	180	3.2	2.1	20.50	2.0	-1.0	-0.4	3.9
17	1	4	7.00	300	13.0	7.0	8.00	5.0	5.6	4.0	9.1
18	[7]	4	6.00	400	24.0	7.0	8.00	8.8	9.2	7.6	12.6
19	[7]	4	8.00	300	5.0	4.0	22.10	-6.3	-9.6	-8.3	-7.6
20	[7]	4	4.00	300	5.0	4.0	9.20	-5.4	-3.3	-7.2	-6.4
21	[9]	4	9.00	210	6.5	5.5	7.70	2.6	8.0	4.5	11.8
22	[9]	4	8.00	226	6.0	6.0	9.00	-1.1	-1.0	-1.4	0.7
23	[16]	4	11.00	300	9.0	4.0	15.50	-11.6	-9.7	-12.4	-3.2
24	[16]	4	8.00	300	14.0	4.0	8.30	-8.4	-6.7	-9.5	-0.9
25	[16]	4	6.00	300	19.0	4.0	5.10	-7.8	-7.2	-9.1	-2.8
26	[16]	4	3.00	300	19.0	4.0	3.30	-6.1	-7.2	-6.1	-6.5
27	[16]	4	5.00	300	24.0	4.0	3.50	-5.7	-5.2	-7.3	-1.6
28	[16]	4	9.00	230	6.5	5.5	9.70	1.0	2.3	0.6	5.6
29	[16]	4	16.00	300	5.0	4.0	34.00	-7.6	-4.2	-6.9	1.6
30	[16]	4	6.00	300	9.0	4.0	11.70	-5.1	-7.8	-6.5	-4.9
31	[16]	4	3.00	300	9.0	4.0	5.50	5.5	6.3	3.7	4.8
32	[16]	4	4.00	300	14.0	4.0	5.80	-1.7	-4.4	-3.2	-2.6
33	[16]	4	2.00	300	14.0	4.0	2.90	17.2	18.0	15.0	15.5
34	[16]	4	2.00	300	19.0	4.0	2.50	16.0	16.0	15.0	14.5
35	[16]	4	3.00	300	24.0	4.0	3.10	9.7	5.9	7.1	6.5
36	[30]	4	5.00	154	7.0	5.0	3.00	6.7	3.9	4.3	5.8
37	[30]	4	9.00	250	7.0	5.0	12.00	-0.8	0.2	-0.5	3.7
38	[6]	4	6.00	285	15.0	3.0	6.70	-7.5	-9.4	-9.1	-5.6
39	[6]	4	3.50	255	10.0	1.5	5.00	-4.0	-4.5	-5.2	-4.4
40	[6]	4	4.50	216	10.0	1.5	5.00	-6.0	-7.8	-6.6	-5.4
41	[6]	4	5.50	199	10.0	1.5	5.00	-6.0	-9.3	-8.2	-5.8
42	[6]	4	6.50	191	10.0	1.5	5.00	-6.0	-8.1	-8.1	-3.6
43	[20]	4	7.50	190	10.0	1.5	5.00	-10.0	-8.5	-10.4	-2.8
44	[31]	4	9.25	145	5.2	2.0	6.00	-3.3	-5.2	-7.0	1.3
45	[31]	4	6.75	290	13.0	7.0	7.10	1.4	3.5	2.0	7.0
46	[31]	4	2.50	290	13.0	7.0	3.00	-3.3	-2.5	-3.3	-3.4
47	[32]	4	3.25	340	25.0	6.0	3.30	-9.1	-12.1	-10.8	-11.0
48	[32]	4	4.50	300	23.0	6.0	3.40	-2.9	-4.3	-5.1	-1.4
49	[32]	4	3.00	300	18.0	6.0	3.30	-3.0	-5.9	-4.7	-5.0
50	[32]	4	5.75	190	9.5	6.0	3.40	0.0	2.5	1.1	5.6
51	[32]	4	3.00	700	90.0	6.0	3.70	-5.4	-4.9	-5.4	-6.7
52	[33]	4	4.00	262	16.0	10.0	2.60	-19.2	-19.9	-19.5	-18.5
53	[33]	4	6.00	392	16.0	10.0	8.80	-11.4	-12.6	-12.4	-10.5
54	[33]	4	8.00	532	16.0	10.0	20.40	-16.7	-17.3	-17.1	-14.6
55	[?]	8	4.00	346	18.0	2.0	5.90	0.0	-1.1	-1.6	-3.6
56	[?]	8	5.00	346	18.0	2.0	7.50	2.7	2.7	0.7	0.3
57	[?]	8	4.00	326	8.0	12.0	5.60	-7.1	-7.7	-7.8	-11.8
58	[?]	8	5.00	326	8.0	12.0	7.20	-2.5	-1.0	-2.8	-5.6
59	[11]	12	6.75	197	8.2	3.0	5.45	1.8	-	1.5	-
60	[11]	12	8.00	198	7.5	3.0	6.30	-0.5	-	-1.8	-
61	[11]	12	7.75	198	6.5	3.0	7.30	-1.9	-	-2.2	-

Table 4.10: Comparison of measured inductance values with field solver inductance values and the various approximate expressions.

expressions make them good candidates for circuit design. They can be included in a physical, scalable lumped-circuit model for spiral inductors where, in addition to providing design insight, they allow efficient optimization schemes to be employed.

Chapter 5

Modeling and Characterization of On-Chip Transformers

This chapter discusses the modeling of on-chip transformers. Section 5.1 introduces the main elements of an ideal transformer and then considers the parasitics present in practical transformer realizations. Section 5.2 compares the advantages and disadvantages of various on-chip transformer realizations. Section 5.3 expands upon the lumped inductor model presented in chapter 2 to model on-chip transformers. A key element in these transformer models is the mutual inductance between the primary and secondary. Sections 5.3.1 and 5.3.2 describe how the current sheet approach developed in chapter 3 and inductance expressions developed in chapter 4 can be used to obtain simple expressions for the mutual inductance and mutual coupling coefficient (k) of a variety of on-chip transformer realizations. Section 5.4 provides expressions for the parasitic resistances and capacitances in the transformer models. Section 5.5 illustrates, with examples, how the concepts developed in the preceding sections may be applied to obtain on-chip transformer models. The predictions of these models are compared to experimental results in section 5.6.

5.1 Transformer Fundamentals

An ideal transformer, as illustrated in figure 5.1 contains three components:

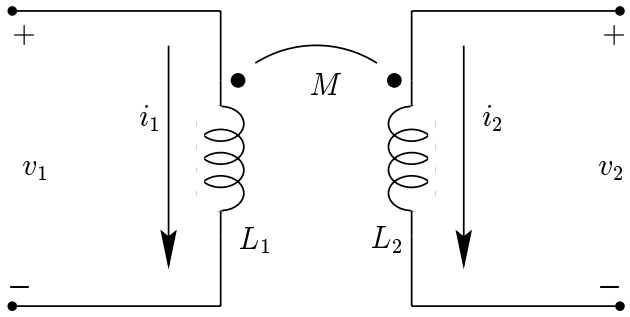


Figure 5.1: Ideal transformer

1. The self inductance of the primary (L_1).
2. The self inductance of the secondary (L_2).
3. The mutual inductance between the primary and the secondary (M).

The terminal voltages and currents of an ideal transformer are specified by equation 5.1:

$$\begin{aligned} v_1 &= L_1\frac{\partial i_1}{\partial t} + M\frac{\partial i_2}{\partial t} \\ v_2 &= L_2\frac{\partial i_2}{\partial t} + M\frac{\partial i_1}{\partial t}. \end{aligned} \tag{5.1}$$

The mutual inductance, M, is related to the self inductances, L_1 and L_2, by the mutual coupling coefficient, k:

$$k = \frac{M}{\sqrt{L_1 L_2}}. \tag{5.2}$$

In general, $|k| \leq 1$ because the transformer is a passive device. While $k = 1$ for an ideal transformer, most practical on-chip transformers exhibit k values between $0.3 - 0.9$. In addition to reduced k, practical transformers suffer from several nonidealities. Figure 5.2 illustrates the important parasitic resistances and capacitances present in practical transformers. Resistances R_1 and R_2 model the series resistances of the primary and secondary spirals respectively. The figure also shows the various

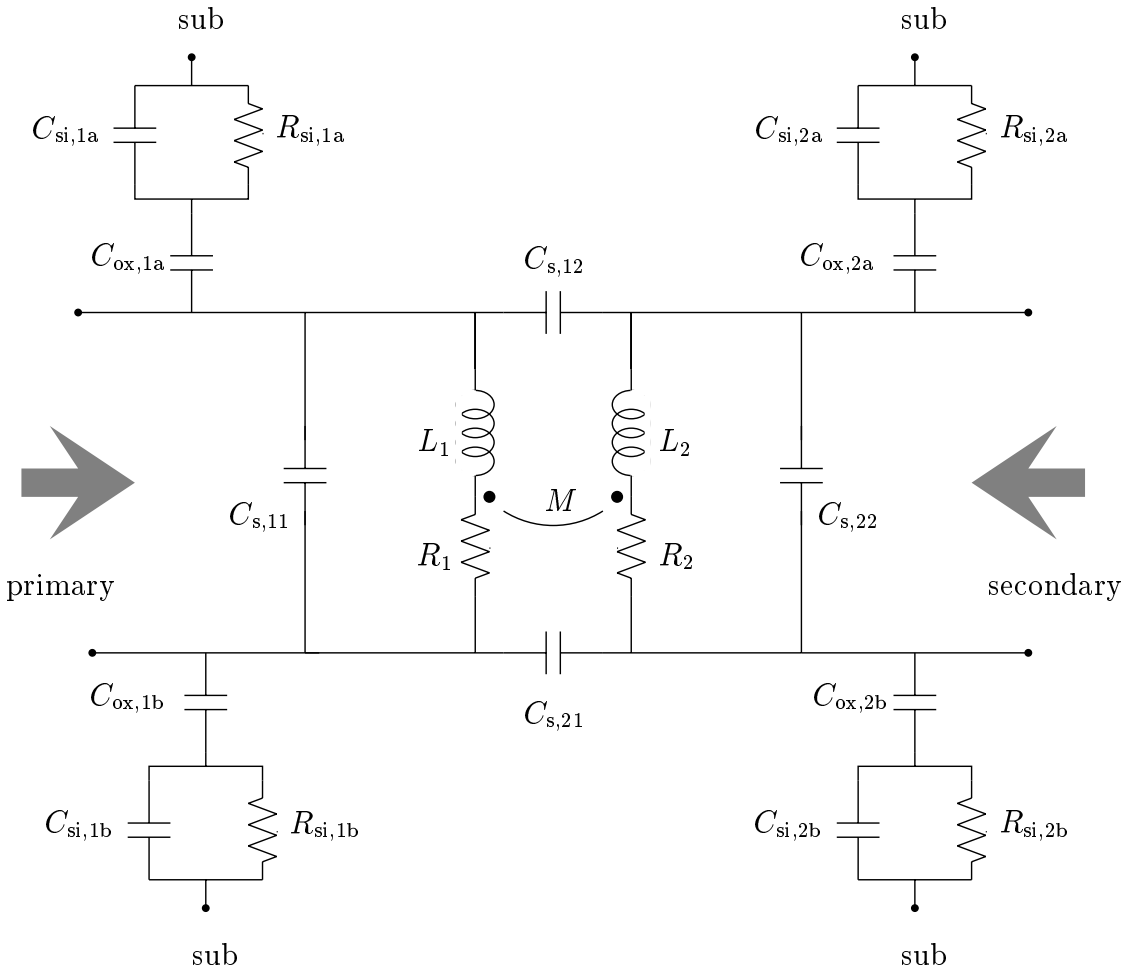


Figure 5.2: Nonideal transformer

elements used to model the spiral-to-substrate oxide capacitances ($C_{\mathrm{ox,1a}}$, $C_{\mathrm{ox,1b}}$, $C_{\mathrm{ox,2a}}$ and $C_{\mathrm{ox,2b}}$), the terminal-to-terminal oxide capacitances ($C_{\mathrm{s,11}}$, $C_{\mathrm{s,22}}$, $C_{\mathrm{s,12}}$ and $C_{\mathrm{s,21}}$) and the resistive and capacitive coupling to the substrate ($R_{\mathrm{si,1a}}$, $C_{\mathrm{si,1a}}$, $R_{\mathrm{si,1b}}$, $C_{\mathrm{si,1b}}$, $R_{\mathrm{si,2a}}$, $C_{\mathrm{si,2a}}$, $R_{\mathrm{si,2b}}$ and $C_{\mathrm{si,2b}}$).

A transformer may be configured as a three or four terminal device. Furthermore, one or more terminals may be connected to incremental ground. The self inductances, series resistances and mutual inductances are independent of the configuration of the transformer. However, some of the capacitive elements may be shorted out. This situation is analogous to that a spiral inductor being used as either a single or dual terminal device.

5.2 Monolithic Transformer Realizations

The relative importance of the parasitic elements varies among different transformer realizations and configurations. This section discusses various on-chip transformer realizations and highlights the dominant non-idealities.

5.2.1 Tapped Transformer

The tapped transformer, illustrated in figure 5.3 is best suited for three-terminal applications. Although not symmetric, it permits a variety of tapping ratios to be realized. This transformer relies only on lateral magnetic coupling. All windings can be implemented with the top metal layer, thereby minimizing terminal-to-substrate capacitances. Since the two inductors occupy separate regions, the self-inductance is maximized while the terminal-to-terminal capacitance is minimized. Unfortunately, this spatial separation also leads to low mutual coupling ($k \approx 0.3 - 0.5$).

5.2.2 Interleaved Transformer

The interleaved transformer, illustrated in figure 5.4 is best suited for four-terminal applications that demand symmetry. Once again, capacitances can be minimized by implementation on top level metal so that high resonant frequencies may be realized.

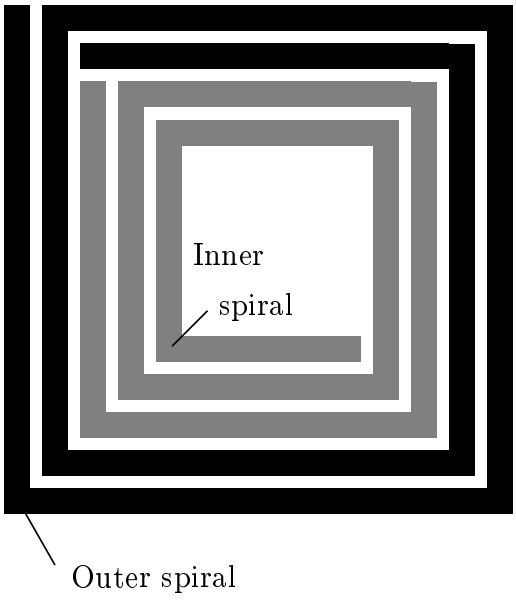


Figure 5.3: Tapped transformer

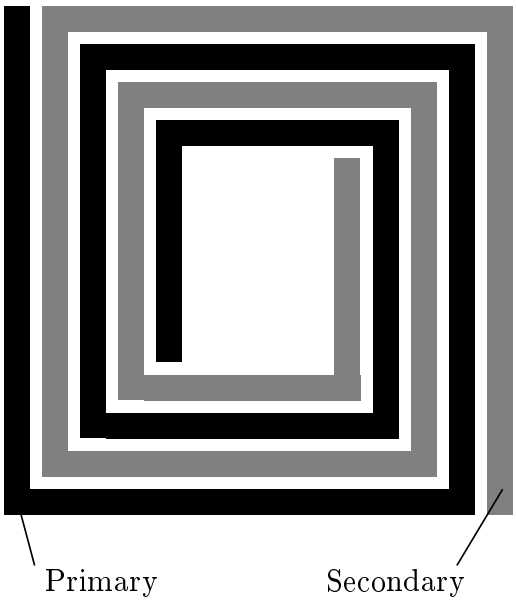


Figure 5.4: Interleaved transformer

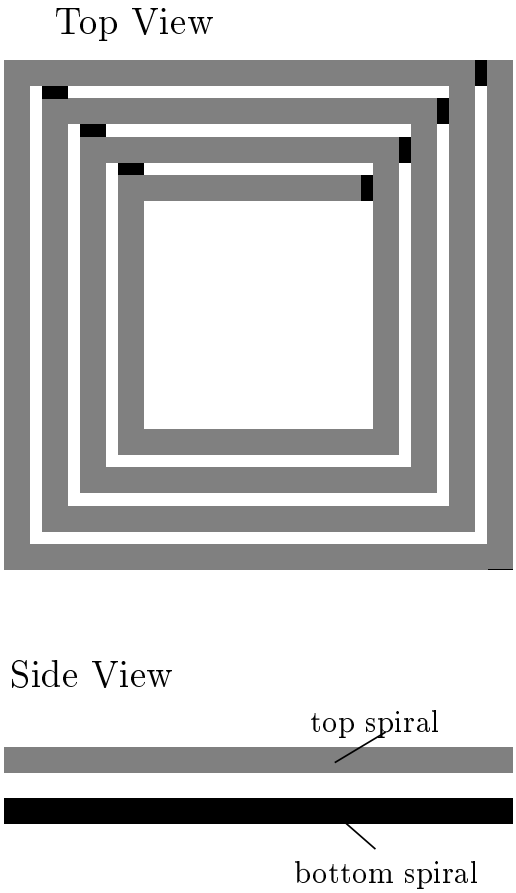


Figure 5.5: Stacked transformer

The interleaving of the two inductances permit moderate coupling ($k \approx 0.7$) to be achieved at the cost of reduced self-inductance. This coupling may be increased at the cost of higher series resistance by reducing the turn width, w, and spacing, s.

5.2.3 Stacked Transformer

The stacked transformer, illustrated in figure 5.4 uses multiple metal layers and exploits both vertical and lateral magnetic coupling to provide the best area efficiency, the highest self-inductance and highest coupling ($k \approx 0.9$). This configuration is suitable for both three and four terminal configurations. The main drawback is

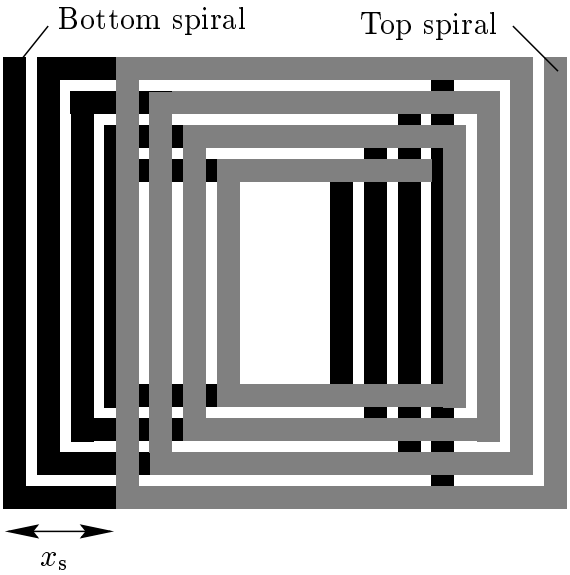


Figure 5.6: Stacked transformer with top and bottom spiral laterally shifted

the high terminal-to-terminal capacitance, or equivalently a low self-resonance frequency. In some cases, such as narrowband transformers, this capacitance may be incorporated as part of the resonant circuit. Also, in modern multilevel processes, the capacitance can be reduced by increasing the oxide thickness between spirals. For example, in a five metal process, $50 - 70\%$ reductions in terminal-to-terminal capacitance can be achieved by implementing the spirals on layers five and three instead of five and four. The increased vertical separation reduces k by less than 5%.

5.2.4 Variations on the Stacked Transformer

As illustrated in figures 5.6 and 5.7, one can trade off reduced k for reduced terminal-to-terminal capacitance by displacing the centers of the stacked inductors either laterally or diagonally.

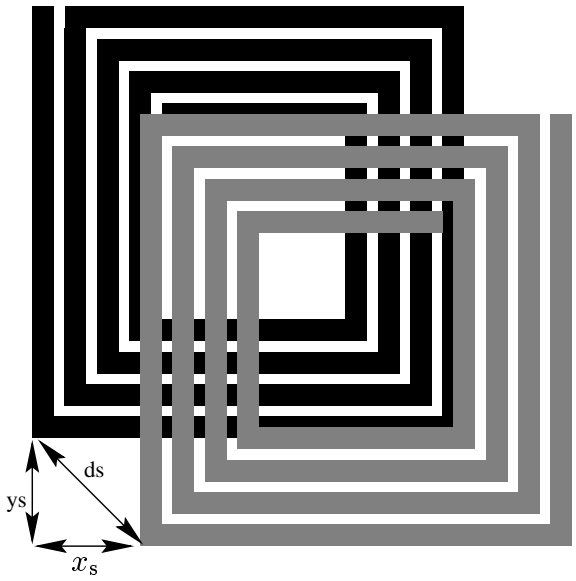


Figure 5.7: Stacked transformer with top and bottom spiral diagonally shifted

5.2.5 Stacked InterleavedTransformer

One potential drawback of the stacked transformer and its variations discussed so far is that these realizations are not symmetric. A symmetric transformer that achieves the area efficiency of a stacked transformer may be obtained by stacking two interleaved transformers on top of one another. Figure 5.8 illustrates the details of such a stacked interleaved transformer. Unlike the stacked transformer where the primary and secondary occupy distinct metal layers, the stacked interleaved transformer has the primary and secondary spirals interleaved on both layers, thereby achieving a symmetrical layout.

In this case, the primary spirals are stacked on top of one another (except of course for the crossover points required to keep the same current orientation in the top and bottom spirals) and so are the secondary spirals. This implementation minimizes the primary-to-secondary capacitance at the cost of increased primary-to-primary and secondary-to-secondary capacitance. In tuned circuit applications, the primary-to-primary and secondary-to-secondary capacitances are more easily

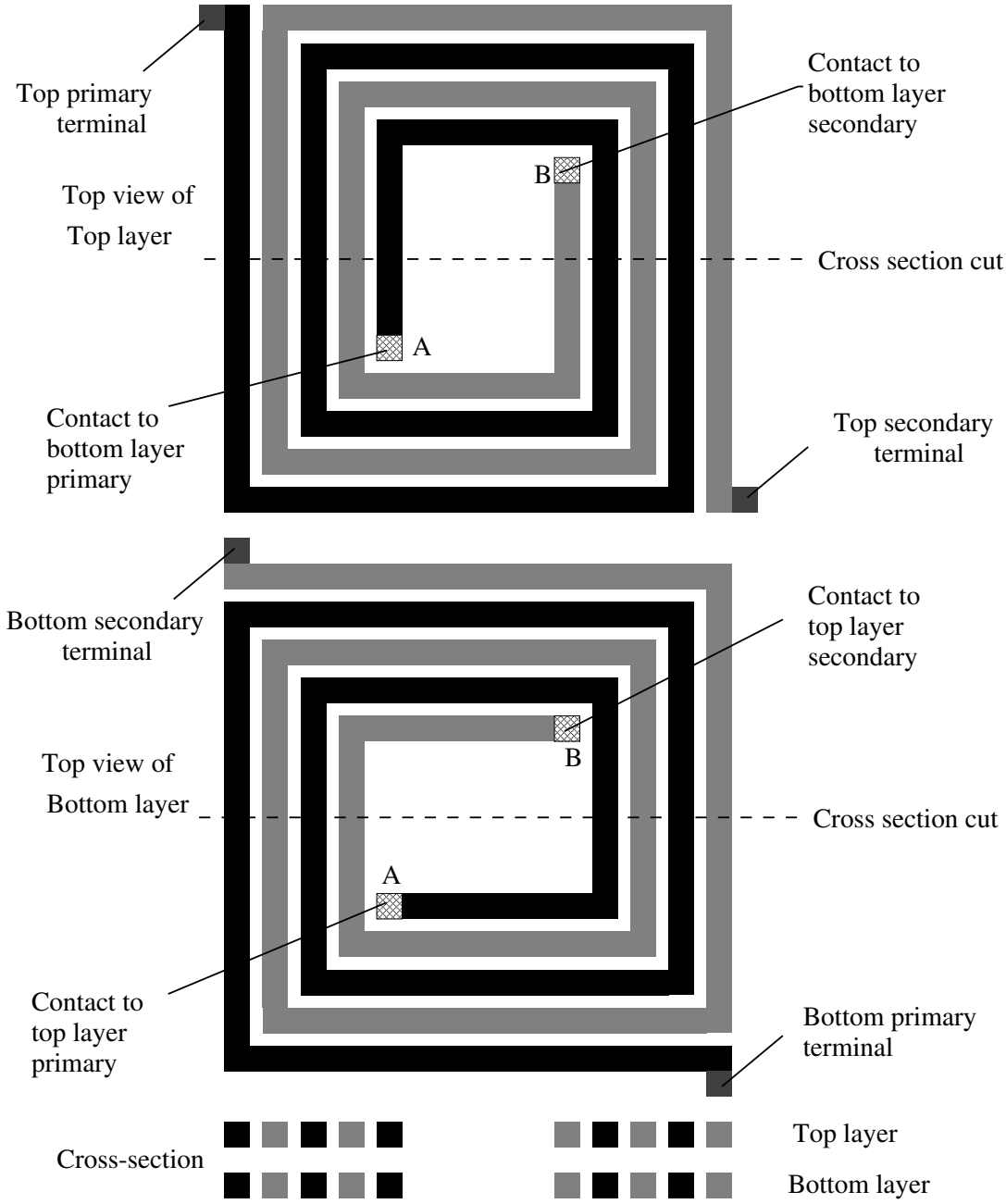


Figure 5.8: Stacked interleaved transformer

incorporated into the tuning network than the primary-to-secondary capacitance. Therefore, this transformer is ideal for those narrowband applications that require symmetry.

The mutual coupling coefficient of the stacked interleaved transformer is comparable to that of the interleaved transformer. However, the stacking of multiple layers enables an increase in the overall inductance density by a factor of $\approx 3.5-3.9$. The self inductances of the primary and secondary are larger than the corresponding stacked transformer implementation. However, the mutual inductance is lower, which is consistent with the observation that the total inductance densities of a stacked transformer and the corresponding stacked interleaved transformer should be approximately the same.

5.2.6 Comparison of Transformer Realizations

The different realizations offer varying trade-offs among the self inductance and series resistance of each terminal, the mutual coupling coefficient, the terminal-to-terminal and terminal-to-substrate capacitances, resonance frequencies, symmetry and area. Table 5.1 summarizes the attributes of the main on-chip transformer realizations. The characteristics desired for a transformer are application dependent. For example, in single-sided to differential conversion, the transformer might be used as a four terminal narrowband device. In this case, a high mutual coupling coefficient and high self-inductance are desired along with low series resistance. On the other hand, for bandwidth extension in broadband circuits, the transformer is used as a three terminal device. In this case, a small mutual coupling coefficient ($k \approx 0.3-0.4$) and high series resistance are acceptable while all capacitances need to be minimized [34].

Accurate, lumped transformer models are needed to select the best transformer realization for a given application. The following sections of this chapter develop a general approach to modeling on-chip transformers with lumped circuit elements.

5.3 Analytical Transformer Models

The modeling approach discussed in this chapter is based on finding analytical expressions for the circuit elements of figure 5.2. The model is realized by representing the primary and secondary spirals by their equivalent lumped π models (in essence by treating them as individual spiral inductors) and then adding in the mutual inductance and primary-to-secondary coupling capacitances. The self inductances, L_1 and L_2, may be computed using the inductance expressions that were presented in chapter 4. The mutual inductance can be calculated with the aid of these inductance expressions as will be outlined in sections 5.3.1 and 5.3.2. The parasitic capacitances and resistances can be estimated by techniques similar to those used in the lumped circuit modeling of on-chip inductors. While figure 5.2 shows a complete lumped model of a non-ideal transformer, a particular realization and configuration of a practical on-chip transformer usually contains a smaller subset of the parasitic capacitances. Furthermore, symmetry considerations can reduce the number of computations.

As in the modeling of any distributed system, the lumped circuit approach breaks down at higher frequencies. The model is typically accurate up to the self-resonance frequencies of the primary and secondary inductors, which is the useful frequency range of the transformer. The advantage of these lumped, analytical models is that they enable the designer to explore trade-offs, to obtain design insight and to identify the most appropriate transformer for a given application. These models also permit the designer to quickly optimize a transformer circuit and to narrow the search region in a design space. Thus, time consuming and computationally intensive field solvers are now needed only at the final design and verification stage at most, thereby significantly reducing the required resources and time.

5.3.1 Inductances of Tapped and Interleaved Transformers

Figure 5.9 illustrates how the inductance expressions developed in chapter 4 can be used to calculate the mutual inductance between the primary and secondary for

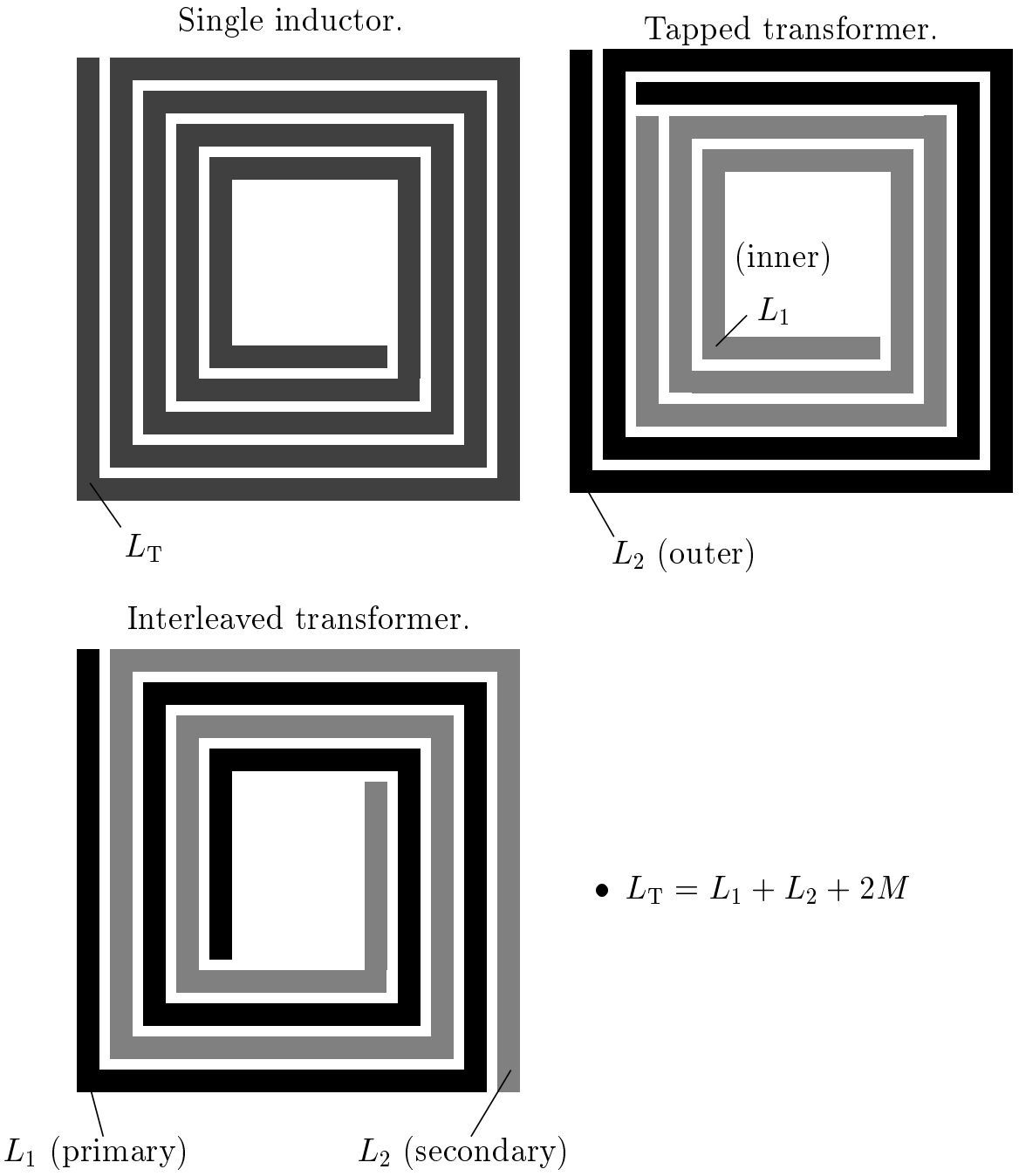


Figure 5.9: Calculation of mutual inductance for tapped and interleaved transformers

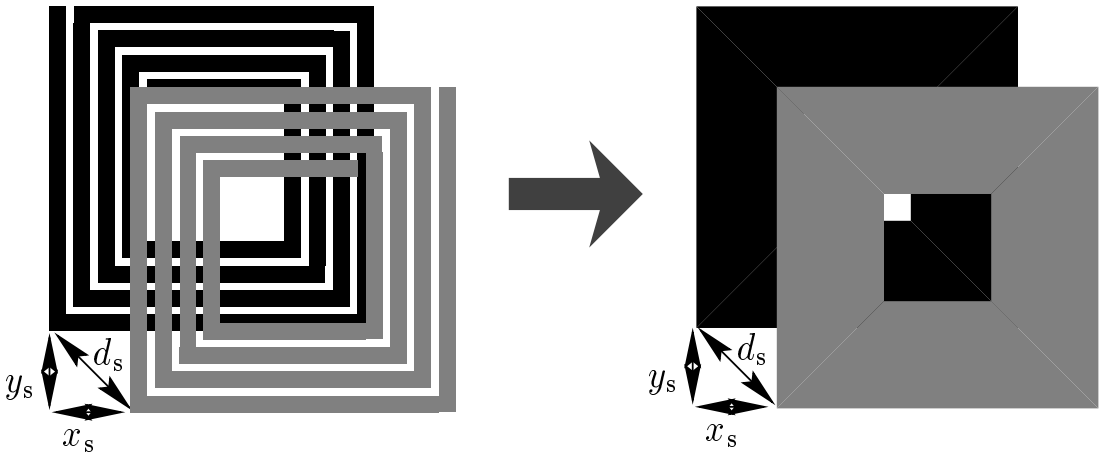


Figure 5.10: Current sheet approximation for estimating k for stacked transformers

a tapped or interleaved transformer. First the self inductance of a single spiral, L_T, containing all the segments of the primary and secondary spirals, is evaluated using the inductance expression. Then, the self inductances of the primary and secondary spirals, L_1 and L_2, are calculated using the same inductance expressions. The mutual inductance, M, is related to the self inductances and the total inductance by $L_T = L_1 + L_2 + 2M$. M is the only unknown in this equality and can therefore be computed as $M = (L_T - L_1 - L_2)/2$.

5.3.2 Inductances of Stacked Transformers

Figure 5.10 illustrates how the two spirals of a stacked transformer can be approximated by equivalent current sheets. This approximation substantially reduces the complexity of calculating the mutual inductance between the spirals. The current sheet approach described in chapter 3 can be applied to obtain an approximate expression for k. For the sake of simplicity, we restrict this discussion to stacked transformers whose top and bottom spirals have identical lateral geometries and therefore approximately equal inductances since the inductances are only weakly dependent on the conductor thickness. The approach may be extended to stacked

spirals with differing dimensions. The current sheet approximation suggests that k may be approximated by:

$$k \approx 0.9 - \frac{d_{\mathrm{s}}}{d_{\mathrm{avg}}}, \tag{5.3}$$

where d_{s} is the center-to-center spiral distance and d_{avg} is the average diameter of the spirals. As one expects, k is maximum when the top and bottom spirals completely overlap one another ($d_{\mathrm{s}} = 0$). As the overlap is reduced, k decreases linearly with increasing d_{s}. Using equation 5.3 to calculate k, and using our inductance expression to calculating the inductance of one spiral (L_{t}), the mutual inductance of a stacked transformer may be calculated from $M = kL_{\mathrm{t}}$.

This approximate expression for k is valid to within 5% for $k > 0.2$. Since most transformer applications seek $k > 0.3$, this approximation is good enough for typical design purposes. The thicknesses of the top and bottom metal layers and the thickness of the oxide between them has only a second order effect on k. This is because the lateral dimensions are much larger than the vertical dimensions for practical on-chip transformers. Thus, variations in the vertical dimension result in k changing by less than 5% and can therefore be neglected at the initial design stage.

As d_{s} increases beyond $0.7d_{\mathrm{avg}}$, the mutual coupling coefficient becomes harder to model with a current sheet approximation. However, this approach is still useful for estimating the order of magnitude of k for large d_{s}. Around $d_{\mathrm{s}} \approx d_{\mathrm{avg}}$, k crosses zero and reaches a minimum value of ≈ -0.1 . As d_{s} increases further, k asymptotically approaches zero. At $d_{\mathrm{s}} \approx 2\mathrm{AD}$, $k \approx -0.02$, indicating that the magnetic coupling between closely spaced spirals is negligible. This insight is valuable because it indicates that one may generally pack many spirals on a chip with impunity.

5.4 Calculation of Parasitic Elements

The series resistances of the primary and secondary spirals of any transformer may be easily calculated using the expression developed for the series resistance of an on-chip inductor. Thus, for the series resistance of the primary, R_1:

$$R_1 = \frac{\rho \cdot l_1}{\delta \cdot w_1 \cdot \left(1 - \mathrm{e}^{-\frac{\mathrm{t}_1}{\delta_1}}\right)}, \tag{5.4}$$

where l_1 is the length of the primary spiral, w_1 is its conductor width, t_1 is its conductor thickness and δ_1 is the corresponding skin depth. The series resistance of the secondary may be computed similarly. Note that the model accounts for the increase in series resistance with frequency due to skin effect.

The calculation of the transformer's parasitic capacitances is, at least in principle, similar to the calculation of an inductor's parasitic capacitance. However, the increased number of capacitances requires more work, especially in the case of stacked transformers with partial overlap. Nevertheless, all dominant capacitances may be modeled using parallel plate capacitance approximations.

For single layer transformer implementations (such as the tapped and interleaved transformers illustrated in figures 5.3 and 5.4) the dominant capacitances are the spiral-to-substrate oxide capacitances of the primary and the secondary. These spiral-to-substrate capacitances are easily calculated using the parallel plate approximation. In the lumped circuit model, each one of these capacitances is represented by two capacitances at the terminals of the corresponding terminal. For example, the primary's spiral-to-substrate oxide capacitances are represented by $C_{\mathrm{ox,1a}}$ and $C_{\mathrm{ox,1b}}$ in figure 5.2. The values of these capacitances are:

$$C_{\mathrm{ox,1a}} = C_{\mathrm{ox,1b}} = \frac{\epsilon_{\mathrm{ox}}}{2\mathrm{t}_{\mathrm{ox}}} \cdot l_1 \cdot w_1, \tag{5.5}$$

where l_1 is the length of the primary spiral, w_1 is its conductor width, and t_{ox} is the thickness of the oxide from the spiral to the substrate. Similarly, terminal-to-terminal oxide capacitances, which are determined by the spiral-to-underpass

capacitances can be computed using the expression obtained for the feedthrough capacitance of a spiral inductor (see figure 5.11 and table 5.2 for an example that provides detailed expressions for the elements of a tapped transformer).

The parasitic capacitance calculations for stacked transformers requires more scrutiny. First, we consider the capacitances of a stacked transformer (made of two spirals with identical lateral dimensions) with maximum overlap so that $d_s = 0$. In this case, the dominant capacitances are the primary-to-secondary capacitances (which correspond to $C_{s,12}$ and $C_{s,21}$ in figure 5.2 with $C_{s,21} = C_{s,12}$) and the spiral-to-substrate capacitance of the bottom spiral, both of which may be computed using the parallel plate approximation. As one of the spirals is laterally or diagonally shifted with respect to the other, d_s increases. Consequently, the spiral-to-substrate oxide capacitances of the top spiral increase while the primary-to-secondary capacitances decrease. As one may expect, the spiral-to-substrate oxide capacitances of the bottom spiral remains unchanged. These capacitances may be quantified by considering the ratio of the overlap area between the spirals to the area of one spiral. Figure 5.12 and table 5.3 illustrate this computation with an example.

The process for evaluating the resistive and capacitive coupling to the substrate is identical to the one used for spiral inductors, and therefore requires prior knowledge of the substrate conductivity, which can vary over a large range with process variations and silicon depth. The use of a patterned ground shield (PGS) eliminates these terms from the model and is therefore valuable when the substrate doping profile is not known. However, the magnetic coupling to the substrate is not eliminated by the PGS. Another drawback is that since the PGS is typically implemented in polysilicon, the oxide capacitance from spiral to ground is increased.

5.5 Examples of Transformer Models

This section illustrates the concepts developed in the last section by providing complete models (except for magnetic coupling to the substrate) for transformers built in particular configurations. These configurations were chosen to permit easy comparison to measurements made using a two terminal network analyzer. Thus, the

models are presented for transformers in a three terminal configuration, with one of these terminals connected to ground or being left as an open. Consequently, when compared to the full model illustrated in figure 5.2, these models have fewer elements as some of the capacitive elements have been shorted out. Furthermore, the substrate coupling elements are not included on the premise that a patterned ground shield is implemented in polysilicon and placed beneath the transformer (once again, with the limitation that the magnetic coupling term is not properly accommodated).

Figure 5.11 presents the analytical model for a tapped transformer implemented with square spirals (see figure 5.3). In this case, the inner end of the inner spiral is connected to ground, while the outer end of the outer spiral is connected to terminal 1 and the inner end of the outer spiral (which is also the outer end of the inner spiral) is connected to terminal 2. Table 5.2 tabulates the corresponding element values (Subscript 'o' refers to the outer spiral, 'i' to the inner spiral and 'T' to the whole spiral)

Figure 5.12 presents the analytical model for a three terminal stacked transformer implemented with square spirals (see figures 5.5, 5.6 and 5.7). Table 5.3 tabulates the corresponding element values (Subscript 't' refers to the top spiral and 'b' to the bottom spiral).

5.6 Experimental Verification

The measurements were conducted on structures designed for operation as three terminal devices. One of the terminals was grounded while the other two terminals were terminated in the 50Ω environment of the test equipment. Two-terminal S-parameter measurements were obtained using an HP8720B network analyzer and coplanar ground-signal-ground probes. Figure 5.13 shows the measurement setup.

5.6.1 Verification of k for Stacked Transformers

The expression provided for the k of stacked transformers (equation 5.3) is verified in the experiment tabulated in table 5.4. Two 20nH inductors are stacked with various

Transformer type	**Area**	**Coupling coefficient, k**	**Self-inductance**	**Self-resonant frequency**
Tapped	High	Low	Mid	High
Interleaved	High	Mid	Low	High
Stacked	Low	High	High	Low

Table 5.1: Comparison of transformer realizations.

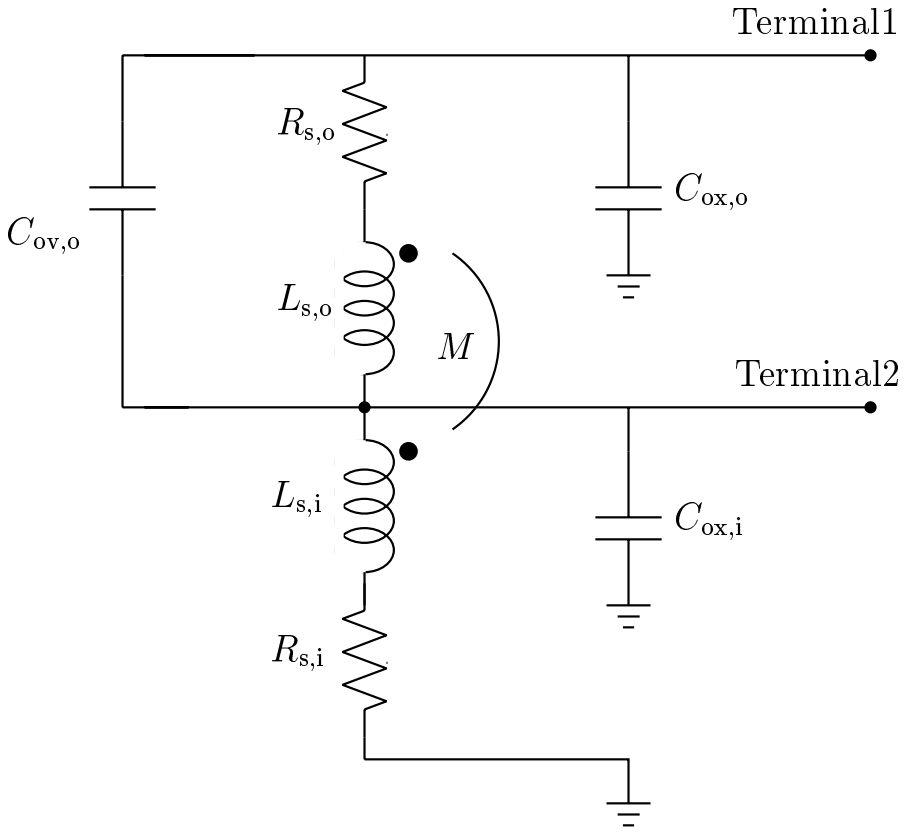


Figure 5.11: Tapped transformer model

Element	Expression
L_{o}	$\frac{2\mu n_{\mathrm{o}}^2 d_{\mathrm{avg,o}}}{\pi}\left[\ln\left(\frac{2.067}{\rho_{\mathrm{o}}}\right)+0.178\rho_{\mathrm{o}}+0.125\rho_{\mathrm{o}}^2\right]$
L_{i}	$\frac{2\mu n_{\mathrm{i}}^2 d_{\mathrm{avg,i}}}{\pi}\left[\ln\left(\frac{2.067}{\rho_{\mathrm{i}}}\right)+0.178\rho_{\mathrm{i}}+0.125\rho_{\mathrm{i}}^2\right]$
L_{T}	$\frac{2\mu n_{\mathrm{T}}^2 d_{\mathrm{avg,T}}}{\pi}\left[\ln\left(\frac{2.067}{\rho_{\mathrm{T}}}\right)+0.178\rho_{\mathrm{T}}+0.125\rho_{\mathrm{T}}^2\right]$
M	$\frac{L_{\mathrm{T}}-L_{\mathrm{o}}-L_{\mathrm{i}}}{2}$
k	$\frac{L_{\mathrm{T}}-L_{\mathrm{o}}-L_{\mathrm{i}}}{2\sqrt{L_{\mathrm{o}}L_{\mathrm{i}}}}$
$R_{\mathrm{s,o}}$	$\frac{\rho\cdot l_{\mathrm{o}}}{\delta\cdot w\cdot\left(1-\mathrm{e}^{-\frac{\mathrm{t}}{\delta}}\right)}$
$R_{\mathrm{s,i}}$	$\frac{\rho\cdot l_{\mathrm{i}}}{\delta\cdot w\cdot\left(1-\mathrm{e}^{-\frac{\mathrm{t}}{\delta}}\right)}$
$C_{\mathrm{ox,o}}$	$\frac{1}{2}\frac{\epsilon_{\mathrm{ox}}}{\mathrm{t}_{\mathrm{ox}}}\cdot l_{\mathrm{o}}\cdot w$
$C_{\mathrm{ox,i}}$	$\frac{1}{2}\frac{\epsilon_{\mathrm{ox}}}{\mathrm{t}_{\mathrm{ox}}}\cdot (l_{\mathrm{o}}+l_{\mathrm{i}})\cdot w$
$C_{\mathrm{ov,o}}$	$\frac{\epsilon_{\mathrm{ox}}}{\mathrm{t}_{\mathrm{ox,t-b}}}\cdot (n_{\mathrm{o}}-1)\cdot w^2$

Table 5.2: Expressions for elements in tapped transformer model (ρ=DC metal resistivity, δ=skin depth, $\mathrm{t_{ox}}$=oxide thickness from top metal to substrate, $\mathrm{t_{ox,t-b}}$=oxide thickness from top level metal to bottom level metal, k= mutual coupling coefficient, n=number of turns, $\mathrm{d_{avg}}$=average diameter, l=length of spiral $\approx 4nd_{\mathrm{avg}}$, w=turn width, t=metal thickness)

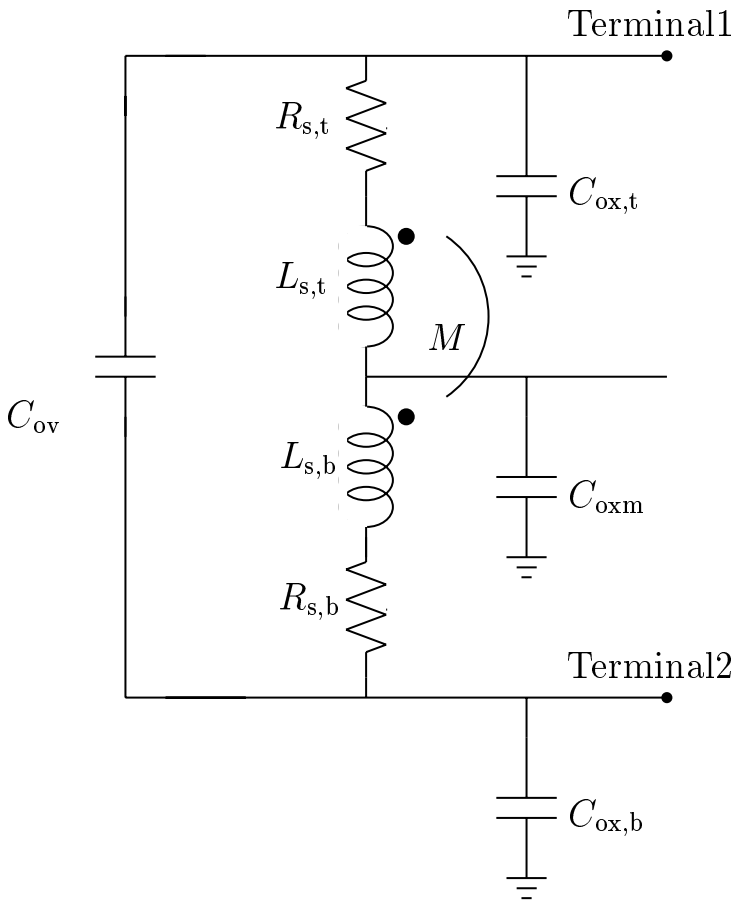


Figure 5.12: Stacked transformer model

Element	Expression
L_{t}	$\frac{2\mu n_{\mathrm{t}}^2 d_{\mathrm{avg,t}}}{\pi}\left[\ln\left(\frac{2.067}{\rho_{\mathrm{t}}}\right)+0.178\rho_{\mathrm{t}}+0.125\rho_{\mathrm{t}}^2\right]$
L_{b}	$\frac{2\mu n_{\mathrm{b}}^2 d_{\mathrm{avg,b}}}{\pi}\left[\ln\left(\frac{2.067}{\rho_{\mathrm{b}}}\right)+0.178\rho_{\mathrm{b}}+0.125\rho_{\mathrm{b}}^2\right]$
k	$0.9-\frac{d_{\mathrm{s}}}{d_{\mathrm{avg}}}$
M	$k\sqrt{L_{\mathrm{t}}L_{\mathrm{b}}}$
$R_{\mathrm{s,t}}$	$\frac{\rho_{\mathrm{t}}\cdot l}{\delta_{\mathrm{t}}\cdot w\cdot\left(1-\mathrm{e}^{-\frac{\mathrm{t_t}}{\delta_{\mathrm{t}}}}\right)}$
$R_{\mathrm{s,b}}$	$\frac{\rho_{\mathrm{b}}\cdot l}{\delta_{\mathrm{b}}\cdot w\cdot\left(1-\mathrm{e}^{-\frac{\mathrm{t_b}}{\delta_{\mathrm{b}}}}\right)}$
C_{ov}	$\frac{1}{2}\frac{\epsilon_{\mathrm{ox}}}{\mathrm{t}_{\mathrm{ox,t-b}}}\cdot l\cdot w\cdot\frac{\mathrm{A_{ov}}}{\mathrm{A}}$
$C_{\mathrm{ox,t}}$	$\frac{1}{2}\frac{\epsilon_{\mathrm{ox}}}{\mathrm{t}_{\mathrm{ox,t}}}\cdot l\cdot w\cdot\frac{\mathrm{A-A_{ov}}}{\mathrm{A}}$
$C_{\mathrm{ox,b}}$	$\frac{1}{2}\frac{\epsilon_{\mathrm{ox}}}{\mathrm{t}_{\mathrm{ox,b}}}\cdot l\cdot w$
C_{oxm}	$C_{\mathrm{ox,t}}+C_{\mathrm{ox,b}}$

Table 5.3: Expressions for elements in the stacked transformer model (ρ=DC metal resistivity, δ=skin depth, $\mathrm{t_{ox,t}}$=oxide thickness from top metal to substrate, $\mathrm{t_{ox,b}}$=oxide thickness from bottom metal to substrate, $\mathrm{t_{ox,t-b}}$=oxide thickness from top level metal to bottom level metal, k=mutual coupling coefficient, n=number of turns, $\mathrm{d_{avg}}$=average diameter, l=length of spiral $\approx 4nd_{\mathrm{avg}}$, w=turn width, t=metal thickness, A=area, $\mathrm{A_{ov}}$=overlapped area of top and bottom spirals, d_{s}=center-to-center spiral distance)

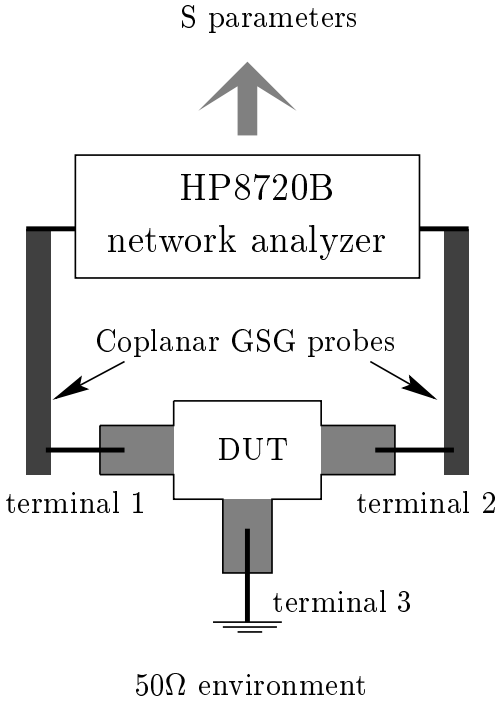


Figure 5.13: Experimental set up for measuring inductance

	x_s (μm)	y_s (μm)	$d_s = \sqrt{{x_s}^2 + {y_s}^2}$	$d_{norm} = (\frac{d_s}{AD})$	$k_{predict} = (0.9 - d_{norm})$	k_{meas}
A	0	0	0	0	0.9	0.88
B	8	8	11	0.09	0.81	0.79
C	42	0	42	0.35	0.55	0.57
D	57	0	57	0.48	0.42	0.45
E	50	50	71	0.59	0.31	0.28

Table 5.4: Comparison of transformer realizations.

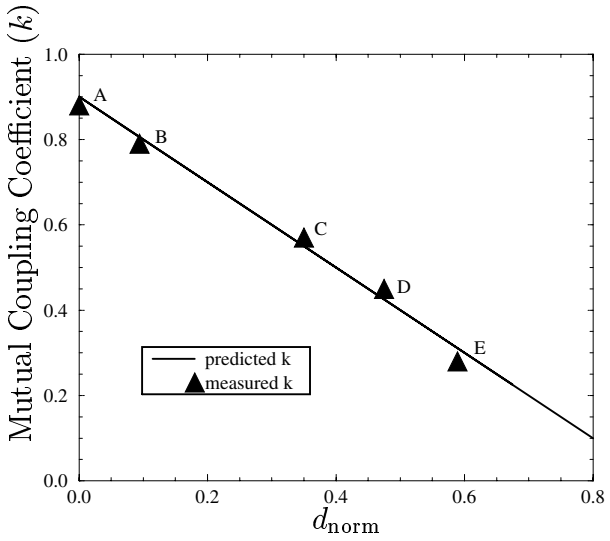


Figure 5.14: Coupling coefficient (k) versus normalized shift (d_{norm})

shifts. The stacked transformers are fabricated on the third and second layers of a triple-metal 0.5μm CMOS epi-process with the patterned ground shields (PGS) being implemented on the polysilicon layer. Each spiral has the following lateral dimensions: $d_{\mathrm{out}} = 180\mu$m, $w = 3.2\mu$m, $s = 2.1\mu$m and $n = 11.75$. Figure 5.14 plots the coupling coefficient as a function of shift. Good agreement between measured and modeled values of k is observed.

5.6.2 Verification of Transformer Models

The measured S parameters of the device under test (DUT) are compared to the S parameters predicted by our analytical model by the following procedure:

1. DUT : S-to-Y ($\mathrm{Y_{DUT}}$)

2. Open calibration: S-to-Y ($\mathrm{Y_O}$)

3. $\mathrm{Y_{Cor}} = \mathrm{Y_{DUT}} - \mathrm{Y_O}$

4. Y_{Cor} to S_{meas}

5. Compare S_{meas} to S_{calc}

The predictions of the analytical models were compared with measurements for a variety of transformers.

Figure 5.15 compares the real and imaginary components of the measured S parameters to those predicted by the analytical model for a tapped transformer. This transformer was fabricated on a quartz substrate, and was designed to have $L_o = 3$nH, $L_i = 2$nH and $k = 0.35$. The figure shows very good agreement between simulated and measured results.

Fig. 5.16- 5.18 show good agreement for stacked transformers (L_t=20nH, L_b=20nH) with various shifts (k=0.9, k=0.55, k=0.3). The stacked transformers are fabricated on the third and second layers of a triple-metal 0.5μm CMOS epi-process with the patterned ground shields (PGS) being implemented on the polysilicon layer. These transformers correspond to the entries labeled A, C and E in table 5.4. Figure 5.16 compares the real and imaginary components of the measured S parameters to those predicted by the analytical model for a stacked transformer with maximum overlap (entry A). Figure 5.17 compares the same for a stacked transformer with top and bottom spirals laterally shifted (entry C), while figure 5.18 compares a stacked transformer with top and bottom spirals diagonally shifted (entry E). In every case, good agreement is obtained between measurements and predictions of the model.

5.7 Summary

This chapter has explored how on-chip transformers may be modeled by lumped circuit models whose elements have analytical expressions. The predictions of these models compare well with measurement results.

- Tapped transformer on quartz substrate
- $d_{\mathrm{out,o}} = 290\mu\mathrm{m}$, $n_{\mathrm{o}} = 2.5$
- $d_{\mathrm{out,i}} = 190\mu\mathrm{m}$, $n_{\mathrm{i}} = 4.25$
- $w = 13\mu\mathrm{m}$, $s = 7\mu\mathrm{m}$

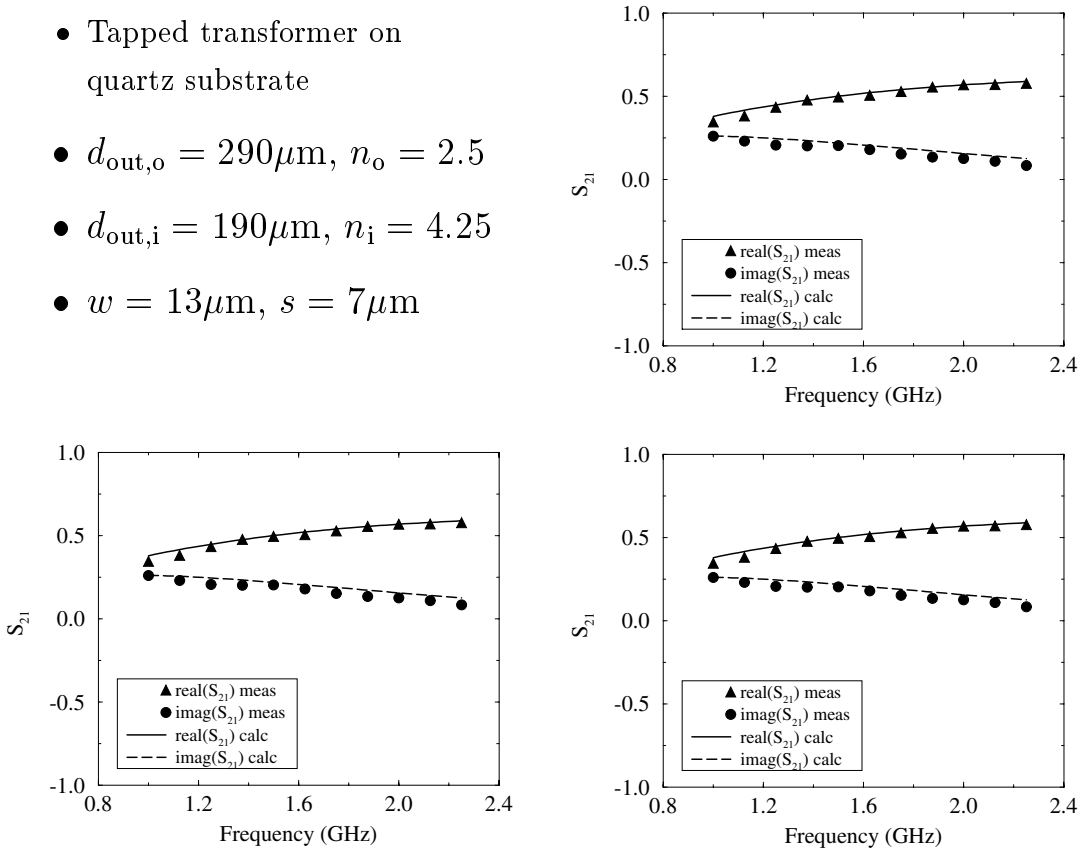


Figure 5.15: Comparison of predicted and measured S parameters for a tapped transformer

- Stacked transformer with top spiral overlapping bottom one
- $d_{\text{out}} = 180\mu\text{m}$, $n = 11.75$, $w = 3.2\mu\text{m}$, $s = 2.1\mu\text{m}$
- $x_{\text{s}} = 0\mu\text{m}$, $y_{\text{s}} = 0\mu\text{m}$, $d_{\text{s}} = 0\mu\text{m}$

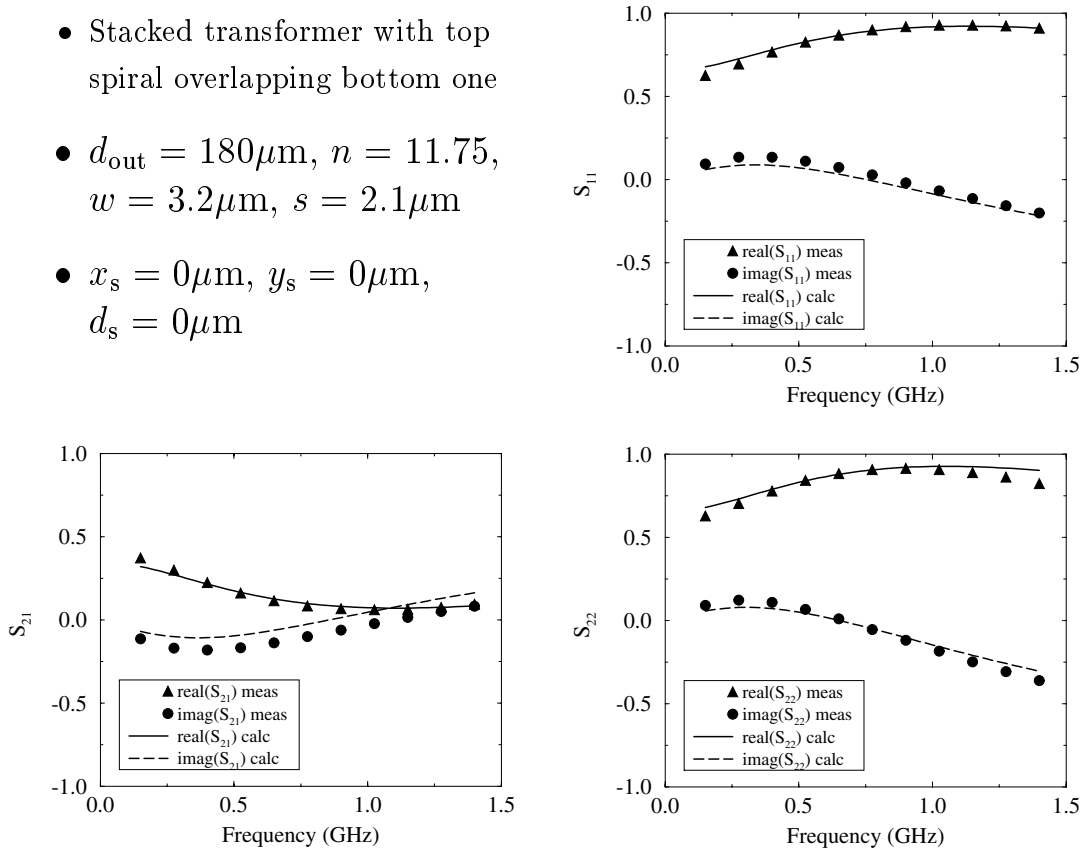


Figure 5.16: Comparison of predicted and measured S parameters for stacked transformer with top spiral overlapping bottom one

- Stacked transformer with top and bottom spirals laterally shifted
- $d_{\text{out}} = 180\mu\text{m}$, $n = 11.75$, $w = 3.2\mu\text{m}$, $s = 2.1\mu\text{m}$
- $x_{\text{s}} = 42\mu\text{m}$, $y_{\text{s}} = 0\mu\text{m}$, $d_{\text{s}} = 42\mu\text{m}$

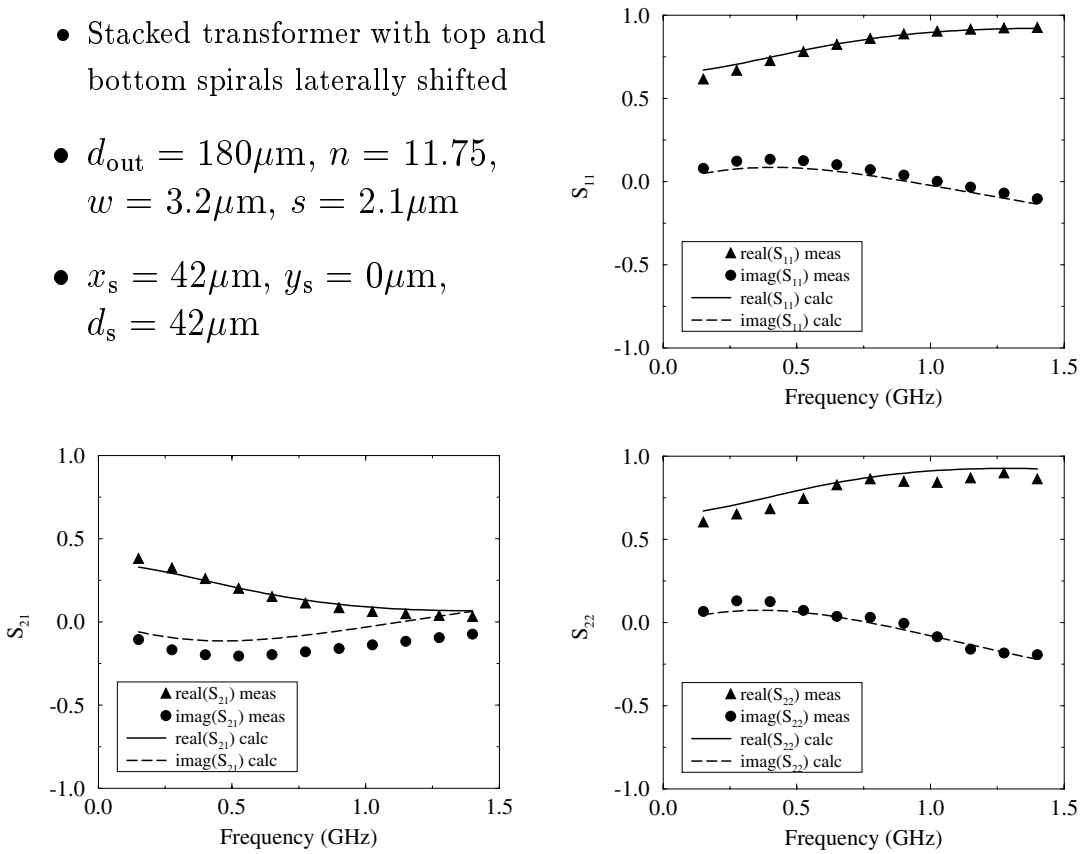


Figure 5.17: Comparison of predicted and measured S parameters for stacked transformer with top and bottom spirals laterally shifted

- Stacked transformer with top and bottom spirals diagonally shifted
- $d_{\text{out}} = 180\mu\text{m}$, $n = 11.75$, $w = 3.2\mu\text{m}$, $s = 2.1\mu\text{m}$
- $x_{\text{s}} = 50\mu\text{m}$, $y_{\text{s}} = 50\mu\text{m}$, $d_{\text{s}} = 71\mu\text{m}$

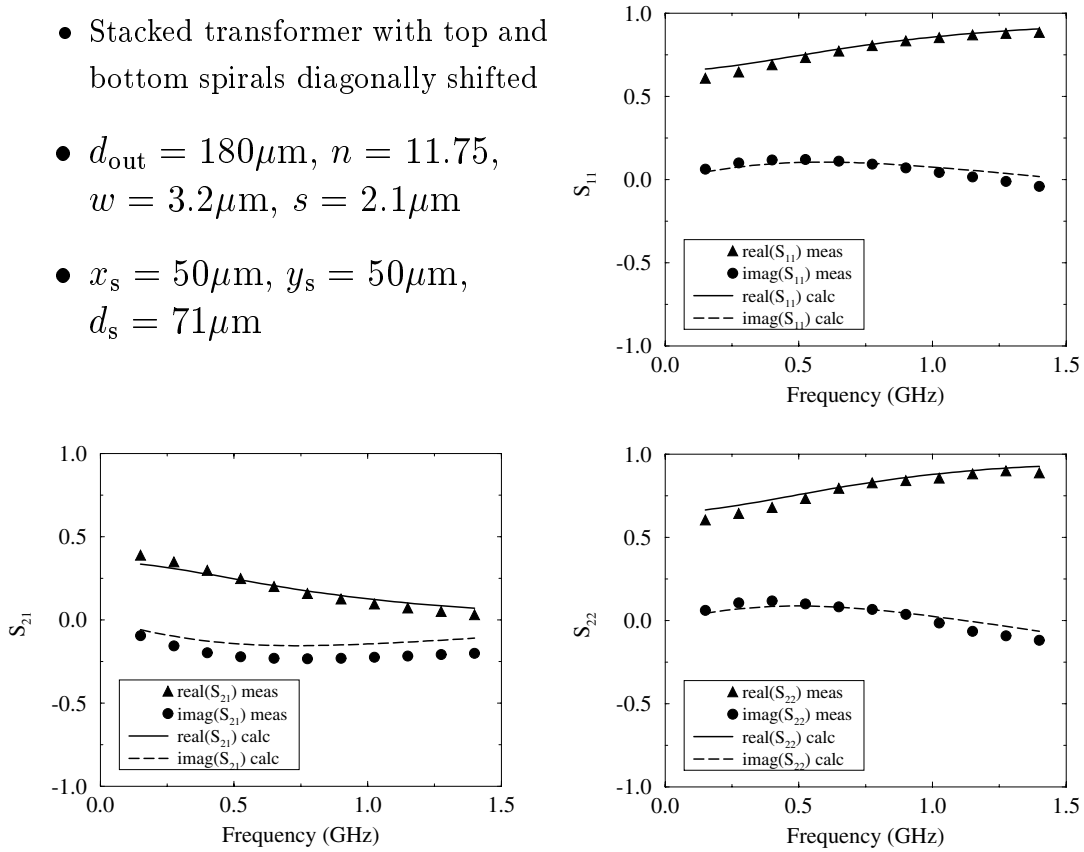


Figure 5.18: Comparison of predicted and measured S parameters for stacked transformer with top and bottom spirals diagonally shifted

Chapter 6

Design and Optimization of Inductor Circuits

This chapter discusses the design and optimization of inductor circuits. Section 6.1 introduces common performance measures used to characterize on-chip inductors. Particular attention is paid to various quality factor definitions and the conditions under which a particular definition is relevant. Section 6.2 compares the optimum performance achieved by square, hexagonal, octagonal and circular inductors. Section 6.3 explores how inductors can enhance the bandwidth of broadband circuits and presents a design methodology for optimizing on-chip inductors for such applications. Section 6.4 introduces *geometric programming* as a means of globally optimizing inductor circuits quickly and efficiently.

6.1 Parameters of Interest

This section describes the common performance parameters used to evaluate on-chip inductors. Analytical expressions for these parameters can be obtained using the elements of the lumped circuit model described in chapter 2. However, these expressions vary, depending on whether the inductor is used in a one terminal or two terminal configuration and on whether a patterned ground shield (PGS) is placed beneath the

inductor to eliminate the resistive and capacitive coupling to the substrate. This section provides expressions for the performance parameters of an inductor with PGS in a one terminal configuration. This configuration was chosen as most RF circuit blocks (such as low noise amplifiers and oscillators) use inductors as one terminal devices, with the second terminal connected to a node that is at incremental ground. Figure 6.1 shows the equivalent lumped circuit for this configuration.

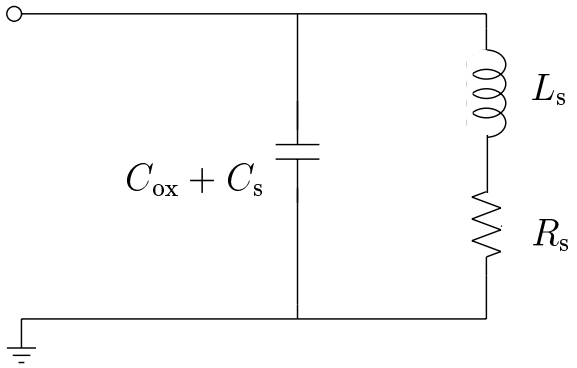


Figure 6.1: Lumped model for one terminal configuration with PGS.

The most commonly quoted performance parameter is the quality factor, Q. The definition of Q depends on the application. For most narrowband applications, it is sufficient to define the inductor quality factor, Q_L, and the tank quality factor, Q_{tank}.

- **Inductor quality factor** (Q_L) is defined as:

$$Q_L(\omega) = 2\pi \frac{[\text{peak magnetic energy} - \text{peak electric energy}]}{\text{energy loss in one oscillation cycle}}. \qquad (6.1)$$

An equivalent definition for Q_L is:

$$Q_L(\omega) = \frac{[\text{Imaginary component of impedance.}]}{\text{Real component of impedance}}. \qquad (6.2)$$

For the one-terminal inductor shown in figure 6.1, the inductor quality factor is given by:

$$Q_{\mathrm{L}}(\omega) = \frac{\omega L_{\mathrm{s}}}{R_{\mathrm{s}}(\omega)} \left[1 - \frac{R_{\mathrm{s}}^2(\omega)(C_{\mathrm{ox}} + C_{\mathrm{s}})}{L_{\mathrm{s}}} - \omega^2 L_{\mathrm{s}}(C_{\mathrm{ox}} + C_{\mathrm{s}}) \right] \tag{6.3}$$

Q_{L} is used in applications where the inductor's parasitic resistances as well as capacitances degrade the circuit performance. An example where Q_{L} is relevant is when an inductor is used as the source degeneration element in narrowband low-noise amplifiers [35, 2, 36]. Q_{L} is also pertinent in some filter applications.

- **Tank quality factor** (Q_{tank}) is defined as:

$$Q_{\mathrm{tank}}(\omega) = 2\pi \frac{\text{peak magnetic energy}}{\text{energy loss in one oscillation cycle}} \tag{6.4}$$

For the one-terminal inductor shown in figure 6.1, the tank quality factor is given by:

$$Q_{\mathrm{tank}}(\omega) = \frac{\omega L_{\mathrm{s}}}{R_{\mathrm{s}}(\omega)} \tag{6.5}$$

This definition is appropriate when only the inductor's parasitic resistances degrade the overall circuit performance. In such cases, the parasitic capacitance of the inductor is incorporated as part of the resonance network. This definition applies in every case where the on-chip inductor is used as part of a resonant tank circuit (hence the term Q_{tank}). The best examples of such circuits are resonators and oscillators where the resonance tank occurs at the drain of MOSFET (or equivalently, the collector of a BJT) [37, 2, 37, 4].

- **Self-resonant frequency** (ω_{res}) is defined the frequency at which $Q_{\text{L}} = 0$. Beyond this frequency, the inductor exhibits a negative reactance thereby rendering it useless as an inductive tuning element. In most on-chip spiral inductors, Q_{L} reaches a maximum at around half the self-resonant frequency. On the other hand, Q_{tank} typically reaches a maximum close to ω_{res}.

6.2 Comparison of Inductor Geometries

This section compares the optimum one terminal Q_{L} achieved using square, hexagonal, octagonal and circular spirals for a fixed inductance at a given frequency. Note that degradation due to magnetic coupling to the substrate is not considered in this treatment. This issue is discussed in 7.

6.2.1 Example: Maximum Q_{L} @ 2GHz for $L = 8$nH

Figure 6.2 compares the maximum Q_{L} achieved at 2GHz by the various spiral geometries for a 8nH inductor. The same process parameters are used for all the polygonal spirals so that the vertical parameters of the spiral are held constant. The lateral geometrical parameters (w, s, n and d_{out}) are optimized to yield a fixed series inductance, L of 8nH with maximum Q_{L} at 2GHz.

Table 6.2.1 summarizes the outer diameter and area of the optimum spirals. For polygons with more than four sides, the inductor area is less than the effective chip area. The effective chip area is defined as the area of the smallest square within which the polygonal spiral may be inscribed. For example, for a circular spiral with an outer diamter of d_{out}, the inductor area is $0.25\pi d_{\text{out}}^2$ whereas the effective chip area is d_{out}^2. In general, the effective chip area is the more relevant metric as it is a measure of how much area is dedicated on-chip to a spiral inductor. For example, if one considers an octagonal spiral, the difference between its inductor area and its effective area is the sum of the four triangular areas which lie outside its four sides that are at an angle of $pi/4$ radians to the sides of the square within which the spiral is inscribed. In most circuit layouts, these four triangular areas are not used for any

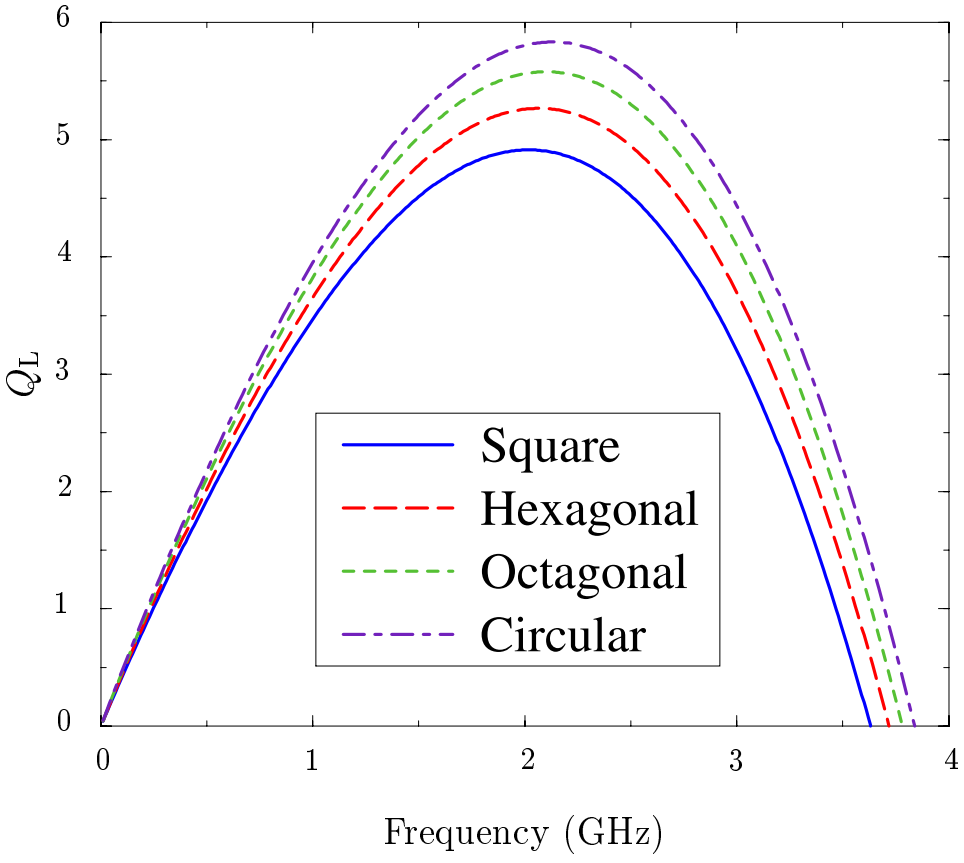


Figure 6.2: Comparison of maximum Q_L @ 2GHz for $L = 8$nH

other purpose and therefore must be included in the area dedicated to the spiral. Thus, the effective chip area is best defined as the smallest square area within which a given spiral fits.

Layout	Outer diameter (μm)	Inductor area mm^2	Effective chip area mm^2
Square	287	0.082	0.082
Hexagonal	308	0.082	0.095
Octagonal	309	0.079	0.095
Circular	314	0.077	0.099

Table 6.1: Outer diameter and area of inductors with maximum Q_{L} @ 2GHz for $L = 8$nH

Using the effective area as a reference, it is clear that the square spiral is most area efficient whereas the circular spiral is least area efficient. However, the circular spiral achieves the best Q_{L}. In general, circular spirals consume around 20% more chip area than square spirals and achieve Q_{L} values that are $\approx 15 - 20\%$ better.

As expected, the performance of hexagonal and octagonal geometries is between that of square and circular ones. The plot suggests that an octagonal spiral achieves Q_{L} values that are within $\approx 3 - 5\%$ of that of a circular one with a corresponding $\approx 3 - 5\%$ reduction in the effective chip area. This suggests that polygons with more than eight sides are not needed for most applications, thereby minimizing the layout complexity.

6.2.2 Example: Maximum Q_{L} @ 3GHz for $L = 5$nH

Figure 6.3 compares the maximum Q_{L} achieved at 2GHz by the various spiral geometries for a 8nH inductor. Table 6.2 summarizes the outer diameter and area of the optimum spirals. Once again, Q_{L} and the effective chip area increase with the number of sides of the spiral. There is a striking resemblance between the performance comparison of the previous example and this one. Since the frequency

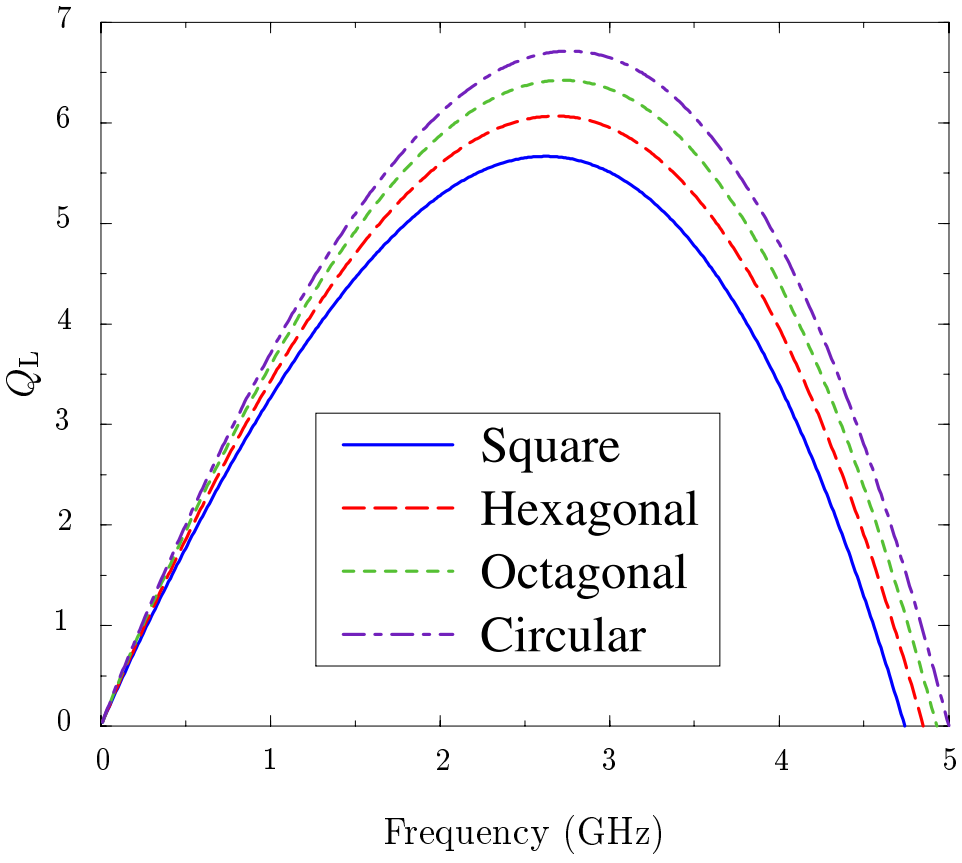


Figure 6.3: Comparison of maximum Q_L @ 3GHz for $L = 5$nH

Layout	Outer diameter (μm)	Inductor area mm^2	Effective chip area mm^2
Square	288	0.083	0.083
Hexagonal	309	0.083	0.095
Octagonal	310	0.080	0.096
Circular	315	0.078	0.099

Table 6.2: Outer diameter and area of inductors with maximum Q_{L} @ 3GHz for $L = 5$nH

is higher and the specified inductance lower, the optimal Q_{L} is higher for a given geometry when compared to the previous example.

6.2.3 Maximum Q_{L} for $L = 5$nH with $d_{\mathrm{out}} = 300\mu$m

Figure 6.4 compares the maximum Q_{L} achieved at the various spiral geometries for a 5nH subject to the constraint that the maximum outer diamter be 300μm. Table 6.3 summarizes the dimensions of the optimum spirals. The addition of the

Layout	d_{out} (μm)	d_{avg} (μm)	w (μm)	s (μm)	n n	ρ ρ
Square	300	229	17.6	2	3.75	0.31
Hexagonal	300	229	16.2	2	4.00	0.31
Octagonal	300	230	16.1	2	4.00	0.31
Circular	300	232	15.5	2	4.00	0.29

Table 6.3: Dimensions of inductors with maximum Q_{L} for $L = 5$nH with $d_{\mathrm{out}} = 300\mu$m

area constraint permits us to compare the maximum Q_{L} achievable by the various geometries for a fixed effective chip area. Now, the Q_{L} of the circular spiral is larger than the square spiral by $\approx 10\%$ at the (fixed) frequency of interest. Note however, that the circular spiral reaches its maximum Q_{L} at a higher frequency than

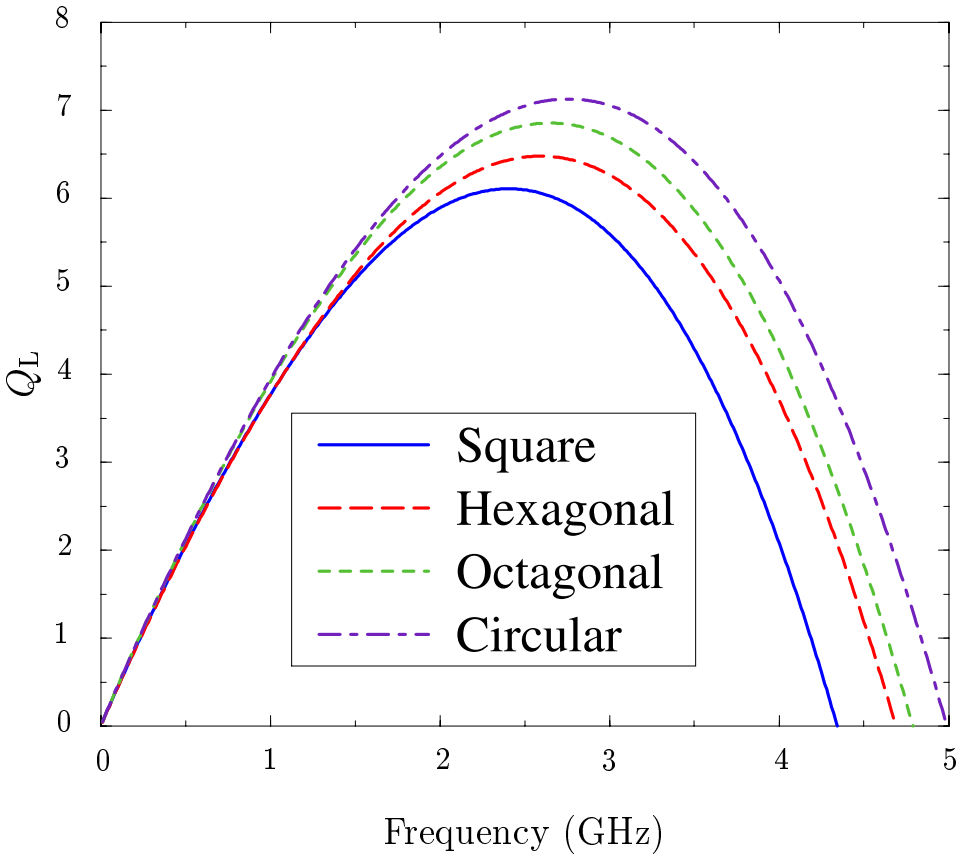


Figure 6.4: Comparison of maximum Q_L for $L = 5$nH with $d_{out} = 300\mu$m

the square one. This observation is consistent with the results of the previous two examples.

6.3 Bandwidth Extension in Broadband Circuits

Although inductors are commonly associated with narrowband circuits, they are useful in broadband circuits as well. In this section we examine how an inductor can be used to enhance the bandwidth of a simple amplifier. We then study how an on-chip inductor can be designed to optimize the performance of this broadband amplifier.

6.3.1 Shunt-peaked Amplification

We illustrate the use of inductors for extending the bandwidth of broadband circuits by considering the simple common source amplifier illustrated in figure 6.5(a). For simplicity, we assume that the small signal frequency response of this amplifier is dominated by the output pole whose value is determined solely by load resistance, R, and the load capacitance, C (figure 6.5(b)):

$$\frac{v_{\text{out}}}{v_{\text{in}}}(\omega) = \frac{g_{\text{m}}R}{1 + j\omega RC}. \tag{6.6}$$

The introduction of an inductance, L, in series with the load resistance alters the frequency response of the amplifier (figure 6.5(c)). This technique, called shunt-peaking, enhances the bandwidth of the amplifier by transforming the frequency response from that of a single pole to one with two poles and a zero (figure 6.5(d))):

$$\frac{v_{\text{out}}}{v_{\text{in}}}(\omega) = \frac{g_{\text{m}}(R + j\omega L)}{1 + j\omega RC - \omega^2 LC} \tag{6.7}$$

The poles may or may not be complex (although, they are complex for practical cases of bandwidth extension). The zero is determined solely by the L/R time constant, and is primarily responsible for the bandwidth enhancement.

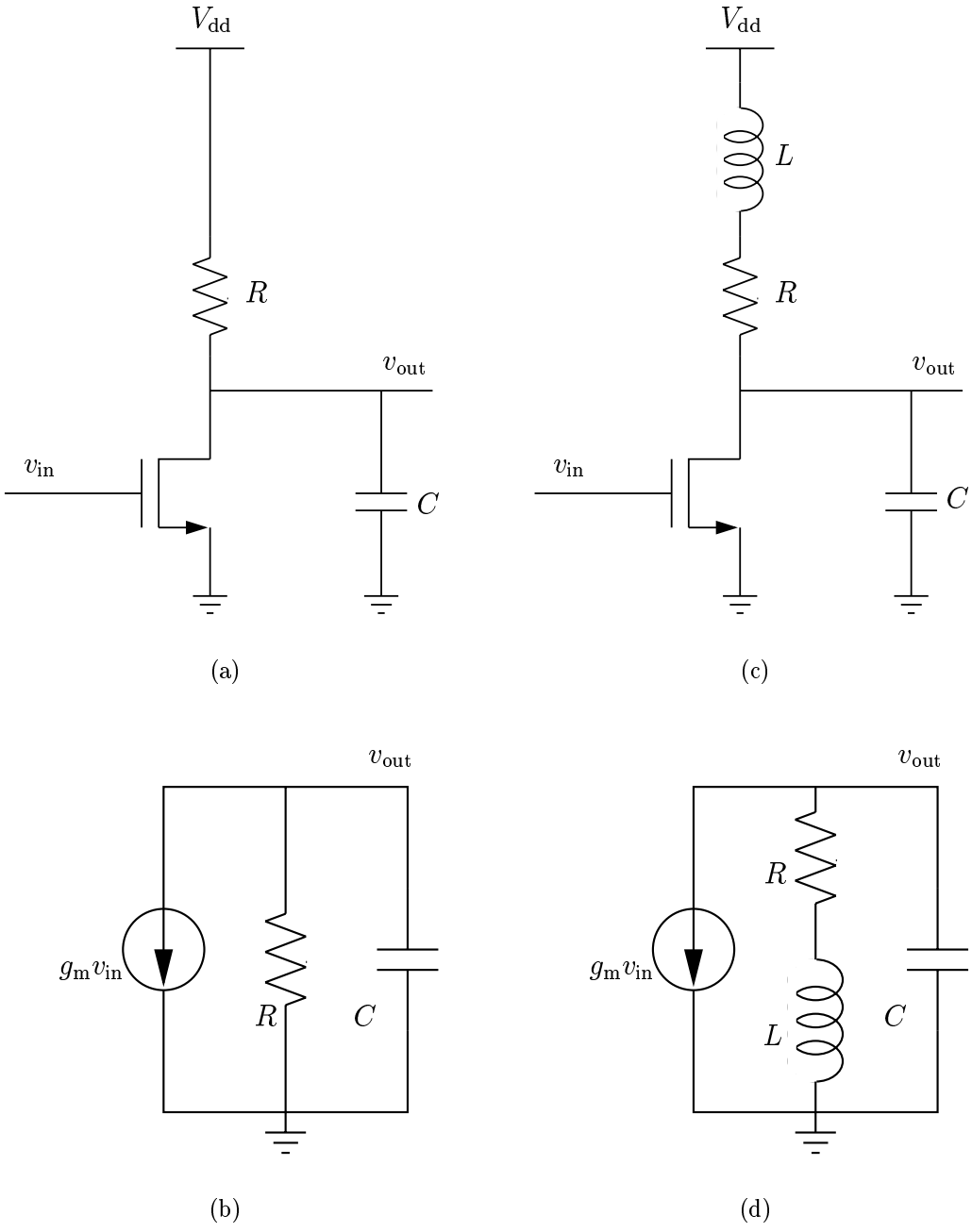


Figure 6.5: Shunt-peaking in a common source amplifier. (a) Simple common source amplifier, and (b) its equivalent small signal model. (c) Common source amplifier with shunt peaking and (d) its equivalent small signal model.

Factor (m)	**Normalized** ω_{3dB}	**Response**
0	1.00	No shunt peaking
0.32	1.60	Optimum group delay
0.41	1.72	Maximally flat
0.71	1.85	Maximum bandwidth

Table 6.4: Benchmarks for shunt peaking

The frequency response of the shunt peaked amplifier is characterized by the ratio of the L/R and RC time constants. This ratio is denoted by m where $L = mR^2C$. Figure 6.6 illustrates the frequency response of the shunt peaked amplifier for various values of m. The frequency and magnitude axes have been normalized so that the low frequency gain is unity and so that the 3dB bandwidth for the case with no shunt peaking ($m = 0$) is unity ($RC = 1$). The frequency response is plotted for the values of m listed in table 6.4 [34]. As expected, the 3dB bandwidth increases as m increases. The maximum bandwidth is obtained when $m = 0.71$ and yields an 85% improvement in bandwidth. However, as can be clearly seen in the magnitude plot, this comes at the cost of significant gain peaking. A maximally flat response may be obtained for $m = 0.41$ with a still impressive bandwidth improvement of 72%.

Another interesting case occurs when $m = 0.32$. As seen in the phase plot, this best approximates a linear phase response up to the 3dB bandwidth, which is 60% higher than the case without shunt peaking. This case is called the 'optimum group delay case' and is desirable for optimizing pulse fidelity in broadband systems that transmit digital signals.

The next section will explore how on-chip inductors can be optimized for use in shunt-peaked amplifiers.

6.3.2 On-Chip Shunt-Peaking

The non-idealities of on-chip inductors present several challenges for implementing shunt-peaked amplifiers on-chip. The biggest issue is the reduction in bandwidth

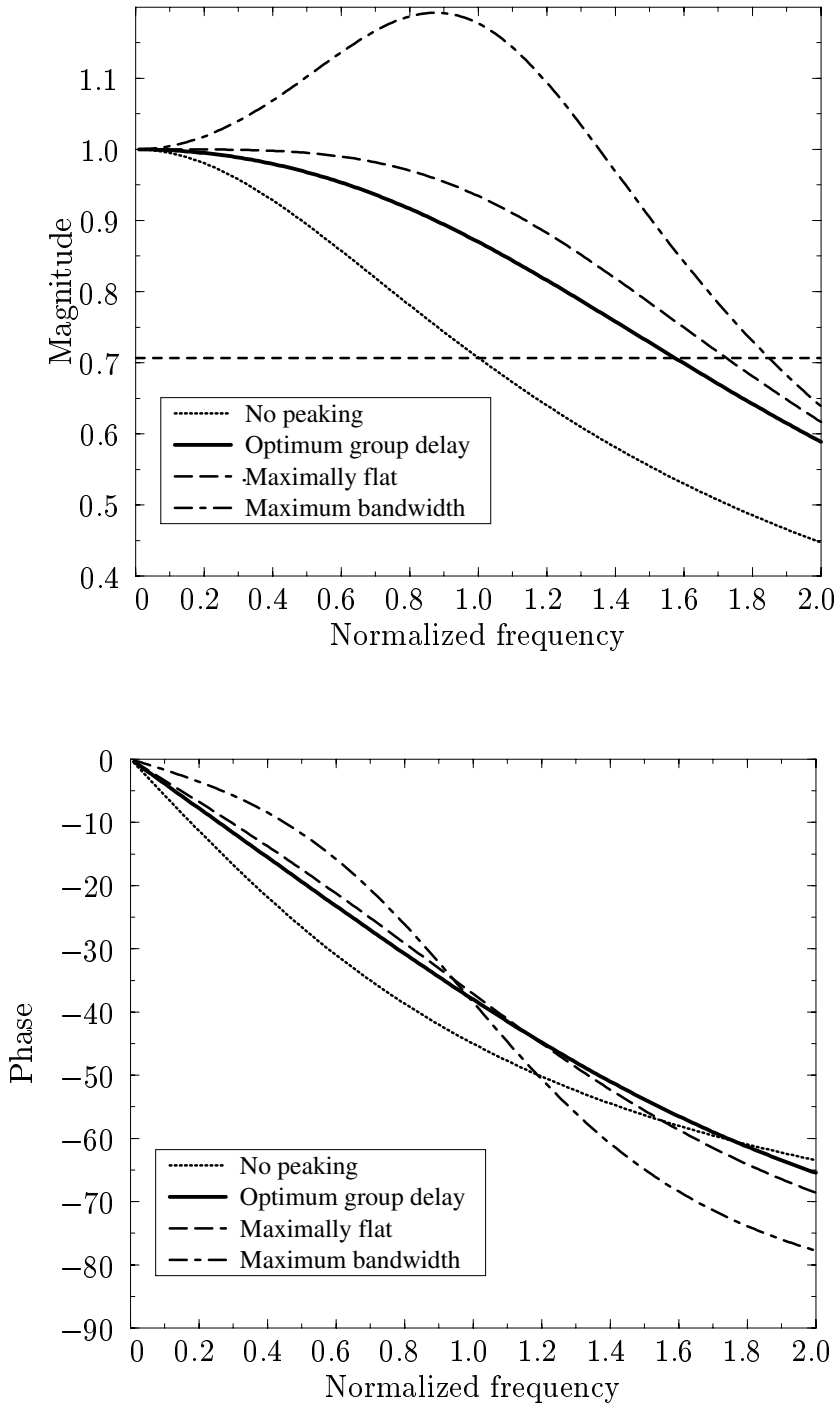


Figure 6.6: Frequency response of shunt-peaked cases tabulated in table 6.4.

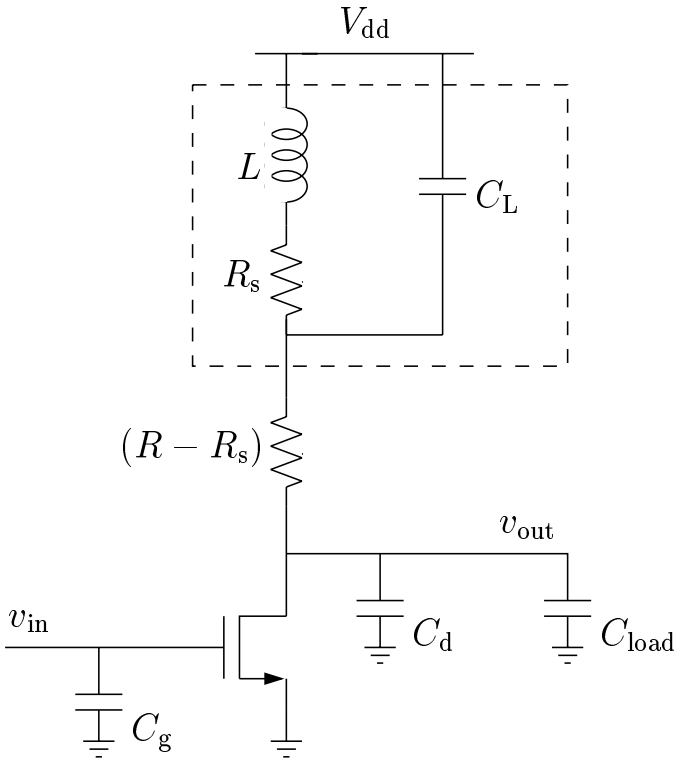


Figure 6.7: Shunt-peaking with optimized on-chip inductor

improvement because of the additional parasitic capacitance introduced by the inductor. Figure 6.7 illustrates how this capacitance can be minimized by paritioning the total load resistance, R, between the inductor's series resistance (R_s) and the external resistance, which now takes on the value of $(R - R_s)$. Since the series resistance is now part of the load resistance, the quality factor of the inductor is largely irrelevant and therefore the inductor's turn width, w, can be made small to permit the desired inductance to be realized while minimizing the spiral area and capacitance. In this case, the minimum w is determined in part by current density limitations as the transistor current also flows through the inductor. The minimum turn spacing, s, is usually set by lithography limitations.

The desired inductance is now a function of both the transistor's and inductor's parasitics as well as the load capacitance and external resistance. Thus the optimization of on-chip shunt-peaking requires the simultaneous optimization of passive and active components. This scenario accentuates the limitations of using a field solver for modeling the inductor. Even if the field solver contains a general purpose optimization routine, it serves no use as the performance parameters of the inductor alone (such as Q_L) cannot specify the optimization goal. Therefore, several iterations would be needed (each requiring an interface between the field solver and the circuit simulator), before an acceptable design could be obtained.

On the other hand, a lumped circuit model (with analytical expressions for all the elements in terms of the spiral's geometrical parameters and process parameters) can be easily incorporated into a circuit simulator and thereby provide a way for the designer to optimize the entire circuit. Thus the inductance expressions discussed in chapter 4 serve as a valuable design tool when combined with the lumped circuit model described in chapter 2.

The use of on-chip shunt peaking is attractive for a variety of broadband applications as it gives better performance with no additional power dissipation. Appendix C illustrates how optimized on-chip spiral inductors can be used as shunt-peaking elements to increase the transimpedance of a preamplifier intended as the front-end of a gigabit optical receiver.

6.4 Optimization via Geometric Programming

Although the availability of simple inductance expressions and lumped models allows engineers to design and optimize inductor circuits in a circuit environment such as *SPICE*, this process can be time consuming. The main reason is that CAD tools built around circuit solvers employ general purpose optimization tools that are slow. Furthermore, these tools can usually identify only local optima. Typically, most designers do variable sweeps over multiple dimensions (guided by prior design knowledge and insight) to arrive at an acceptable design. In such cases, the number of iterations increases exponentially with the number of variables. Considering that a planar spiral inductor has four geometrical parameters, it is clear that the simultaneous optimization of active and passive components can only be carried out for circuits with a couple of transistors and inductors.

This section introduces an efficient method for the optimal design and synthesis of RF CMOS inductor circuits. The method is based on *geometric programming*. This method is attractive as it quickly generates a design that is globally optimal for a given set of specifications and constraints. Moreover, when no solution exists for a problem, this method unambiguously declares infeasibility.

6.4.1 Geometric Programming

Let f be a real-valued function of n real, positive variables $x_1, x_2, \ldots, x_n$. It is called a *posynomial* function if it has the form

$$f(x_1, \ldots, x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}}$$

where $c_j \geq 0$ and $\alpha_{ij} \in \mathbf{R}$. When $t = 1$, f is called a *monomial* function. Thus, for example, $0.7 + 2x_1/x_3^2 + x_2^{0.3}$ is posynomial and $2.3(x_1/x_2)^{1.5}$ is a monomial. Posynomials are closed under sums, products, and nonnegative scaling.

A *geometric program* (GP)) has the form

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \leq 1, \quad i = 1, 2, \ldots, m, \\ & g_i(x) = 1, \quad i = 1, 2, \ldots, p, \\ & x_i > 0, \quad i = 1, 2, \ldots, n, \end{array} \tag{6.8}$$

where f_i are posynomial functions and g_i are monomial functions. If f is a posynomial and g is a monomial, then the constraint $f(x) \leq g(x)$ can be expressed as $f(x)/g(x) \leq 1$ (since f/g is posynomial). From closure under non-negativity, constraints of the form $f(x) \leq a$, where $a > 0$ can also be used. Similarly, if g_1 and g_2 are both monomial functions, the constraint $g_1(x) = g_2(x)$ can be expressed as $g_1(x)/g_2(x) = 1$ (since g_1/g_2 is monomial).

The key to solving GPs is a change of variables that converts the posynomial objective and constraint functions into *convex* functions of the new variables. We define new variables $y_i = \log x_i$, and take the logarithm of a posynomial f to get

$$h(y) = \log\left(f\left(e^{y_1}, \ldots, e^{y_n}\right)\right) = \log\left(\sum_k^t e^{a_k^T y + b_k}\right)$$

where $a_k^T = [\alpha_{1k} \cdots \alpha_{nk}]$ and $b_k = \log c_k$. It can be shown that h is a *convex* function of y. This transformation converts the standard geometric program (6.8) into the convex optimization program:

$$\begin{array}{ll} \text{minimize} & \log f_0(e^{y_1}, \ldots, e^{y_n}) \\ \text{subject to} & \log f_i(e^{y_1}, \ldots, e^{y_n}) \leq 0, \quad i = 1, \ldots, m \\ & \log g_i(e^{y_1}, \ldots, e^{y_n}) = 0, \quad i = 1, \ldots, p, \end{array} \tag{6.9}$$

which is called the *convex form* of the geometric program. Even though this problem is highly nonlinear, it can be solved globally and very efficiently by recently developed interior-point methods [39].

For our purposes, the most important feature of geometric programs is that they can be *globally* solved with great efficiency. Such solution algorithms also determine

whether the problem is infeasible. Also, the starting point for the optimization algorithm does not have any effect on the final solution; indeed, an initial starting point or design is completely unnecessary.

Many circuit problems may be posed as geometric programs [28, 40]. In particular, the design specifications of inductor circuits can be formulated in a way suitable for geometric programming [41, 42]. The application of geometric programming in analog circuit design is discussed in detail in the Ph.D. thesis of Maria del Mar Hershenson [40].

6.5 Summary

This chapter described how inductors can be optimally designed for use in inductor circuits. Section 6.1 introduces common performance measures used to characterize on-chip inductors. Various quality factor definitions were presented and the appropriate conditions for their use was identified. The optimum performance achieved by square, hexagonal, octagonal and circular inductors were compared. Techniques for extending the bandwidth of broadband circuits using inductors as shunt-peaking elements were presented. Particular attention was paid to the optimization of on-chip inductors used for shunt-peaking. Finally, a new and efficient method for optimizing inductors, based on *geometric programming* was introduced.

Chapter 7

Magnetic Coupling from Spiral to Substrate

The performance of an on-chip spiral inductor is degraded by resistive, capacitive and inductive coupling to a conductive substrate. The resistive and capacitive coupling mechanisms have been well understood and modeled as discussed in chapter 2. Furthermore, the patterned ground shield (PGS) can be used to eliminate these effects. On the other hand, the magnetic coupling to the substrate has not been well understood. Although this mechanism is known to limit the performance of inductors built on the high conductivity substrate processes typical of modern CMOS, no simple models exist to provide design guidance.

In this chapter, we will study how magnetic coupling from an on-chip spiral to the silicon substrate affects the performance of an inductor. Section 7.1 develops a current sheet based approach for modeling the magnetic coupling to the substrate. This model provides valuable design insight and quantifies the degradation in inductor performance as a function of frequency, substrate conductivity, and the spiral and process parameters. The predictions of this model agree well with experimental results as demonstrated in section 7.2.

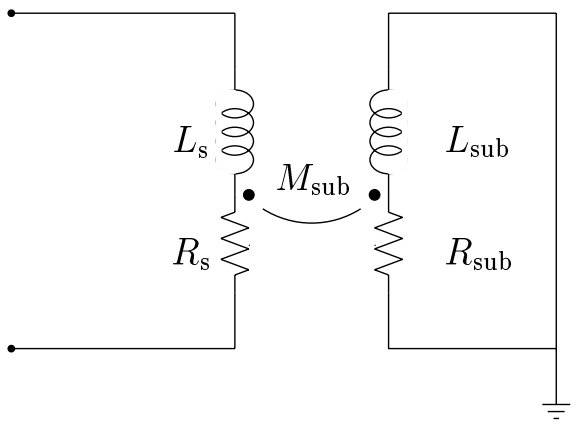


Figure 7.1: Circuit model of inductor with substrate magnetic coupling

7.1 Modeling of Substrate Magnetic Coupling

The effect of substrate magnetic coupling on an inductor is modeled with a transformer as indicated in Figure 7.1. R_s and L_s are the series resistance and inductance of the spiral inductor, M_{sub} is the mutual inductance between the spiral and substrate, and R_{sub} and L_{sub} are the substrate resistance and inductance associated with eddy current flow. Thus, the equivalent impedance between the two ports of the inductance is $Z(\omega)$ where

$$Z(\omega) = R_s + j\omega L_s + \left(\frac{\omega^2 M_{sub}^2}{R_{sub} + j\omega L_{sub}} \right). \tag{7.1}$$

The substrate coupling is therefore reflected at the terminals of the inductor as an increase in the series resistance and a decrease in the inductance, both of which degrade performance. Figure 7.1 shows the equivalent one-port model. The effective resistance, R_{eff}, and effective inductance, L_{eff}, are:

$$R_{eff} = R_s + R_{sub} \left(\frac{\omega^2 M_{sub}^2}{R_{sub}^2 + \omega^2 L_{sub}^2} \right) \tag{7.2}$$

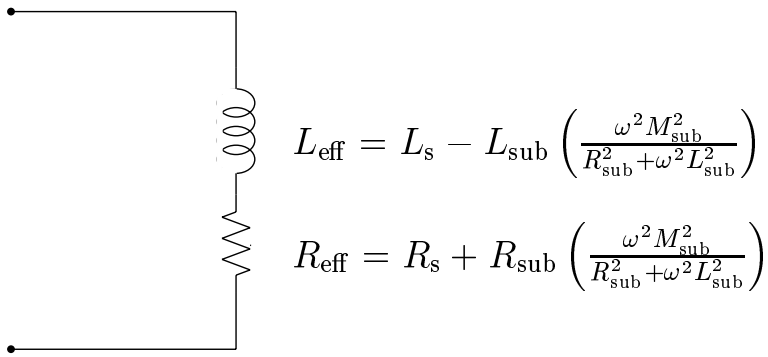


Figure 7.2: Equivalent circuit model

$$L_{\text{eff}} = L_{\text{s}} - L_{\text{sub}} \left(\frac{\omega^2 M_{\text{sub}}^2}{R_{\text{sub}}^2 + \omega^2 L_{\text{sub}}^2} \right) \tag{7.3}$$

Thus, magnetic coupling to the substrate reduces the inductance and increases the series resistance.

7.1.1 Simplifying Approximations

Clearly, a small M_{sub}, large R_{sub} and large L_{sub} are desired to minimize the adverse effects of magnetic coupling to the substrate. Unfortunately, the distributed, three dimensional nature of the substrate makes it difficult to accurately model M_{sub}, R_{sub} and L_{sub}. This difficulty is exacerbated by the fact that the substrate conductivity can change by a factor of 2-3 or more from process variations and with depth. Furthermore, temperature variations can change the substrate conductivity by almost an order of magnitude. This section first presents a qualitative overview of the variables and then simplifies the problem by using approximations that are valid for current silicon substrates.

As one may expect, M_{sub} and R_{sub} are dependent on the skin depth of the substrate as well as the parameters of the spiral. The toughest parameter to model is L_{sub}. Since the maximum substrate conductivity is $\approx 10^4 \text{Sm}^{-1}$, and therefore three orders of magnitude smaller than that of metals, it is safe to assume that

the resistive term (R_{sub}) associated with the eddy currents completely dominates the corresponding inductive term (L_{sub}) for frequencies up to 10GHz. Since these terms are in series, the denominator of equation 7.1 may be approximated by $R_{\text{sub}} + j\omega L_{\text{sub}} \approx R_{\text{sub}}$, yielding simpler expressions for the elements in figure 7.2:

$$R_{\text{eff}} \approx R_{\text{s}} + \left(\frac{\omega^2 M_{\text{sub}}^2}{R_{\text{sub}}} \right) \tag{7.4}$$

$$L_{\text{eff}} \approx L_{\text{s}} \tag{7.5}$$

Thus the primary effect of magnetic substrate coupling is an increase in the series resistance. The following sections develop approximate expressions for M_{sub} and R_{sub} permitting R_{eff} to be quantified.

7.1.2 Effective Substrate Skin Depth

The skin depth of the substrate, δ_{sub}, decreases as the frequency and substrate conductivity increase:

$$\delta_{\text{sub}} = \sqrt{\frac{2}{\mu\omega\sigma_{\text{sub}}}}. \tag{7.6}$$

Equation 7.6 defines the skin depth of an infinitely thick substrate. For a substrate with finite thickness, t_{sub}, the effective skin depth, d_{sub}, is given by:

$$d_{\text{sub}} = \delta_{\text{sub}} \left[1 - e^{\left(\frac{-t_{\text{sub}}}{\delta_{\text{sub}}}\right)} \right]. \tag{7.7}$$

The effective depth approaches δ_{sub} when the skin depth is much smaller than the substrate thickness. This is the typical operating regime at gigahertz frequencies for epi-processes, as typical silicon substrate thicknesses range from $300 - 700\mu$m. For example, modern epitaxial processes have conductivities of 10^4Sm^{-1} giving a δ_{sub} of 160μm at 1GHz and 70μm at 5GHz. For a substrate thickness of 300μm, the corresponding effective skin depth is 135μm at 1GHz and 69μm at 5GHz. Since

M_{sub} and R_{sub} become significant as d_{sub} becomes small, we may safely assume that $d_{\text{sub}} \approx \delta_{\text{sub}}$ in the region of interest.

For bulk processes, the substrate conductivity is typically very low ($\approx 10\text{Sm}^{-1}$) and therefore the effective skin depth must be used. However in this case, the magnetic coupling to the substrate can be neglected precisely because of this low conductivity.

The next section will consider how M_{sub} and R_{sub} can be estimated for an epi-process.

7.1.3 Computation of M_{sub} and R_{sub}

Figure 7.3 illustrates the cross section of a spiral inductor on an epi-process. The epi-layer is typically $3 - 10\mu$m thick and has very low conductivity ($10 - 100\text{Sm}^{-1}$) and therefore negligible eddy current flow. The substrate layer is highly conductive ($10^3 - 10^4\text{Sm}^{-1}$) and can support large eddy currents.

The exact computation of the eddy current density is difficult. We simplify the problem by treating the spiral inductor as an equivalent current sheet and by assuming that the substrate eddy currents flow in a current block directly below the current sheet. Figure 7.4 illustrates this approximation. The current density in the substrate block decreases with increasing depth because of two effects:

1. the skin effect in the substrate causes the induced current density to roll off exponentially with increasing depth

2. the induced currents depend on the magnetic field of the spiral inductor. This magnetic field decays as the distance from the spiral increases

We assume that the eddy current density at a given depth is proportional to the *product* of:

1. the exponential decay due to the substrate skin effect so that:

$$I_{\text{sub,fact1}}(z_{\text{sub}}) \propto \frac{1}{\delta_{\text{sub}}} \exp\left(\frac{-z_{\text{sub}}}{\delta_{\text{sub}}}\right) \tag{7.8}$$

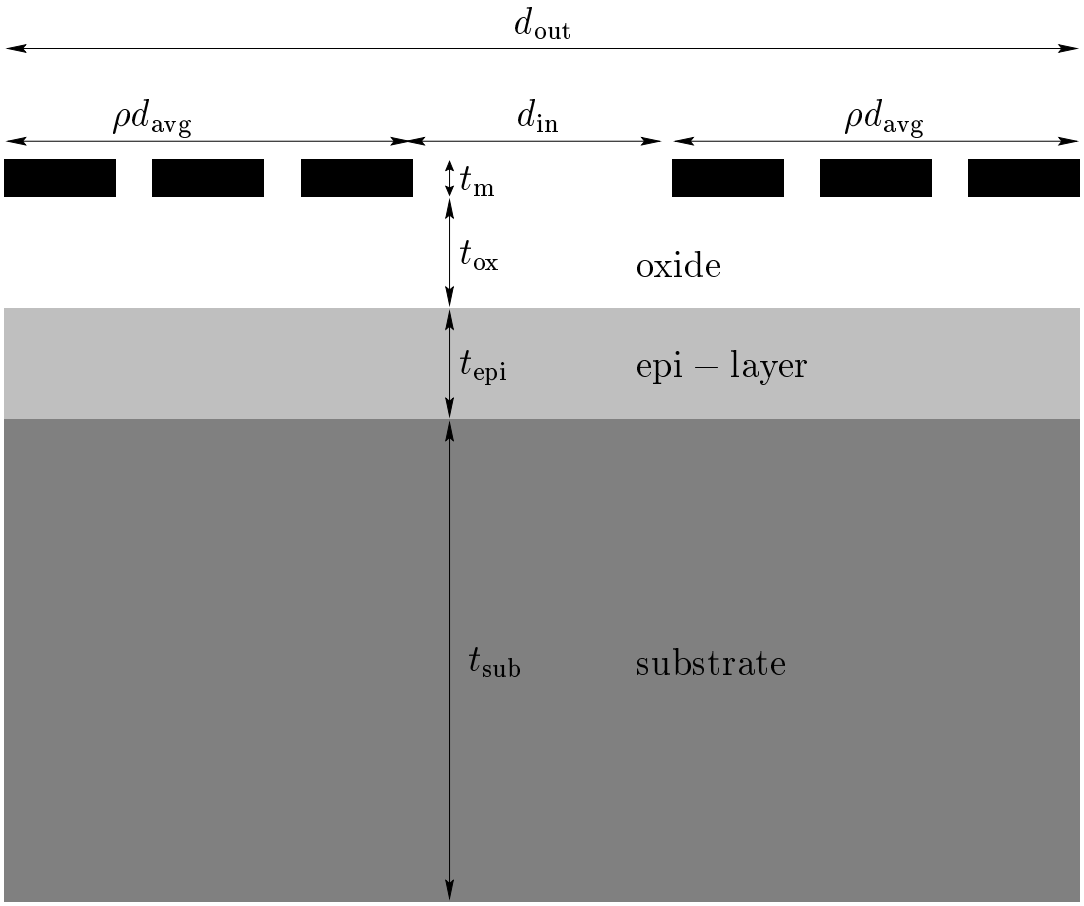


Figure 7.3: Cross section of an epi-process

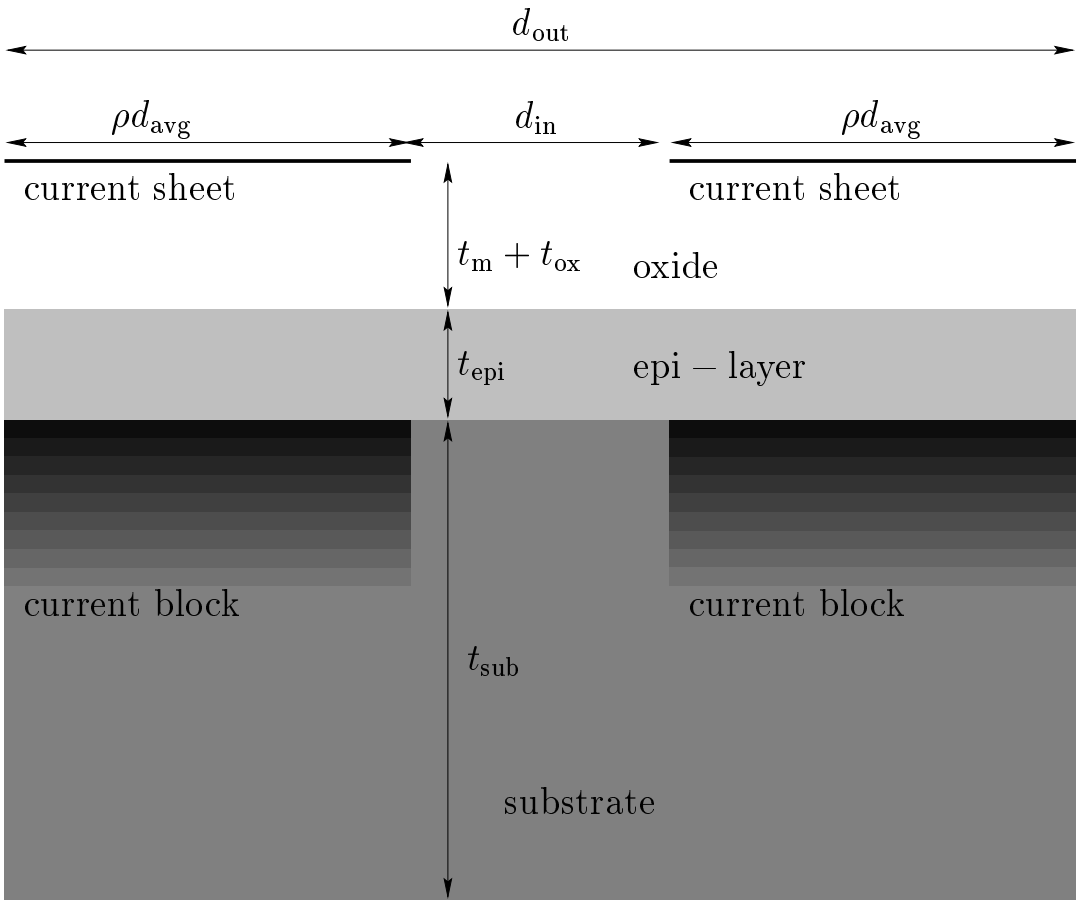


Figure 7.4: Current sheet and current block approximations

and

2. the mutual inductance between the spiral's equivalent current sheet and an equivalent current sheet placed at depth $z_{\rm sub}$:

$$I_{\rm sub,fact12}(z_{\rm sub}) \propto M_{\rm subsheet}(z_{\rm sub}). \tag{7.9}$$

The factor $M_{\rm subsheet}(z_{\rm sub})$ is calculated using the theory developed for current sheets in chapter 3. Note that $M_{\rm subsheet}(z_{\rm sub})$ is dependent on the parameters of the spiral inductor (which for the current sheet approximation are the number of turns, n, the average diameter, $d_{\rm avg}$ and the fill factor, ρ) as well as the total distance of separation, which is equal to $(t_{\rm m} + t_{\rm ox} + t_{\rm epi} + z_{\rm sub})$. The total effective mutual inductance between the spiral and the substrate, $M_{\rm sub}$, is obtained by taking a weighted average of $M_{\rm subsheet}(z_{\rm sub})$ over all values of $z_{\rm sub}$:

$$M_{\rm sub} \approx \frac{\int_0^{t_{\rm sub}} M_{\rm subsheet}(z_{\rm sub}) I_{\rm sub,fact1}(z_{\rm sub}) I_{\rm sub,fact2}(z_{\rm sub}) dz}{\int_0^{t_{\rm sub}} I_{\rm sub,fact1}(z_{\rm sub}) I_{\rm sub,fact2}(z_{\rm sub}) dz}. \tag{7.10}$$

$M_{\rm sub}$ increases as $t_{\rm m}$,$t_{\rm ox}$,$t_{\rm epi}$, $\delta_{\rm sub}$ and ρ decrease and as $d_{\rm avg}$ and n increase. An approximate expression for $M_{\rm sub}$ is obtained by evaluating the integrals in equation 7.10 over a wide design space and data-fitting:

$$M_{\rm sub} \approx \frac{\mu n d_{\rm avg}}{2\pi} \rho^{-0.2} z_{\rm n,ins}^{-0.3} z_{\rm n,sub}^{-0.2}. \tag{7.11}$$

In this expression, $z_{\rm n,ins} = (t_{\rm m} + t_{\rm ox} + t_{\rm epi})/d_{\rm avg}$ and $z_{\rm n,sub} = \delta_{\rm sub}/d_{\rm avg}$. Thus, $z_{\rm n,ins}$ is the ratio of the total thickness of the insulating layers to the spiral's average diameter and $z_{\rm n,sub}$ is the ratio of the substrate skin depth to the spiral's average diameter. This expression has a worst case of error of 10% with respect to the value predicted by equation 7.10.

The resistance $R_{\rm sub}$ is dependent on the effective length, width and thickness of the substrate as well as the conductivity of the substrate. The effective length and width for the current block approximation are $4d_{\rm avg}$ and $\rho d_{\rm avg}$, respectively. The effective thickness is obtained from considering the current density distribution as

a function of depth. Applying the same assumption used in the calculation of M_{sub} (namely that the current distribution is proportional to $I_{\text{sub,fact1}}(z_{\text{sub}})I_{\text{sub,fact2}}(z_{\text{sub}})$), we obtain an approximate expression for the effective thickness:

$$t_{\text{sub,eff}} \approx e^{-1} d_{\text{avg}} \rho^{0.1} z_{\text{n,ins}}^{0.05} z_{\text{n,sub}}^{0.5}. \tag{7.12}$$

Thus, R_{sub} evaluates to:

$$R_{\text{sub}} \approx \frac{\text{length}_{\text{sub,eff}}}{\sigma_{\text{sub}} w_{\text{sub,eff}} t_{\text{sub,eff}}} \approx \frac{4e}{\sigma_{\text{sub}} d_{\text{avg}}} \rho^{-1.1} z_{\text{n,ins}}^{-0.05} z_{\text{n,sub}}^{-0.5}. \tag{7.13}$$

As one expects, the effective resistance of the substrate decreases as the ρ, $z_{\text{n,ins}}$ and $z_{\text{n,sub}}$ increases and as d_{avg} decreases.

7.1.4 Increase in Resistance Due to Magnetic Coupling to the Substrate

The equivalent reflected resistance due to magnetic coupling to the substrate is obtained by combining equations 7.11 and 7.13:

$$R_{\text{eq,reflsub}} \approx \left(\frac{\omega^2 M_{\text{sub}}^2}{R_{\text{sub}}} \right) \approx \frac{\sigma_{\text{sub}}}{4e} \left(\frac{\omega \mu n}{2\pi} \right)^2 d_{\text{avg}}^3 \rho^{0.7} z_{\text{n,ins}}^{-0.55} z_{\text{n,sub}}^{0.1}. \tag{7.14}$$

Since this expression is obtained using several approximations, its accuracy is limited. Nevertheless, the expression provides valuable design insight as it identifies the relative effect of inductor and process parameters on the energy coupled to the substrate. In particular, note that the reflected resistance is proportional to the *cube* of the average diameter, the *square* of the frequency and to the square of the number of turns. We pointed out earlier that magnetic coupling from the substrate to the spiral can be thought of as a transformer with the spiral in the primary, the substrate resistance, R_{sub}, as the load of the secondary and the substrate-to-spiral mutual inductance, M_{sub}, as the mutual inductance between the primary and the secondary. This suggests that the load of the secondary, when reflected to the primary, looks like a resistance, $R_{\text{eq,reflsub}}$, that is equal to the square of the impedance

of M_{sub} divided by R_{sub}. Since the impedance of M_{sub} is simply ωM_{sub}, we expect $R_{\text{eq,reflsub}}$ to be proportional to ω^2. Furthermore, since the mutual inductance M_{sub}, just like the spiral's self inductance, is proportional to the spiral's average diameter, d_{avg}, and the substrate resistance is inversely proportional to d_{avg}, the reflected impedance $R_{\text{eq,reflsub}}$ is proportional to the cube of d_{avg}.

7.2 Measurements

The predictions of the substrate model were compared to measurement results for a 0.5μm CMOS epi-process with a 7μm epi layer with a conductivity of 33Sm^{-1} and a bulk conductivity of 10^4Sm^{-1}. The spirals were designed for use in a GPS receiver so that the frequency of interest was centered at 1.575GHz. A PGS was placed beneath each spiral so that only magnetic coupling to the substrate would degrade the effective resistance. The results are displayed for four spirals in figures 7.5- 7.8.

In each case, the top figure plots R_{s}, $R_{\text{eq,reflsub}}$ and R_{eff} versus frequency. The resistance plots clearly show that the effective series resistance is dominated by the magnetic coupling to the substrate at high frequencies.

The lower figure compares the measured and predicted inductor quality factor (Q_{L}) when only R_{s} and R_{eff} are individually considered. The predictions based on R_{eff} show better agreement with measurements (compared to the predictions based on R_{s}) for all four spirals confirming the importance of modeling magnetic coupling to the substrate.

7.3 Summary

This chapter studied the effect of magnetic coupling from an on-chip spiral to the substrate. A simple model was developed to estimate this effect's impact on performance. While the inductance is not affected significantly, this effect dominates the effective series resistance at high frequencies for modern CMOS-epi processes whose bulk substrate conductivities are $10^3 - 10^4\text{Sm}^{-1}$. Measurements indicate that the simple model correctly estimates the increase in the effective series resistance

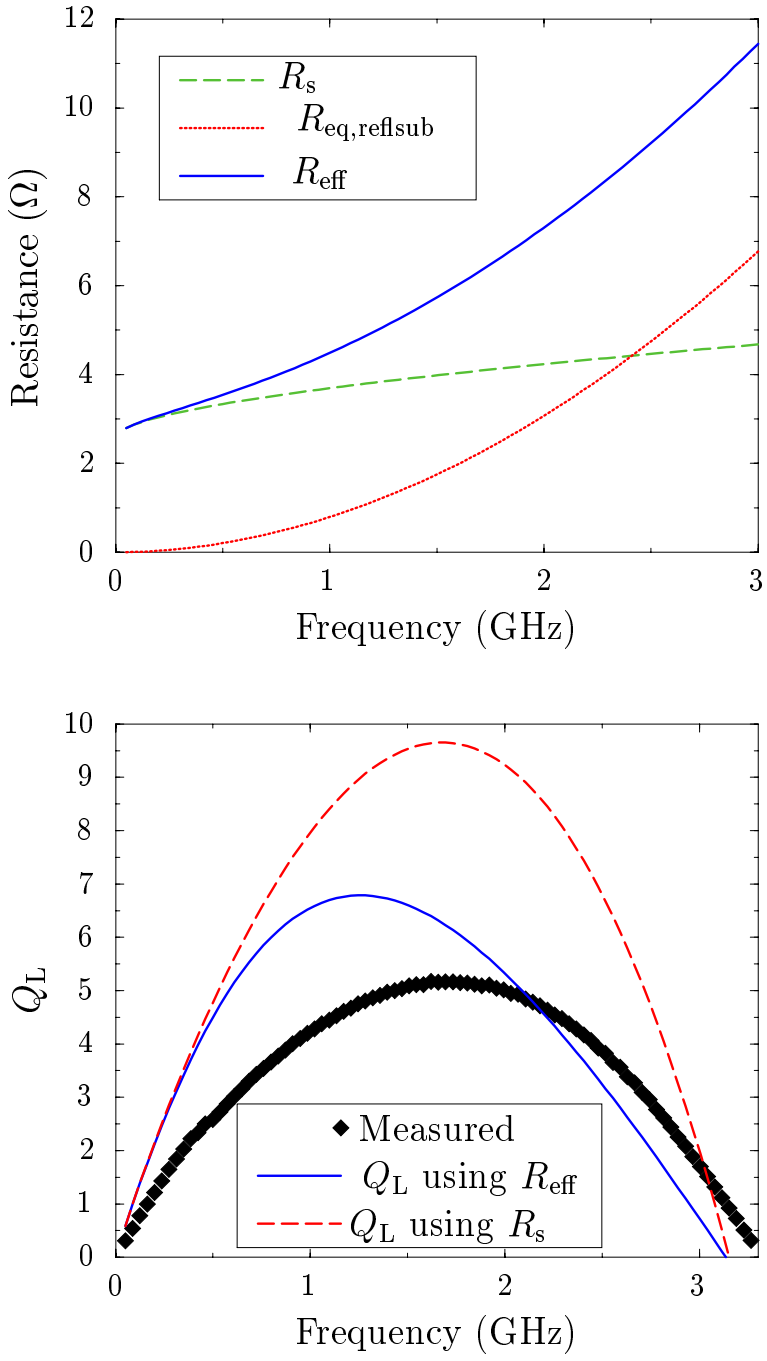


Figure 7.5: Impact of magnetic coupling on series resistance and inductor Q (Q_L) for square spiral with $d_{out} = 345\mu$m, $w = 22.4\mu$m, $s = 2.1\mu$m and $n = 3.75$.

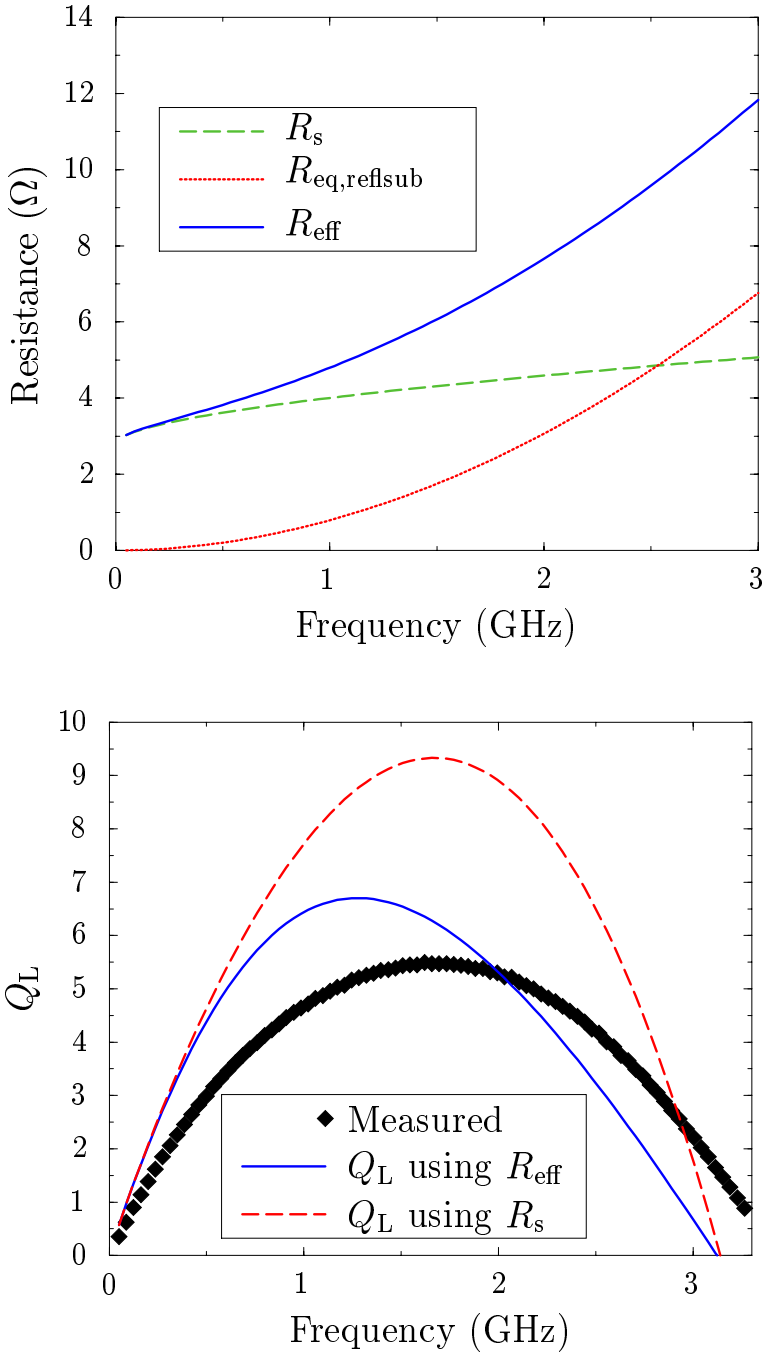


Figure 7.6: Impact of magnetic coupling on series resistance and inductor Q (Q_L) for square spiral with $d_{out} = 325\mu$m, $w = 21.0\mu$m, $s = 2.1\mu$m and $n = 4.25$.

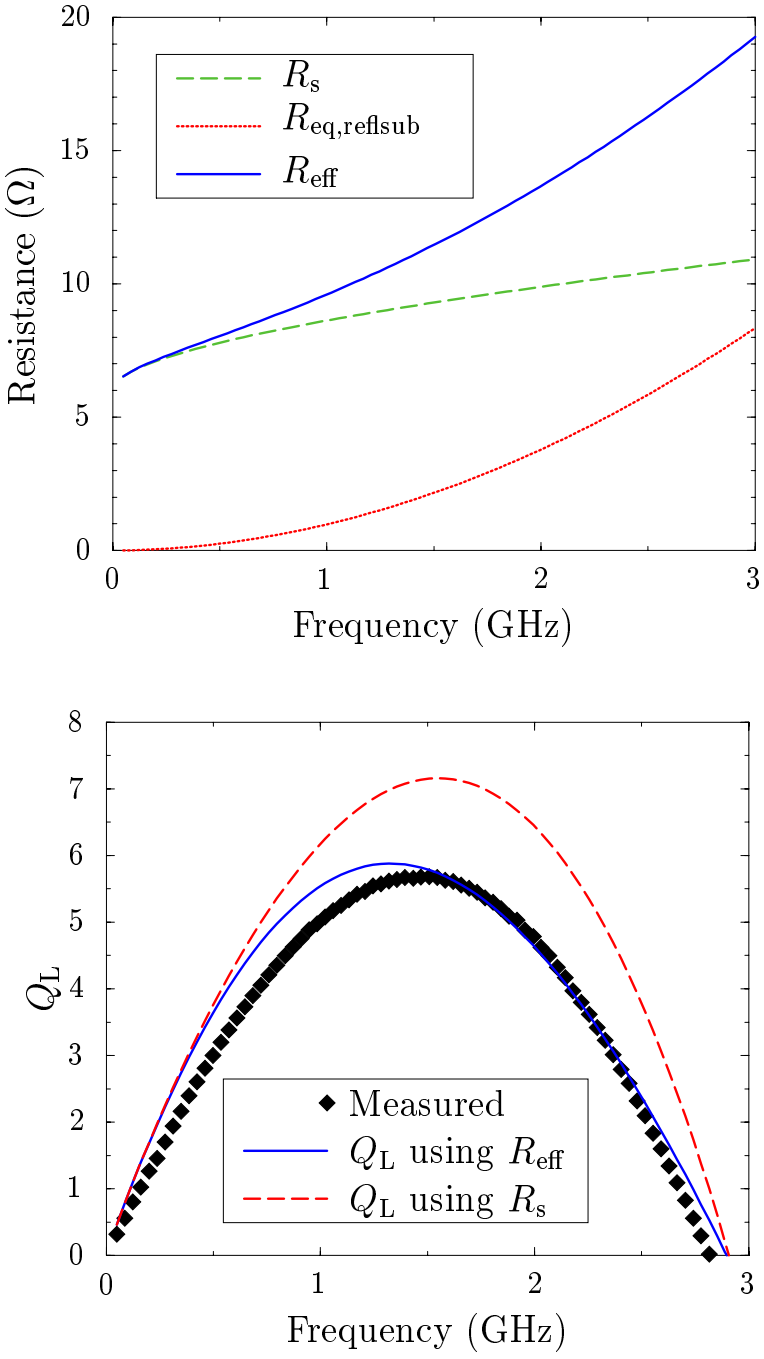


Figure 7.7: Impact of magnetic coupling on series resistance and inductor Q (Q_L) for square spiral with $d_{out} = 300\mu$m, $w = 12.0\mu$m, $s = 2.1\mu$m and $n = 5.25$.

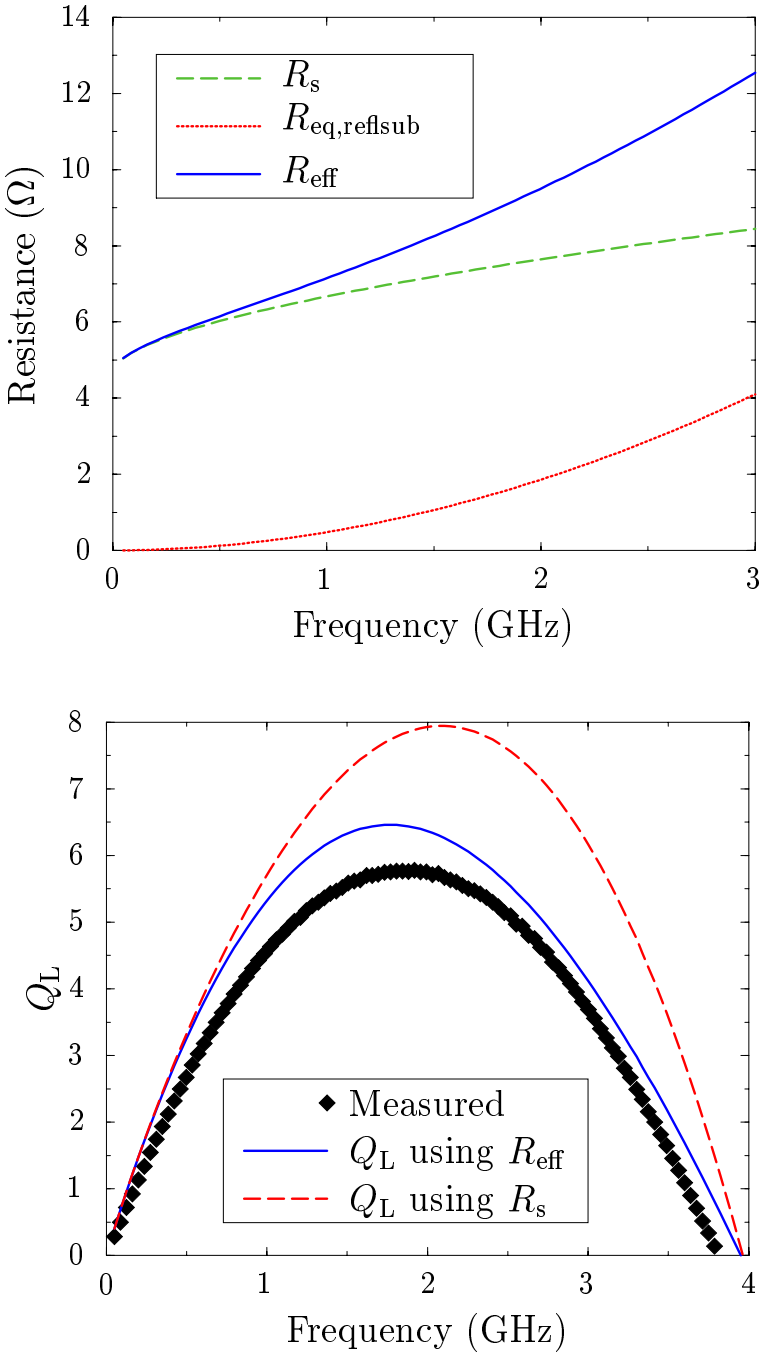


Figure 7.8: Impact of magnetic coupling on series resistance and inductor Q (Q_L) for square spiral with $d_{out} = 240\mu$m, $w = 12.0\mu$m, $s = 2.1\mu$m and $n = 5.75$.

to within 20%. More important, the model provides design insight on how a spiral could be optimized so as to minimize degradation to magnetic coupling to the substrate.

As higlighted during the discussion of equation 7.14, the resistive loss term arising from magnetic coupling to the substrate is proportional the cube of the average diameter, d_{avg}. Clearly, minimizing the average diameter is paramount. However, this reduction in d_{avg} should not affect the value of the inductance nor the series resistance of the spiral's conductor. One possible solution is to use a series connected stack of spirals to achieve a higher inductance density thanks to the boost provided by the mutual inductance between the stacked spirals. Chapter 5 discussed stacked spiral configurations and pointed out that the maximum achievable mutual coupling coefficient, k, is around 0.9. This corresponds to an increase in inductance density of $2(1+k) = 3.6$ if one uses two stacked spirals with maximum overlap. Assuming that the two spirals are built on metal layers of equal conductivities, this would result in a factor of two increase in the interconnect's series resistance. For a fixed inductance and interconnect series resistance, the area of the stacked spiral is a factor of ≈ 1.9 smaller than that of a single layer implementation. Therefore its d_{avg} is a factor of $\approx \sqrt{1.9}$ smaller than that of a single layer spiral. This suggests that the increase in resistance due to magnetic coupling to the substrate can be reduced by a factor of $\approx 2-3$ by using two layer stacked spirals, implying significant Q boosts are possible.

The drawback of the stacked spiral is the reduction in the self-resonant frequency due to the increase in parasitic capacitance. While the dominant capacitance of a single layer implementation is the spiral-to-substrate capacitance, the stacked spiral's capacitance is typically dominated by the capacitance between the stacked spirals. Furthermore, the capacitance density from the spiral-to-substrate increases because the use of multiple layers reduces the distance between the spiral and the substrate. This increase in capacitance density is partially offset by the reduction in the area of a stacked spiral. It is this reduction in self-resonant frequency that limits the optimum number of stacked spirals to two or three. More work is needed to quantify and compare the performance improvement afforded by stacked spirals.

Chapter 8

Conclusion

This thesis has investigated the design and modeling of on-chip spiral inductors and transformers. This chapter summarizes the major contributions of this work and identifies areas that merit future study.

8.1 Contributions

- A current sheet approach was developed that permits simple, accurate expressions to be derived for the inductance of commonly used conductor geometries.

- Simple, accurate expressions were derived for the inductance of on-chip planar spirals. These expressions, which exhibit typical errors of $\approx 2-4\%$ with respect to simulations of field solvers and measured data, are easily incorporated into existing lumped circuit inductor models.

- Techniques for calculating the mutual inductance and the mutual coupling coefficient of single layer and two-layer planar on-chip transformers were presented. These techniques, based on the current sheet approach and the inductance expressions mentioned above, yield simple, accurate, analytical expressions for the mutual inductance and mutual coupling coefficient.

- A general approach to modeling planar, on-chip transformers using a scalable, lumped circuit model was studied for both single layer and multiple layer implementations. The predictions of these models agree well with measurements. The lumped circuit transformer models provide valuable design insight and can easily be incorporated into a standard circuit design environment (such as *SPICE*)

- The simple inductance expressions were applied in circuit design problems to quickly and easily evaluate the optimum inductor designs. The availability of these expressions allows the user to simultaneously optimize both passive and active components, thereby facilitating the design of a variety inductor circuits including low-noise amplifiers (LNAs), oscillators, matching networks and filters.

- An area and power efficient technique was developed for extending the bandwidth of broadband amplifiers by using optimized on-chip inductors as shunt-peaking elements. This technique was applied to the implementation of a transimpedance preamplifier designed as the front-end of a gigabit optical communication system. This preamplifier is the first CMOS implementation that uses planar spiral inductors as shunt-peaking elements.

- Magnetic coupling between a planar spiral inductor and the substrate was studied. A simplified current sheet based approximation yielded valuable insight on the nature of this interaction and identified the critical geometrical and process parameters associated with this coupling. A simple, approximate expression was developed to provide design guidelines. This work serves as a good foundation for incorporating magnetic coupling to the substrate into a lumped circuit inductor model.

While the current sheet approach forms the theoretical basis for this thesis, the accurate inductance expressions and transformer models presented are valuable design tools for any practicing circuit designer. All in all, the contributions of this work

substantially reduce the time required to optimize monolithic inductor circuits, by eliminating the need for a field solver during the initial design stages.

8.2 Future Work

This sections identifies topics covered in this thesis which merit more detailed study.

8.2.1 Magnetic Coupling to the Substrate

Chapter 7 investigated the effect of magnetic coupling between a spiral inductor and a lossy substrate. This study provided valuable design insight and identified the major design parameters that influence the severity of this coupling. Simple expressions for estimating the mutual inductance between the spiral and substrate, the eddy current resistance of the substrate and the associated increase in the effective series resistance of the spiral were obtained through this treatment.

Magnetic coupling to substrate is a serious concern in modern sub-micron CMOS epitaxial processes which use high conductivity bulk substrates. The robust optimization of inductor circuits in such processes can be accomplished only if a lumped inductor model accounts for magnetic substrate coupling. The work in this thesis suggests that this effect can be accounted for by an additional term in the series resistance of lumped circuit model. However, more work is needed to obtain a simple accurate expression that quantifies this additional term.

8.2.2 Nonuniform Current Distributions

The current sheet approach assumes that the current density in all the conductors is uniform. This assumption does not hold at high frequencies for a system of conductors. First, the skin effect causes more current to flow close to the surface of the conductors. Second, the proximity effect produces an uneven current distribution in multiple closely-spaced parallel conductors.

Although nonuniform current distributions have only a second-order effect on the inductance of planar spirals, they have a first order impact on the series resistance.

The lumped circuit model described in chapter 2 uses a very simple expression to model the skin effect. The proximity effect is not modeled at all. Further study is required to understand the impact of these mechanisms, especially in the presence of a conductive substrate.

8.3 Summary

This thesis has contributed to a better understanding of on-chip spiral inductors and transformers. This work has provided accurate expressions, new models and engineering insight, all of which facilitate the design and optimization of monolithic inductor and transformer circuits.

Appendix A

Inductances of Current Sheets

In this appendix, we derive simple expressions for the self and mutual inductances of various current sheet geometries. These geometries, in addition to being useful in their own light, also serve as good approximations to more complicated structures such as square spirals.

A.1 Rectangular Current Sheet

We wish to compute the self inductance of a rectangular current sheet of length, l, and width, w, with $w < l$. We approach this problem by considering two line filaments that are spaced at distances x_1 and x_2 from the center of the sheet as illustrated in Figure A.1. Hence, x_1 and x_2 are variables that can take any values between $-\frac{w}{2}$ and $\frac{w}{2}$. We start off with the simplified equation (accurate to within 5% for $R < l$) that was introduced in chapter 3 for the mutual inductance between parallel straight line filaments of equal length:

$$M \approx \frac{\mu l}{2\pi}\left[\ln(2l) - \ln(R) - 1 + \frac{R}{l} - \frac{R^2}{4l^2}\right], \tag{A.1}$$

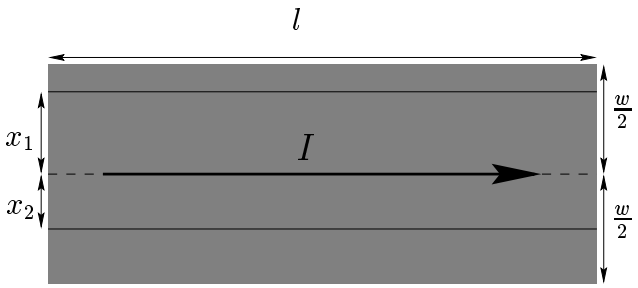


Figure A.1: Rectangular current sheet

where l is the length of each line, and R is the distance between the two lines. In our case, $R = x_1 + x_2$ so that:

$$M \approx \frac{\mu l}{2\pi}\left[\ln(2l) - \ln|x_1 + x_2| - 1 + \frac{|x_1 + x_2|}{l} - \frac{(x_1 + x_2)^2}{4l^2}\right]. \tag{A.2}$$

The self inductance of the current sheet is obtained by obtaining the mean values of the terms involving the variables x_1 and x_2 The term involving the natural logarithm may be replaced by the GMD of a straight line of length, w:

$$\begin{aligned}\overline{\ln|x_1 + x_2|} &= \ln \mathrm{GMD}_{\mathrm{line}} \\ &= \ln w - 1.5.\end{aligned} \tag{A.3}$$

The linear term may be replaced by the AMD of a straight line of length, w:

$$\begin{aligned}\overline{|x_1 + x_2|} &= \mathrm{AMD}_{\mathrm{line}} \\ &= \frac{w}{3}.\end{aligned} \tag{A.4}$$

The quadratic term may be replaced by the AMSD of a straight line of length, w:

$$\begin{aligned}\overline{(x_1 + x_2)^2} &= {\mathrm{AMSD}_{\mathrm{line}}}^2 \\ &= \frac{w^2}{6}\end{aligned} \tag{A.5}$$

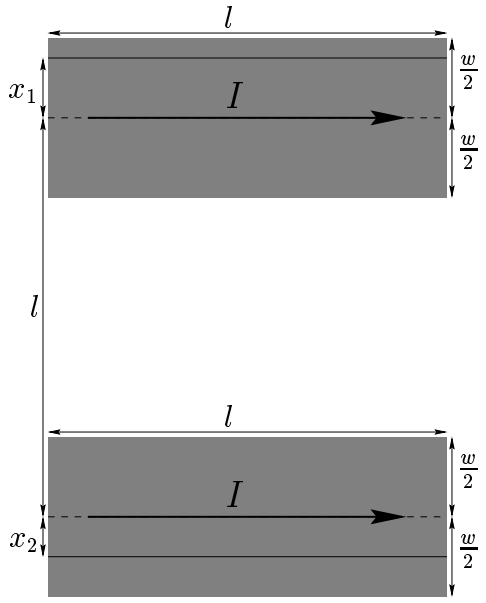


Figure A.2: Parallel rectangular current sheets

Hence, the self inductance of the the rectangular current sheet is:

$$L_{\text{rectsheet}} \approx \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{w}\right) + 0.5 + \frac{w}{3l} - \frac{w^2}{24l^2}\right]. \tag{A.6}$$

A.2 Parallel Rectangular Current Sheets

We wish to compute the mutual inductance between two identical parallel rectangular current sheets, each of length, l, and width, w. The two sheets are separated by a center-to-center distance that is the same as each sheet's length, l. We approach this problem by considering two line filaments that are spaced at distances x_1 and x_2 from the centers of each sheet (see figure A.2). Hence, x_1 and x_2 are variables that can take any values between $-\frac{w}{2}$ and $\frac{w}{2}$. Since $w < l$, x_1 and x_2 are restricted to values less than $\frac{l}{2}$. We begin with the exact expression for the mutual inductance

between parallel straight lines of equal length:

$$M = \frac{\mu}{2\pi}\left[l\ln\left(\sqrt{\left(\left(\frac{l}{R}\right)^2+1\right)}+\frac{l}{R}\right)-\sqrt{(l^2+R^2)}+R\right], \tag{A.7}$$

where l is the length of each line, and R is the distance between the two lines so that $R = l + x_1 + x_2$. We note that $(x_1 + x_2) < l$ and write the mutual inductance in terms of the quantity $\frac{(x_1+x_2)}{l}$:

$$\begin{aligned} M \approx & \frac{\mu l}{2\pi}\left[\ln(1+\sqrt{2})-\sqrt{2}+1+\ln(l)-\ln(l+x_1+x_2)\right] \\ & +\frac{\mu l}{2\pi}\left[\frac{(1-\sqrt{2})(x_1+x_{2)}}{l}+\frac{(\sqrt{2}-2)(x_1+x_2)^2}{4l^2}\right]. \end{aligned} \tag{A.8}$$

The mutual inductance between the current sheets is derived by obtaining the mean values of the terms involving the variables x_1 and x_2. The term involving the natural logarithm may be replaced by the GMD between two equal lines of length, w:

$$\begin{aligned} \overline{\ln|l+x_1+x_2|} &= \ln \mathrm{GMD}_{\mathrm{line}} \\ &\approx \ln l - \frac{w^2}{12l^2}. \end{aligned} \tag{A.9}$$

The linear term evaluates to zero as both x_1 and x_2 are zero mean variables:

$$\overline{x_1+x_2} = 0. \tag{A.10}$$

The mean of the quadratic term may be evaluated by noting that the calculation matches the definition for the AMSD of a line of length, w, so that:

$$\begin{aligned} \overline{(x_1+x_2)^2} &= \mathrm{AMSD}_{\mathrm{line}}{}^2 \\ &= \frac{w^2}{6}. \end{aligned} \tag{A.11}$$

Hence, the mutual inductance between the two rectangular current sheet is:

$$\begin{aligned} M_{\text{rectsheet}} &\approx \frac{\mu l}{2\pi}\left[\ln(1+\sqrt{2})+1-\sqrt{2}+\ln l-\ln l+\frac{w^2}{12l^2}+\frac{(\sqrt{2}-2)w^2}{24l^2}\right] \\ &\approx \frac{\mu l}{2\pi}\left[\ln(1+\sqrt{2})+1-\sqrt{2}+\frac{\sqrt{2}w^2}{24l^2}\right] \\ &\approx \frac{\mu l}{2\pi}\left[0.467+\frac{0.059w^2}{l^2}\right]. \end{aligned} \tag{A.12}$$

A.3 Trapezoidal Current Sheet

We wish to calculate the self inductance of the trapezoidal current sheet illustrated in figure A.3. This current sheet is completely specified by the average length, l, and width, w, with $w < l$. As shown in the figure, we approach this problem by considering two line filaments that are spaced at distances x_1 and x_2 from the center of the sheet. The variables x_1 and x_2 can take any values between $-\frac{w}{2}$ and $\frac{w}{2}$. Noting that the lengths of the filament are not equal, we begin with expressions for the mutual inductance between two parallel straight lines of unequal length:

$$\begin{aligned} M = &\frac{\mu}{2\pi}\left[\left(\frac{l_1+l_2}{2}\right)\ln\left(\sqrt{\left(\frac{l_1+l_2}{2R}\right)^2+1}+\left(\frac{l_1+l_2}{2R}\right)\right)-\sqrt{\left(\frac{l_1+l_2}{2}\right)^2+R^2}\right] \\ &-\frac{\mu}{2\pi}\left[\left|\frac{l_1-l_2}{2}\right|\ln\left(\sqrt{\left(\frac{l_1-l_2}{2R}\right)^2+1}+\left|\frac{l_1-l_2}{2R}\right|\right)-\sqrt{\left(\frac{l_1-l_2}{2}\right)^2+R^2}\right]. \end{aligned} \tag{A.13}$$

For the geometry under consideration $l_1 = l + 2x_1$, $l_2 = l + 2x_2$ and $R = x_1 - x_2$. Hence $\frac{(l_1+l_2)}{2} = (l + x_1 + x_2)$ and $R = \frac{|l_1-l_2|}{2} = |x_1 - x_2|$. Once again, $(x_1 - x_2) < l$, allowing us to write the expression for the mutual inductance as a series expansion in terms of $\frac{(x_1+x_2)}{l}$ and $\frac{(x_1-x_2)}{l}$:

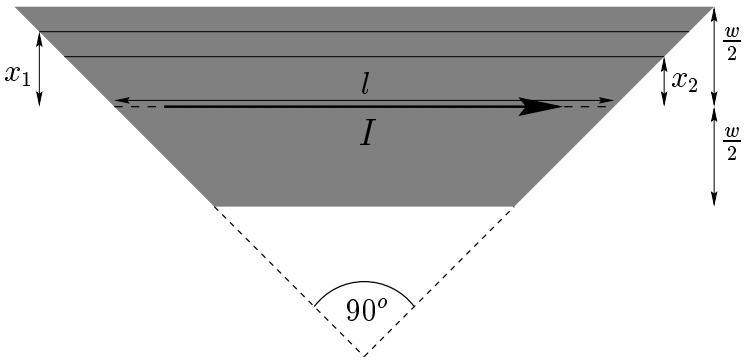


Figure A.3: Trapezoidal current sheet

$$M \approx \frac{\mu l}{2\pi}\left[\ln 2l - \ln|x_1 - x_2| - \frac{|x_1 - x_2|(\ln(\sqrt{2}+1) - \sqrt{2})}{l}\right] + \frac{\mu l}{2\pi}\left[\frac{(x_1+x_2)^2}{2l^2} - \frac{(x_1-x_2)^2}{4l^2}\right]. \tag{A.14}$$

The self inductance of the current sheet is obtained by evaluating the mean values of the terms involving the variables $(x_1 + x_2)$ and $|x_1 + x_2|$. The term involving the natural logarithm may be replaced by the GMD of a straight line of length w:

$$\begin{aligned}\overline{\ln|x_1 - x_2|} &= \mathrm{GMD}_{\mathrm{line}} \\ &= \ln w - 1.5.\end{aligned} \tag{A.15}$$

The linear term may be replaced by the AMD of a straight line of length w:

$$\begin{aligned}\overline{|x_1 + x_2|} &= \mathrm{AMD}_{\mathrm{line}} \\ &= \frac{w}{3}.\end{aligned} \tag{A.16}$$

Both quadratic terms may be replaced by the AMSD of a straight line of length w:

$$\begin{aligned}\overline{(x_1 + x_2)^2} = \overline{(x_1 - x_2)^2} &= {\mathrm{AMSD}_{\mathrm{line}}}^2 \\ &= \frac{w^2}{6}.\end{aligned} \tag{A.17}$$

Hence, the self inductance of the trapezoidal current sheet is:

$$\begin{aligned} L_{\text{trapsheet}} &\approx \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{w}\right) + 0.5 + \frac{w}{3l}\left(\sqrt{2} - \ln\left(1+\sqrt{2}\right)\right) + \frac{w^2}{24l^2}\right] \\ &\approx \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{w}\right) + 0.5 + \frac{0.178w}{l} + \frac{0.0417w^2}{l^2}\right]. \end{aligned} \tag{A.18}$$

A.4 Parallel Trapezoidal Current Sheets

Figure A.4 shows two identical parallel trapezoidal current sheets of average length, l, and width, w that are separated by center-to-center distance, l. As shown in the figure, we approach this problem by considering two line filaments that are spaced at distances x_1 and x_2 from each of the centers of the sheets. The variables x_1 and x_2 can take any values between $-\frac{w}{2}$ and $\frac{w}{2}$. Once again we use the expression for the mutual inductance between two parallel straight lines of unequal length:

$$\begin{aligned} M = \frac{\mu}{2\pi}&\left[\left(\frac{l_1+l_2}{2}\right)\ln\left(\sqrt{\left(\frac{l_1+l_2}{2R}\right)^2+1}+\left(\frac{l_1+l_2}{2R}\right)\right) - \sqrt{\left(\frac{l_1+l_2}{2}\right)^2+R^2}\right] \\ -\frac{\mu}{2\pi}&\left[\left|\frac{l_1-l_2}{2}\right|\ln\left(\sqrt{\left(\frac{l_1-l_2}{2R}\right)^2+1}+\left|\frac{l_1-l_2}{2R}\right|\right) - \sqrt{\left(\frac{l_1-l_2}{2}\right)^2+R^2}\right]. \end{aligned} \tag{A.19}$$

For the geometry under consideration, $l_1 = l + 2x_1$, $l_2 = l + 2x_2$ and $R = l + x_1 + x_2$. Hence $\frac{(l_1+l_2)}{2} = R = (l + x_1 + x_2)$ and $\frac{|l_1-l_2|}{2} = |x_1 - x_2|$. Noting that $(x_1 - x_2) < l$, we write the expression for the mutual inductance as a series expansion in terms of $\frac{(x_1+x_2)}{l}$ and $\frac{(x_1-x_2)}{l}$:

$$M \approx \frac{\mu l}{2\pi}\left[(\ln(\sqrt{2}+1) - \sqrt{2} + 1) + (x_1+x_2)(\ln(\sqrt{2}+1) - \sqrt{2} + 1) - \frac{(x_1-x_2)^2}{2l^2}\right]. \tag{A.20}$$

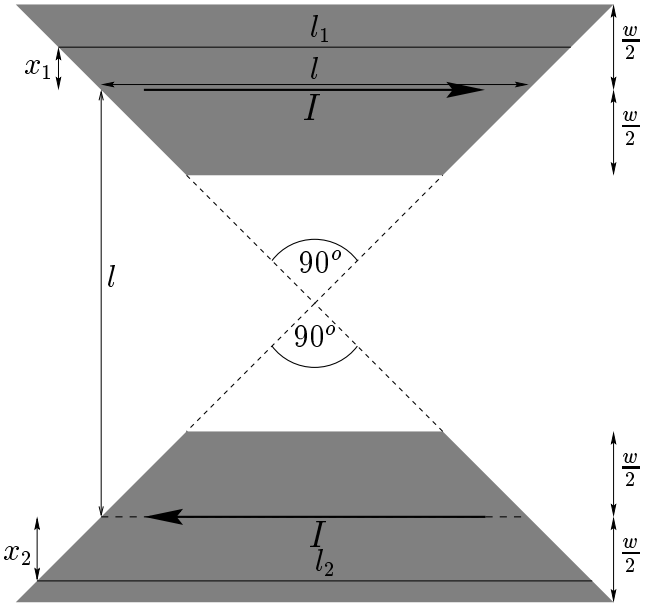


Figure A.4: Parallel trapezoidal current sheets

The mutual inductance between the current sheets is obtained by determining the mean values of the terms involving the variables $(x_1 + x_2)$ and $|x_1 + x_2|$. The linear term evaluates to zero as both x_1 and x_2 are zero mean variables:

$$\overline{x_1 + x_2} = 0. \tag{A.21}$$

The mean of the quadratic term may be evaluated by noting that the calculation matches the definition of the AMSD of a straight line of length, w, so that:

$$\begin{aligned} \overline{(x_1 - x_2)^2} &= \mathrm{AMSD}_{\mathrm{rectsheet}}{}^2 \\ &= \frac{w^2}{6}. \end{aligned} \tag{A.22}$$

Hence, the mutual inductance between the two trapezoidal current sheets is:

$$\begin{aligned} M_{\text{trapsheet}} &\approx \frac{\mu l}{2\pi}\left[\ln(1+\sqrt{2})+1-\sqrt{2}-\frac{w^2}{12l^2}\right] \\ &\approx \frac{\mu l}{2\pi}\left[0.467-\frac{0.083w^2}{l^2}\right]. \end{aligned} \tag{A.23}$$

Appendix B

Inductances of Planar Circular Geometries

In this appendix, we will derive simple expressions for the self and mutual inductances for circular filaments, circular current sheets and circular rings.

B.1 Planar Concentric Circular Filaments

Let us consider the mutual inductance between two concentric circular filaments of radii r_1 and r_1 as illustrated in figure B.1. We begin with the Neumann double integral for the mutual inductance between two current elements:

$$M = \frac{\mu}{4\pi} \oint\oint \frac{1}{R} \mathbf{dl_1} . \mathbf{dl_2}, \tag{B.1}$$

where $\mathbf{dl_1}$ and $\mathbf{dl_2}$ are the vector current elements and R is the distance between the elements. The distance between the two elements on the circles is given by:

$$R = \sqrt{r_1^2 + r_2^2 - 2r_1 r_2 \cos\theta}. \tag{B.2}$$

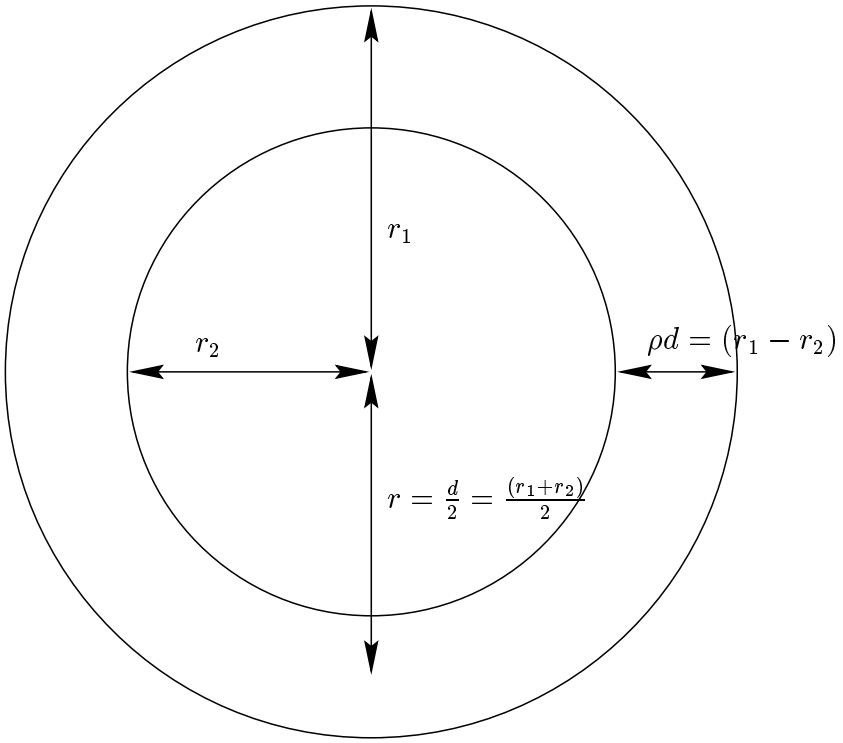


Figure B.1: Mutual inductance between circular filaments

By circular symmetry, the expression for the mutual inductance reduces to a single integral:

$$M = \frac{\mu}{4}\int_0^{2\pi} \frac{2r_1 r_2 \cos\theta}{\sqrt{r_1^2 + r_2^2 - 2r_1 r_2 \cos\theta}}\, d\theta. \tag{B.3}$$

This may be rewritten as:

$$M_{\text{circfil}} = \frac{\mu(r_1^2 + r_2^2)}{r_1 + r_2}\left[\int_0^{\pi/2} \frac{1}{\sqrt{1 - \frac{4r_1 r_2 \sin^2\phi}{(r_1+r_2)^2}}}\, d\phi\right] - \mu(r_1 + r_2)\left[\int_0^{\pi/2} \sqrt{1 - \frac{4r_1 r_2 \sin^2\phi}{(r_1+r_2)^2}}\, d\phi\right]. \tag{B.4}$$

Using the average diameter, $d = (r_1 + r_2)$, and the ratio of the separation to the average diameter, $\rho = \frac{(r_1 - r_2)}{d}$, we recast this integral as:

$$M = \frac{\mu d}{2}(1 + \rho^2)\left[\int_0^{\pi/2} \frac{1}{\sqrt{1 - (1 - \rho^2)\sin^2\phi}}\, d\phi\right] - \mu d\left[\int_0^{\pi/2} \sqrt{1 - (1 - \rho^2)\sin^2\phi}\, d\phi\right]. \tag{B.5}$$

Noting that the integrals are complete elliptic integrals of the first and second kind, we obtain:

$$M_{\text{circfil}} = \frac{\mu d}{2}\left[(2 - m)K(m) - 2E(m)\right], \tag{B.6}$$

where $K(m)$ is the complete elliptic integral of the first kind and $E(m)$ is the complete elliptic integral of the second kind, with argument $m = (1 - \rho^2)$. A simpler, more insightful expression may be obtained via series expansion in terms of ρ. This approach yields an expression that resembles the approximate expression obtained for the mutual inductance between two straight, parallel lines:

$$M_{\text{circfil}} \approx \frac{\mu d}{2}\left[\ln\left(\frac{1}{\rho}\right) - 0.6 + 0.7\rho^2\right]. \tag{B.7}$$

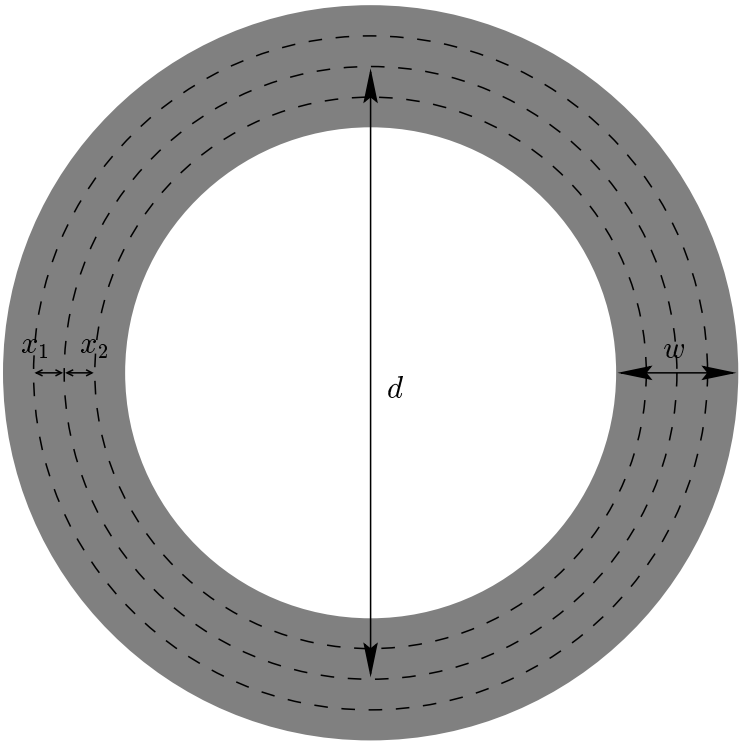


Figure B.2: Mutual inductance between circular filaments

This expression is accurate to within 5% for $\rho < 0.6$ and is good enough for most practical cases.

B.2 Self Inductance of a Circular Sheet

Figure B.2 shows a circular current sheet of average diameter, d, and width, w. We approach this problem by considering the mutual inductance between two circular filaments of diameters $(d + 2x_1)$ and $(d - 2x_2)$. The spacing between these filaments is $|x_1 + x_2|$. The variables x_1 and x_2 may each take values ranging from $-w/2$ to

$w/2$. We use the approximate expression (equation B.7) for circular filaments that was derived in section B.1:

$$M \approx \frac{\mu(d + x_1 - x_2)}{2} \left[\ln \left(\frac{(d + x_1 - x_2)}{|x_1 + x_2|} \right) - 0.6 + 0.7 \left(\frac{|x_1 + x_2|}{(d + x_1 - x_2)} \right)^2 \right]. \quad \text{(B.8)}$$

The self inductance of the current sheet is obtained by determining the mean values of the terms involving the variables $(d + x_1 - x_2)$ and $|x_1 + x_2|$. This task is simplified by using series approximations of the quantities $|x_1 + x_2|$ and $|x_1 - x_2|$. Such expansions are valid as both these quantities are always less than the average diameter, d. For our purposes, we only need terms up to the second order:

$$\overline{(d + x_1 - x_2) \ln (d + x_1 - x_2)} \approx d \ln d + \frac{w^2}{12d}. \quad \text{(B.9)}$$

$$\overline{(d + x_1 + x_2) \ln |x_1 - x_2|} \approx d(\ln w - 1.5). \quad \text{(B.10)}$$

$$\overline{\left(\frac{|x_1 + x_2|^2}{|d + x_1 - x_2|} \right)} \approx \frac{w^2}{6d}. \quad \text{(B.11)}$$

The final expression is:

$$L_{\text{circsheet}} \approx \frac{\mu d}{2} \left[\ln \left(\frac{d}{w} \right) + 0.9 + 0.2 \frac{w^2}{d^2} \right]. \quad \text{(B.12)}$$

B.3 Planar Concentric Current Sheets

Figure B.3 shows two circular concentric current sheets of average diameters d_1 and d_2. The sheets have equal width, w, and are separated by a center to center distance, ρd, where d is the mean of the two average diameters ($d = 0.5(d_1 + d_2)$). Note that $\rho d = w + s$. Once again, we approach this problem by considering the mutual inductance between two circular filaments of diameters $(d_1 + 2x_1)$ and $(d_2 + 2x_2)$.

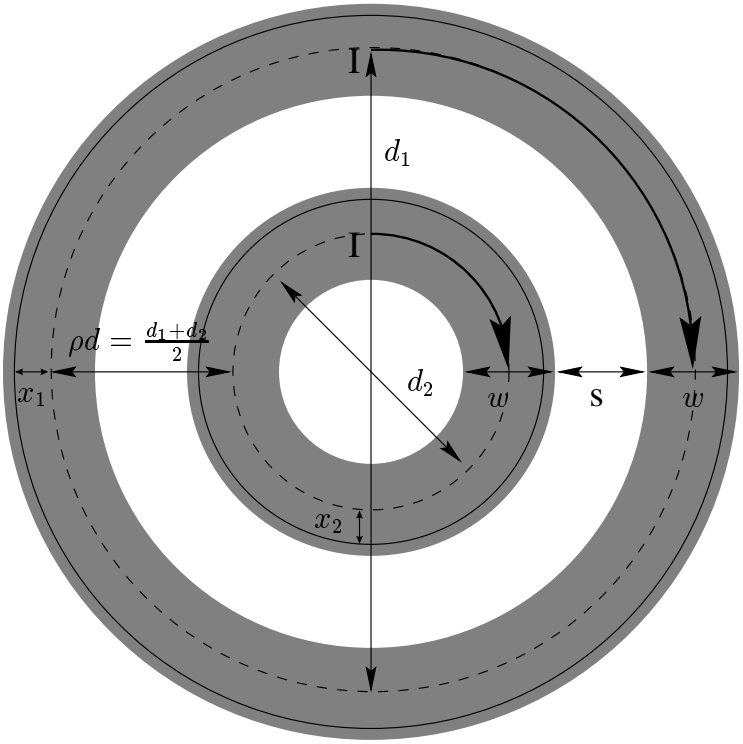


Figure B.3: Mutual inductance between circular filaments

The spacing between these filaments is $(\rho d + x_1 - x_2)$. The variables x_1 and x_2 may each take values ranging from $-w/2$ to $w/2$. Applying equation B.6, we obtain:

$$M_{\text{circ2sheets}} = \overline{\frac{\mu(d + x_1 + x_2)}{2}\left[(2-m)K(m) - 2E(m)\right]}, \tag{B.13}$$

where m is a variable in terms of x_1 and x_2:

$$m = 1 - \frac{(\rho d + x_1 - x_2)^2}{(d + x_1 + x_2)^2}. \tag{B.14}$$

The overall mutual inductance is computed by using the GMD and AMSD concepts to estimate the mean value over all values of x_1 and x_2:

$$M_{\text{circ2sheets}} \approx \frac{\mu d}{2}\left[(2-m)K(m) - 2E(m) + \left(0.2 + \frac{1}{12\rho^2}\right)\frac{w^2}{d^2}\right]. \tag{B.15}$$

In this case, the parameter, m, is a constant and is simply given by $m = (1 - \rho^2)$. An approximate series expansion of this expression, using techniques similar to the ones used in section B.1, yields:

$$M_{\text{circ2sheets}} \approx \frac{\mu d}{2}\left[\ln\left(\frac{1}{\rho}\right) - 0.6 + 0.7\rho^2 + \left(0.2 + \frac{1}{12\rho^2}\right)\frac{w^2}{d^2}\right]. \tag{B.16}$$

Appendix C

Bandwidth Extension using Optimized On-Chip Inductors

This appendix discusses the design of a monolithic amplifier that uses on-chip spirals as shunt peaking elements to achieve better performance. The bandwidth extension technique discussed in chapter 6 is applied in the implementation of a 2.125Gbaud preamplifier that employs a common-gate input stage followed by a cascoded common-source stage. On-chip shunt-peaking is introduced at the dominant pole to improve the overall system performance, including a 40% increase in the transimpedance (alternatively, one could state that the bandwidth increase is around 40% while keeping the transimpedance fixed). This implementation achieves a 1.6kΩ transimpedance and a 0.6μA input referred current noise, while operating with a photodiode capacitance of 0.6pF. A fully differential topology ensures good substrate and supply noise immunity. The amplifier, implemented in a triple metal, single poly, 14GHz $f_{\mathrm{T_{max}}}$, 0.5μm CMOS process, dissipates 225mW of which 110mW is consumed by the 50Ω output driver stage. The optimized on-chip inductors consume only 15% of the total area of 0.6mm^2.

Section C.1 discusses some system considerations for the application. Section C.2 outlines fundamental limits on the performance of traditional transimpedance amplifier architectures. Section C.3 proposes a topology for circumventing these limits. Section C.4 discusses the design methodology for incorporating shunt-peaking into

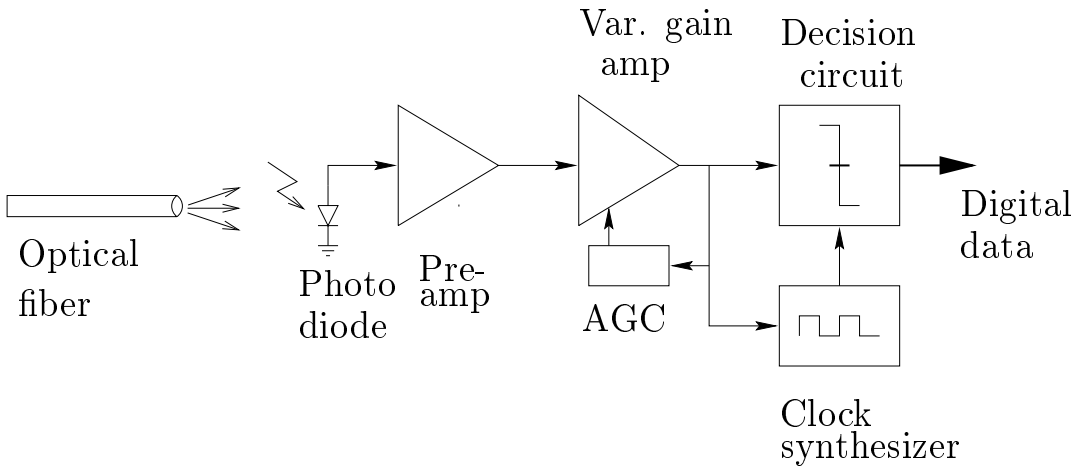


Figure C.1: System overview

transimpedance amplifiers. Section C.5 discusses the differential prototype that was implemented while section C.6 addresses sensitivity issues. Layout details and experimental measurements are presented in section C.7 which is followed by a summary in section C.8.

C.1 System Overview

This section illustrates how optimized on-chip spiral inductors can improve the performance of a preamplifier intended for the front-end of a gigabit optical system. Figure C.1 shows the block diagram of a typical optical communication receiver. The key performance parameters of such a front-end are bandwidth, sensitivity, stability and dynamic range. The system's bandwidth and sensitivity are determined largely by the preamplifier [43, 44, 45, 46]. While a high bandwidth demands a small input resistance, good sensitivity requires the resistors in the signal path to be large in order to minimize thermal noise. Thus, the preamplifier is typically implemented using a transimpedance architecture as it provides a large bandwidth by synthesizing a small input resistance using a much larger feedback resistor.

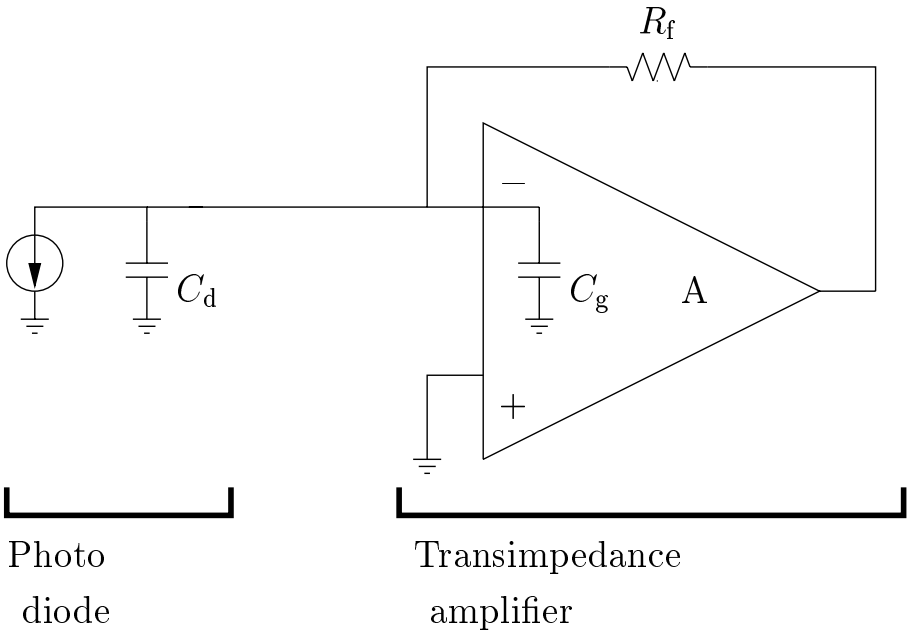


Figure C.2: Conventional preamplifier architecture

C.2 Transimpedance Limit

Figure C.2 illustrates the main elements of a transimpedance preamplifier. Assuming that the bandwidth of the amplifier is set by the input pole, we obtain:

$$\omega_{3dB} = \frac{1}{R_{in}C_{in}}, \tag{C.1}$$

where ω_{3dB} is the 3dB bandwidth of the circuit, R_{in} is the input resistance and C_{in} is total input capacitance.

The input resistance R_{in} is given by:

$$R_{in} = \frac{R_f}{A+1} \approx \frac{R_f}{A} \tag{C.2}$$

where R_f is the feedback resistance and A is the open loop gain of the amplifier. The approximate expression is valid when $A >> 1$.

The input capacitance $C_{\rm in}$ is given by :

$$C_{\rm in} = C_{\rm g} + C_{\rm D}, \tag{C.3}$$

where $C_{\rm g}$ is the input gate capacitance of the amplifier and $C_{\rm D}$ is the sum of the capacitances of the active area of the photodiode as well as associated parasitic capacitances (arising from bondpads etc.). In GaAs implementations, $C_{\rm D}$ can be kept small by integrating the photodiode and the preamplifier on the same die. In such technologies, $C_{\rm D}$ as small as 50fF are common [47]. Silicon bipolar and CMOS implementations are not so fortunate: a $C_{\rm D}$ of $\approx 300 - 600$fF is typical.

The gain bandwidth product determines the maximum available gain for a given bandwidth. Denoting the transition frequency as $\omega_{\rm T}$, we relate the gain, A, to the 3dB bandwidth $\omega_{\rm 3dB}$:

$$A \approx \frac{\omega_{\rm T}}{\omega_{\rm 3dB}}. \tag{C.4}$$

Substituting equations C.2-C.4 in to equation C.1, we obtain a maximum achievable transimpedance, $R_{\rm f,max}$:

$$R_{\rm f,max} \approx \frac{\omega_{\rm T}}{\omega_{\rm 3dB}^2 (C_{\rm g} + C_{\rm D})} \tag{C.5}$$

Noting that the transconductance, $g_{\rm m}$, of the input stage is related to $C_{\rm g}$ by $g_{\rm m} \approx \omega_{\rm T} C_{\rm g}$, and that for optimum sensitivity, $C_{\rm g} \approx C_{\rm D}$, we conclude that the maximum achievable transimpedance is determined by the system bandwidth specification, the total input capacitance and the process constant, $\omega_{\rm T}$.

C.3 Circumventing the Transimpedance Limit

Figure C.3 illustrates a modified preamplifier architecture that circumvents the transimpedance limit. The transimpedance stage is decoupled from the photodiode by a common-gate stage and the gain-bandwidth product of the transimpedance stage is enhanced by shunt-peaking. Now, the sensitive feedback node of the transimpedance

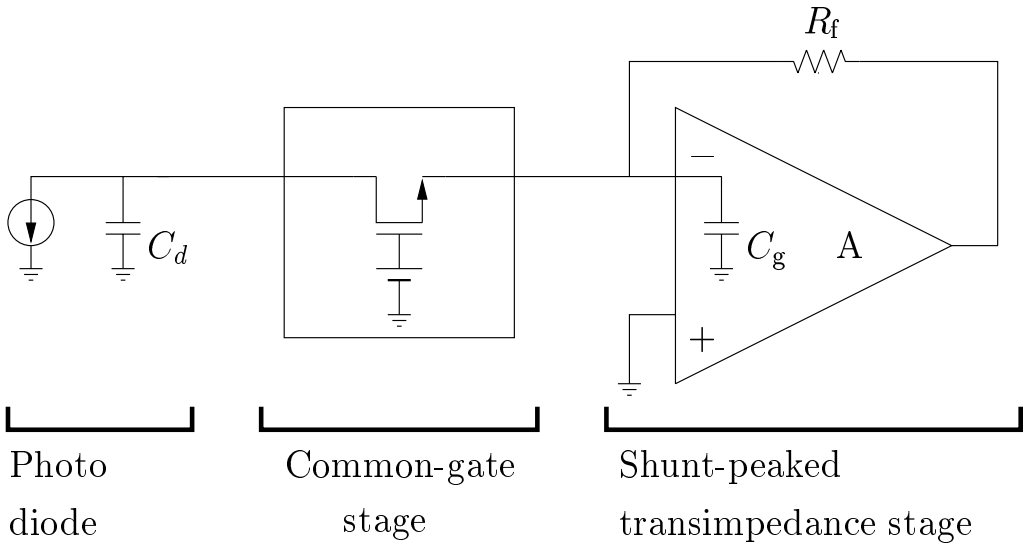


Figure C.3: Preamplifier with shunt peaking

stage is more robust as its poles are not determined by any off-chip components. Furthermore, the common-gate stage permits the transistors of the transimpedance stage to be sized smaller enabling a higher transimpedance to be achieved.

Note that the common-gate stage is not necessary to obtain the benefits of shunt-peaking. If desired, one could connect the photodiode directly to a shunt-peaked transimpedance stage, an implementation that is particularly attractive for applications that demand the best achievable sensitivity for a given power. However, such an approach requires the parasitic impedance of the photodiode to be known so that the transimpedance stage can be sized for optimal performance [46]. The introduction of the common-gate stage offers an additional degree of flexibility for the designer and permits stable operation over a wider range of photo diode capacitances. This is valuable in cases (such as our prototype) where the capacitance of the photodiode structure is not known in advance. The drawback of the common-gate source is the degradation in the high frequency noise performance due to the source junction capacitance of the common-gate transistor, an issue that will be addressed more in section C.6.

C.4 Shunt-peaked Transimpedance Stage

Figure C.4 illustrates the shunt-peaked transimpedance stage. The cascode eliminates the bandwidth degradation due to the Miller capacitance of the common-source stage's gate-drain capacitance. This degradation is particularly significant in CMOS circuits, where the gate-drain capacitance can be as high as one-third of the gate-source capacitance. The cascode also enhances the overall gain by increasing the stage's output impedance.

The dominant pole in the amplifier occurs at the drain of the cascode transistor. The bandwidth of the amplifier is improved by applying shunt-peaking at this node. The inductor, resistors and transistors are sized for optimum group delay over the signal bandwidth. The design methodology can be summarized as follows:

1. Design and optimize transimpedance stage for desired signal bandwidth without shunt peaking.

2. Use transistor current and interconnect current density specification to determine inductor's turn width, w.

3. Determine minimum turn spacing, s, from process specifications.

4. Choose number of turns, n, and outer diameter d_{out} to realize optimum L while minimizing parasitic capacitance and area.

5. Increase the transimpedance resistance, R_{f}, and the total load resistance, R.

The availability of a lumped inductor model (with analytical expressions for all elements including the inductance) and the use of geometric programming allows this entire design and optimization process to be automated so that no iteration is needed on the part of the designer (see chapter 6 for more details and references). In this case, the 20nH peaking inductor has an outer diameter of only 180μm. This inductor has 11.75 turns, a width of 3.2μm, a spacing of 2.1μm, implemented on the third (top) metal layer with thickness 2.1μm. The shuntpeaking yields a 40% increase in the transimpedance of this stage (for a fixed signal bandwidth) with no

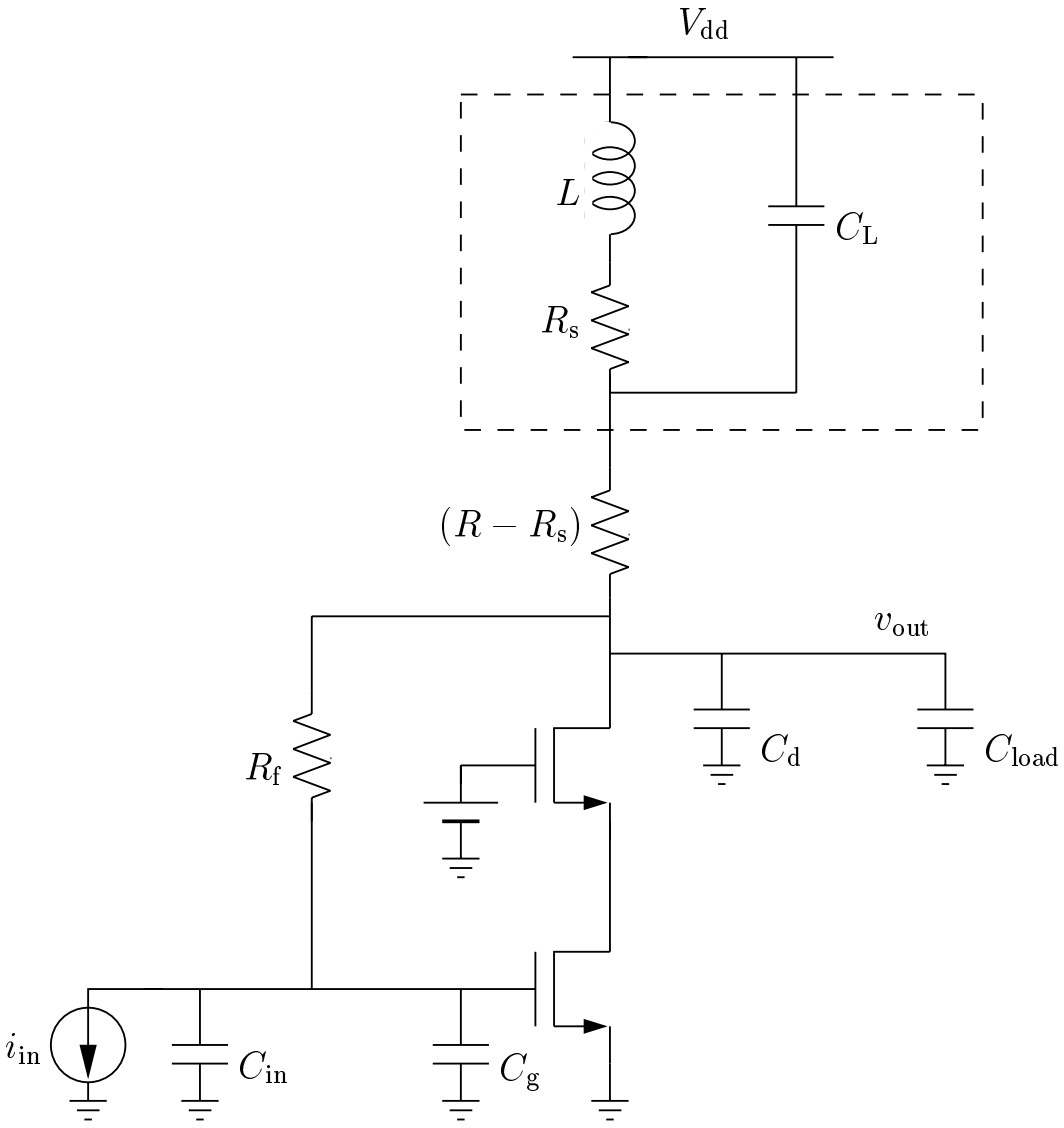


Figure C.4: Shunt-peaked transimpedance stage

additional power dissipation. Alternatively, the shunt peaking could have been used to increase the signal bandwidth (by $\approx 40\%$ with respect to the unpeaked case) for a fixed transimpedance.

C.5 Differential Implementation

Compared to differential architectures, single-ended architectures consume less power, take up less die area, and exhibit better noise performance (when power consumption is fixed). However at high frequencies they are susceptible to supply noise and are plagued by stability problems stemming from parasitic feedback paths. By providing good common-mode rejection, differential architectures circumvent these disadvantages, and are therefore preferred in systems where integration of the analog and digital functions is the ultimate goal. In keeping with this premise, the architecture described here is fully differential and provides complementary outputs, which is a necessity given that high-speed digital and clocking circuitry operate in differential mode.

Figure C.5 shows the schematic of the complete prototype preamplifier. The common-gate (CG) stage is followed by the common-source (CS) transimpedance stage, whose output feeds a source follower that buffers the output driver. The output driver is only needed for testing purposes and is neither needed nor desired in a system where the analog and digital components of a receiver are integrated.

The chip consumes a total of 225mW, of which the 50Ω output driver consumes 110mW. For optimum sensitivity, the total power consumption of the common-gate and common-source stages is roughly proportional to the photodiode capacitance. This preamplifier has been designed to operate with an external capacitance as large as 600fF. The need to support such a large capacitance arises because the photodiodes are external to the chip with correspondingly large bondpad capacitances. Recent research has explored flip-chip bonding techniques for reducing the capacitance loading of the front-end to less than 100fF. Such a low input capacitance would permit a higher input impedance and therefore allow smaller devices to be

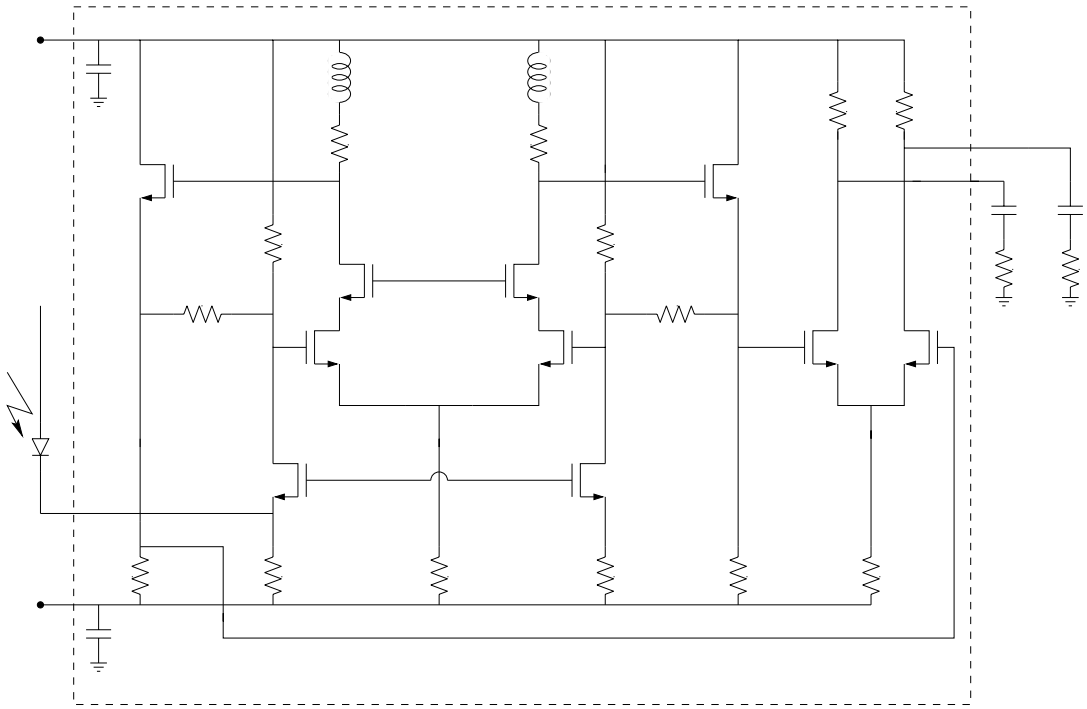


Figure C.5: Simplified circuit diagram

used throughout the preamplifier, resulting in a substantial power saving, while retaining the same bandwidth and improving sensitivity. Alternatively, the reduced capacitance would allow the design of preamplifiers with increased bandwidth supporting faster baud rates.

C.6 Noise Considerations

The sensitivity of the preamplifier is usually expressed as the equivalent integrated input-referred current noise density. Much literature exists concerning the minimum noise conditions for conventional optical preamplifiers [43, 48]. Some studies have also investigated how inductors can increase the sensitivity of optical preamplifiers implemented in GaAs [44].

The noise performance of the common-gate (CG) input stage followed by the common-source (CG) transimpedance stage has been studied in GaAs HBT and BiCMOS processes [49]. Although a simulation involving a single-ended CMOS version was reported, it ignored the effects of the source and drain junction capacitances and did not consider the impact of short-channel effects on small signal behavior and noise [50].

Junction capacitances in submicron CMOS processes are comparable to the gate capacitances and therefore significantly influence both noise behavior and bandwidth. A rigorous analysis that includes the impact of the junction capacitances and short-channel behavior yields two conditions for a noise optimum. First, the saturation mode gate capacitance of the common-source stage must equal the saturation mode drain capacitance of the common-gate stage so that $C_{\mathrm{gs,CS}} + C_{\mathrm{gd,CS}} = C_{\mathrm{gd,CG}} + C_{\mathrm{db,CG}}$. Second, the saturation mode input capacitance of the common-gate stage (which is the gate-source capacitance, $C_{\mathrm{gs,CG}}$, plus the source-substrate capacitance $C_{\mathrm{sb,CG}}$) must equal βC_{ext}, where $\beta \approx 0.8 - 1$. The factor β is a function of ω_{T}, the coefficients of channel thermal noise (γ), and the ratios of junction capacitance to gate capacitance, all of which are bias dependent. For a typical CMOS device in saturation, $(C_{\mathrm{gs}} + C_{\mathrm{sb}})$ is around 3-4 times as big as $(C_{\mathrm{gd}} + C_{\mathrm{db}})$ and therefore the common-source stage can now be sized smaller, allowing a corresponding increase

in the feedback resistance and a dramatic decrease in power consumption, while retaining the same device f_T. The buffer stage that follows the common-source stage can also be sized smaller, as can the width of all the interconnects, resulting in a smaller die area. The transconductance of the common-gate stage only needs to be large enough to ensure that the input pole is non-dominant, enabling the power consumption of the first stage to be small.

The introduction of the common-gate stage introduces three new noise sources: the thermal noise of the source resistor, the thermal noise of the drain resistor, and the thermal channel noise of the common-gate transistor. Of these terms, careful design ensures that the resistors are made large enough so as not to significantly affect the noise performance. The thermal channel noises of the common-gate and common-source devices are reflected at the input by equivalent current noise spectral densities proportional to the square of the frequency. When integrated over frequency, these terms dominate, a behavior typical of short-channel CMOS processes, where carrier velocity saturation conditions cause thermal channel noise to increase due to excess noise stemming from hot electron effects [35, 51]. Balancing that degradation is the higher f_T delivered by the continuing reduction in gate length, thereby improving noise performance. However, carrier velocity saturation causes the small signal transconductance (and f_T) to be smaller than that predicted by long channel (square-law) approximations.

C.7 Layout and Experimental Details

As shown in the die photo (figure C.6), the chip area is dominated by the passive components, which is typical of RFICs. However, the two inductors combined occupy less than 15% of the total area, thanks to the optimized shunt-peaking technique described in the earlier sections. A patterned ground shield is used beneath the inductors to reduce substrate coupling [52]. Differential symmetry and cross quad layout are used to ensure maximum matching, thereby reducing common-mode noise and systematic offset. On chip capacitance of 16pF is used to provide supply decoupling. Several substrate contacts, placed around the transistors, minimize source

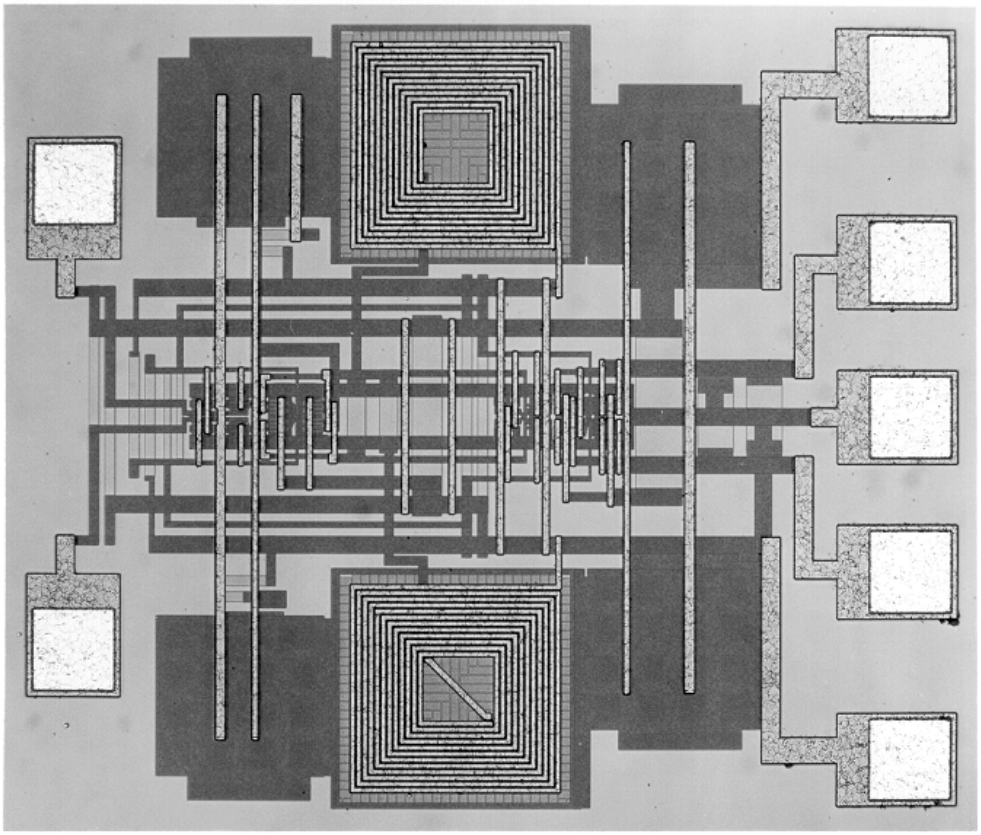


Figure C.6: Preamplifier die photo

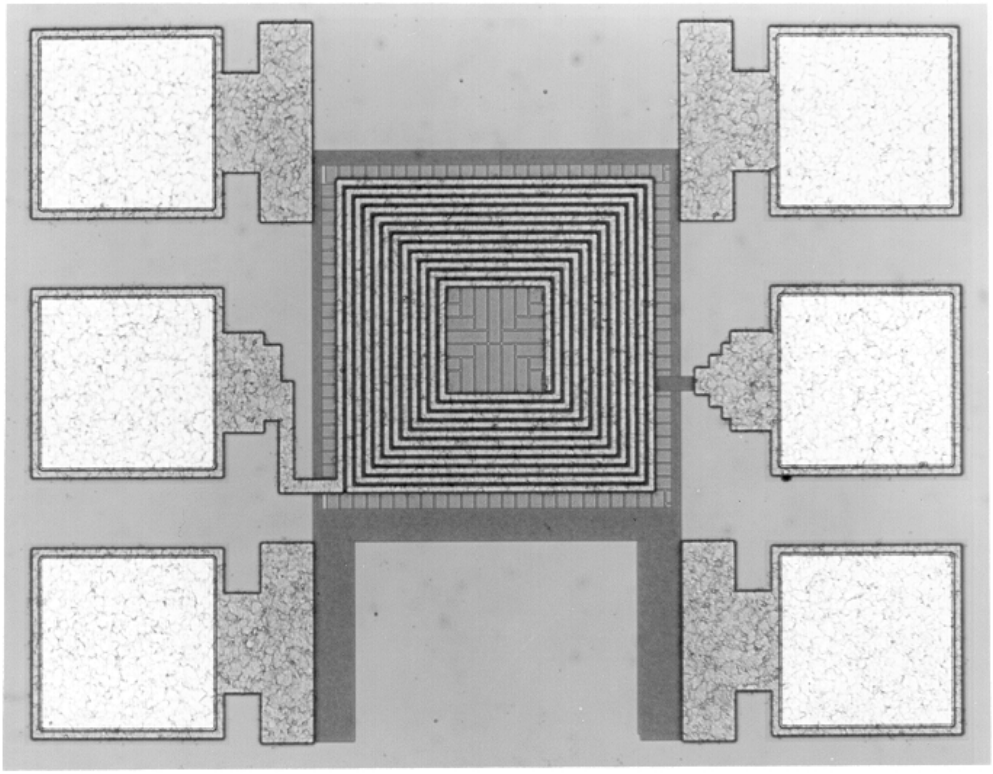


Figure C.7: Inductor test structure

inductance. The floor plan keeps the sensitive input bond pads as far away from the other pads as possible.

Figure C.7 shows the test structure of the spiral inductor used for shunt-peaking. The S-parameters of the inductor were measured using coplanar ground-signal-ground (GSG) probes and an open calibration structure. The inductance and the one-terminal impedance (which is the relevant measure in our amplifier) were extracted from these measurements. As shown in figure C.8, good agreement between the prediction of the lumped circuit inductor model and measured data is obtained for the equivalent one-terminal impedance of the spiral inductor used for shunt-peaking. In particular, we note that the measured inductance of 20.5nH matches

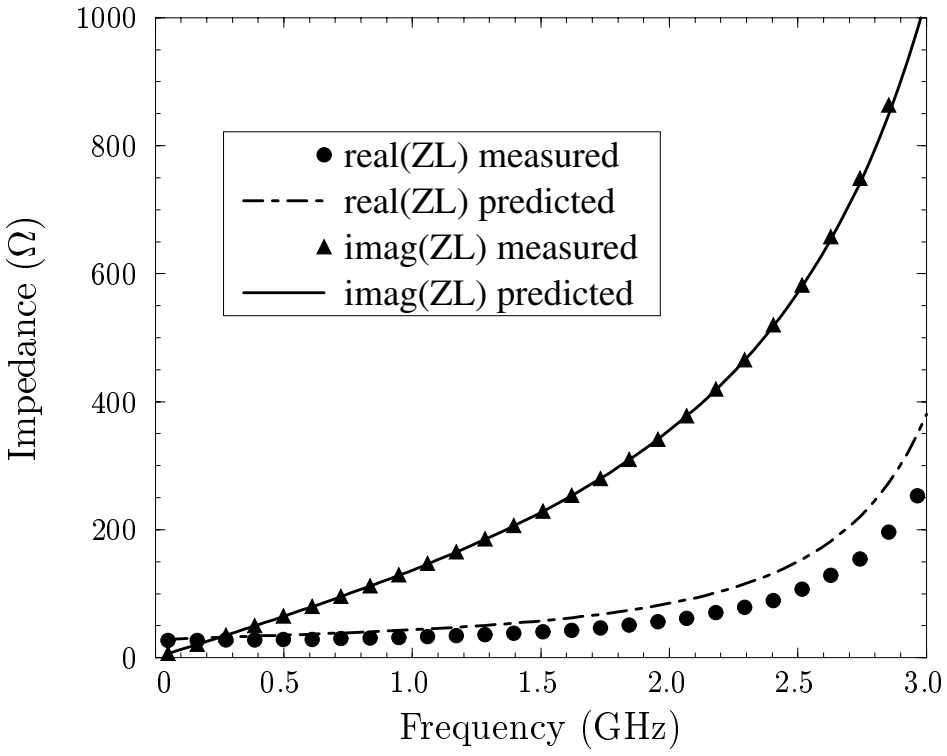


Figure C.8: Simulated and measured one-terminal impedance of the spiral inductor used for shunt-peaking: $d_{\text{out}} = 180\mu$m, $n = 11.75$ turns, $w = 3.2\mu$m, $s = 2.1\mu$m and $t = 2.1\mu$m with $L = 20$nH

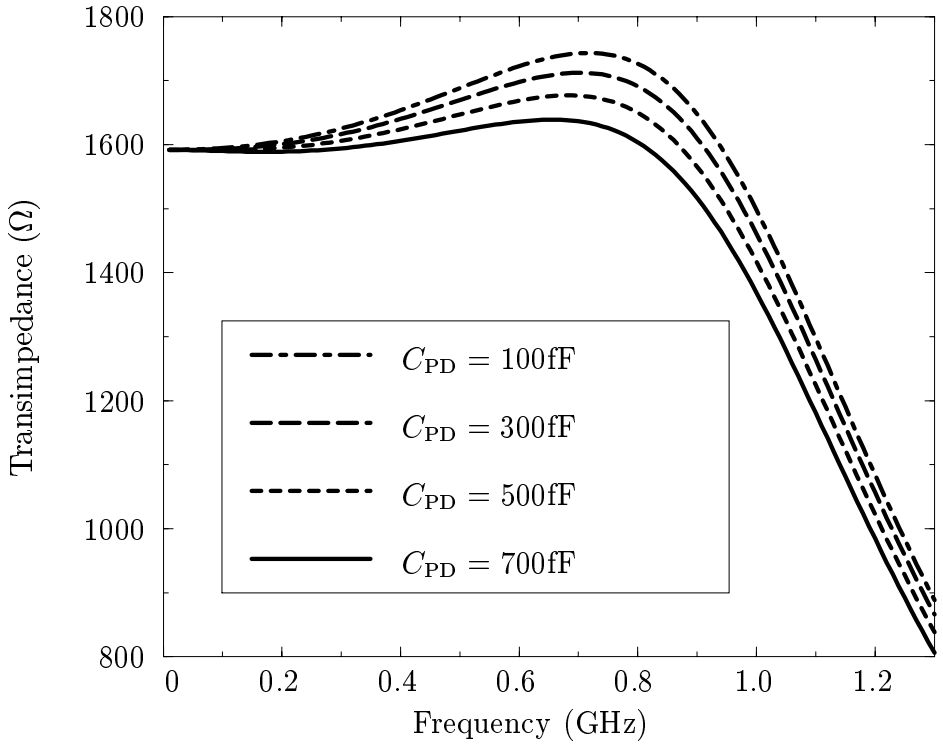


Figure C.9: Simulated transimpedance vs. frequency

the 20.3nH value predicted by our simple inductance expressions to within a 1% error.

Figure C.9 shows the preamplifier's simulated transimpedance versus frequency for photodiode capacitances varying from 100fF to 700fF. As can be seen, the 3dB bandwidth is around 1.2GHz and is only weakly dependent on the photodiode capacitance. Maximum gain peaking is 1dB. These simulations are run with the output driving a 50Ω resistance and 1pF capacitance.

Figure C.10 illustrates the preamplifier's simulated equivalent input referred current noise spectral density for a photodiode capacitance of 600fF. The coefficient of

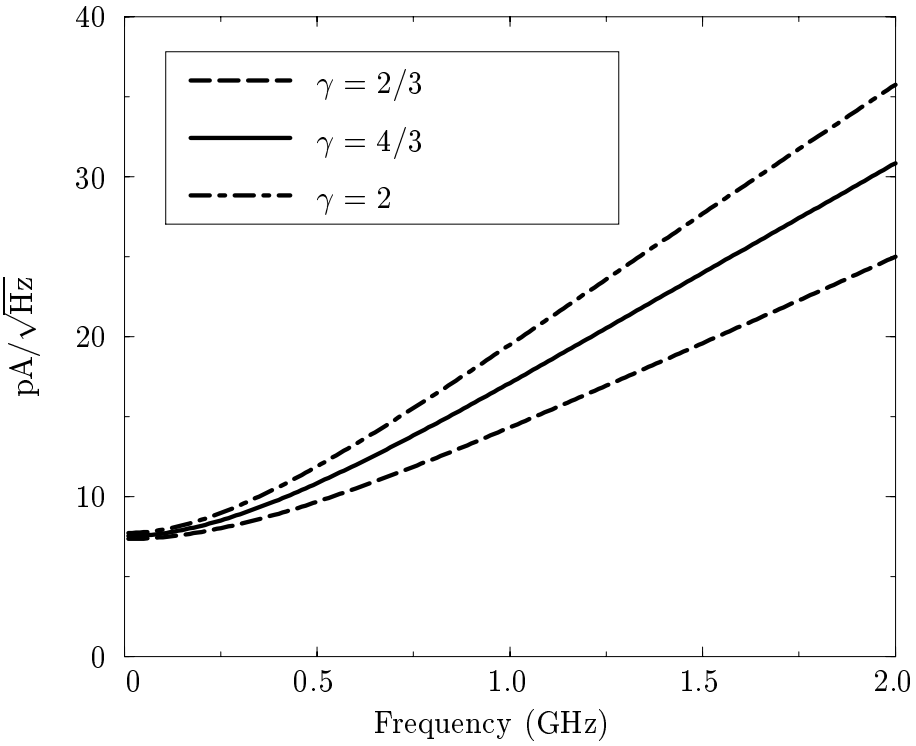
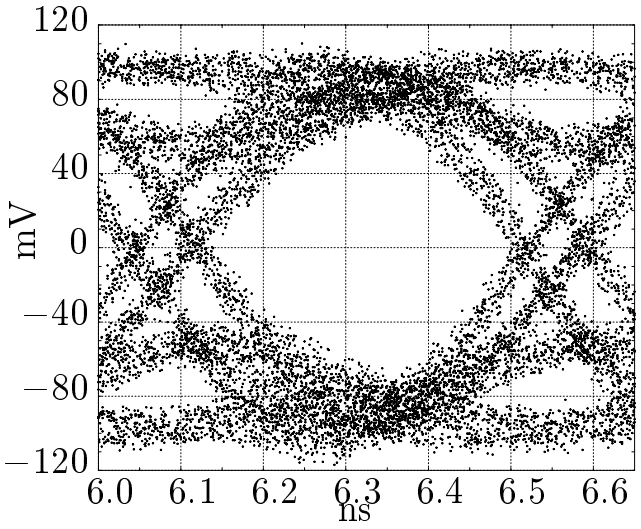


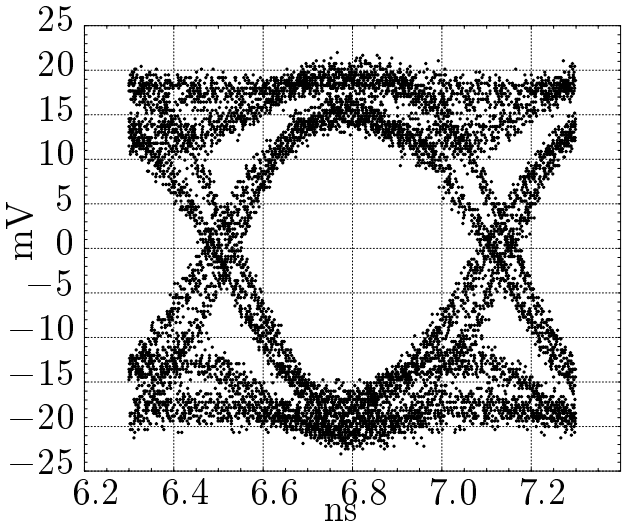
Figure C.10: Input referred current noise density

channel thermal noise (γ) is varied from 2/3, the long-channel value, to 2, to discern the degradation in sensitivity due to excess noise in short channel devices. The worst case value of 2 predicts an input referred current noise of 0.6μA, a significant degradation from the 0.4μA predicted by long-channel estimates.

Figure C.11(a) and Figure C.11(b) display the measured single-sided output eye diagrams for operation at 2.1 and 1.6 Gbaud respectively. An open eye is obtained for single-sided output voltages extending from 4mV to 500mV. Table C.1 summarizes the performance of the prototype chip.



(a)



(b)

Figure C.11: Measured output eye diagrams (a) at 2.1Gbaud, and (b) at 1.6Gbaud.

Transimpedance (small-signal)	1600Ω (differential)
	800Ω (single-ended)
Bandwidth (3dB)	1.2GHz
Max. photodiode capacitance	0.6pF
Max. input current	1.0mA
Simulated input noise current	0.6μA
Max. output voltage swing	1.0V_{pp} (differential)
(50Ω load at each output)	0.5V_{pp} (single-ended)
Power consumption	115mW (core)
	110mW (50Ω driver)
Die area	0.6mm^2
Technology	0.5μm CMOS

Table C.1: Performance summary

C.8 Summary

This appendix presented an area and power efficient technique for boosting the bandwidth of broadband systems using optimized on-chip inductors as shunt-peaking elements. These bandwidth extension and circuit optimization techniques were applied in the implementation of a 2.125Gbaud, 1.6kΩ differential transimpedance preamplifier with an equivalent input current noise of 0.6μA. The chip has a die area of 0.6mm^2, of which less than 15% is consumed by the two inductors. Designed in a triple metal, single poly, 0.5μm CMOS process, this chip was intended as a test vehicle to demonstrate how on-chip bandwidth extension techniques can push the limits of low-cost CMOS processes. To the best of our knowledge, this chip is the first CMOS implementation that uses planar spiral inductors as shunt-peaking elements.

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