

# Practical Dynamic Element Matching Techniques for 3-level Unit Elements

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# Outline

- Brief background
  - Motivations and Applications
  - 3-level vs. 2-level unit element: advantages and challenges
  - What problems DEM does and does not solve
- Practical dynamic element matching (DEM) techniques
  - 2-level DEM review
  - 3-level DEM
  - Limitations of each technique
  - Solution spaces
- Higher-order DEM
  - Issues in 2<sup>nd</sup>-order DEM
  - Solutions
- Application specific concept of DEM
  
- Q and A

# Applications of 3-level unit elements

Safety radar



In cabin ANC



Active Noise Cancelling (ANC)



# What is Dynamic Element Matching?

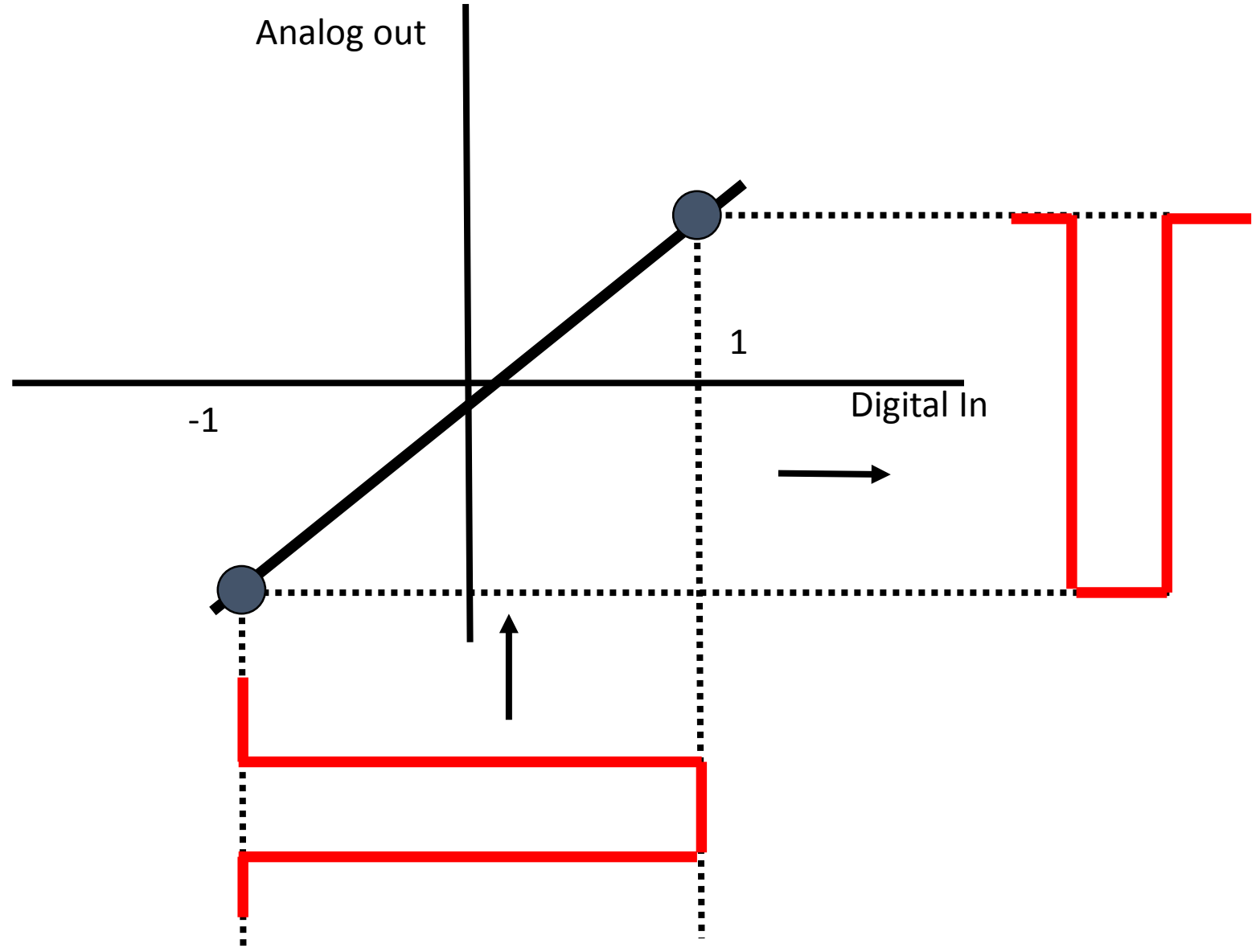
- A technique to achieve perfect matching of analog elements ***over time***.

# Euclid's 5<sup>th</sup> definition for plane geometry

“Through a pair of points in space, there exists one and only one straight line”

# What it means in the converter world ....

- Can achieve “perfect linearity” if the circuit output has only 2 states



Year 1995 .....



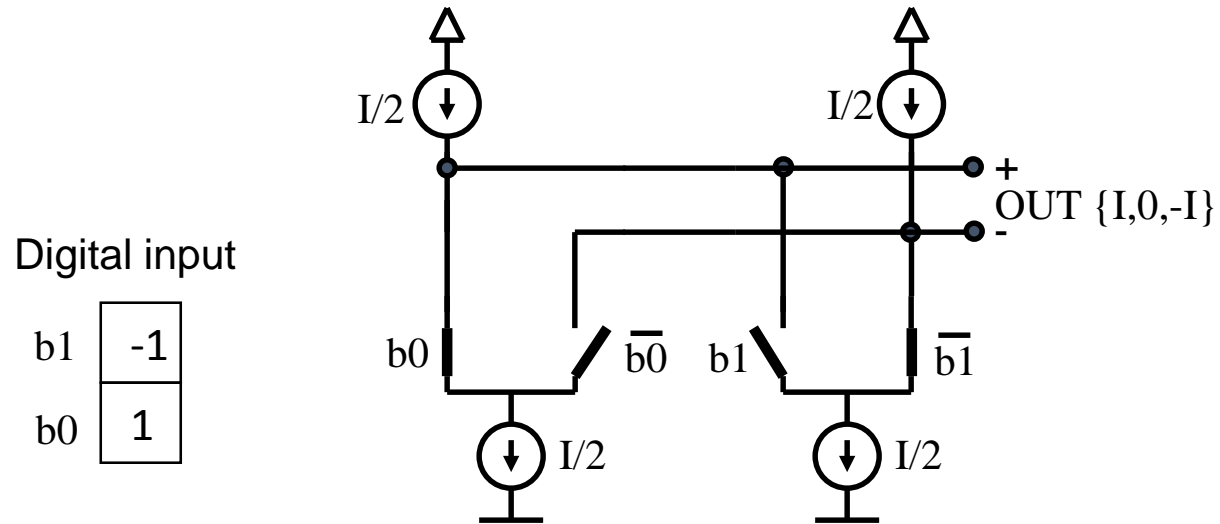
The "Perfect DAC" !

# Why multi-bit ?

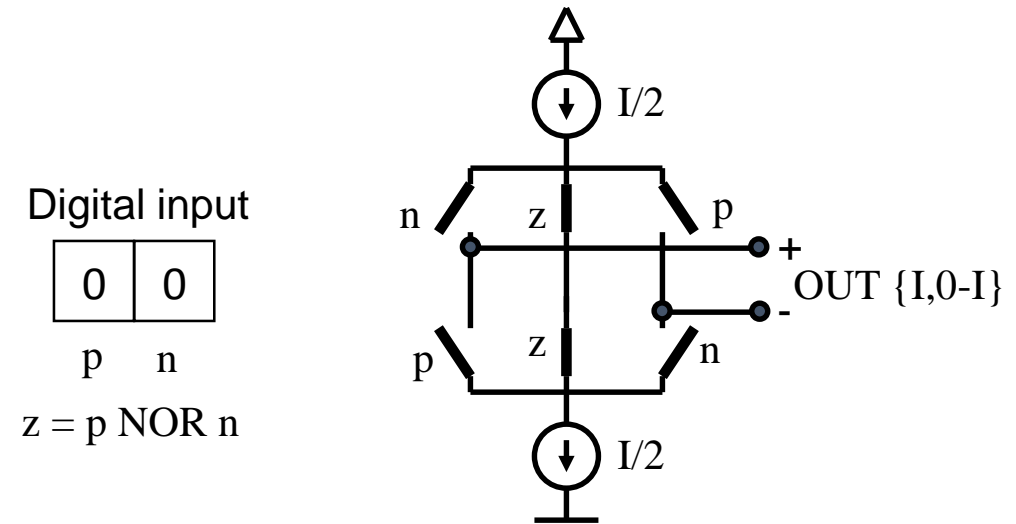
- Drawback of single-bit
  - High out-of-band noise → Requires stringent post-analog filter → costly, bulky
  - Limited usable input range with high-order noise shapers → Challenging to improve dynamic range
  - Stringent bandwidth and slew rate requirements for reconstruction amplifier → Challenging to reduce power consumption
- Multi-bit
  - Solves all the above but introduces linearity issue due to element mismatch → Mismatch shaping is the remedy
    - Each element is 2-level
- ***Why 3-level element ?***



# Current steering DAC cell comparison



a) 2-level element architecture



b) 3-level element architecture

- **3-level element properties**

- + Power efficient

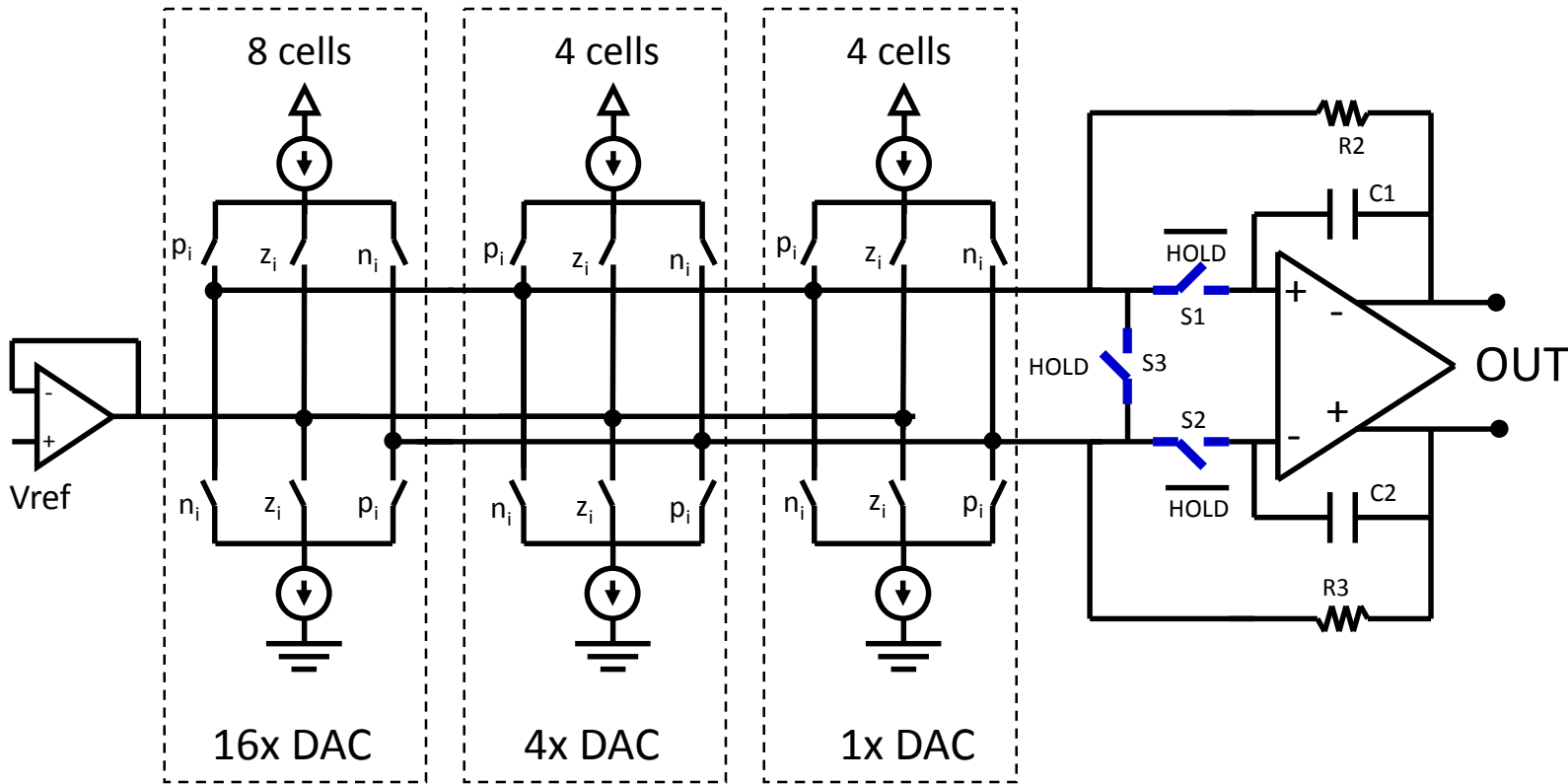
- + Best noise performance: No noise contribution in the “zero” state.

- ***Needs a new dynamic element matching logic***

- Needs a low power solution for ISI problem

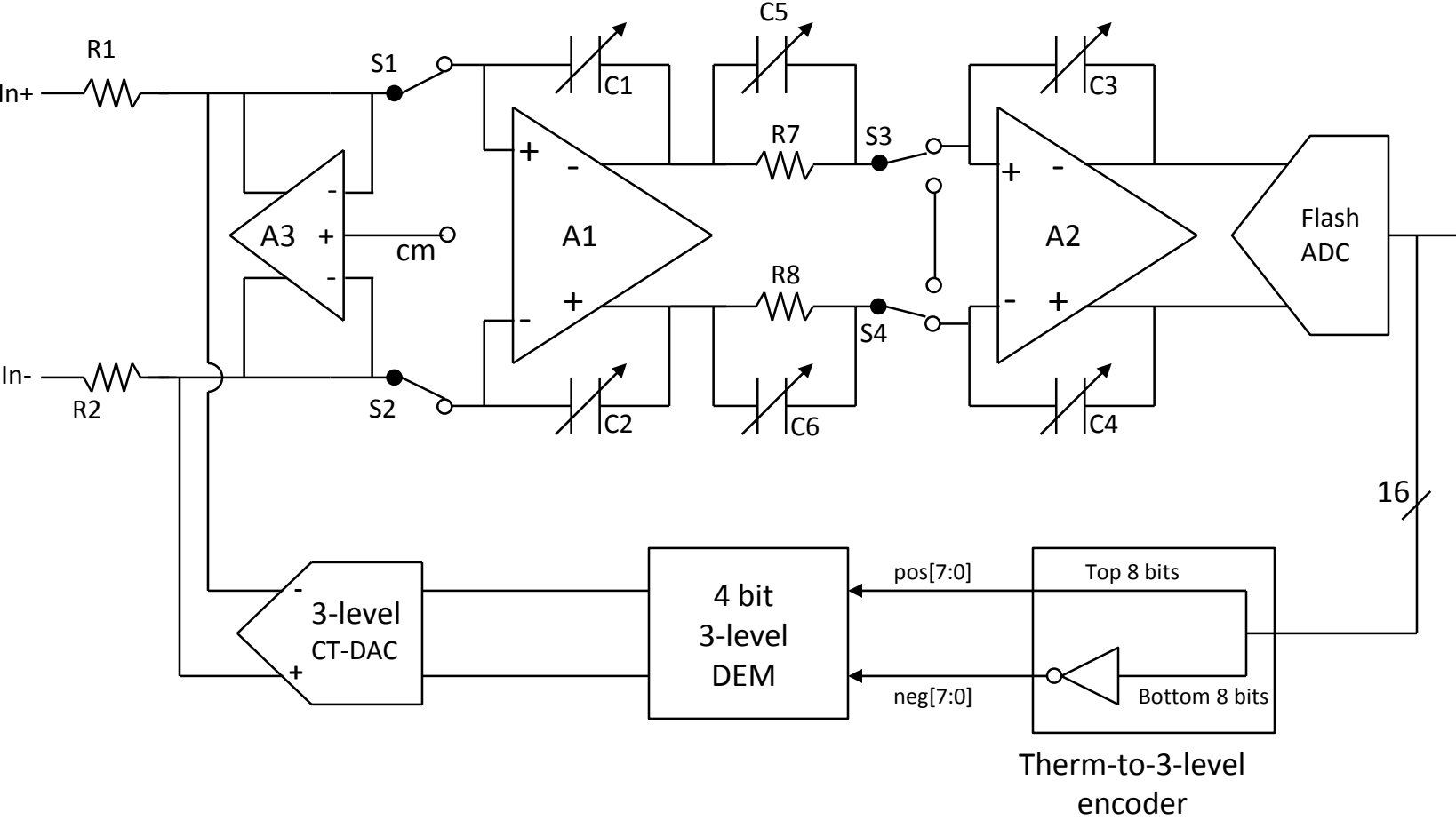
- Drain voltage modulation degrades THD

# Example 1: High performance $\Sigma\Delta$ audio DAC



<b>Process</b>	<b>0.18<math>\mu</math>m CMOS</b>
<b>Supply</b>	<b>1.8 V</b>
<b>Full scale differential output</b>	<b>0.9 V<sub>rms</sub></b>
<b>Digital power consumption</b>	<b>0.4 mW / channel</b>
<b>Analog power consumption</b>	<b>0.7 mW / channel</b>
<b>OSR</b>	<b>64</b>
<b>Clock frequency</b>	<b>3.072 MHz</b>
<b>SNR (A-weighted)</b>	<b>108 dB</b>
<b>THD+N</b>	<b>-97 dB</b>

# Example 2: High performance $\Sigma\Delta$ audio ADC



<b>Process</b>	<b>0.18<math>\mu</math>m CMOS</b>
<b>Supply</b>	<b>3.3 V</b>
<b>Digital power consumption</b>	<b>0.4 mW / channel</b>
<b>Analog power consumption</b>	<b>2 mW / channel</b>
<b>OSR</b>	<b>128</b>
<b>Clock frequency</b>	<b>6.144 MHz</b>
<b>SNR (A-weighted)</b>	<b>111 dB</b>
<b>THD+N</b>	<b>-97 dB</b>

# 3-level element in $\Sigma\Delta$ ADC

- Additional advantages:
  - Minimum noise contribution from current steering DAC at low level signal (below -60dB full scale)
  - Equivalent to a current noise from a large resistor  $R$ ,  $i_N = \sqrt{4kt/R}$ 
    - I-DAC current noise is not the dominant source anymore
  - Dominant noise sources : input  $R$  and amplifier
    - For the same SNR target : Larger allowable  $R \rightarrow$  Smaller integration capacitor size  $\rightarrow$  Silicon area saving
  - Less switching activity at low level  $\rightarrow$  Less spectral leakage due to ISI
- Cautions
  - Signal dependent switching activity  $\rightarrow$  A source of harmonic distortions
  - Slight noise modulation due to signal amplitude

# DEM: What it does and does not solve

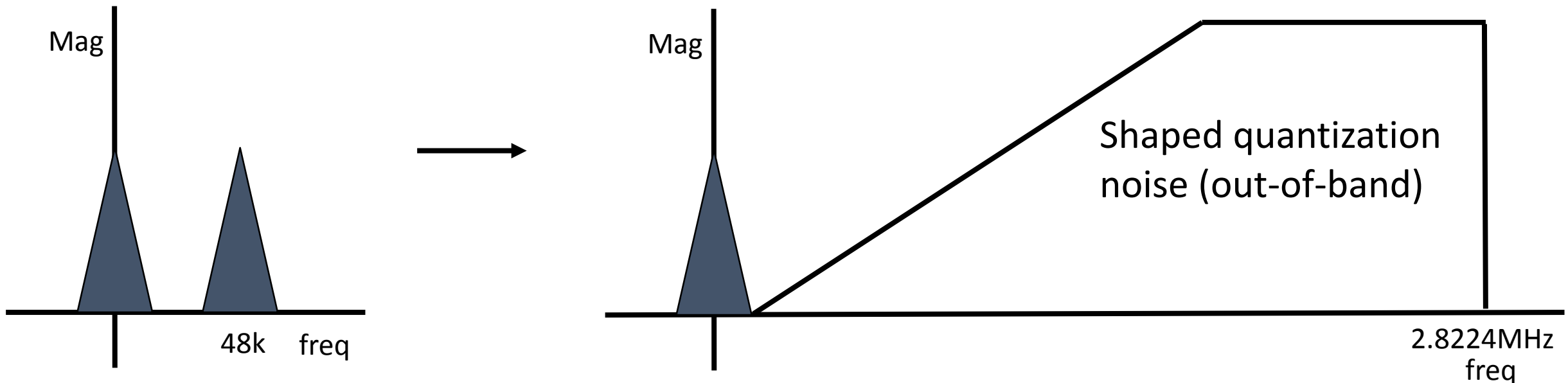
- Solves
  - Cell-to-cell static mismatch (born or due to aging)
    - Between the +1s' and the -1s'
  - 1/f noise of cells
- Does not solve
  - Magnitude error between "+1" and "-1" of a single cell
    - Circuit design technique exists as remedy for this issue
  - Cell-to-cell mismatch due to switching dynamics

# Recap

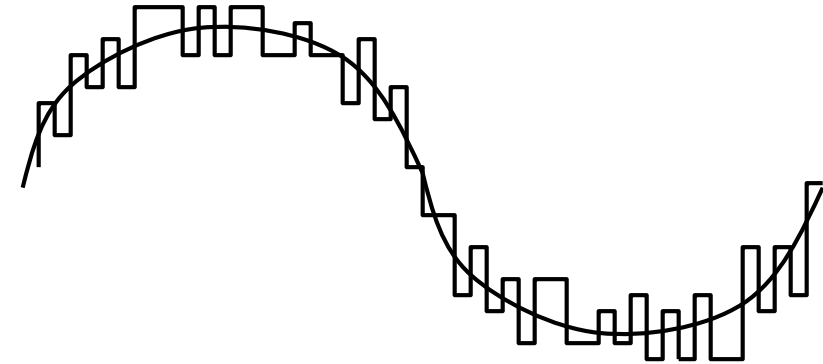
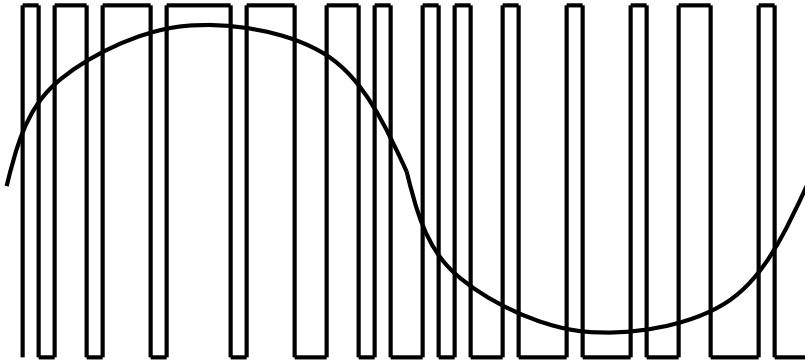
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  - Motivations and Applications
  - 3-level vs. 2-level unit element: advantages and challenges
  - What problems DEM does and does not solve
- **Practical dynamic element matching (DEM) techniques**
  - 2-level DEM review
  - 3-level DEM
  - Limitations of each technique
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- Higher-order DEM
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# Review: Noise shaping concept

- High precision multi-level analog quantity is “difficult” to reconstruct
- Noise shaping: Trade off frequency band usage for word-width
  - 16b @ 44.1kHz  $\rightarrow$  1b at 5.6488MHz



# 1-bit versus multi-bit DAC



## ◆ 1-bit Advantages

- Linear – no matching issue

## ◆ 1-bit problems

- Large step size → jitter sensitivity
- Tonal quantization noise can cause “idle tones” (quantizer can't be dithered properly)
- High-order loops become unstable with large inputs

## ■ Multi-bit advantages

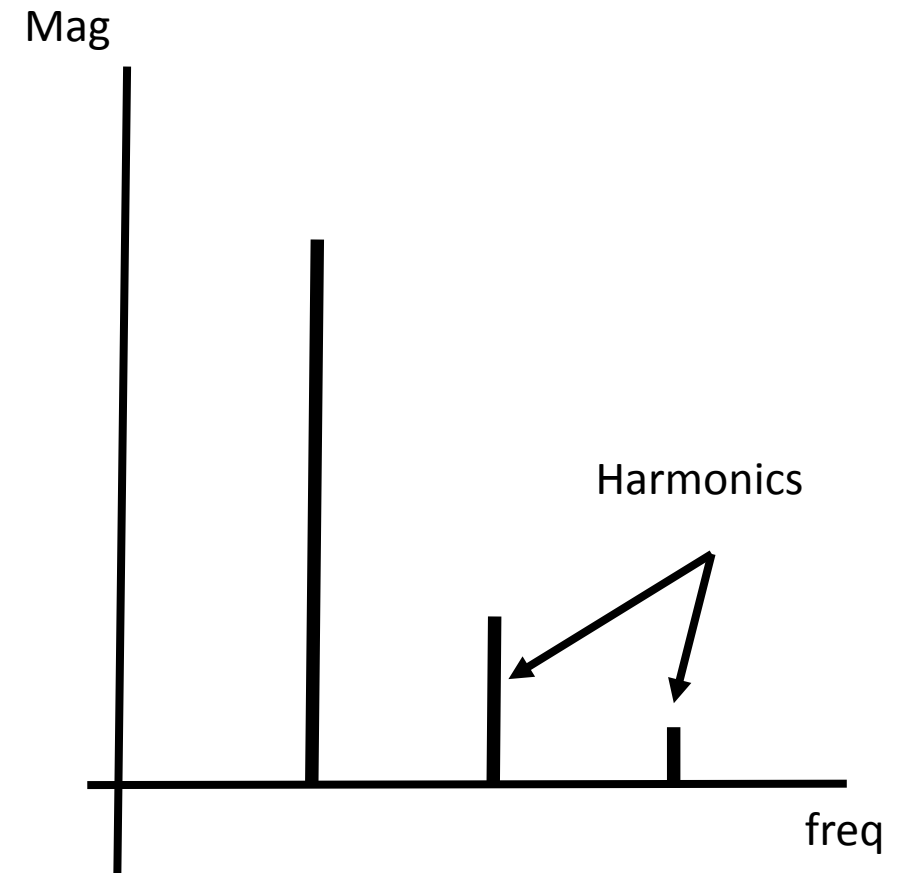
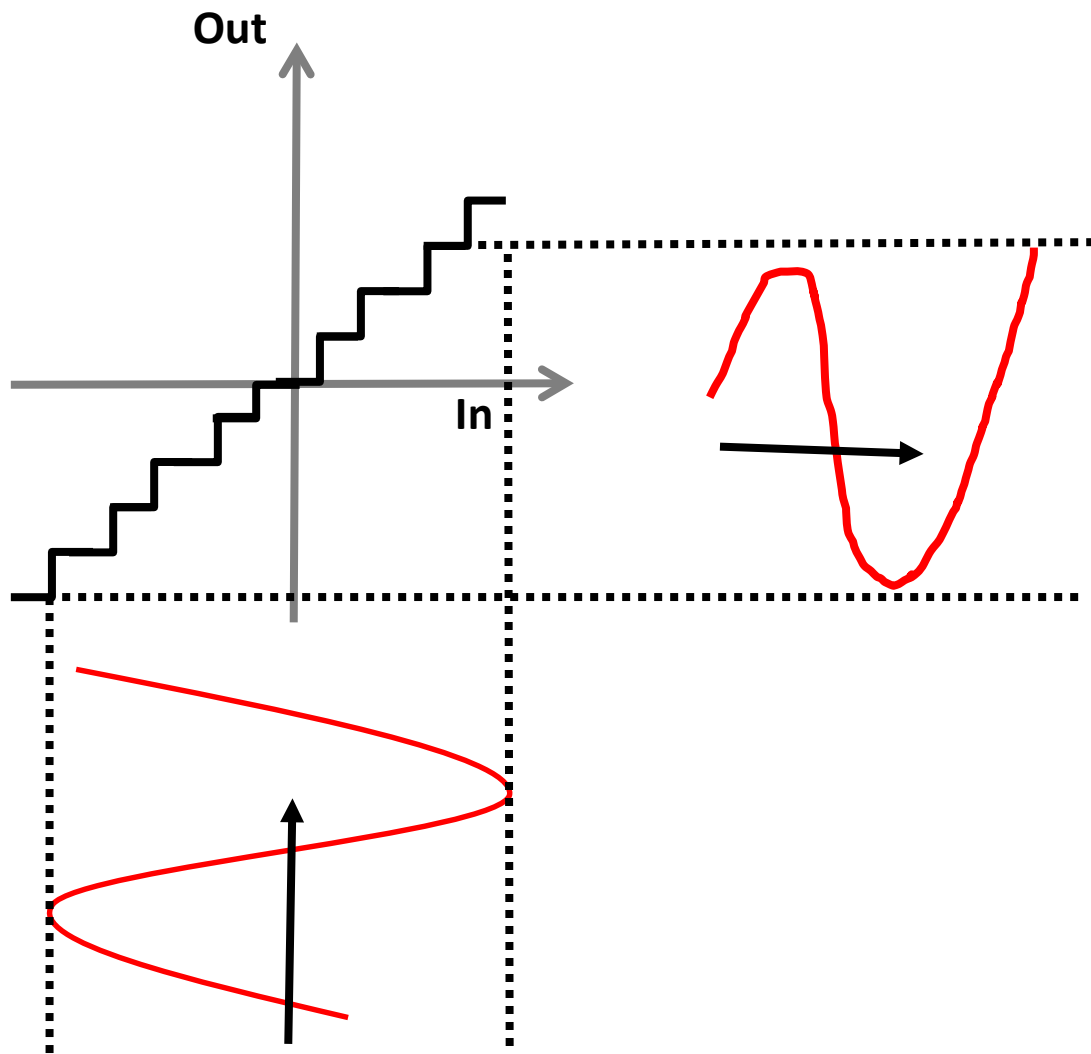
- Tone-free quantization noise (can be dithered)
- Lower-order loops can often be used (easier stability)
- Small steps (low jitter sensitivity, less filtering required)

## ■ Multi-bit problems

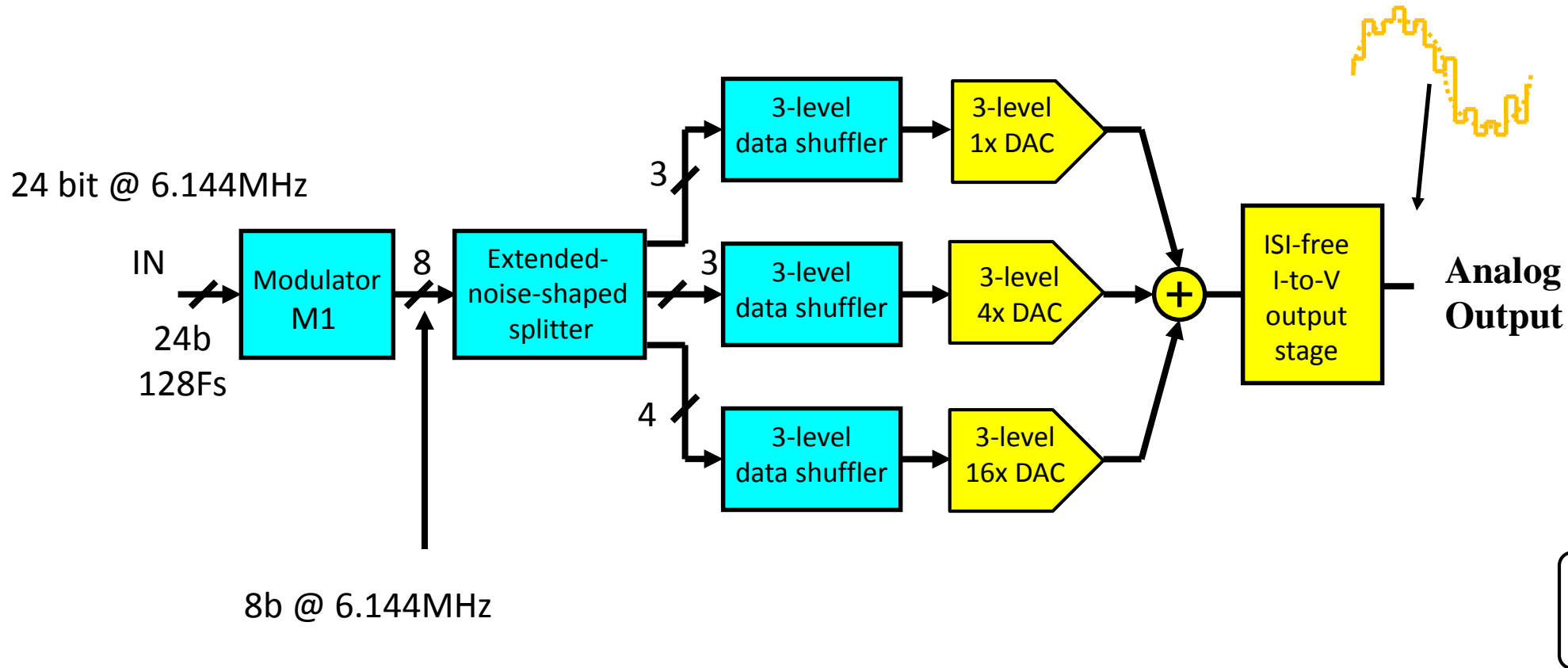
- Matching; DAC element errors cause distortion + noise



# Multi-bit with element mismatch



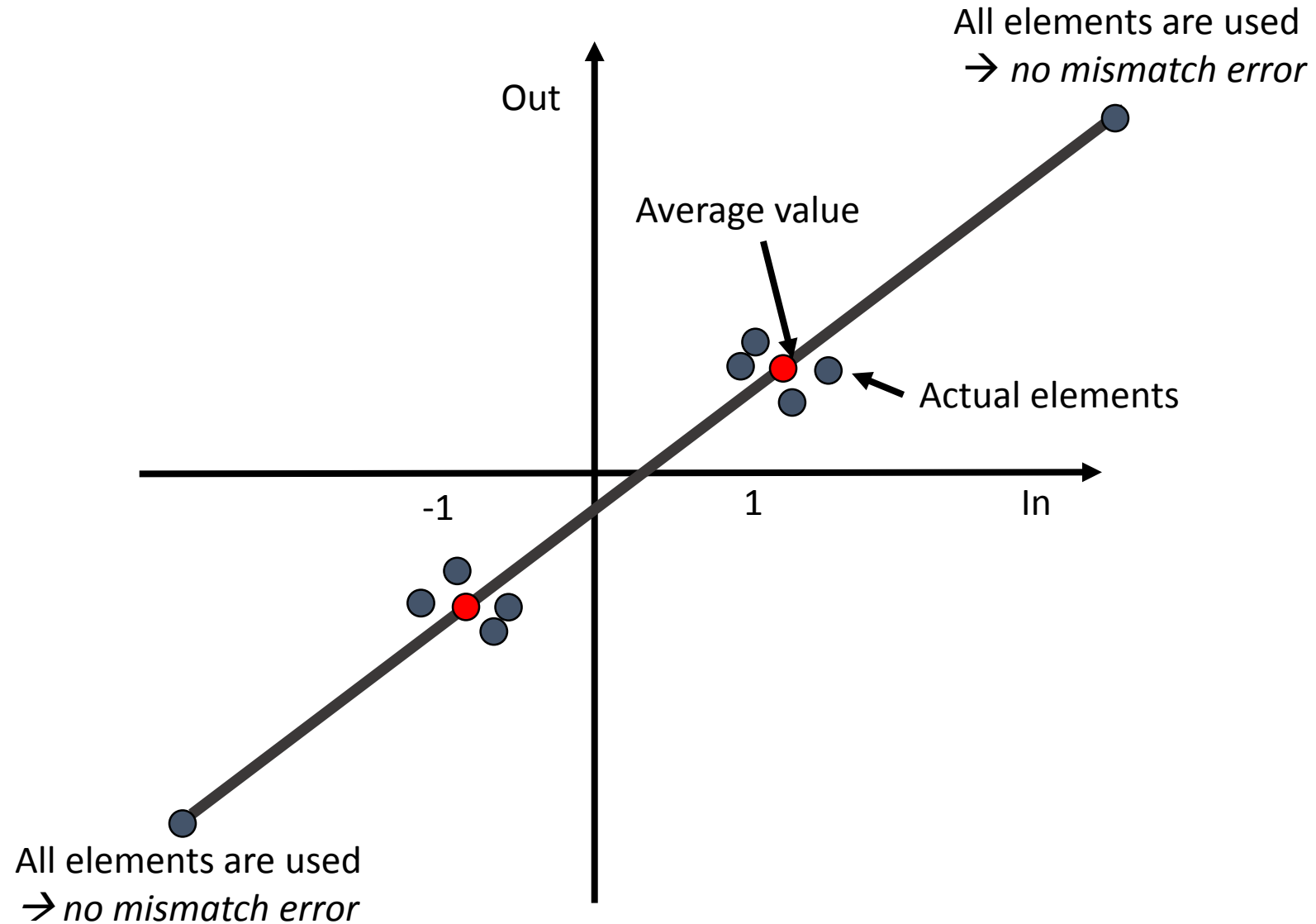
# Example of multi-bit audio DAC



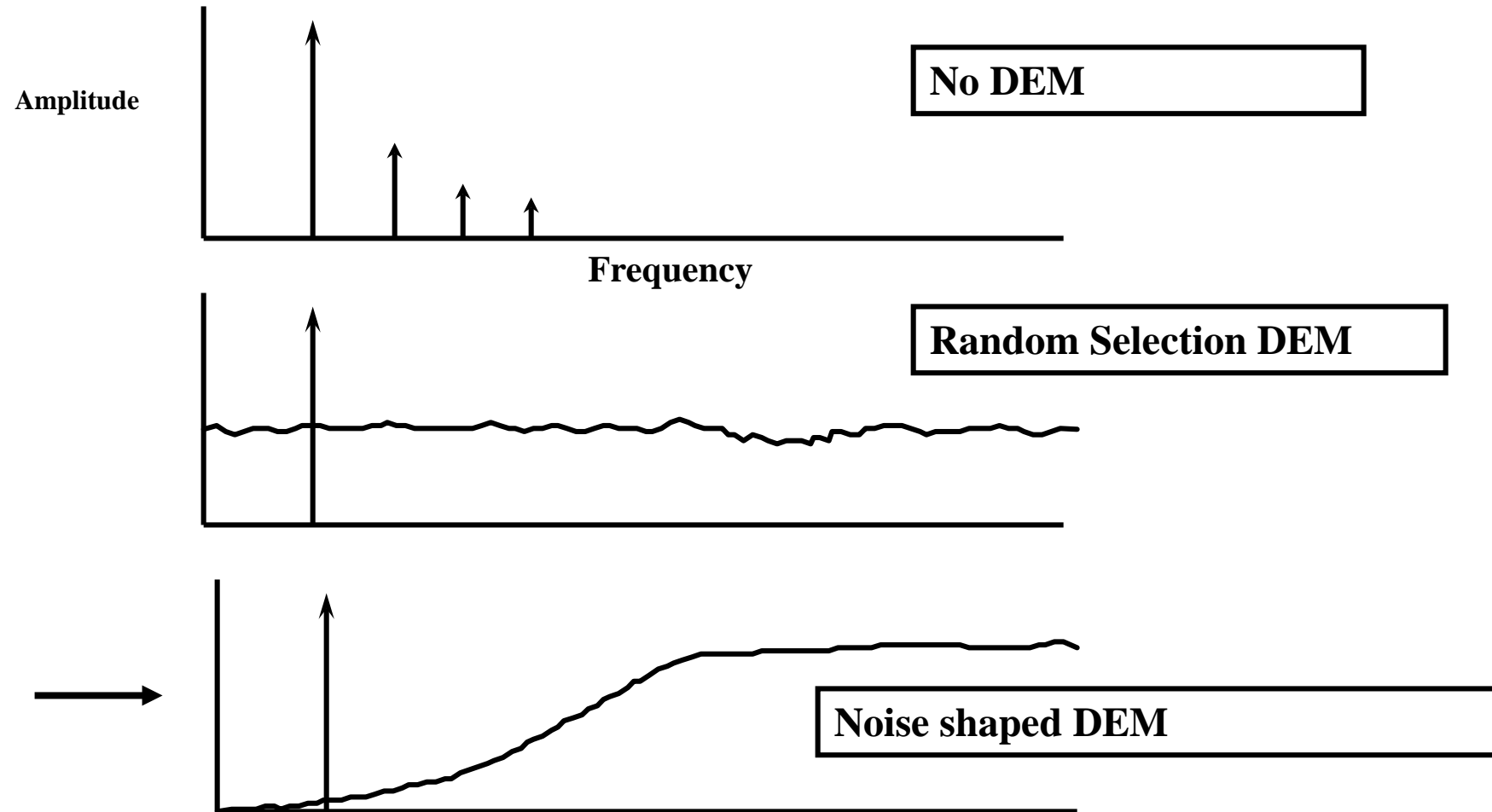
# The essence of DEM

- Linearizing the transfer function
  - Making each element appears as average value → Reconstructed values are “perfectly” linear **in the band of interest**
- Requirements
  - Use thermometer coded data (**uniformly weighted elements**)
  - Must have multiple ways (**redundancy**) to reconstruct any value
  - Have an “out-of-band” region to push shaped mismatch errors to. i.e., **oversampling ratio larger than 1 (practical OSR  $\geq 16$ )**

# Multi-bit transfer function



# Spectral contents with and without DEM



# Approaches to 2-level unit element DEM

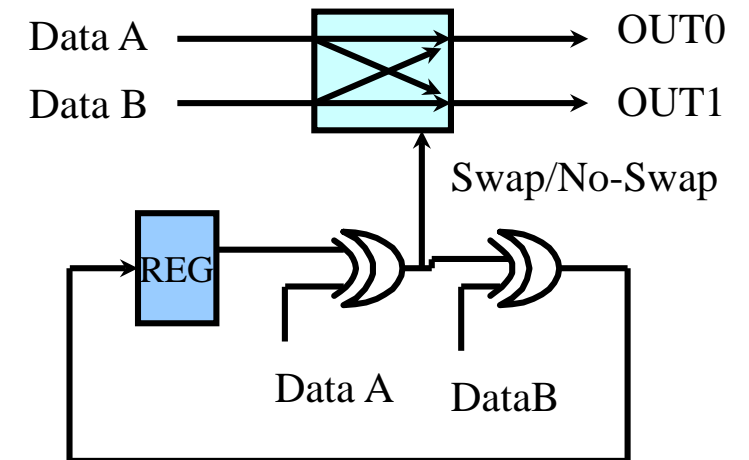
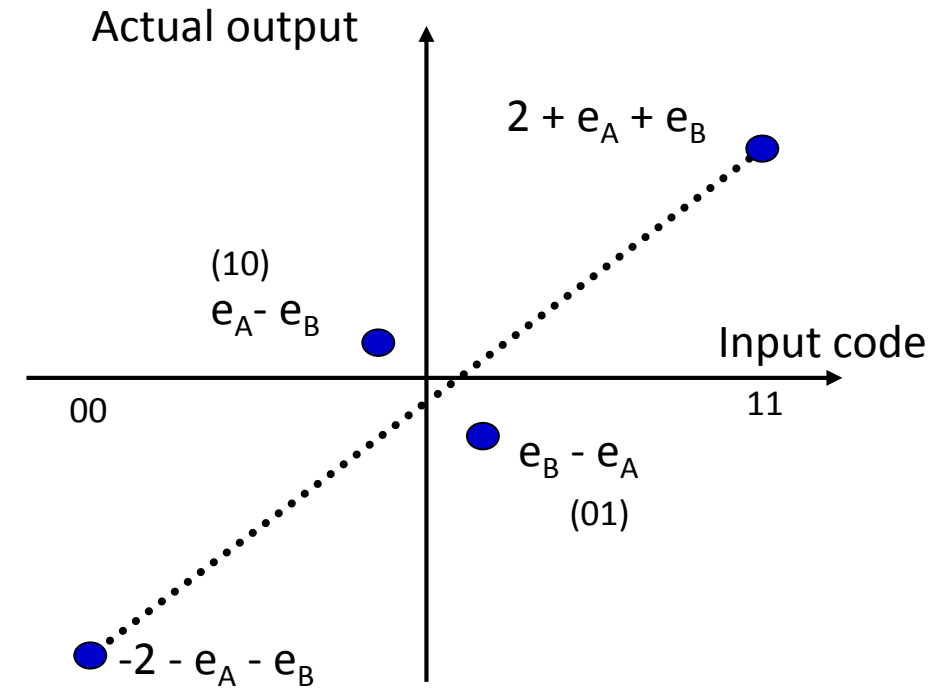
1. Data directed
2. Rotational
3. Tree structure
4. Vector quantization
5. Real-time

# 1. Data directed shuffling

- Consider a 2-bit thermometer code DAC
  - Cell A =  $1 + e_1$
  - Cell B =  $1 + e_2$

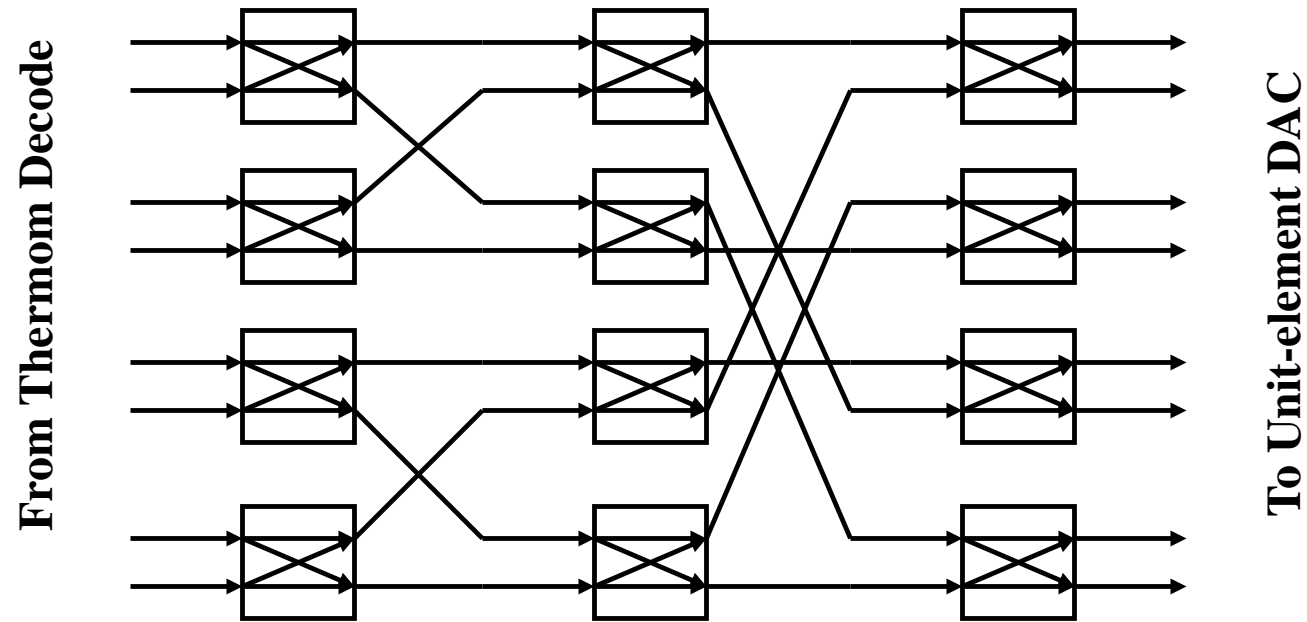
AB	Out	Instantaneous error (ei)
00	$-(2+e_1+e_2)$	0
01	$-e_1 + e_2$	$-e_1+e_2$
10	$e_1 - e_2$	$e_1-e_2$
11	$2+e_1+e_2$	0

- Goal: Make the cumulative error approach zero.
  - Done by alternating use of OUT1 and OUT2 when  $A \neq B$



Swapper cell

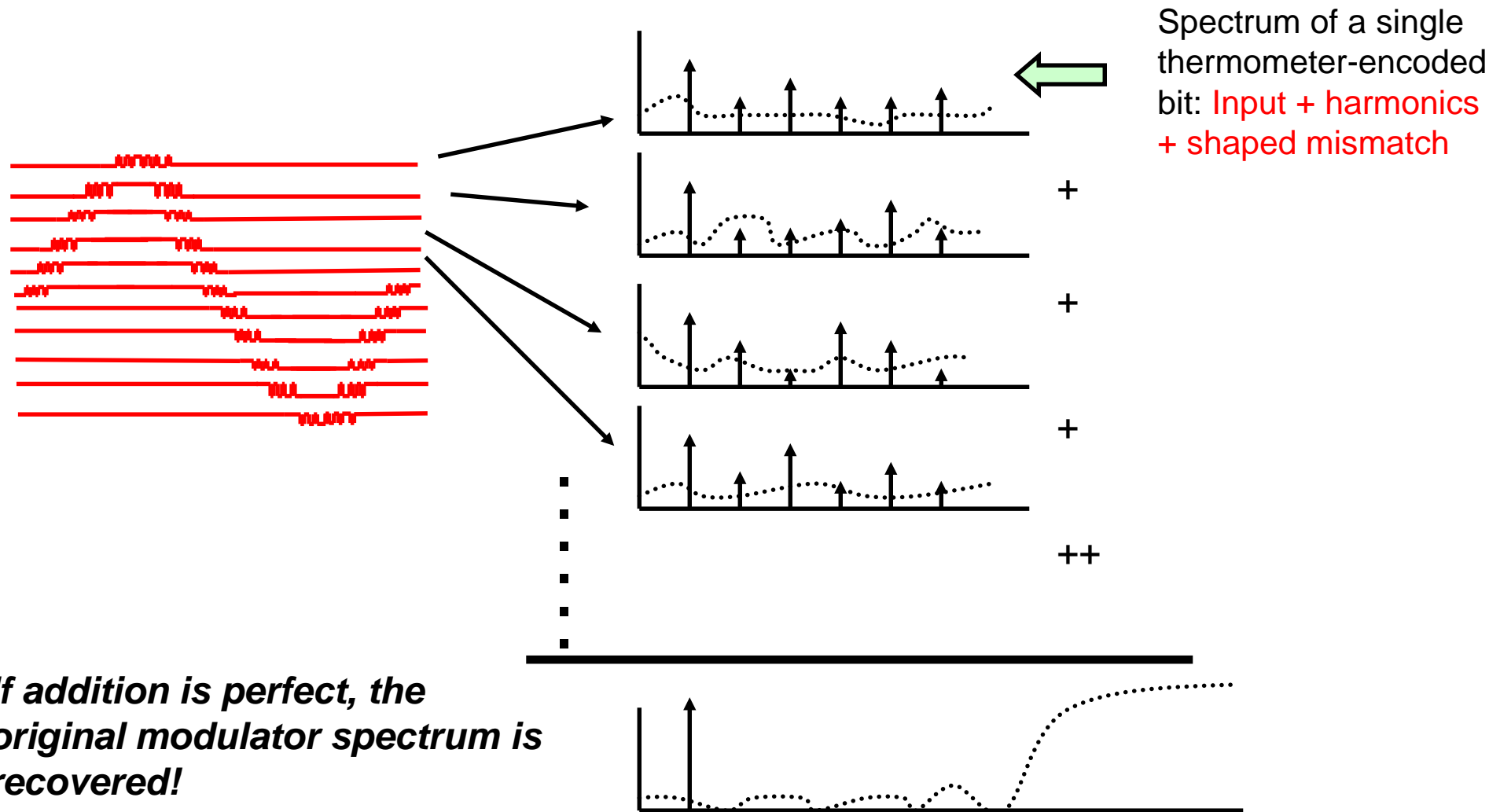
# How to make a multi-bit shuffler



- Butterfly network works as “usage” correlator
- Every input can reach every output
- Decision to swap is made by swapper cell

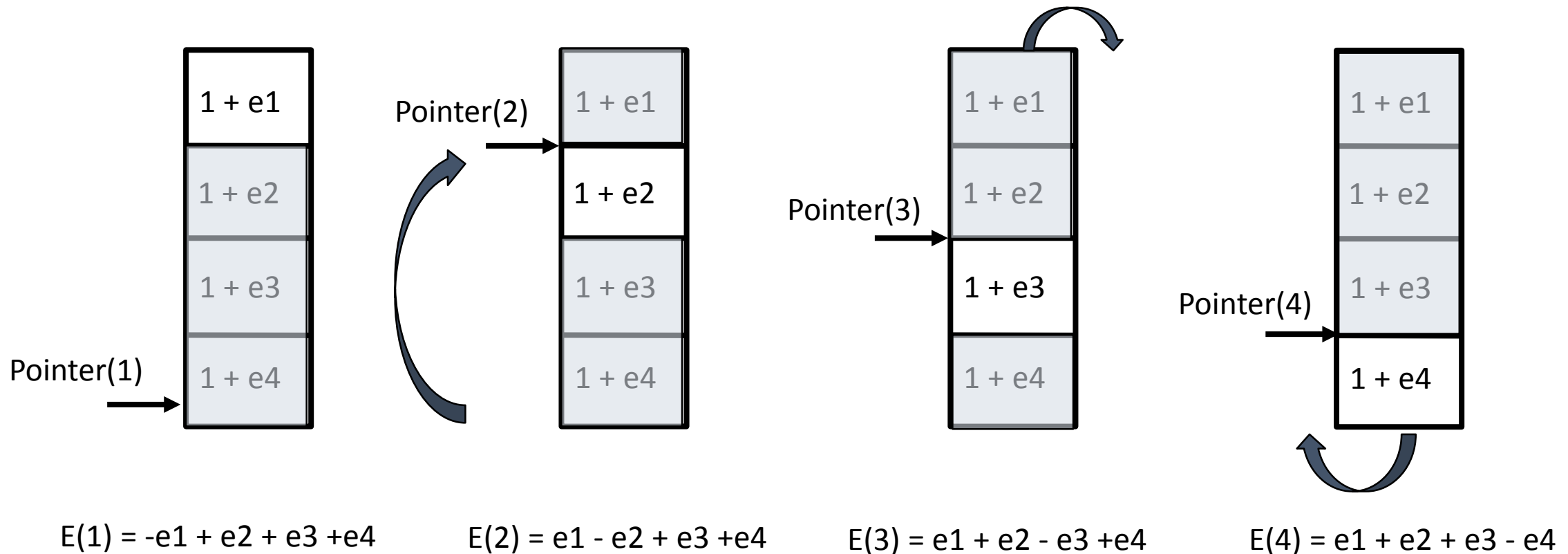


# Spectral view of mismatch shaping



## 2. Rotational DEM

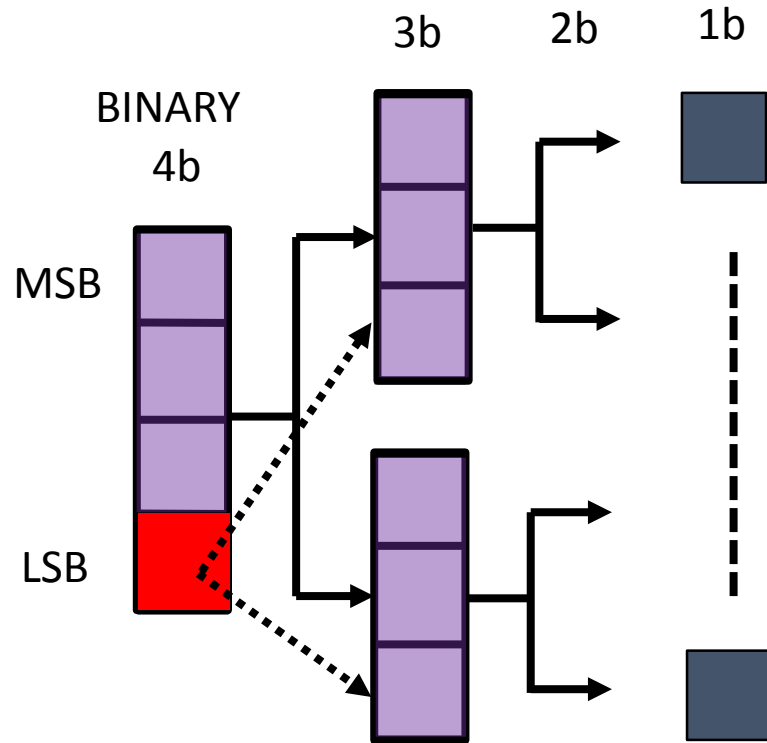
- Example: Digital in = 1, element selection in 4 clock cycles



◆ Cumulative error after 4 cycles =  $2(e_1 + e_2 + e_3 + e_4)$

◆  $(e_1 + e_2 + e_3 + e_4)$  : all elements are used equally  $\rightarrow$  cumulative error = zero!

# 3. Tree structure DEM



## ◆ DEM algorithm

- Start with N-bit binary word
- Divide by 2 ( shift left by 1)
- If LSB = 1, use  $\Sigma\Delta$  modulator to decide which sub-word to receive the LSB
- Update modulator

## ◆ Observation

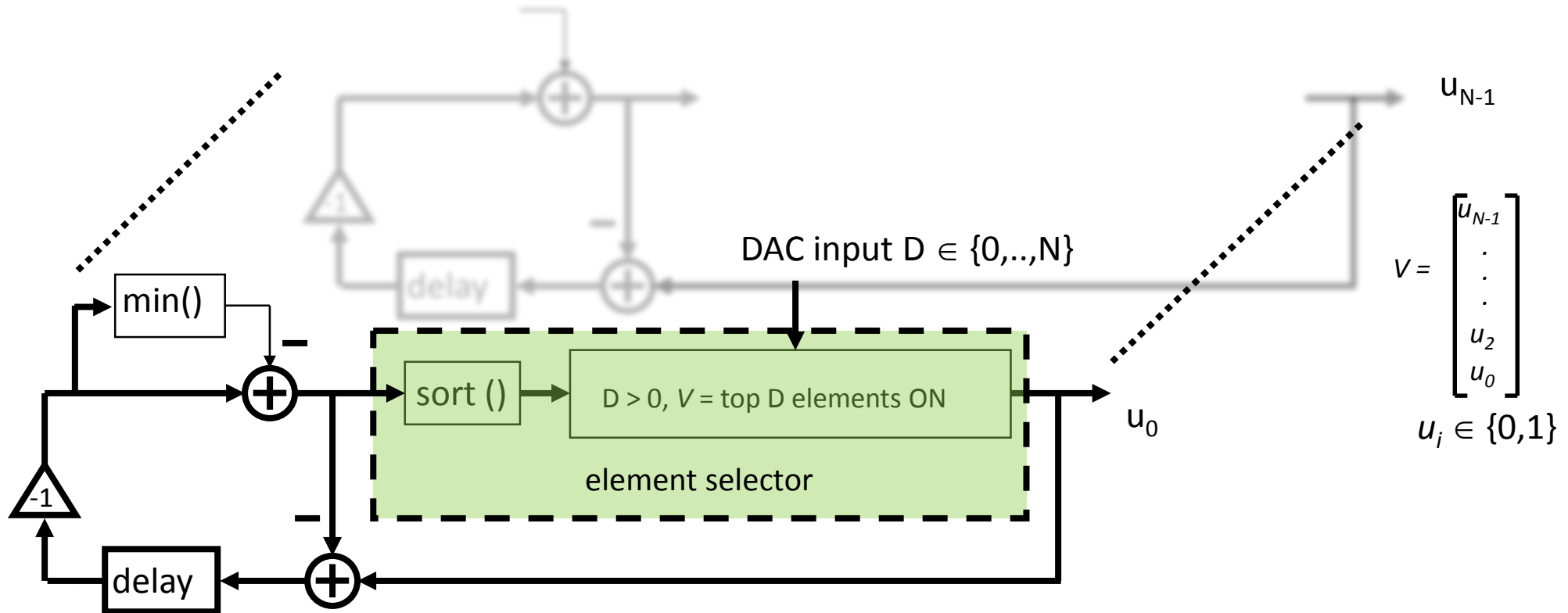
- **Difference between 2 words is a noise shaped sequence** → Gain mismatch is high-passed

## ◆ Note:

- Needs headroom to not overflow
- Works fine for first-order shaping, what happens if input is EVEN for a while!

# 4. Vector quantization

- Generalized version of all DEM algorithms → Excellent model to study DEMs
- Hardware intensive

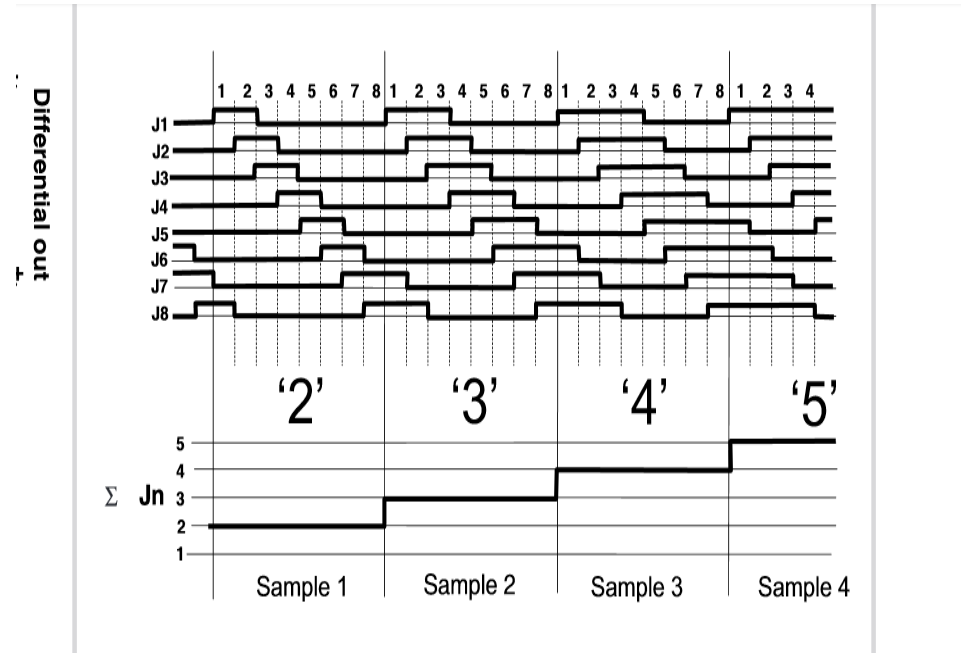


Example of a 1<sup>st</sup>-order DEM (using the error feedback  $\Sigma\Delta$  structure)

# Element selection logic

- Rank N input vectors with least used first
- Turn on (assert “1”) D output elements in output vector V
- Feedback the elements of V to the corresponding integrators (or loops)
- Can apply the use of a dithering vector to the input of the sorting routine to cure idle tone behavior

# 5. Real-time DEM



- Use all elements in every modulator clock cycle
  - Advantage:
    - Very simple logic
  - Drawbacks:
    - Need a fast clock ( $2^N$  times) for an N-bit DAC
    - Cannot go beyond 1<sup>st</sup>-order shaping

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# Approaches to 3-level unit-element DEM

1. Data directed shuffling
2. Rotational
3. Tree structure
4. Vector quantization

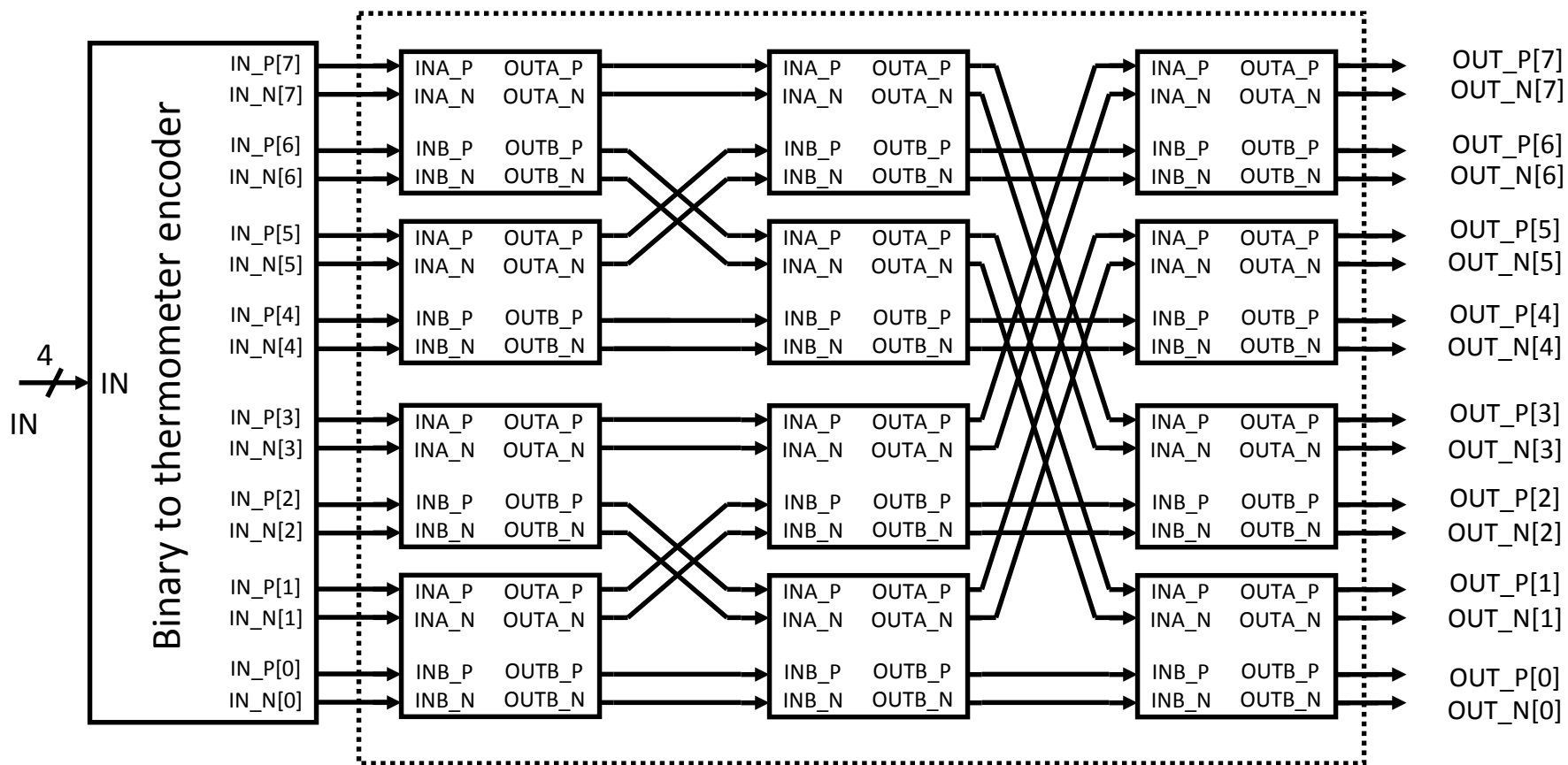


# Encoding style for 3-level data

- Best to treat data as **positive and negative thermometer codes** separately
- Results in simplest logic manipulation and decoding logic in the current steering cells
- Truth table

Positive thermometer code	Negative thermometer code	Analog value
1	0	+1
0	1	-1
0	0	0
1	1	Unused

# Approach #1: Data directed shuffling

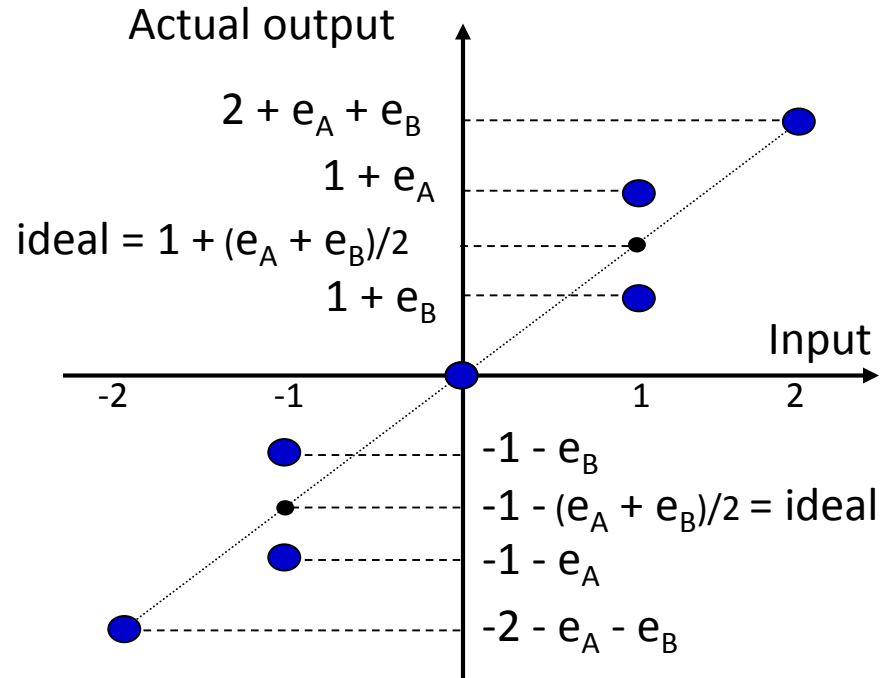


A 4-bit example

- Butterfly network serves as the usage correlator

$$\# \text{ of cells} = \frac{N}{4} \log\left(\frac{N}{2}\right), \text{ for } N + 1 \text{ output levels}$$

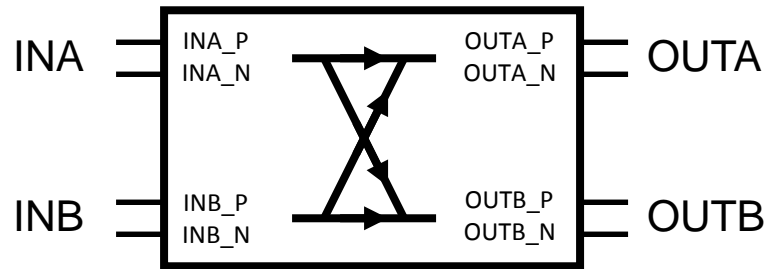
# 3-level mismatch error analysis



Transfer function of a DAC formed by a pair of analog elements A and B

- $e_A$  and  $e_B$ : individual error of element A and B
- Error delivered:
 
$$\text{Ideal} - \text{Actual} \in \begin{cases} (e_A - e_B)/2 \\ (e_B - e_A)/2 \\ 0 \end{cases}$$
- Goal: Select elements so that the long term average of each output level approaches its ideal value
- A 2b state machine to keep track of cumulative error

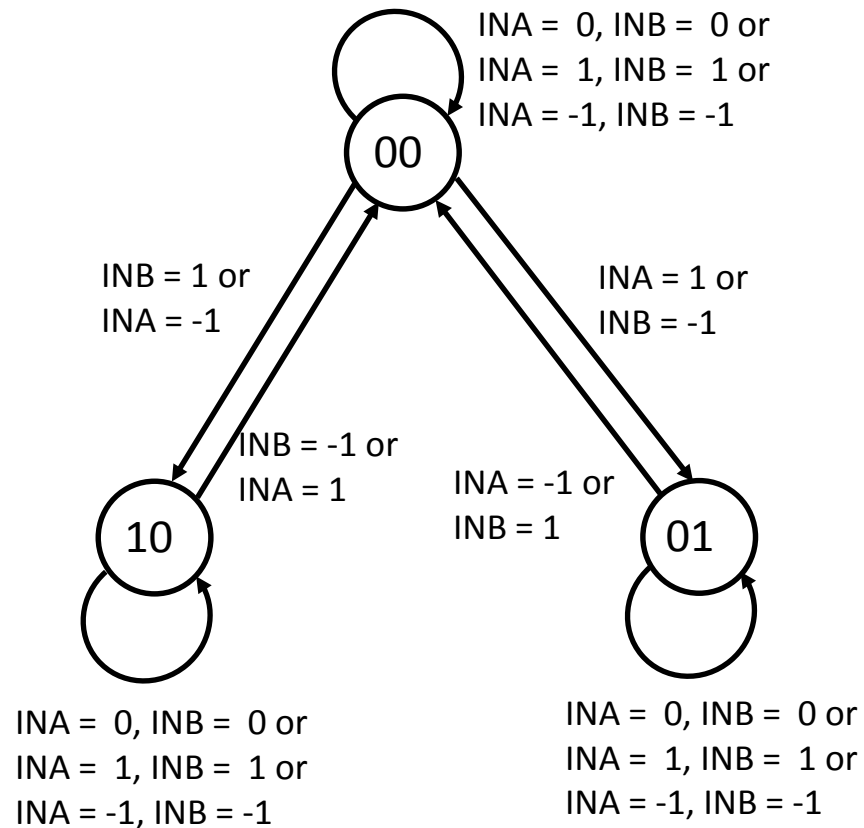
# Cell implementation



INA, INB, OUTA, OUTB are 2b quantities	
Value	Code (PN)
+1	10
-1	01
0	00
unused	11

- ◆ Output value =  $OUTA + OUTB$ ,  $\in \{-2, \dots, 0, \dots, 2\}$
- ◆ Simple modification of thermometer code
  - A and B always have the same sign
- ◆ Input can be rerouted to either output
- ◆ Needs a state machine

# State diagram

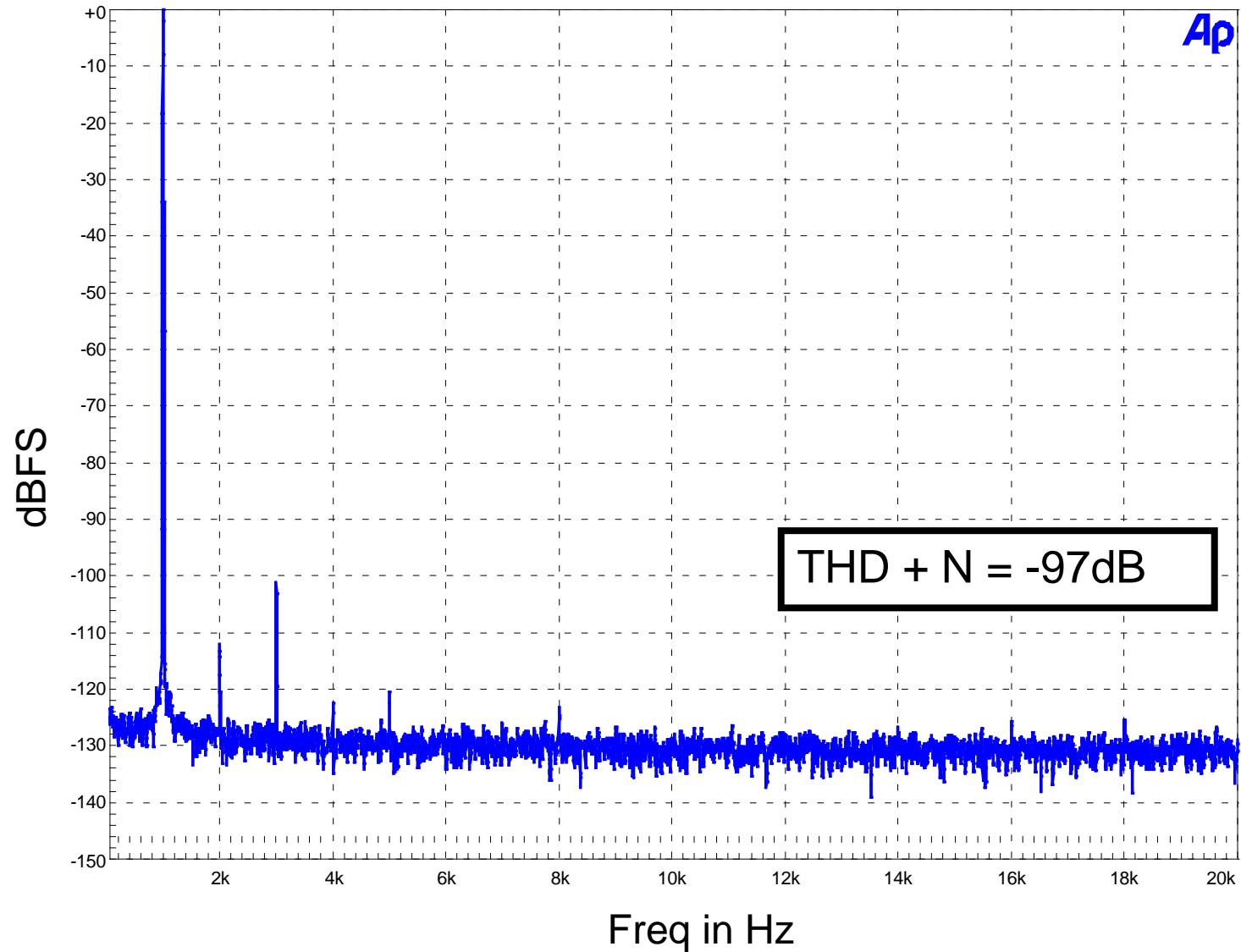


- Cumulative error:  
“00” : zero  
“01” :  $(e_B - e_A)/2$   
“10” :  $(e_A - e_B)/2$
- Apply the DEM rules to reroute data and keep cumulative error at zero
- The shuffler cell operates similarly to the generalized DEM model

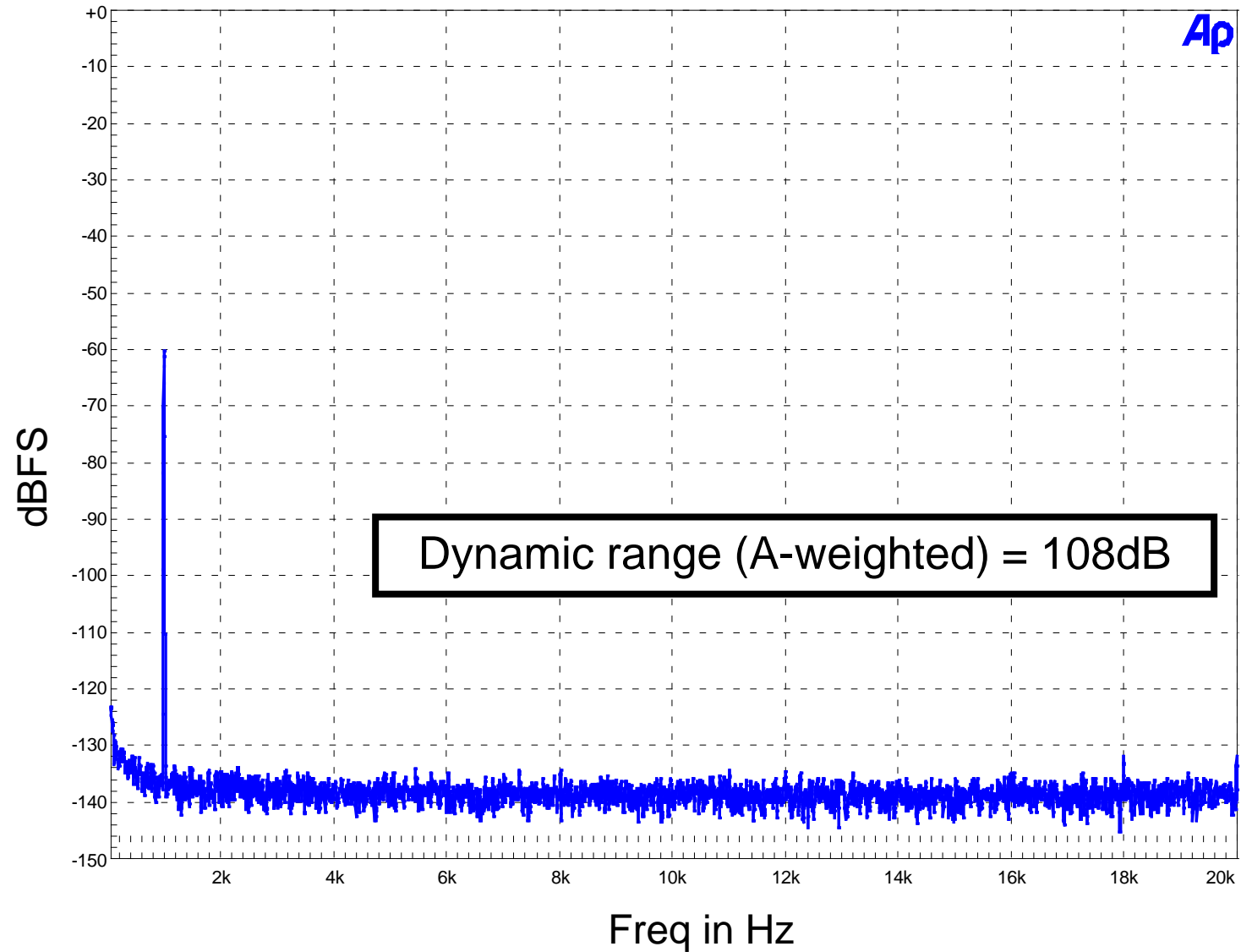
# Idle tones in first-order data-direct shuffling

- Reasons:
  - Each shuffling cell is a 1<sup>st</sup>-order noise shaper (can create large inband tones)
    - With gain mismatch between cells, these result in idle tones
  - At low level (below -60dBFS), input has a tendency to travel through only a certain path due to the construct of the butterfly network
  - At low level input, some cells in the network become “starve” in activity
  - Can be detected by sweeping the input amplitude with small DC range
- Remedy
  - Precede the shuffler network with a randomizer
  - Ensure that each cell will have equal amount of data activity over time
  - Mismatch shaping effectiveness is slightly degraded but still can perform very well with high OSR ( $\geq 64$ )

# Measured result ADAU1361 at -0.5dbFS



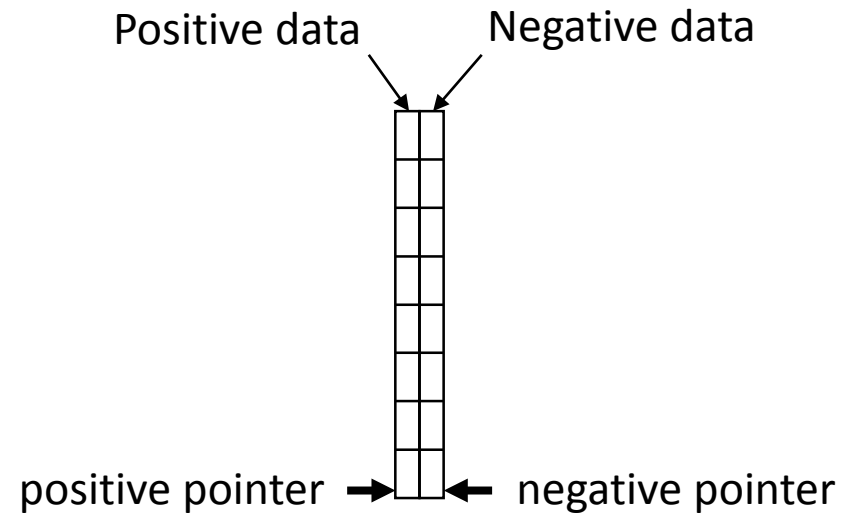
# Measured result ADAU1361 at -60dBFS



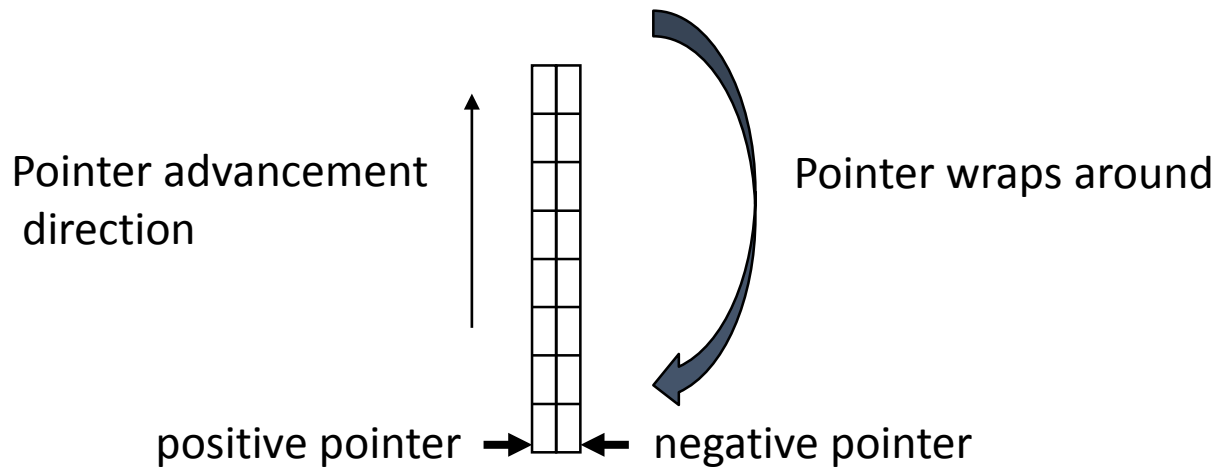


# Approach #2a: Dual-pointer Rotational DEM

- Use 2 separate pointers: one for positive and one for negative thermometer data
- Use the same encoding scheme previously shown

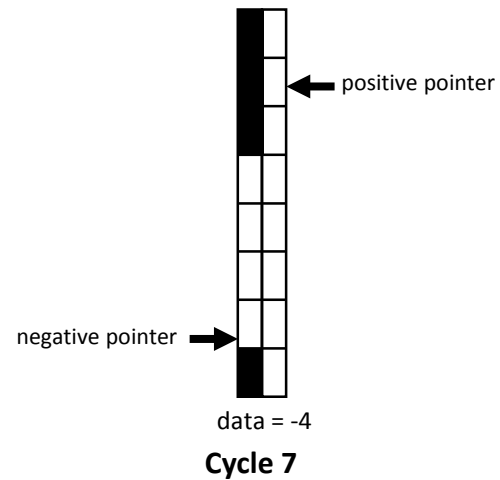
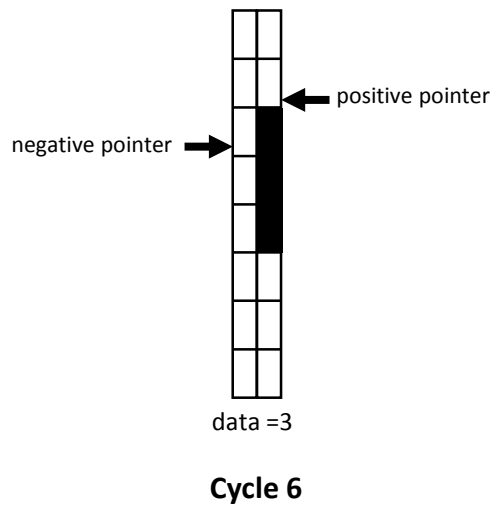
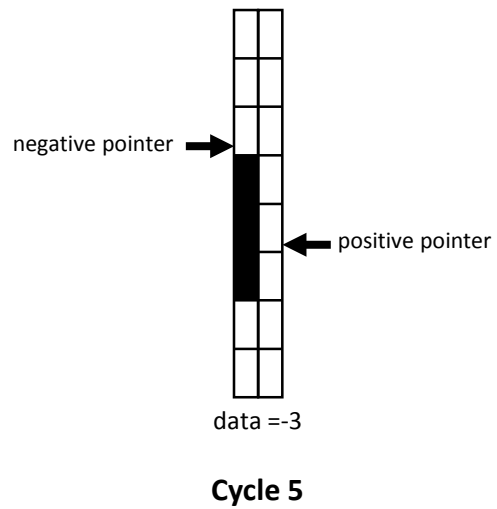
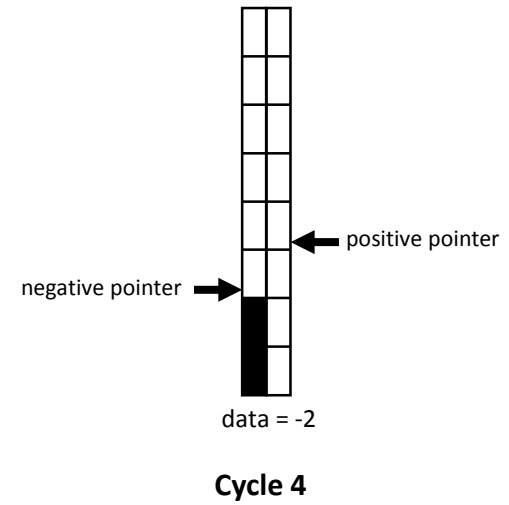
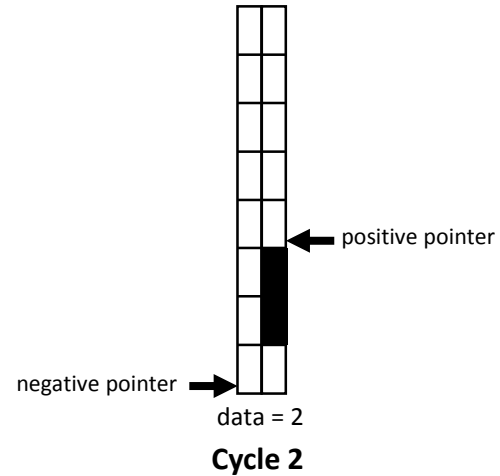
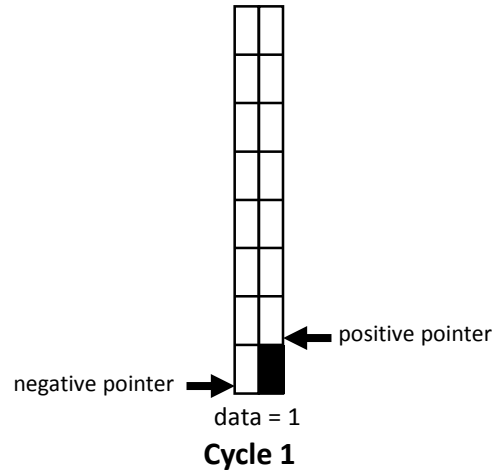
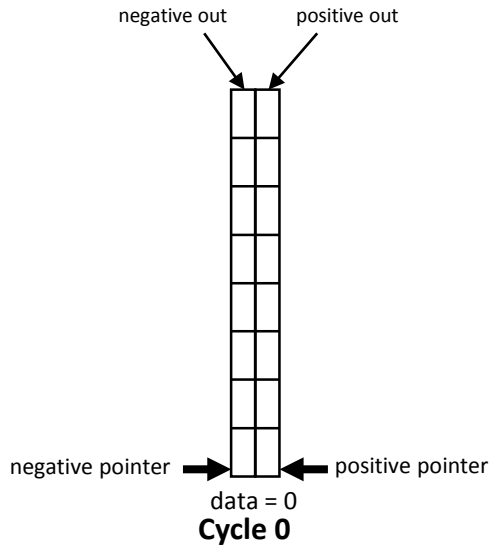


# Rules for rotational DEM

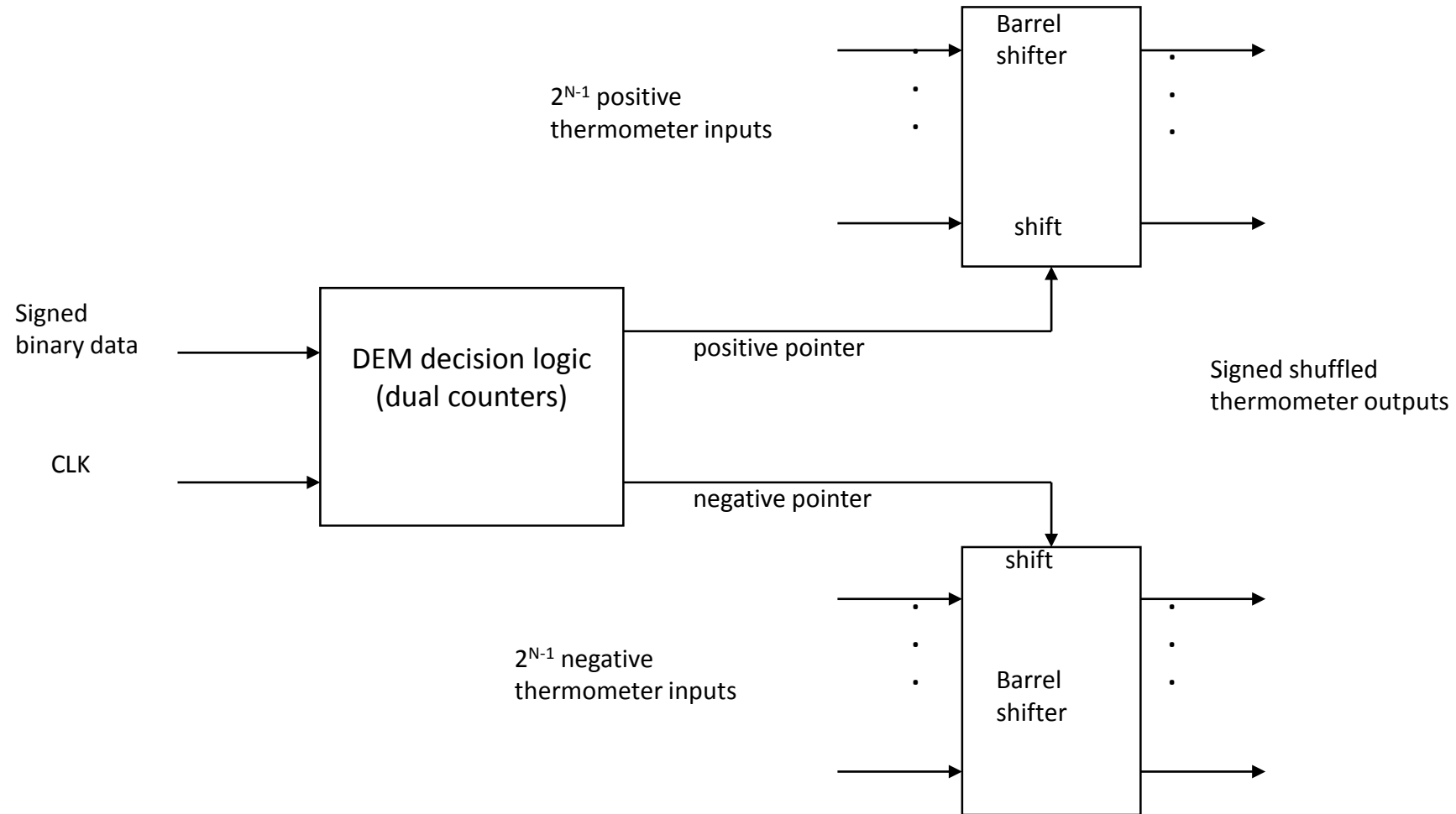


- Rules of DEM
  - For positive data, only positive pointer moves forward. Vice versa for negative data
  - Both pointers move in the same direction
  - Pointers wrap around in a circular manner
- Observations
  - If a pointer wraps arounds, the respective cumulative error is equal zero
  - If both pointers are at the same location, the cumulative error is equal to zero

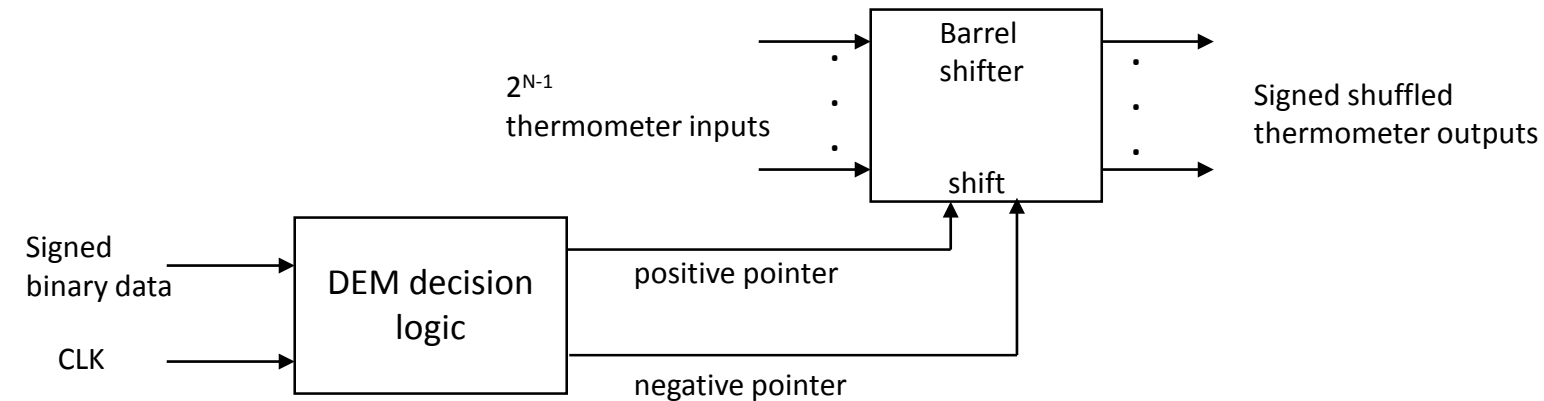
# Example



# Implementation of dual pointer DEM



# Implementation of dual pointer DEM with sign-magnitude data

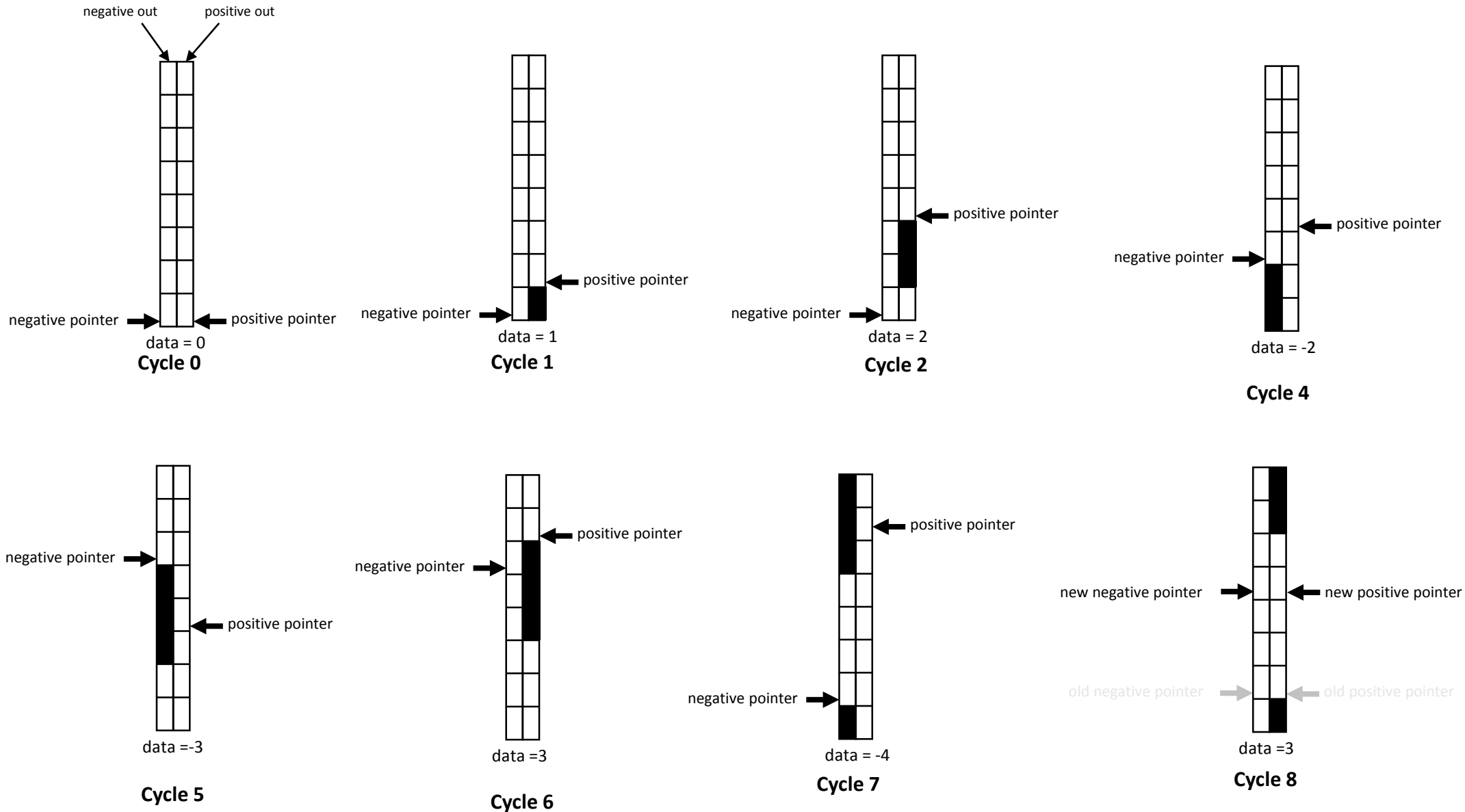


- Area efficient single barrel implementation
- Only 1 pointer is active and used at a time
- Barrel shift control is dependent on sign
- Barrel shifter only takes in magnitude
- Sign bit is used as a decoding

# Idle tones in dual pointer DEM

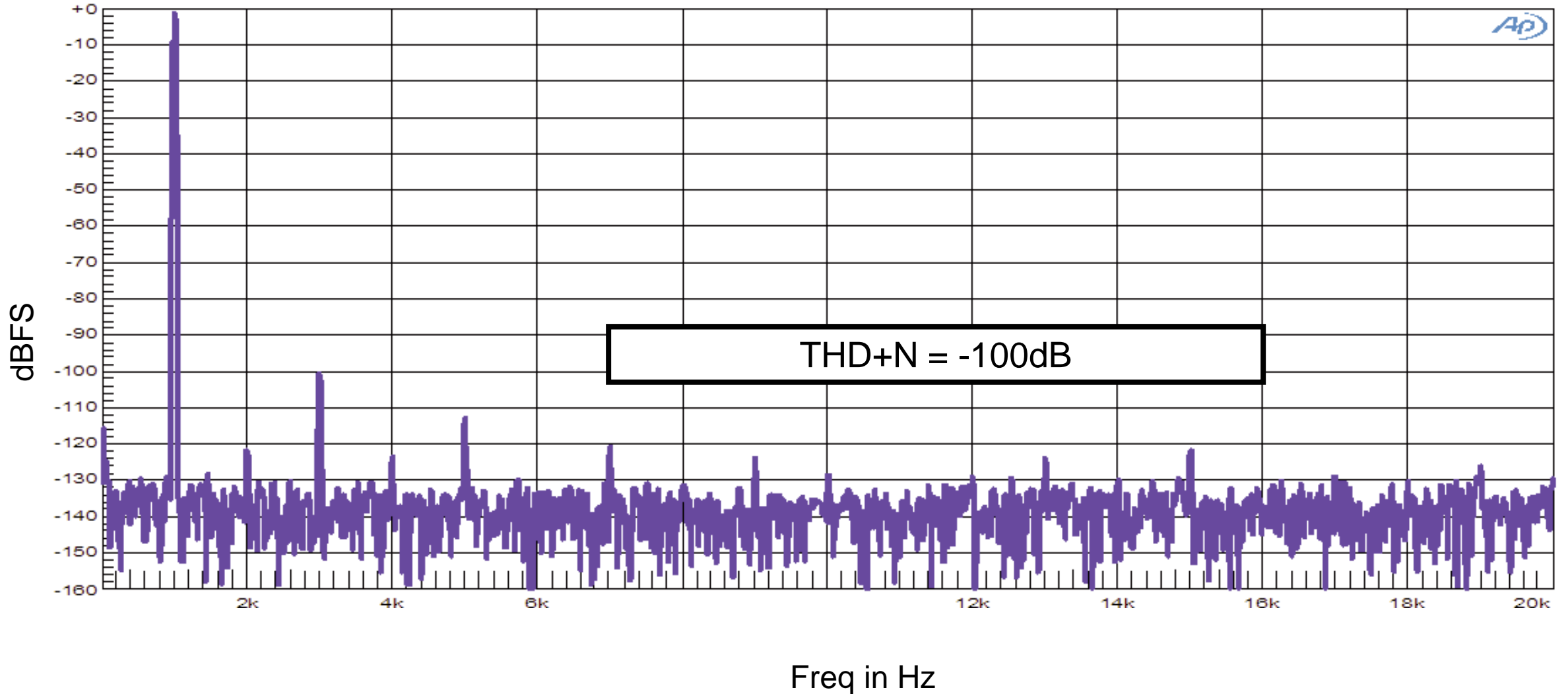
- Reasons:
  - Similar to those found in 2-level single pointer DEM
  - Static born-mismatch pattern shows up at low input level
- Remedy
  - Observe that when both pointers are at the same location, the cumulative error is zero
    - **Both pointers can be repositioned to a randomly chosen location**
    - Static mismatch error pattern will be broken up
  - A slight degradation to the SNR due to the introduction of the randomness into the first-order single-bit noise-shaped sequences
  - Mismatch shaping effectiveness is still very good with high OSR ( $\geq 64$ )

# Example: With idle tone remedy



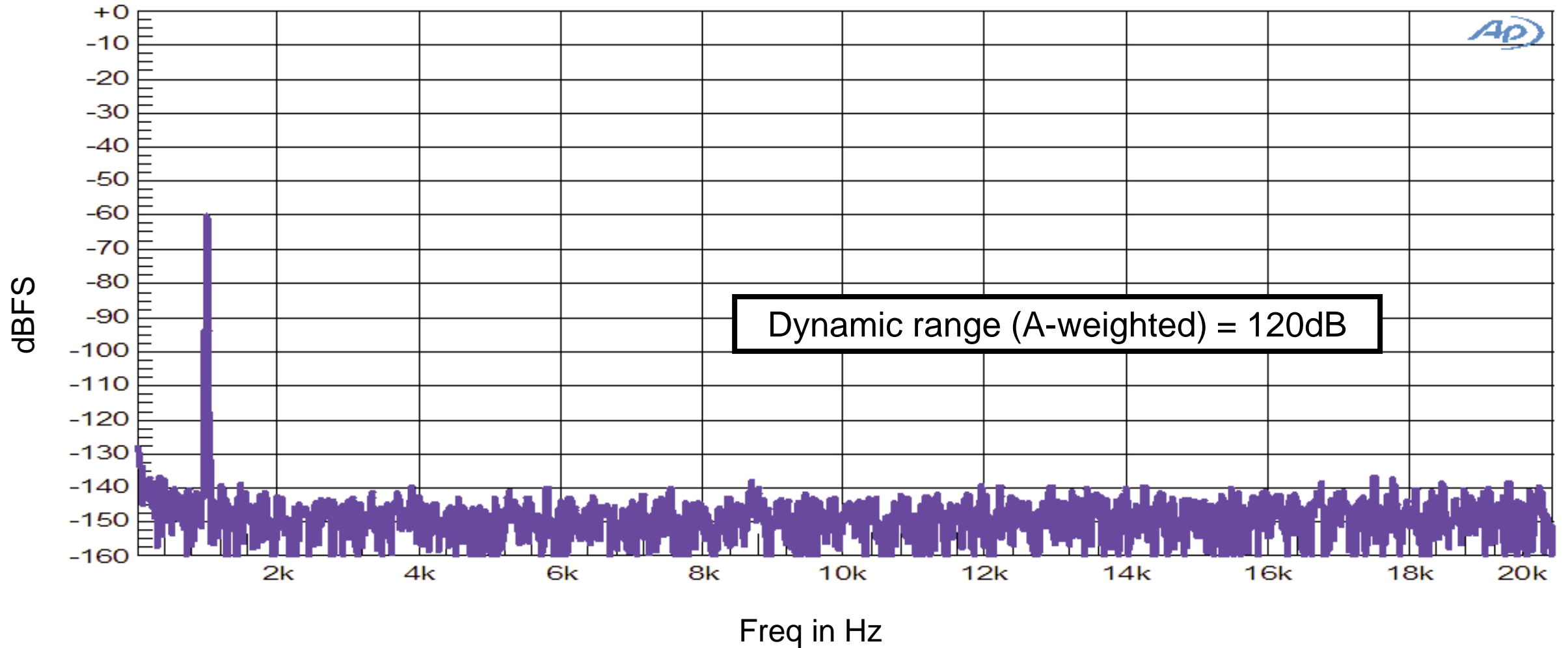
When positive and negative pointers are equal, randomize the position of both pointers.

# Measured result ADAU1966 at -0.5dbFS



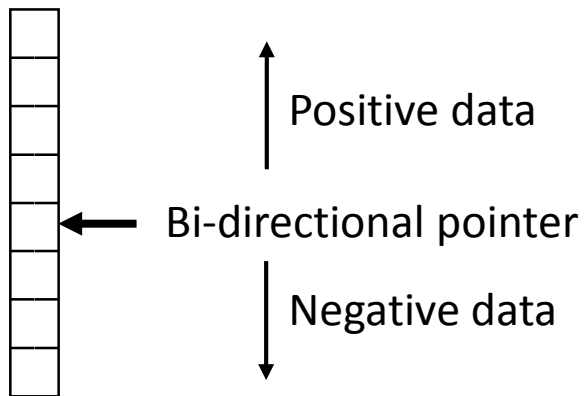


# Measured result ADAU1966 at -0.5dbFS



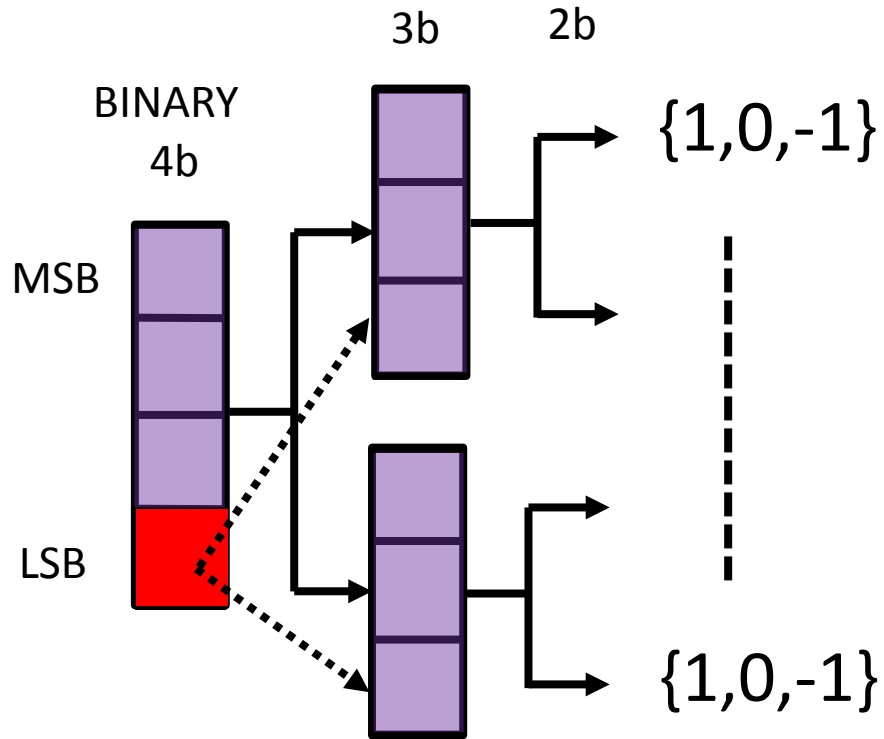
# Approach #2b: Single-pointer rotational DEM

- One pointer that moves forward when data is positive and backward when data is negative



- Possible remedy for idle tone
  - Set up a reference point
  - Keep track of wrapping around the reference point
  - After wrapping around (single or multiple times) and ending at the reference point, reposition pointer to a new randomly chosen reference point.
  - Repeat the entire procedure

# Approach #3: Tree structure DEM

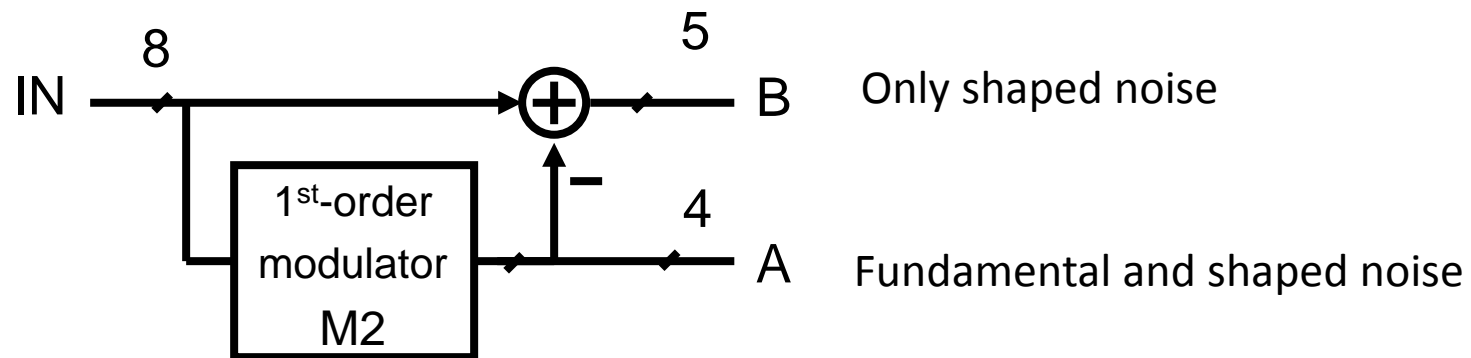


Example of a 4b implementation

- Use the tree structure to split the word until the last 2MSBs
- Decode the leaf cells to get the  $\{+1,0,-1\}$
- Remedy for idle tone
  - If data is even for a while, consider add 1 to one branch and subtract 1 in the other branch. This increases the data activity.
  - Watch out for headroom issue in the digital words
- **Note:** that each bit is still a 1<sup>st</sup>-order noise shaped sequence which has the fundamental component and shaped noise.

# Other possible solutions to tree-structure DEM

- Applicable when input word width is large for any straight implementations of DEM
- Consider noise shaped segmentation principle
  - Only one component in the sub-level has the signal fundamental. Easier to derive solution for idle tones.
  - May be done recursively
  - A and B can then be followed by a butterfly, rotational or tree-structure shuffler





# Approach #5: Real-time DEM

- Direct concept can be re-used
  - Requires fast clock
  - Switching loss due to logics may become significant to not be considered for low power implementation

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  - Solution spaces
- **Higher-order DEM**
  - Issues in 2<sup>nd</sup>-order DEM
  - Solutions
- Application specific concepts of DEM
- Q and A

# Why need 2<sup>nd</sup>-order DEM

- 1<sup>st</sup>-order DEM
  - Effective when OSR  $\geq 64x$
  - At lower OSR
    - Shaped mismatch noise degrades SNR.
    - DEM tones appear inband.
    - Over-clocking DEM (2x) may offer small improvement (not enough). Switching dynamics become a source of noise.
- **Solution:** 2<sup>nd</sup>-order shaping
- Issues with 2<sup>nd</sup>-order:
  - Ineffective for low input amplitude.
  - Area intensive especially with number levels  $>8$ .



# Approaches to 2<sup>nd</sup>-order DEM

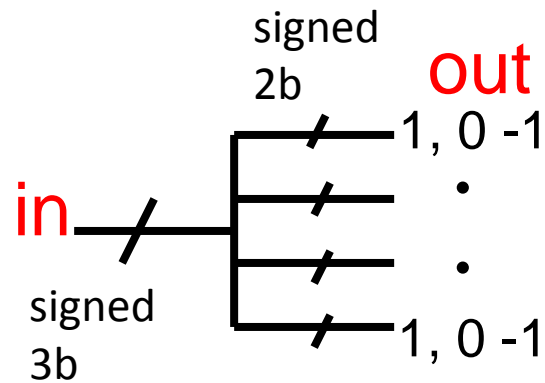
- Data directed : Cannot produce second-order mismatch shaping effectively
  - When inputs are both 11 or 00, mismatch shaper cells get “overloaded”
- Rotational: Can produce a second-order, but extremely hardware intensive, tends to revert to first-order shaping
- Tree-structure: Can produce second-order shaping but tends to revert back to first-order in real life use case (signal conditions)
- Vector quantization: Very hardware intensive due to realization of sorter and element selector
  - ***Hardware implementation at size = 2-bit (4 elements) is affordable***

# Design challenges and solutions

- Full implementation of vector quantization is extremely hardware intensive
  - Solution: **Segmentation (or tree structure)**
    - Break it down to smaller chunks where realization is affordable

# 2<sup>nd</sup>-order DEM for 3-level unit elements

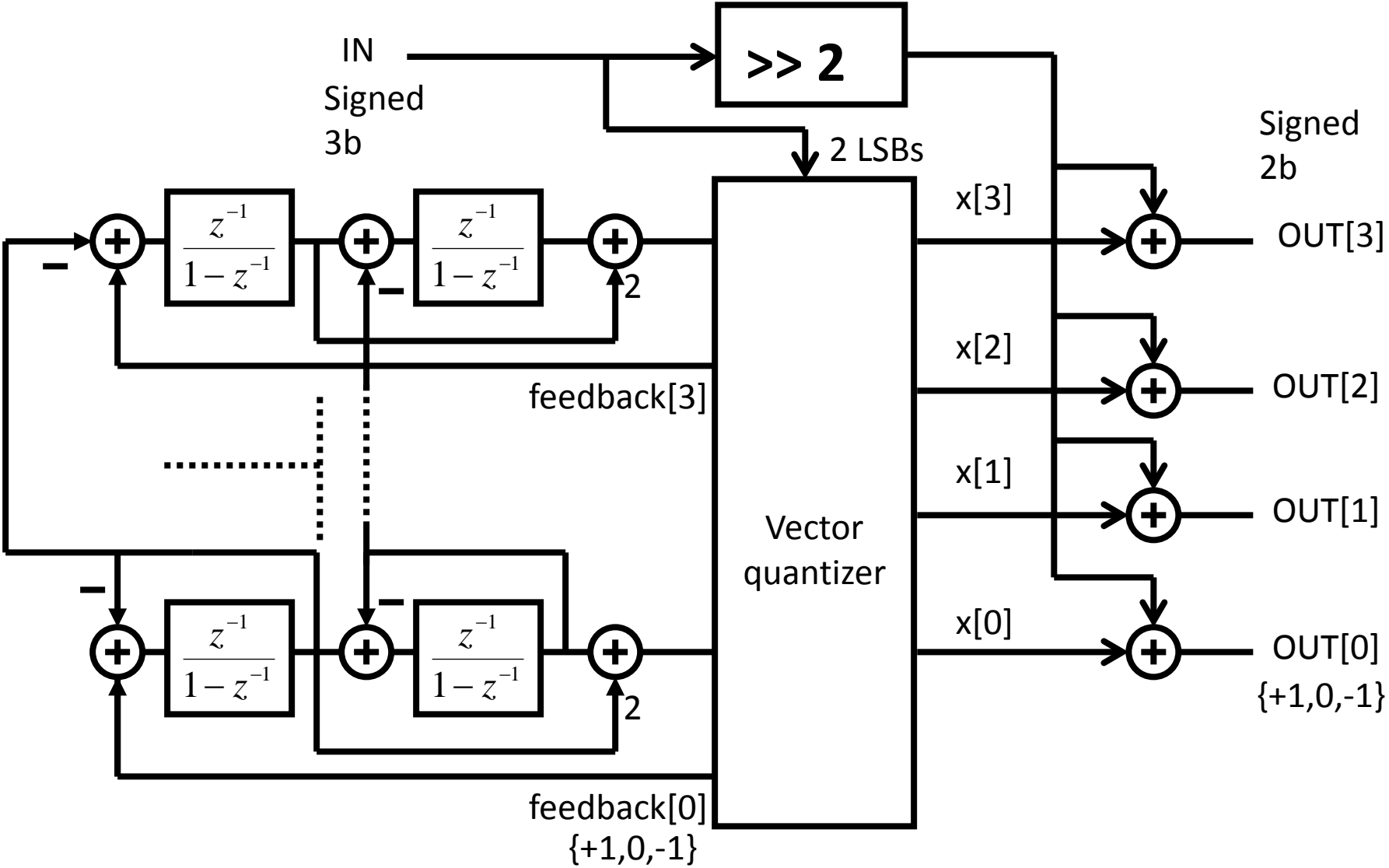
- Each leaf cell needs 2 bits:  $\begin{cases} 00 \text{ for } 0 \\ 01 \text{ for } +1 \\ 11 \text{ for } -1 \end{cases}$
- At one level higher in the tree, minimum size = 3 bits
  - Will need 4 cells to represent  $\{+3, \dots, -4\}$



## Operations:

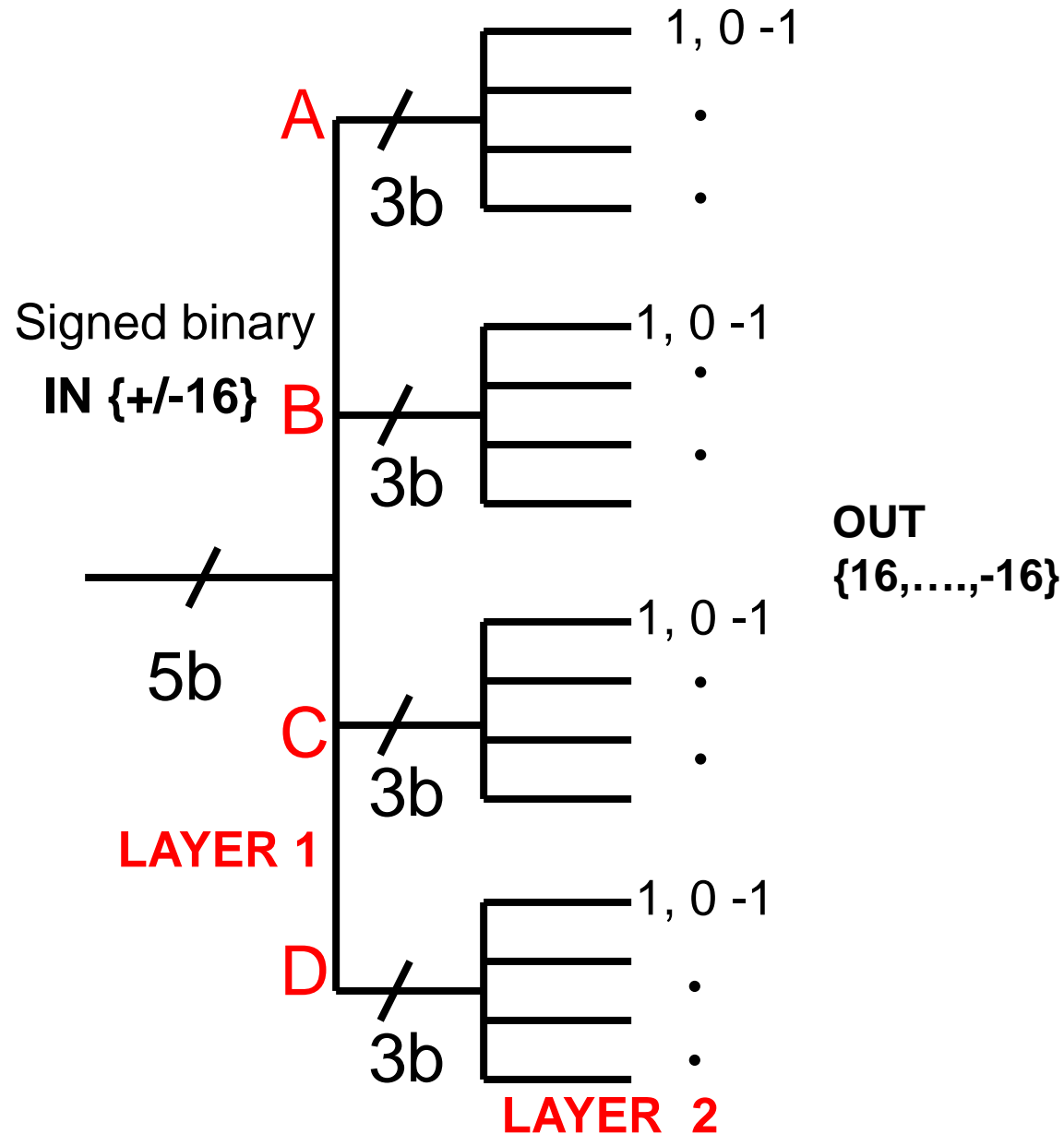
- 1)  $OUT[1:0] = IN \gg 2$
- 2)  $RESIDUE = 2 \text{ LSBs of } IN$
- 3) Use a 2<sup>nd</sup>-order NS loop to decide how to distribute the residue to the outputs

# Block diagram of a 3-bit, 2<sup>nd</sup>-order DEM



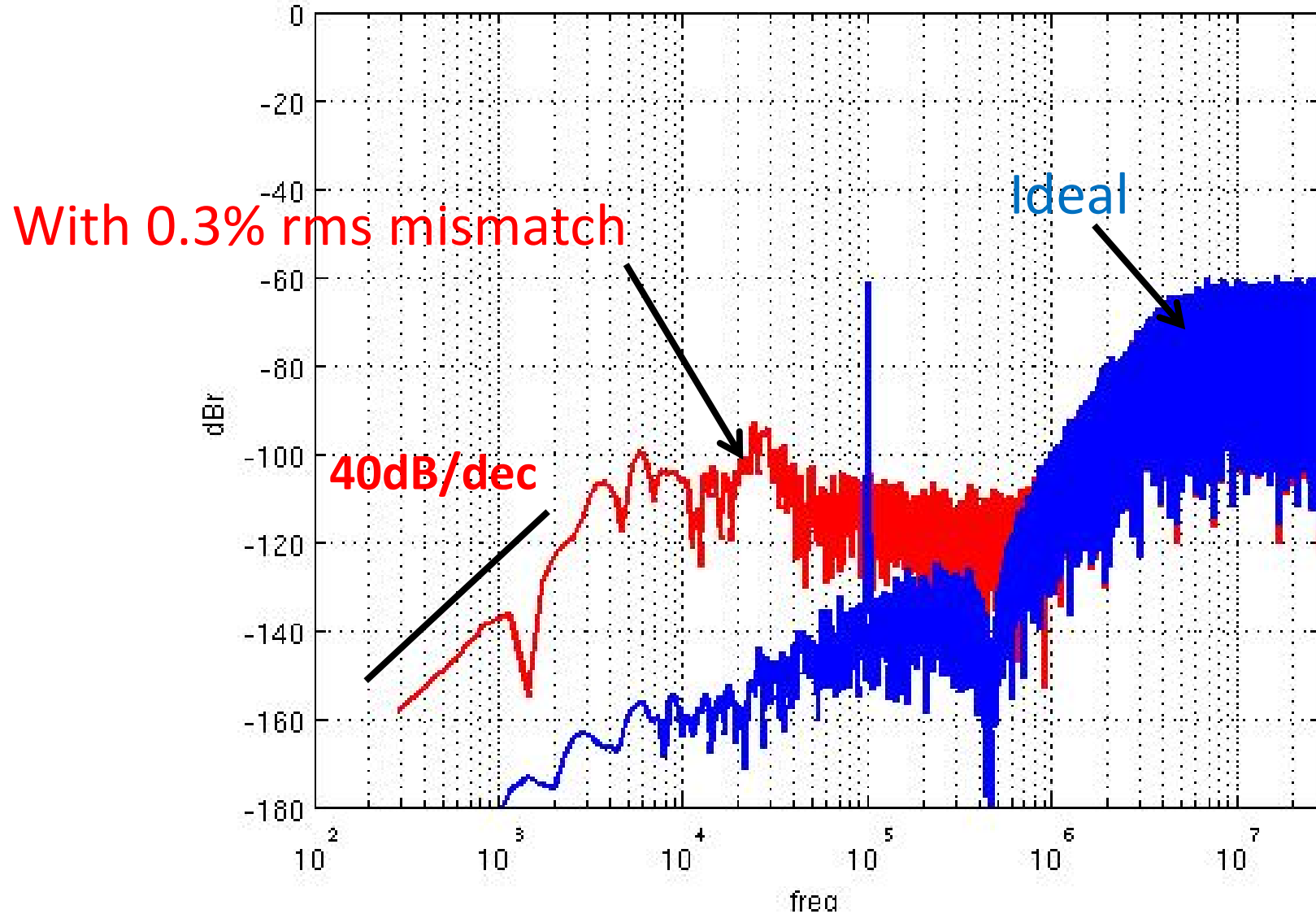
Feedback is ONLY produced when there is an instantaneous error made

# Block diagram of a 5-bit, 2<sup>nd</sup>-order DEM



1. **A + B + C + D = IN.**
2. **The spectral difference between every pair in layer 1 must show a 2<sup>nd</sup>-order highpass function**
  - DAC-to-DAC gain error will be 2<sup>nd</sup>-order shaped.
3. **The spectral difference between any pair of unit elements in layer 2 must also show a 2<sup>nd</sup>-order highpass function**
  - Element mismatch will be 2<sup>nd</sup>-order shaped.

# Simulation result

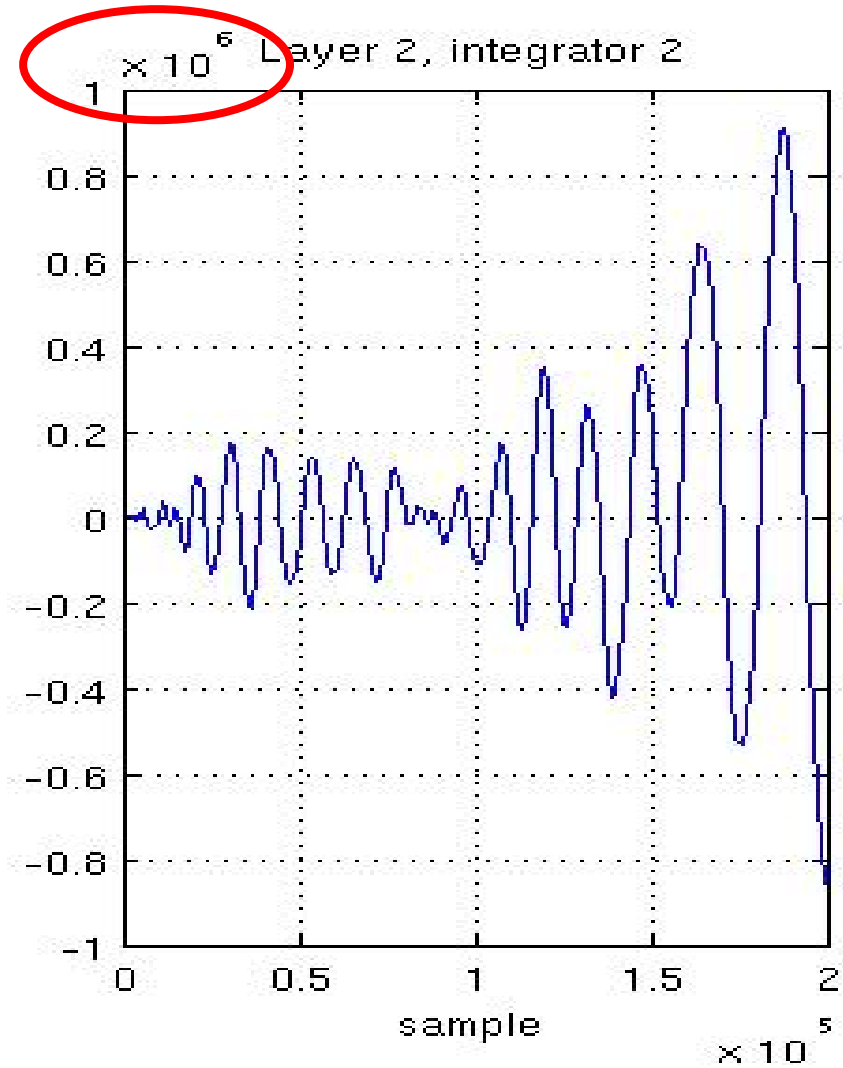
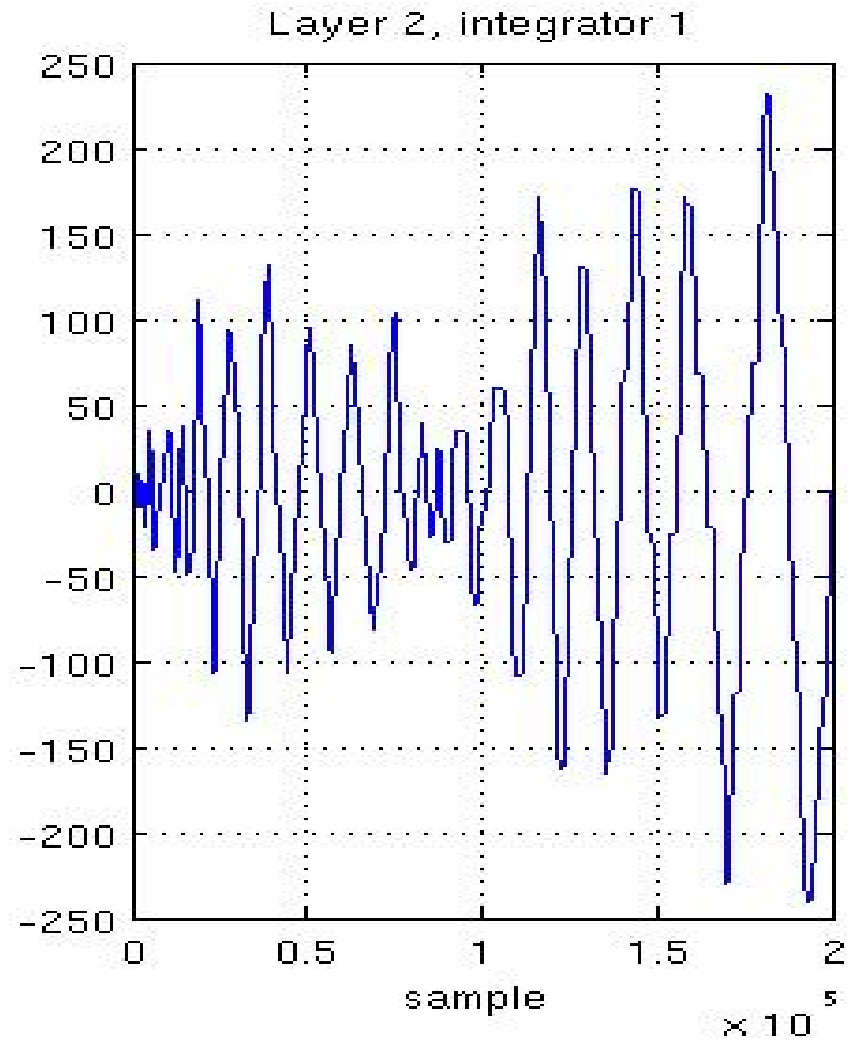


**Input = -60dBFS at 100kHz**

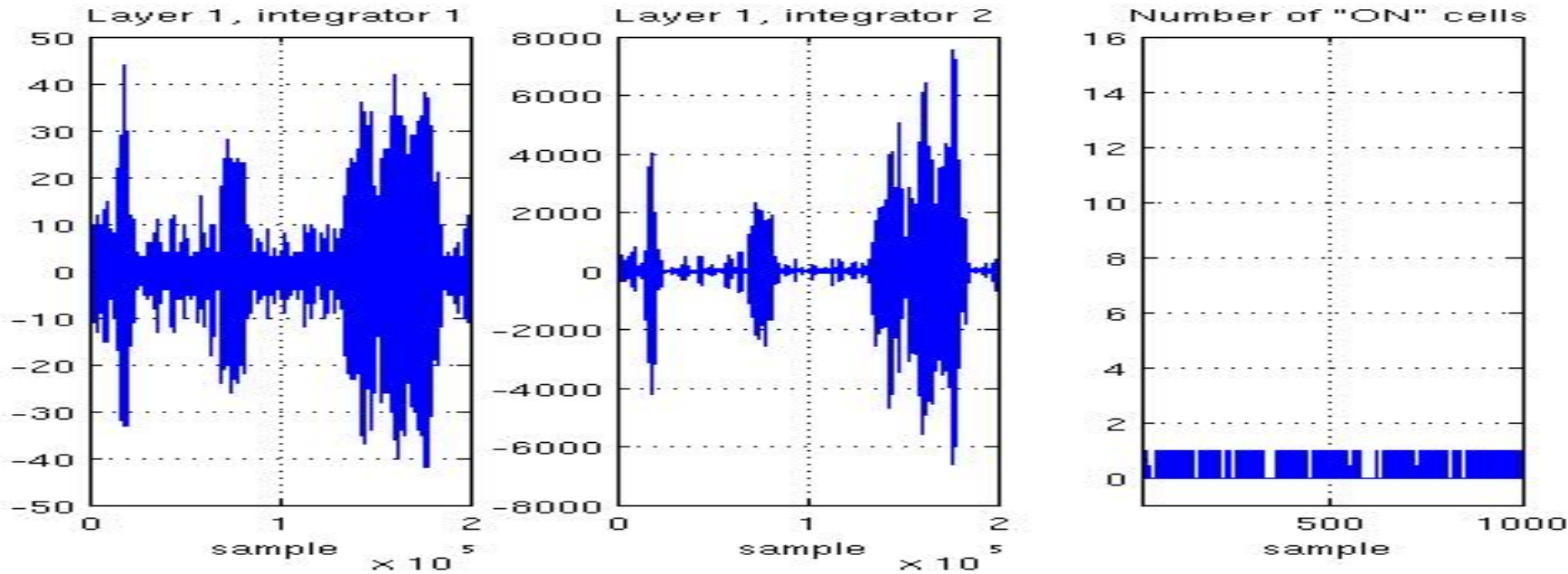
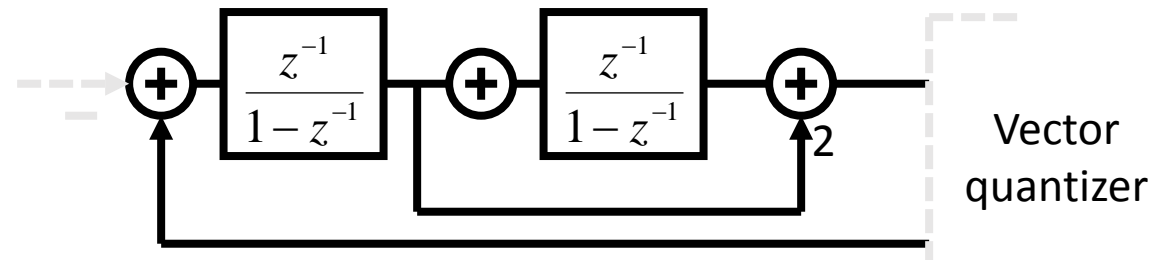
**Fclk = 64MHz**

**SNR is severely degraded !**

# Closer look at the integrator outputs at low input level



# The cause: low data activity



- Very large dynamic range integrator required
- Clipping makes the matter worse



# Design challenges and solutions

- Full implementation of vector quantization is extremely hardware intensive
  - Solution: Segmentation (or tree structure)
    - Break it down to smaller chunks where realization is affordable
- Inadequate data activity: cause large growth in integrator word widths
  - Solution: Trade off a small thermal noise performance: **Dynamics enhancement**

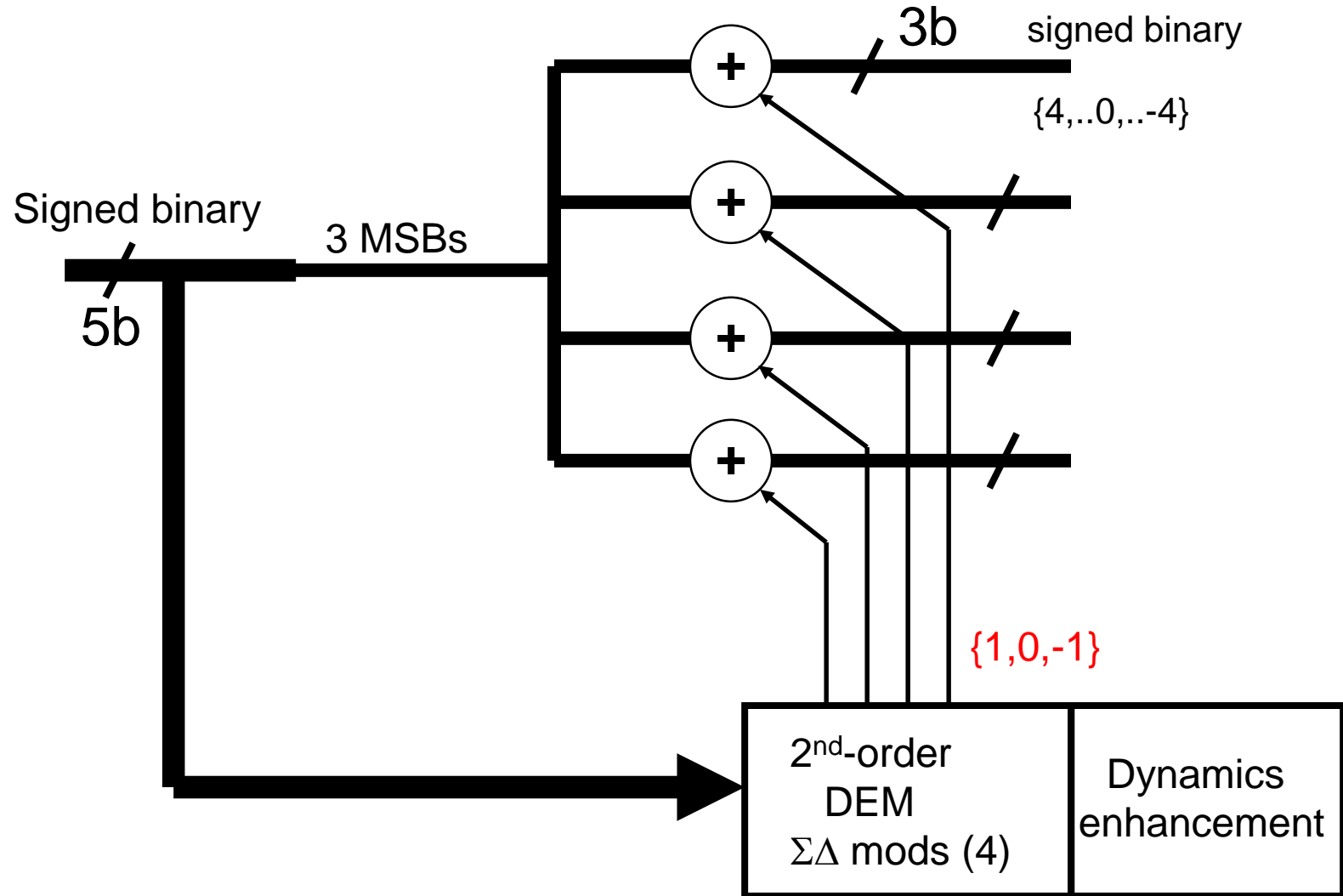
# Dynamics enhancement (DE)

- Increases the data activities while maintaining the digital **value** unchanged.
  - Add +1 and -1 to digital input when possible
- Trades off thermal noise for mismatch
  - Goal: keep # of ON cells as low as possible
- Reduces the integrator output swing tremendously. Very hardware efficient.

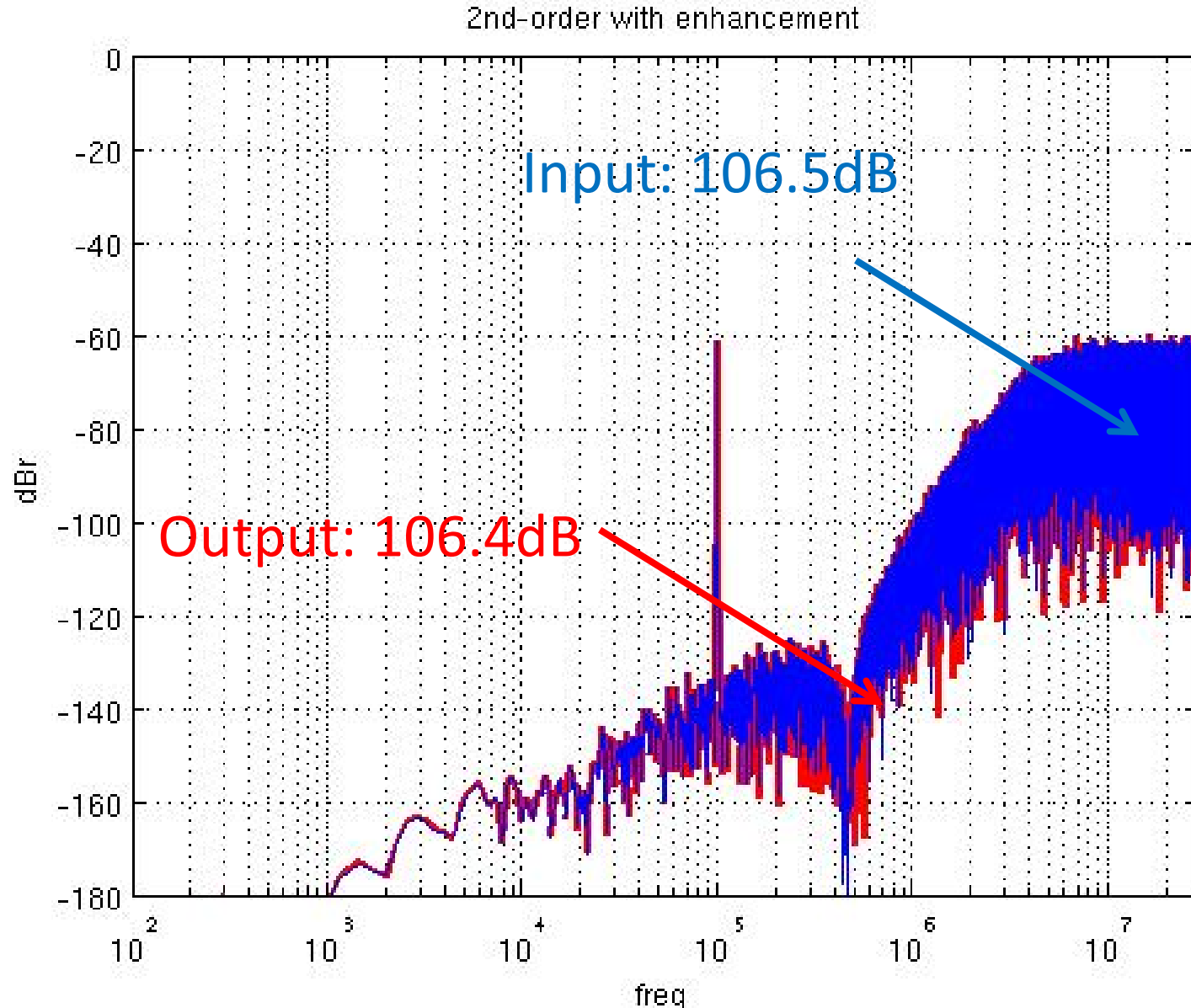
# Dynamics enhancement (DE)

- If 2LSB = “00”, start counting
- If count exceeds a designated number “wait\_time”
  - Check if signal(s) are in safe range
    - Add +1 and -1 to the branches. Reset wait\_time.
- Parameters to adjust
  - Wait\_time: affects integrators word width
  - Amount of +1/-1 added, restricted by thermal noise performance
  - Choice of where to direct +1 and -1 to.

# Combining 2<sup>nd</sup>-order DEM and dynamics enhancement



# Simulation: With dynamics enhancement

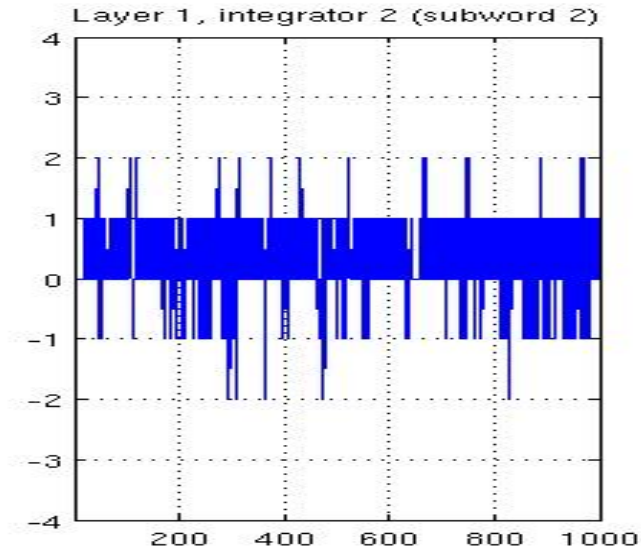
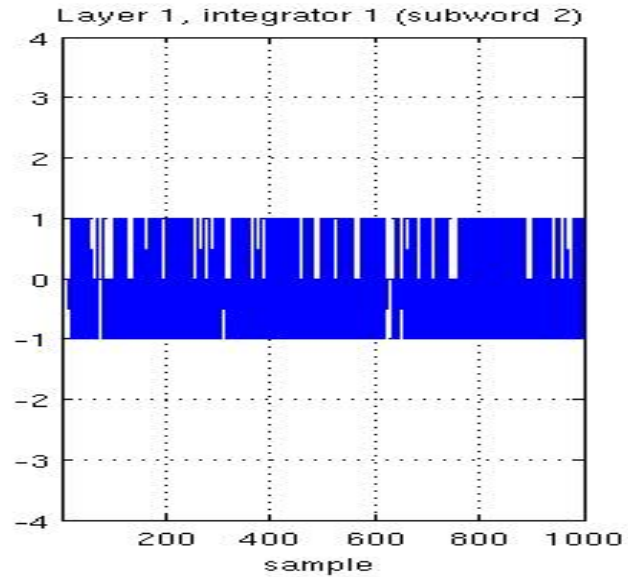


**Input = -60dBFS at 100kHz**

**Fclk = 64MHz**

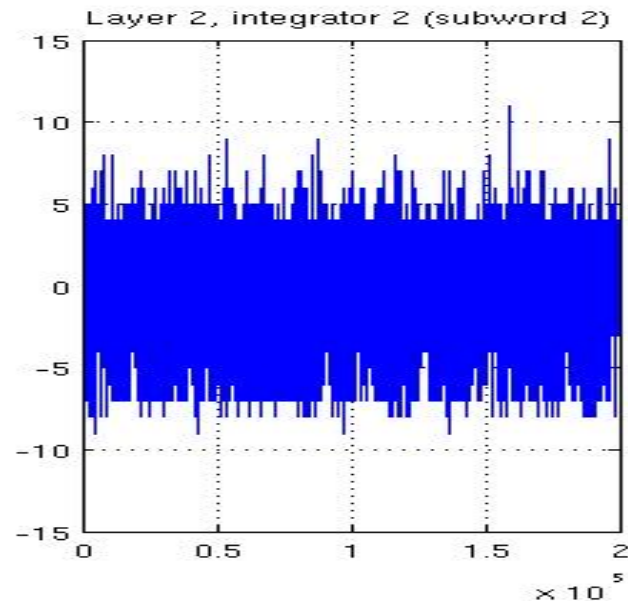
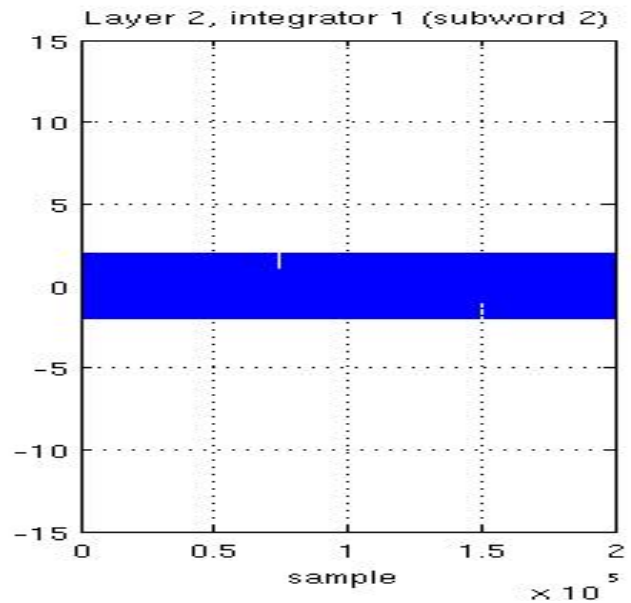
**Mismatch: 0.3% rms**

# Integrator outputs with DE



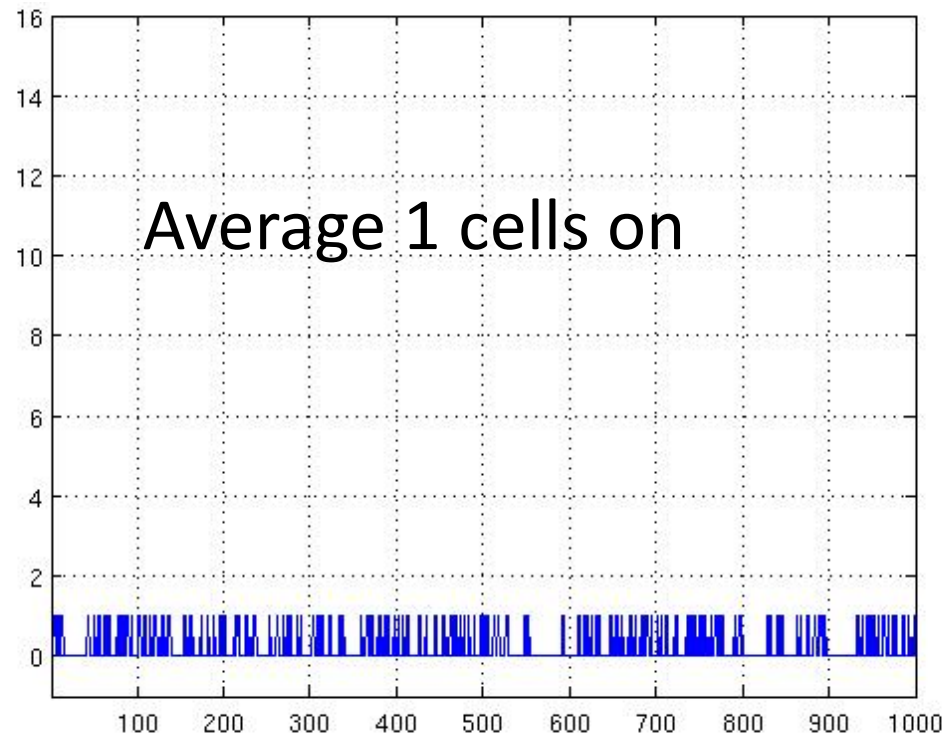
LAYER 1

**Much smaller dynamic range needed !**

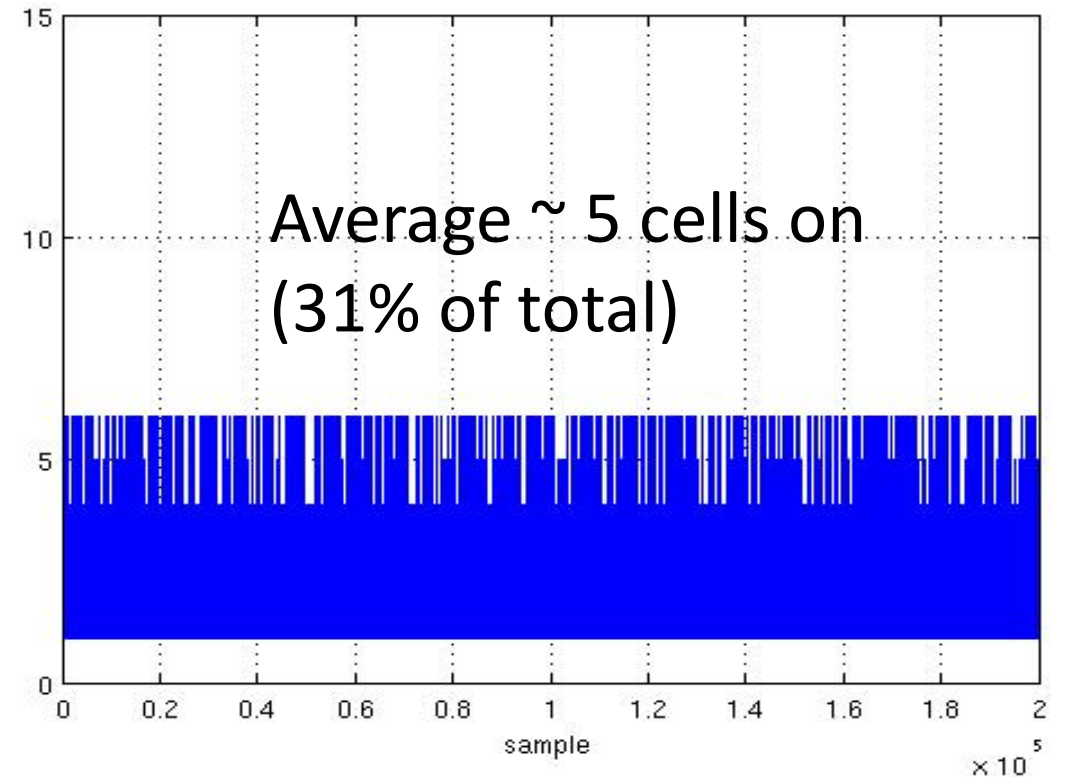


LAYER 2

# Number of DAC cells used at -60-dB input

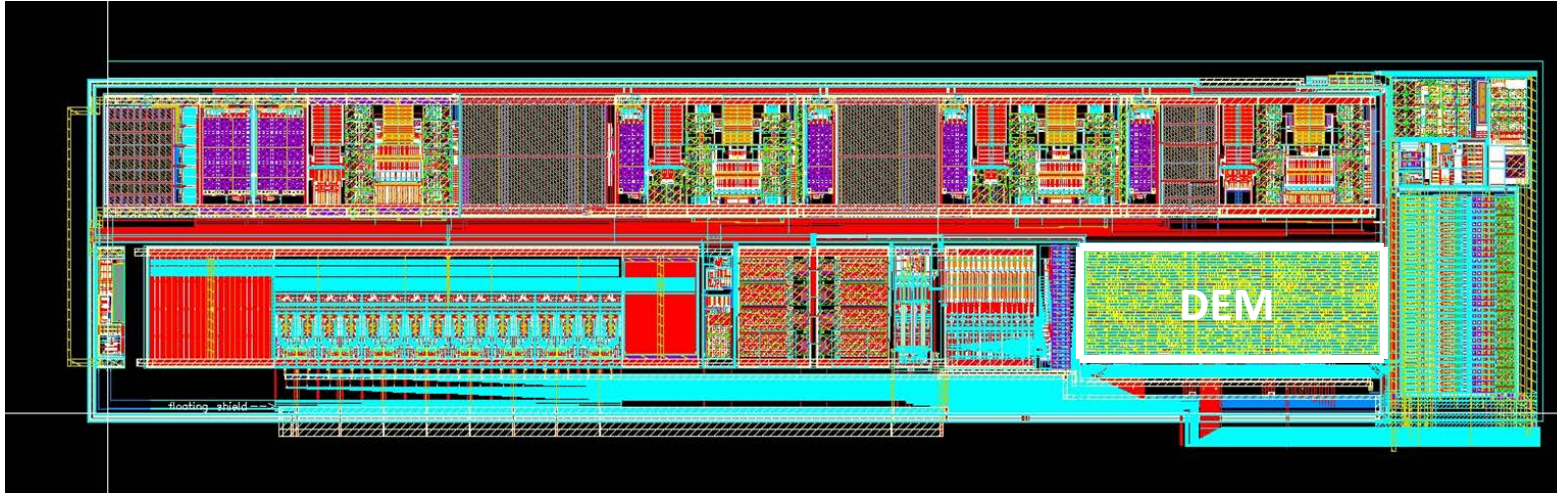


WITHOUT dynamics enhancement



WITH dynamics enhancement

# Layout of a Multibit Continuous Time $\Sigma\Delta$ ADC



A CT sigma delta 3<sup>rd</sup>-order modulator with 2<sup>nd</sup>-order DEM



# Recap

- Brief background
  - Motivations and Applications
  - 3-level vs. 2-level unit element: advantages and challenges
  - What problems DEM does and does not solve
- Practical dynamic element matching (DEM) techniques
  - 2-level DEM review
  - 3-level DEM
  - Limitations of each technique
  - Solution spaces
- Higher-order DEM
  - Issues in 2<sup>nd</sup>-order DEM
  - Solutions
- **Application specific concept of DEM**
- Q and A

# Problem definition

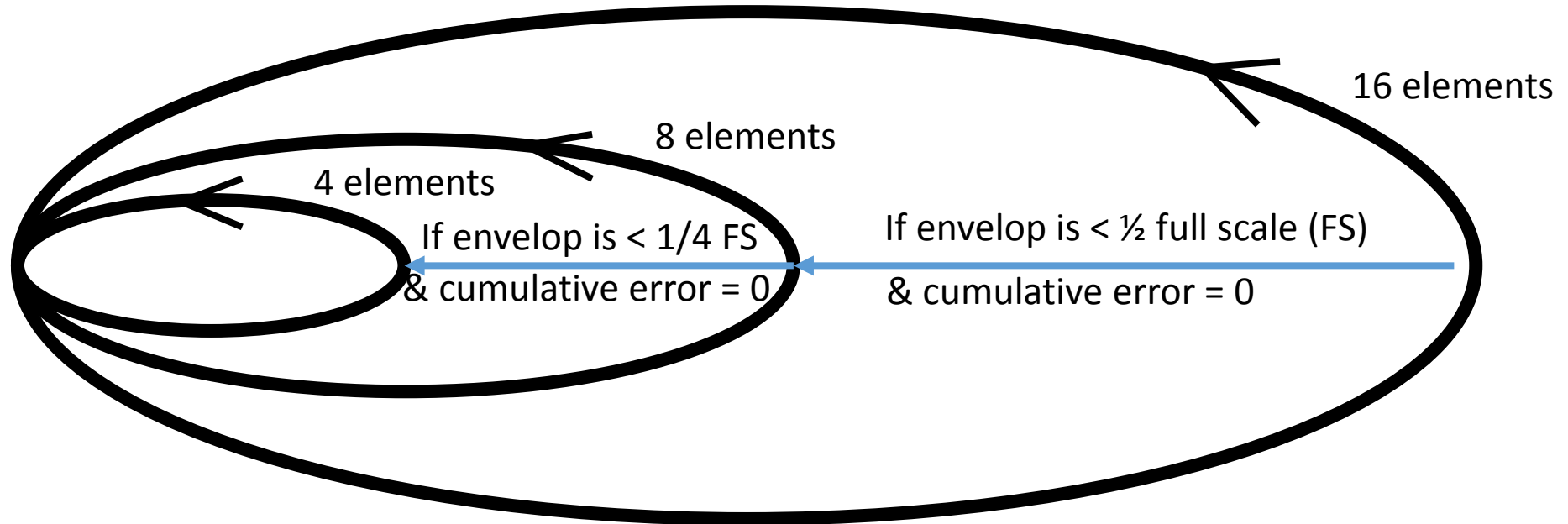
- **Reduce power consumption in the 3-level unit element DAC**
- In particular, when the input is small (-60dB) , only 1 or 2 cells are used, the rest of the cells are not used but still burn power.
- **Goal:** to turn off those unused cells without degrading performance.
- Note: *Dynamically turning off cells will cause degradation due to power consumption constraints and other dynamic effects.*

# Variable-length DEM

- Group size changes according to the envelop of the input signal
- Depends on the input data amplitude, the full group, half-group or quarter-group of the elements is used to create the signal
- The switch over to smaller group sizes is done at the time when the CUMMULATIVE ERROR is zero → DOES NOT interfere with the DEM activities
- Once the smaller group is selected, the unused elements (outside of the smaller group) will be turn off to save power
- With small group of elements, there is LESS mismatch error → Smaller shaped mismatch error in output.
- With less elements, the dynamics of the DEM is more → the DEM becomes more effective!

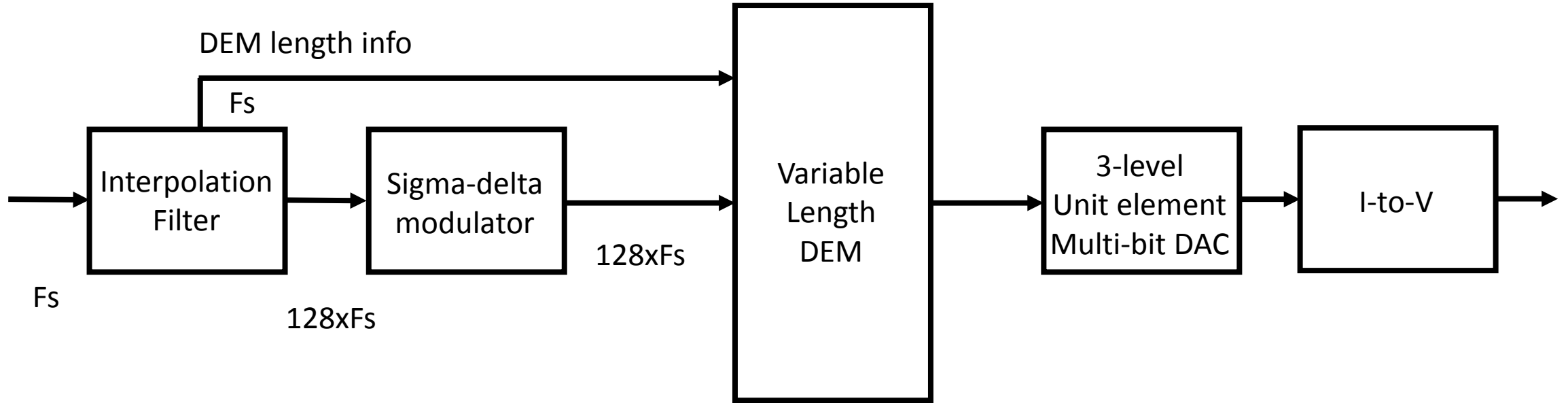
# Variable-length DEM

- Example of a 16 units 3-level thermometer-code DAC.



Rotation rings of DEM

# Example: Application in audio DAC

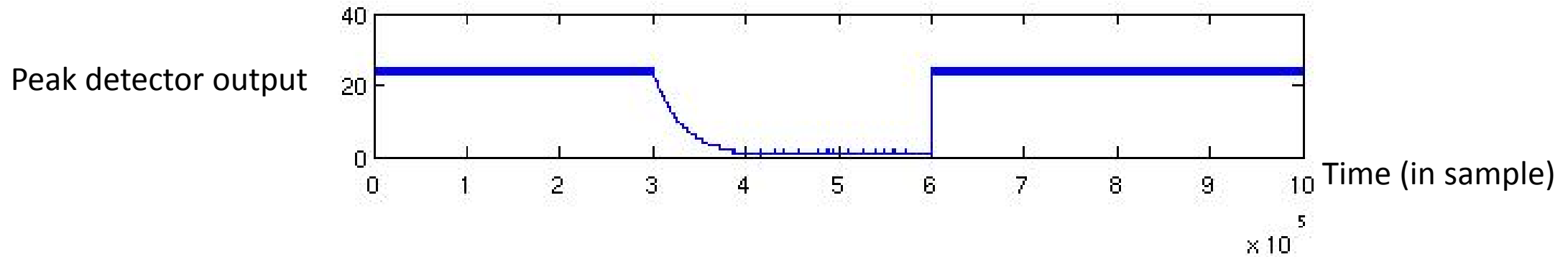
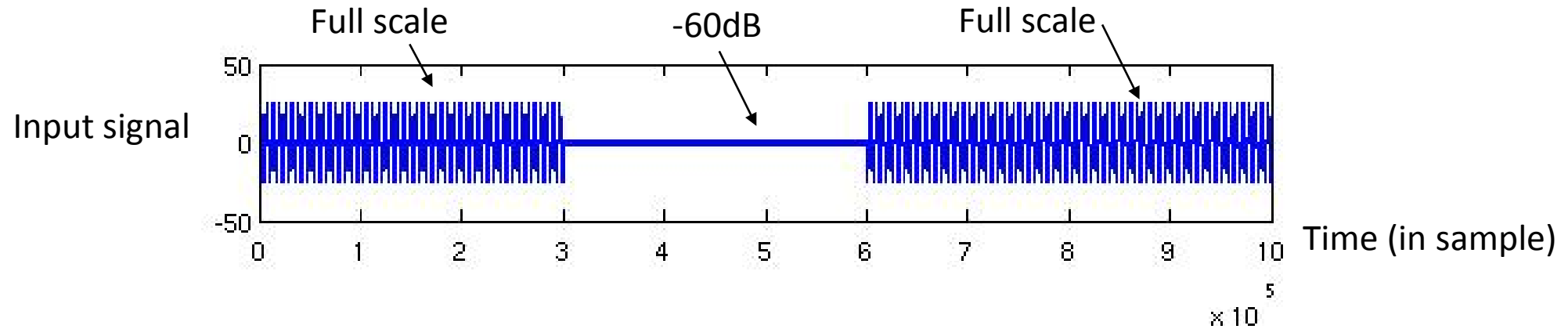


- Peak detector is used at the interpolation filter input
- Hysteresis is needed to avoid chatting (in and out of variable length mode)

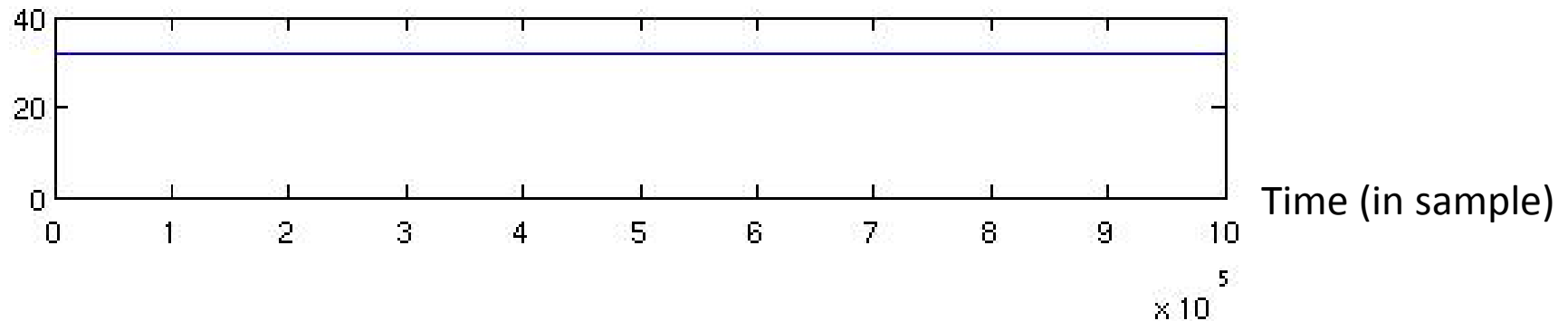
# Simulation case

- 2<sup>nd</sup> order sigma delta , 128x OSR, 6b output
- Input frequency = 1kHz
- Analog elements have 0.2% rms mismatch error
- Amplitude changes from full scale to -60dB FS
  - Demonstrate the switching from full-size group to quarter-size group
  - Demonstrate the improvements in SNR
  - Demonstrate the ability to turn off the unused elements to save power

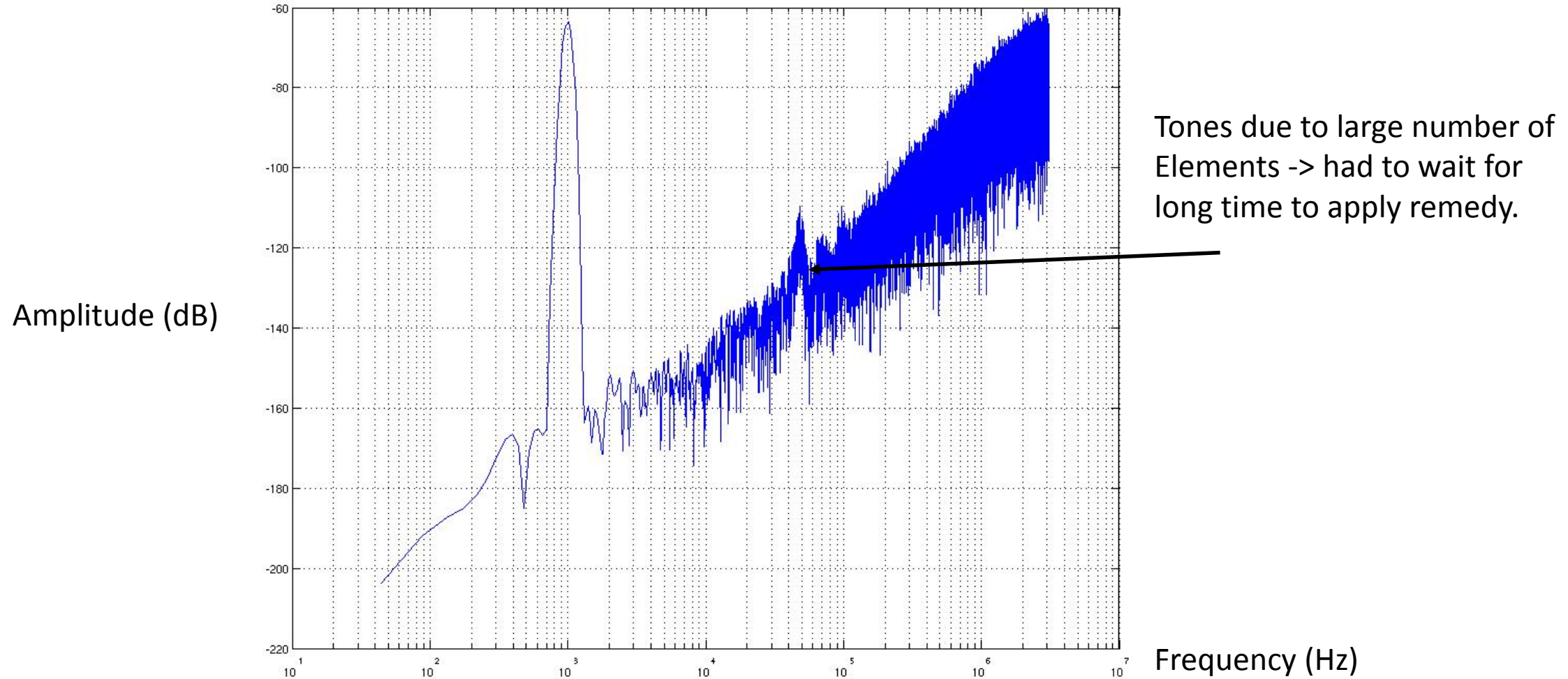
# Simulation result: No Variable-length



Number of elements used  
= 32

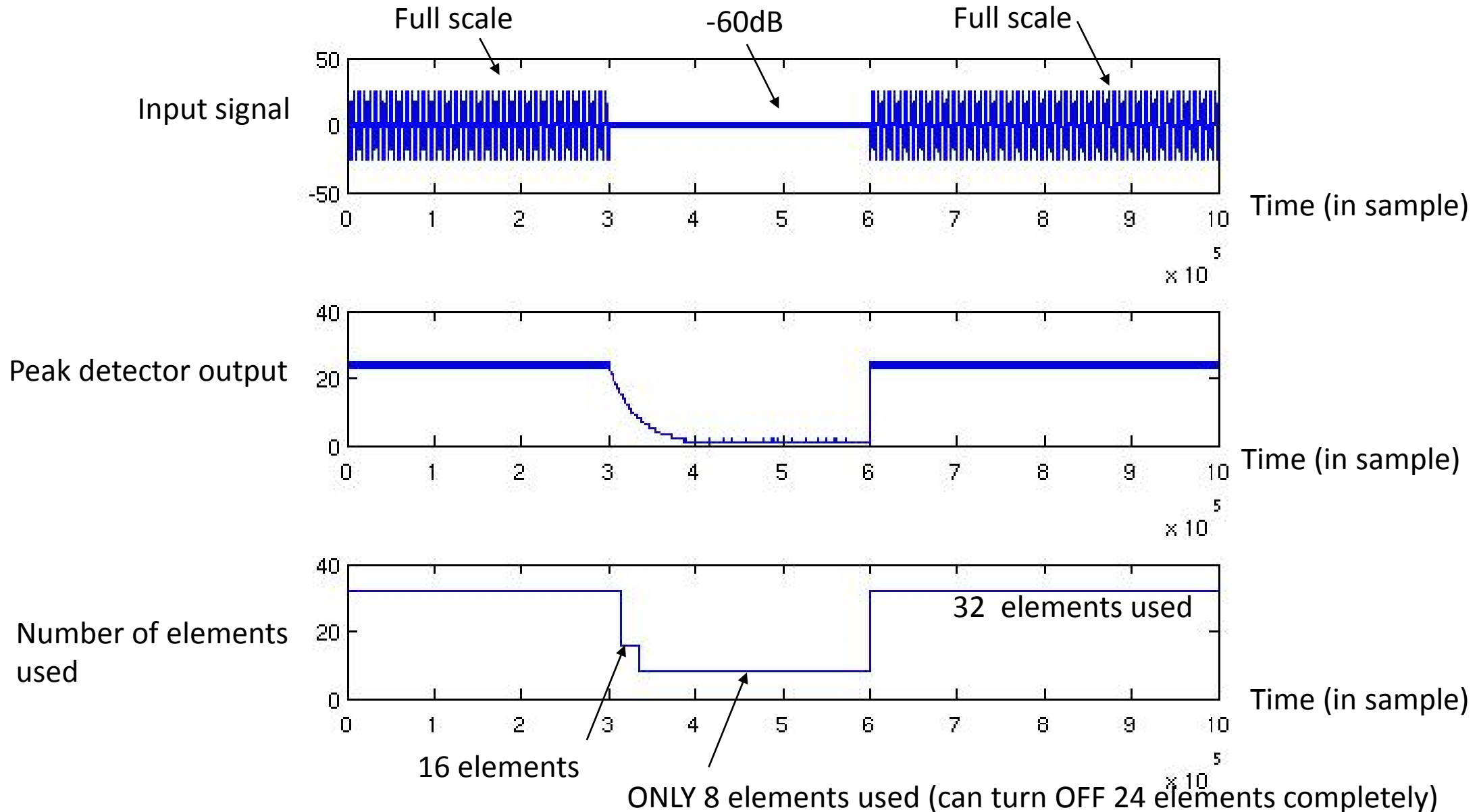


# No Variable-length: FFT of the -60dB input

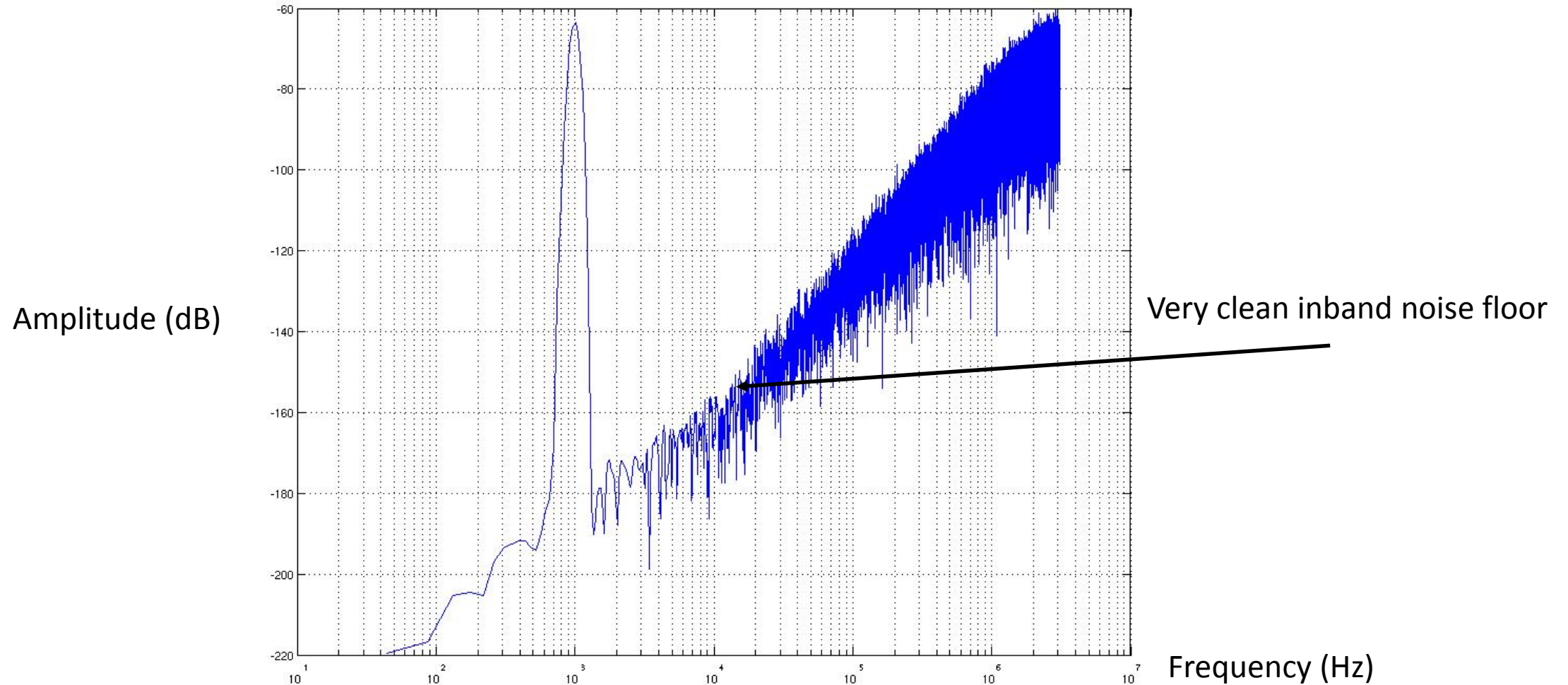




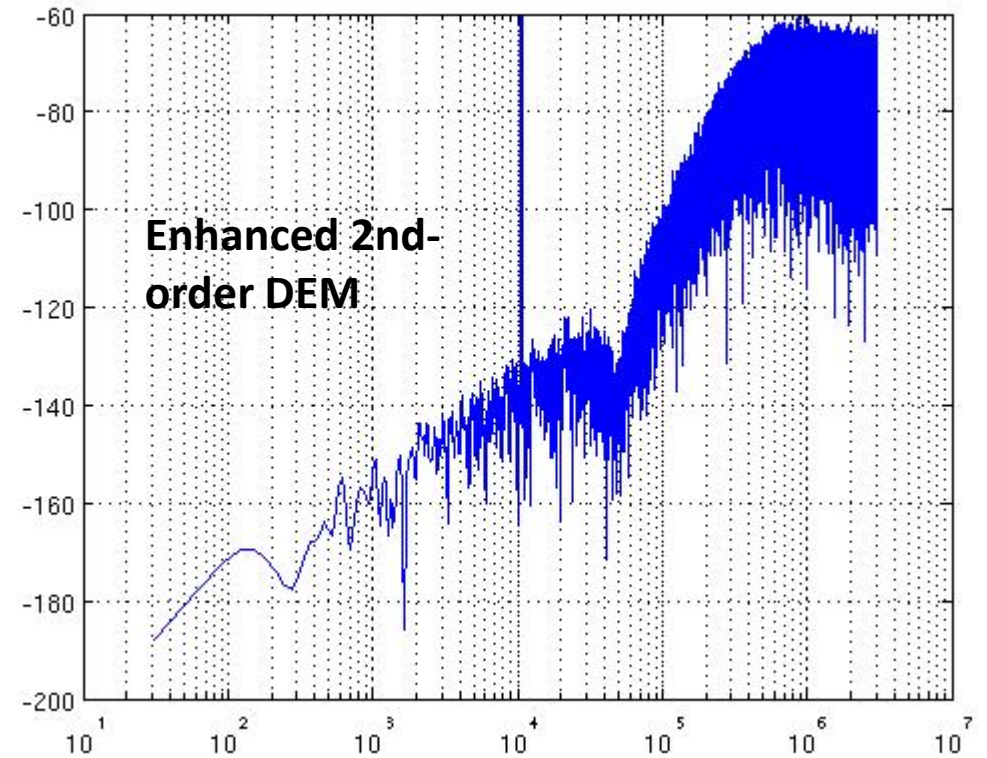
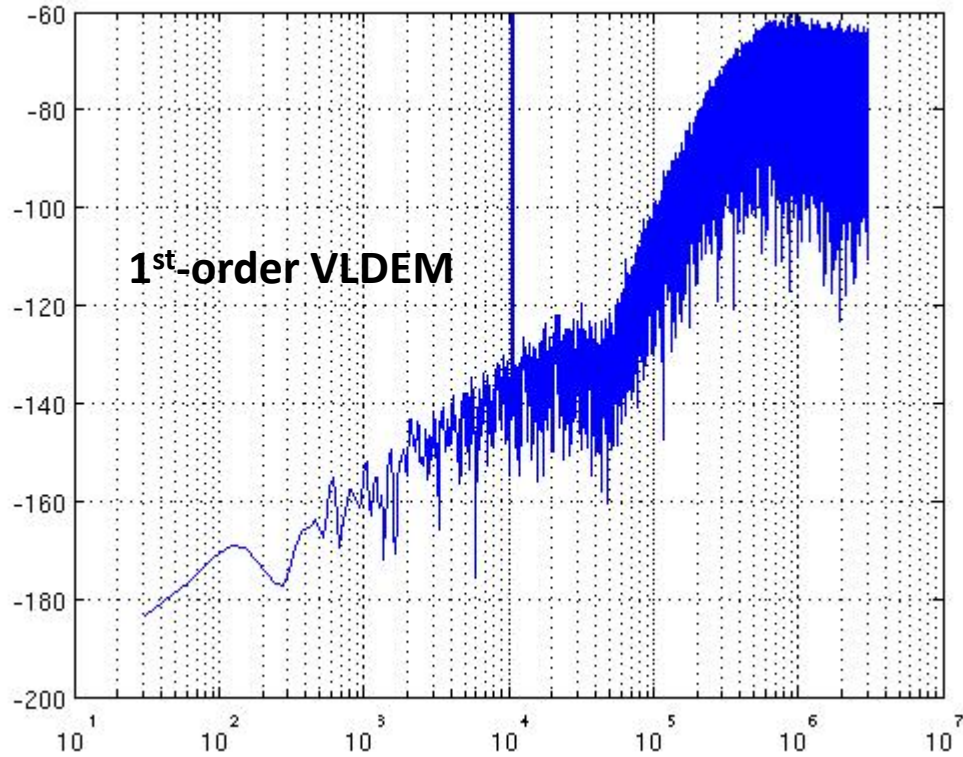
# Simulation: With Variable-length DEM



# With Variable-length: FFT of the -60dB input



Performance compared to 2<sup>nd</sup> order DEM @ -60dBFS, 0.25% rms mismatch



- Performs comparably to a **properly done** 2<sup>nd</sup>-order DEM (Both @ 103dB SNR)
- Much lower hardware requirement

# Notes

- Optimized power consumption for DAC at low input level
- Very effective first order DEM for the sub segment(s)
- Very effective for DEM idle tone remedy
- Trade off the gain accuracy across signal amplitude range (there is NO distortion because there is no switching back and forth between smaller DACs and the large DAC , on the fly).
- Suitable for applications that require high AC linearity and not DC accuracy

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# References

- Richard Schreier et al., “Delta-Sigma Data Converter”, IEEE press 1977
- Tom Kwan and Bob Adams, “ A stereo multibit DAC with asynchronous master clock interface”, JSSC Dec 1996.
- Khiem Nguyen et al., “A 108dB SNR, 1.1mW Oversampling DAC with Three-level DEM technique”, ISSCC 2008
- A. Bandyopadhyad , K Nguyen, “A 120dB SNR 21.5mW CT SD DAC”, ISSCC 2011
- I. Fujimori et al., “A Multibit Delta–Sigma Audio DAC with 120-dB Dynamic Range”, JSSC vol. 38, no. 8, Aug 2000
- I. Galton et al., “Why Dynamic-Element-Matching DACs Work”, Trans on Circuits and Systems II, vol. 57, no. 2, pg. 69-74, Feb 20
- I. Galton et al., “Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters”, Trans on Circuits and Systems II, vol. 48, no. 11, pg. 1014-1027, Nov 2001
- P. Rombouts et al., “A Study of Dynamic Element-Matching Techniques for 3-Level Unit Elements”, Trans on Circuits and Systems II, vol. 47, no. 11, pg. 1077-1087, Nov 2000
- A. Bandyopadhyad , K Nguyen, “A 96dB SNR 600kHz CT SD ADC”, Symposium on VLSI Circuits Digest of Technical Papers 2014
- E. Folgman et al., “A Dynamic Element Matching Technique for Reduced-Distortion Multibit Quantization in Delta–Sigma ADCs”, Trans on Circuits and Systems II, vol. 48, no. 2, pg. 158-170, Feb 2001
- R. Wang et al., “Split-set data weighted averaging”, Electronic Letters, 16th February 2006 Vol. 42 No. 4.

# References

- Anas Hamoui and K. Martin, “Linearity enhancement of multi-bit SD modulators using pseudo data weighted averaging”, ISCAS 2002, pg 285-288.