Calibre DRC and LVS

Key Product Benefits

• Unparalleled Performance and Capacity: Calibre’s powerful hierarchical engine, with automatic, design-style independent hierarchy analysis and optimization, delivers verification results in hours instead of days, even on the largest designs. The multi-threading option (CalibreMT) radically boosts verification speed by leveraging multiple CPUs. Support for 64-bit operating systems ensures unlimited capacity.

• Highest Accuracy Verification: Calibre’s advanced Design Rule Checking (DRC) algorithms have been tailor-made to accurately and efficiently check even the most complex DSM rules in a manner that is easy to interpret. The most robust Layout vs. Schematic (LVS) device extraction and netlist comparison features pinpoint error detection, regardless of design style or methodology, and without significant performance degradation, even in the face of many errors. This combination makes Calibre the best choice for digital, analog, mixed-signal and SoC designs.

• Seamless Design Flow Integration: Calibre’s ability to interactively verify and make corrections in an existing design framework, without being constrained to proprietary tools or flows, dramatically reduces iteration runtime and error debugging. This intimate setting enables designers to use Calibre as a single platform for cell/block and full-chip verification.

Calibre is the Industry Standard for Deep Submicron Physical Verification

The Calibre tool suite is the first verification solution built specifically to meet not only the need to produce the highest quality cells and blocks, but also the growing challenges of large, complex integrated chips and systems-on-chip. Mentor Graphics engineers have developed a proven breakthrough technology that provides accuracy for analog mixed-signal designs and performance and capacity for large designs and SoCs. Calibre significantly reduces verification cycle times, even as IC device counts ascend to the hundreds of millions. Calibre offers fast, reliable design rule checking (DRC), layout vs. schematic (LVS) and electrical rule checking (ERC) on flat and hierarchical designs. Calibre is also design-style independent, allowing it to integrate easily “out-of-the-box” with various design methodologies, flows and tools. As a result, Calibre has not only been chosen by a majority of engineers for deep submicron verification, it is also the dominant physical verification internal/sign-off tool for the world’s semiconductor foundries, fabs, library companies and IP providers.

www.mentor.com/dsm
Calibre’s Hierarchical Engine Sets the Standard for DRC/LVS Physical Verification

Calibre’s hierarchical processing engine offers robust performance, capacity and accuracy across design styles. This makes it the best choice for companies creating blocks with hierarchy (RAMS, ASICS, etc.), blocks with little or no hierarchy (analog blocks, standard cell libraries, etc.) or large ICs and SoCs.

Calibre’s intelligent algorithms take advantage of the repetition inherent in modern IC design; rather than process a cell each time it occurs in a design, Calibre recognizes the repetition of a cell, checks its content once, then ensures that each cell is instantiated properly. Because the cell is processed just once, verification performance is significantly improved and database memory requirements are dramatically reduced, improving total throughput capacity.

Calibre does more than work with explicit hierarchy; it also works with implicit hierarchy, recognizing repeated polygons that were not intentionally created as cell instantiations. In addition, Calibre gains a performance boost on large, flat polygon data by breaking the data into individual bins and analyzing each separately. Each bin is treated as a unique cell with no repetition, but total performance is improved because Calibre finds fewer polygons it must operate on at once. This enables Calibre to run efficiently on flat data or data with little hierarchy.

Fast turn-around time is a key benefit, with physical verification results delivered in minutes and hours rather than days. Because it runs in RAM, (the only disk requirements are for output files), it can operate in common network environments with little overall impact due to network I/O traffic. These same algorithms which provide Calibre’s top-notch performance also improve capacity. With this efficiency, Calibre allows continued use of existing equipment, saving design teams additional capital expenditures.

Multi-Threaded Power

Calibre’s multi-threading technology (CalibreMT) offers significant performance gain in a multiple CPU environment. Calibre leverages multi-processor workstations or servers by geometrically dividing the layout hierarchically into thousands of individual “threads.” Each thread is run on a separate processor, multiplying the speed at which results are returned. CalibreMT is enabled with the “turbo” command line option; there are no auxiliary files or setup constraints required. CalibreMT is highly scalable on many CPUs and can continue without a significant increase in RAM.
Advanced DRC Capabilities

The market acceptance of Calibre DRC helps to ensure the capabilities required for advanced checking. The DRC product is continually enhanced to allow for simple rule syntax and the fastest possible performance for the challenges of deep submicron designs. Features include:

- Concurrent checking capabilities allow simultaneous running of multiple checks.
- All-angle checking provides the ability to verify even the most complex analog components.
- Edge-based checking algorithms make identification of geometry lengths and widths simple.
- Quickly identify improper contact/via geometries in a single check.
- Optimally identify difficult contact/via end-of-line enclosure and floating rules properly in a single line.
- Improve the ability to check for tap coverage to diffusion.
- Instantly identify metal slots for verification purposes.
- By outputting errors on a per check basis, DRC debugging can begin well in advance of the full-run completion.

Calibre DRC can be further augmented to properly identify and address yield limiting issues. NET AREA RATIO offers a robust yet comprehensible solution to identifying even the most complex antenna checking capabilities.

- Equation support, incremental connectivity, and charge accumulation.
- Error information is reported with statistics, by net and by layer, dramatically speeding repair.
- Stepped window density checking with support for multiple layer equations, identifies only those regions of a chip with inadequate planarity requirements, even for the most complex process definitions.
- Planarity violations can be quickly resolved with an automated density fill mechanism. The RECTANGLES command allows users to populate low density regions automatically with rectangles of a specified length, width and spacing.
- Dramatically reduce database sizes by recognizing arrayed structures (metal fill, contacts, vias, slots, etc.) and streaming them back as GDSII array references instead of polygon placements.

Powerful LVS Capabilities

Calibre LVS offers efficient and accurate layout device and connectivity extraction as well as circuit comparison. The robust SVRF syntax language ensures that Calibre can compare all device and circuit types. Features include:

- Minimal text methodology dependencies make ramp-up fast and easy.
- Automatic short isolation.
- Standard and user-defined device extraction statements allow users to extract 3, 4, or N-terminal devices easily for digital, analog, and RF designs.
- Robust parameter extraction capabilities allow users to extract standard or complex equation based user defined parameters of any physical data.
- Automated gate recognition, standard device reduction, and other options simplify rule writing.
- Supported extraction and comparison of device M-parameters ensure tight tolerance for analog circuits.
- User-defined device reduction algorithms provide unparalleled user control.
- Verilog translator allows easy input through standard supported SPICE input.
- Calibre Connectivity Interface allows the creation of annotated GDSII for interfacing to third party parasitic extraction products.
**Design Flow Integration**

Because Calibre is easily accessible from within popular layout environments, design teams can adopt a single, efficient physical verification flow. This prevents discrepancies between cell/block and full chip verification and eliminates the duplicate maintenance, training and costs associated with supporting multiple verification tools.

**Calibre RVE**

Calibre’s unique architecture capabilities have been shown to dramatically reduce physical verification runtimes. But physical design is still a highly iterative process, requiring numerous debug and re-verification cycles. For large DSM designs, the time spent in debug can dramatically impact the total time to manufacturing. Calibre RVE specifically addresses this problem by identifying design errors instantly in the user’s own design environment. RVE makes debugging quick and intuitive for cell/block and full chip designs. Features include:

- User-friendly, intuitive graphical interface.
- Sort Calibre DRC results by check or cell.
- Mark Calibre DRC errors as fixed or waived for subsequent runs to save debug time.
- Cross probe results between layout, schematic, source netlist, layout netlist and Calibre LVS result files.
- Automated integration into common layout environments including: Calibre DESIGNrev, Mentor Graphics IC Station, Cadence Virtuoso, Seiko, Avanti Apollo Avanti Enterprise and more.
- Highlight to schematic capture products including: Mentor Graphics Design Architect-IC and Cadence Composer.
- Automated short isolation debugging makes even the most complex power ground short simple to fix.
- Fast and intuitive hierarchical SPICE browser for source and layout netlists.
- Export Calibre DRC results back to design database.

Calibre’s RVE hierarchical SPICE netlist browser enables fast and easy traversal through even the most complex netlist. Components are easily distinguishable by color coding and can be quickly highlighted with convenient cross-probing back to layout and schematic forms.

A powerful hierarchical engine is at the core of Calibre’s robust design-to-manufacturing tool suite.
Calibre DRC and LVS can be easily invoked from a pull-down menu in Cadence Virtuoso.

Calibre Interactive

Identifying physical errors in the user’s existing design database improves total debug time dramatically, but once errors have been identified and debugged, a follow-up verification step is required.

Calibre Interactive reduces the amount of time required to invoke verification runs. Features include:

- Intuitive graphical interface.
- Interactive integration with popular layout tools automates the information required for verification.
- Built-in memory for common run-tasks with runset support.
- Set Calibre LVS run options on the fly.
- Rerun only those Calibre DRC checks effected by previous edits to reduce total runtime.
- Rerun Calibre DRC only in an area where edits have been made to reduce stream-out and total runtime.
- LSF support eases runtime environment constraints.

Calibre DESIGNrev

As database sizes increase, standard layout editors are reaching capacity limits. Making necessary post-DRC or LVS revisions in this type of environment is becoming difficult if not impossible. Calibre DESIGNrev resolves this problem by combining fast, high-capacity GDSII database viewing capabilities with strong revision function. Features include:

- Open multiple gigabyte database files in minutes.
- Translate layer color and fill attributes from common layout environments such as IC Graph and Virtuoso.
- Quickly zoom, pan, and probe hierarchies.
- Forward/back icons remember visualization history.
- Set bookmarks for commonly visited views.
- Merge multiple databases.
- Perform common revision functions including cut, copy, paste, add, delete, move, stretch, notch and more.
- Unlimited undo/redo functionality.
- Keep transcript history of all edits.
- Integration with RVE and Calibre Interactive provides a full-chip, incremental DRC methodology.

Design-to-Silicon Solution

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC, LVS and RVE with xCalibre, Calibre xRC, Calibre RET and Calibre MDP simplifies and strengthens the design flow.

xCalibre, for analog/flat designs and Calibre xRC, for complex, hierarchical designs, accurately model the parasitic effects of passive interconnects that can cause design failure in deep submicron IC designs. Automated interfacing of Calibre LVS to xCalibre/Calibre xRC provides simplicity (one rule file, one invocation), automated back annotation for accurate parasitic extraction results, and ensures accurate and intentional device extraction with parameter calculation and parasitic device extraction for accurate simulation.

The Calibre RET tool suite, Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.
**Design for Manufacturing Silicon Partners Program**

Through Calibre’s Design for Manufacturing Silicon Partners™ program, companies can leverage the relationship that we have secured with the major silicon foundries, library companies and IP providers. Designers gain access to the most extensive set of pre-qualified standard rule files for deep submicron technology processes. This eliminates the time and effort required to translate process rules into verification rule files.

Designers can be confident knowing that libraries and purchased IP have been verified with the same level of accuracy they demand of themselves, and very often with the same technologies used for sign-off at the top foundries.

For more detailed information on industry partners go to www.mentor.com/dsm.

**Foundry Partners**

Complete Calibre rule files and extensive coverage of the DSM processes for both DRC and LVS are available at a majority of the world’s semiconductor foundries, including Chartered, IBM, Jazz Semiconductor, TSMC, and UMC. Calibre is the physical verification tool used internally by Chartered, Jazz Semiconductor, TSMC and UMC.

**Library Partners**

Calibre is the physical verification tool used by Artisan Components, Faraday, Nurlogic, Virage, Virtual Silicon and other respected library houses.

**IP Partners**

Calibre is the physical verification tool used by many IP companies, including Adaptive Silicon, ARM, BOPS, Chip Express, DSP Group, GlobalCAD, Global UniChip, InSilicon, LEDA Systems, MacroTech Research, MIPS Technologies, Nordic VLSI ASA, Rambus, Zoran, and Mentor Graphics own IP division.

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