A Low-Power 20-Gb/s Continuous-Time Adaptive Passive Equalizer

by

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Abstract

The speed of serial link I/O and optical communication systems went beyond 10 Gb/s recently and will continue to increasing. While the advance of silicon technology provides the feasibility of building very-high-speed electronics, communication channel becomes the barrier on the way to further improve the data rate because of its imperfections. One of the most important limitations is due to inter-symbol interference (ISI) which is caused by the fact that the channel response are generally like a low-pass filter, instead of an all-pass filter ideally. To reduce ISI, various equalizers have been devised, and the majority of them are digital or discrete-time implementations. Despite of the existence of vast amount of DSP algorithms to achieve optimum ISI reduction, digital/discrete-time equalizers work at low data rate and consume a lot of power. Conventional continuous-time equalizers utilize active circuitries to obtain gain boosting in high frequencies, thus compensate the channel loss. However, the power consumption is significant, especially as the frequency of operation becomes higher than 10 GHz. This thesis proposes a low-power, 20-Gb/s continuous-time adaptive passive equalizer relying on on-chip lumped *RLC* filter to reduce the power consumption and improve the attainable data rate. A modified continuous-time adaptation servo loop is integrated into the system to automatically adjust the frequency response of the passive equalizer for the optimal gain compensation. The servo generates the control voltage by estimating the power spectrum of the output data from the equalization filter, which is different from the conventional continuous-time adaptation technique, for which a slicer has to be used. Simulations verify the correct operation of the designed equalizer on different channels. Implemented in a 0.13-μm CMOS BiCMOS process, the equalizer can compensate up to 20-dB channel loss at 10 GHz while the power consumption is merely 11.5 mW excluding the output driver. The test chip of the passive equalization filter was fabricated and the measurement data agree with the simulation results.

Acknowledgments

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Chapter 1 Introduction

1.1 Equalization for High-Speed Data Communication

A typical digital data communication system contains three basic building blocks: a transmitter, a receiver and a channel, as illustrated in Figure 1.1. The transmitter converts the digital bits into electrical or optical signals. Signals pass through the transmission channel (copper wire, coaxial cable, and optical fiber etc.) to the receiver. The receiver converts the analog signals back into binary data.

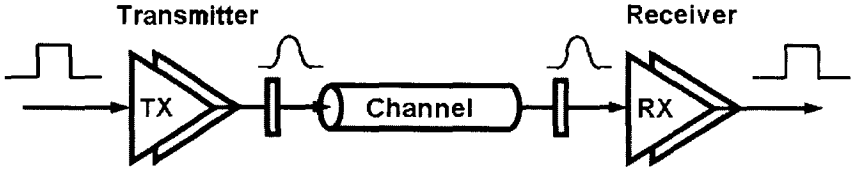
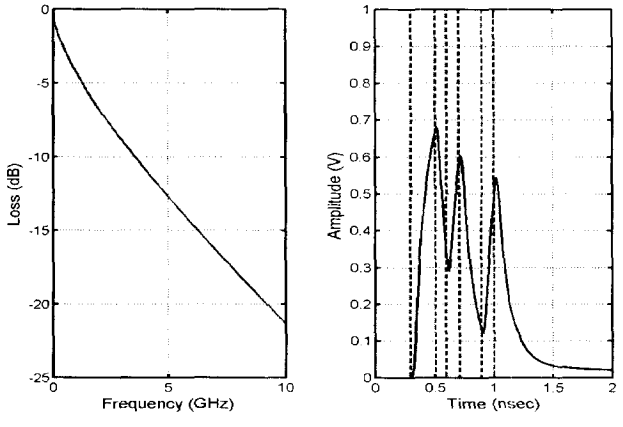


Figure 1.1: Block diagram of a typical high-speed digital data transceiver.



(a) (b)

Figure 1.2: Inter-symbol interference in (a) frequency domain, (b) time domain.

Digital data have a broad spectrum. Unfortunately, a practical baseband communication channel is not an ideal all-pass filter, and as shown in Figure 1.2 (a), it usually behaves like a low-pass filter. As a consequence, different frequency components will lose different amount of power (frequency dependent loss) and experience different amount of phase distortion.

(frequency-dependent dispersion) when propagating through the channel. Both of these effects contribute to the corruption of the original signal, which is the well-known inter-symbol interference (ISI). It is more intuitive to understand the ISI phenomenon in the time-domain, as shown in Figure 1.2 (b). During the transmission, one single bit which ideally should only occupy one unit interval (UI, or bit-time) spreads over several UIs. Obviously, the adjacent bits will be interfered such that an error may occur.

Most of the electrical communication channels are built with copper, and their bandwidths usually are below GHz. To maintain a reliable data communication running at several Gb/s or even higher, equalization is needed to remove or reduce ISI. An equalizer provides an inverse channel response such that the overall (i.e. combination of channel and equalizer) frequency response is flat over the bandwidth of interest. This can be illustrated in Figure 1.3.

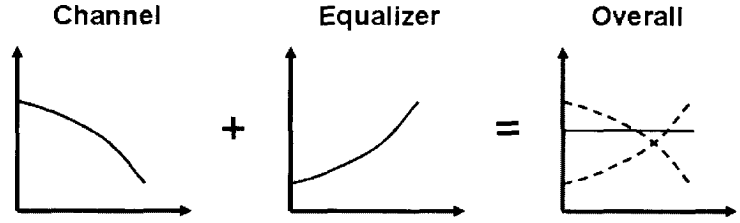


Figure 1.3: Effect of channel equalization.

Theoretically, for a channel which can be modeled as a linear time-invariant (LTI) system, the relation between the received data and the transmitted data can be described by following equation:

$$y_n = \sum_k h_k x_{n-k} = h_0 x_n + \sum_{k \neq 0} h_k x_{n-k} \tag{1-1}$$

where y_n is the received data, x_n is the transmitted data, and h_k is the channel impulse response. The second term in Equation (1-1) represents the ISI. Applying Z-transform to Equation (1-1), we get the according relation in the frequency domain:

$$Y(z) = H_{ch}(z)X(z) \tag{1-2}$$

where $Y(z)$ is the z-transform of y_n, $X(z)$ is the z-transform of x_n, $H_{ch}(z)$ is the channel transfer function. The continuous-time counterpart of Equation (1-2) is:

$$Y(s) = H_{ch}(s)X(s) \tag{1-3}$$

Based on Equation (1-2) and (1-3), one kind of the equalizer is a filter with a frequency response:

$$H_{eq}(s) = \frac{1}{H_{ch}(s)} \tag{1-4}$$

The final output at the receiver is given by

$$Z(s) = H_{eq}Y(s) = H_{eq}(s)H_{ch}(s)X(s) = X(s) \tag{1-5}$$

In the other word, the received data is same as the transmitted data. Such kind of equalization is called linear equalization (LE), which was described in the previous paragraph.

The other kind of equalization is nonlinear decision-feedback equalization (DFE). From Equation (1-1), if an error-correction bit sequence b_n can be constructed such that

$$b_n = -\sum_{k \neq 0} a_k x_{n-k} \tag{1-6}$$

Then after adding y_n and b_n together, we can obtain the error-free data:

$$z_n = y_n + b_n = a_0 x_n \tag{1-7}$$

In general, DFE provides a better performance compared with LE especially in a noisy environment.

For digital or discrete-time implementation, finite-impulse-response (FIR) filter can be used to build both LE and DFE. For multi-Gb/s data link, the digital equalization requires very fast and accurate analog-to-digital converter (ADC) or digital-to-analog converter (DAC), which is costly and power hungry. The discrete-time analog FIR filters are extensively used in today's high-speed transceivers [1][2][3][4][5]. A typical block diagram of such kind of receiver is shown in Figure 1.4. It is easy to identify two feedback loops in the system: one is the adaptation loop inside the equalizer, and the other is the feedback in the timing recovery circuit. As a result, a dilemma of operation may occur: with the ISI, it is hard

to extract correct timing information from the incoming data; at the same time, without a correct clock signal, discrete-time filter cannot work properly. Thus there is a convergence problem in this kind of system. Power consumption of these equalizers is still a concern, especially when the channel response is so complex that the required number of equalization taps is large.

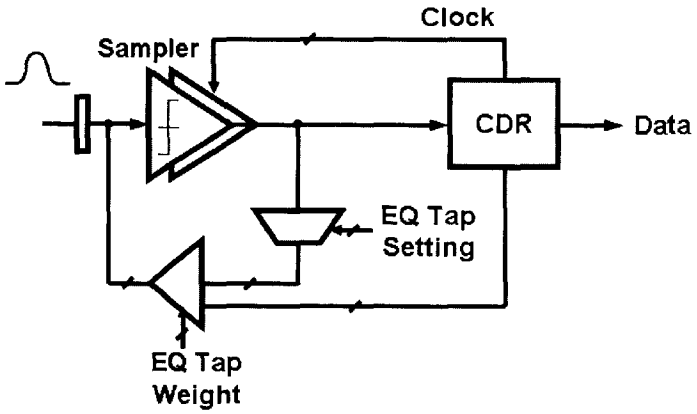


Figure 1.4: Block diagram of a receiver with discrete-time equalization.

To solve these problems, high-speed continuous-time equalizers became attractive [6][7][8][9][10]. However, as most of the continuous-time equalization filters are active circuits, higher speed and lower power consumption is still a challenge.

1.2 Adaptive Equalization Techniques

The characteristics of a communication channel can vary significantly. Temperature, the properties of the materials made of the channel, and the length of cable are all variable. It is desired to design an adaptive equalizer. For digital or discrete-time equalizers, there are many adaptation methods [11][12], for example, least mean square (LMS) algorithms(*). As the contrast, only few adaptation techniques exist for continuous-time equalizers.

One of the most widely used continuous-time adaptive equalization techniques is shown in Figure 1.5 [14][15]. The problem is that the feedback output is only determined by the slope of the data transition, which essentially the high-frequency information of the input

(*) Note: LMS ... ed for continuous-time equalizers, as demonstrated in [13].

signals. If the signal amplitude at point A is not equal to the signal amplitude at point B, as shown in Figure 1.6, although the ISI has been removed at the output of the equalization filter, the adaptive control loop may still output an error signal to change the filter response. This behavior is not desired for the passive equalizer, since the passive filter will attenuate the signal while the limiting amplifier will restore the signal such that the signal amplitudes at A and B are indeed unequal. So, the proper adaptation servo suitable for the passive equalizer has to be developed, which will be discussed in Chapter 2.

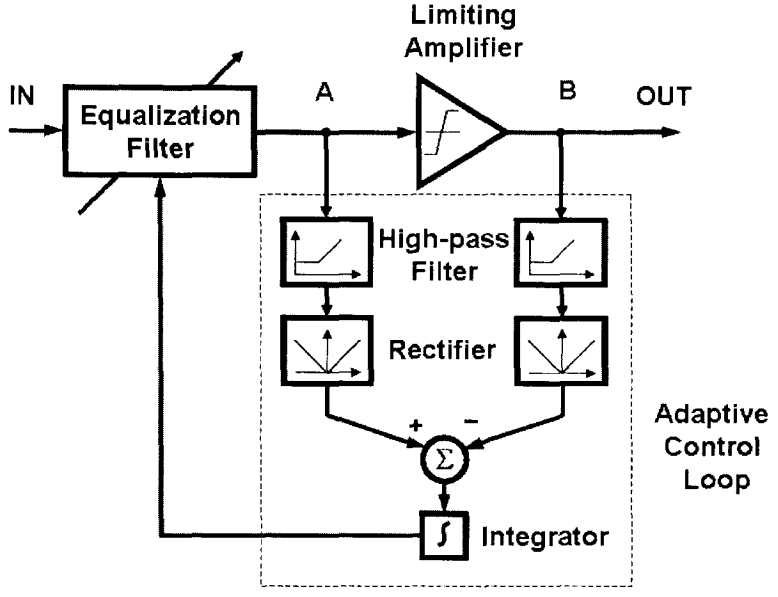


Figure 1.5: Conventional continuous-time adaptive equalization technique.

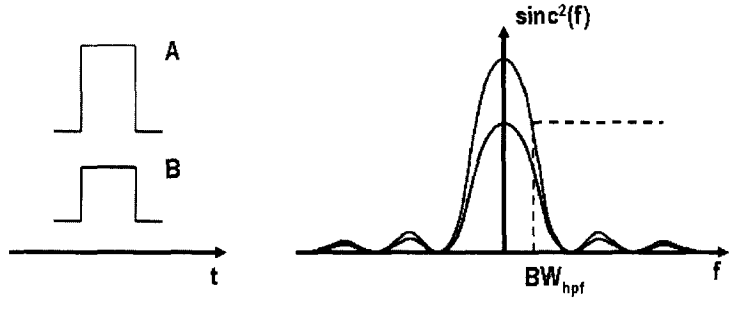


Figure 1.6: Limitation of the conventional continuous-time adaptation technique.

Finally, most of the adaptive equalizers are placed in the receiver, since the information of the channel ISI is embedded in the incoming data and can be easily extracted. However, there are some designs with adaptive equalization in the transmitter, for example, as in [3].

1.3 Organization

As the main motivation is to achieve low power and maintain the flexibility of an adaptive equalizer, a novel continuous-time adaptive passive equalizer is proposed in this thesis. Chapter 2 analyzes the proposed equalizer at the system level. To reduce the power consumption, passive filter was used in place of the active filter. The performance of a tunable on-chip RLC filter will be examined. Because the conventional continuous-time adaptive technique is not suitable for the passive equalizer, it was modified to fit into the new design. The transistor-level circuit design of each building block is explored in Chapter 3. The Spectre® simulation was used to verify the design in various aspects. A new design of the power detector and the error comparator, which overcomes the problem of input offset voltage, is compared with the old design. The new design also simplifies the adaptation servo and saves the power. In Chapter 4, top-level simulation results are discussed, along with the measurement results of the tunable passive equalization filter. It begins with describing the random data generation, which is followed by a discussion of channel modeling. Eye-diagrams are obtained from the Spectre® simulation, and used as the criteria to evaluate the performance of the equalizer. The passive filter was fabricated in a 0.13-μm, 1P8M BiCMOS process, and the measurement results are presented. Chapter 4 ends with a comparison of the performance of our low-power continuous-time adaptive passive equalizer with other recently published state-of-arts continuous-time equalizers. Finally, conclusions are drawn in Chapter 5, and the directions of future works are discussed briefly.

Chapter 2 System Architecture Design and Analysis

The overall system architecture of the proposed equalizer is shown in Figure 2.1. A tunable passive filter performs the equalization function, and the limiting amplifier restores the signal level. Passive equalizers have been commercially available [17], but with fixed equalization. To change the equalization amount, a p-type MOSFET has been used as a variable resistor in the passive filter to obtain an adjustable frequency response. In addition, because the conventional continuous-time adaptation circuit is not suitable for the passive equalizer, a new low-power design of the continuous-time adaptation servo loop will be developed.

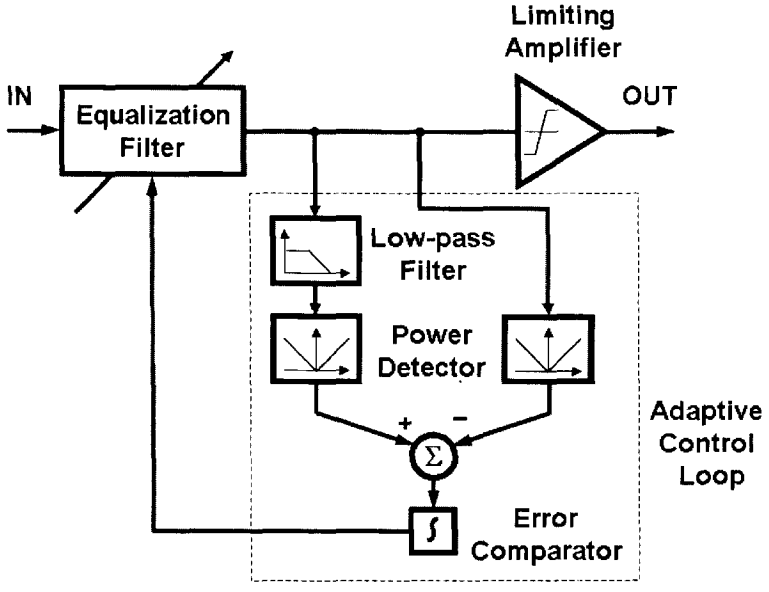
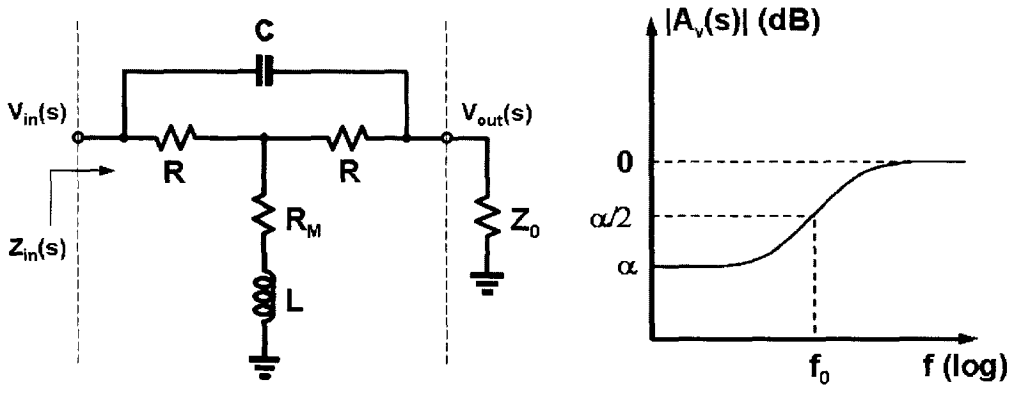


Figure 2.1: System-level block diagram of the adaptive passive equalizer.

2.1 Analysis of the Tunable RLC Passive Filter

The proposed tunable passive equalization filter is based on a RLC filter shown in Figure 2.2. The latter has been widely used as a passive equalizer [17][18] because of two inherit merits: first, with ideal termination (Z_0), the input impedance of the filter will equal to Z_0 at any frequency which ensures an ideal matching; second, the filter characteristic is insensitive

to the parasitics of the RLC components (i.e. Q value of the capacitor and inductor), which is practically important.



(a) (b)

Figure 2.2: An ideal high-pass RLC filter: (a) circuit diagram, and (b) frequency response.

The voltage transfer function of this RLC filter with a load of Z_0 can be derived to be Equation (2-1) (see Appendix A),

$$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{s^2 + s\left(\frac{R_M}{L} + \frac{1}{2RC} + \frac{R}{2L}\right) + \frac{1}{LC}\cdot\frac{R_M}{2R}}{s^2 + s\left[\frac{R_M}{L} + \left(1+2\frac{R}{Z_0}\right)\frac{1}{2RC} + \frac{R}{2L}\right] + \frac{1}{LC}\cdot\left(\frac{R_M}{2R} + \frac{R_M}{Z_0} + \frac{R}{2Z_0} + \frac{1}{2}\right)} \quad (2\text{-}1)$$

and the input impedance is given by Equation (2-2),

$$Z_{in}(s) = \frac{v_{in}(s)}{i_{in}(s)} = Z_0 \frac{s^2 + s\left[\frac{R_M}{L} + \left(1+2\frac{R}{Z_0}\right)\frac{1}{2RC} + \frac{R}{2L}\right] + \frac{1}{LC}\cdot\left(\frac{R_M}{2R} + \frac{R_M}{Z_0} + \frac{R}{2Z_0} + \frac{1}{2}\right)}{s^2 + s\left(\frac{R_M}{L} + \frac{Z_0}{L} + \frac{1}{2RC} + \frac{R}{2L}\right) + \frac{1}{LC}\cdot\left(\frac{R_M}{2R} + \frac{Z_0}{2R} + \frac{1}{2}\right)} \quad (2\text{-}2)$$

To have a constant output impedance equal to Z_0 and a loss of α-dB ($\alpha < 0$) at frequency ω_0 (as indicated in Figure 2.2(b)), the following criteria need to be satisfied,

$$
\begin{aligned}
&K = 10^{-\frac{\alpha}{20}} \ (>1) \\
&\omega_0 = 2\pi f_0 \\
&\frac{\omega_0 L}{Z_0} = \omega_0 C Z_0 = \frac{\sqrt{K}}{K-1} \\
&\frac{R}{Z_0} = \frac{K-1}{K+1} \\
&\frac{R_M}{Z_0} = \frac{2K}{K^2-1}
\end{aligned}
\tag{2-3}
$$

Plug these values into Equation (2-1), then the transfer function becomes,

$$
\begin{aligned}
A_v(s) &= \frac{s^2 + s\cdot\frac{K+1}{\sqrt{K}}\omega_0 + \omega_0^2}{s^2 + s\cdot 2\sqrt{K}\omega_0 + K\omega_0^2} = \frac{\left(s+\sqrt{K}\omega_0\right)\cdot\left(s+\frac{1}{\sqrt{K}}\omega_0\right)}{\left(s+\sqrt{K}\omega_0\right)^2} \\
&= \frac{s+\frac{1}{\sqrt{K}}\omega_0}{s+\sqrt{K}\omega_0} = \frac{s+\omega_z}{s+\omega_p}
\end{aligned}
\tag{2-4}
$$

And surprisingly, this is a very simple first-order system with 1 pole and 1 zero, although in general, Equation (2-1) represents a 2-pole and 2-zero system. The -3-dB bandwidth (ω_{3dB}) is located at,

$$
\omega_{-3dB} = \sqrt{K - \frac{2}{K}}\cdot\omega_0 \cong \omega_p \ \left(for\ K >> 1\right) \tag{2-5}
$$

Equation (2-3) and (2-5) can be used to design the passive equalizer. For example, to construct a filter which can compensates up to 20-dB channel loss (α = -20dB) at 10GHz ($\omega_{3dB} = 2\pi\times 10$Grad/s), then the procedure is,

1. Using Equation (2-3) to calculate K;
2. Using Equation (2-3) to get the values of R and R_M;
3. Using Equation (2-5) to determine ω_0;
4. Using Equation (2-3) to calculate the values of L and C.
5. Equation (2-2) automatically gives us $Z_{in} = Z_0$.

A Matlab program has been written to calculate the desired R, L, and C values, which is given in Appendix A.

Figure (2-1) tells us

$$A_{DC} = \frac{\frac{R_M}{2R}}{\frac{R_M}{2R} + \frac{R_M}{Z_0} + \frac{R}{2Z_0} + \frac{1}{2}}, \quad A_{f\to\infty} = 1 \tag{2-6}$$

where A_{DC} is the dc gain and $A_{f\to\infty}$ is the high frequency gain. Equation (2-6) implies that the maximum equalization that the filter can provide is (in dB),

$$\begin{aligned} A_{f\to\infty,dB} - A_{DC,dB} &= 20\log_{10}\left(\frac{\frac{R_M}{2R} + \frac{R_M}{Z_0} + \frac{R}{2Z_0} + \frac{1}{2}}{\frac{R_M}{2R}}\right) \\ &= 20\log_{10}\left(1 + \frac{2R}{Z_0} + \frac{\frac{R}{Z_0}+1}{\frac{R_M}{R}}\right) \end{aligned} \tag{2-7}$$

Apparently, this value will decrease monotonically as R_M increases. In the other words, if we can change the value of R_M, then we have a tunable equalizer. This leads to the circuit shown in Figure 2-3, where R_M is replaced by a MOSFET working in triode region whose resistance depends on the gate voltage.

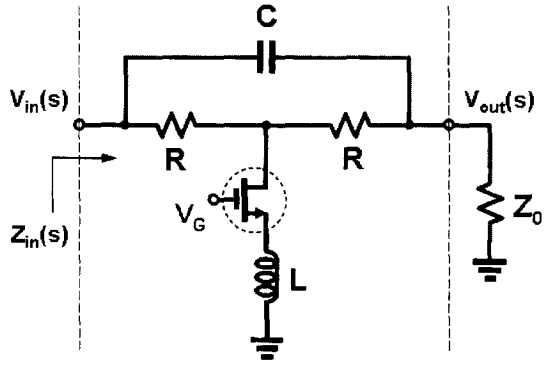


Figure 2.3: Tunable high-pass RLC filter: a MOSFET-R-L-C version.

There are two variables in Equation (2-6) that determine the attenuation: R_M and R. The main reason that we choose R_M instead of R is because of the simplicity of the circuit. However, this choice does impose limitation of the equalizer tuning range. As R_M

approaches infinity, Equation (2-7) approaches a minimum value of 8.42dB for α = 20dB. So the tuning range is only about 12dB.

How will input impedance change as we change R_M? It should not deteriorate the property of perfect matching in the original ideal condition. Fortunately, as can be verified by the simulation results (presented in Chapter 3), S_{11} is kept within a reasonable range.

Finally, a practical issue is the effect of the loss associated with the real R, L and C components on the filter performance. Theoretically, a filter with ideal behavior described previously is still realizable given the quality factors (Q) of inductors and capacitors are equal and satisfy the following condition, [17]

$$Q > \sqrt{K} = 10^{\frac{\alpha}{40}} \tag{2-8}$$

For out design target, this translates to a minimum device Q about 3.2. However, it is difficult to maintain a constant Q over a broadband and to have equal Qs for inductors and capacitors. Fortunately, as can be seen from the simulation results presented in next Chapter, the existence of the parasitics does not change the frequency response of the filter from the ideal case dramatically. In fact, very little difference was observed (Figure 3.2).

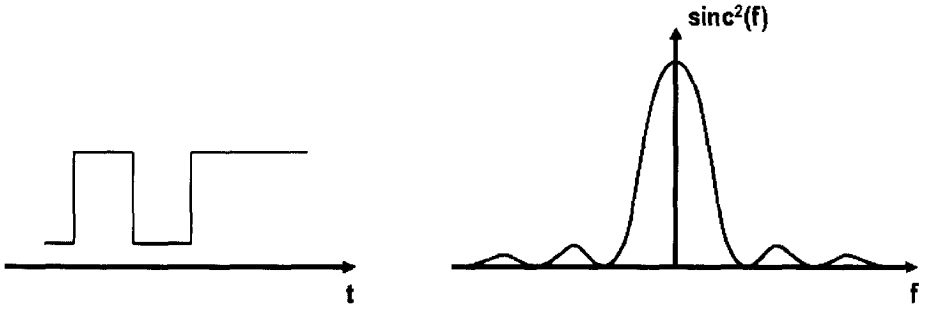
2.2 A Modified Continuous-Time Adaptation Technique

As being pointed out in Chapter 1, the conventional continuous-time adaptation loop cannot satisfy the need of an adaptive passive equalizer because the signal amplitudes before and after the equalization filter are different. To overcome this problem, a suitable adaptation scheme has to be developed.

As we know, the power spectrum of a pseudo-random bit sequence (PRBS) with the ideal pulse shape (i.e., a square waveform) can be described by [19],

$$S(f) = A^2 T \, sinc^2(fT_b) \tag{2-9}$$

where, A is the amplitude, T is the UI. This is illustrated in Figure 2-4.



(a) (b)

Figure 2.4: A pseudo-random bit sequence in (a) time domain, and (b) frequency domain.

The ratio of the signal powers at any two frequencies is thus fixed. For instance, for a 20-Gbit/s PRBS at 100MHz (f_1) and 10GHz (f_2), this ratio is then given by

$$\frac{P_1}{P_2} = \frac{\sin c^2(\pi f_1 T_b)}{\sin c^2(\pi f_2 T_b)} = \frac{\sin c^2(100M \times 50p \times \pi)}{\sin c^2(10G \times 50p \times \pi)} \cong 2.47 \qquad (2\text{-}10)$$

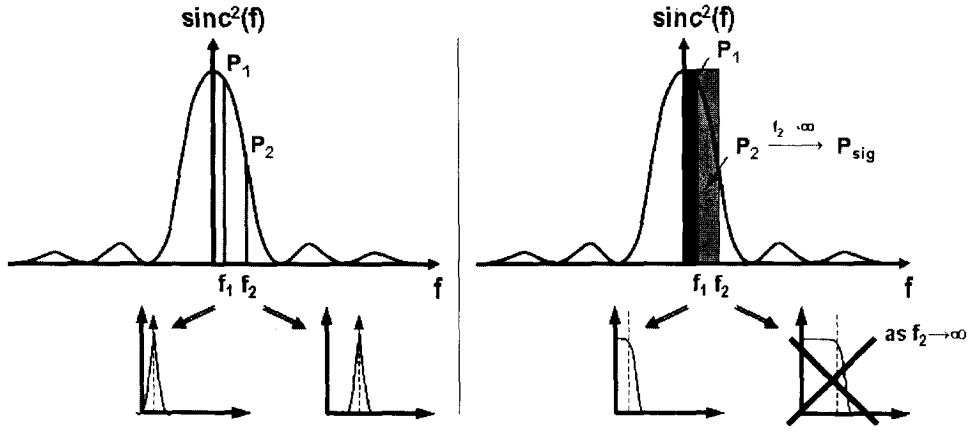
If we could sense the powers at above frequencies of a post-equalized PRBS signal, and compare the ratio with the value given by Equation (2-10), we are able to obtain an error signal to control the equalizer. The signal power at a specific frequency can be measured by using a band-pass filter centered at that frequency followed by a power detector. Unfortunately, building a band-pass filter with very high center frequency is impractical due to large power consumption. Although we can reduce the center frequency, the power ratio will become too small to be accurately sensed.

An alternate way is to check the ratio of the signal power within two different frequency ranges. For example, we can calculate the ratio of the signal power within (*DC*, 100 MHz) and (*DC*, *infinity*) for the same PRBS:

$$\frac{P_1}{P_2} = \frac{\int_0^{\pi \cdot f_1 T_b} \sin c^2(x)dx}{\int_0^{\infty} \sin c^2(x)dx} \cong 98 \qquad (2\text{-}11)$$

Apparently, now the band-pass filter can be replaced with a low-pass filter. In addition, the denominator in Equation (2-11) simply implies all of the signal power, and it in turn [illegible] es

to connect the input signal directly to the power detector. Consequently, only one low-pass filter is needed. The principle of this new continuous-time adaptive scheme can be illustrated in Figure 2-5. The function block diagram is already shown in Figure 2-1.



(a) Band-pass approach (b) Low-pass approach

Figure 2-5: Principle of the adaptation scheme for the passive equalizer.

There are two notes worth being mentioned. First, the result obtained from Equation (2-11) is power ratio, so the voltage gain the low-pass filter will be the square-root of this value (for example, ~10 for the power ratio given in Equation (2-11)). Besides, in practice, the power detector cannot detect signal power over all frequencies, so the real value will be slightly different from the theoretical value. Secondly, if we are using a one-pole low-pass filter instead of the ideal low-pass filter (i.e. the one with brick-wall response), the equivalent cut-off frequency is given by [20]

$$BW_{cut-off} = \frac{\pi}{2} BW_{-3dB} \tag{2-12}$$

where, BW_{-3dB} is the -3dB-bandwidth of the low-pass filter.

2.3 Summary

In this chapter, we first examine in detail the behavior of a passive equalization filter with fixed frequency response. Since it's necessary to obtain tunable frequency response to form

an adaptive system, a tuning mechanism is established based on the analysis of the original filter. Also, a new feedback servo is developed to fit into the adaptive passive equalizer system. The property of the power spectrum of a random bit sequence is utilized to obtain the necessary control signal (this also impose a limitation that the incoming data have to be "random" enough to make the adaptation work). Compared with the conventional implementation, this new servo circuitry potentially consumes lower power due to the elimination of band-pass filter.

Chapter 3 Design of Equalizer Components

In this chapter, transistor-level implementation of the adaptive passive equalizer will be discussed. A high-performance BiCMOS technology was used to design the circuits, but bipolar devices were only used in the output stage. Whenever possible, fully differential (FD) circuits are employed to improve the noise immunity. Two different implementations of the adaptive control loop are explored and compared, and the new design improves the performance reliability.

3.1 Passive Equalization Filter

Based on the discussion in the section 2.1, it is straightforward to implement the passive equalization filter. The circuit diagram of a fully differential implementation is shown in Figure 3.1. The biasing of the MOSFET is established by setting the common-mode voltage of the input differential signals at 0.95 V, while the equalizer is DC coupled to the channel.

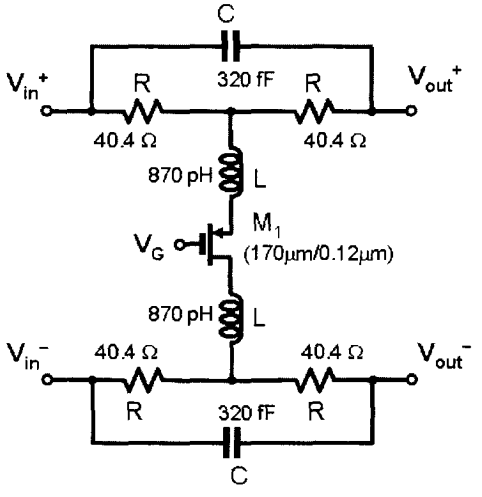


Figure 3.1: Circuit diagram of the differential passive equalization filter.

In Figure 3.2, the simulated S_{21} of this filter are compared with that of an ideal filter (i.e. consisting ideal R, L and C elements). The results are well matched, which indicates the circuit is insensitive to the device parasitics.

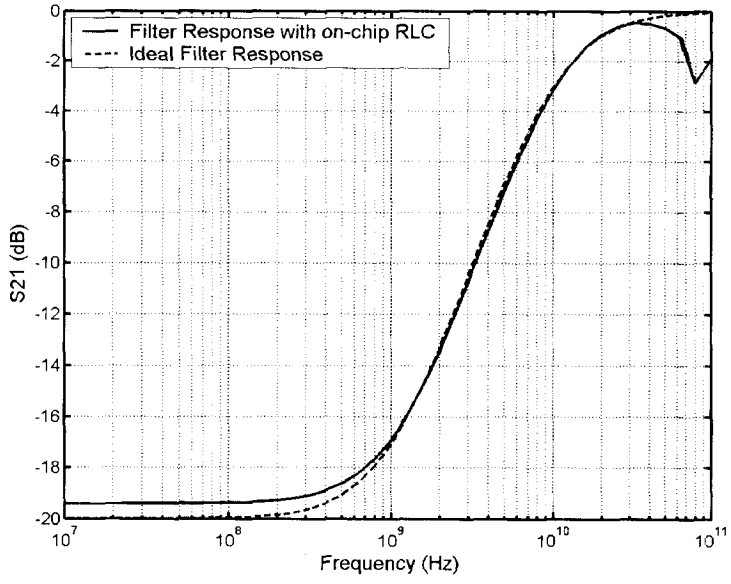


Figure 3.2: S_{21} of the passive equalization filters.

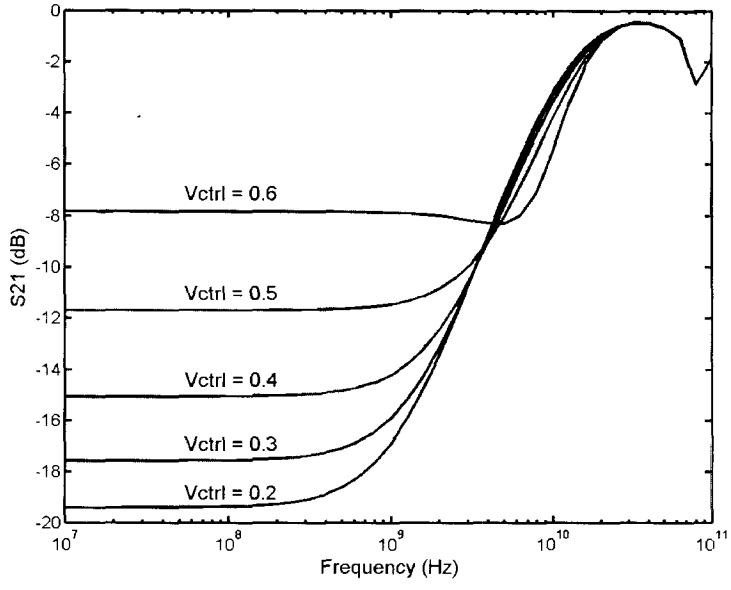


Figure 3.3: Tuning of the S_{21} of the passive equalization filter.

Figure 3.3 demonstrates the tuning capability of the filter. As expected, the tuning range is limited to be about 12dB, and the minimum attenuation (about 8dB) is obtained when the pMOS enters cut-off region. As shown in Figure 3.4, S_{11} is below -10dB for the entire tuning range.

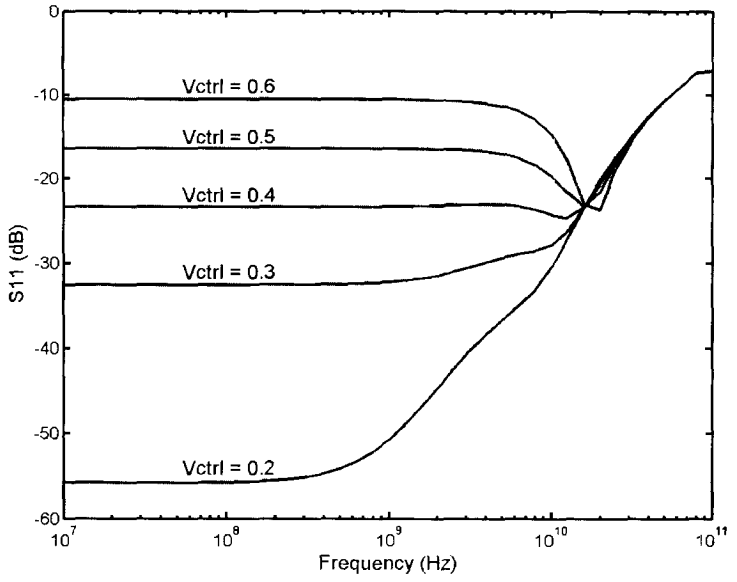


Figure 3.4: Variation of S_{11} of the passive equalization filter.

3.2 Output Stage

The function of the output stage is to restore the signal amplitude due to the attenuation of the passive equalization filter. In a first glance, it seems to be a natural choice to use a linear amplifier with a gain of 20dB. However, the bandwidth then needs to be at least 10GHz. This results in a desired gain bandwidth product (GBW) of more than 100GHz, which increases the difficulty of design. Divide-and-conquer method can be applied to ease the design. In reality, the next stage following the passive equalization filter will be either an output driver (for stand-alone application, as in this project) or a receive sense amplifier (for integrated solution), and in both cases, as long as the amplitude of the input signal is large enough to switch the output gate, the correct output can be obtained. Consequently, the output stage can be divided into two sub-stages: (1) the first sub-stage is a pre-driver, which should have *just* enough gain such that its output signal is able to completely switch the second stage; (2) the second sub-stage can be either a output driver with large bias current to drive off-chip 50Ω load, or a latch, which uses positive feedback to regenerate the signal.

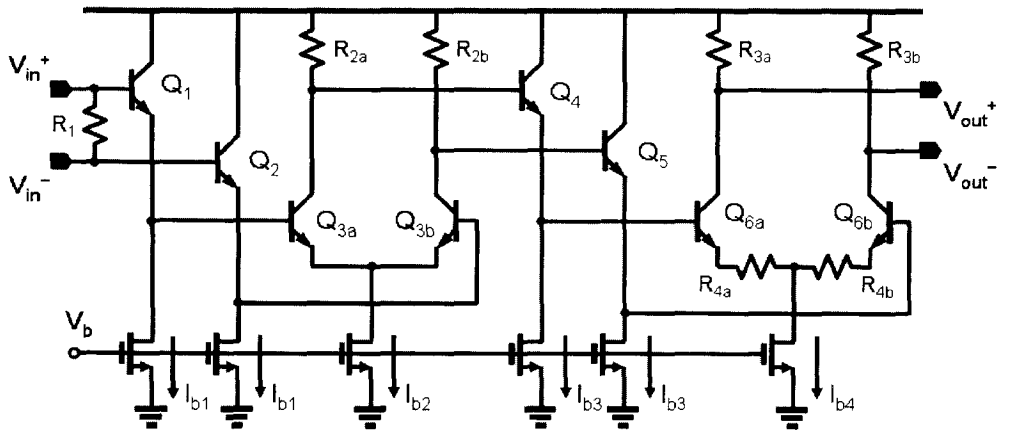


Figure 3.5: Circuit diagram of the fully differential output stage.

Table 3.1: Design parameters of the output stage.

Device	Value	Device	Value
Q_1, Q_2	1 μm × 0.12 μm	R_{3a}, R_{3b}	76 Ω
Q_{3a}, Q_{3b}	1 μm × 0.12 μm	R_{4a}, R_{4b}	7 Ω
Q_4, Q_5	1 μm × 0.12 μm	I_{b1}	0.82 mA
Q_{6a}, Q_{6b}	1 μm × 0.12 μm	I_{b2}	0.85 mA
R_1	100 Ω	I_{b3}	2.07 mA
R_{2a}, R_{2b}	184 Ω	I_{b4}	13.63 mA

The circuit diagram of the output stage designed in BiCMOS technology is shown Figure 3.5, and the design parameters are given in Table 3.1. A 100-Ω resistor at the input is used to provide proper termination for the passive equalization filter. At the output, 75-Ω on-chip resistors are used to reduce the effect of double reflections on the output transmission line. This resistance value, although it is not ideally 50 Ω, will provide a reflection coefficient (S_{22}) less than -14 dB. At the same time, it reduces the amount of bias current in the output driver for a given output signal amplitude. To obtain 0.8-V differential peak-to-peak output signal swing, I_{b4} is about 13.33 mA. Care must still be taken of choosing proper device size (and metal width when doing layout) to accommodate such amount of current.

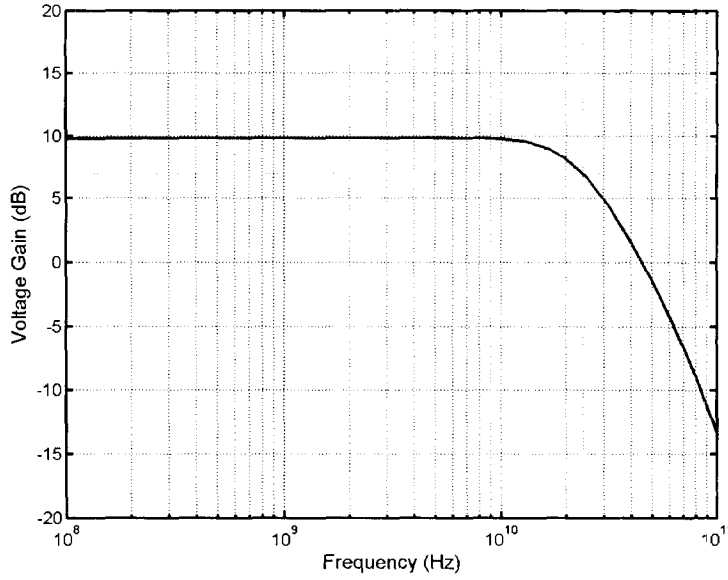


Figure 3.6: Frequency response of the pre-driver.

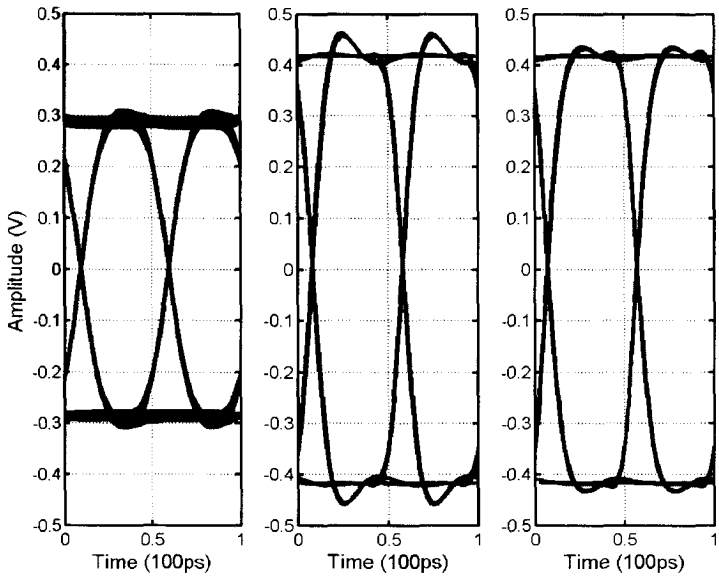
Due to the large current driving ability of the *npn* bipolar transistor, the output driver can be fully switched by an input signal with relatively small amplitude. To see this, assume the switching of the differential pair occurs when the currents flowing through Q_{6a} and Q_{6b} differ by 100 times, then

$$\begin{aligned} & I_{cc,Q_{6a}} = I_S e^{\frac{V^+ - V_e}{V_T}}, \quad I_{cc,Q_{6b}} = I_S e^{\frac{V^- - V_e}{V_T}} \\ & \Rightarrow \frac{I_{cc,Q_{6a}}}{I_{cc,Q_{6b}}} = e^{\frac{V^+ - V^-}{V_T}} = e^{\frac{V_{in,pp-s}}{V_T}} = 100 \\ & \Rightarrow V_{in,pp-s} \cong 4.6 \times V_T \cong 120mV \end{aligned} \tag{3-1}$$

where, $I_{cc,Q6a}$ and $I_{cc,Q6b}$ are the currents flowing through the left and right sides of a differential pair; $V_{in,pp-s}$ is the single-ended peak-to-peak input signal swing of the output driver; V_e is the common-emitter voltage; $V_T = kT/q$ = 26mV at room temperature. To have a safety margin, assume the minimum $V_{in,pp-s}$ is 150mV. In the worst case, the single-ended peak-to-peak voltage of the input signal to the pre-driver is 50mV (i.e. 500mV input signal attenuated by 20-dB by the passive filter). As a result, only 3V/V (~10dB) gain is needed for the pre-driver. Because of npn BJT with f_t around 200GHz was used, resistor-loaded

differential amplifier (as shown in Figure 3.5) will satisfy the design targets. None of the special bandwidth enhancement techniques, such as inductor shunt peaking and capacitor emitter degeneration, were used. The frequency response of the pre-driver is shown in Figure 3-6 in the previous page, where a -3-dB bandwidth about 24GHz can be found.

The emitter followers inside the circuit have two functions: (1) level shifting; and (2) isolation of the load capacitance. However, they may cause extra ringing in the output signal due to its second-order transfer function and the possible complex poles [19]. This may explain the overshoot of the output signal in the eye-diagrams shown in Figure 3.7. The output signal amplitude limiting function is also apparent in Figure 3.7.



(a) (b) (c)

Figure 3.7: Eye-diagrams of the output signals of the output driver: (a) input amplitude = 50 mV, (b) input amplitude = 250 mV, (c) input amplitude = 500 mV.

The bias voltage is generated by using a replica bias circuit. The circuit is shown in Figure 3.8 and the design parameters are given in Table 3.2. The size of the replica is scaled down by 4 times to save power. The internal reference voltage (V_{ref}) is created by a resistor divider connecting between power supply and ground. The voltage swing of the output signal

is determined by Equation (3-5), and it is relatively insensitive to the process and temperature variations.

$$V_{out,pp-s} = V_{DD} - V_{ref} = \left(1 - \frac{R_1}{R_1 + R_2}\right) \cdot V_{DD} = \frac{1}{\left(\frac{R_1}{R_2}\right) + 1} \cdot V_{DD} \tag{3-5}$$

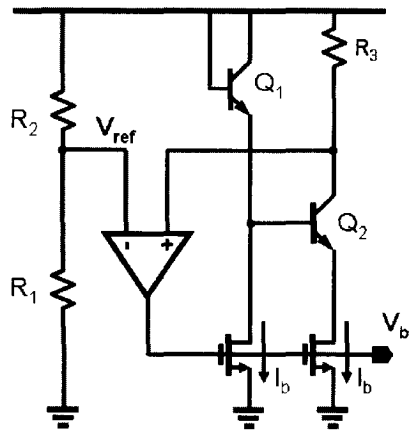


Figure 3.8: Circuit diagram of the biasing circuit of the output stage.

Table 3.2: Design parameters of the output biasing circuit.

Device	Value	Device	Value
Q_1, Q_2	0.6 μm × 0.12 μm	R_3	735 Ω
R_1	1.6 kΩ	I_b	0.21 mA
R_2	19.2 kΩ		

The large gate capacitance of the biasing nMOS transistors (about 2 pF) place a dominant pole at the output of the opamp, and the loop stability is ensured by this fairly low dominant pole. As can be seen from Figure 3.9, a phase margin larger than 90° is achieved.

The total power consumption of the output stage is about 41 mW, while the pre-driver only consumes 9.7 mW.

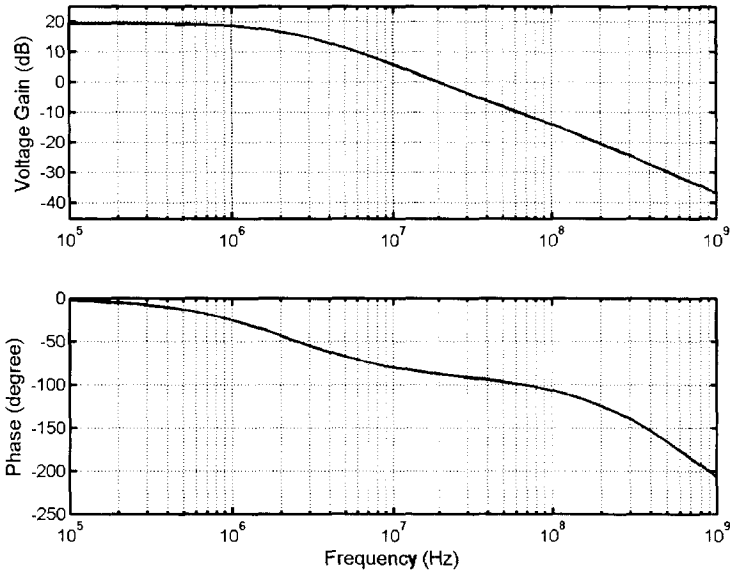


Figure 3.9: Open-loop frequency response of the feedback in the replica bias circuit.

3.3 Adaptive Control Loop

In the first attempt to implement the adaptive control loop shown in Figure 2-1, the power detector was implemented using an "alternating-voltage-follower"[21] and the error comparator was a high-gain amplifier. However, this kind of comparator is very sensitive to the input offset voltage. The need for offset cancellation circuit complicates the design. To solve this problem, a new circuit was developed. In addition, this new circuit integrates the functions of power detection and error comparison, which simplifies the design. In both approaches, the same low-pass filter design was used, so we start with discussing the low-pass filter design.

3.3.1 Low-Pass Filter

The design target of the low-pass filter is such that only signal contents within a frequency band can pass through, and at the same time, they are amplified such that the power of the filtered signal is equal to the total power of the original signal. A lower bandwidth means a higher gain to achieve this goal. Several possible bandwidths and gains are listed in Table 3.1. They are calculated using Equation (2-10) and (2-11).

Table 3.3: Possible design specifications for the low-pass filter.

-3-dB Bandwidth (MHz)	DC Gain (V/V)	GBW (MHz)
50	11.2	560
100	7.9	790
150	6.5	975

Lower GBW (gain-bandwidth product) implies ease of the design and smaller power consumption, but higher gain will raise the problem of the input offset voltage. Thus, a compromise was made in this project and the designed filter has a DC gain about 6 V/V (~16 dB) and a bandwidth of about 120 MHz, as shown in Figure 3.11. The circuit diagram is shown in Figure 3.10, and the design parameters are given in Table 3.4. This fully-differential amplifier doesn't need a common-mode feedback circuit. An nMOS is used as an adjustable resistor to control the gain as well as improve the linearity. The power consumption is about 1.2mW.

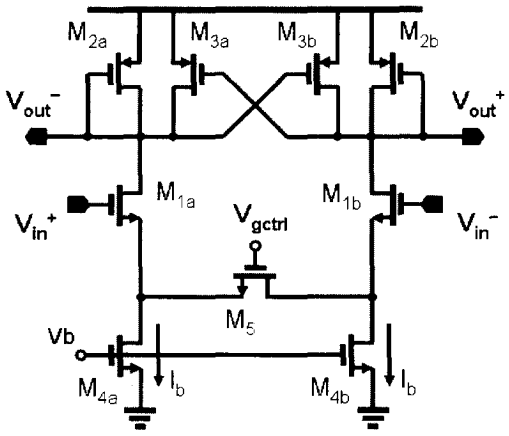


Figure 3.10: Circuit diagram of the low-pass filter.

Table 3.4: Design parameters of the low-pass filter.

Device	Value	Device	Value
M_{1a}, M_{1b}	20 μm / 0.2 μm	M_5	40 μm / 0.2 μm
M_{2a}, M_{2b}	49.6 μm / 0.4 μm	I_b	0.45 mA
M_{3a}, M_{3b}	43.4 μm / 0.4 μm		

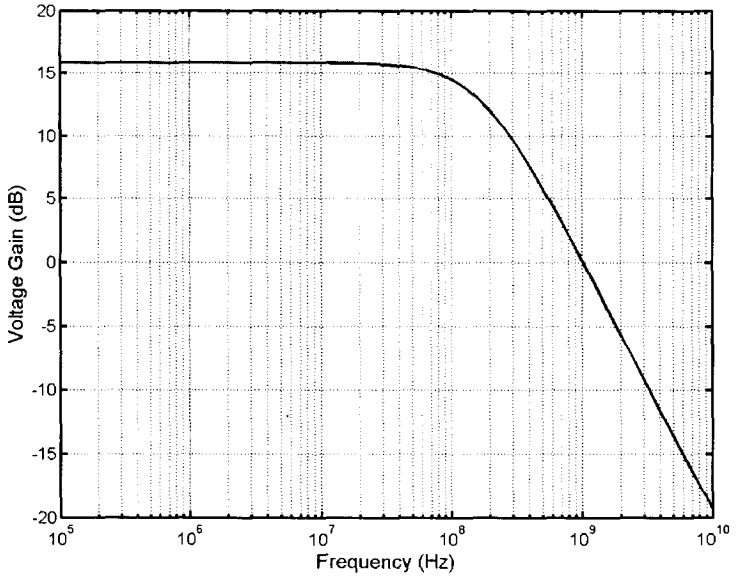


Figure 3.11: Frequency response of the low-pass filter.

3.3.2 Old design of power detector and error comparator[21]

As already being pointed out, although this design approach was found to be problematic with the input offset voltage, it is still discussed here because it provides us a better understanding of the design issues inside the servo loop.

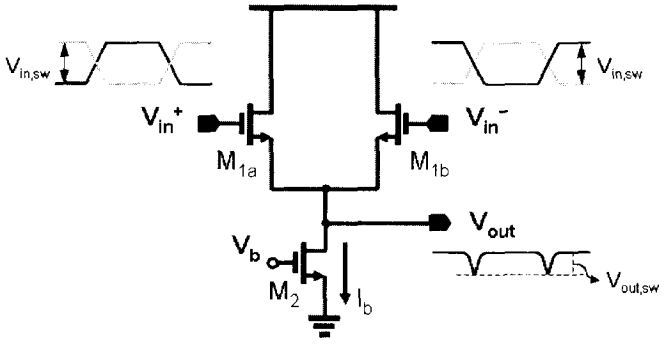


Figure 3.12: Circuit diagram of the power detector.

Shown in Figure 3.12 is the circuit diagram of the power detector. Note that the output is at the coupled source node of a differential pair. If the gate overdrive voltage (V_t) is small compared with the input signal amplitude, M1a and M1b will alternately conduct

such that the output follows the positive and negative input signals during two half cycle of the input signal. In this way, the output is a rectified version of the input signal. The design parameters of the circuit shown in Figure 3.12 are given in Table 3.5. However, if the input signal swing is small, for example, as in this project it could be as small as 50-mVpp, then the transistors are not fully switched, and the output signal swing turns out to be very small, as can be confirmed by the simulation results shown in Figure 3.13.

Table 3.5: Design parameters of the power detector.

Device	Value	Device	Value
M_{1a}, M_{1b}	80 μm / 0.12 μm	I_b	0.7 mA

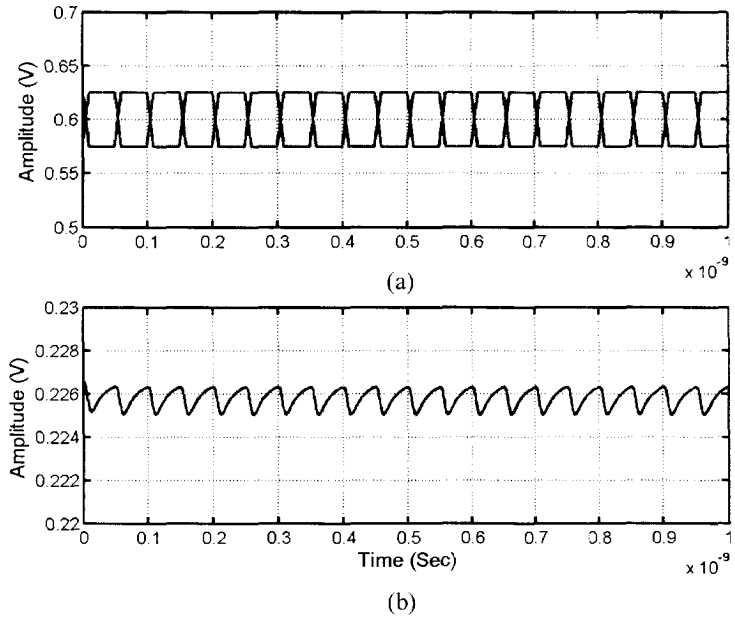


Figure 3.13: Input and output signals of the power detector: (a) input, and (b) output.

The circuit diagram of the error comparator is shown in Figure 3.14, and the design parameters are given in Table 3.6. It is a two-stage amplifier. The lead compensation is not necessary if the amplifier was not used in a feedback, which is the case when such an amplifier is used as a comparator. However, for some input-offset cancellation circuits, unity-gain feedback is employed (as will be seen shortly), so the loop stability has to be ensured. Simulation gives about 60 dB DC gain and larger than 80 degree phase margin, as shown in Figure 3.15.

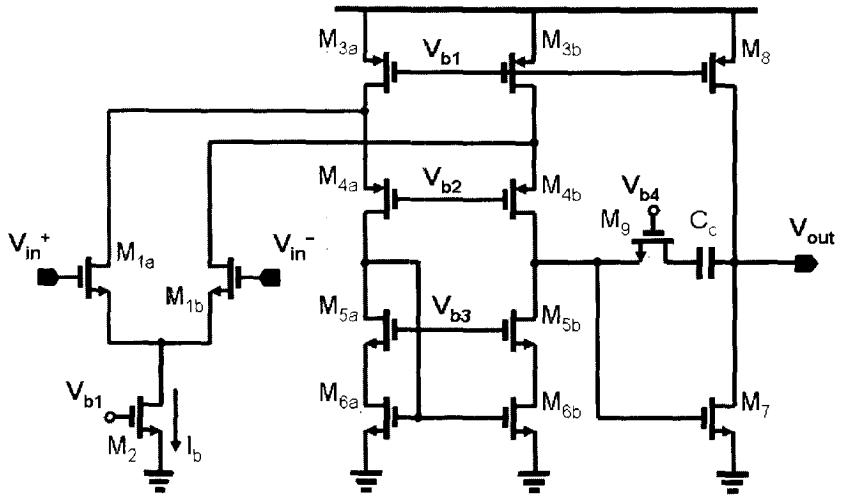


Figure 3.14: Circuit diagram of the error amplifier.

Table 3.6: Design parameters of the error amplifier.

Device	Value	Device	Value
M_{1a}, M_{1b}	60 μm / 0.3 μm	M_7	20 μm / 1.6 μm
M_{3a}, M_{3b}	120 μm / 1.6 μm	M_8	60 μm / 1.6 μm
M_{4a}, M_{4b}	120 μm / 1.6 μm	M_9	30 μm / 1.6 μm
M_{5a}, M_{5b}	40 μm / 1.6 μm	C_c	3.6 pF
M_{6a}, M_{6b}	50 μm / 1.6 μm	I_b	58 μA

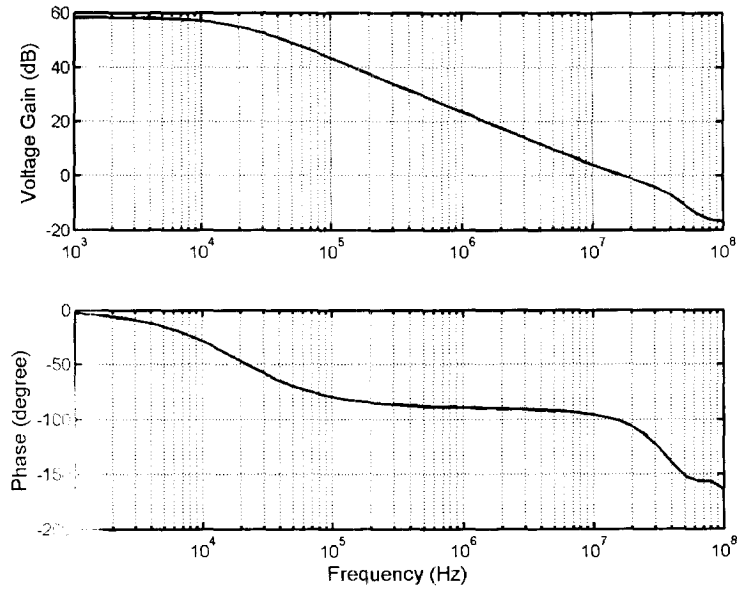


Figure 3.15: Frequency response of the error amplifier.

The very small input signal and the very high gain cause the output signal can easily be corrupted by the input offset voltage. There are several techniques to reduce the input offset voltage, and one of them is called "input offset storage" [20][23] and shown Figure 3.16. However, all of these techniques increase the design complexity (due to the additional switches and the required clock signals).

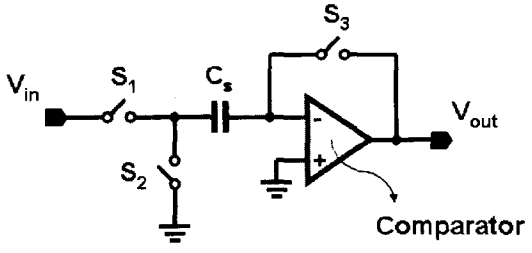


Figure 3.16: An input offset cancellation technique for the error amplifier.

3.3.3 Improved design of the power detector and error comparator

The proposed design utilizes the unique characteristic of a differential pair to detect the signal power. Shown in Figure 3.17 is an nMOS pair. The total current flowing through it is,

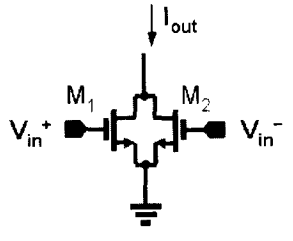


Figure 3.17: A coupled differential pair.

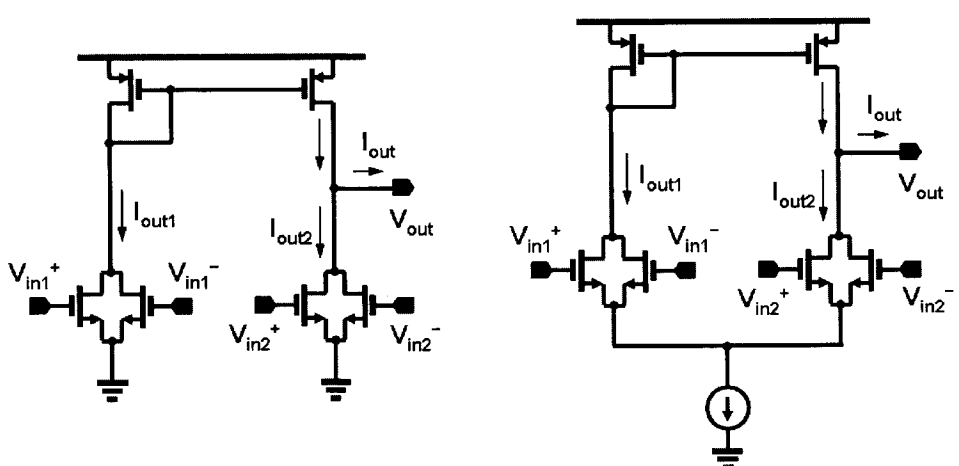
$$
\begin{aligned}
I_{out} &= I_{ds1} + I_{ds2} \\
&= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{in,cm} + \frac{V_{in,dm}}{2} - V_{tn}\right)^2 + \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{in,cm} - \frac{V_{in,dm}}{2} - V_{tn}\right)^2 \\
&= \mu_n C_{ox}\left(\frac{W}{L}\right)\left[\left(V_{in,cm} - V_{tn}\right)^2 + \frac{V_{in,dm}^2}{4}\right]
\end{aligned}
\tag{3-6}
$$

where I_{ds1} and I_{ds2} are the drain currents of M_1 and M_2, respectively; $V_{in,cm}$ is the input common-mode voltage; $V_{in,dm}$ is the input differential-mode voltage. Clearly I_{out} is a measure

of the input signal power because of the squaring term of Equation (3-6). Above conclusion can be extended to the case that the current-voltage relation doesn't obey square law, such as for short-channel MOSFET. As long as the relation can be expressed in the form of a Taylor series, only even-order terms of $V_{in,dm}$ affect the total output current.

Based on this mechanism, two types of circuits have been developed, which perform power detection and error comparison simultaneously, as shown in Figure 3-18 (a) and (b), respectively. In both of the circuits, one of the nMOS pairs generates a current (I_{out1}) proportional to the signal power of V_{in1}, while the other generates a current (I_{out2}) representing the signal power of V_{in2}. The active load mirrors I_{out1} to the output node, thus the output current (I_{out}) is the difference of two currents (Equation (3-7)). As a result, the comparison function is realized.

$$I_{out} = I_{out1} + I_{out2} = \frac{1}{4}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{in1,dm}^2 - V_{in2,dm}^2\right) \tag{3-7}$$



(a) Type-I (b) Type-II

Figure 3.18: The improved power detector: (a), Type-I, and (b) Type-II.

Type II design was used in this project, and the circuit diagram of the final implementation is shown in Figure 3-19. The design parameters are given in Table 3.7. Transistor M_{3a} and M_{3b} are used to improve the gain. The second stage is used to obtain a

wide output swing. The operation is same as described previously. Because the input signal now directly comes from the equalizer output, the amplitude becomes much larger. As a consequence, the effect of the input offset voltage is reduced.

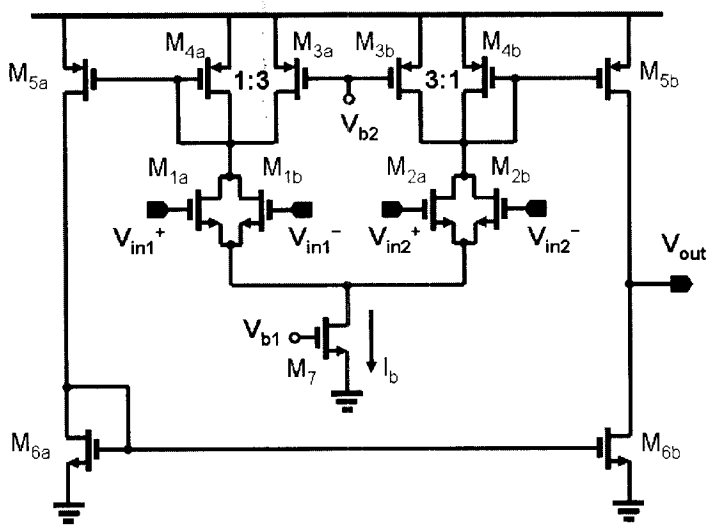
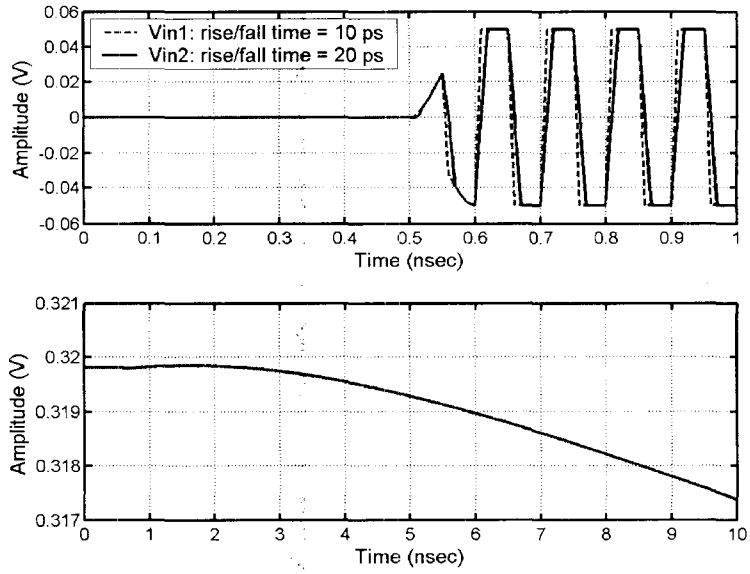


Figure 3.19: Improved design of the power detector and error comparator.

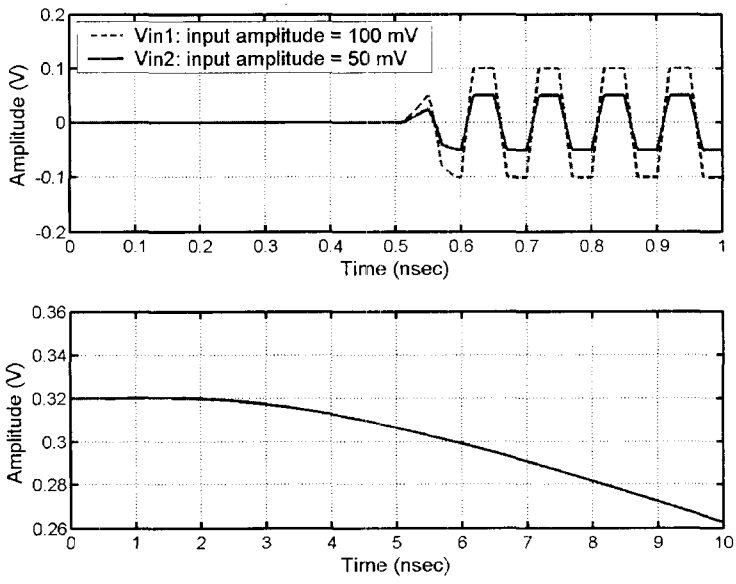
Table 3.7: Design parameters of the circuit shown in Figure 3.19.

Device	Value	Device	Value
M_{1a}, M_{1b}	10 μm / 0.5 μm	M_{5a}, M_{5b}	36 μm / 1.5 μm
M_{2a}, M_{2b}	10 μm / 0.5 μm	M_{6a}, M_{6b}	8 μm / 1.5 μm
M_{3a}, M_{3b}	54 μm / 1.5 μm	I_b	0.2 mA
M_{4a}, M_{4b}	18 μm / 1.5 μm		

The functionality of the circuit shown in Figure 3.19 can be demonstrated by simulation results, as shown in Figure 3.20. In the simulations, both V_{in1} and V_{in2} are periodic pulse signals. In Figure 3.20 (a), they have same amplitudes, but the rising and falling times of V_{in1} is shorter than those of V_{in2}. In Figure 3.20 (b), the amplitude of V_{in1} is larger while the rising and falling times are same. In both cases, V_{in2} has a less signal power than V_{in1}. Accordingly, the output signal continuously decreases to reflect the fact that in both cases, the signal power of V_{in1} is larger than that of V_{in2}.



(a)



(b)

Figure 3.20: Functionality of the improved design: two inputs with (a) different rise/fall times, and (b) different amplitudes.

3.4 Summary

The transistor-level design of the adaptive passive equalizer is discussed in this chapter. Reducing the power consumption and the design effort are main design guidelines. Designing

the passive equalization filter is straightforward. With high-performance BiCMOS technology, the high-speed output stage is readily realizable. The low-pass filter is essentially a fully differential amplifier without CMFB. A new circuit, which merges power detection and error comparison together, was designed to relief the problem of the input offset voltage encountered in the previous design. With this circuit, the block diagram shown in Figure 2.1 can be simplified, as shown in Figure 3.21. The new servo loop only consists of two blocks, so the design complexity is greatly reduced. New design also lowers the power consumption, as can be found in Table 3.8, where the performances of each building block are summarized.

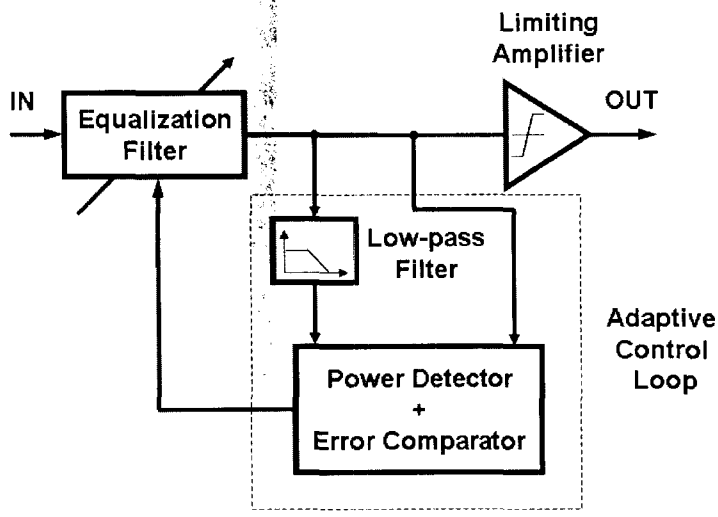


Figure 3.21: Block diagram of the passive equalizer with new adaptive loop.

Table 3.8: Summary of the performance of equalizer components.

Passive Equalization Filter: • Max. Attenuation: 20 dB • Tuning Range: -20 ~ -12 dB • Power consumption: ~0 mW	**Old Power Detector:** • Power consumption: 0.96 mW
Output Stage: • Pre-driver gain: 10 dB • -3-dB Bandwidth: 24 GHz • Pre-driver power consumption: 9.7 mW • Total power consumption: 41 mW	**Old Error Amplifier:** • DC Gain: 60 dB • -3-dB Bandwidth: 10 kHz • Phase Margin: 80° • Power consumption: 0.58 mW
Low-Pass Filter: • DC Gain: 6 V/V • -3-dB Bandwidth: 120 MHz • Power consumption: 1.2 mW	**New Power Detector and Error Amp:** • Power consumption: 0.42 mW

Chapter 4 Results and Discussion

To validate the operation of the equalizer, a signal source which is capable to generate 20-Gb/s random bit sequence and a channel model which can provide reasonable approximation of a real transmission channel are necessary. They will be discussed first. Various simulation results are shown to demonstrate the proper behaviors of the adaptive passive equalizer under different test conditions. Both eye-diagrams and S-parameters are used to evaluate the performance.

4.1 Data Generation and Channel Modeling

4.1.1 Data Generation

The input data have to be random in nature to ensure the function of the adaptation servo loop. Generating truly random bits is very difficult, and the most widely used replacement is so called pseudo-random bit sequence (PRBS). Usually, PRBS can be produced by a linear feedback shift register (LFSR). The details of the LFSR are out of the range of this thesis, but they can be found in many references such as [24]. The block diagram of a LFSR being able to generate a 2^{23}-1 PRBS is shown in Figure 4.1, and the according primitive polynomial is given in Equation (4-1).

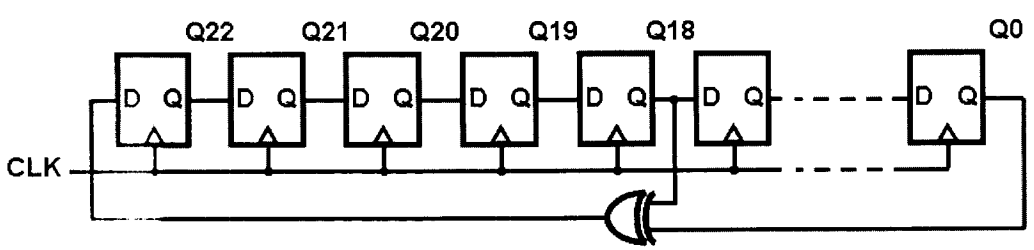


Figure 4.1: Block diagram of a LFSR generating 2^{23}-1 PRBS.

$$F(X) = X^{23} + X^{18} + 1 \tag{4-1}$$

Even with such a simple structure, it is difficult to create a real-time PRBS at the data rate suitable for this project. Instead, Matlab® is used to obtain PRBS data, and they are imported into circuit simulator for transistor-level simulation. A Matlab® program has been designed and is given in Appendix B. This program takes UI, rising and falling time, and voltage levels as inputs, and outputs a 2^{23}-1 PRBS.

4.1.2 Channel Modeling

Two kinds of channel model were used in this project. The first one (Channel-I) models the loss behavior of a CAT-5 cable. The frequency-dependent loss of a CAT-5 cable can be described by the following equation [25]:

$$\alpha(f) = 1.967\sqrt{f} + 0.023f + \frac{0.05}{\sqrt{f}} \quad (dB/100m) \tag{4-2}$$

Based on Equation (4-2), curve-fitting method was used, and two systems were built using Simulink®, whose transfer functions are given by

$$H_1(s) = \frac{2.63\times10^{-30}s^3 + 1.50\times10^{-19}s^2 + 1.95\times10^{-9}s + 1}{4.13\times10^{-87}s^8 + 8.28\times10^{-75}s^7 + 5.52\times10^{-63}s^6 + 1.57\times10^{-51}s^5 \ldots} \tag{4-3}$$
$$\frac{}{+ 2.04\times10^{-40}s^4 + 1.22\times10^{-29}s^3 + 3.07\times10^{-19}s^2 + 2.17\times10^{-9}s + 1}$$

$$H_2(s) = \frac{6.33\times10^{-20}s^2 + 1.63\times10^{-9}s + 1}{1.31\times10^{-86}s^8 + 2.00\times10^{-74}s^7 + 1.08\times10^{-62}s^6 + 2.51\times10^{-51}s^5 \ldots} \tag{4-4}$$
$$\frac{}{+ 2.80\times10^{-40}s^4 + 1.49\times10^{-29}s^3 + 3.38\times10^{-19}s^2 + 2.14\times10^{-9}s + 1}$$

$H_1(s)$ and $H_2(s)$ approximate the loss of a 2-m and 5-m CAT-5 cables (Channel-I-2m and Channel-I-5m), respectively. They are compared with the system described by Equation (4-2) in Figure 4.2. Note that the phase information has been discarded completely. However, we should emphasize that our equalizer is a gain equalizer, so phase dispersion won't be considered. The outputs from the Simulink® were taken into the circuit simulator (Spectre®) and sent to the equalizer directly.

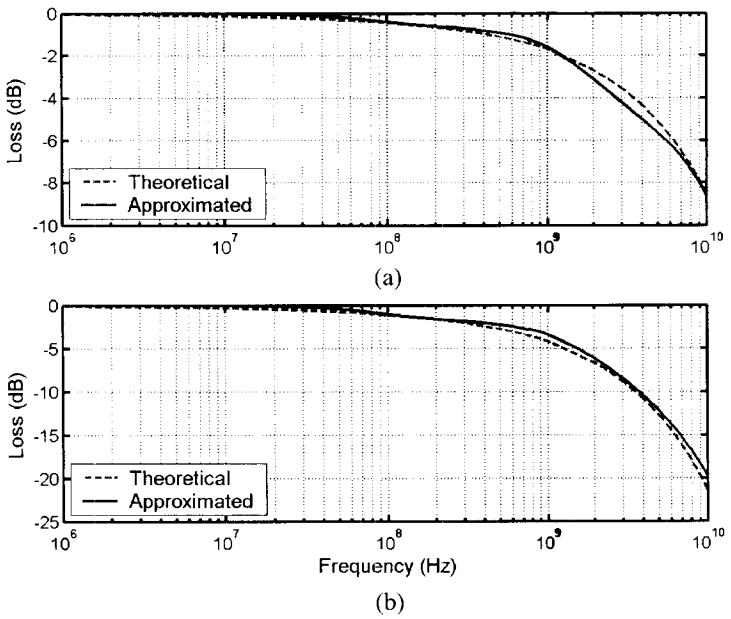


Figure 4.2: Comparison of simulated and calculated CAT-5 cable loss: (a) 2-m CAT-5 cable, and (b) 5-m CAT-5 cable.

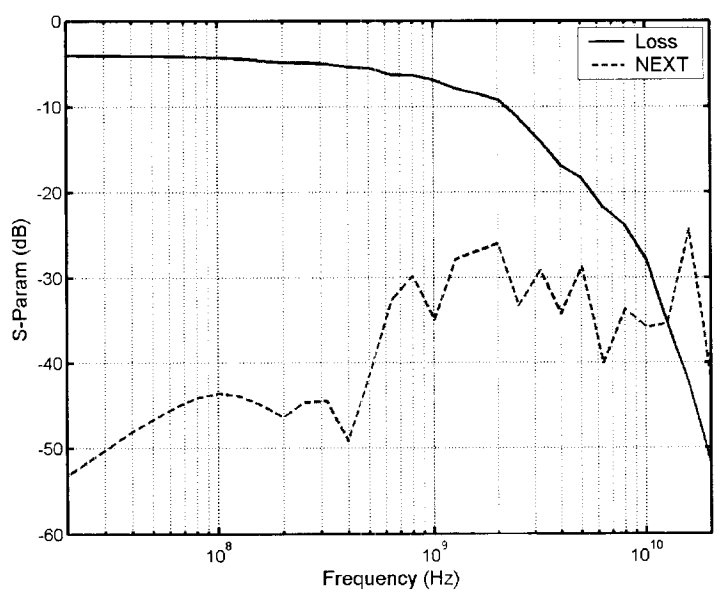
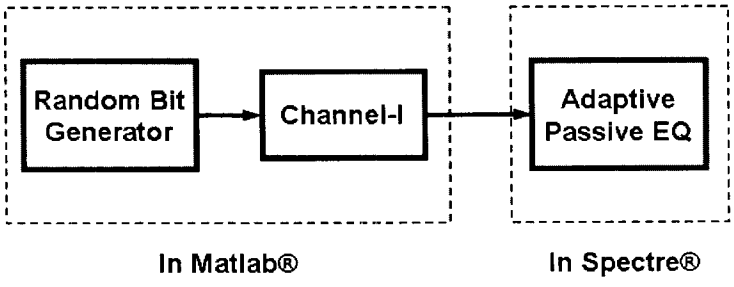


Figure 4.3: Measurement results of Channel-II.

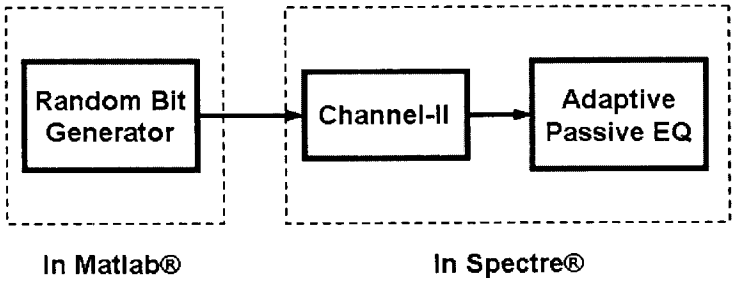
The second model (Channel-II) is based on the measurement results provided by a company. It is a chip-to-chip link channel including traces, vias, and connectors. The measured S-parameters are shown in Figure 4.3. An element from "analogLib" library

in Cadence® was used to model this channel. The PRBS signal (from Matlab) is feed into this "channel" which is connected to the passive equalizer.

The block diagrams of the simulation test benches for the passive equalizer are shown in Figure 4.4.



(a)



(b)

Figure 4.4: Simulation test bench for the equalizer: (a) Channel-I, and (b) Channel-II.

4.2 Simulation Results

The simulated S-parameters of the complete adaptive equalizer (i.e., the passive equalization filter, the output stage, and the adaptive control servo are all connected together) with V_{ctrl} (the control voltage of the passive equalization filter) equal to 0.2V are shown in Figure 4.5. The output stage compensates the attenuation due to the passive filter. The residue attenuation is due to the fact that the output stage is not a linear amplifier (as discussed in Chapter 3, we are not designing output stage with 20-dB gain.), while the S-parameter is the small signal quantity. The S11 is still good even though the existence of the extra ringing due to the output stage and the adaptive servo loop.

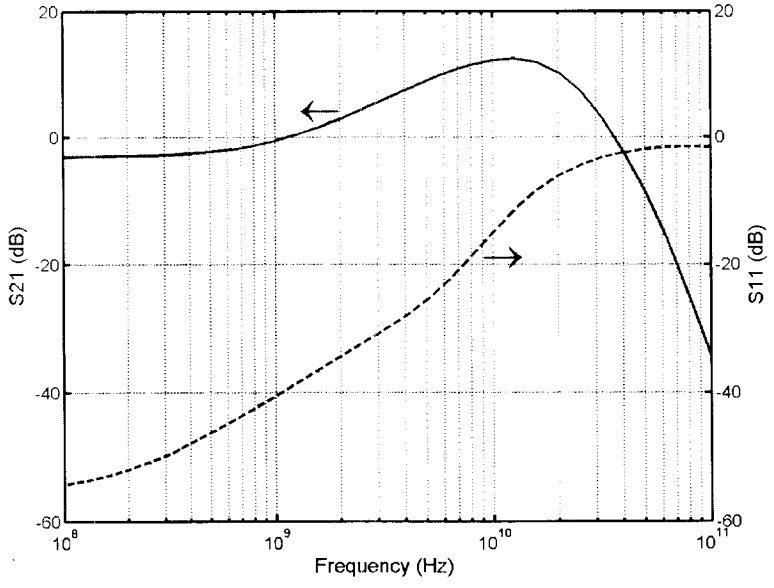
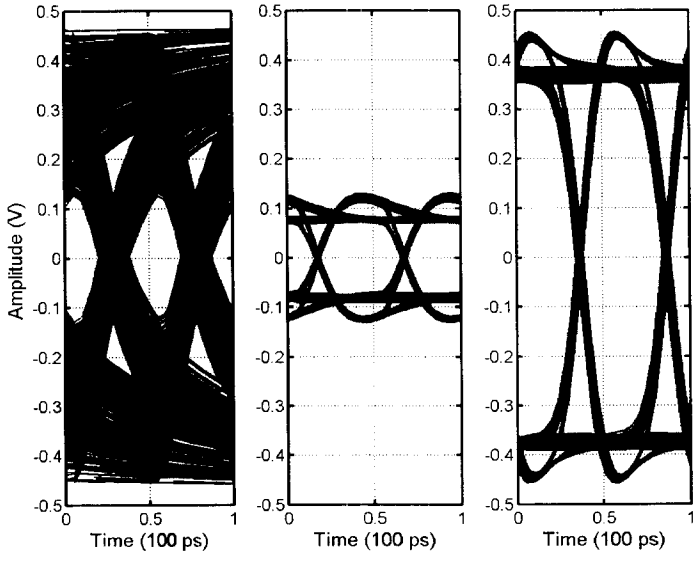


Figure 4.5: Simulated S-Parameters of the equalizer.

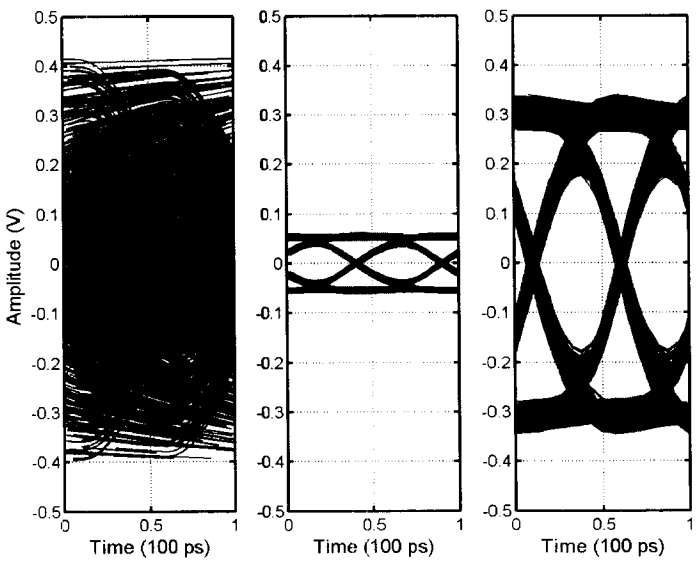


(a) Output of the channel, (b) Output of the passive filter, (c) Final output

Figure 4.6: Eye-diagrams of the input and output signals for Channel-I 2-m CAT-5

The input and output data eye-diagrams for Channel-I-2m are shown in Figure 4.6. It can be seen that the equalizer increases the size of the eye opening. For the worse channel 5-m CAT-5 cable, simulation results are shown in Figure 4.7. The channel loss is so heavy that the

eyes are completely closed at the output of the channel. Still, the equalizer produces well defined eyes. To illustrate the behavior of the adaptation servo loop in these two different cases, Figure 4.8 is shown. Clearly, the control voltage continuously evolves to different values to optimize the equalization amount in both cases.



(a) Output of the channel, (b) Output of the passive filter, (c) Final output

Figure 4.7: Eye-diagrams of the input and output signals for Channel-I 5-m CAT-5 cable.

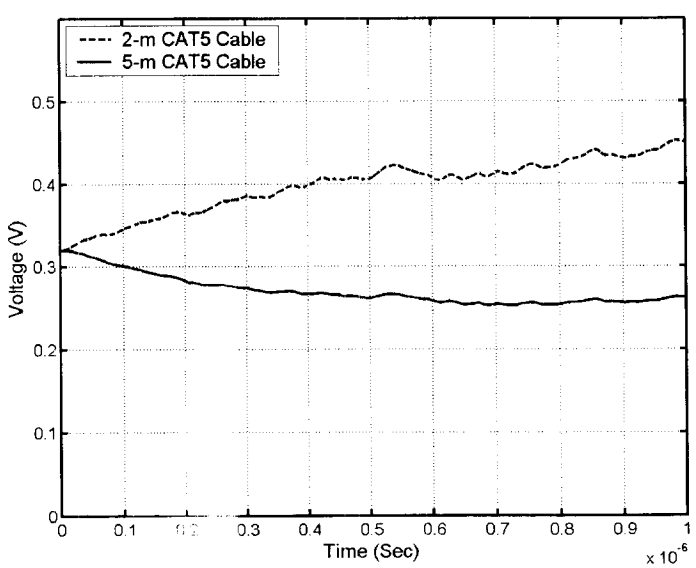
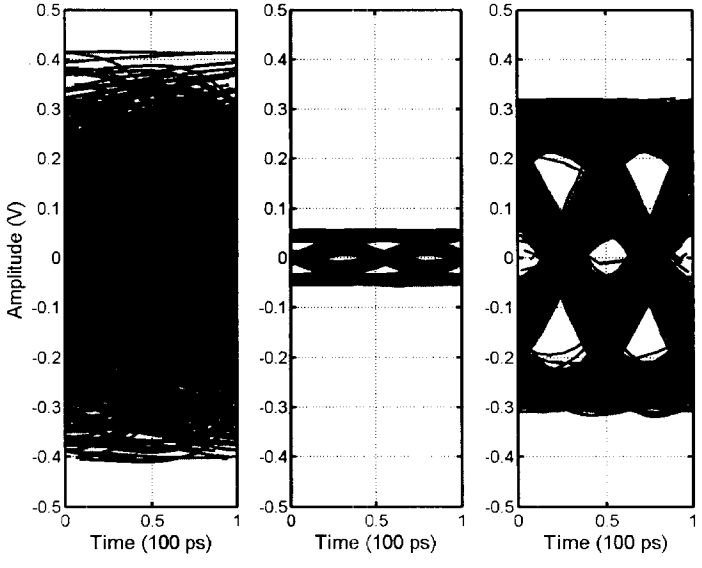


Figure 4.8: Adaptation process of the control voltage for Channel-I.

To test the performance of the equalizer for Channel-II, initially a 20 Gb/s 2^{23}-1 PRBS was used. However, the eye opening is not really good, as shown in Figure 4.9. However, if the frequency response of the Channel-II was examined carefully, it can be seen that the channel loss is indeed about 26 dB at 10 GHz (Figure 4.3), which exceeds our design expectation.



(a) (b) (c)

Figure 4.9: Eye-diagrams of the input and output signals for Channel-II with 20-Gb/s 2^{23}-1 PRBS input: (a) equalizer input, (b) passive filter output, and (c) equalizer output.

To see the effectiveness of the equalizer and to find the maximum data rate for this channel, the overall frequency response of the channel and the equalizer was inspected, which is shown in Figure 4.10. The magnitude response is flat till about 5 GHz, which implies the maximum data rate which the equalizer can support might be 10 Gb/s. This was confirmed by the simulation results shown in Figure 4.11. The output eye is clearly opened for 10-Gb/s 2^{23}-1 PRBS input data.

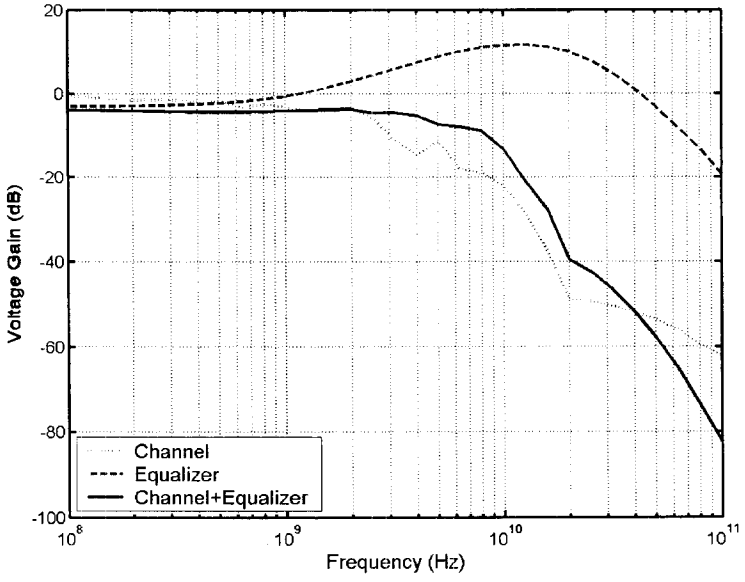
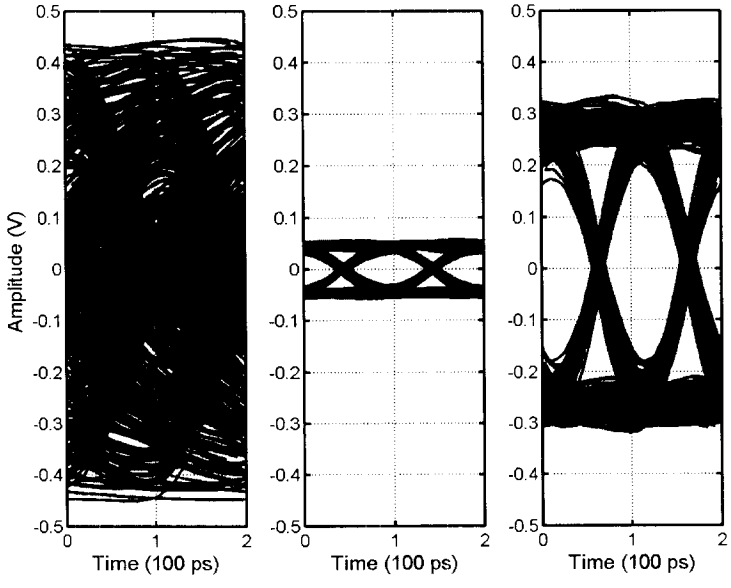


Figure 4.10: Frequency response of the Channel-II, the equalizer and the overall system.



(a) (b) (c)

Figure 4.11: Eye-diagrams of the input and output signals for Channel-II with 10-Gb/s 2^{23}-1 PRBS: (a) equalizer input, (b) passive filter output, and (c) equalizer output.

...ible problem associated with the linear equalization is the noise enhancement due to the ...pass characteristics of the equalization filter [*]. A noise analysis was performed to

[*] SNR is affected by both ISI and noise [26]. For applications where ISI is much more ... noise, the improvement of SNR due to reduction of ISI will overcome the degradation ...e to increasing of noise. Here, we just want to demonstrate that the noise enhancement

study this effect. A 1-kΩ resistor (~4nV/sqrt(Hz)) was placed at the input to represent the thermal noise source. The integrated RMS noise voltage at the output of the passive equalization filter is shown in Figure 4.12. As we can see, within 20-GHz bandwidth, the integrated RMS noise voltage is about 0.15 mV. From Figure 4.7, in the worst case, the vertical eye opening at the output of the passive equalization filter is higher than 80 mV. This translates to a SNR larger than 48 dB. According to Equation (4-5) [18],

$$BER \le 2Q\left(\frac{V_{sig,pp}}{\sqrt{2}\sigma_n}\right) = erfc\left(\frac{V_{sig,pp}}{2\sigma_n}\right) = erfc(SNR) \tag{4-5}$$

where BER is the bit error rate of binary data, $V_{sig,pp}$ is the peak-to-peak signal swing, which is equal to the eye opening, σ_n is the RMS noise voltage, and SNR is the signal-to-noise ratio, the BER will be almost 0, as indicated in Figure 4.13. However, in reality, the thermal noise at the input will be larger than the equivalent of a 1-kΩ resistor, and there are many other noise sources (for example, interference, input offset of the following amplifier, timing noise (jitter) etc.), so the BER performance will be worse. Here, the purpose is to demonstrate that the noise enhancement will not become a concern.

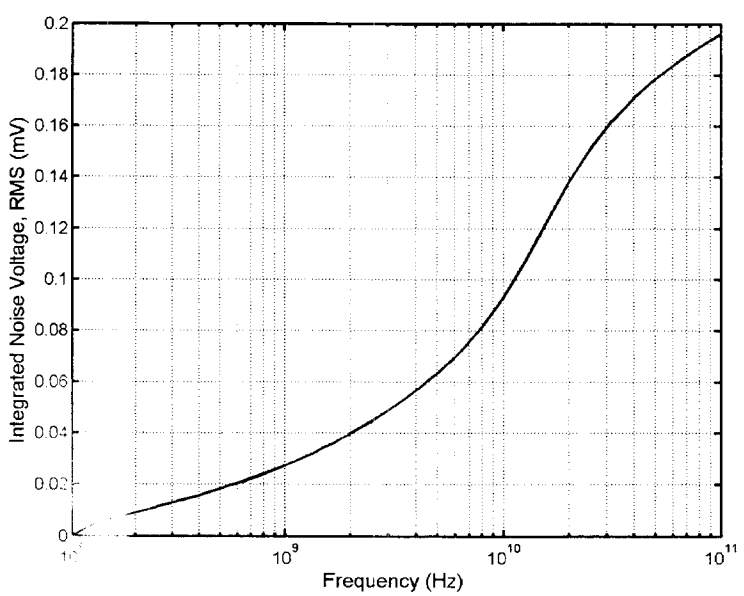


Figure 4. Output RMS noise voltage of the passive equalization filter.

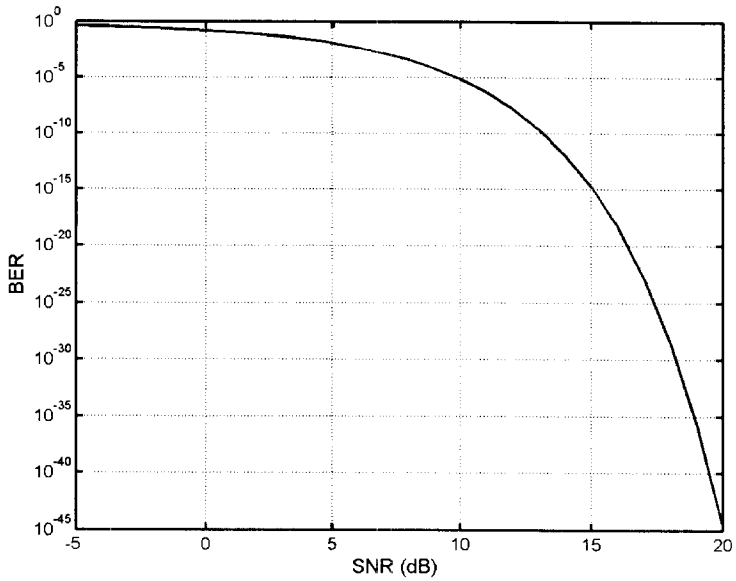


Figure 4.13: BER vs. SNR for binary data.

4.3 Measurement Results

A prototype tunable passive equalization filter was fabricated in a 0.13-μm, 1P8M BiCMOS process. The chip micrograph is shown in Figure 4.14. The active area is about 555 μm × 160 μm.

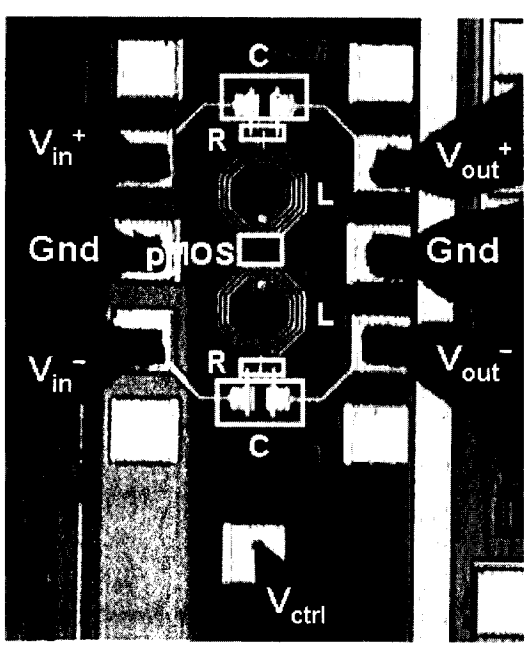


Figure 4.14: Chip micrograph of the tunable passive equalization filter.

The component values of the fabricated tunable passive equalization filter are given in Table 4.1. Note that L and C values are larger than those shown in Figure 3.1. The original purpose for doing this is that the design shown in Figure 3.1 gives a -3 dB loss at 10 GHz, and the peaking frequency is actually higher than 10 GHz, so by increasing L and C (according to Equation (2-3) and (2-5), this means a lower -3-dB frequency.), the loss at 10 GHz is close to 0 dB and the peaking frequency moves close to 10 GHz (see the simulation results shown in Figure 4.17). However, the larger size L and C increases the parasitics, which degrade the frequency response (see the measurement results shown in Figure 4.17 and 4.18).

Table 4.1: Design parameters of the fabricated tunable passive filter.

Device	Value	Device	Value
R	40.1 Ω	L	2.36 nH
pMOS	145 μm / 0.12 μm	C	1.0 pF

The 4-port S-parameters were measured using Vector Network Analyzer (VNA). The measurement setup is shown in Figure 4.15, where DUT is device under test.

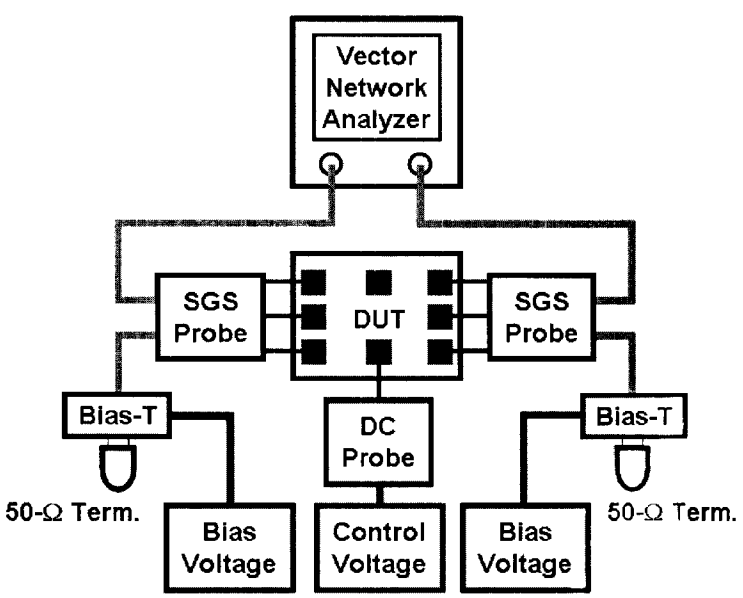
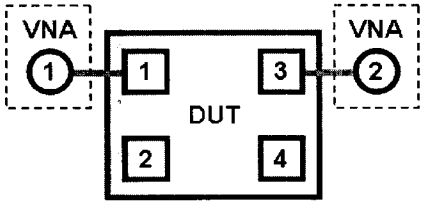
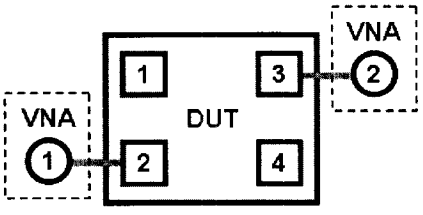


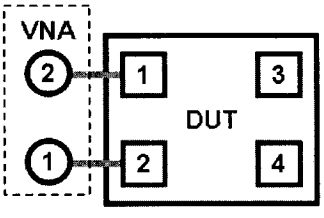
Figure 4.15: Measurement setup for S-parameters of the passive Equalization filter.



(a) Measure S_{11} and S_{13},



(b) Measure S_{14},



(c) Measure S_{12}.

Figure 4.16: Three connections between VNA and DUT to obtain the 4-port S-parameters from 2-port S-parameter measurement.

Due to the lack of a 4-port probe station, several 2-port S-parameter measurements have to be performed to obtain all of the 4-port S-parameters. By recognizing the circuit of the passive equalization filter (Figure 3.1) is highly symmetric, it is easy to derive that only 4 independent S-parameters are necessary to characterize the frequency response of the circuit: S_{11}, S_{12}, S_{13}, and S_{14}, and the 4-port S-parameters $[S_{ij}]$ can be written as,

$$[S_{ij}] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{11} & S_{14} & S_{13} \\ S_{13} & S_{14} & S_{11} & S_{12} \\ S_{14} & S_{13} & S_{12} & S_{11} \end{bmatrix} \tag{4-6}$$

As a consequence, three 2-port S-parameter measurements are enough to determine $[S_{ij}]$. The according configurations of the connection between the VNA and the DUT for these measurements are shown in Figure 4.16(a), (b), and (c), respectively, where numbers in the circles indicate 2 ports of VNA, and numbers in the square indicate 4 ports of the circuit.

Open, short and through calibrations were performed for each configuration before measuring. Because of the difficulty of a one-time calibration over a wide frequency range from 50 MHz ~ 40 GHz, the calibration and subsequently the measurement were done separately for two frequency ranges: 50 MHz ~ 250 MHz and 200 MHz ~ 40 GHz. The results were jointed together to form one set of 4-port S-parameters.

The measured 4-port S-parameters were converted into mixed-mode S-parameters using the following equation,

$$[S_{mm,ij}] = [M_{ij}] \times [S_{ij}] \times [M_{ij}]^{-1} \tag{4-7}$$

where $[S_{mm,ij}]$ is the mixed-mode S-parameters, in which $S_{dd,ij}$ is the differential-mode-input-to-differential-mode-output S-parameters, $S_{dc,ij}$ is the differential-mode-input-to-common-mode-output S-parameters, $S_{cd,ij}$ is the common-mode-input-to-differential-mode-output S-parameters, $S_{cc,ij}$ is the common-mode-input-to-common-mode-output S-parameters,

$$[S_{mm,ij}] = \begin{bmatrix} S_{dd,11} & S_{dd,12} & S_{dc,11} & S_{dc,12} \\ S_{dd,21} & S_{dd,22} & S_{dc,21} & S_{dc,22} \\ S_{cd,11} & S_{cd,12} & S_{cc,11} & S_{cc,12} \\ S_{cd,21} & S_{cd,22} & S_{cc,21} & S_{cc,22} \end{bmatrix} \tag{4-8}$$

and $[M_{ij}]$ is the conversion matrix.

$$[M_{ij}] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{4-9}$$

The measurement results of differential-mode S_{21} and S_{11} for different control voltages are shown in Figure 4.17 and Figure 4.18, respectively. As a comparison, the simulation results are also shown in the same figure accordingly.

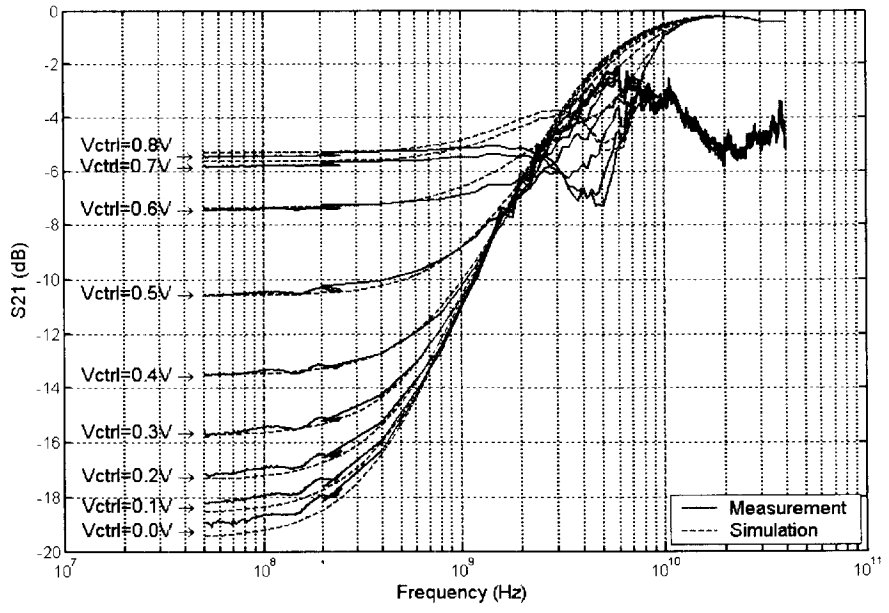


Figure 4.17: Comparison of the measured and the simulated S_{21} of the passive equalization filter.

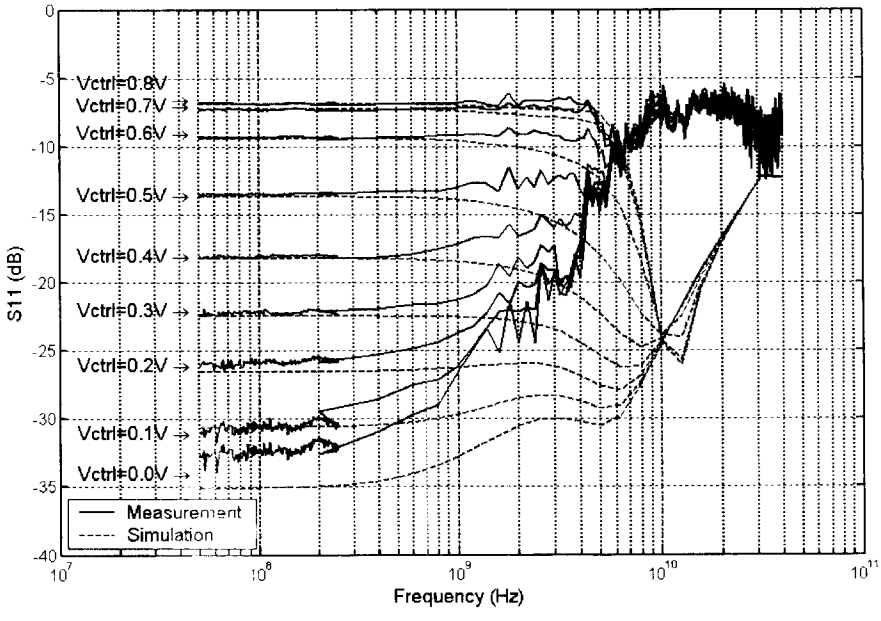


Figure 4.18: Comparison of the measured and the simulated S_{11} of the passive equalization filter.

At low frequencies, the measured data have a good match with the simulated data. The correct tuning behavior is also easily observed. However, the measured S_{21} starts to roll off, and the measured S_{11} starts to become worse at lower frequency compared with the simulated S_{21} and S_{11}. Although the calibration and the measurement could bring some error, the insufficient amount of parasitics modeled by the device models might have a larger contribution to these differences. To confirm this conclusion, the effects of the parasitic capacitors at various nodes in the circuit shown in Figure 3.1 were studied. It was found that the parasitic capacitance at the node where two Rs and the inductor are connected together plays an important role. As shown in Figure 4.19 and Figure 4.20, after a 400-fF capacitor was inserted at that node, the simulation results now match to the measurement results much better for both S_{21} and S_{11}.

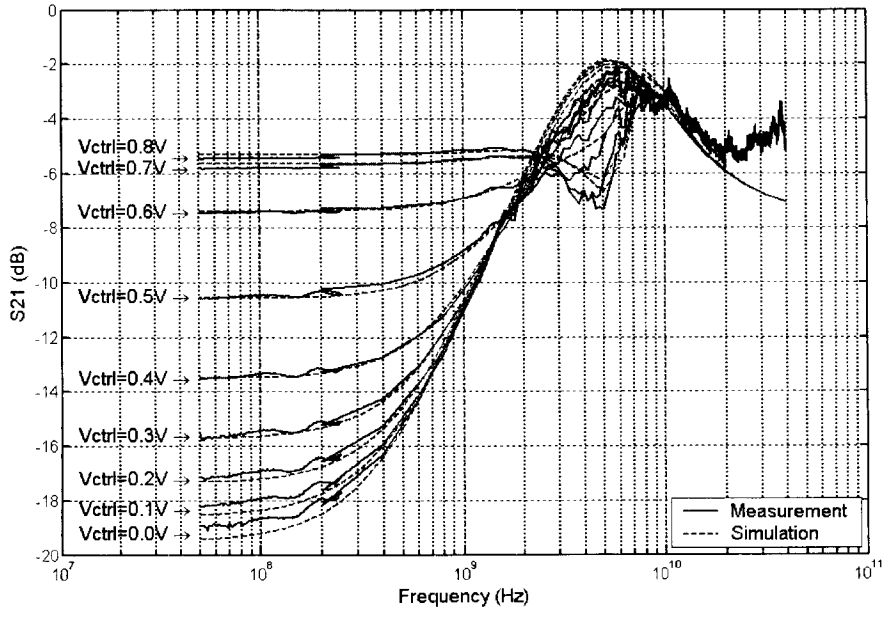


Figure 4.19: Comparison of the measured and the simulated S_{21} after considering the extra parasitic capacitance.

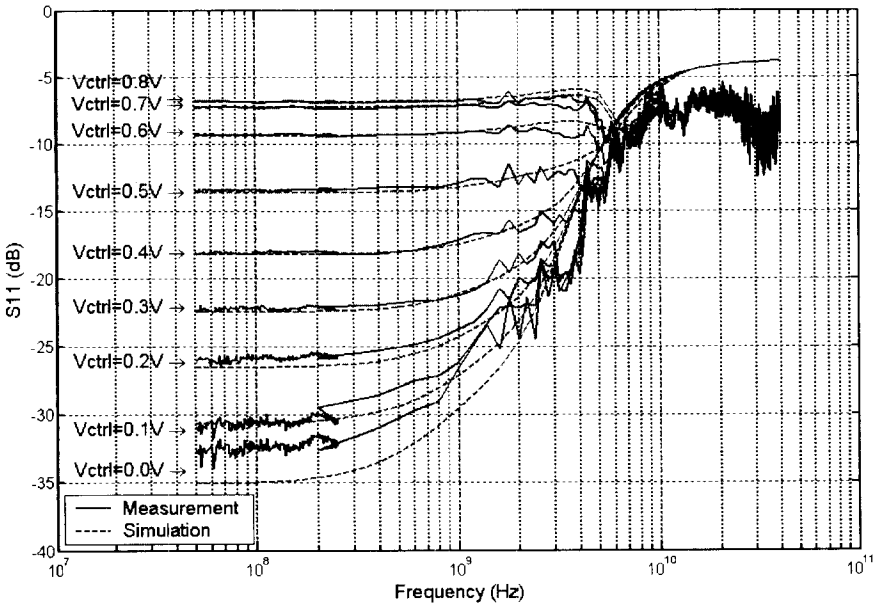


Figure 4.20: Comparison of the measured and the simulated S_{11} after considering the extra parasitic capacitance.

Since a signal generator capable to produce 20-Gb/s PRBS data was not available at the time when the measurement was done, the time-domain characterization of the performance of the tunable passive equalization filter, i.e., the eye-diagram, was not captured. However, the measured S-parameters were imported into Spectre®, and transient simulation was done to verify the performance of the fabricated passive equalization filter. An "n4port" element was used to model the filter, and Channel-II was used. The simulated eye-diagrams of 10-Gb/s 10^{23}-1 PRBS data at the channel output and the passive equalization filter (V_{ctrl} equal to 0.2V) output are shown in Figure 4.21. As can be seen, the equalization filter output has a clearly opened eye.

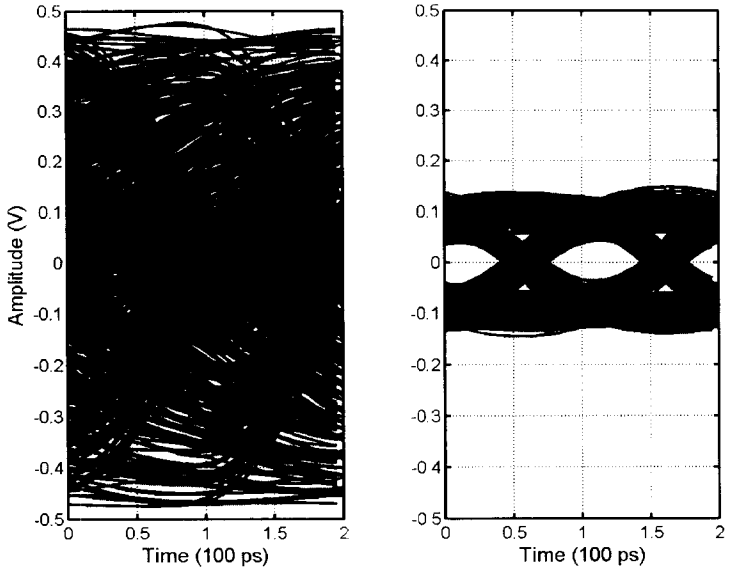


Figure 4.21: Eye-diagrams of a 10-Gb/s 2^{23}-1 PRBS signal at (a) channel output, and (b) passive filter output for Channel-II.

4.4 Summary

In this chapter, PRBS data generation and channel modeling are first discussed due to their importance for system-level simulation. A 2^{23}-1 PRBS was used as input to the channel. Two kinds of channel models were used. Channel-I approximates the loss behavior of CAT-5 cable and the model was obtained by curve-fitting. Channel-II model was built on the measurement results of a short-range chip-to-chip PCB link. In either case, the designed adaptive passive equalizer is able to open the completely closed eye at the input of the equalizer. In addition, by monitoring the transient response of the control voltage of the passive equalization filter for two different CAT-5 cables, the functionality of the adaptation servo loop was verified. Part of the chip – the tunable passive equalization filter – was fabricated in a 0.13-μm 1P8M BiCMOS process, and the measurement results demonstrated the correct tuning behavior. Finally, the performance of the low-power continuous-time adaptive passive equalizer is summarized in Table 4.1, along with a comparison with other

recently published results. Our design consumes a much lower power while achieving a much higher data rate.

Table 4.2: Performance comparison of recently published high-speed equalizers.

Data Rate (Gb/s)	Power (mW)	Max. Compensation (dB)	Technology	Ref
3.2	80	21	0.18-μm CMOS	[8]
5	10	9	0.13-μm CMOS	[10]
10	155	25	0.18-μm BiCMOS	[6]
20	**11.5**	**20**	**0.13-μm BiCMOS**	**This work**

Chapter 5 Conclusion

5.1 Conclusion

In summary, a low-power, 20-Gb/s continuous-time adaptive passive equalizer has been designed. The tunable passive equalization filter demonstrates significant improvements in both operating speed and power consumption when compared with other recently published designs. A modified continuous-time servo loop controls the frequency response of the equalizer and finds the optimal channel equalization. Simulations confirm the proper operation of the equalizer for different channel conditions. Moreover, the equalizer can occupy a relatively small area because its *LC* components have small values and require only moderate-Q values. Implemented in a 0.13-μm, 1P8M BiCMOS technology, all of the active circuits except for the output stage have been designed using only MOS devices. The entire design could be easily ported to a CMOS technology in which the high-speed devices are available. The total power consumption is 11.5 mW for the core and 52.4 mW including the output driver.

5.2 Directions of the Future Work

As this thesis is finishing, only the passive equalization filter was fabricated in silicon. A tape-out of the complete chip is needed and the measurement results must be obtained to fully validate the design.

For the future research works, there are several aspects which may require further investigation. Since the passive filter itself is a linear system, so theoretically it can be placed anywhere in the system. One possibility is that there might be a system configuration such that the power-performance trade-off is optimized. The other possibility is that several cascaded stages can be used to achieve more compensation (than 20 dB in this project). A block diagram illustrates this idea is shown in Figure 5.1. However, the amplifier between each stage must be linear. If any non-linear amplifier, such as limiting amplifier or multi-

based sense amplifier, presents, it will produce wrong output based on the under-compensated input, any further compensation becomes worthless.

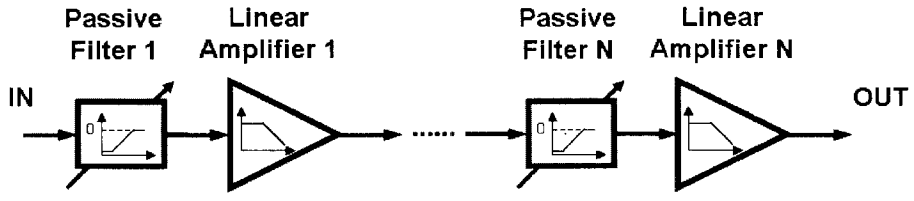


Figure 5.1: Cascading several passive equalization filters.

The limited tuning range, as described in Chapter 2, may also need to be solved, possibly by investigating other passive filter structures [17]. In addition, they may provide more flexibility to control the frequency responses. For the current filter, only the low frequency attenuation is easily changed, and the frequency location where the gain peaking occurs is relatively constant (Figure 3.3). Another way to solve this problem is to use variable capacitors and inductors. Most modern processes provide varactors, but it is difficult to make the tunable inductors. One possible solution is to use a switch-controlled inductor array, and the same concept can be applied to capacitors to improve the tuning range, as illustrated in Figure 5-2.

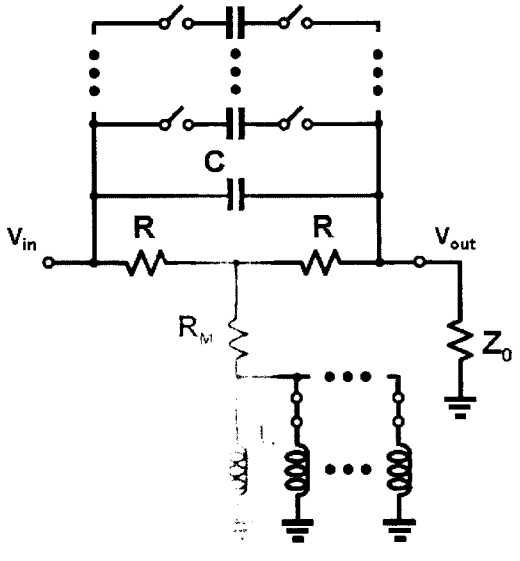


Figure 5.2: Passive filter with inductor array and capacitor array.

The other concern about passive RLC filter is the large area consumed due to the large size of the on-chip inductor. Although the required inductance for the passive filter is small (and it will become smaller as the data-rate goes up.), techniques that will lead to an area-efficient implementation of on-chip inductors should be explored. Some useful research results have been presented, for example, in [26].

Appendices

Appendix 1 Derivation of Equation (2-1) and (2-2)

A two-port network with loading is shown in Figure A.1. The interaction between input port and output port can be described by *Y*-parameters, which can be expressed in the form of – *Y* matrix ($[Y_{ij}]$), defined by

$$\begin{aligned} i_1 &= y_{11}v_1 + y_{12}v_2 \\ i_2 &= y_{21}v_1 + y_{22}v_2 \end{aligned} \tag{A-1}$$

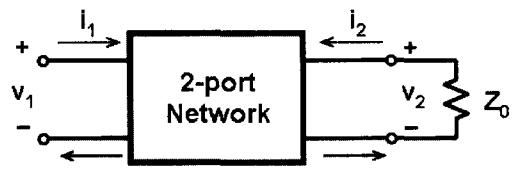


Figure A.1: A two-port network with impedance loading.

In addition, output voltage and current are related by Equation (A-2),

$$v_2 = -Z_L \cdot i_2 \tag{A-2}$$

where Z_L is the load impedance. From Equation (A-1) and (A-2), the voltage gain and the input impedance of the two-port network can be calculated,

$$\begin{aligned} A_v &= \frac{v_2}{v_1} = \frac{-Z_L \cdot y_{21}}{Z_L \cdot y_{22} + 1} \\ Z_{in} &= \frac{1 + Z_L \cdot y_{22}}{y_{11} + Z_L \cdot \Delta y} \end{aligned} \tag{A-3}$$

where Δy is the determinant of the *Y* matrix:

$$\Delta y = y_{11}y_{22} - y_{12}y_{21} \tag{A-4}$$

The passive equalization filter shown in Figure 2.2(a) can be decomposed into two parallel two-port networks, as shown in Figure A.2, and the *Y* matrixes representing these two two-port networks are

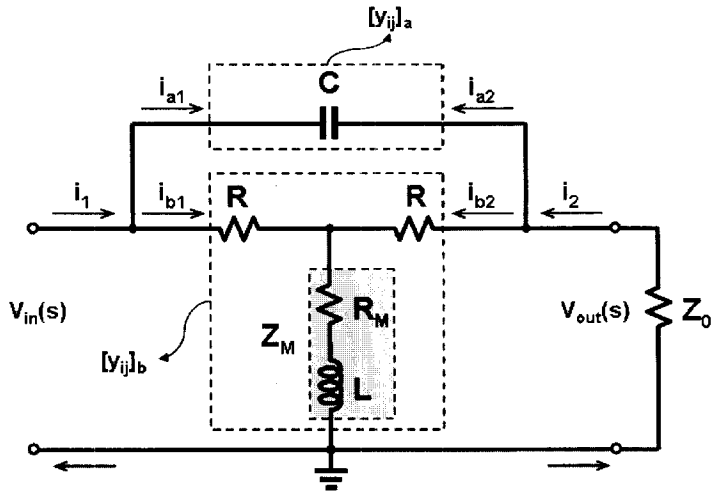


Figure A.2: The passive filter consists of two parallel two-port networks.

$$[y_{ij}]_a = \begin{bmatrix} sC & -sC \\ -sC & sC \end{bmatrix} \tag{A-5}$$

$$[y_{ij}]_b = \begin{bmatrix} \dfrac{1}{R+(R//Z_M)} & -\dfrac{(R//Z_M)}{R+(R//Z_M)}\cdot\dfrac{1}{R} \\ -\dfrac{(R//Z_M)}{R+(R//Z_M)}\cdot\dfrac{1}{R} & \dfrac{1}{R+(R//Z_M)} \end{bmatrix} \tag{A-6}$$

respectively, where $Z_M = sL + R_M$. The Y matrix of the original circuit is

$$[y_{ij}] = [y_{ij}]_a + [y_{ij}]_b \tag{A-7}$$

where,

$$y_{11} = y_{22} = sC + \frac{1}{R+(R//Z_M)}, \tag{A-8}$$

$$y_{12} = y_{21} = -sC - \frac{(R//Z_M)}{R+(R//Z_M)}\cdot\frac{1}{R}$$

Based on Equation (A-3) and (A-8), after a little bit work of rearranging and simplifying the equations, we can get,

$$A_v(s)=\frac{v_{out}(s)}{v_{in}(s)}$$
$$=\frac{s^2+s\left(\frac{R_M}{L}+\frac{1}{2RC}+\frac{R}{2L}\right)+\frac{1}{LC}\cdot\frac{R_M}{2R}}{s^2+s\left[\frac{R_M}{L}+\left(1+2\frac{R}{Z_0}\right)\frac{1}{2RC}+\frac{R}{2L}\right]+\frac{1}{LC}\cdot\left(\frac{R_M}{2R}+\frac{R_M}{Z_0}+\frac{R}{2Z_0}+\frac{1}{2}\right)} \quad \text{(A-9)}$$

$$Z_{in}(s)=\frac{v_{in}(s)}{i_{in}(s)}$$
$$=Z_0\frac{s^2+s\left[\frac{R_M}{L}+\left(1+2\frac{R}{Z_0}\right)\frac{1}{2RC}+\frac{R}{2L}\right]+\frac{1}{LC}\cdot\left(\frac{R_M}{2R}+\frac{R_M}{Z_0}+\frac{R}{2Z_0}+\frac{1}{2}\right)}{s^2+s\left(\frac{R_M}{L}+\frac{Z_0}{L}+\frac{1}{2RC}+\frac{R}{2L}\right)+\frac{1}{LC}\cdot\left(\frac{R_M}{2R}+\frac{Z_0}{2R}+\frac{1}{2}\right)} \quad \text{(A-10)}$$

which are Equation (2-1) and (2-2), respectively.

To get the component values listed in Equation (2-3), first, notice that to have constant input impedance Z_0 over all frequencies, the numerator and the denominator in Equation (A-10) have to be equal to each other regardless to values of s. Consequently, the coefficients of two polynomials have to be same, which leads to,

$$s^0\ coeff. \Rightarrow 2R_M + R = \frac{Z_0^2}{R}, \quad \text{(A-11)}$$
$$s^1\ coeff. \Rightarrow \frac{L}{C} = Z_0^2$$

Secondly, the DC gain is $\alpha = -20\cdot log_{10}(K)$, so from Equation (A-9),

$$\frac{\frac{R_M}{2R}}{\frac{R_M}{2R}+\frac{R_M}{Z_0}+\frac{R}{2Z_0}+\frac{1}{2}}=\frac{1}{K} \quad \text{(A-12)}$$

ng Equation (A-11) and (A-12), values of R and R_M can be solved. Finally, combining n Equation (A-11), using the fact that the attenuation becomes half of DC value will luce values of L and C as given in Equation (2-3).

A Matlab® program ("eqf_param_cal.m") was written to calculate the R, R_M, L and C ues given by Equation (2-3), and the code is given here.

Figure A.3: Source code of "eqf_param_cal.m".

```
%==========================================================================
% This program will calculate the device parameters for a
% single-ended high-pass passive equalization filter.
%
%                    C
%           ----------||----------
%          |                      |
%          |    R1          R1    |
%     o-------xxxxx--------xxxxx-------o
%                    |
%                    |
%                    x
%                    x R2
%                    x
%                    |
%                    |
%                    c
%                    c L
%                    c
%                    |
%                    |
%                    __
%                    \/
% Input:
% (1) DC attenuation amount in dB;
% (2) Transmission date rate in Gb/s;
%
% Output: values of R1, R2, L, and C.
%
% Ruifeng Sun, 2005
%

clc;clear;

% DC attenuation
atten_dc = input('DC attenuation of passive filter (dB): ');

% Data rate
data_rate = input('Data transmission rate (Gb/s): ');
UI = 1/data_rate/1e9; % sec
fc = 1/(2*UI);        % Hz

% Transmission line characteristic impedance
Z0 = 50;              % Ohm

K = 10^(atten_dc/20);

% Frequency at which the attenuation becomes half of DC value
f0 = fc/sqrt(K-2/K);
w0 = 2*pi*f0;

% Component values
R1 = (K-1)/(K+1)*Z0;                    % Ohm
R2 = 2*K/(K^2-1)*Z0;                    % Ohm
L  = sqrt(K)/(K-1)*Z0/w0*1e9;     % nH
C  = sqrt(K)/(K-1)/Z0/w0*1e15;    % fF

sprintf('R1 =   %.2f Ohm\n', R1)
sprintf('R2 =   %.2f Ohm\n', R2)
sprintf('L  =   %.3f nH\n', L)
sprintf('C  =   %.1f fF\n', C)

% Save data into a file
filename = 'eqf_param_cal.out';
fid = fopen(filename,'a');
fprintf(fid,'Data generated on %s\n\n',date);
fprintf(fid,'DC attenuation =   %.1f    dB\n',atten_dc);
```

```
fprintf(fid,'Data rate      =   %.1f    Gb/s\n\n',data_rate);
fprintf(fid,'R1             =   %.2f    Ohm\n', R1);
fprintf(fid,'R2             =   %.2f    Ohm\n', R2);
fprintf(fid,'L              =   %.3f    nH\n', L);
fprintf(fid,'C              =   %.1f    fF\n', C);
fprintf(fid,'\n====================\n\n');
fclose(fid);
sprintf('Data have been saved into %s\n',filename)
=========================================================================
```

Appendix 2 Matlab Programs to Generate 2^23-1 PRBS

Matlab program "prbs23_data_gen.m" produces 2^23-1 PRBS (according to Equation (4-1)) differential signals whose amplitude, UI, and rise/fall time (which are same) are set by users. It calls two sub-routines: "prbs23_gen.m" and "bit2pwl.m". The former creates a 0/1 bit sequence without electrical and timing information, and the latter converts this bit sequence into a time-domain waveform.

Figure A.4: Source code of "prbs23_data_gen.m".

```
%=========================================================================
% Create fully differential PRBS 2^23-1 electrical signals.
%
% The output data are saved into 2 files: "prbs23_data_p_*" and
% "prbs23_data_n_*", where "*" indicate different frequencies.
% They can be used in the SPCIE simulation as the differential
% input signals (e.g. in a PWL voltage source).
%
% User should give the number of bits he/she wants. Keep in mind,
% if you ask 100 bits, the total run time of this bit sequence
% will be 100UI.
%
% Input:
% (1) Singl-ended signal amplitude;
% (2) Common-mode voltage;
% (3) Bit time(UI);
% (4) Risefall time;
%
% Output: PRBS 2^23-1 differential signals with above characteristics
%
% -- Ruifeng Sun, 2005

clear;clc;

% Electrical signal amplitude -- signle-end
% vamp = 250e-3; % V
vamp = input('Single-ended signal amplitude = ? ');
% Differential signal common-mode voltage
% vcm = 2.25;    % V
vcm = input('Differential signals common-mode voltage = ? ');
% Bit time (UI)
% ui = 50e-12;  % sec => 20 Gb/s
ui = input('Bit-time (UI) = ? ');
bit_rate = 1/ui/1e9; % Gb/s
% Risefall time
% trf = 5e-12; % sec => knee frequency = 100GHz
trf = input('Rising and falling time = ? ');

% Digital 0/1 bit sequence
data_len = input('How many bits do you want?');
digital_data = prbs23_gen(data_len);
% -1/1 sequence
digital_data_p = sign(digital_data-0.5);
% complementary
digital_data_n = -digital_data_p;

% Convert ditial bit sequence into electrical signals
% timing information
electrical_data_p = bit2pwl(vcm+digital_data_p*vamp,ui,trf);
electrical_data_n = bit2pwl(vcm+digital_data_n*vamp,ui,trf);

% Save data into files
```

```
save_file = input('Save data to files?(yes=1/no=0)');
if save_file
    %save prbs23_data_p electrical_data_p -ASCII;
    %save prbs23_data_n electrical_data_n -ASCII;
    if bit_rate == floor(bit_rate)
        filename1                                                    =
strcat('prbs23_data_p','_',num2str(bit_rate),'G');
        save(filename1, 'electrical_data_p', '-ASCII');
        filename2                                                    =
strcat('prbs23_data_n','_',num2str(bit_rate),'G');
        save(filename2, 'electrical_data_n', '-ASCII');
    else
        filename1                                                    =
strcat('prbs23_data_p','_',num2str(floor(bit_rate)),'p',num2str(round
(10*(bit_rate-floor(bit_rate)))),'G');
        save(filename1, 'electrical_data_p', '-ASCII');
        filename2                                                    =
strcat('prbs23_data_n','_',num2str(floor(bit_rate)),'p',num2str(round
(10*(bit_rate-floor(bit_rate)))),'G');
        save(filename2, 'electrical_data_n', '-ASCII');
    end
end
sprintf('Save output data into %s and %s\n',filename1, filename2)

% Plot
% figure(1);
%
plot(electrical_data_p(:,1),electrical_data_p(:,2),'r',electrical_dat
a_n(:,1),electrical_data_n(:,2),'b')
% grid;
% xlabel('Time (s)');
% ylabel('Voltage (V)');
================================================================================
```

Figure A.5: Source code of "prbs23_gen.m".

```
================================================================================
function [out]=prbs23_gen(in)
% Generate a 2^23-1 PRBS with length given by "in".
% Polynomial: [23 18]
%
% -- Ruifeng Sun, 2005

out = [];
seed = [zeros(1,22) 1];
prbs23_len = in;

matrix_a = eye(23);
matrix_b = matrix_a(1:size(matrix_a)-1,:);
matrix_c = zeros(1,23);
prbs23_xform_matrix = [matrix_c;matrix_b];

for i=1:prbs23_len
    bit_array_cur = seed;
    out=[out seed(1)];
    seed = seed*prbs23_xform_matrix;
    seed(23) = xor(bit_array_cur(1),bit_array_c...(9));
end
================================================  ==================
```

Figure A.6: Source code of "bit2pwl.m".

```
================================================================================
function [out] = bit2pwl(in1, in2, in3)
% out = bit2pwl(in1,in2,in3)
%   |              |   |   |
%   |              |   |    -------------------------------
%   |              |    --------------------              |
%   |              |                       |              |
% output PWL    input bit sequence       bit time(UI)  risefall time
%
% Convert a bit sequence without timing information into a
% piece-wise-like(PWL) sequence with timing information.
%
% e.g. [1 0 0 1] --> [0 40e-12 50e-12 90e-12 100e-12 140e-12 150e-12;
%                     1 1      0      0      0       0       1]
% in above example, a bit sequence [1 0 0 1] is converted into a PWL
% waveform with one bit time(UI) = 50ps, rise and fall time = 10ps.
%
% -- Ruifeng Sun, 2005.

bit_len = length(in1);

bit_matrix = [in1;in1];
bit_sequence = reshape(bit_matrix,1,2*bit_len);

UI = in2;
trf = in3;
time_matrix = [UI*(0:bit_len-1);(UI-trf)+UI*(0:bit_len-1)];
time_sequence = reshape(time_matrix,1,2*bit_len);

out = [time_sequence;bit_sequence]';
================================================================================
```

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