Flicker Noise in CMOS Transistors from Subthreshold to Strong Inversion at Various Temperatures

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Abstract-Flicker noise is the dominant noise source in silicon MOSFET'S. Even though considerable amount of work has been done in investigating the noise mechanism, controversy still exists as to the noise origin. In this paper, a systematic study of flicker noise in CMOS transistors from twelve different fabricators is reported under various bias conditions corresponding to the gate voltage changing from subthreshold to strong inversion, and the drain voltage changing from linear to saturation regions of operation. The measurement temperature was varied from room temperature down to 5 K. Experimental results consistently suggest that 1/f noise in n-channel devices is dominated by carrier-density fluctuation while in p-channel devices the noise is mainly due to mobility fluctuation.

I. Introduction

LOW-FREQUENCY noise in silicon MOSFET'S is dominated by flicker noise. It is commonly known as *1/f* noise since the noise spectral density is inversely proportional to frequency. Because MOSFET'S have large flicker noise, it sets a lower limit to the level of signal that can be processed by VLSI devices and circuits. Much effort has been spent in understanding and reducing the noise for better performance in VLSI circuits. In the last four decades, a considerable number of papers have been published dealing with *1/f* noise in MOSFET'S [1]-[30].

In the carrier-density fluctuation model, the noise is explained by the fluctuation of the channel free carriers due to the random capture and emission by the interface traps known as slow states. Using this model, the input referred noise will be independent of the gate bias voltage and the magnitude of the noise spectra is proportional to the density of the interface trap density. The slope η of the $1/f^{\eta}$ noise spectra is usually chosen to be 1 if the trap density is assumed to be uniform in the gate oxide. However, experimental values for the slope of the noise spectra are rarely exactly 1, but varies from 0.7 to 1.2. This might be due to a number of reasons, such as generation-recombination noise (caused by traps with only a definite relaxation time constant) [14] and nonuniform distribution of traps. Surya and Hsiang [15] found that the slope decreased with increasing gate bias magnitude in p-channel MOSFET'S, and explained this observation by a modified carrier density fluctuation model where the spatial distribution of traps in the oxide was not uniform, and hence the noise was a function of gate bias voltage. Celik–Butler and Hsiang [13] found that the slope increased with gate bias in n-channel transistors, and a similar trap-induced carrier density fluctuation model was derived. Exponential expressions for the trap concentrations were used in these models. The argument is that trap density across the band gap varies with energy, and even though there is no intrinsic spatial nonuniformity of the traps, band bending with increasing gate voltage will "pull down" the traps, effectively causing a nonuniform distribution.

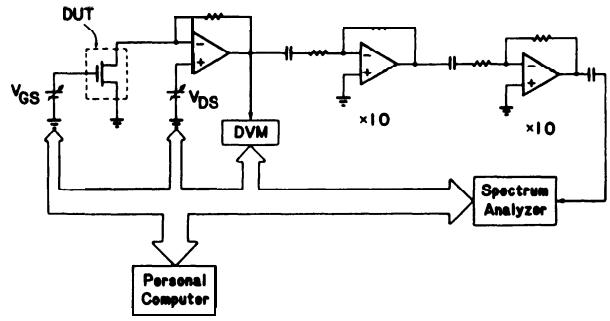

Fig. 1. Schematic of the low frequency noise measurement setup, consisting of three stages of operational amplifiers.

On the other hand, the mobility fluctuation model suggests a gate voltage dependence in the input-referred noise. The model is based on the empirical experimental observation of the noise in homogeneous samples, and the input referred noise shows strong gate bias dependence.

Research has focused on resolving these two theories, but has not provided any satisfactory resolution. Inconsistent experimental results were reported for both the n- and p-channel devices. One of the problem could be due to the different fabrication conditions of the samples used. Park and van der Ziel [17] have tried to discriminate between the models by comparing the drain flicker noise current spectral density. It was suggested that $S_I(f)/I^2$ reaches its maximum at saturation when carrier density fluctuation noise dominates; whereas $S_I(f)/I^2$ reaches a maximum well before saturation if mobility fluctuation noise dominates. As a result, it was concluded that carrier density fluctuation predominated in diffusion FET's while mobility fluctuation predominated ion-implanted devices. However, it was later suggested that

Manuscript received September 20, 1993; revised July 1, 1994. The review of this paper was arranged by Editor-in-Chief R. P. Jindal. This work was supported in part by the California MICRO Program, and in part by Hughes Aircraft Company.

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IEEE Log Number 9405330.

TABLE I
PROCESS CHARACTERISTICS AND NOISE PARAMETERS FOR THE n – AND p-CHANNEL DEVICES FROM THE DIFFERENT FABRICATORS

Fabricator	Well Type	Gate Oxide Thickness	n-MOS			p-MOS	
			Size (μm^2)	slope η	$N_T(E_F)kT$	Size (μm^2)	α_H
Fab A	P	485 Å	12×3	0.82	2.2×10^{15}	12×3	2.6×10^{-6}
Fab B	P	440 Å	12×3	0.81	2.4×10^{15}	12×3	1.9×10^{-6}
Fab C	N	300 Å	20×3	0.80	1.8×10^{15}	20×3	2.9×10^{-6}
Fab D	P	500 Å	20×3	0.80	8.4×10^{15}	20×3	4.0×10^{-7}
Fab E	P	620 Å	100×6	0.84	7.6×10^{15}	100×6	1.7×10^{-5}
Fab F	P	145 Å	75×1.5	1.00	4.9×10^{15}	75×1.5	1.6×10^{-6}
Fab G	P	600 Å	5×5	0.72	2.4×10^{16}	100×5	6.3×10^{-6}
Fab H	N	775 Å	80×6	0.70	1.0×10^{15}	80×6	2.1×10^{-6}
Fab I	P	300 Å	100×10	0.80	3.0×10^{15}	100×10	8.9×10^{-6}
Fab J	P	700 Å	10×20	0.71	2.5×10^{15}	10×20	7.1×10^{-6}
Fab K	N	400 Å	200×2	0.86	2.1×10^{15}	200×2	3.9×10^{-6}
Fab L	N	110 Å	10×1	0.95	8.1×10^{15}	10×1	8.1×10^{-5}

ion-implanted channels act as buried channels and this could cause $S_I(f)/I^2$ to reach a maximum before saturation sets in [18]. As a result, the original question still remained unsolved. Other researchers have combined the earner-density fluctuation model and the mobility fluctuation model, in an uncorrelated [19] or correlated [8] manner, to explain the frequently observed dependence of the noise magnitude and slope of the spectra with gate bias voltages. Recently, noise behavior in ultrathin gate oxide devices of nominal dimensions in the range of 1 μm channel lengths and widths were studied. Results [2], [3] indicated that the single trap found in these devices can cause induced-mobility fluctuation noise to be dominant in the n-channel transistors, while carrier density fluctuation type of noise can be dominant in the p-channel devices. However, the devices that we used in this study were larger area devices with relatively thicker gate oxides and the mechanisms of the single trap might not be applicable.

Moreover, most work was performed on MOSFET'S operating in the linear region. Comparatively little has been done on noise in saturation region of operation. Most expressions for the low frequency noise were obtained for small drain voltages where inversion charge density is assumed to be constant over the entire channel.

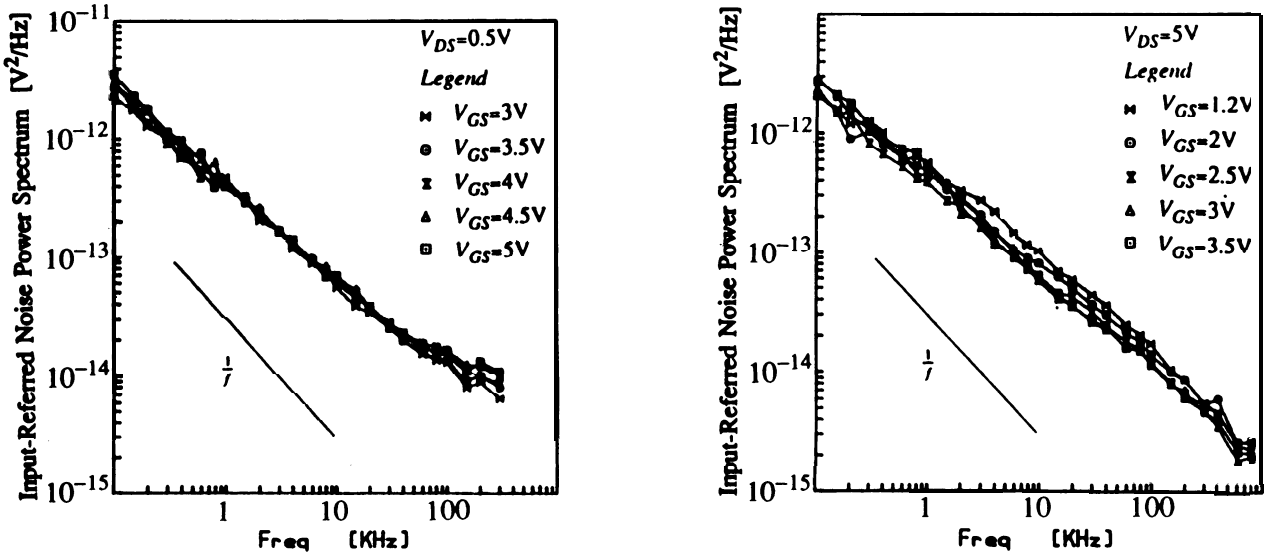
Operation of MOSFET'S at low temperatures has been proposed as a method of improving device performance. At lower temperatures, electron and hole nobilities, leakage current and interconnection conductivity improve substantially. It is also generally believed that noise will decrease as the temperature decreases. However, only limited amount of work has been carried out in characterizing low temperature noise behavior in silicon MOSFET'S.

Similarly, very little is known on noise in the subthreshold region of operation. Duh and van der Ziel [28] suggested that it is advantageous to operate MOS transistors under weak inversion to obtain better noise performance than under strong inversion. However, Aoki, Katto, and Yamada [29] showed input-referred noise that increased near threshold and in weak inversion, and argued that it was due to decrease in mobility caused by surface potential roughness.

In this paper, we report the study of flicker noise behavior of transistors obtained from twelve different highly reputable CMOS fabricators from the United States, Japan, and Europe. Bias conditions were varied from linear to saturation regions of operations, as well as in the subthreshold regime. Measurements were also done from room temperature down to 5 K. Results obtained from different fabricators suggested that input referred noise from the n-channel transistors very often is independent of gate bias and can be modeled as carrier density fluctuation while that of p-channel devices is dependent of gate bias and can be modeled as mobility fluctuation.

II. EXPERIMENTAL SETUP

Fig. 1 shows the schematic of the low frequency noise measurement system. The amplifier is made from commercially available IC op amps and has an equivalent noise voltage of the order of 3 $nV/\sqrt{Hz}$ and an equivalent noise current of 2 $pA/\sqrt{Hz}$. It consists of three stages. The first one is a transresistance amplifier (current to voltage converter) while the second and third stages are 10× voltage amplifiers. Linear Technology low noise operational-amplifier LT1007 is used to construct the first stage amplifier whose noise has to be very low as it will be amplified by the latter stages. The second and third stage amplifiers are TL0740N 's. The circuit is laid out on a glass epoxy board and the whole amplifier is contained in a metal shielding box. Extreme care was taken in laying out various components so as to minimize pick up and noise. Coaxial cables have to be used for some critical connections. The DC bias used are GP-IB controlled power supplies. Variable biasing are available at the gate, drain and substrate terminals of the device. The drain of the device under test (DUT) is biased through the differential input of the first stage amplifier. With this experimental arrangement, the gate and drain voltages can be independently controlled and varied; and the drain current through the DUT can be characterized by the voltage drop across the feedback resistor using the remote-controlled Fluke 8860A digital multimeter. Thus, the small-signal transconductance used in the calculation of input-referred noise is measured, rather than calculated, for each bias point. As was pointed out by van der Ziel, Park, and Liu [30], this is crucial in minimizing error in the noise



(a) (b)

Fig. 2. Input referred noise spectra for the 12 x 3 μm^2 n-channel transistor from Fabricator A, (a) in the linear, and (b) in the saturation region of operation.

data. The amplified noise power is measured by the hp 3561A spectrum analyzer.

A shielded Signatone general purpose probe station is used to characterize devices at room temperature. Isolated probe holders are used to avoid parasitic. For low temperature studies down to 5 K, an adapted Janis Research 68-pin liquid helium cryostat is used. The temperature controller was calibrated to within +2 K for the range of 20 to 295 K. Samples had to be wire-bonded onto 68 pin flatpacks, and the liquid helium cooled the copper cold finger which in turn cooled the flatpack by thermal conduction. The temperature was continuously controlled from 5 K to 300 K by a Lakeshore DRC 82C temperature controller.

The first three column of Table I summarizes the characteristics of the test samples. Devices used in the study are CMOS transistors from both n- and p-well processes, with gate oxide thickness varying from 110 to 775 A. Device channel lengths varied from 1.0 to 10 µm. Fabricator *G* samples were obtained from Europe while fabricator *J* samples were from Japan. Transistors from Fabricator *L* are short channel devices with LDD's on both the drain and source. p-channel devices obtained from fabricator *C* and *J* are surface channel devices and did not receive any boron threshold adjust implants.

III. Room Temperature Flicker Noise Behavior

Fig. 2 shows the input referred noise spectra for the 12 x 3 μm^2 n-channel transistor from Fabricator ***A.*** As can be seen, the gate-referred noise spectra in these n-channel transistors vary very little (less than a factor of two) as the gate bias voltage changes, both in the linear and saturation regions of operations. Considering the margin of error which had been estimated to be about 10%, no consistent gate bias dependence parameters can be extracted from the data. This behavior is typical of the n-channel devices from all fabricators, except for the LDD devices from Fabricator *L.* In the Fab *L* short

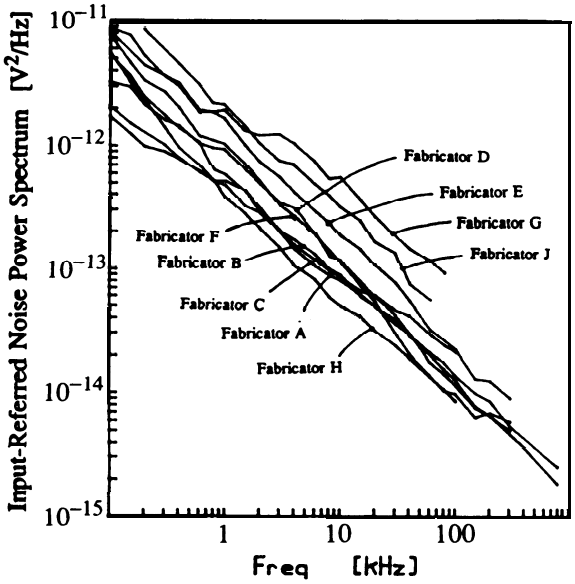


Fig. 3. Comparison of the n-channel input referred noise from various fabricators with respect to Fab. A. Noise spectra are normalized for their different oxide thickness and device dimensions.

channel LDD n-channel devices, strong gate bias dependence was observed. Li and Vandamme [1] explained this gate bias dependent component of the noise by attributing it to the voltage dependent series resistance of the LDD structure at the drain end of the device.

The "independence" from gate bias voltage in the input-referred noise suggests that flicker noise from these n-channel devices is due to carrier-density fluctuation rather than mobility fluctuation and the noise is caused by the slow states. In the carrier-density fluctuation model, the interface trap density is usually assumed to be uniform in space and energy, and that capture and emission processes of the traps follow the Shockley–Read–Hall statistics. Then the spectral density of

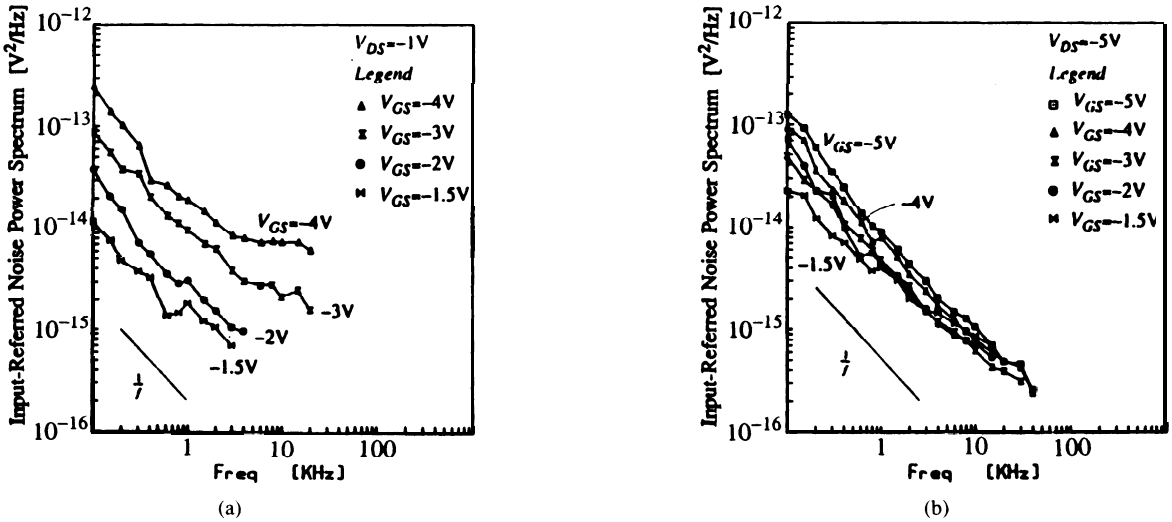


Fig. 4. Input referred noise spectra of a 12 x 3 μm^2 p-channel transistor from Fabricator A, (a) in the linear, and (b) in the saturation region of operation. Strong gate bias dependence is observed_.

the number of carriers trapped can be shown to be

$$S_{\Delta N_t}(f) = \frac{N_T(E_F)kT}{\gamma f^{\eta}} WL \tag{1}$$

where $N_T(E_F)kT$ is the interface state density per unit energy at the Fermi Energy level, and γ is McWhorter's tunneling parameter. Assuming the device is biased in the linear region of operation, it can be shown that the input referred noise can be obtained from (1), such that

$$S_{V_G}(f) = \left(\frac{q}{C_{\text{ox}}}\right)^2 \frac{1}{WLf^{\eta}} \frac{N_T(E_F)}{\gamma}. \tag{2}$$

As can be seen in ***(2),*** the input-referred noise shows no gate bias dependence and is proportional to the interface state density. Fig. 3 shows the comparison of the n-channel input referred noise among various fabricators. The noise spectra are normalized for their different oxide thickness and device dimensions, according to (2). It can be seen that the noise power of all these devices are within a decade of magnitude, suggesting that the oxides in the state-of-the-art fabrication process have fairly consistent and repeatable properties. Using (2), and assuming that McWhorter's tunneling parameter to be $10^8\,\text{cm}^{-1}$, the interface trap density $N_T kT$ at the Fermi energy level can be calculated. The fourth and fifth column of Table I summarizes the noise parameters for the n-channel devices for the different fabricators. As can be seen, $N_T kT$ varies from 2 x 10^{15} to 2 x $10^{16}\,\text{cm}^{-3}$; while the slope η varies from 0.7 to 1.0 among various fabricators.

Low-frequency noise characteristics in the p-channel FET's behave very differently. It very often shows gate--voltage dependence in both the linear and saturation regions of operations. Fig. 4 shows the input referred noise spectra of a 12 x 3 μm^2 p-channel transistor from Fabricator ***A.*** Depending on the bias points, the input noise power in p-channel devices can be 10--100 times less as compared to n-channel transistors of the same dimensions on the same chip. This gate bias dependence is typical of the p-channel devices for all of the fabricators used in the study. To model this gate bias dependent noise, the mobility fluctuation theory can be used. It is based on empirical observation of the noise in homogeneous samples [23], where

$$\frac{S_I}{I^2} = \frac{\alpha_H}{Nf}. \tag{3}$$

In this equation, I is the current through the sample and α_H is the Hooge's parameter and is an experimental fitting parameter. For a MOSFET operating in the linear region of operation, the input-referred noise for mobility fluctuation can be shown to be

$$S_{V_G}(f) = \left(\frac{q}{C_{\text{ox}}}\right) \frac{\alpha_H}{WLf} (V_{\text{GS}} - V_T). \tag{4}$$

As a result, the noise spectra increases with V_{GS}. The last column of Table I summarizes the noise parameter of the p-channel devices for the different fabricators.

This gate bias dependence has been explained by buried channel conduction in ion-implanted devices, where bulk mobility fluctuation noise dominate. However, our experimental data from p-channel devices without ion-implantations show similar gate bias dependence: Fabricator ***C*** p-channel FET's are in the n-well; while Fabricator ***J*** p-channel devices are in the n-substrate. Moreover, input-referred noise on ion-implanted buried channel n-MOS devices show very different behavior.

Fig. 5 shows the normalized noise spectra for both the n-MOS and p-MOS transistors from Fabricators ***A, B, D, F,*** and ***H.*** As can be seen, the p-channel noise amplitude increases with the gate bias and approaches the n-charnel noise magnitude. The normalized noise amplitude and the gate bias dependence seems to be very similar among all five fabricators with different gate oxide thicknesses. As the magnitude of the gate bias voltage increases, the input-referred noise increases and saturates as gate bias is increased to about 10 V. The noise amplitude where the p-channel devices saturates coincides remarkably with the noise amplitude of the same dimension n-channel device on the same chip (the

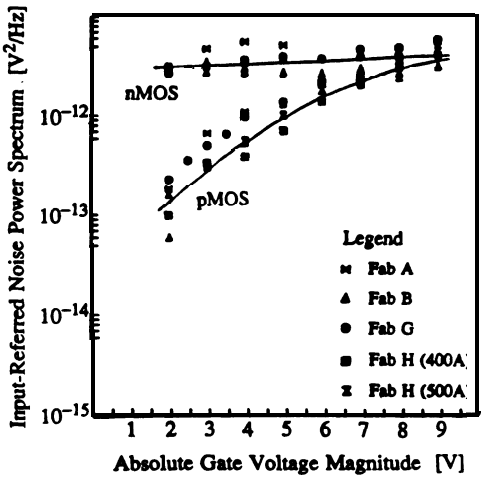


Fig. 5. Normalized spot noise spectra for both the n-MOS and p-MOS transistors from Fabricators .4, *B, D, F,* and *H,* at frequency = 100 Hz.

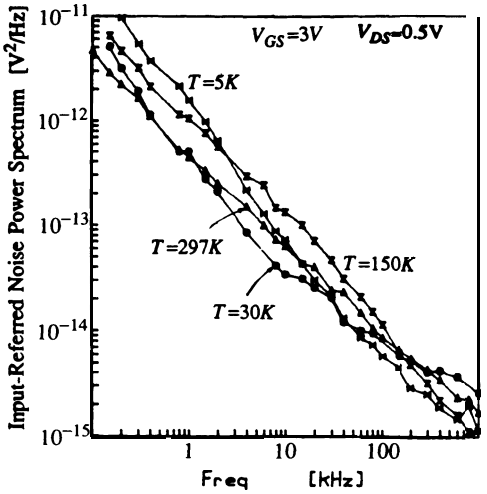


Fig. 6. Noise spectra for the 80 x 6 μm² n-channel transistor from Fabricator H from room temperature down to 5 K

solid lines in the figure). This suggests that p-channel devices generally suffer from mobility fluctuation and carrier density fluctuation phenomenon becomes dominant under high field conditions.

IV. Low Temperature Noise Characteristics

Devices from Fabricator *H* were used in the low temperature studies. The n- and p-channel transistors are 80 **x** 6 μm². When carrying out measurements at temperatures below 30 K, care had to be taken to make sure the device is operating in equilibrium before measurements are carried out. Transient measurements indicate that our n-channel samples have response times of over 5 rein, due to freezeout at low temperatures. Since the transient caused by the delay in the ionization of the dopants is much faster at slightly higher temperatures, the process can be speeded up by biasing up the test sample at higher temperatures, such as 30 K, to reach equilibrium, and then lowered to the testing temperature.

The n-MOS input-referred noise spectra show no bias dependence at all temperatures. For transistors from this fabricator, the noise spectra show an increase in slope at lower frequencies at very low temperatures. This peculiar behavior is found only in devices from this particular fabricator, and is probably due to a generation-recombination noise source at low frequency. Fig. 6 shows the temperature dependence of the noise from room temperature down to 5 K. Contrary to common belief, flicker noise at low temperatures does not decrease in any significant order of magnitude except that there is a significant and consistent shift in the slope of the spectra from $\eta = 1.09$ at 30 K to $\eta = 0.84$ at room temperature. This again gives credence to a tunneling model such as carrier-density fluctuation, which is temperature-independent to the first order.

On the other hand, the p-MOS input-referred noise spectra show gate bias dependence at all temperatures down to 5 K. To compare the p-MOS noise behavior versus temperature, the noise measured at a fixed drain voltage of – 0.5 V and a bias current of 0.2 mA in the p-channel device is plotted at different temperatures in Fig. 7. The noise power decreases **as the** temperature decreases to about 150 K and the slope of

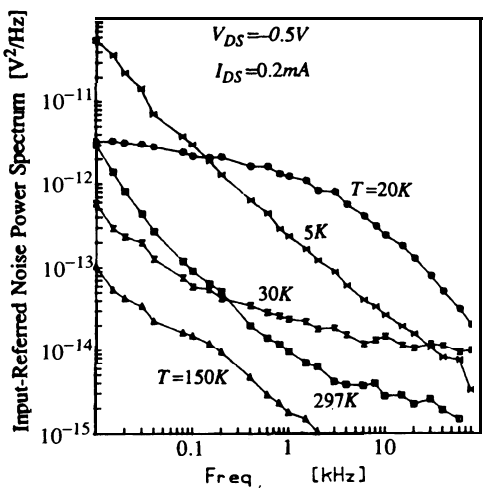


Fig. 7. Noise spectra for the 80 x 6 μm² p-channel transistor from Fabricator H from room temperature down to 5 K, at a fixed drain voltage of –0.5 V and a drain current of 0.2 mA.

the spectrum shows practically no change. However, noise increases when the temperature is lowered beyond 150 K. At 30 K, the slope of the spectrum becomes very small for frequencies larger than 1 kHz. At 20 K, the noise definitely displays a generation-recombination type of behavior. At 5 K, the peak due to the generation-recombination (g-r) noise appears to have moved to much lower frequencies. This dominant trap level that causes the g-r noise can be characterized by an Arrhenius' plot. It is determined from the Arrhenius' plot that the trap level has an activation energy of 0.025 eV above the valence band. This g-r noise level has been determined to be caused by the frozen out boron threshold adjust implant. But the dramatic changes in the *1/f* noise amplitude in the p-channel transistors suggest that flicker noise in p-MOS devices varies with temperature and can be more conveniently modeled as mobility fluctuation rather than carrier density fluctuation.

V. Subthreshold Region Noise Behavior

When the MOSFET gate voltage is below the threshold voltage, the semiconductor surface is in weak inversion. The

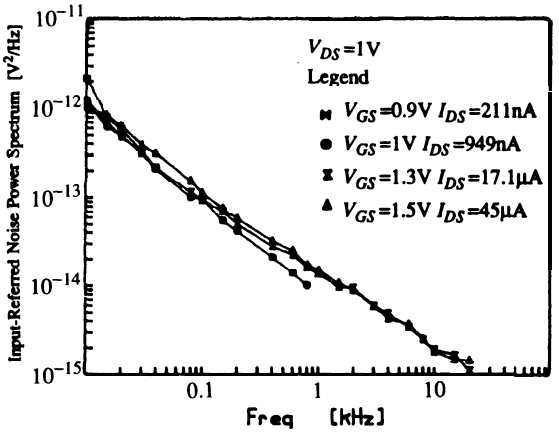


Fig. **8.** Input referred noise of a 100 **x** 10 μm² n-channel MOSFET from Fabricator *I* at room temperature. No gate bias dependence is observed as VG changes from subthreshold to strong inversion.

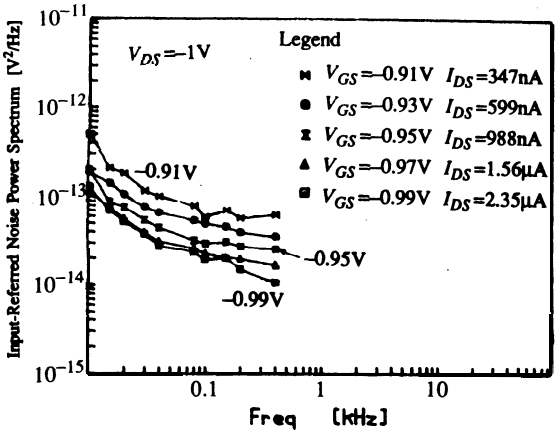


Fig. 9. Input-referred noise of a 100 x 5 μm² n-channel MOSFET from Fabricator *I* at room temperature. Gate bias is varied from subthreshold to strong inversion.

drain current is dominated by diffusion rather than drift. The subthreshold region of operation is particularly important for low voltage, low-power applications, such as in focal plane arrays, where noise directly affects memory errors and logic voltage swings. Devices from Fabricator I were designed for this application, and were used in the subthreshold noise characterization.

Fig. 8 shows the room temperature input referred noise spectrum of a 100 x 10 μm² n-charnel MOSFET device from Fabricator *I* It can be seen that input referred noise in the subthreshold region has the same behavior as that in the strong inversion. No gate bias dependence is observed, even in the weak inversion regime where the free carriers are moving under diffusion.

Subthreshold noise characteristics in p-channel devices behaved very differently from that of the n-channel FET's. Fig. 9 shows the input-referred noise of a Fabricator *I* 100 x 5 μm² p-channel MOSFET at room temperature. Contrary to what has been observed before, the input referred noise decreases in magnitude as the device bias is varied from subthreshold (V_{GS} = 0.91 V; I_{DS} = 347 nA) into strong inversion (V_{GS} = −0.99 V; I_{DS} = 2.35 μA.) This is very different from the noise behavior of the n-channel transistors. This again gives credence to the fact that different noise mechanisms exist in the n-and p-channel devices.

VI. Discussion

An experimental study of flicker noise in CMOS devices, obtained from different fabrication lines, indicates that the noise characteristics of the devices do not depend on the doping type of the CMOS well; and their behavior 'do not vary dramatically among fabricators. In n-channel transistors, the input-referred noise shows no gate bias dependence, when the gate bias is varied from subthreshold to strong inversion and the measurement temperature is changed from room temperature down to 5 K. This suggests that flicker noise in n-channel devices follows carrier density fluctuation. In p-channel devices, strong gate-bias as well as temperature dependence in the input-referred noise is observed. Mobility fluctuation seems to be able to explain the p-charnel noise behavior.

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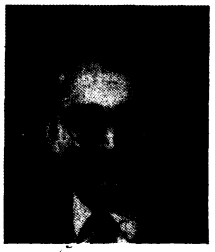

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