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A standard CMOS high-voltage transmitter for ultrasound medical imaging applications

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A high-voltage (HV) transmitter for ultrasound medical imaging applications is designed using 0.18-μm CMOS (complementary metal oxide semiconductor) technology. The proposed HV transmitter achieves high integration by employing standard CMOS transistors in a stacked configuration with dynamic gate biasing circuit while successfully driving the capacitive output load with an HV pulse without device breakdown reliability issues. The HV transmitter, which includes the output driver and voltage level-shifters, generates up to 30-Vp-p pulses at 1.25 MHz frequency and occupies 0.035 mm² of layout area.

Keywords: ultrasound; transmitter; high voltage; output driver; level-shifter

1. Introduction

Ultrasound imaging has gained much interest in recent years in the medical community due to its safe characteristic to the human body in comparison to other widely used modalities such as computed tomography (CT), positron emission tomography (PET), magnetic resonance imaging (MRI), and X-ray (Khuri-Yakub & Oralkan, 2011). A typical ultrasound imaging system, as shown in Figure 1, is comprised of a transducer array, a transceiver interface integrated circuit (IC), and signal/image processing blocks. The transducer elements interface with the multi-channel analogue front-end, consisting of high-voltage (HV) pulsers, low-noise preamplifiers and HV protection switches to isolate the HV from the low-voltage (LV) circuits in order to prevent breakdown. On the transmitter side, the HV pulsers are driven by LV trigger pulses generated by the digital signal processor (DSP) with controlled delays for beamforming. On the receiver part, time-to-gain compensation (TGC) amplifiers follow the preamplifiers to control the receiver gain according to the depth of the received echo signal. The anti-aliasing filters follow the TGC amplifiers, with analogue-to-digital converters (ADCs) to digitise the signals and connect to the DSP for further signal processing and ultimately construct an image from the pulse-echo signal information. Most recently, two-dimensional (2D) capacitive micromachined ultrasound transducer (CMUT) arrays with integrated front-end ICs have been developed for three-dimensional (3D) ultrasound volumetric imaging for improved benefits such as higher resolution and signal-to-noise ratio (SNR) (Wygant et al., 2008).

In order to support large-size 2D arrays, a large number of transducer elements are required, which leads to an increase in the number of closely packed interfacing front-

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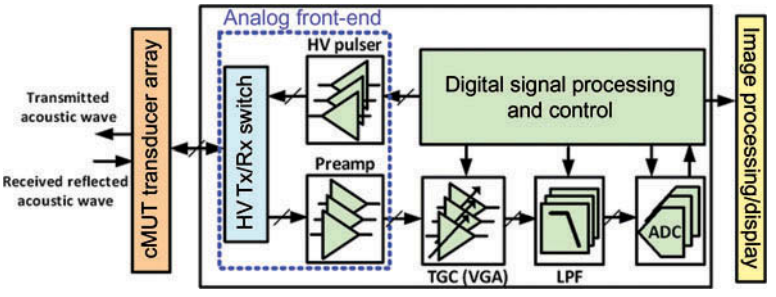

Figure 1. Block diagram of a typical ultrasound imaging system.

end IC cells, posing critical integration issues due to the limited die area available for each cell. One of the main issues is the area-hungry HV transmitter in the interfacing analogue front-end IC as it usually utilises large-size double-diffused lateral MOS (DMOS) transistors (Chebli & Sawan, 2007; Borg & Johansson, 2011; Zhao et al., 2011) in order to generate HV output pulse signals to drive the capacitive micromachined ultrasound transducer (CMUT) to produce large acoustic pressure while maintaining the reliability to prevent possible device junction breakdown.

In this paper, a highly integrated HV transmitter utilising standard CMOS transistors targeted for multi-array ultrasound medical imaging applications is presented. The transmitter adopts the proposed multiple-stacked architecture with dynamic gate biasing circuit in order to generate up to 30-Vp-p pulse signal at 1.25 MHz frequency while driving the capacitive load mimicking the CMUT device. Section 2 briefly addresses the transmitter architecture, while Section 3 describes the circuit design in detail. Section 4 presents the simulation results followed by the conclusions in Section 5.

2. Architecture of HV transmitter

The overall architecture of the HV ultrasound transmitter is shown in Figure 2. The architecture consists of two level-shifters and an HV output driver. The first level-shifter converts the 1.8-Vp-p input trigger signal generated externally from a DSP to a 6-Vp-p pulse signal. Then the 6-Vp-p signal is divided into two different paths. The first routing path contains a second level-shifter and a tapered buffer to convert the signal to swing between 24 and 30 V in order to drive the gate of PMOS transistor of the HV output driver. The second path, on the other hand, goes through inverter-based buffers to drive the gate of NMOS transistor of the output driver. The output driver is followed by the CMUT element where the CMUT is driven with a 30-Vp-p HV pulse so that an ultrasound

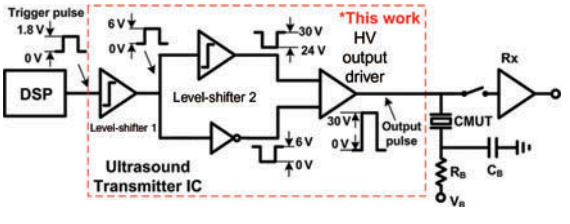

Figure 2. Architecture of HV ultrasound transmitter.

signal with sufficient acoustic pressure is generated for propagation through the acoustic medium. The pulse width, period and the required amount of generated acoustic pressure which relates to the maximum voltage of the output pulse signal are decided in the system level depending on the specific medical imaging application as well as the device characteristics of the following transducer. The other terminal of the CMUT device is connected to a DC bias voltage through a large bias resistor R_B, and a bypass AC capacitor C_B, for biasing the CMUT near the breakdown voltage for high transmit efficiency. The output driver and CMUT interface is also connected to the receiver analogue front-end, which consists of an HV isolation switch and a low-noise preamplifier to amplify the incoming weak ultrasound-to-electrical current converted reflected signal. This work includes the HV transmitter part of the overall ultrasound analogue transceiver front-end.

3. Circuit design

3.1. *Previous HV transmitter*

Figure 3 shows the conventional HV transmitter (Chebli & Sawan, 2007; Zhao et al., 2011), which consists of a level-shifter and an output driver to drive the following transducer with a large voltage swing in order to generate sufficiently high acoustic pressure signal. In order to prevent junction breakdown of the regular MOS transistors during HV operation, DMOS transistors which can sustain a high drain-to-source voltage are used in both the level-shifter and output driver so that reliability in the circuit operation is maintained. The disadvantages of these DMOS transistors are the added process cost, increased layout size and parasitic capacitance. In addition, the device on-resistance of these transistors is larger than regular CMOS transistors and the sizing has to be sufficiently large in order to drive the following CMUT element to an HV at megahertz frequencies. As more ultrasound systems for medical imaging applications require high-density 2D arrays for improved system performance, it is inevitable that the analogue front-end IC provide higher integration to minimise the overall die area and lower the manufacturing cost.

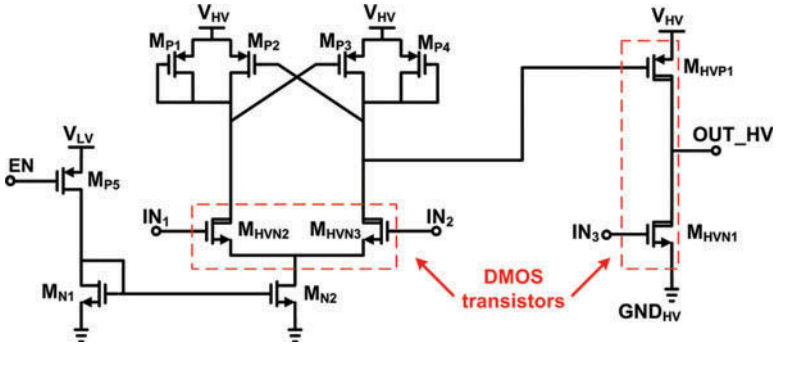

Figure 3. Simplified schematic of the previous HV transmitter.

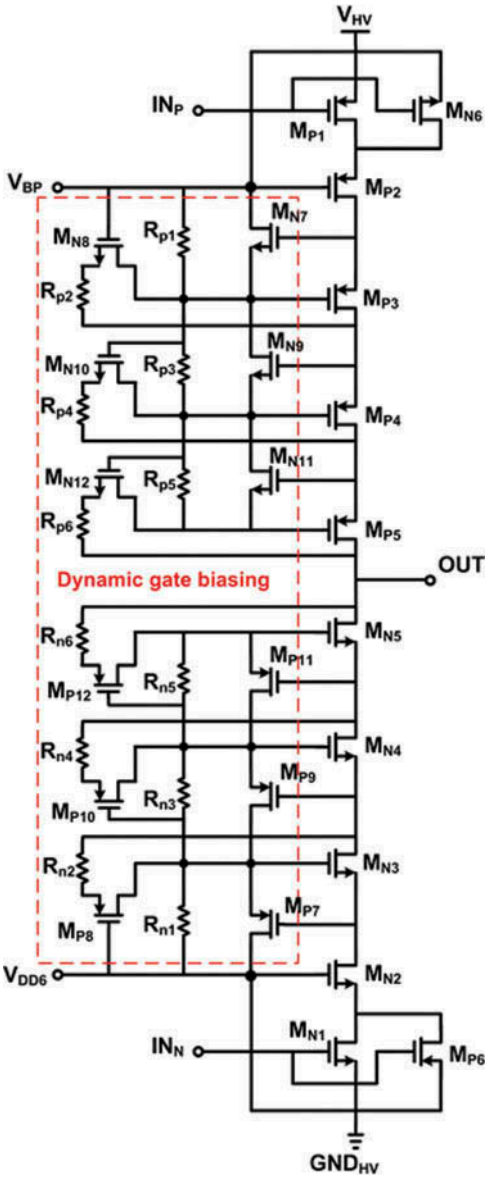

Figure 4. Schematic of the proposed HV output driver.

3.2. *Proposed HV transmitter*

The proposed ultrasound transmitter IC consists of three stages as described in the previous section. The key part of the transmitter chain is the push–pull output driver which excites the following CMUT with an HV pulse signal to generate a large acoustic pressure signal. Figure 4 shows the schematic of the proposed HV output driver. In comparison to the output driver stage in the previous HV transmitter, all the HV DMOS transistors M_{HVN1}, M_{HVP1} in Figure 3 are replaced with 6-V standard CMOS transistors. Five stacks of NMOS transistors M_{N1}, M_{N2}, M_{N3}, M_{N4} and M_{N5} and PMOS

transistors M_{P1}, M_{P2}, M_{P3}, M_{P4} and M_{P5} are used in this version to support up to 30-Vp-p output swing to operate without oxide or junction breakdown reliability issues for all different process corners. To make the smooth push–pull operation possible, dynamic gate biasing circuit is utilised to correctly bias the gate of the stacked transistors during ON–OFF transitions, and also limits the internal drain-source nodes to be within the allowable voltage range. The dynamic gate biasing circuit is comprised of R_{n1} to R_{n6} resistors and M_{P7} to M_{P12} transistors for the NMOS output driver part, and R_{p1} to R_{p6} resistors and M_{N7} to M_{N12} transistors for the PMOS output driver part. This is a modified and improved version from Serneels, Piessens, Steyaert, & Dehaene's (2005) with reduced overall complexity. For this design, area-consuming capacitors in the dynamic biasing circuit have been removed as the parasitic gate-drain capacitance which causes the overshoot during transitions observed in Serneels et al.'s (2005) was not critical as the operation frequency is lower and the transistor sizes are smaller.

For the operation analysis of the output driver, two operation state transitions are considered for the NMOS output part.

When IN_N becomes logic 'high' (a low-to-high input transition from 0 to 6 V), this will turn ON M_{N1} which will cause the source node of M_{N2} to become discharged and turn ON M_{N2} as the gate of M_{N2} is constantly biased at V_{DD6}. As the drain of M_{N2} becomes discharged, this turns on M_{P7} and causes the gate of M_{N3} to be shorted to V_{DD6}, also turning on M_{N3}. This is similar for M_{N4} and M_{N5}. The voltage at the output node is discharged and approximately becomes equal to $GND_{HV} + V_{DS\_MN1,2,3,4,5}$, where $V_{DS\_MN1,2,3,4,5}$ is equal to the voltage drop due to the dynamic current flowing through the transistor channels multiplied by the combined R_{ON} resistance of M_{N1}, M_{N2}, M_{N3}, M_{N4} and M_{N5}. The size ratio (W/L) of the output transistors is relatively large in order to reduce the on-resistance to minimise the voltage drop between the drain and source terminals during ON operation. However, the area and the parasitic capacitance which results as a trade-off is also considered which decides the overall size. Careful simulations are done in order to optimise the sizes of the output transistors so that required transitions can be achieved between 0 and 30 V with the output capacitive load. At this state, M_{P8}, M_{P10} and M_{P12} are OFF as the source-gate voltage is nearly equal and thus is at cut-off.

When IN_N becomes logic 'low' (a high-to-low input transition), this will turn OFF M_{N1}, M_{N2}, M_{N3}, M_{N4} and M_{N5}, and the internal nodes will automatically be set at appropriate voltages by the dynamic bias circuit to make sure gate oxide or junction breakdown is prevented and that 30 V is evenly distributed among drain-to-source terminals of the stacked transistors. For example, the gate voltage of M_{N5} is decided by the resistive division of R_{n6}, R_{ON_MP12} and R_{n5} resistors between the output node voltage and the bias voltage of M_{N2}, which is at V_{DD6}. The operation for the PMOS part is identical to the NMOS part, except that it is complementary.

Figure 5 shows the second level-shifter and tapered buffer used to convert a 0–6 V swinging pulse to a 24–30 V pulse to drive the PMOS gate of the output driver. Similar to the output driver, all the transistors used are standard thin-oxide 1.8-V or thick oxide 6-V CMOS transistors provided by the process. The gate of M_{N1} (IN_N) is driven by a 6-Vp-p pulse signal, while the gate of M_{N2} (IN_P) is driven by the inverted 6-Vp-p pulse. When IN_N is logic 'high', this will turn ON M_{N1} which will cause the source node of M_{N2} to become discharged and turn ON M_{N3} as the gate of M_{N3} is constantly biased at V_{DD6}. As the drain of M_{N3} becomes discharged, this turns on M_{P5} and causes the gate of M_{N3} to be shorted to V_{DD6}, also turning ON M_{N3}. Again, this is similar for M_{N4} and M_{N5}. The voltage of 'A' node becomes V_{HV}-V_{DS_MP1}, which turns ON M_{P3}, and node 'B' is shorted

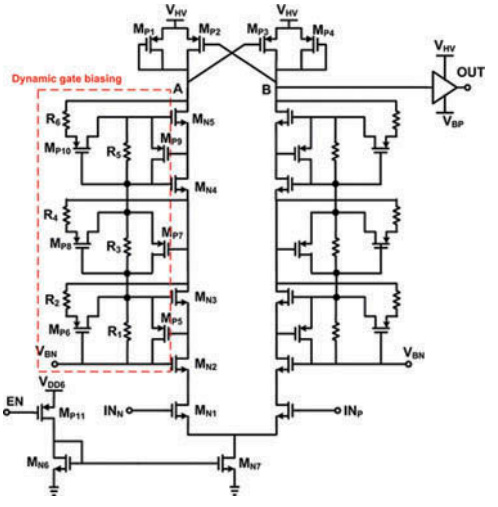

Figure 5. Schematic of the proposed **6**-to-24 V level-shifter.

to V_{HV}. Both the 'A' and 'B' nodes transit between V_{HV} and V_{HV}-$V_{DS\_MP1,4}$, in which $V_{DS\_MP1,4}$ is decided to be around 6 V controlled by the sizing of the $M_{P1,4}$ transistors. The following tapered buffer, which drives the PMOS input of the following output driver, adjusts the output signal to swing between V_{HV} and V_{BP}, where V_{BP} is controlled to be approximately around V_{HV}-6 V.

The first stage level-shifter in Figure 1 is a conventional static level-shifter (Osaki, Hirose, Kuroki, & Numa, 2011) used to convert a 1.8-Vp-p signal to 6-Vp-p signal.

4. Simulation results

The HV ultrasound transmitter IC is designed using 1-poly 6-metal 0.18-µm CMOS process. Figure 6 shows the transient simulation plot using Cadence Spectre in which a 1.8-Vp-p, 384-ns pulse width input trigger signal is applied to the first level-shifter input and the 30-Vp-p pulse signal results at the output of the driver with small delay. Less than 10 ns delay and rise/fall times are observed in the simulations. To check the reliability of

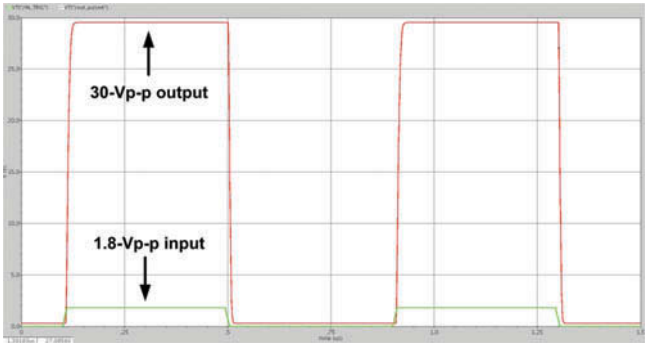

Figure 6. Transient simulation plot capture for input trigger versus HV output pulse.

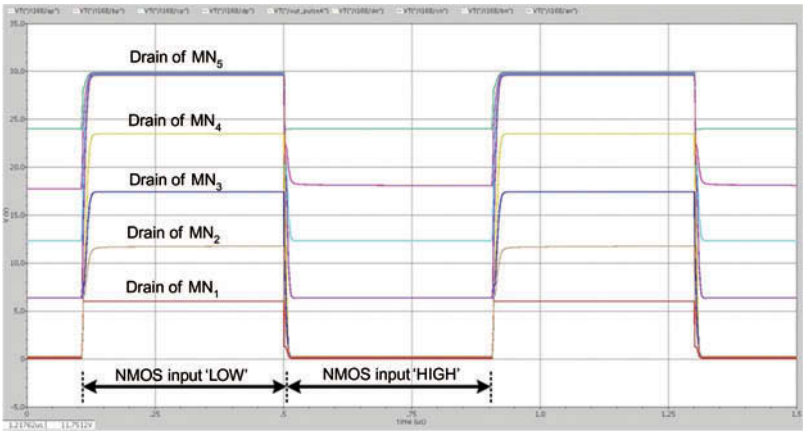

Figure 7. Transient simulation plot capture of drain nodes of stacked transistors.

the proposed stacked architecture, Figure 7 shows the probed drain node voltages of NMOS output driver transistors during ON–OFF transitions. 30 V is distributed evenly among the stacked transistors to make sure all the terminal voltages are within the technology limit of 6 V. All the internal nodes in the output driver, including the dynamic bias circuit, meet the process limits for all simulation process, voltage, temperature corners. Similarly, the internal nodes of the second level-shifter are checked for reliability during ON–OFF transitions. The load condition at the output driver in this simulation is an equivalent electrical CMUT model with additional parallel parasitic capacitance of 10 pF. The performance summary of the proposed transmitter with a comparison to other previous HV transmitters is summarised in Table 1. In comparison to previous HV

Table 1. Performance summary of designed CMOS HV transmitter.

Parameter	This work	[3]	[4]
Blocks	Two voltage level-shifters + HV output driver	Two voltage level-shifters + HV output driver	DC–DC, level-shifter, HV output driver
Transmitter input voltage	1.8 Vp-p	1.8 Vp-p	5 Vp-p
Transmitter output voltage	30 Vp-p unipolor pulse	30 Vp-p unipolar pluse	59 Vp-p
Transmitter input trigger frequency	1.25 MHZ	50 MHz	2 MHz
Input–output delay	<10 ns	N/A	N/A
Rise/fall time	<10 ns	N/A	69/58 ns
Output loading capacitance	20 pF	44 pF	20 pF
Power consumption	45 mA dynamic/ 0.68 mA	300 mA dynamic/ 28 mA static (simulated)	200 mA dynamic (simulated)
Chip area	0.15 × 0.25 mm^2	0.19 × 0.45 mm^2	5 × 0.85 mm^2
Process technology	0.18µm CMOS	0.18µm CMOS/DMOS	0.18µm CMOS/DMOS

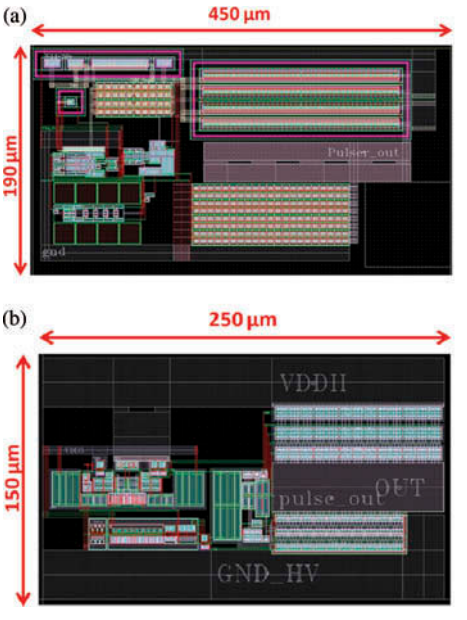

Figure 8. Layout comparison of transmitter IC (a) previous approach and (b) proposed approach.

transmitters, this work shows reduction in area, while providing a low-cost solution by utilising only standard CMOS transistors in the design.

A special attention is given in the layout stage to isolate the HV operating circuits and the regular voltage parts. Also, wide top metals are used to route the HV supply, HV ground and output nodes from the core to the pads to minimise the parasitic resistance and support high dynamic current through this path. In comparison with our previously developed conventional transmitter using area-hungry DMOS devices (Zhao et al., 2011), the core area including the output driver and two level-shifters has been dramatically reduced by over 50%. The layout capture comparison is shown in Figure 8, where the total chip area of the proposed core using stacked standard CMOS transistors and dynamic bias circuit is 0.0375 mm² including wide TOP metal routing paths for the HV supply and ground lines.

5. Conclusions

An HV ultrasound transmitter IC for multi-array medical imaging applications is designed using 0.18-µm standard CMOS process. The HV transmitter, which includes the proposed output driver and level-shifter with dynamic bias circuits, achieves up to 30-Vp-p output pulse signal with robust reliability while only utilising standard CMOS transistors for high integration and low-cost approach. In comparison with the previous works which utilise HV transistors, the area of the HV transmitter IC is reduced by more than 50% under similar operation conditions.

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