Digital RF and Digitally-Assisted RF (Invited)

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***Abstract*—One of the most important developments in the wireless industry within the last decade was the digitization of RF circuitry. This was in response to the incredible advancements of the mainstream CMOS technology in both processing speed and circuit density, as well as the relentless push to reduce total solution costs through integration of RF, analog and digital circuitry. Since the digital baseband part of a wireless communication channel has been traditionally implemented in the most advanced CMOS technology available at a given time for mass production, the need for single-chip CMOS integration has forced permanent changes to the way RF circuits are fundamentally designed. In this low-voltage nanometer-scale CMOS environment, the high-performance RF circuits must exploit the time-domain design paradigm and heavily rely on digital assistance. This paper revisits the digitization journey of RF circuits.**

***Index Terms*—All-digital phase-locked loop (ADPLL), built-in self-test (BIST), calibration, compensation, digital-assistance of RF, digitally-controlled oscillator (DCO), digitally-controlled power amplifier (DPA), discrete-time receiver (DT-RX), nanometer-scale CMOS, time-to-digital converter (TDC).**

I. Introduction

A. Analog-Intensive RF Transceivers

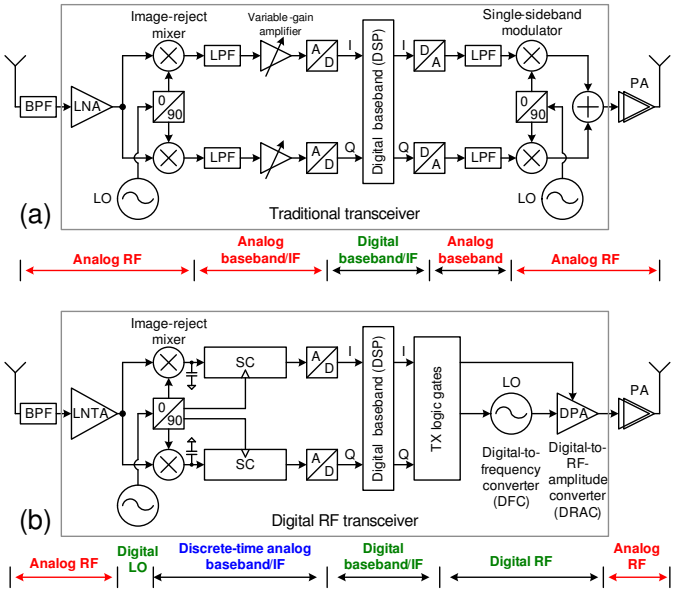

Fig. 1. Comparison between (a) conventional analog-intensive RF transceiver and; (b) new transceiver based on the Digital RF principles.

Until around mid-1990's, virtually all radio frequency (RF) transmitters/receivers (transceivers) have been analog intensive and based on an architecture similar to that shown in Fig. 1(a) [1]. On the receiver (RX) path, the signal from an antenna is filtered by a typically-external bandpass filter (BPF) to attenuate out-of-band blockers. The signal is then amplified by a low-noise amplifier (LNA) and downconverted (i.e., frequency translated) to a baseband frequency (dc or a low intermediate frequency, IF, being a fraction of a channel separation) through an image-reject downconversion mixer operating in in-phase ($I \equiv \Re(S)$) and quadrature ($I \equiv \Im(S)$) complex-number signal S domain. $\Re(S)$ and $\Im(S)$ are the real and imaginary components, respectively, of a complex signal S. The signal is then further low-pass filtered (LPF) and amplified before being finally converted into digital discrete-time samples through analog-to-digital converter (ADC or A/D). The digital baseband processes the signal samples to estimate the original transmitted symbols, from which the user information data is obtained.

On the transmitter (TX) path, the user information data gets converted into symbols, which are then pulse-shaped to obtain baseband I and Q digital samples that are frequency-band-constrained. They are then converted into analog continuous-time domain through a digital-to-analog converter (DAC or D/A) with a typical zero-order-hold function. The LPF following the DAC then filters out the switching harmonics. Thus obtained analog baseband signal gets then upconverted (frequency translated) into RF through an image-reject single-sideband (SSB) modulator. The following (typically external) power amplifier (PA) increases the RF power level at the antenna to that that required by the wireless standard, which could be as high as 2 W for a GSM handset. While the complex-number representation of the baseband signal is known to be always I/Q for the receiver, the complex number representation for the transmitter could be realized as either I/Q (shown in Fig. 1(a)) or polar, in which the two orthogonal components are amplitude $A = |S|$ and phase $\phi = \angle S$, or $S = Ae^{j\phi}$. The phase modulation could be performed by a direct or indirect frequency modulation of a phase-locked loop (PLL). The amplitude modulation could be performed by V_{DD} modulation of a high-efficiency class-E PA.

The frequency synthesizer-based local oscillator (LO) performs the frequency translation for both the RX and TX. It is typically realized as a charge-pump PLL with $\Sigma\Delta$ dithering of the modulus divider to realize the fractional-N frequency division ratio.

The complete architecture and monolithic circuit design techniques of the conventional transceivers of Fig. 1(a) have been well described in numerous literature and text books. The architecture has been successfully used in integrated CMOS transceivers [2] for over a decade (since late 1990's). Unfortunately, its useful lifetime is slowly coming to an end [3] in favor of more digitally-intensive architectures, such as

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the one shown in Fig. 1(b).

B. Digitally-Intensive RF Transceivers

The main reasons behind this sea-like transformation are the ever-improving cost advantages and processing capabilities of the CMOS technology, which have been happening at regular intervals with the pace according to the so-called Moore's Law. Basically, with every CMOS process technology advancement node (i.e., from 130-nm to 90-nm, then to 65-nm, and then to 40-nm, and so on) happening every 18–24 months, the digital gate density, being a measure of the digital processing capability, doubles (i.e., gate area scaling factor of 0.5x). At the same time, the basic gate delay, being a measure of the digital processing speed, improves linearly (i.e., gate delay scaling factor of 0.7x). Likewise, the cost of fabricated silicon per unit area remains roughly the same at its high-volume production maturity stage. Indeed, over the last decade, the cost of silicon charged by integrated circuit (IC) fabs has remained constant at around US$ 0.10–0.25/mm^2, depending on the wafer volume and targeted gross profit margin (GPM). The main implication of this is that a cost of a given digital function, such as a GSM detector or an MP3 decoder, can be cut in half every 18-24 months when transitioned to a newer CMOS technology. At the same time, the circuits consume proportionately less power and are faster.

Unfortunately, these wonderful benefits of the digital scaling are not shared by the traditional RF circuits. What's more, the strict application of the Fig. 1(a) architecture to the advanced CMOS process node might actually result in a larger silicon area, poorer RF performance and higher consumed power. The constant scaling of the CMOS technology has had an unfortunate effect on the linear capabilities of analog transistors. To maintain reliability of scaled-down MOS devices, the V_{DD} supply voltage keeps on going down, while the threshold voltage V_t remains roughly constant (to maintain the leakage current). This has a negative effect on the available voltage margin when the transistors are intended to operate as current sources. What's more, the implant pockets added for the benefit of digital operation, have drastically degraded the MOS channel dynamic resistance r_{ds}, thus severely reducing the quality of MOS current sources and the maximum available voltage self-gain $g_m \cdot r_{ds}$ (g_m is the transconductance gain of a transistor). Furthermore, due to the thin gate dielectric becoming ever thinner, large high-density capacitors realized as MOS switches are becoming unacceptably leaky. This prevents an efficient implementation of low-frequency baseband filters and charge-pump PLL loop filters.

The above observation is graphically captured in Fig. 2. The raw analog performance, which is based on the traditional linear transistor operation, keeps on getting worse with each CMOS process node advancement in almost every aspect. On the other hand, the raw digital capability, in terms of processing sophistication and speed, is improving. An interesting question is whether the new powerful, yet inexpensive, digital logic and memory can compensate (through well-known techniques such as calibration, compensation and predistortion) for the increasing handicap of analog performance.

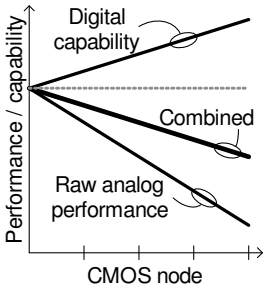

Fig. 2. Effect of CMOS process advancement on digital and, ultimately, RF performance.

The unfortunate answer is generally "no". The raw performance degradation of RF circuits is much worse than the assistance the digital processing can offer. The chief reason for this negative answer is the sheer complexity of the transceiver component interaction. While it might be possible in an isolated case to calibrate or compensate for single parameter degradation, a degraded component typically affects multitude of parameters, which are very difficult or even impossible, within a given processing budget, to simultaneously calibrate. For example, an imperfection of active devices in an RX down-conversion mixer can simultaneously increase the leakage between the LO and input ports, which then increases dc offset at the mixer output, as well degrades the mixer's linearity in addition to skewing the delay between the I and Q paths. All these three system imperfections contribute to the signal distortion in a way that is difficult to isolate from each other. This makes the calibration algorithm disproportionately more complex or even unfeasible.

A quick survey of the most recent literature reveals no such impending doom and gloom. In fact, the RF performance of highly integrated system-on-chip (SoC)'s actually keeps on improving. The reason for this apparent paradox is the *changing* nature of the RF circuit design. Just like it has happened with the analog audio processing in the 1980's and 1990's, when new digitally-intensive techniques (oversampling, $\Sigma\Delta$ noise shaping, calibration, etc.) started being employed, the same level of sea change is being experienced now in the field of RF circuit design. Arguably, the first demonstrations of the new all-digital approaches to RF [4] [5] were so revolutionary that they must have been perceived as threatening enough to the traditionally-minded RF design community, such that a frantic search for more evolutionary alternatives has been spurred. Even though the new Digital RF approach is now dominant in mobile phones, the analog-intensive alternatives still exist. However, their nature has been changed forever.

II. New Paradigm of RF Design in Nanometer-Scale CMOS

The author considers himself fortunate enough that his small group at Texas Instruments in Dallas, TX, USA, back at the end of 1999 was believed the first ever in the world to have tried to design RF circuits in deeply-scaled CMOS

environment (130 nm CMOS node at that time). To put this into proper perspective: The design of RF circuits in any type of CMOS around the year 2000 was so uncommon in industry that it was generally met with incredulity and derision, and it took a few prominent researchers in academia [2] [6] to gradually change that negative perception. On top of that, our desire was not only to use CMOS for RF circuit design but rather its most advanced digital version for the purpose of single-chip radio integration. This general atmosphere of ignorance, negativity and avoidance outside of our immediate group has given us enough head start and secure a few years of development advantages. As a result, Texas Instrument's market share in RF has risen from virtually zero in 1999 to about 33% nowadays.

Our early attempt at designing RF circuits in advanced CMOS has made it clear that we were facing a new paradigm, which has allowed us to form a foundation of a new area of electronics: Digital RF. The new paradigm was first formulated in the author's 2002 Ph.D. thesis [7] (subsequently republished as a 2006 Wiley book [8]) and is repeated below:

> In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals.

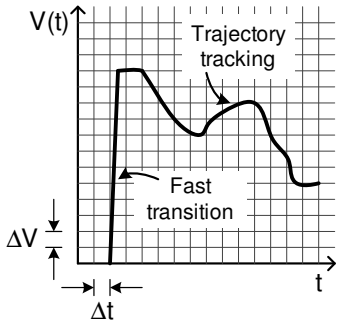

Fig. 3. Time-domain vs. voltage-domain view of a signal representation.

In the good old days of analog IC design with the supply voltage of ± 15 V (yes! both positive and negative feeds simultaneously available), then 12 V, then 5 V, then 3.3 V, and finally 2.5 V, a large voltage headroom could be exploited for precise voltage tracking and setting of an analog waveform. Nowadays, with only 1.1–1.4 V, which needs to be spent on 500–600 mV of threshold voltage per each NMOS and PMOS transistor, there is little voltage headroom to perform any sophisticated analog processing. However, the MOS transistors are now extremely fast and can switch between V_{SS} and V_{DD} supply levels in almost no time. Hence, the information can be tracked and processed as timestamps of sharp transitions between V_{SS} and V_{DD}.

Fig. 3 further illustrates this point. The increasing level of noise makes the voltage resolution ΔV worse. Combined with the decreasing levels of supply voltage $V_{DD} - V_{SS}$, which lowers the maximum voltage swing V_{max}, the dynamic range $(V_{max}/\Delta V)$ of the signal gets lower.

Consider now the references available to the IC designers. A typical tolerance of monolithic voltage/current sources or resistive/capacitative components ranges from 0.5 to 10%. Trimming, heavily used in precision analog IC's, can bring down these tolerances to the 0.1–1% level, albeit at a high cost, which could virtually make it prohibitive for high-volume consumer products. At the same time, a mixed-signal IC would typically contain a crystal-stabilized reference clock with the tolerance of 1–100 ppm (parts per million), which is orders of magnitude better. It all means that the time reference already available to the analog/mixed-signal/RF designers has superior relative quality to the other components and the timestamps of level transition events could be used as a means of transmitting information. This is another argument for moving towards the time-domain operation. "It is time to use time..."

Despite the early misconceptions that the digitalization of RF would somehow produce more phase noise, spurs and distortion, the resulting digitally-intensive architecture is likely to be overall more robust by actually producing lower phase noise and spurious degradation of the transmitter chain and lower noise figure of the receiver chain in face of millions of active logic gates on the same silicon die, as repeatedly proven in subsequent publications [4] [5] [9] [10]. Additionally, the new architecture would be highly reconfigurable with analog blocks that are controlled by software to guarantee the best achievable performance and parametric yield. Another benefit of the new architecture would be an easy migration from one process node to the next without significant rework.

III. RF-SoC Landscape

Let us examine the landscape of RF system-on-chip (RF-SoC)'s based on the published literature. Table I shows the list of seven disclosures. They all came from commercial efforts involving large design teams.

The very first published report of an RF-SoC was in 2001 from Alcatel [11] targeting the Bluetooth standard. Its silicon area was 40 mm^2 in 250 nm CMOS. It was a significant commercial endeavor but, to the author's best knowledge, the chip never went into volume production. The second published RF-SoC [4] was from the author's former group in Texas Instruments (TI). It occupies only 10 mm^2 in 130 nm CMOS and is based on the presented Digital RF principles. It was put into volume production a few years earlier, which continues to this moment despite the fact that the original 130 nm architecture was subsequently fine-tuned to the 90-nm, then 65-nm and, most-recently, 45-nm CMOS nodes and adjusted for the polar TX modulation to handle the extended data rates (EDR) of 2 Mb/s and 3 Mb/s.

The third published RF-SoC and the first one targeting a cellular standard, was in 2006 from Infineon [12]. The GSM single-chip radio occupies 34 mm^2 in 130 nm CMOS and got created by combining Infineon's existing digital baseband (DBB) and transceiver (TRX) 130 nm chips. The RF/analog portion takes 13 mm^2, which is 38% of the total area. The fourth published RF-SoC [13] was also in the same year but targeted the Personal Handy-Phone System (PHS) standard in

TABLE I
PUBLISHED WIRELESS RF-SOC'S.

	Company	Year	Wireless Standard	CMOS node [nm]	SoC area [mm^2]	RF area [mm^2]	RF supply [V]	TX current [mA]	RX current [mA]	LO arch	TX arch	RX arch
[11]	Alcatel	2001	Bluetooth	250	40.1	10	2.5	52	41	$\Sigma\Delta$ CP-PLL	ana.-IQ	ana.-IQ
[4]	TI	2004	Bluetooth	130	10	3	1.5	25	37	ADPLL	dig.-FM	SC-IQ
[12]	Infineon	2006	GSM	130	34	13	2.5	90	120	$\Sigma\Delta$ CP-PLL	frac-PLL	ana.-IQ
[13]	Atheros	2006	PHS (1.9GHz)	180	33	12	3.0/1.8	54	57	$\Sigma\Delta$ CP-PLL	ana.-IQ	ana.-IQ
[9]	TI	2008	GSM	90	24	3.8	1.5	47	56	ADPLL	dig.-polar	SC-IQ
[14]	Atheros	2008	Bluetooth v2	130	9.2	3	1.2	19.3	29.7	$\Sigma\Delta$ CP-PLL	ana.-polar	ana.-IQ
[15]	Atheros	2008	2x2 .n WLAN	130	36	11	3.3/1.2	280	310	$\Sigma\Delta$ CP-PLL	ana.-polar	ana.-IQ

the 1900 MHz frequency band used mainly in Japan and in parts of China. It occupies 35 mm^2 SoC in 180 nm CMOS and RF/analog area is 11 mm^2, which is about 30% of the total.

The fifth RF-SoC [9] and the first implemented in a nanometer-scale CMOS (feature size less than 100 nm), was in 2008 from the author's group in TI targeting GSM and based on the second-generation of the Digital RF principles. The silicon area is 24 mm^2 in 90 nm CMOS, 3.8 mm^2 of which is used by RF/analog, which makes it only 16%.

In the same year of 2008, there were two other disclosures, both from Atheros and using 130 nm CMOS. The first [14] is targeting the EDR version of Bluetooth, and the second [15] is targeting the 2x2 MIMO wireless LAN. The silicon area is 9.2 mm^2 and 36 mm^2 and the RF/analog occupies 33% and 31%, respectively.

All the seven RF-SoC's, except for the two from TI based on the Digital RF principles, are based on the conventional analog-intensive architecture: The LO's frequency synthesizer is build using a charge-pump PLL in which the fractional frequency resolution is obtained through $\Sigma\Delta$ dithering of the modulus divider. The transmitter is either analog I/Q or analog polar topology, while the receiver is a typical continuous-time mixer-based architecture. In contrast, the digitally-intensive implementations by TI [4] [9] use all-digital phase-locked loop (ADPLL) for LO, digital polar modulator for TX and switched-cap (SC)-based discrete-time RX. All of them, however, disclose employment of the digital assistance of RF (except for [12]).

Table I clearly shows the CMOS scaling trend when implementing fully-integrated RF radios, whether using the traditional analog-intensive or new digital-intensive approaches. The analog-intensive approaches, however, do not fully benefit from scaling. Their silicon area and power consumption (RF supply times TX/RX current) tend to be much higher. Non-cellular wireless applications require less stringent RF performance but the lower supply voltage of core transistors appears to be achievable only with Bluetooth, which is considered the least demanding of all popular standards. As no publications for single-chip radios in nanoscale CMOS have yet been reported for that traditional approach, their scaling effectiveness is yet to be seen. It should be noted that fair comparison of the proposed techniques is best afforded against other SoC radios with predominantly digital content, which typically allocate only 15–40% of the die area to the RF transceiver functionality. Production issues, such as yield loss due to parametric variability of analog/RF circuits, test coverage, required time and cost of RF test, calibration and compensation [16], are not appreciated to the same degree as with testchips and stand-alone RF transceivers but can significantly impact the SoC design style and architectural choices.

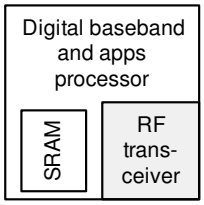

Fig. 4. RF transceiver as part of a larger RF-SoC.

The examples of published commercial RF-SoC's consistently reveal that the RF portion of entire SoC is only 15-40%, as shown in Fig. 4. It means that the majority of the area is occupied by the digital logic and memory in order to implement the digital baseband together with various controller and application processor functionality. For this reason, the logic and memory determine the technology choice and it is rather not favorable to the linear RF operation.

IV. DIGITAL RF PROCESSOR (DRP$^{\mathrm{TM}}$)

The Digital RF principles have been used in TI to develop three generations of a commercial Digital RF Processor (DRP$^{\mathrm{TM}}$): single-chip Bluetooth [4], GSM [9] and EDGE [10] radios realized in 130-nm, 90-nm and 65-nm digital CMOS process technologies, respectively. Fig. 5 shows the chip micrographs. It is estimated that the cellular market share of DRP is currently 33% of the worldwide annual production. In addition, TI's high-volume wireless connectivity RF-SoC's in 90 nm, 65 nm and 45 nm CMOS are designed according to these principles. When combined with TI's competitors' products also having embraced these principles, it appears that Digital RF is now the predominant architecture found in entry-level and feature cellular phones.

Fig. 6 highlights the common RF-SoC architecture of DRP products with added features specific to the cellular radio. At the heart of the transceiver lies the all-digital PLL

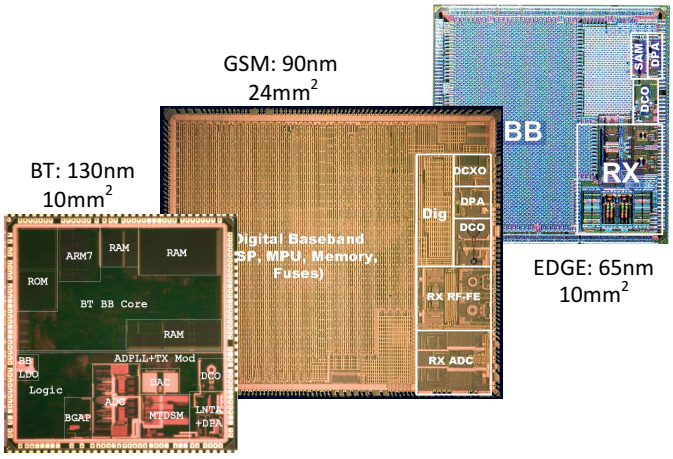

Fig. 5. Chip micrographs of the commercial single-chip RF-SoC's employing three generations of DRP: (left-to-right) 130 nm Bluetooth; 90 nm GSM; and 65 nm GSM/GPRS/EDGE.

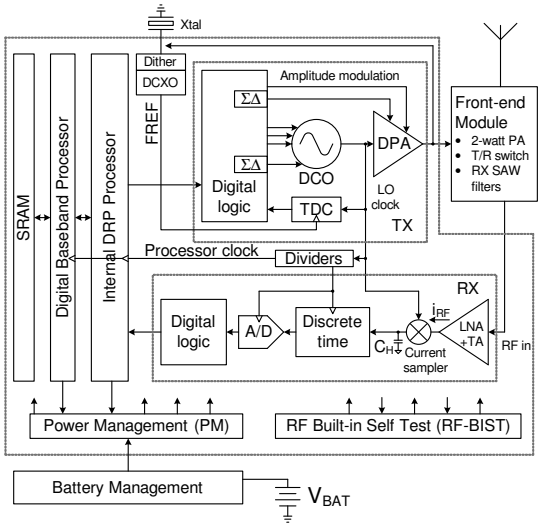

Fig. 6. Single-chip GSM cellular radio based on the second generation of DRP. Script Processor communicates with the digital baseband processor and oversees the entire RF transmitter and receiver functionality.

(ADPLL) [5], generating local oscillator (LO) and almost all other clocks, including those for the DBB. The ADPLL-based transmitter employs the polar architecture with all-digital phase/frequency and amplitude modulation paths. The receiver [17] employs a discrete-time architecture in which the RF signal is directly sampled and processed using analog and digital signal processing techniques. The antenna RF input signal is amplified and converted into the current domain by a low noise transconductance amplifier (LNTA). The RF current is then directly sampled or mixed to zero-IF or very-low-IF in the charge domain. The signal is then filtered and converted into the digital domain for further conditioning. A digitally-controlled crystal oscillator (DCXO) generates a high-quality basestation-synchronized frequency reference such that the transmitted carrier frequencies and the received symbol rates are accurate to within 0.1 ppm. A power management system consists of a bandgap generator and multiple low drop-out (LDO) linear regulators to supply voltage to various radio subsystems as well as to provide good noise isolation between them. Various calibration and compensation procedures are exercised to keep the transceiver performance at optimum irrespective of the process and environmental conditions. One such example is a periodic "just-in-time" compensation of the DCO gain variations [18]. An RF built-in self-test (RF-BIST) [16] executes an autonomous transceiver performance and compliance testing of the GSM standard. The embedded processor [19] handles various TX and RX process calibration, voltage and temperature compensation, sequencing and lower-rate datapath tasks and encapsulates the transceiver complexity in order to present a much simpler software programming model. The data and high-level control is routed from/to digital baseband processor via data bus router. The transceiver is integrated with the digital baseband, SRAM memory in a complete system-on-chip (SoC) solution.

A. Patents on Digital RF

TABLE II
MOST RECENT US PATENTS (OR PATENT PUBLICATIONS) RELATED TO DIGITAL RF.

US patent	Issue date	Company	Country	Area
8,036,611	2011-10-10	ITRI	Taiwan	Dig polar TX
8,032,094	2011-10-04	Panasonic	Japan	DT-RX
8,031,007	2011-10-04	Mediatek	Taiwan	ADPLL
8,031,025	2011-10-04	Mediatek	Taiwan	ADPLL
0234270	2011-09-29	Toshiba	Japan	ADPLL
8,014,487	2011-09-06	NXP	Netherlands	ADPLL
8,013,641	2011-09-06	ETRI	Korea	ADPLL
7,999,623	2011-08-16	Realtek	Taiwan	ADPLL
7,999,586	2011-08-16	Intel	USA	ADPLL
7,999,707	2011-08-16	ETRI	Korea	ADPLL
7,994,867	2011-08-09	Toshiba	Japan	ADPLL
7,994,850	2011-08-09	Qualcomm	USA	DT-RX
7,990,191	2011-08-02	Renesas	Japan	ADPLL
0183639	2011-07-28	Panasonic	Japan	DT-RX
7,982,534	2011-07-19	ITRI	Taiwan	DT-RX
0170640	2011-07-14	Panasonic	Japan	DT-RX
7,979,046	2011-07-12	Orca	USA	DT-RX
7,978,014	2011-07-12	NCTU	Taiwan	ADPLL
7,973,578	2011-07-05	Samsung	Korea	ADPLL
7,974,807	2011-07-05	Qualcomm	USA	ADPLL
7,973,586	2011-07-05	Panasonic	Japan	DT-RX
7,973,609	2011-07-05	Panasonic	Japan	ADPLL
0156783	2011-06-30	NXP	Netherlands	ADPLL

Since TI was years ahead of anyone else in researching this area (see Sec. II), it owns most of the early fundamental patents. The situation nowadays, however, is entirely different. A great majority of the newly issued patents in the area of Digital RF are owned by other companies, as Table II indicates. With the total count of a few hundreds, the Digital RF IP ownership is now mostly spread around the world. This is an indication of a dynamically growing and very healthy industry and parallels the historical development of IC chip. Even though TI invented the IC chip and held the fundamental patents, it obviously did not hurt its fantastic commercial growth. In fact, only a small minority of the patents related to IC nowadays belongs to TI.

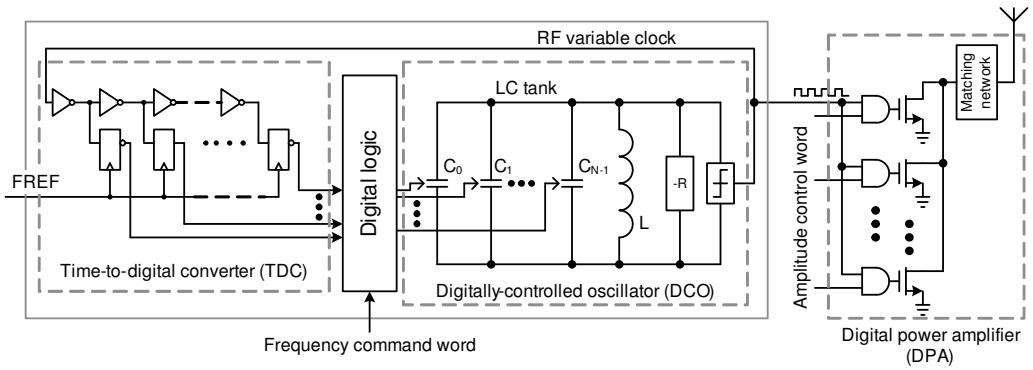

Fig. 7. Simplified view of an all-digital transmitter.

B. All-Digital PLL (ADPLL)-Based Transmitter

The ADPLL, which has replaced the conventional analog-intensive PLL, features a time-to-digital converter (TDC) and digitally-controlled oscillator (DCO). The ADPLL, combined with a novel digital power amplifier (DPA) that replaces the traditional analog-intensive power amplifier, has given rise to an all-digital polar transmitter shown in Fig. 7.

The DCO, which performs RF frequency generation, consists of a large number (hundreds) of tiny binary-controlled varactors, whose step size is only 40aF (atto-farads or 10E-18 farads). This is the smallest the most advanced lithography can create. Despite their miniscule size, their frequency step at the RF (2 GHz) output is as high as 10 kHz, which is too coarse for most wireless standards. The solution was to performed high-speed (100's of MHz) $\Sigma\Delta$ dithering of the single varactor to obtain a much finer time-averaged fractional capacitance. The DCO is a form of a digital-to-analog converter (DAC), where the "analog" output is a frequency deviation. All traditional DAC design concerns, such as device matching, careful layout are applicable here. The DPA is also a form of a DAC, where the "analog" output is an amplitude of the RF sinusoidal output. The amplitude is controlled by regulating the number of active MOS transistor switches by virtue of AND gates. Fine amplitude resolution is achieved also by $\Sigma\Delta$ dithering.

C. Discrete-Time Receiver (DT-RX)

The conventional continuous-time analog-intensive receiver has been replaced with a novel direct-sampling discrete-time (DT) receiver that performs sophisticated filtering right at the mixer level. The receiver architecture uses *direct RF sampling* [4] [20] [21] [22] in the receiver front-end path. In the past, only *subsampling* mixer receiver architectures have been demonstrated: They operate at lower IF frequencies [23] [24] and suffer from noise folding and exhibit susceptibility to clock jitter. A recent study [25] uses a high sampling frequency of 480 MHz after the mixer but adds an RC filtering stage. In this architecture, DT analog signal-processing is used to sample the RF input signal at Nyquist rate of the carrier frequency as it is then down-converted, down-sampled, filtered and converted from analog to digital with a DT $\Sigma\Delta$ ADC. This method achieves great selectivity right at the mixer level. The selectivity is digitally controlled by the local oscillator (LO) clock frequency and capacitance ratios, both of which are extremely well controlled and precise in deep-submicron CMOS processes. The DT filtering at each signal-processing stage is followed by successive decimation. The main philosophy in building the receive path is to provide all the filtering required by the standard as early as possible using a structure that is quite amenable to migration to the more advanced deep-submicron processes. This approach significantly relaxes the design requirements for the following baseband amplifiers.

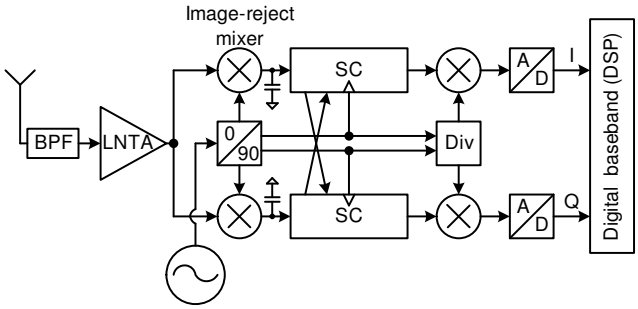

Fig. 8. High IF discrete-time receiver architecture.

The DT RX approach also appears to be a good candidate to realize a fully-monolithic superheterodyne (i.e., high-IF) RX that does not require external IF filters. The conversion from zero-IF (or low-IF) to high-IF processing is as follows: The receiver front-end of Fig. 1(b), which processes the DT signals using separate real-valued I/Q paths, needs to be converted to a complex-valued I/Q path that exhibits a complex-valued band-pass filtering (BPF) characteristics in order not to suffer from the well-known image problems. The BPF is realized via charge-packet sharing between the I and Q paths and is shown in Fig. 8 as the cross-coupling between the two switched-cap (SC) circuits.

The LPF characteristics of DT FIR and IIR filters can be readily converted into BPF characteristics using capacitors and switches of substantially similar sizes. Fig. 9 illustrates the principle and techniques of converting a DT real-valued LPF I/Q path into a complex-valued BPF path. In the conventional architecture, each rotating capacitor C_R [20] is permanently

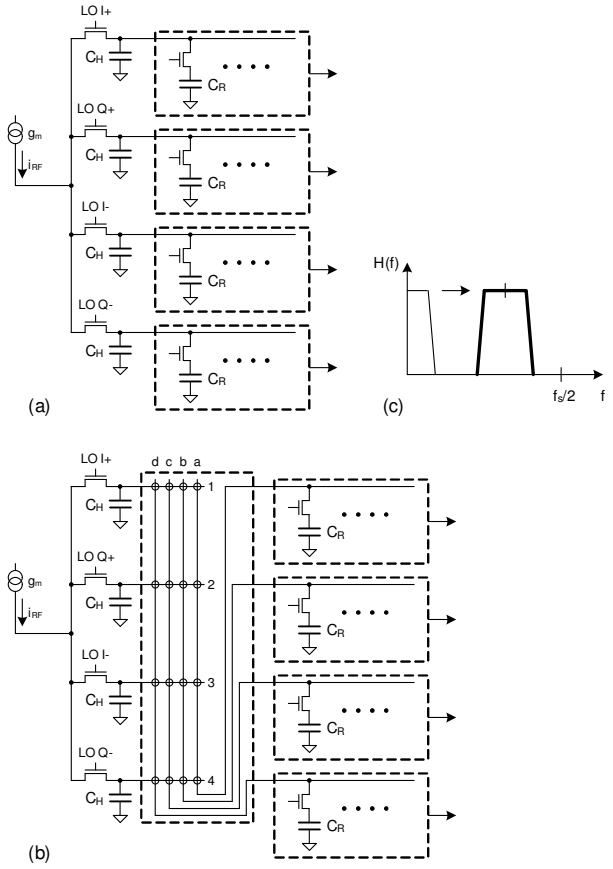

Fig. 9. Details of the DT signal processing: (a) "conventional" zero-IF receiver of Fig. 1(b); (b) proposed high-IF receiver of Fig. 8 that introduces a dynamic switching matrix; (c) principle of LPF conversion into BPF while preserving the transition band characteristics.

assigned to the respective history capacitor C_H. The new architecture breaks that fixed configuration and allows C_S's to be periodically assigned to all four C_H's. This way, the charge holding the information is shared between the quadrature paths and the complex BPF characteristics is realized.

D. RF Built-In Self-Test (RF-BIST)

The testability issues of an RF circuit are probably last on the RF circuit designer's mind. However, a considerable portion of the overall RF-SoC fabrication cost is in its testing. The testing costs are high in case of a complex mixed-signal SoC for RF wireless applications involving extensive and time-consuming defect, performance, and standard compliance measurements. These factory measurements are traditionally made using expensive and sophisticated test equipment. Furthermore, due to the complexity of the equipment and test settings, these measurements cannot be executed at-probe on wafer, before the IC chip is packaged, nor in the field after the chip leaves the factory environment. Consequently, it is desirable to improve testing costs and coverage during the complete life-cycle of an SoC in order to maximize wafer yield, profitability, and customer satisfaction [26].

Frequency synthesizers and transmitters are conventionally tested for RF performance and wireless standard compliance by measuring their output RF port for the correct carrier frequency, phase noise spectrum, integrated phase noise, spurious content, modulated spectrum, and modulated phase trajectory error while stimuli and control signals are applied. The RF-BIST measurement method performs signal-processing calculations on a lower-frequency internal signal to ascertain the RF performance without external test equipment. This significantly saves test time and costs, and increases coverage.

Several RF-BIST functions are now feasible with the all-digital transmitter and digitally-intensive discrete-time receiver. They include digital loop-back, mixed-signal feedback loop (for dc offset cancellation) and TX-RX RF loop-back at the mixer. Coupling at the package can be used to realize an external TX-RX feedback loop that incorporates the entire transceiver. A programmable sine/cosine waveform generates feedback signals that are fed to the mixer through the offset correction loop to establish an additional analog feedback. This loop can be used to perform several calibration and test functions. Because of reuse of the on-die processor, very little hardware overhead is required for RF-BIST.

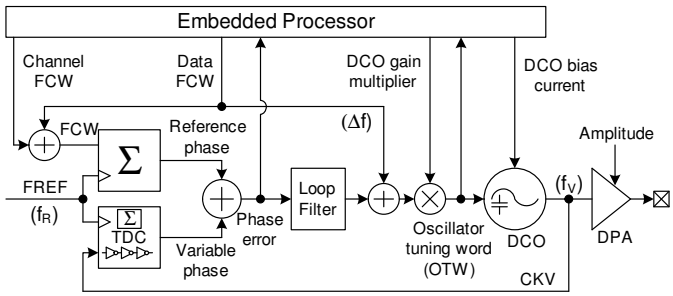

Fig. 10. An embedded processor providing digital assistance to the ADPLL-based transmitter. DPA is a digitally-controlled amplifier.

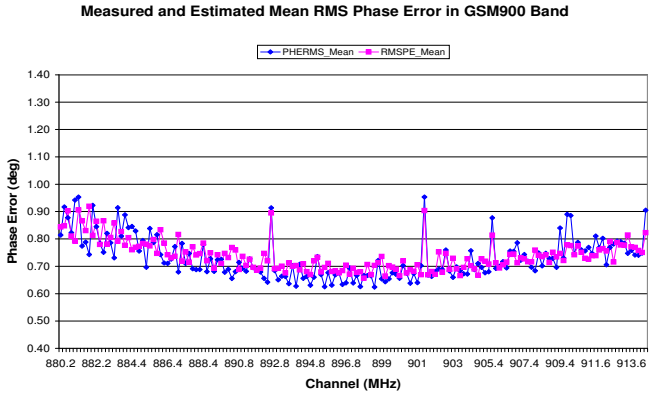

Fig. 11. Measured modulation distortion (i.e., phase trajectory error) vs. calculated from the digital phase error statistics (i.e., rms of PHE).

The embedded processor is also used to reduce the overall current consumption while maximizing the RF performance [19]. The parameter of interest to which the DCO current and voltage need to be adjusted is the overall close-in RF transmitter performance captured in such metrics as the modulation

spectrum, as well as rms and peak of the phase trajectory error (PTE), in case of GSM. These measurements are fairly complicated and require the use of an expensive external test equipment connected to the RF TX output port. At best, they can be used in factory to calibrate for the process changes but they simply rule out compensation for environmental conditions. The novel approach proposed in [16] solves the problem by calculating statistics of an internal signal, i.e., digital phase error samples of Fig. 10, as a proxy for the performance at the RF output port. In this method, the FFT, rms and peak of the digital phase error samples are processed by the internal processor in real-time to estimate the phase noise spectrum, and rms and peak of the PTE, respectively, at the RF output. The calculated statistics are then compared directly against the GSM specifications. Fig. 11 shows such comparison. This allows to trade off supply voltage and current consumption versus the required circuit performance. For example, the max. DCO bias current of 18 mA in [9] can be reduced to as low as 6 mA if the wafer process is not weak and the die temperature is not high. Fig. 11 shows the tradeoff between the measured phase noise performance and the current consumption.

V. Conclusion

We have presented the recent revolution in the area of RF circuit design in highly-scaled CMOS processes. It was driven by the desire to exploit the increasing power and affordability of CMOS technology for the purpose of reducing the wireless solution costs through system-on-chip (SoC) integration. It was found that implementing the traditional RF circuits in more and more advanced CMOS would make its performance increasingly worse, so the new RF architectures and design approaches had to be invented. Enter "Digital RF": The transformation of the RF transceiver functionality into the novel time-domain operation, as embodied by the time-to-digital converter (TDC)- and digitally-controlled oscillator (DCO)-based all-digital phase-locked loop (ADPLL), and the discrete-time receiver exploiting sophisticated signal processing, such as IIR. Enter "Digital assistance of RF": heavy use of digital logic and memory to assist with the linear performance of analog transistors – it also falls under the umbrella of this new technology. The new approach has proven to be very successful in the commercial world by substantially reducing cost, form factor and current consumption while increasing production yield and time-to-market.

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