Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator

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***Abstract*—This paper presents the design of a low-voltage ultralow-power relaxation oscillator without external components. The application field for this oscillator is the clock generation of low-power wake-up functions for battery-operated systems. A detailed analysis of the oscillator, including the temperature performance, is derived and verified with experimental results. The oscillator operates at a typical frequency of 3.3 kHz and consumes 11 nW from a 1-V supply at room temperature, and a temperature drift of less than 500 ppm/°C is achieved over the temperature range of −20 °C to 80 °C. An efficient design implementation has resulted in a cell area of 0.1 mm^2 in a standard 0.35-μm digital CMOS technology.**

***Index Terms*—Clock generator, CMOS integrated circuits, low power, low voltage, relaxation oscillators, weak inversion.**

I. Introduction

LOW-POWER building blocks are essential for battery-operated medical devices such as heart rate monitors, blood glucose meters, or pacemakers in order to maximize the battery lifetime [1]. Such devices are in standby mode most of the time and are woken up at a regular interval for a very short time to perform a measurement. The system is set into a power-down mode afterward where the power consumption is minimized in order to preserve the available battery capacity [2], [3]. It is therefore vital that the wake-up function does not consume excessive energy from the battery in order not to become the dominant energy consumer against the primary function of the device. Thus, ultralow-power operation is a major challenge in such applications. Usually, low-frequency oscillator circuits are employed in standby operation with a current consumption in the nanoampere range [4], [5].

Furthermore, the low-power design of battery-powered devices such as portable medical equipment is an important objective to reduce the system cost as an increased energy demand has to be covered by a higher battery capacity. Given the constraint of a fixed service time, a more expensive battery has to be selected for higher current requirements. Thus, it is essential to calculate the required energy for a guaranteed lifetime by considering the standby current and the averaged operating current. The latter is given by the implemented active-to-standby time duty cycle, whereas the accuracy of this duty cycle is determined by the wake-up oscillator frequency accuracy. In case of an excessive frequency variation, the battery capacity needs an extra margin to offset a potential early battery discharge. However, such a margin is undesirable because it results in higher system cost [6]. Typically, a frequency accuracy of 10% is acceptable to avoid this expensive margin while the required service time for a selected battery type is still ensured.

Recently, several publications have been made in the area of low-power precision oscillators due to an increasing demand of stable clock sources [7]–[9].

Ring oscillators exhibit excellent characteristics for ultralow-power operation when operated in the subthreshold region [10], but their accuracy and temperature drift are determined by the bias-current stability [11].

Crystal oscillators are superior frequency generators with excellent stability in respect of variations in supply voltage, temperature, and process. The feasibility of low-power operation in nanoscale technology has been reported in [12]. However, crystals are bulky devices and lead to excessive system cost. Consequently, alternative frequency reference schemes have been proposed, which make the external crystal redundant [13].

Relaxation oscillators are usually employed for low-power operation with a relatively good accuracy. Relaxation oscillators are preferred against crystal oscillators because the former do not require any external components and can be cheaply implemented in a CMOS technology. In addition, they draw less current than crystal oscillators at the cost of larger clock jitter. Fortunately, jitter is not an issue if the clock is used as a wake-up timing source only. As opposed to that of crystal oscillators, the absolute frequency accuracy of relaxation oscillators is restricted by the tolerances of on-chip capacitors and resistors that determine the time constant of the oscillator. Such tolerances are on the order of 40% but can easily be tightened by factory trimming.

A major drawback of relaxation oscillators is their susceptibility to temperature variations, whereas the operating temperature of portable medical measurement devices is typically 0 °C−70 °C. Assuming a maximum frequency tolerance of 3% after trimming at a single temperature, it is essential that the oscillator exhibits a temperature drift of less than 1000 $\mathrm{ppm}/^{\circ}\mathrm{C}$ in order to achieve an overall accuracy of 10% over the whole operating temperature range. Recently, an *RC* oscillator has been reported, which makes use of mixing polysilicon resistors with opposite temperature coefficients to achieve a superior temperature drift [14]. The utilization of electron mobility in a MOS transistor offers an alternative method to realize an accurate frequency reference without the requirement of a special process

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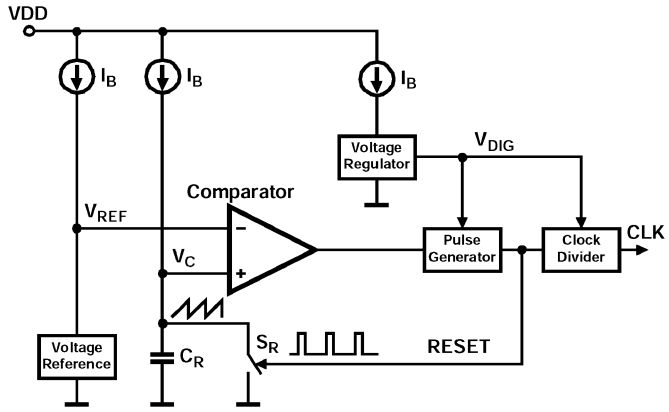

Fig. 1. System diagram of the proposed oscillator.

option. As opposed to polysilicon resistors, mobility is less subject to process variations and offers excellent frequency stability over temperature [15].

Most of the reported oscillators either require external components or consume excessive power [16], thus making them unsuitable for low-cost medical applications with long battery lifetime.

In this paper, an ultralow-power frequency generator that exploits electron mobility as a time reference is presented. The oscillator is capable of operating with a 1-V supply over a wide temperature range with low sensitivity to temperature and does not need any external components. Special attention was paid to an implementation in a standard CMOS process for low mass-production cost.

II. Circuit Description

A common oscillator structure comprises a capacitor that is charged by a constant current and is periodically discharged as soon as the capacitor voltage exceeds a certain voltage threshold [17], [18]. Previous implementations employ two comparators [8], while the proposed oscillator contains only one comparator to reduce the current consumption.

The system diagram of the low-power oscillator has been disclosed in [19], with the structure being shown in Fig. 1. It comprises a reference voltage generator that is supplied by bias current I_B and a time constant defining reference capacitor C_R. This capacitor is charged with a replica bias current I_B, and its voltage is compared against the reference voltage $V_{\rm REF}$ by means of a comparator. When the capacitor voltage exceeds the reference voltage, the output of the comparator goes high and triggers the digital control circuitry. Subsequently, a reset pulse is generated by a pulse generator in order to close switch S_R, which discharges the reference capacitor immediately. The reset pulse has to be sufficiently long to avoid a residual charge on the capacitor for the subsequent oscillator cycle.

A relaxation oscillator requires a simple digital circuit for controlling the charging/discharging cycle. The digital circuit that forms the pulse generator in Fig. 1 usually consists of an RS flip-flop and consumes a dynamic current that is proportional to the operating frequency, total load capacitance, and supply voltage. The latter can be reduced to below 1 V, which leads to a reduction of the dynamic current by a factor of three if the system is supplied by a 3-V battery. Thus, a voltage regulator is employed to produce a reduced digital supply voltage $V_{\rm DIG}$ for the digital circuitry.

A clock divider can optionally be implemented to generate a proper 50% duty cycle from the oscillator signal or to produce different polling intervals for sensor-based applications [4].

The oscillator period has the expression

$$T_{\rm OSC} = \frac{C_R \cdot (V_{\rm REF} + \Delta V)}{I_B} + t_P \tag{1}$$

where C_R, $V_{\rm REF}$, I_B, and t_p are the reference capacitor, reference voltage, bias current, and pulsewidth of the pulse generator, respectively. ΔV is the comparator overdrive voltage required to generate a high level at the comparator output. This term can be neglected if the comparator provides high gain (gain $\gg 20$). If the reference capacitor or bias current is made sufficiently large or small, respectively, the term t_P can be neglected as well because $T_{\rm OSC} \gg t_P$. Hence, the oscillator frequency can be approximated by

$$f_{\rm OSC} \approx \frac{I_B}{C_R \cdot V_{\rm REF}}. \tag{2}$$

This expression reveals the design strategy for a temperature-stable oscillator. The temperature characteristics of I_B can be chosen arbitrarily but needs to be matched with the temperature drift of $V_{\rm REF}$ or vice versa. In addition, I_B must be minimized for low-power operation. These design constraints for the bias source and reference voltage will be addressed in the following sections.

A. Bias-Current Generator

The bias source is the most important building block for the oscillator circuit because it defines the overall power consumption and temperature properties. Several schemes that enable low-power operation have been published [20], [23]. A resistorless variant has been disclosed in [24] and has been proposed for ultralow-power operation in [25], with the structure being shown in Fig. 2. The reported approximate PTAT characteristics make it well suitable for a low-temperature-drift oscillator, given that $V_{\rm REF}$ in (2) is realized as a proportional-to-ambient temperature (PTAT) voltage.

The bias generator in Fig. 2 consists of two pMOS transistors MP2 and MP3 that form a first current mirror with gain J. MN4 and MN3 form a second current mirror with gain N, where the voltage drop across MN1 can be neglected for low currents. These two loops are interconnected to a closed loop with a total current gain of $J \cdot N$. This loop gain is chosen > 1 such that the current in all branches increases. MN1 is operated in the triode region, acts as a high-impedance degeneration resistor, and causes the gain to reduce while the current increases. Equilibrium is achieved when the current gain is reduced to one. If MN3 and MN4 are operated in weak inversion with the same gate-bulk potential ($V_{\rm GB,MN3} = V_{\rm GB,MN4}$), bias voltage $V_{\rm B}$ is given by [20]

$$V_B = \phi_t \cdot \ln\left(\frac{S_{\rm MN3} S_{\rm MP3}}{S_{\rm MN4} S_{\rm MP2}}\right), \qquad \phi_t = \frac{kT}{q} \tag{3}$$

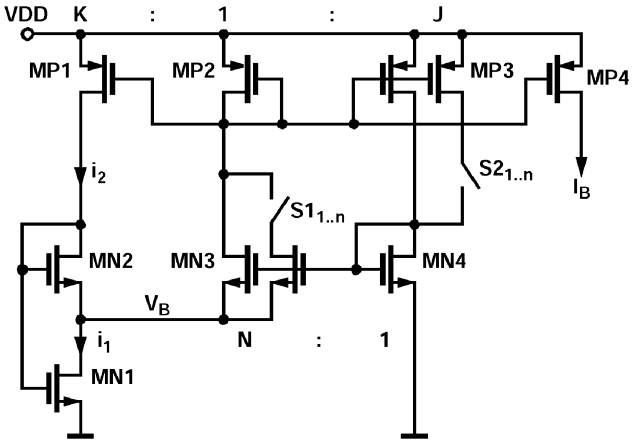

Fig. 2. Bias-current generator with adjustable current ratios.

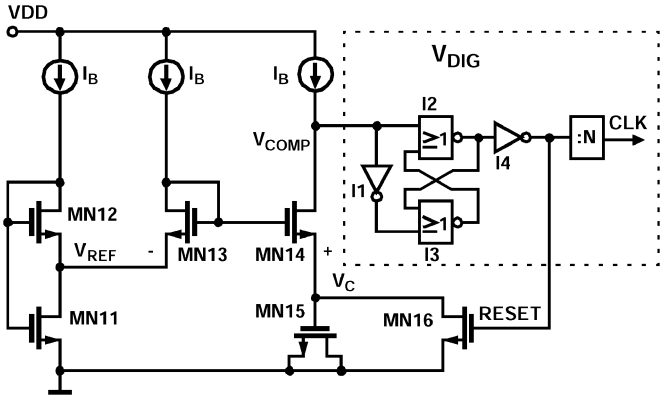

Fig. 3. Oscillator circuit with current-mode comparator.

where $S_{\mathrm{MNx/MPx}}$ denotes the W/L ratios of the respective transistors and ϕ_t is the thermal voltage.

MP1 and MP2 form an additional current mirror with gain K for biasing transistor MN2. By defining the specific current of MN1 with

$$I_S = S_{\mathrm{MN1}} \cdot \mu \cdot C'_{\mathrm{OX}} \cdot (2n) \cdot \phi_t^2 \tag{4}$$

where μ, C'_{OX}, and n are the effective mobility, gate capacitance per unit area, and slope factor, respectively, MN1 is forced to operate in the triode region with $K = 1$ and $S_{\mathrm{MN2}}/S_{\mathrm{MN1}} > 1$.

The bias-current generator has two operating points, namely, the desired state where a bias current I_B is provided, and the undesired state where all currents are zero. Although the circuit is self-starting if the leakage current of MN3 is higher than that of MN4, a start-up circuit (not shown) that does not consume a static current was included in the design for a defined start-up sequence. The circuit provides a supply independent bias current if the finite output resistances of the transistors are neglected. A detailed analysis using the advanced compact MOSFET (ACM) model can be found in [25], [26], where it is shown that the reference current can be written as

$$I_B = K_I \cdot I_S \tag{5}$$

with K_I being a scaling factor that has to be determined numerically for a given set of dimensions of MN1, MN2, K, and imposed bias voltage V_B. I_B can be made PTAT by controlling the inversion level of MN1, as further analyzed in Section III. With reference to (2), the PTAT property facilitates the implementation of a temperature-stable oscillator because a PTAT voltage generation for V_{REF} is straightforward.

B. Oscillator

The current consumption of a system is reduced by decreasing the number of current-conducting branches. Thus, the comparator in Fig. 1 has been implemented in current mode, as shown in Fig. 3. The input differential pair is formed by MN13 and MN14, which are biased by current I_B. The inverting input at the source of MN13 is connected to a reference voltage V_{REF}, while a MOS capacitor MN15 is connected to the noninverting input. This scheme shares the comparator current with the reference voltage generator and capacitor charging. Such a current-sharing scheme reduces the number of current-conducting branches and leads to a lower current consumption against previous relaxation oscillator implementations.

Transistor MN15 acts as a capacitor, and its voltage V_C is reset by MN16. After the reset is released, V_C increases steadily due to bias current I_B through MN14. As soon as V_C approaches reference voltage V_{REF}, MN14 is turning off and causes comparator output V_{COMP} to increase. This triggers the clock-form generator that consists of digital gates I1–I4. I2 and I3 build an RS flip-flop that is set by the comparator output and causes an immediate discharge of capacitor MN15 through switch MN16. As soon as the capacitor is discharged, the comparator output goes low and resets the flip-flop. This operation results in a sawtooth waveform across the capacitor and produces narrow clock pulses for the reset signal.

The given structure is beneficial to suppress the temperature-dependent trip point of the clock-form generator because the digital circuitry is triggered when the comparator is in equilibrium. This occurs when V_C rises to the V_{REF} level and causes V_{COMP} to be equal to the gate voltage of MN13. If the trip point of the digital gates is mainly determined by the nMOS threshold, any temperature effects inherently cancel out as the threshold voltage of MN13 tracks the digital trip point over temperature.

If MN11 and MN12 are operated in weak inversion, a PTAT voltage results for oscillator reference voltage V_{REF}. The transistors are operated at different current densities, whereas their respective V_{GS} difference is extracted. Because MN11 and MN12 are in a common well, they exhibit the same gate-bulk potentials, and hence, the slope factor does not appear in V_{REF}

$$V_{\mathrm{REF}} = \phi_t \cdot \ln\left(2 \cdot \frac{S_{\mathrm{MN12}}}{S_{\mathrm{MN11}}}\right). \tag{6}$$

If the reference capacitor is implemented as a MOS capacitor, its capacitance value can be written as follows:

$$C_R = K_C \cdot (W \cdot L)_{\mathrm{MN15}} \cdot C'_{\mathrm{OX}}. \tag{7}$$

K_C is a scaling factor that is one in strong inversion and decreases if MN15 is operated in weak inversion as the capacitance value is dominated by the depletion region capacitance in

the absence of an inversion layer [27]. K_C is defined in weak inversion as

$$K_C = \left(1 + \frac{4}{\gamma^2}(V_C - V_{\mathrm{FB}})\right)^{-\frac{1}{2}} \tag{8}$$

where γ, V_C, and V_{FB} are the body factor, capacitor voltage, and flat-band voltage, respectively. Using (2), (4)–(7) and defining

$$K_F = \frac{2}{\ln\left(2 \cdot \frac{S_{\mathrm{MN12}}}{S_{\mathrm{MN11}}}\right)} \cdot \frac{S_{\mathrm{MN1}}}{(W \cdot L)_{\mathrm{MN15}}} \tag{9}$$

the oscillator frequency can be written as

$$f_{\mathrm{OSC}} = \frac{K_I \cdot K_F}{K_C} \cdot n \cdot \mu \cdot \phi_t. \tag{10}$$

Employing a gate capacitance rather than a poly or metal capacitance for C_R in (2) features the advantage that a basic digital process without any additional process options can be used for low-production-cost purposes. Additionally, given that MN15 is operated in strong inversion $(K_C = 1)$, process-dependent parameter C'_{OX} cancels out in (2) for the reason that I_B is proportional to specific current I_S, as defined in (4). This results in an advantage against standard *RC* oscillators that suffer from the spread of both reference resistor and capacitor. From (10), it is obvious that the oscillator's frequency process dependence is simply determined by the accuracy of effective mobility μ and slope factor n. Additional errors arise from transistor mismatch, as seen in (9), and offset of the differential pair MN13/MN14.

Expression (10) emphasizes that the absolute frequency is only dependent on well-controlled process parameters. Thus, this oscillator structure offers opportunities for applications where a good accuracy without calibration is of interest. A low K_C value implies a low reference voltage and was chosen to be 0.27 for the experimental implementation in order to limit the capacitor voltage swing and, hence, current consumption. In addition, the voltage dependence of C_R is almost negligible in this operation mode according to (8) and is discussed further in Section III for the temperature-drift analysis.

C. Voltage Regulator

All digital gates shown in Fig. 3 are operated on a reduced supply voltage that is generated with a voltage regulator, as shown in Fig. 4. The regulator scheme is based on a known structure where a replica gate formed by MP21 and MN21 is biased with a bias current [28]. The voltage across the replica gate is buffered with an operational transconductance amplifier (OTA) and generates the reduced digital supply. A solution with a fixed bias current would restrict the operating frequency to a certain upper limit unless excessive current is spent for the biasing. However, such an oversized current leads to an unnecessary current consumption at low operating frequencies. Hence, an adaptive biasing scheme accommodates the increased digital current demand at higher operating frequencies by boosting the tail current of the OTA while maintaining a low current at low frequencies. The detailed schematic of the OTA is shown

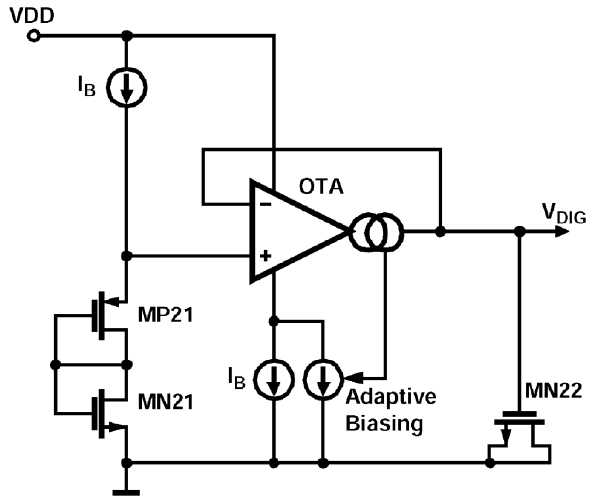

Fig. 4. Voltage regulator for the provision of a reduced digital supply voltage.

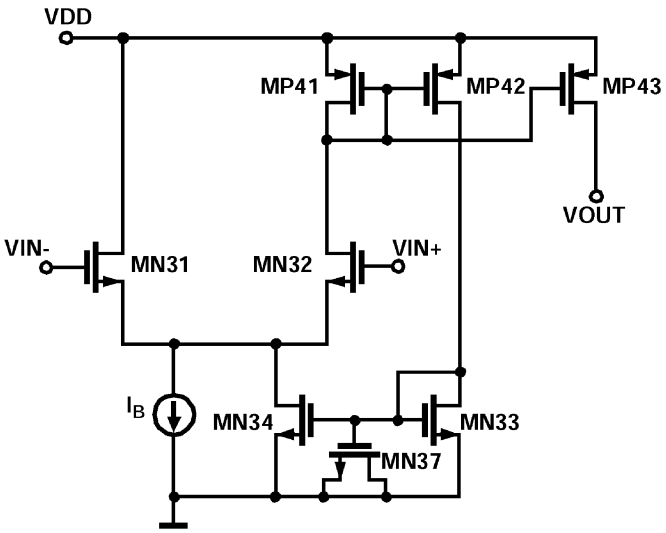

Fig. 5. OTA with adaptive biasing for the voltage regulator.

in Fig. 5. It consists of a standard OTA with an additional current loop that comprises transistors MP41, MP42, MN33, and MN34. This loop boosts the tail current upon a rise in load current. MN37 acts as a capacitor for loop-stabilization purposes.

The current consumption of the implemented voltage regulator is defined with four unit currents I_B's of the current source. Hence, assuming that $I_B = 750$ pA, the regulator accounts for 3-nA supply current. The dynamic-current consumption of the digital circuitry is defined with

$$I_{\mathrm{VDIG}} = f_{\mathrm{OSC}} \cdot V_{\mathrm{DD}} \cdot C_{\mathrm{LOAD}}. \tag{11}$$

V_{DD} is the digital operating voltage, and C_{LOAD} is the total load capacitance of the digital circuit including layout parasitics. If the oscillator frequency is chosen to be 3.5 kHz and $C_{\mathrm{LOAD}} = 0.8$ pF, the digital current consumption would account for 8.4 nA with a 3-V supply. The consumption is even higher in practical circuits due to cross-currents in the logic gates during a transition. By employing a voltage regulator and

TABLE I
CURRENT CONSUMPTION WITH $I_B = 750$ pA

	Current Consumption (nA)
Bias Source	3.75
Oscillator	2.25
Voltage Regulator	3.0
Digital Circuitry	0.4
Total	9.4

reducing the digital supply to typically $V_{\mathrm{DIG}} = 0.8$ V, the digital-circuit consumption is reduced to 3.4 nA including the regulator current. This gives a significant benefit at high supply voltages against a solution without a voltage regulator.

The overall current budget of the oscillator is summarized in Table I, where the current contributions by the different blocks are given with $I_B = 750$ pA.

III. TEMPERATURE DRIFT

One of the main process parameters that are responsible for the oscillator temperature drift is the effective mobility, which is known to decrease with temperature [27]. An often-used approximation is

$$\mu(T) = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{-m} \tag{12}$$

where μ_0 is the mobility at reference temperature T_0 and m is the process-dependent mobility exponent.

In consideration of (2), it has already been pointed out that the oscillator frequency becomes independent from temperature if a PTAT characteristic of V_{REF} is offset by a PTAT bias current I_B, given that the reference capacitor is independent from temperature. An almost PTAT characteristic of the bias-current generator results if the process-dependent effective-mobility temperature exponent m is close to one [26]. Numbers in the range of 1.2–2 have been reported in [29], where m becomes approximately 1.2 when the doping concentration increases above 10^{17} cm^{-3}, which applies for the selected 0.35-μm CMOS process. From (10), it can be derived that a negative temperature drift of the oscillator frequency results with $m > 1.0$ under the assumption that the slope factor in (4) remains constant. This is applicable if MN1 is operated in weak inversion, where the slope factor remains nearly stable as the surface potential of MN1 changes almost proportionally to $\mathrm{VGB}_{\mathrm{MN1}}$.

However, if MN1 is operated in or close to moderate inversion, its slope factor changes with temperature due to the threshold-voltage (VT) temperature dependence that effects a nonconstant gate-bulk potential $(V_{\mathrm{GB,MN1}})$ over temperature. The negative temperature drift of $\mathrm{VT}_{\mathrm{MN1}}$ causes the slope factor to increase with temperature as $V_{\mathrm{GB,MN1}}$ drops roughly with the same rate as $\mathrm{VT}_{\mathrm{MN1}}$. Although the slope factor itself is only a weak function of temperature, the variation over temperature affected by a negative temperature drift of $V_{\mathrm{GB,MN1}}$ can be modeled with a slope factor n_0 defined at temperature T_0 and a respective temperature exponent mn

$$n(T) = n\left(V_{\mathrm{GB,MN1}}(T)\right) = n_0 \cdot \left(\frac{T}{T_0}\right)^{mn}. \tag{13}$$

Temperature exponent mn has its maximum value in moderate inversion, while a higher inversion level of MN1 causes mn to drop because the surface potential becomes almost pinned to a constant value in strong inversion. Because the inversion level of MN1 is determined by current loop gain $J \cdot N$, as shown in Fig. 2, temperature exponent mn can be altered with different bias-current settings. A higher loop gain causes an increase of both PTAT voltage V_B and bias current I_B and, hence, a higher inversion level that results in a lower value of mn.

Using (4), (5), (12), and (13), the bias current can be written with $\phi_t = \phi_{t0} \cdot T/T_0$ as

$$I_B(T) = K_I \cdot I_{S0} \cdot \left(\frac{T}{T_0}\right)^{2-m+mn} = I_{B0} \cdot \left(\frac{T}{T_0}\right)^{mi} \tag{14}$$

where I_{S0} and I_{B0} are the specific and bias currents at reference temperature T_0, respectively. The contributors to the temperature drift are summed up in temperature exponent mi. A temperature-sweep simulation of the bias-current generator with $J \cdot N = 4$ resulted in $mi = 1.34$, while $mi = 0.5$ was obtained with a loop gain of 30. Consequently, an appropriate selection of the loop gain gives rise to an almost-perfect PTAT bias current when $mi = 1$. This permits an implementation of a virtually temperature-independent frequency generation without the requirement of a dedicated temperature compensation scheme.

Expression (8) shows that the capacitance value is dependent on the reference voltage and therefore decreases with temperature because V_{REF} is PTAT. In addition, the effective surface carrier concentration decreases at low temperatures, which causes a negative temperature drift of the gate capacitance [21], [22]. These effects can be combined by expressing scaling factor K_C as a function of temperature with K_{C0} at temperature T_0

$$K_C(T) = K_{C0} \cdot \left(\frac{T}{T_0}\right)^{mc}. \tag{15}$$

Temperature exponent mc is approximately -0.2 for the given circuit configuration and is therefore only a minor error source for the oscillator temperature drift.

By using (10), (14), and (15), the oscillator frequency can be rewritten as

$$f_{\mathrm{OSC}}(T) = \frac{K_F \cdot K_I}{K_{C0}} \cdot \mu_0 \cdot n_0 \cdot \phi_{t0} \cdot \left(\frac{T}{T_0}\right)^{mi-mc-1}. \tag{16}$$

The oscillator frequency temperature coefficient tc_{OSC} at reference temperature T_0 normalized to $f_{\mathrm{OSC}}(T_0)$ is obtained from (16) as follows:

$$tc_{\mathrm{OSC}} = \left.\frac{\partial f_{\mathrm{OSC}}}{\partial T}\right|_{T=T_0} / f_{\mathrm{OSC}}(T_0) = \frac{mi - mc - 1}{T_0}. \tag{17}$$

TABLE II
KEY ELEMENT DESIGN PARAMETERS

MN1 (W/L [μm])	2/1000
MN2	2/800
MN4	8/6
J/K/N Ratio	1…2.5/1/4...12
MN11	4/32
MN12	4/4
MN15	10/180
Bias Current I_B	0.15 … 2.5nA

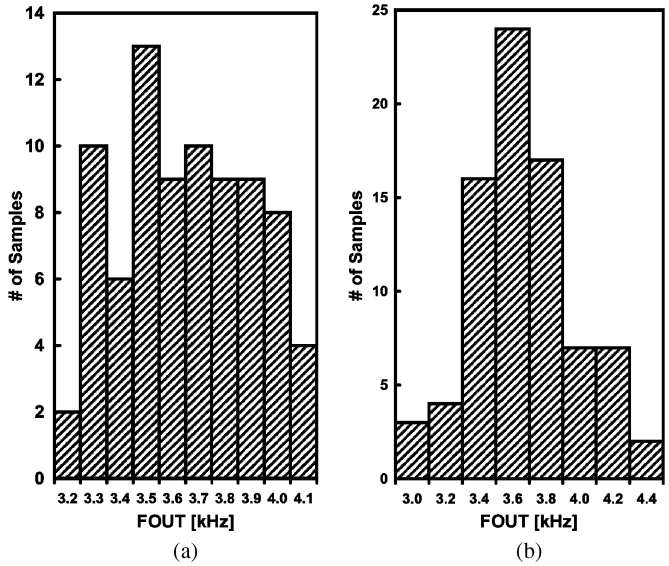

Fig. 6. Histogram of the oscillator frequency for 80 Monte Carlo runs with (a) process variation simulation and (b) device mismatch simulation.

Using $mi = 0.5$ to 1.34, $mc = -0.2$, and $T_0 = 300$ K, the predicted oscillator temperature coefficient can be varied from $+1835$ to -973 ppm/°C by changing the bias-current loop gain, whereas the temperature drift becomes negative with a higher loop gain.

IV. TEST STRUCTURE AND EXPERIMENTAL RESULTS

A. Design

A test chip has been designed and fabricated in austriamicrosystems' 0.35-μm CMOS technology, with the design parameters being summarized in Table II.

With a nominal bias-current setting of 750 pA ($J = 1$, $K = 1$, and $N = 10$), the oscillator frequency was calculated using (2) with $C_R = 2$ pF and resulted in a nominal oscillator frequency of 3.5 kHz. In order to evaluate the sensitivity to mismatch and process variations, a Monte Carlo simulation was performed, where the respective results are shown in Fig. 6. The simulation results show a mean frequency of 3.7 kHz and standard deviations of 6.9% for process variations and 8.5% for mismatch errors, respectively. Obviously, mismatch errors dominate against process variations due to weak-inversion operation where matching is significantly degraded.

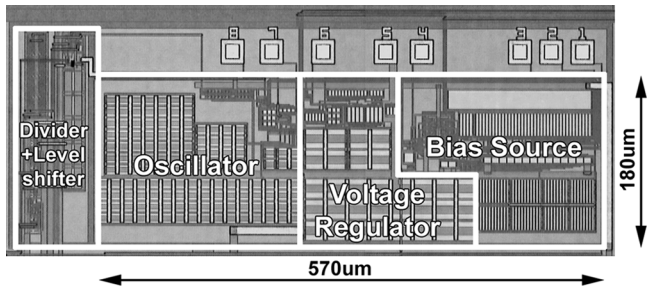

Fig. 7. Oscillator cell photograph.

B. Implementation

A photograph of the cell is shown in Fig. 7. The oscillator core area is 0.1 mm^2 and includes a large decoupling capacitor for the internally generated digital supply. A frequency divider consisting of standard T flip-flops was included for test purposes.

The fabricated test chip additionally houses a digital noise block to evaluate the robustness of the oscillator against substrate noise. Some 156 individually selectable digital blocks, comprising 80 digital gates each, can be clocked with an external clock signal to generate substrate noise.

Fig. 8(a) shows the structure of a digital noise logic unit (NLU). An NLU consists of sequential and combinatorial logic to emulate the behavior of a finite-state machine with 80 equivalent gates. The block is enabled by a memory cell that connects the global clock signal to the local clock buffer. The memory cells are connected in series and build up a 156-bit shift register, which can externally be written. Consequently, the noise logic can be configured to emulate a finite-state machine up to 12 480 active gates in steps of 80 gates.

The digital noise block was placed around the oscillator cell to emulate a mixed-signal system, as shown in Fig. 8(b). Because an n-well process was used, both the oscillator cell and digital noise block are surrounded by a p+ guard ring connected to a dedicated VSS pad to reduce crosstalk [31].

C. Measurement Results

The oscillator was measured with a supply voltage from 0.9 to 3.6 V. A stable frequency is provided above 1.0 V, as shown in Fig. 9. A significant increase of the oscillator frequency is observed at voltages above 3.0 V, which is caused by hot-carrier degradation (impact ionization) [27]. An improved performance could be obtained by limiting the drain–source voltages with cascoding at the cost of a higher minimum supply voltage. The line sensitivity was measured to be 3.5% in the supply voltage range of 1.0–2.5 V.

Fig. 10 shows the oscillator current consumption over the temperature range of -20 °C$to80$ °C with $I_B = 1$ nA at room temperature. The current consumption was measured with a Keithley Picoammeter KE 487 and includes the consumption of the bias source, oscillator, and voltage regulator with the associated digital circuitry. The supply current rises almost linearly with temperature due to the nearly PTAT characteristic of the bias current [26]. At high temperatures, the current

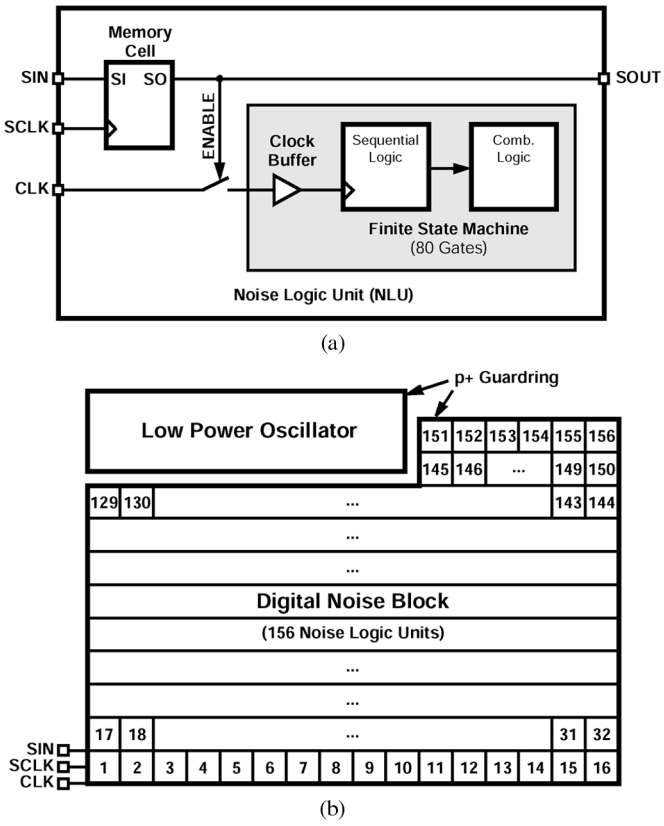

Fig. 8. (a) NLU. (b) Digital noise logic.

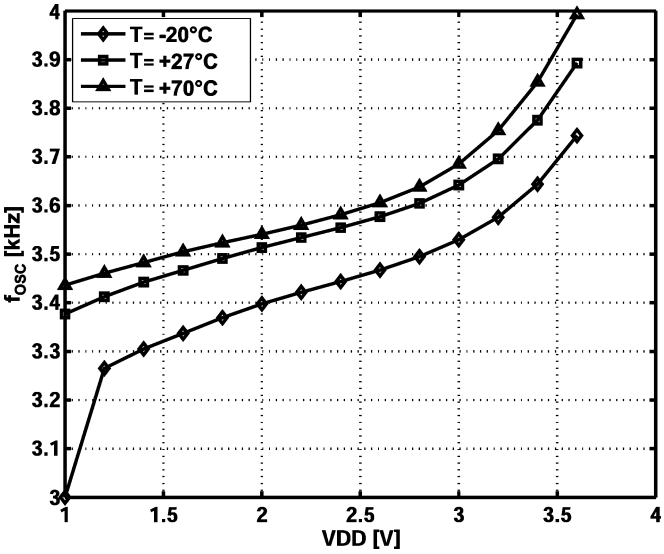

Fig. 9. Oscillator line sensitivity at different operating temperatures.

increases exponentially as a result of the leakage currents of the electrostatic-discharge protection devices.

In addition, the oscillator was measured with eight different bias configurations ($J \cdot N = 4/6/8/10/12/18/24/30$) with a 1.0-V supply. The lowest bias configuration provided a 158-Hz clock signal at a power consumption of 0.3 nW. This results in a figure of merit (FOM) of 1.9 nW/kHz, which is significantly lower than the previously reported results. The output frequency

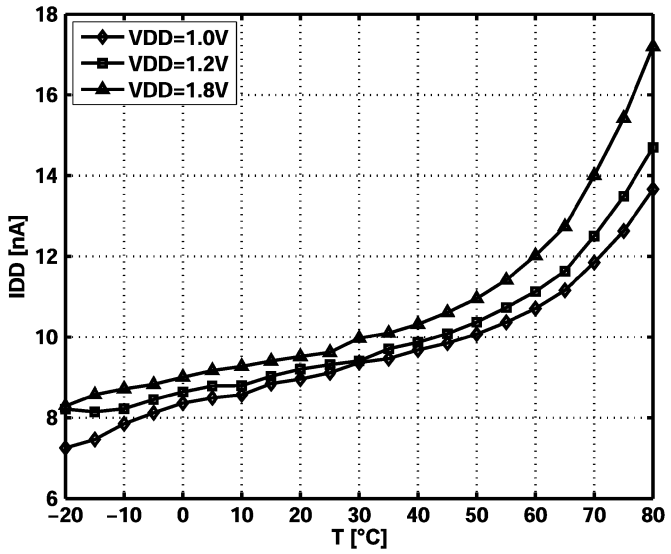

Fig. 10. Oscillator current consumption with $I_B = 1$ nA.

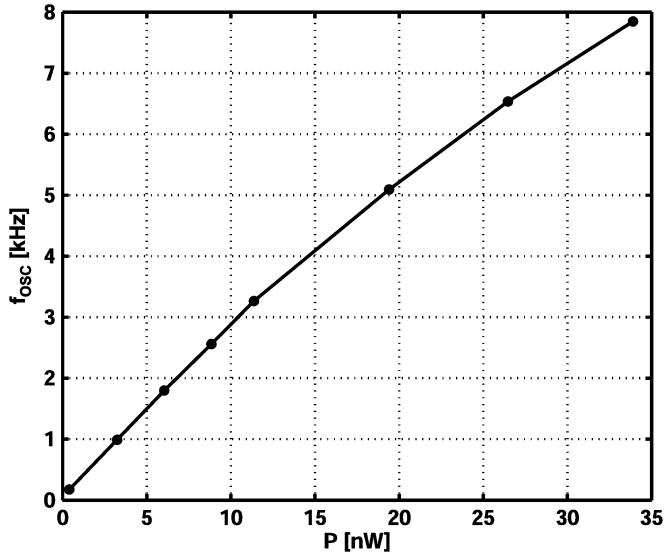

Fig. 11. Output frequency in respect of the power consumption. A FOM of 1.9 nW/kHz is achieved with $I_B = 150$ pA.

in respect of the power consumption is shown in Fig. 11. The power consumption increases to 33 nW with the maximum configurable bias current ($I_B = 2.5$ nA) and provides a 7.8-kHz clock. At this operation point, the FOM has increased to 4.2 nW/kHz, which is attributable to the higher dynamic current demand of the digital circuit.

A temperature evaluation was performed in the temperature range of $-20\,^{\circ}$Cto $80\,^{\circ}$C with six different bias-current settings ($J \cdot N = 8/10/12/18/24/30$) ranging from 500 pA to 2.5 nA at room temperature. The temperature drift of the normalized frequency is shown in Fig. 12. Values between -370 ppm/°C (with $I_B = 2.5$ nA) and $+685$ ppm/°C (with $I_B = 0.5$ nA) were measured, whereas the temperature drift is positive for a low current loop gain and becomes negative with higher current loop gains, as predicted in (17). The transition point between the positive and negative temperature drifts occurs at gains of

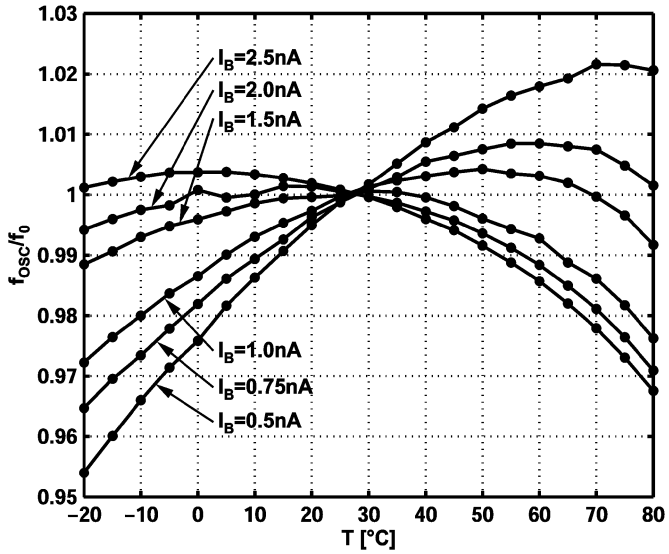

Fig. 12. Oscillator temperature drift with different bias-current configurations. Oscillator frequency f_{OSC} is normalized to reference frequency f_0 at room temperature.

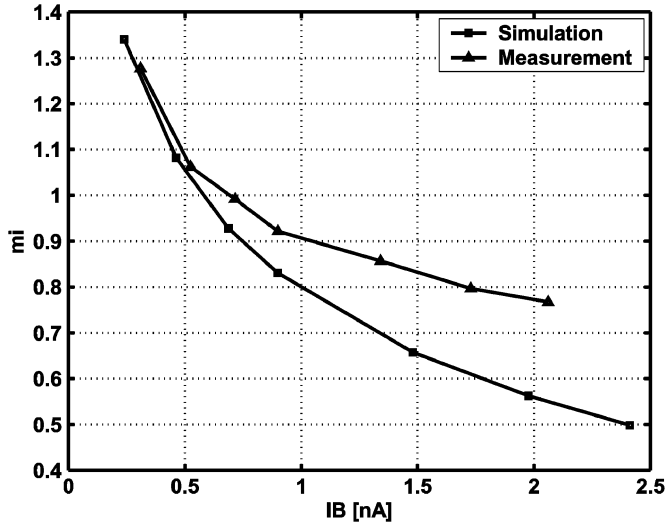

Fig. 13. Bias-current temperature exponent.

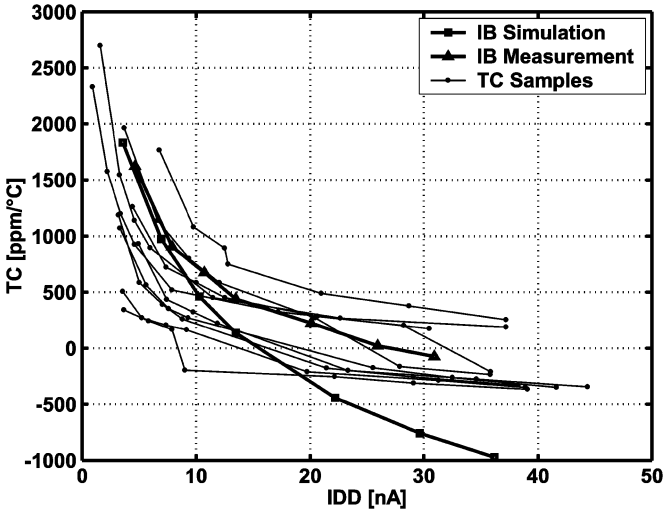

Fig. 14. Predicted temperature coefficient with both simulated and measured bias currents in comparison with ten measured samples. The samples were evaluated over temperature with different bias-current settings.

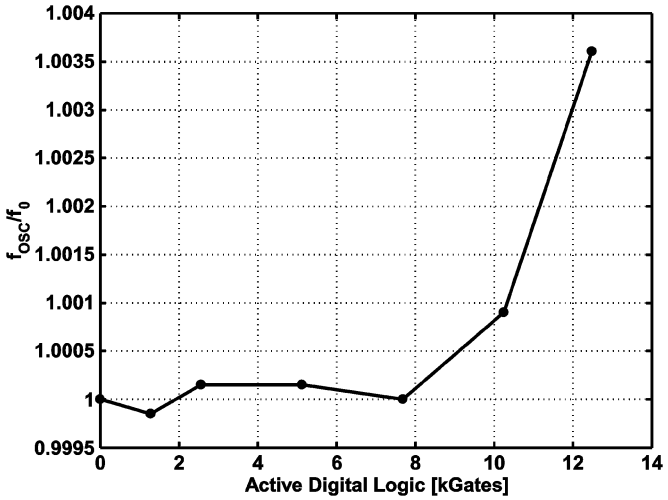

Fig. 15. Oscillator nominal frequency deviation with $I_B = 150$ pA in respect of the number of active gates.

$J \cdot N = 12$ and 18, while the simulated transition takes place at $J \cdot N > 12$.

The loop-gain-dependent temperature exponent mi in (14) was evaluated by measuring bias current I_B over temperature with $J \cdot N = 6/8/10/12/18/24/30$. A comparison with the simulated values is made in Fig. 13. It is noticable that an almost-perfect PTAT characteristic results with $I_B = 700$ pA ($J \cdot N = 10$). Additionally, it is visible that the simulation overestimates the slope factor variation at higher inversion levels due to the model accuracy limitations in the triode range.

A temperature-drift evaluation of the oscillator frequency was performed with ten samples with $J \cdot N = 6/8/10/12/18/24/30$. The extracted temperature coefficient is shown in Fig. 14 and compared with the predicted value according to (17). An additional comparison was made by evaluating (17) with the measured temperature exponent mi of I_B. It is apparent that the simulation slightly overvalues the temperature drift at higher bias currents, while the evaluation with the measured temperature exponent mi predicts more accurate values for the temperature coefficient. The transition point between the positive and negative temperature coefficients occurs at an approximate loop gain of $J \cdot N = 24$. This configuration offsets the minor error produced by a nonideal reference capacitor C_R, as shown in (15).

It is evident that a temperature coefficient of < 500 ppm/°C is achievable with a minimum supply current of 20 nA. A calibration of the temperature drift by means of varying $J \cdot N$ to control the inversion level of MN1 would result in a performance of better than 260 ppm/°C according to the measurements.

Robustness against substrate noise was evaluated with an external 20-MHz clock signal and a 1.8-V supply for the digital noise block. The measured substrate-noise voltage increases virtually linearly with the number of active gates and achieves 40 $\mathrm{mV_{rms}}$ with 12 500 active gates. This result corresponds with the measurements reported in [32]. The oscillator was

TABLE III
COMPARISON WITH OTHER REPORTED OSCILLATORS

Ref.	Tech.	Min. Supply (V)	Freq. (kHz)	Power (μW)	Line Sens. (%/V)	TC (ppm/°C)	Rel. Acc. 3σ (%)	FOM (nW/kHz)	Area (mm^2)	Notes
This work	0.35μm CMOS	1.0	3.3	0.011	3.5	>1000 <500 (<260)	20.7	1.9 4.0	0.1	J N=4 J N=18 (calibrated)
De Smedt et al. [14]	65nm CMOS	1.2	6000	66	N/A	86	0.9	11	0.03	Dual poly TC compensation
De Vita et al. [8]	0.35μm CMOS	1.0	80	1.06	-2.5	842	11.9	13.3	0.24	Simulation only
Bala and Nandy [7]	0.18μm CMOS	1.25	6000	938	N/A	N/A	4	156	0.14	External RC
Hwang et al. [16]	2 μm CMOS	2.0	0.1	0.3	N/A	N/A	N/A	170	0.281	
Sebastiano et al. [15]	65nm CMOS	1.05	100	41	0.1	5200 (100)	7 (<1.1)	410	0.11	Uncalibrated (calibrated)
Lasanen and Kostamovaara [9]	0.35μm CMOS	1.2	200	84	0.14	900	0.7	420	0.077	External RC

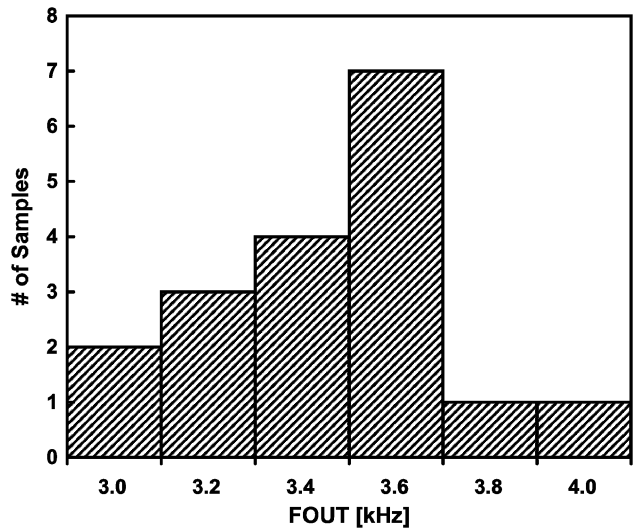

Fig. 16. Histogram of the measured oscillator frequency for 18 samples.

configured with the lowest possible bias current of 150 pA at room temperature, which resulted in a consumption of less than 1 nW, while the digital power consumption was approximately 20 mW. Fig. 15 shows the normalized oscillator frequency in respect of the number of active gates. A slight frequency increase is observed with more than 10 000 active gates, and the output frequency increases by 0.36% with the maximum configuration of 12 500 active gates. Substrate noise causes a common-mode error only for the given oscillator configuration because all relevant reference nodes are referenced to ground. This makes this oscillator arrangement robust against digital crosstalk, as any ground bouncing is suppressed by the power-supply rejection performance.

A summary of the measured oscillator parameters in comparison with previous work is given in Table III. This oscillator exhibits the lowest power-to-frequency ratio, whereas an FOM of 1.9 nW/kHz is achieved with $J \cdot N = 4$. The frequency accuracy that is shown in Fig. 16 for 18 samples is slightly worse than that of previous work but can be improved by factory trimming. A temperature drift of < 500 ppm/°C is obtained by choosing $J \cdot N = 18$. Thus, assuming a trimming accuracy of 2%, the oscillator achieves an absolute accuracy of 5.5% within the temperature range of 0°C−70 °C at a FOM of 4.0 nW/kHz.

V. CONCLUSION

A novel oscillator scheme that utilizes electron mobility as a time reference and current sharing for power consumption reduction has been presented. Experimental results show that the oscillator is capable of operating with less than 1 nW at room temperature and is robust against digital crosstalk. It has been shown that the structure operates over a wide temperature range with a minimum supply of 1.0 V without using external components. The realization in a standard CMOS process permits an economical implementation for low-cost products and has the potential for many mixed-signal applications demanding low power and low temperature drift.

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