CMOS Comparators

Course *Integrated Circuit Design*, 2009

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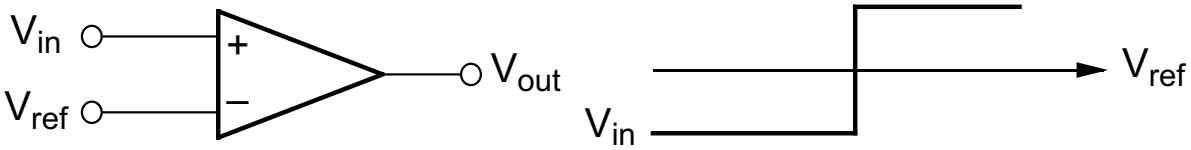
Outline

Introduction

Definitions

- A comparator detects whether its input is larger or smaller than a reference voltage



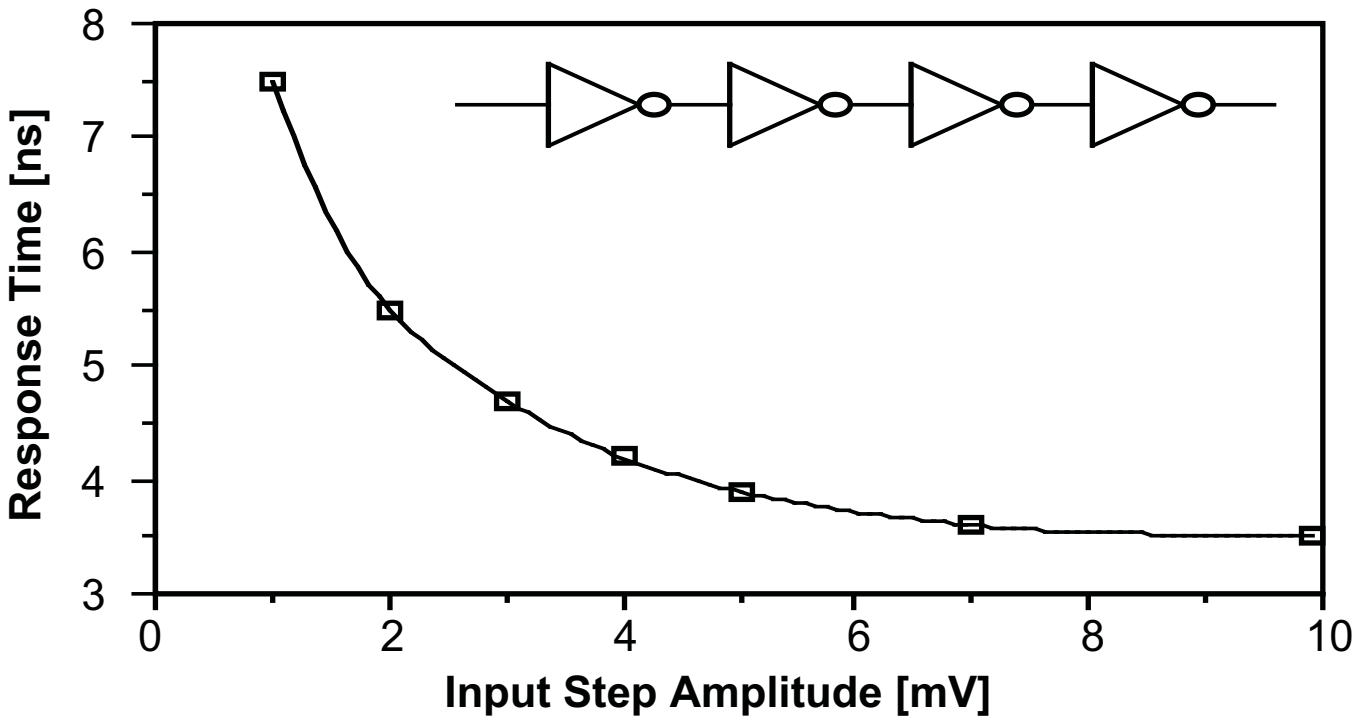
- The output of a comparator a digital signal (“1” or “0” level)
- Overdrive ➜ If the input of the comparator is driven with a voltage larger than the minimum voltage required to achieve the correct digital level, the comparator is overdriven

Use of comparators

- Threshold detector
- Zero-crossing detector
- High immunity noise digital line receiver

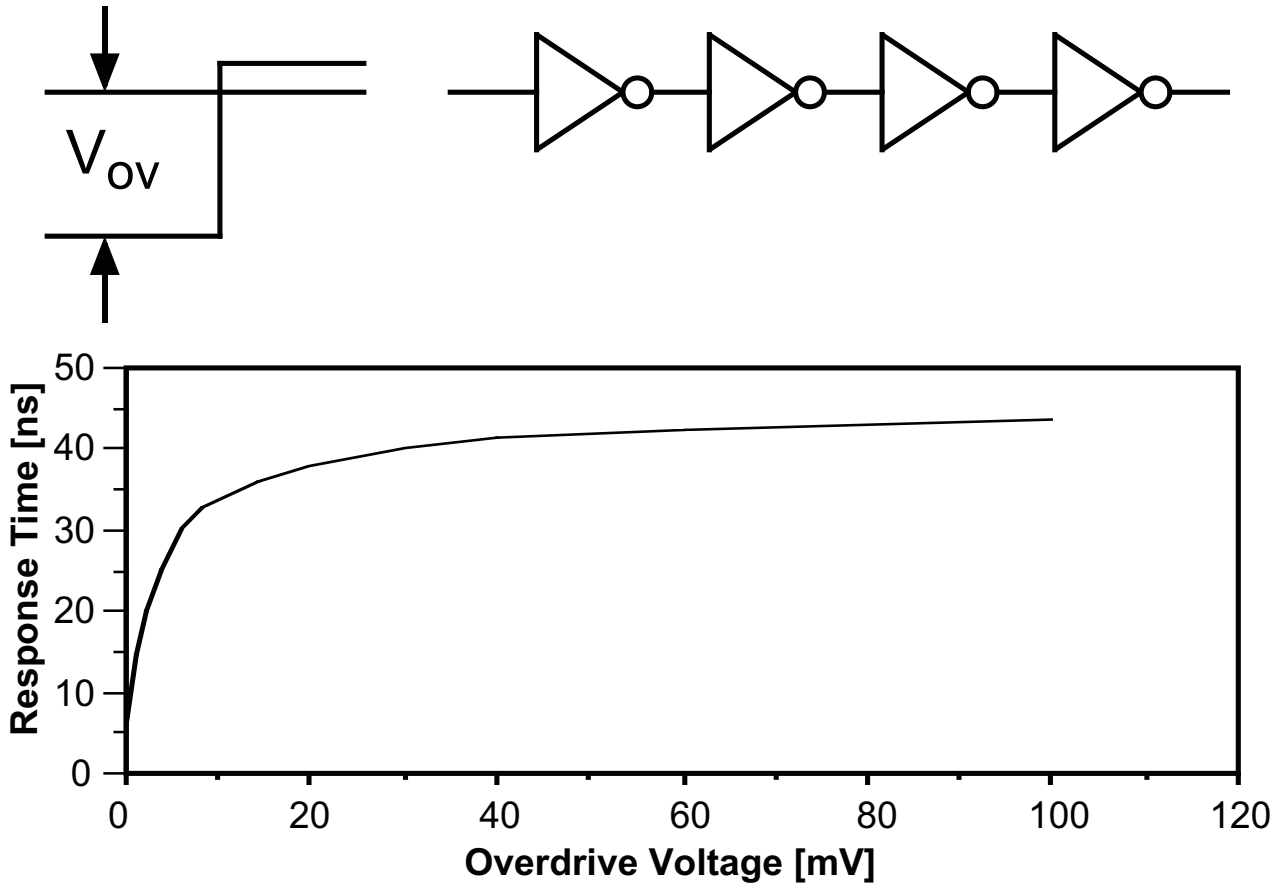
Performance characteristics

- Voltage gain (A_v) ➜ Differential DC gain of a comparator
- Input offset (V_{os}) ➜ Voltage that must be applied to the input to obtain a transition between the low and the high state
- Response time (t_r) ➜ Time interval between the instant when a step input is applied and the instant when the output reaches the corresponding logic level (depends on the input step amplitude)



Performance characteristics

- Overdrive recovery ➜ Time interval required to recover from overdrive (the response time, for a given input step amplitude, depends on how much the comparator was previously overdriven)



Performance characteristics

- Latching capability ➜ A latch command and an unlatch command store and release the output logic state
- Power supply rejection ratio (*PSRR*) ➜ Transfer function between the supply rails and the output of the comparator
- Power consumption ➜ Power dissipated at DC (static) and during comparisons (dynamic)
- Hysteresis ➜ The threshold voltage for rising input signals is different from the threshold voltage for falling input signals

Comparator Gain and Response Time

Basic considerations

- A comparator is basically an open loop gain stage
- Any gain stage can be used as comparator, from a simple inverter to a complex operational amplifier
- If required a latch can be connected at the output of the gain stage

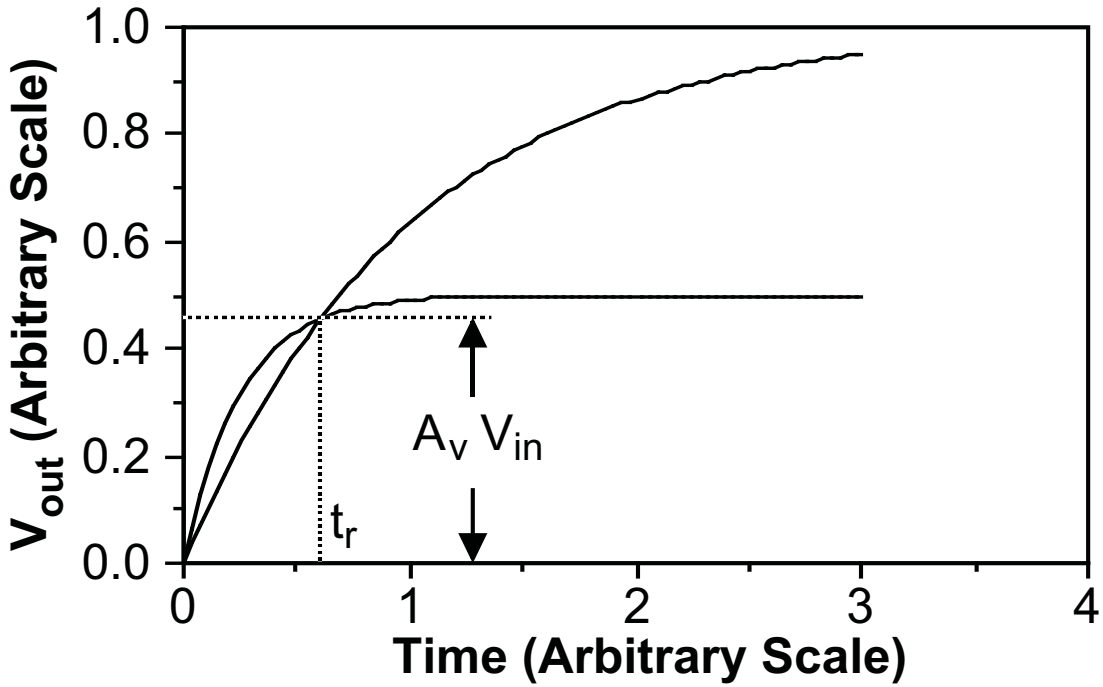
Key issues in comparator design

- Gain obtained by using a single complex stage or by using a cascade of simple stages (stability is not an issue)
- Offset cancellation
- Power supply rejection
- Overdrive recovery
- Power consumption

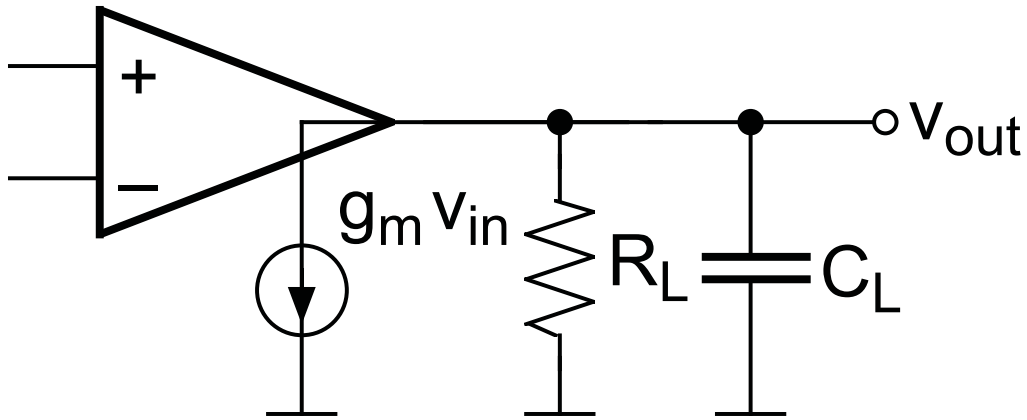
Comparator Gain and Response Time

Comparator gain vs bandwidth trade-off

- Due to the finite bandwidth of the circuit V_{out} reaches $A_v V_{in}$ with a delay with respect to the input step (response time t_r)
- The same values of V_{out} and t_r are obtained by using stages with different bandwidths and DC gains



Comparator Gain and Response Time



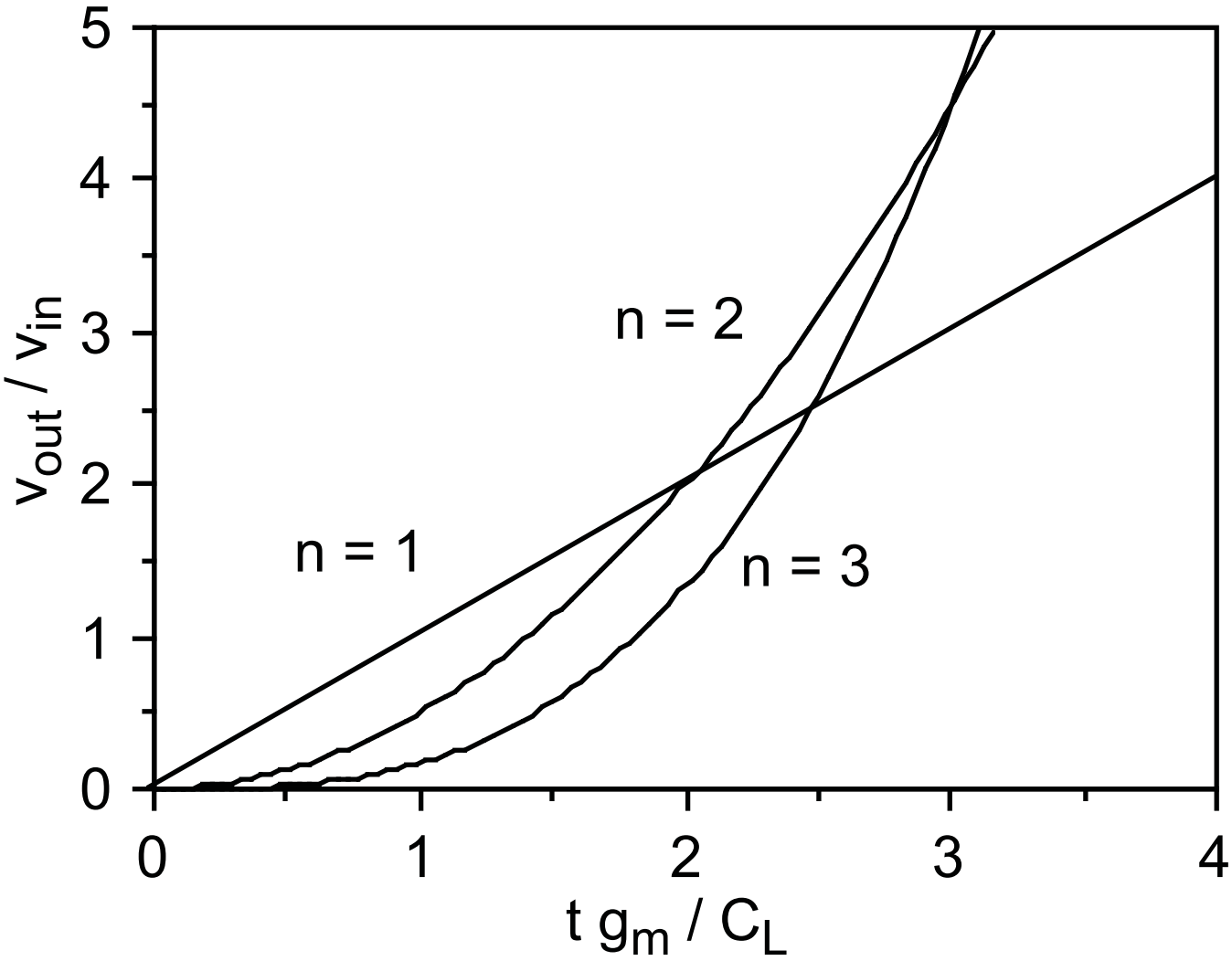
- Single-stage comparator

$$t \ll \tau = R_L C_L \Longrightarrow v_{out} = g_m R_L v_{in} \left(1 - e^{-\frac{t}{\tau}}\right) \cong v_{in} \frac{g_m}{C_L} t$$

- Multi-stage comparator (n stages)

$$t \ll \tau = R_L C_L \Longrightarrow v_{out} \cong v_{in} \left(\frac{g_m}{C_L}\right)^n \frac{t^n}{n!}$$

Comparator Gain and Response Time



Comparator Gain and Response Time

- For a given gain, it exists an optimum number of stages which gives the best response time

$$A_{v,n} = \frac{(n+1)^n}{n!} \Longrightarrow t_{r,n} = (n+1)\,\frac{g_m}{C_L}$$

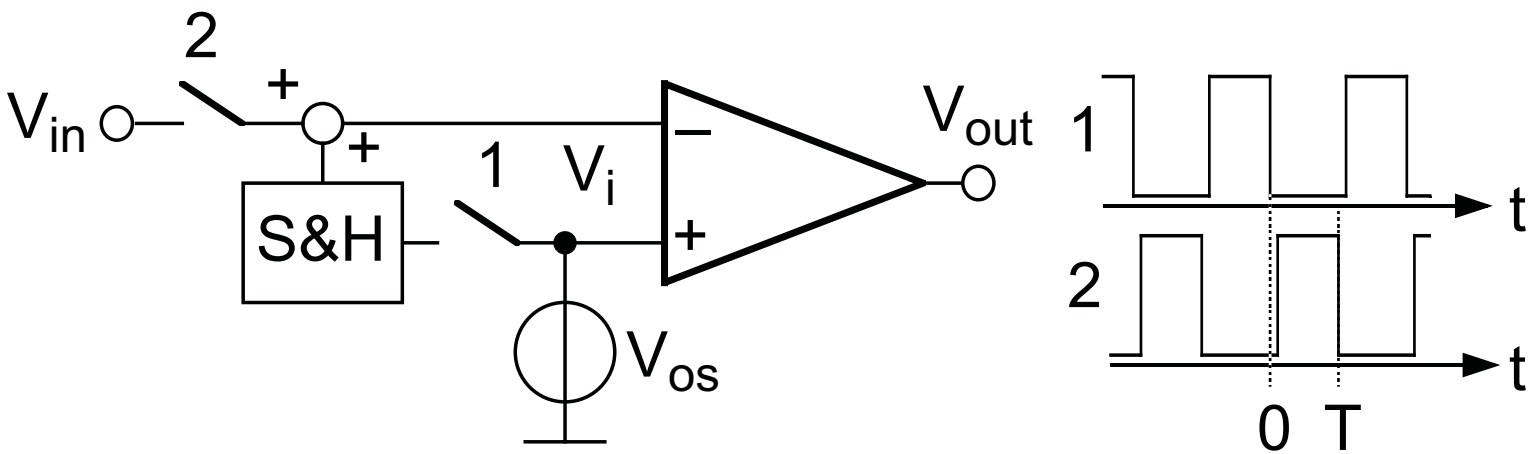
- For a small gain we achieve a smaller response time with a single stage than with several stages
- For a large gain we achieve a smaller response time with several stages than with a single stage

n	1	2	3	4	5	6	7	8	9
$A_{v,n}$	2	4.5	10.6	26	64.8	163	416	1067	2755

Offset Cancellation Techniques

Autozero technique

- Basic idea ➜ Sample the offset during one clock phase and subtract it from the signal during the other clock phase
- Two non-overlapping clock phases are required
  - Phase 1 ➜ Autozero
  - Phase 2 ➜ Comparison



Offset Cancellation Techniques

- Time-domain analysis

$$V_i(T) = V_+(T) - V_-(T) = V_{os}(T) - [V_{in}(T) + V_{os}(0)]$$

- If V_{os} varies slowly with respect to T, then $V_{os}(T) \cong V_{os}(0)$

$$V_i(T) \cong -V_{in}(T)$$

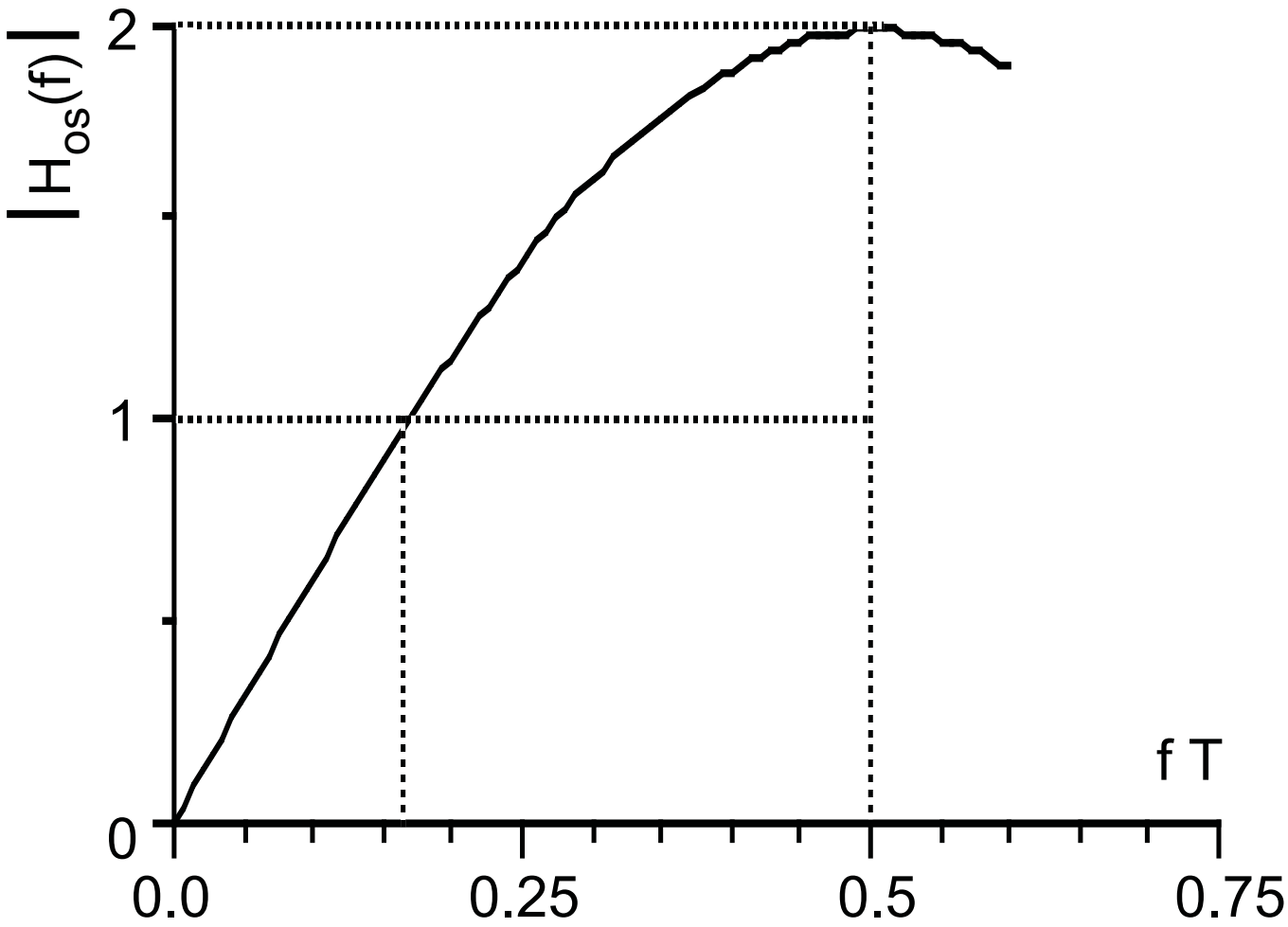
- Frequency-domain analysis (Laplace transform)

$$V_i(s) = V_{in}(s) + V_{os}(s)\left(1 - e^{-sT}\right)$$

$$H_{os}(s) = 1 - e^{-sT} = 2je^{-\frac{sT}{2}} \sin\left(\frac{sT}{2}\right)$$

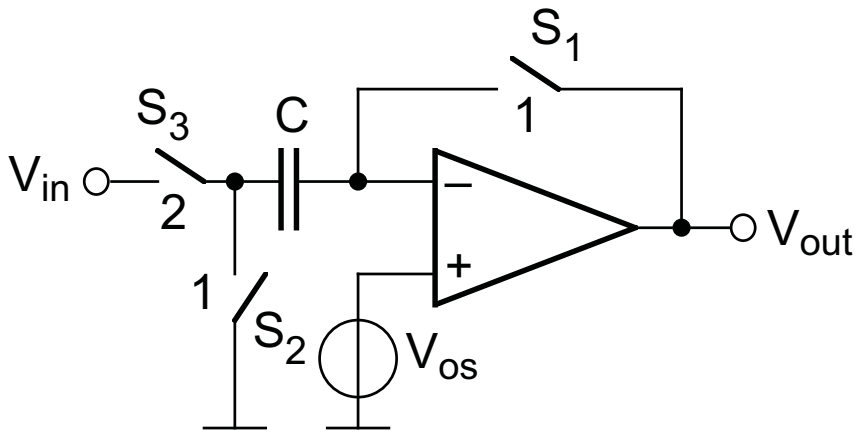
- The low frequency components of V_{os} are canceled

Offset Cancellation Techniques



Offset Cancellation Techniques

Autozero in single-stage comparators



- During phase 1 the gain stage is in unity-gain closed-loop configuration and V_{os} is sampled on capacitor C
- During phase 2 the gain stage is in open-loop configuration and the offset-free comparison is performed
- Capacitor C represents an output load of the gain stage during phase 1
- Stability of the gain stage during phase 1 has to be considered

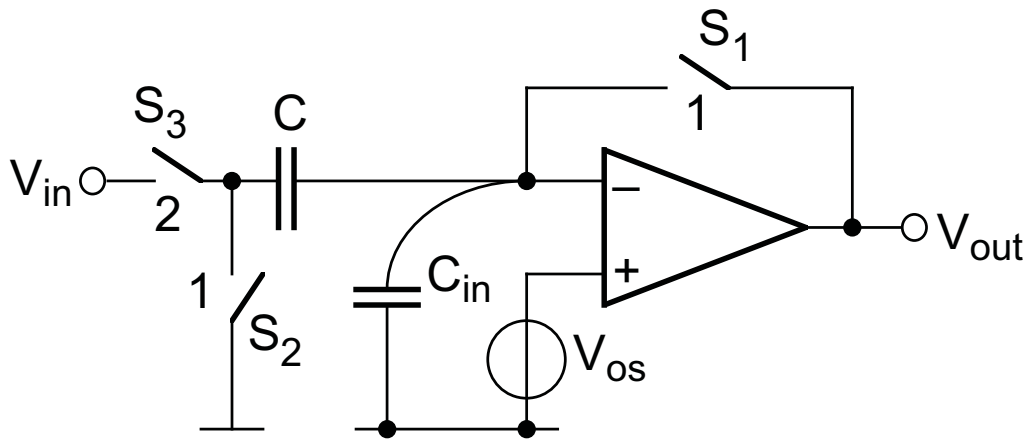
Offset Cancellation Techniques

- The finite gain A_v of the gain stage produces a residual offset error

$$V_{os,res} = V_{os} - V_{os}\frac{A_v}{1+A_v} = V_{os}\frac{1}{1+A_v}$$

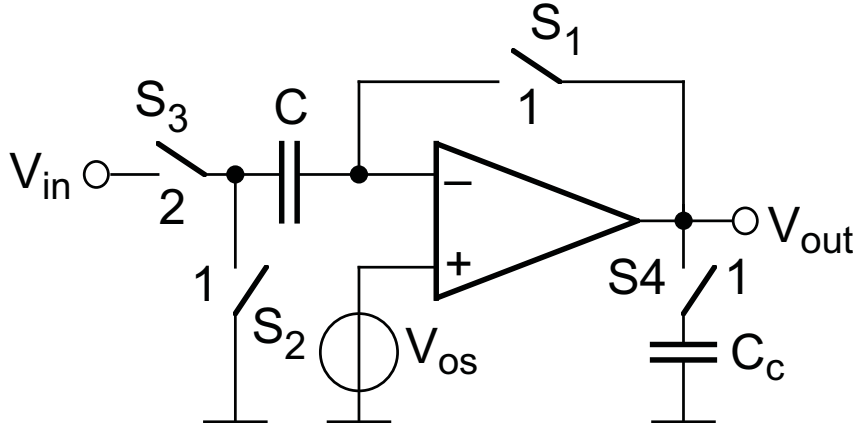
- The clock feedthrough at the opening of S_1 determines an equivalent offset error ($V_{os,ck}$)

$$V_{os,res} = V_{os}\frac{1}{1+A_v} + v_{os,ck}$$



Offset Cancellation Techniques

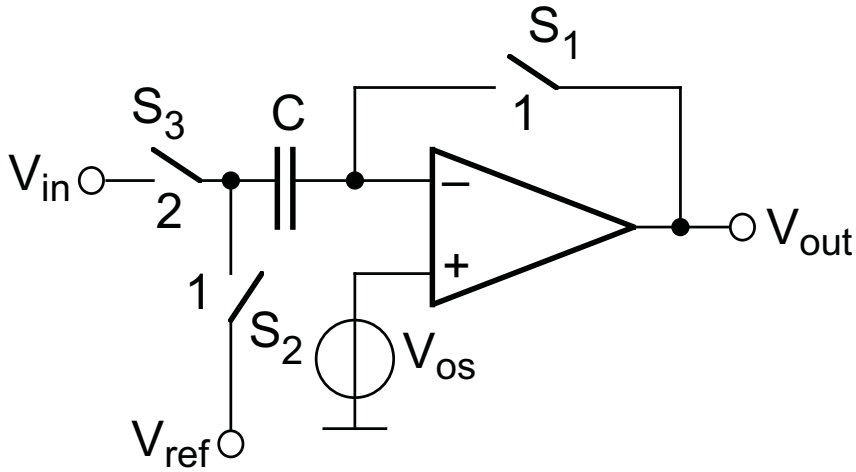
- The charge injected by the switch S_1 is integrated onto C and the input capacitance of the gain stage
- The input signal is attenuated by the factor $C/(C + C_{in})$
- In order to reduce the attenuation and the equivalent offset $V_{os,ck} = Q_{ck}/(C + C_{in})$, C must be chosen much larger than C_{in}
- If complex gain stages are used it is necessary to compensate the stage during the autozero phase with capacitor C_c



- With the autozero technique the comparator can only detect zero-crossing

Offset Cancellation Techniques

Threshold voltage implementation



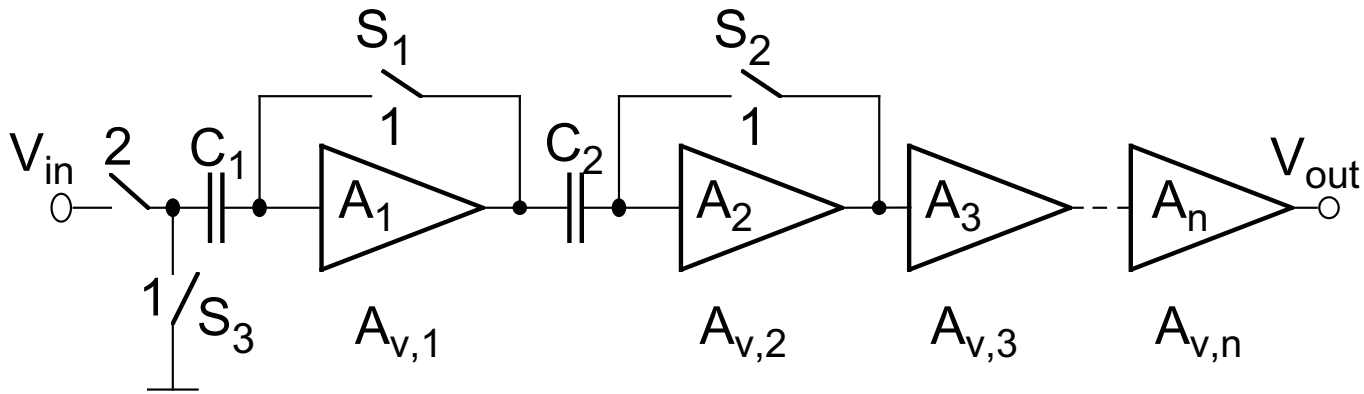
- The offset is canceled and the input voltage of the comparator during the comparison phase becomes

$$V_+ - V_- = -(V_{in} - V_{ref}) + V_{os,res}$$

- The comparator operates with the same input common-mode voltage independently of the value of V_{ref}

Offset Cancellation Techniques

Autozero in multi-stage comparators



- The gain of the comparator is $A_v = A_{v,1} A_{v,2} \cdots A_{v,n}$
- The offset of the third stage is referred to the input attenuated by the factor $A_{v1} A_{v2}$ ➜ It is negligible
- The input referred offset without autozero is

$$V_{os} = V_{os,1} + \frac{1}{A_{v,1}} V_{os,2}$$

Offset Cancellation Techniques

- The residual offset due to finite gain of A_1 is sampled on C_2 and canceled
- The overall residual offset with autozero is

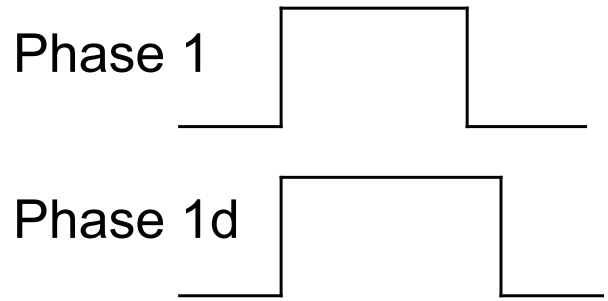
$$V_{os,res} = V_{os,2} \frac{1}{A_{v,1}\left(1 + A_{v,2}\right)}$$

- The clock feedthrough at the opening of S_1 and S_2 determines two equivalent offset errors at the input of A_1 and A_2 ($V_{os,ck,1}$ and $V_{os,ck,2}$)

$$V_{os,res} = V_{os,2} \frac{1}{A_{v,1}\left(1 + A_{v,2}\right)} + V_{os,ck,1} + V_{os,ck,2} \frac{1}{A_{v,1}}$$

- To reduce the residual offset due to clock feedthrough ➜ Open S_1 before S_2

Offset Cancellation Techniques

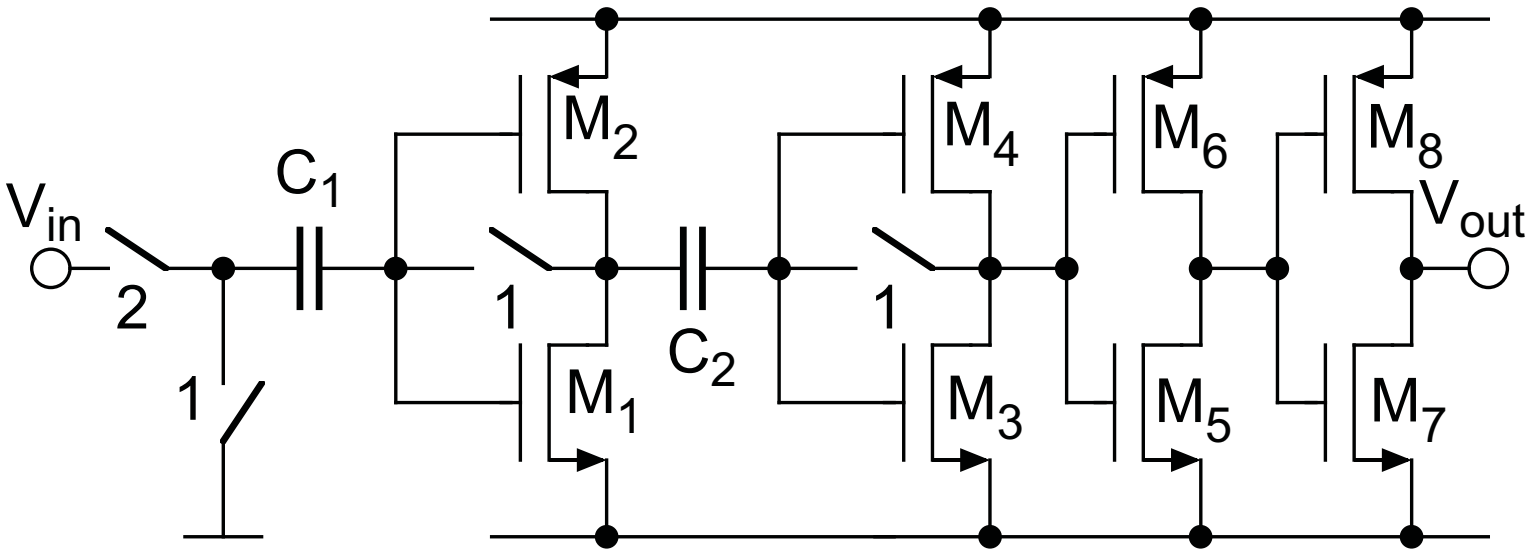


- S_1 is driven with phase 1, while S_2 and S_3 with phase 1d
- The charge injected by S_1 is collected on C_1 and the equivalent offset is amplified by $A_{v,1}$, but since S_2 is still on, the output voltage of A_1 is sampled and stored onto C_2
- $V_{os,1}$ and $V_{os,ck,1}$ are completely canceled, while $V_{os,2}$ and $V_{os,ck,2}$ are referred to the input attenuated by a factor $A_{v,1}$

$$V_{os,res} = V_{os,2}\frac{1}{A_{v,1}\left(1+A_{v,2}\right)} + V_{os,ck,2}\frac{1}{A_{v,1}}$$

Offset Cancellation Techniques

- Each gain stage can be implemented with a CMOS inverter ($A_v = 5 \div 20$)

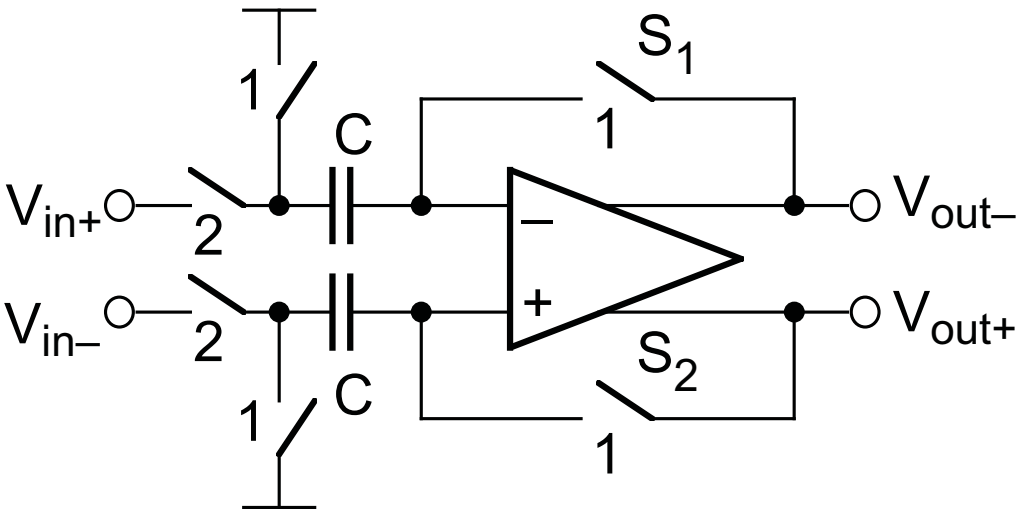


- During the autozero phase M_1, M_2, M_3 and M_4 are diode-connected ➜ The current consumption is not controlled
- Large W/L for M_1, M_2, M_3 and M_4 ➜ Fast inverters with large transconductance ➜ Low response time but large power consumption

Offset Cancellation Techniques

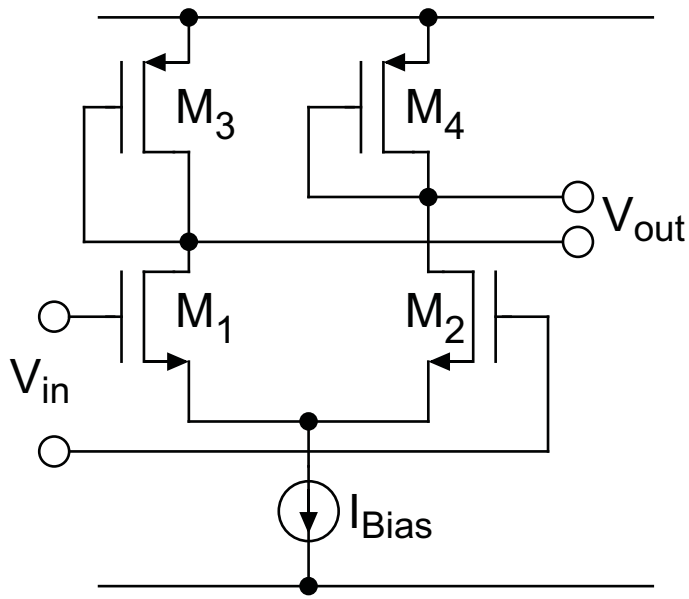
Fully-differential comparators

- In a fully-differential comparator, the clock feedthrough due to the opening of S_1 and S_2 produces a common mode signal
- The effect is attenuated by the common-mode rejection ratio (*CMRR*)
- Residual offset is only due to mismatches in the fully-differential structure



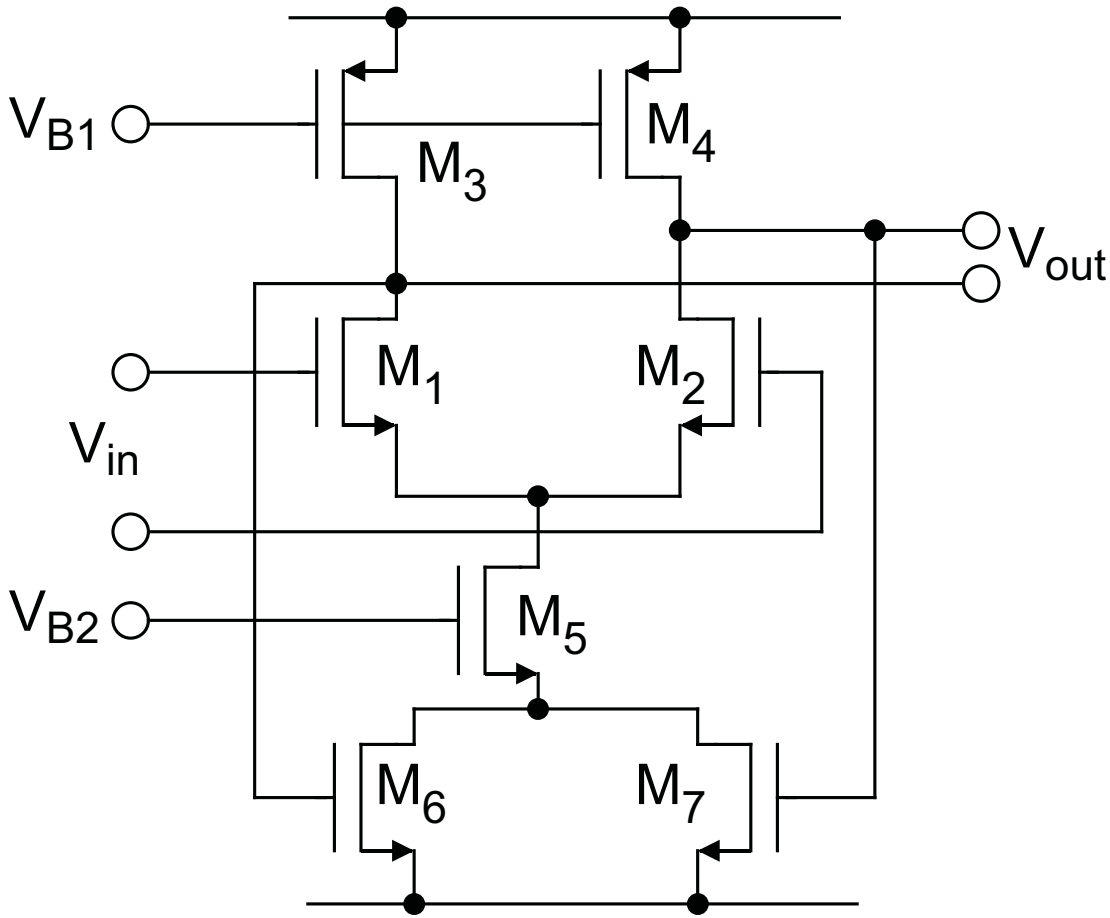
Offset Cancellation Techniques

- Fully-differential comparator gain stages
  - Stages with very low gain
  - Stages with low gain and common-mode feedback
  - Conventional fully-differential amplifiers
- Stages with very low gain
  - The common-mode feedback is not required [+]
  - The parasitic capacitances $C_{gs,3,4}$ load the output node [−]

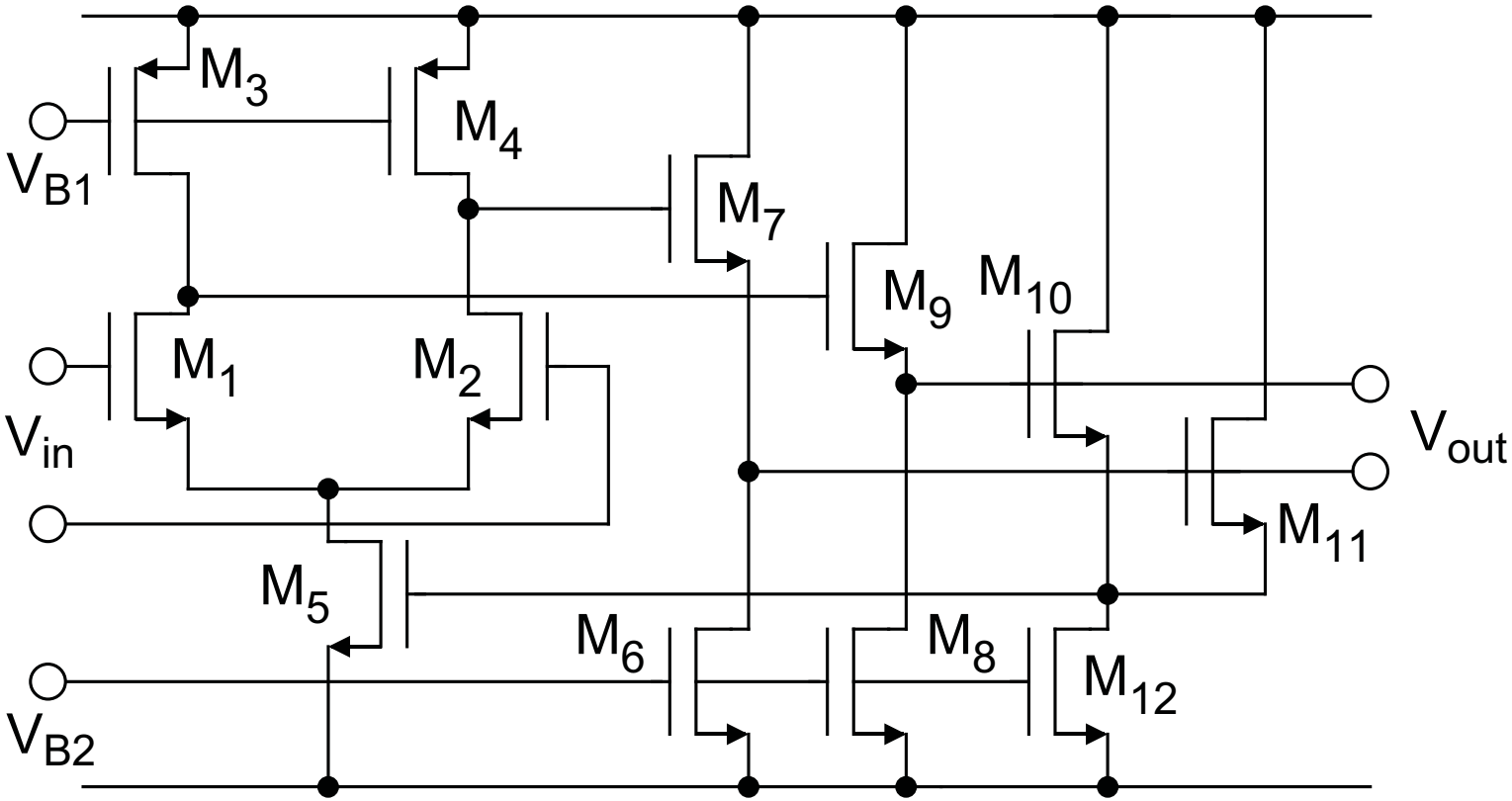


Offset Cancellation Techniques

- Stages with low gain and common-mode feedback
  - Low capacitive load at the high impedance nodes [+]
  - Common-mode feedback is required [−]



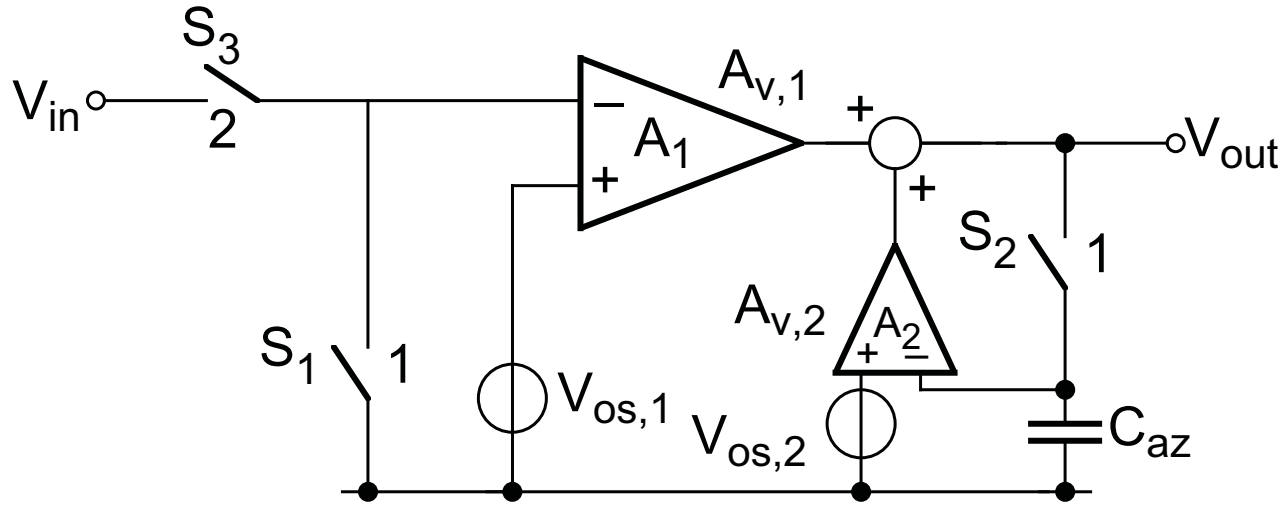
Offset Cancellation Techniques



Offset Cancellation Techniques

Offset compensation by auxiliary input stage

- Basic idea ➜ Store the offset at the output of the gain stage and use it in feedback connection to cancel the input offset



- During phase 1, the inputs of A_1 are short-circuited, the output of A_1 becomes $A_{v,1}\,V_{os,1}$ and the output of the comparator is

$$V_{out} = V_{os,1}\frac{A_{v,1}}{1+A_{v,2}} + V_{os,2}\frac{A_{v,2}}{1+A_{v,2}}$$

Offset Cancellation Techniques

- During phase 2, the residual input referred offset is

$$V_{os,res} = V_{os,1}\frac{1}{1+A_{v,2}} + V_{os,2}\frac{A_{v,2}}{(1+A_{v,2})A_{v,1}} \cong \frac{V_{os,1}}{A_{v,2}} + \frac{V_{os,2}}{A_{v,1}}$$

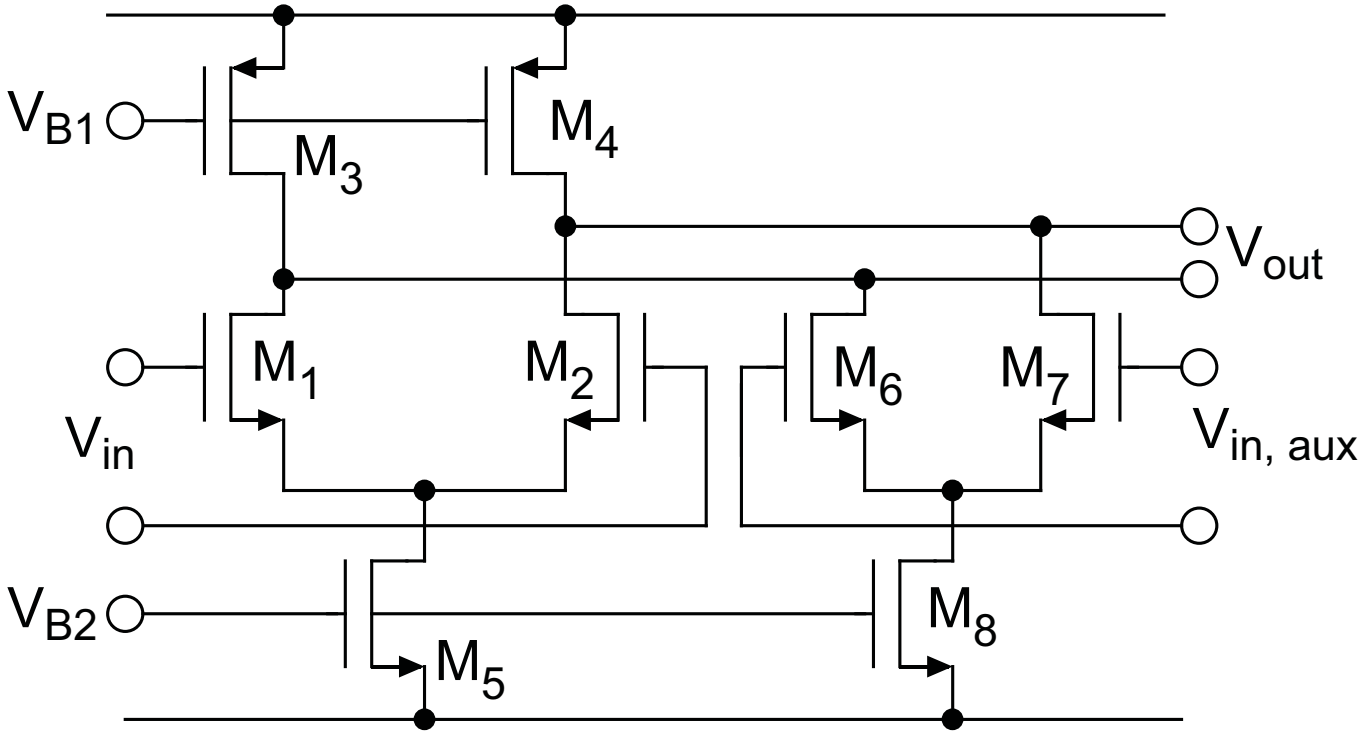
- If S_1 is opened while S_2 is still closed, the additional offset caused by the clock feedthrough from S_1 is attenuated by a factor $1/(1+A_{v,2})$
- When S_2 is opened the clock feedthrough produces an equivalent input referred offset $V_{os,az}$ on C_{az}, which referred to the input becomes

$$V_{os,ck} = V_{os,az}\frac{A_{v,2}}{A_{v,1}}$$

- If $A_{v,1}$ is larger than $A_{v,2}$, then $V_{os,ck}$ is reduced (optimal choice is $A_{v,2} = \sqrt{A_{v,1}}$)

Offset Cancellation Techniques

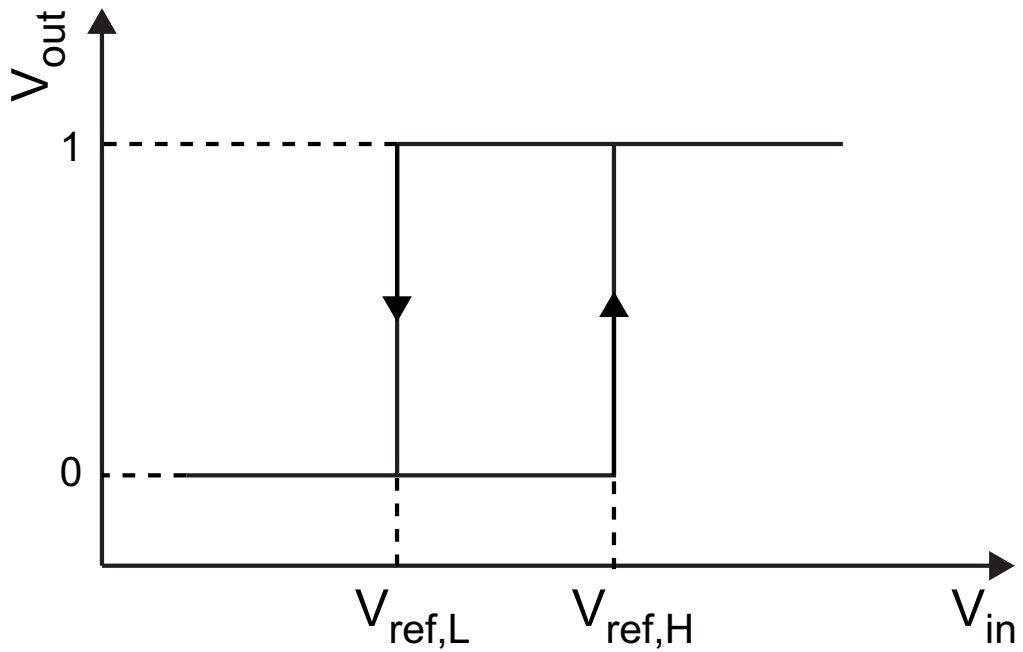
- Implementation with double differential stage



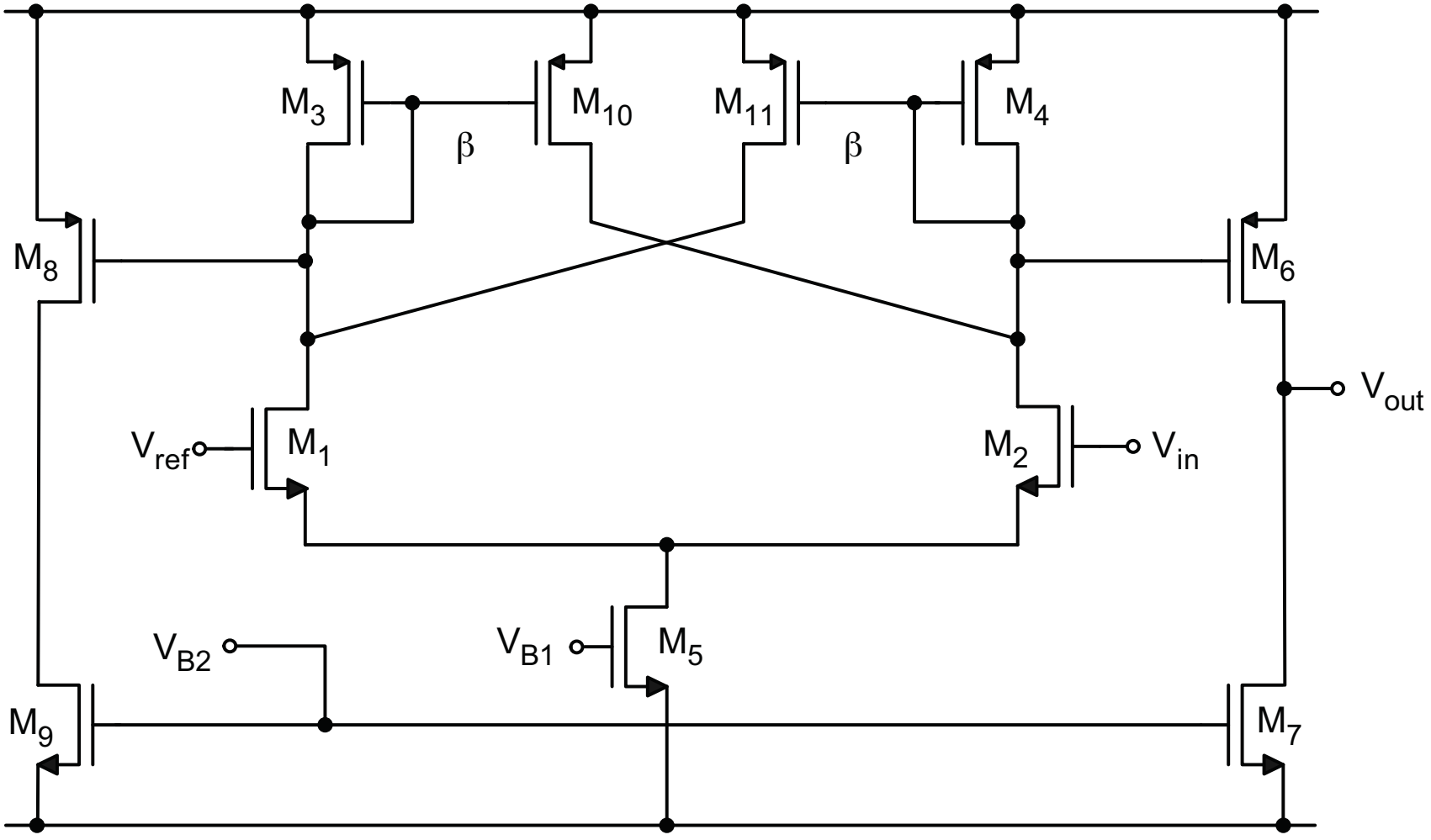
$$\frac{A_{v,1}}{A_{v,2}} = \frac{g_{m1,2}}{g_{m6,7}}$$

Comparators with Hysteresys

- When in a comparator the input signal is near the threshold voltage and varies slowly with respect to the response time, noise can produce oscillations in the output
- Hysteresis ➜ The threshold voltage when the output changes from “0” to “1” ($V_{ref,H}$) is larger than the threshold voltage when the output changes from “1” to “0” ($V_{ref,L}$)



Comparators with Hysteresys



Comparators with Hysteresys

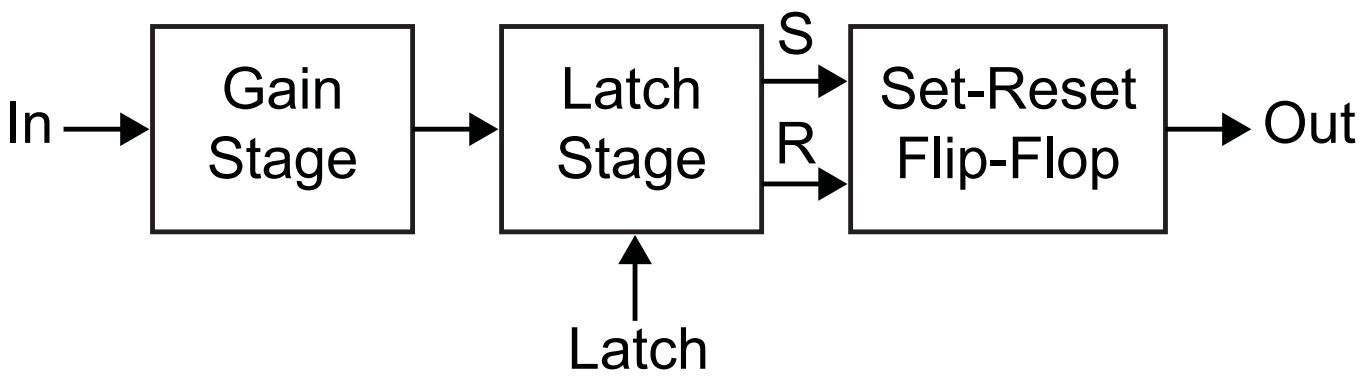
- If $V_{in} \ll V_{ref}$ then M_1 and M_3 are on, M_2, M_4 and M_{11} are off, M_{10} is in the triode region ➜ $V_{out} = 0$
- If $V_{in} \gg V_{ref}$ then M_2 and M_4 are on, M_1, M_3 and M_{10} are off, M_{11} is in the triode region ➜ $V_{out} = 1$
- If $V_{out} = 0$, $V_{in} \cong V_{ref}$ and rising, when $I_2 > \beta I_1$ ➜ M_4 turns on, M_3 turns off and $V_{out} = 1$ ➜ $V_{ref,H} > V_{ref}$
- If $V_{out} = 1$, $V_{in} \cong V_{ref}$ and falling, when $I_1 > \beta I_2$ ➜ M_3 turns on, M_4 turns off and $V_{out} = 0$ ➜ $V_{ref,L} < V_{ref}$
- The hysteresis is controlled by the current mirror ratio β

$$\beta = \frac{W_{10} L_3}{L_{10} W_3} = \frac{W_{11} L_4}{L_{11} W_4}$$

- Transistors M_{10} and M_{11} create a positive feedback loop that, besides introducing hysteresis, makes the response time of the comparator faster

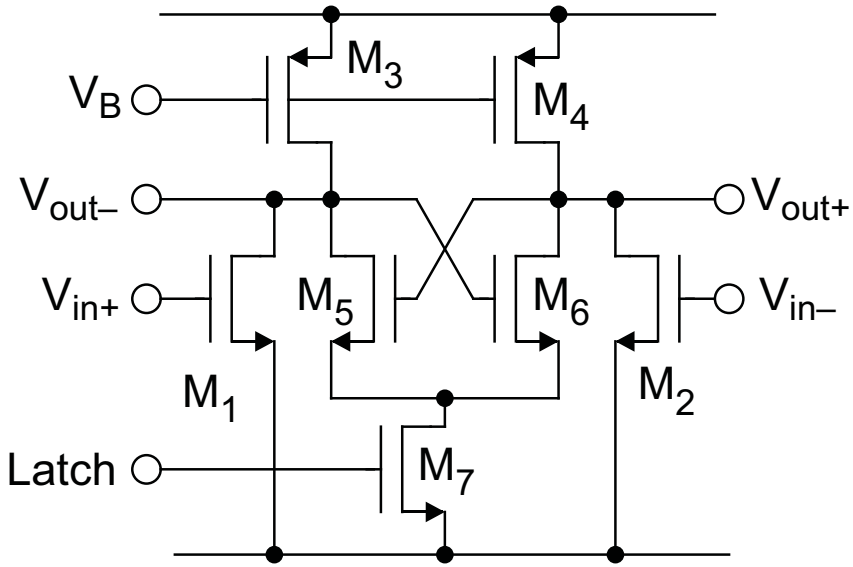
Latched Comparators

- In latched comparators, comparison is performed at given time instants (controlled by the *Latch* signal) and the result is maintained until the next comparison is performed
- Latched comparators are typically used in sampled-data systems (e.g. data converters), where the latch signal is the clock
- A latched comparator consists of a gain stage followed by a latch stage and eventually a set-reset flip-flop to hold the output signal while the latch is reset ($\overline{Latch}$ signal)
- The latch stage is based on a positive feedback loop ➜ Very fast response time



Latched Comparators

Simple latch stage



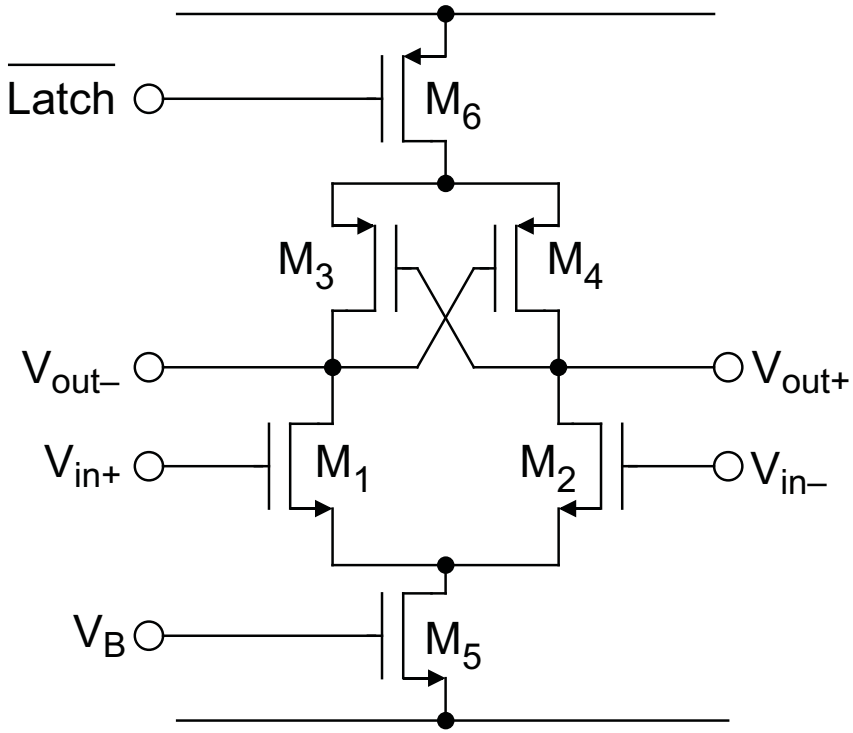
- During the reset phase ($\overline{Latch}$) M_1, M_3 and M_2, M_4 form two inverters with active load
- The parasitic capacitances at nodes V_{out+} and V_{out-} are precharged to the desired logic signals

Latched Comparators

- During the latch phase (*Latch*) the positive feedback is enabled and the latch reaches a stable state
- The state of the latch depends on the logic level precharged in the parasitic capacitances
- Thanks to the regenerative behavior of the positive feedback loop the response time is very short even with small input signals
- The offset of the latch cannot be canceled with autozero or auxiliary stages
- To reduce the offset transistors M_5 and M_6 must have relatively large area (WL) ➜ Speed limitation
- Since the latch is reset before each comparison overdrive recovery is not an issue

Latched Comparators

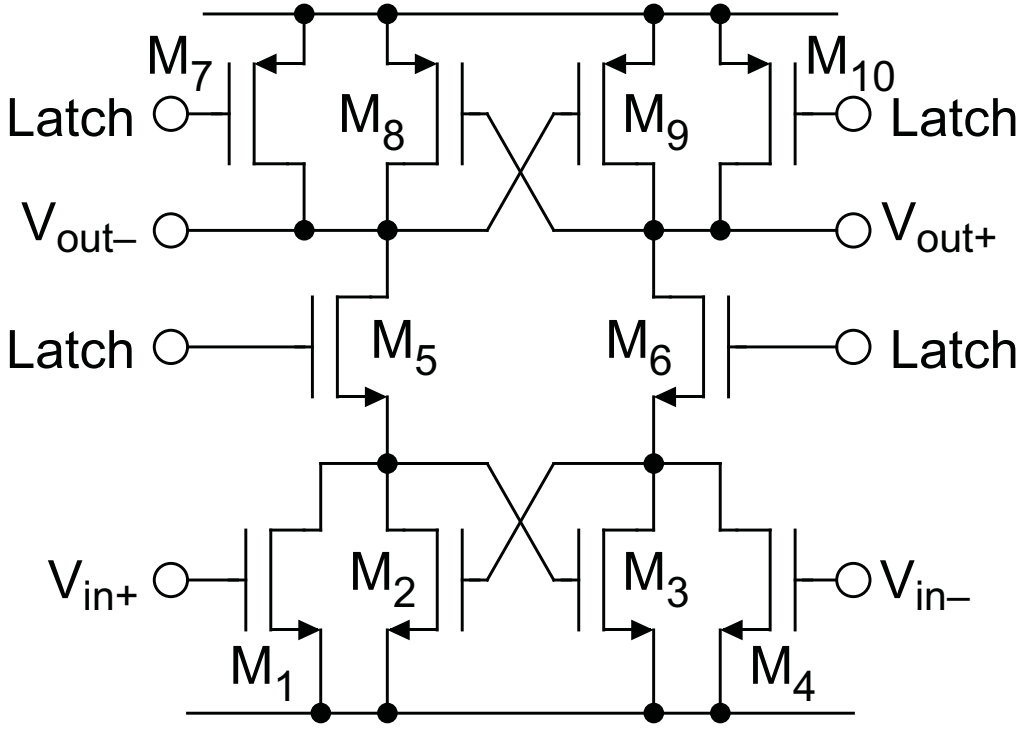
Differential stage with regenerative load



- The input signal unbalances the currents flowing in M_1 and M_2
- When the *Latch* signal is applied, in the regenerative loop (M_3 and M_4) the transistor with the largest current wins

Latched Comparators

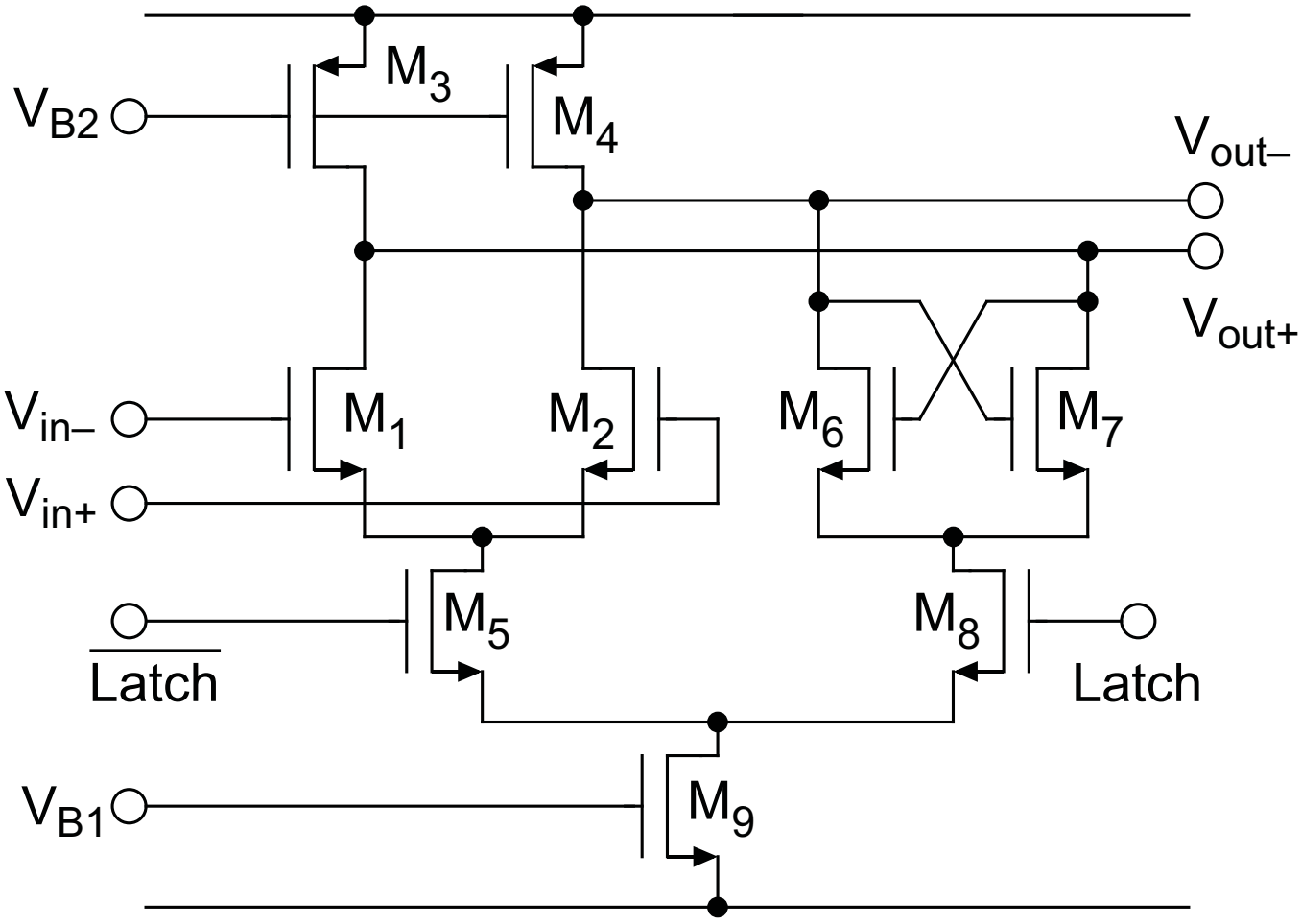
Latch stage with double regenerative loop



- Double positive feedback loop ➜ Fast response
- One positive feedback loop strengthens the other

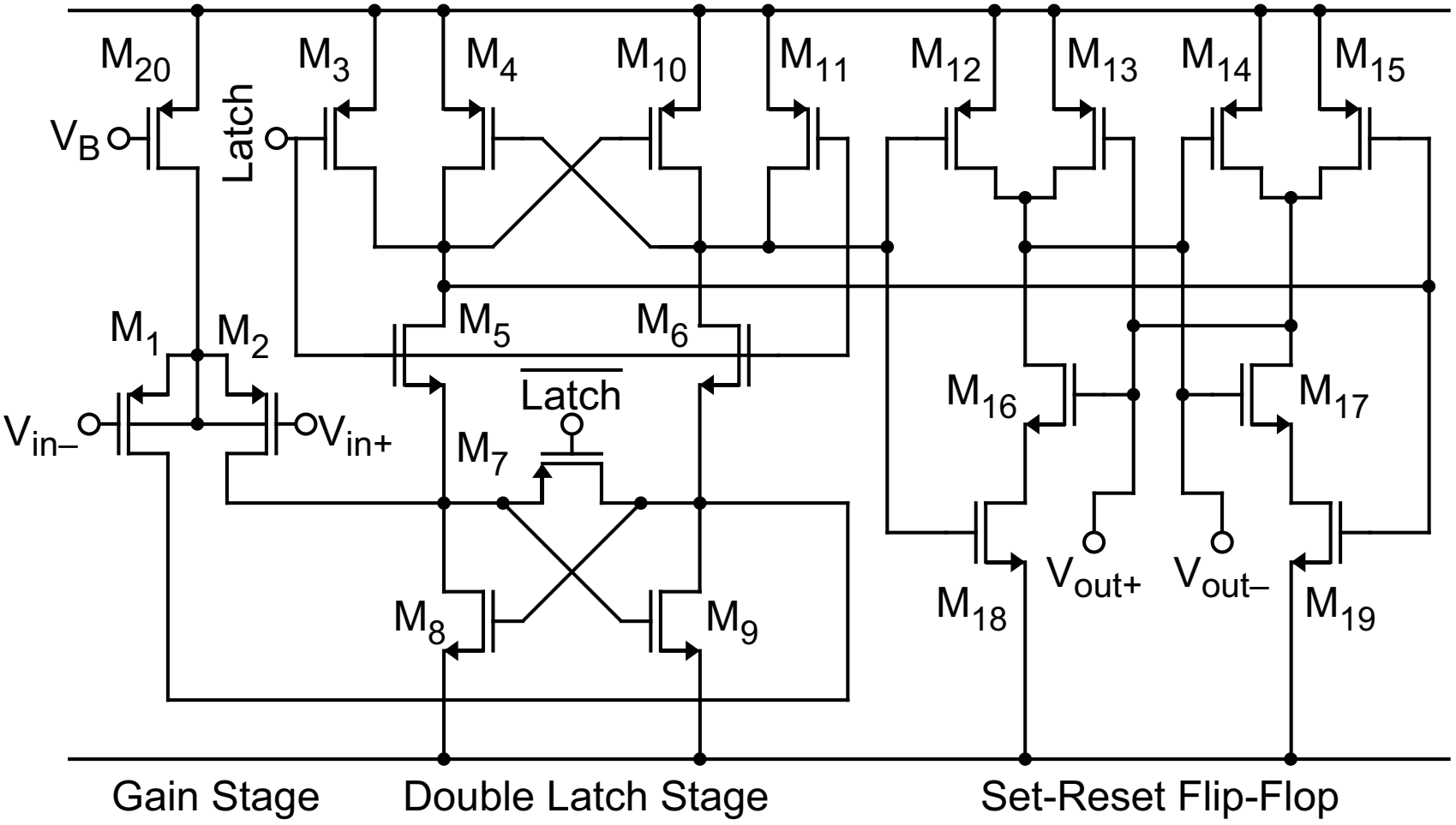
Latched Comparators

Combination between gain stage and latch



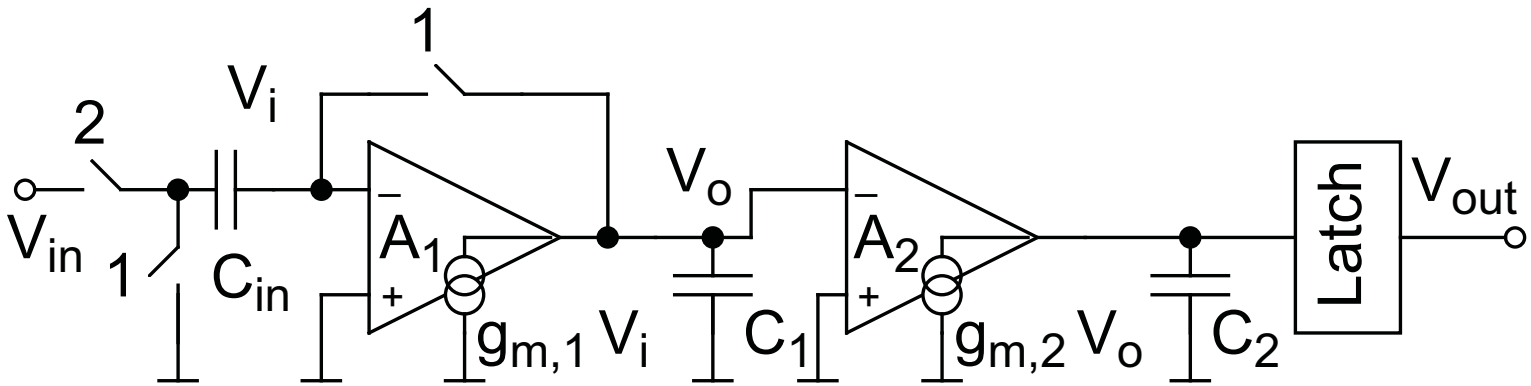
Latched Comparators

Complete latched comparator



Power Consumption

Comparator with two gain stages, autozero and latch



- The voltage at the output of the first stage is

$$V_o(t) = \frac{g_{m,1}}{C_1} \int_0^t V_{in}(t)\, dt$$

- The voltage swing at the output of the second stage is

$$V_{out}(t) = \frac{g_{m,2}}{C_2} \int_0^t V_o(t)\, dt$$

Power Consumption

- For constant or slowly varying signal at the end of the comparison phase (γ/f_{ck}) the output voltage V_{out} is

$$V_{out}\left(\frac{\gamma}{f_{ck}}\right) = \frac{1}{2} V_{in} \frac{g_{m,1} g_{m,2}}{C_1 C_2} \left(\frac{\gamma}{f_{ck}}\right)^2$$

- MOS transistors in strong inversion

$$g_m = \sqrt{\frac{2\mu C_{ox} I_D W}{L}}, \; I_D > 2n\mu C_{ox} \frac{W}{L} \left(\frac{kT}{q}\right)^2$$

- MOS transistors in weak inversion

$$g_m = \frac{qI_D}{nkT}, \; I_D < 2n\mu C_{ox} \frac{W}{L} \left(\frac{kT}{q}\right)^2$$

Power Consumption

- If the input voltage of a gain stage exceeds the critical value $V_{crit} = nkT/q$ or $V_{crit} = (V_{GS} - V_{th})/2$, the output current saturates to the maximum value $I_{max} = 2I_D$
- To achieve a given value of V_{out} the current in the second stage must be

$$I_{D,2} > \frac{V_{out} C_2 f_{ck}}{2\gamma}$$

- The current in the first stage can be obtained from

$$\begin{cases} g_{m,1} > \frac{V_{crit} C_1 f_{ck}}{V_{in,min}\gamma}, & V_{in,min} < V_{crit} \\ I_{D,1} > \frac{V_{crit} C_1 f_{ck}}{2\gamma}, & V_{in,min} > V_{crit} \end{cases}$$

- The obtained values of $I_{D,1}$ and $I_{D,2}$ lead to the minimum theoretical value of the comparator power consumption
- In practical designs a safety margin has to be considered

References

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