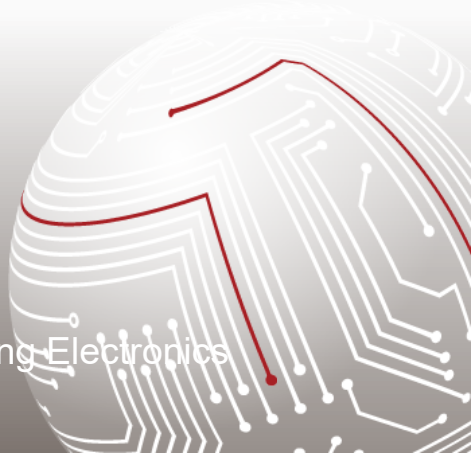
JEDEC

Global Standards for the Microelectronics Industry

LPDDR5 Clocking and Read/Write Operation

Samsung Electronics



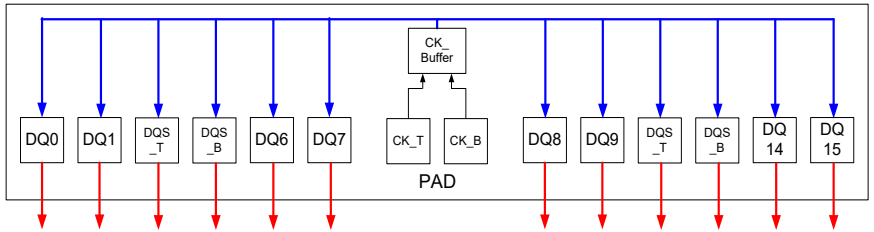
LPDDR5 Workshop

Copyright © 2019 Samsung Electronics

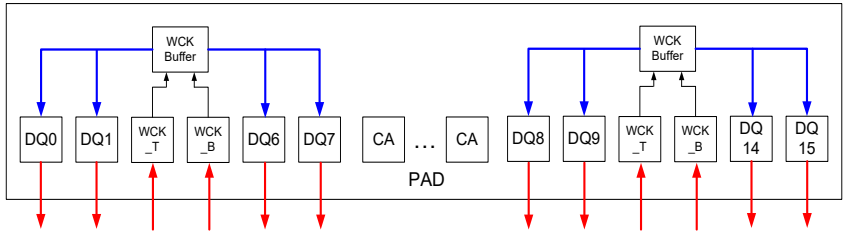
LPDDR5 WCK clocking for High frequency

- Low Power CMD clocking (WCK:CK=2:1 or 4:1 mode)
- Better jitter characteristic with shorter strobe signal path
- Requires CK/WCK domain sync before RD/WR operation

LPDDR4/4X

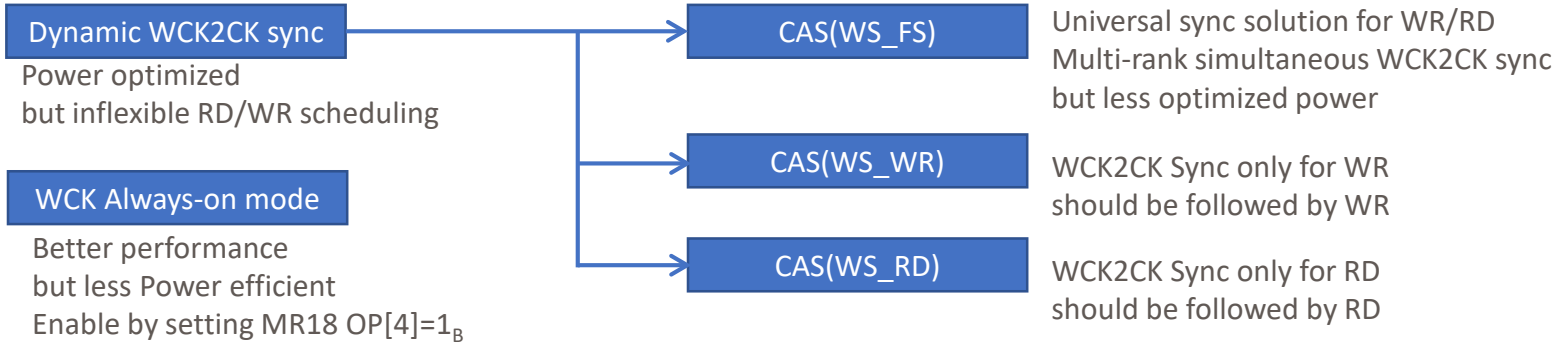


LPDDR5



WCK2CK sync operands in CAS and it's use.

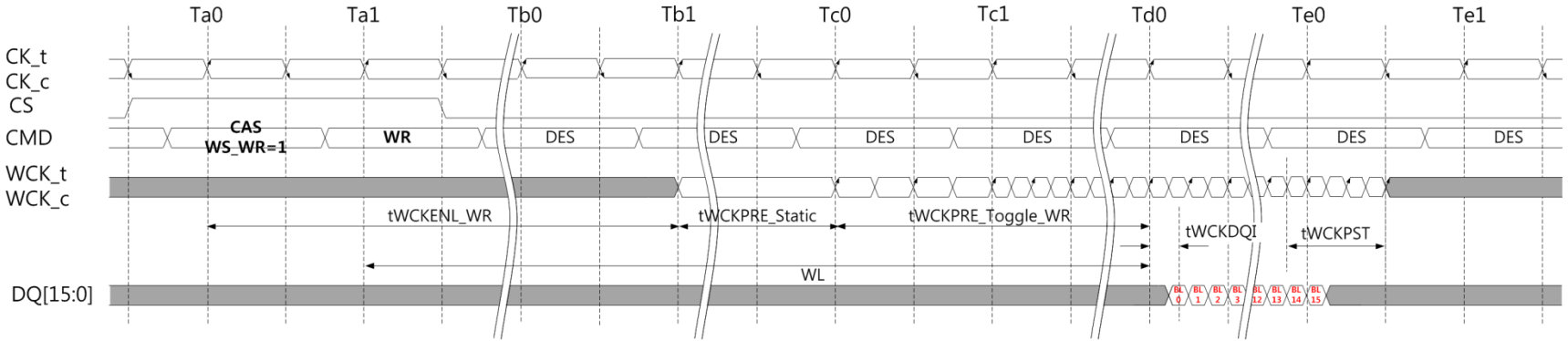
- Make your own system's WCK2CK sync plan with below options.



SDRAM COMMAND	BK ORG (BG, 16B, 8B)	SDR CMD PIN	DDR COMMAND PINS						
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6
CAS	Any	H	L	L	H	H	WS_WR	WS_RD	WS_FS
		X	DC0	DC1	DC2	DC3	WRX	V	B3

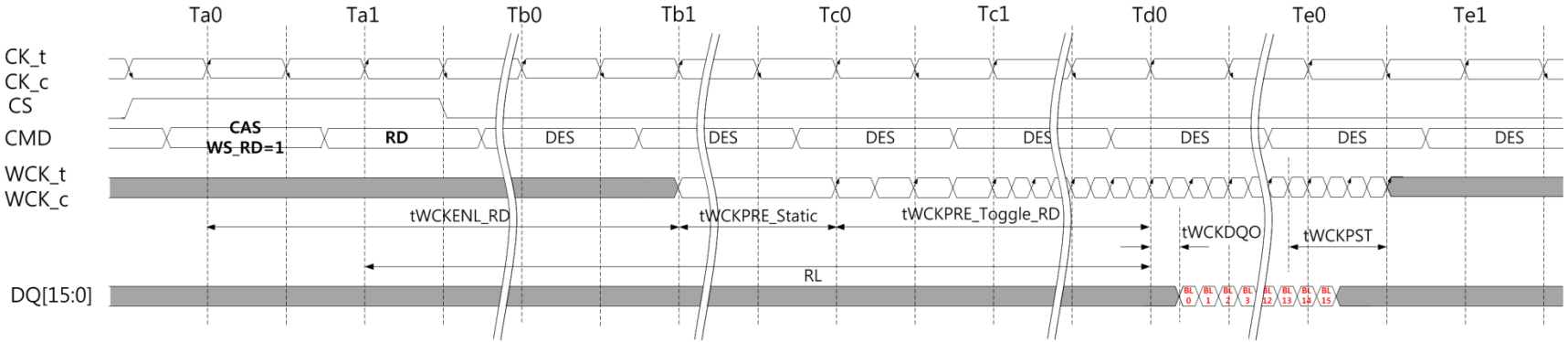
Write Operation with WCK2CK sync

- WR CMD should be precede by CAS(WS_WR=1) without gap.
- Need “tWCKENL_WR + tWCKPRE_Static + tWCKPRE_Toggle_WR” for WCK2CK sync operation before WR data input



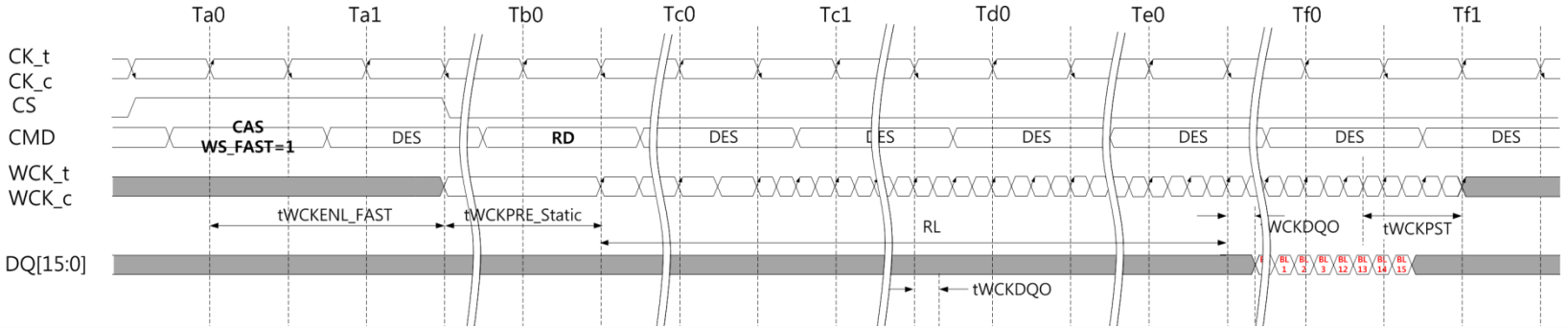
Read Operation with WCK2CK sync

- WR CMD should be precede by CAS(WS_WR=1) without gap
- Need “tWCKENL_RD + tWCKPRE_Static + tWCKPRE_Toggle_RD” for WCK2CK sync operation before RD data output



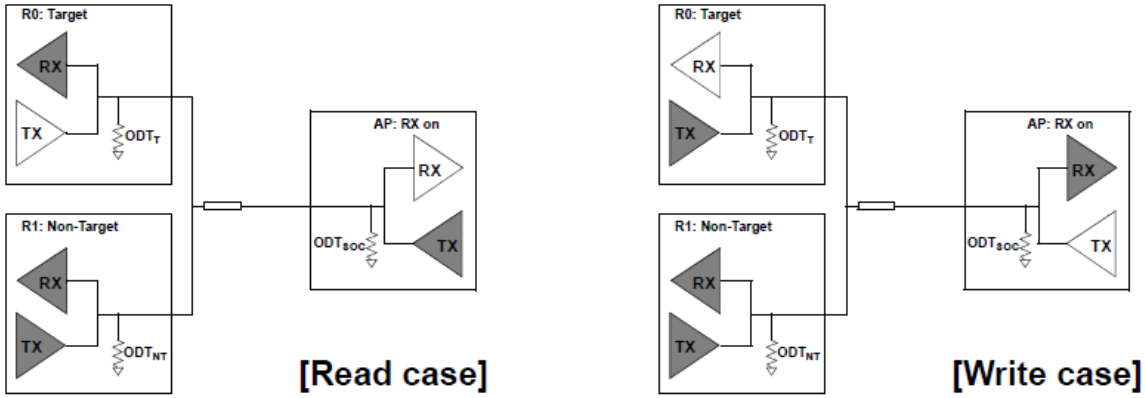
WCK2CK Fast sync for both RD & WR

- Allow timing gap btw CAS(WS_FS) and READ/WRITE
- Support multi-rank simultaneous WCK2CK sync operation
- Need “tWCKENL_FAST + tWCKPRE_Static” for WCK2CK sync operation
- Guarantee WCK toggle to maintain synced-state until WCK2CK sync off
- DRAM automatically turns off WCK2CK sync logic after “WCK2CK Sync off timing” constraint



Interface

- Same as LPDDR4x(LVSTL), but supports two VDDQ levels (0.5V, 0.3V)
- During DVFSQ mode, LVSTL_0.3 can be used (with limited frequency)
- NT-ODT (Non-target ODT) – SI improvement in 2-rank config.



Power saving features

- Traditional DBI_DC
- New feature from LP5
  - Data Copy
  - Write X
  - Deep Sleep Mode
  - DVFSQ/ DVFSC

Data Masking and DBI_DC

- DMI(Data Mask Inversion) – Bus inversion, write DM and *parity bits*
  - LPDDR5 device supports Data Mask (DM) function for WR
  - LPDDR5 device supports Data Bus Inversion (DBI-DC) function for WR & RD
  - LPDDR5 supports DM and DBI-DC function with a byte granularity
  - LPDDR5 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel
- DMI behavior: link ECC (write) & data copy (write and read) combinations

Pin name	DBI enable	Link Protection disabled		Link Protection enabled	
		Write	Read	Write	Read
DMI	No	DM	N/A	DM	Parity
	Yes	DMI	DBI	DMI	Parity

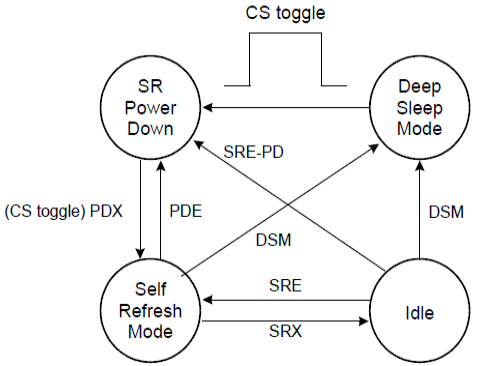
Power Down Mode

- Removed CKE pin from LPDDR5
- Command based power down entry and exit
  - Holding CS HIGH, CA[5:0] LOW and CA6 HIGH at the first rising edge of the clock
  - No refresh operations are performed in Power-Down mode except Self-Refresh Power-Down and Deep Sleep Mode
  - The Power-Down state is asynchronously exited when CS toggles HIGH (VDD2H)

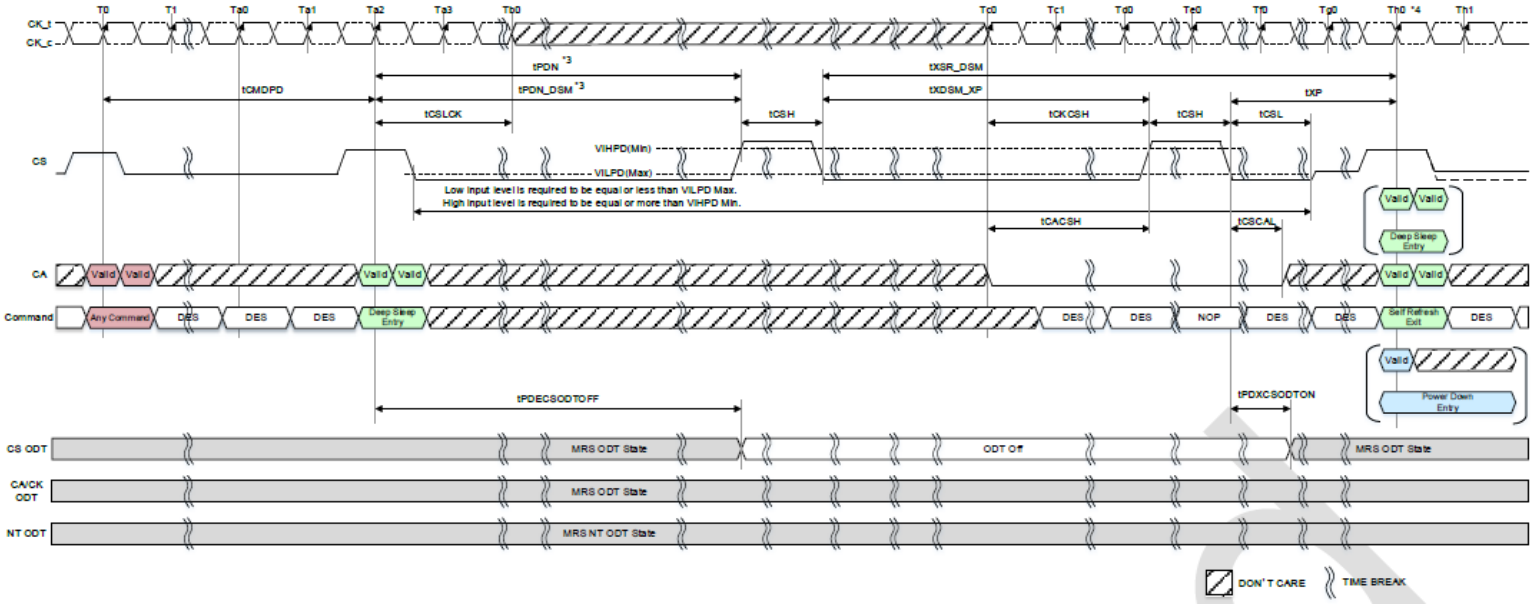
Deep Sleep Mode

- Additional self-refresh mode with longer entry/exit times
  - Allow the DRAM to manage internal circuits for lower current consumption
  - DRAM is almost turned off except for self-refresh operation parts
- DSM is only allowed when read data burst is completed and SDRAM is idle state or self-refresh state

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Deep Sleep Mode Timing					
Minimum interval between Deep Sleep Mode Entry and Exit	t_{PDN}	Min	Max(TBDns, TBDnCK)	ns	
Minimum Deep Sleep Mode duration time for DRAM compliance with IDD tbd power specification	t_{PDN_DSM}	Min.	4	ms	
Delay from Deep Sleep Mode Exit to SRX	t_{XSR_DSM}	Min.	200	us	

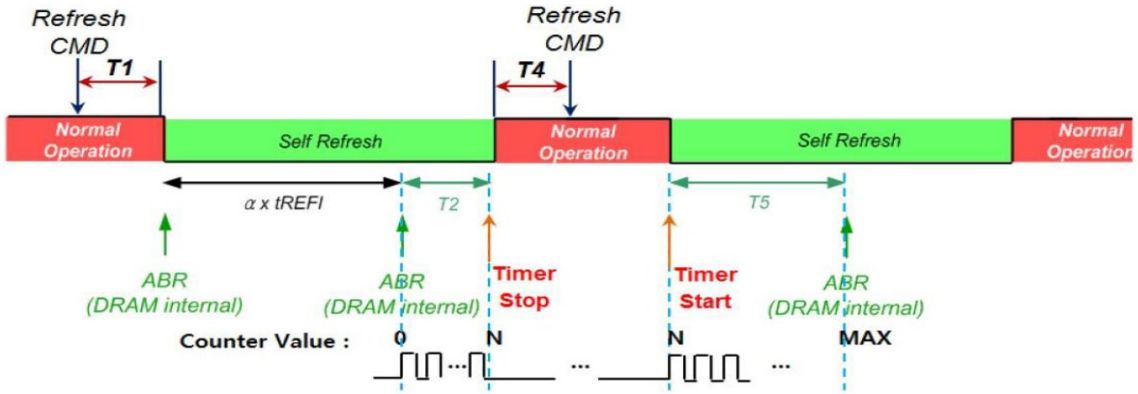


Timing diagram of DSM



Optimized Refresh - Background

- The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered.
- Upon exit from Self Refresh, it is required that at least one REFRESH command is issued before entry into a subsequent Self Refresh.



Optimized Refresh - Implementation

- Upon exit from self refresh mode, LPDDR5 SDRAM freeze and store the refresh timer value. When the DRAM enters self refresh mode, it shall resume the refresh timer from the saved value and increase it to the next value so that LPDDR5 can operate ABR only when the refresh timer expires in self refresh mode.

MR25 OP[7] for Optimized Refresh Control

Function	Register Type	Operand	Data
Optimized Refresh mode	Write-Only	OP[7]	0_B: Optimized Refresh mode disabled 1_B: Optimized Refresh mode enabled (default)

PASR (Partial Array Self Refresh)

- The LPDDR5 SDRAM adopts 8 bank base refresh schemes. A segment in each bank for 8 bank bases of the LPDDR5 SDRAM can be independently configured whether a Self Refresh operation is taking place.
- The mask bit to the segment controls a refresh operation of entire memory within the segment. When the segment is masked via MRW, a refresh operation to the entire segment is blocked and data retention by a segment is not guaranteed in Self Refresh mode. To enable a refresh operation to the segment, a coupled mask bit has to be programmed, “unmasked”.

Table 88 — MR23 Definition

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write Only	[7:0]	0_B: Segment Refresh Enable (default) 1_B: Segment Refresh Disable	1,2

Table 89 — Row Address of Masked Segment for x16 Mode

Segment	OP[n]	Segment Mask	2Gb R12:R10	3Gb R13:R11	4Gb R13:R11	6Gb R14:R12	8Gb R14:R12	12Gb R15:R13	16Gb R15:R13	24Gb R16:R14	32Gb R16:R14
0	0	xxxxxxx1	000_B								
1	1	xxxxxx1x	001_B								
2	2	xxxxx1xx	010_B								
3	3	xxxx1xxx	011_B								
4	4	xxx1xxxx	100_B								
5	5	xx1xxxxx	101_B								
6	6	x1xxxxxx	110_B	Not Allowed	110_B	Not Allowed	110_B	Not Allowed	110_B	Not Allowed	110_B
7	7	1xxxxxxx	111_B		111_B		111_B		111_B		111_B
NOTE 1	This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.										
NOTE 2	For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00_B).										

PAAR (Partial Array Auto Refresh)

- LPDDR5 SDRAM supports Partial Array Refresh Control (PARC) to reduce IDD5 power consumption.
- If PARC MR25 OP[6]=1B, LPDDR5 SDRAM skips the refresh of segment where defined PASR Segment Mask: MR23 OP[7:0] when All bank or Per bank Refresh command is received.

Table 94 — MR25 Definition

Function	Register Type	Operand	Data	Notes
PARC (Partial Array Refresh Control)		OP[6]	0_B: PAAR disable (default) 1_B: PAAR enable	3,4

Tx and UI Jitter

- DQ to RDQS differential jitter over NUI of mismatch.
- Appropriate RDQS preamble mode must be selected
  - tDQSQ_NUI=tDQSQ(NUI)-N*UI
  - tQH_NUI = tQH(NUI)-N*UI

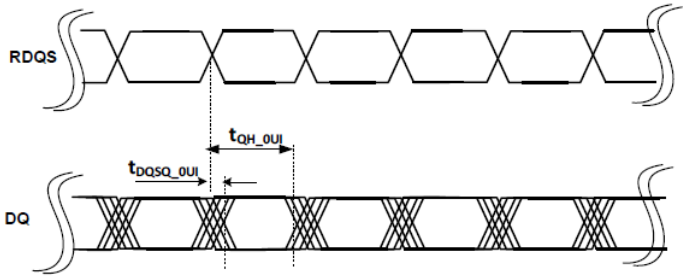


Figure 215 — DQ to RDQS 0UI read data timing example

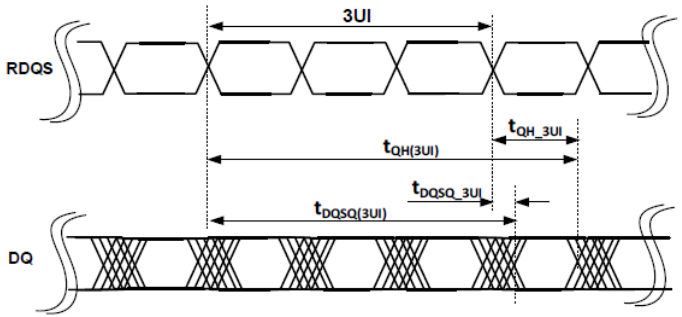


Figure 216 — DQ to RDQS 3UI read data timing example