INVITED PAPER

Technologies for Cofabricating MEMS and Electronics

Several different strategies show commercial promise for fabricating electronic and micro electromechanical devices on the same substrate; a de-facto standard has not yet been chosen.

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ABSTRACT | Microfabrication technologies initially developed for integrated electronics have been successfully applied to batch-fabricate a wide variety of micromechanical structures for sensing, actuating, or signal-processing functions such as filters. By appropriately combining the deposition, etching, and lithography steps for microelectromechanical devices with those needed for microelectronic devices, it is possible to fabricate an integrated microsystem in a single process sequence. This paper reviews the strategies for cofabrication, with an emphasis on modular approaches that do not mix the two process sequences. The integrated processes are discussed using examples of physical sensors (infrared imagers and inertial sensors), chemical and biochemical sensors, electrostatic and thermal actuators for displays and optical switching, and nonvolatile memories. By adding new functionality to integrated electronics, the use of microelectromechanical systems is opening new applications in sensing and actuating, as well as enhancing the performance of analog and digital integrated circuits.

KEYWORDS | Integrated circuit fabrication; microelectromechanical systems (MEMS); micromachining

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I. INTRODUCTION

Silicon microelectromechanical systems (MEMS) technology has its roots in the planar lithography and etching processes used to make integrated circuits. The cofabrication of electromechanical and electronic devices on the same substrate is technically feasible, although the specific requirements of each can impose constraints on the process sequence, thermal budget, and material selection. There are several incentives for MEMS— electronics integration, including enhanced signal transduction, reduced chip pinout, improved immunity from electromagnetic interference, and potentially lower cost compared with multichip implementations. These considerations partly motivated the conception and demonstration of the resonant-gate transistor in the 1960s and polysilicon microstructures integrated with n-channel metal–oxide–semiconductor (NMOS) transistors in the 1980s. With the accelerating commercialization of silicon MEMS since the late 1980s, several integrated MEMS technologies have been introduced for applications in inertial sensing, pressure sensing, displays, and microphones, with several being well-established commercial successes. A variety of technologies for cofabricating MEMS are currently on the verge of introduction. Over the past decade, several research groups have demonstrated modular approaches to cofabricating MEMS and electronics, which promise to reduce the manufacturing challenges.[1]

The advantages of cofabrication are balanced by complementary drawbacks. As a result, cofabricated or integrated MEMS coexist in the market with "system in package" approaches, in which the MEMS and electronic interface and signal-processing electronics are fabricated

[1]Rather than provide lengthy lists of references in the Introduction, the literature will be cited in the body of this paper in the context of specific materials, processes, and applications.

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separately. The high mask count, which is typically one or two masks more than the sum of the numbers required for the MEMS and electronic structures, reduces the process yield. The higher cost of a wafer with cofabricated MEMS and electronics, due to the added complexity and lower yield, must be compared with the cost of separate MEMS and electronics chips with assembly and packaging. In addition, the various constraints on the combined process may lead to compromises in the performance of the MEMS and/or the electronics. For example, the stress gradient in the microstructural thin film may be relatively large due to the requirement that any postdeposition stress-reduction anneal must stay within the thermal budget of the electronic structures. In some cases, very conservative design rules are used for the electronic devices to make them as robust as possible to the thermal process budget needed for MEMS, leading to low-density and low-performance circuits. Finally, the long turnaround in fabrication can slow the development cycle in comparison to multichip approaches with separate MEMS and electronics fabrication.

This paper reviews the major approaches to cofabricating MEMS and electronics. Although custom processes that interleave MEMS and electronic fabrication steps are feasible and have been commercialized, the trend in recent developments is toward more modular approaches. Fig. 1 illustrates several options for the modular cofabrication of complementary metal–oxide–semiconductor (CMOS) electronics and MEMS. In some cases, the MEMS process sequence, or at least most of it, can be completed prior to the CMOS transistor and metallization stack fabrication sequences—a "MEMS first" approach as shown in Fig 1. Processes that use silicon deep-reactive ion etching (DRIE) to fabricate silicon microstructures from silicon-on-insulator (SOI) substrates fall into this category, since most of the MEMS-specific fabrication steps are completed prior to the electronic fabrication sequence, with the exception of the silicon DRIE and sacrificial buried oxide etch at the end to define and release the microstructures. The second group of processes, termed "MEMS last" in Fig. 1, involves the deposition and patterning of MEMS layers after completion of the transistor and metallization stack fabrication sequences. Although these processes offer a high degree of modularity, the thermal budget of the MEMS process is severely constrained by the temperature limitations of the previously fabricated transistor and metallization structures. A variety of materials have been demonstrated to be suitable for low-temperature MEMS fabrication, including metals, amorphous silicon, and polycrystalline silicon-germanium (SiGe). These "MEMS-last" processes have the advantage of allowing the vertical stacking of microstructures on top of the electronics, which reduces the die size and can improve performance through reduced interconnect parasitic resistance and capacitance. The final category illustrated in Fig. 1 includes processes that fabricate microstructures by etching the CMOS metallization stack, which will be referred to as "CMOS MEMS" technologies. These processes require only the addition of an anisotropic reactive-ion etching step and an isotropic release-etching step. Since these technologies have been reviewed recently [88], this paper concentrates on emerging applications in inertial sensing, signal processing, and nonvolatile memory.

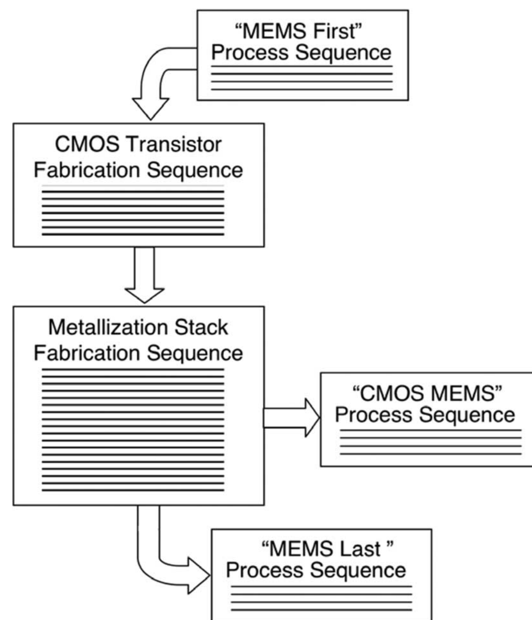


Fig. 1. ***Options for process integration of microelectromechanical structures and electronic fabrication sequences: i) interleaved steps, ii) MEMS-first, and iii) MEMS-last, including formation of microstructures from the metallization stack layers.***

II. SINGLE CRYSTAL SILICON AND OTHER MEMS-FIRST PROCESSES

Single crystal silicon (SCS) microstructures were initially cofabricated with junction field-effect or bipolar transistors for pressure sensing applications [1]–[3]. The microstructures were diaphragms formed by wet anisotropic etching from the backside of the wafer after completion of the frontside processing to form the transistor, piezoresistor, and interconnections—an early example of modular processing. For several reasons, integrated pressure sensors did not initially dominate the market. The low impedance output signal from the piezoresistive bridge is easily amplified using off-chip electronics. Also, the large area of the diaphragm compared to the small area of the adjacent interface amplifier area resulted in inefficient use of the lengthy process sequence.

In parallel with the early pressure sensor technologies, micromachined silicon neural probes with integrated amplifiers and multiplexer circuits were also investigated [4], [5]. Probes with multiple recording sites along the shank and CMOS electronics located in the base have been

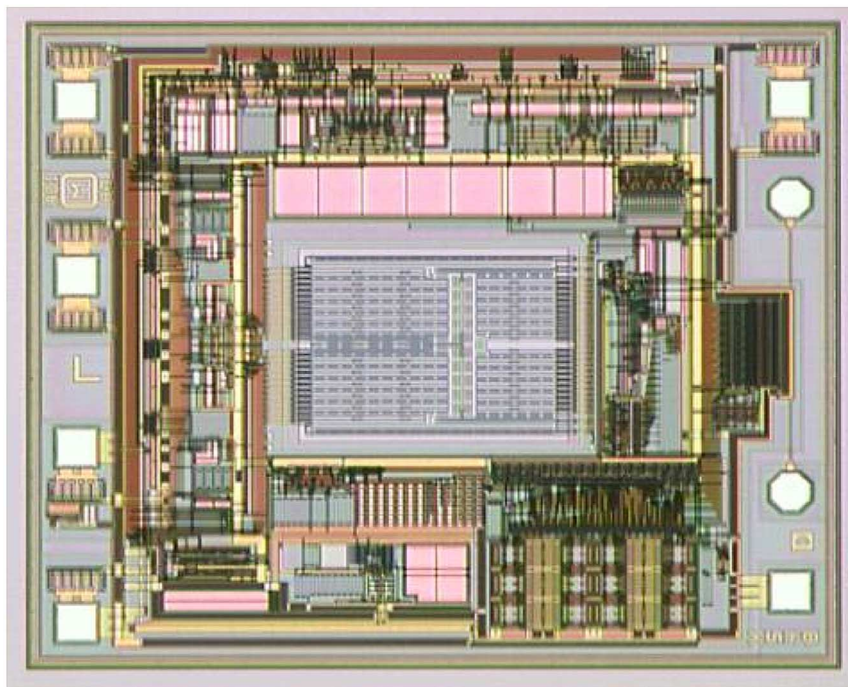


Fig. 2. ***Optical micrograph of prototype integrated SOI-MEMS accelerometer, in which silicon-on-insulator microstructures are cofabricated with CMOS (courtesy of Dr. T. Chen, Analog Devices, Inc.).***

fabricated and used by neurophysiology research groups. In order to fabricate the probe structure, a heavily boron-doped region is diffused into the wafer, which stops the wet silicon etchant. The electronics are protected from the wet etch by means of dielectric passivation layers as well [4]. Recently, these processes have been further extended to fabricate a wireless, battery-free pressure sensor for use in monitoring of arterial blood flow [5]. This microsystem is among the most sophisticated ever demonstrated, with 22 masking steps being used on a silicon wafer and a bonded glass substrate to fabricate the compliant antenna structure for telemetry and power delivery, the capacitive pressure sensing diaphragm, and the bipolar-CMOS (BiCMOS) signal conditioning and control circuitry.

In recent years, the advent of DRIE processes for silicon [6] and the widespread availability of SOI wafers has enabled the cofabrication of more complex single crystal silicon microstructures together with CMOS electronics. The initial demonstration of surface micromachining using SOI substrates was by Diem *et al.* in the early 1990s [7]. An early MEMS-first process used DRIE to define thick mechanical structures in polysilicon formed over a buried oxide during epitaxial silicon growth [8]. Bipolar transistors and interconnects were then fabricated in the surrounding epitaxial layer. In the case of thick (10 μm or more) SOI microstructures, cofabrication with electronics was problematic until trench-refill isolation processes were demonstrated [9]. SOI-based microstructures have been cofabricated with commercial CMOS electronics [10], [11] using the sidewall trench isolation approach (see Fig. 2 for example). In this technology, the electrical isolation trenches are etched and refilled with oxide, and the wafer is planarized prior to the CMOS transistor fabrication process. After completion of the CMOS process, the SOI microstructures are defined with a second DRIE step, followed by the removal of the sacrificial (buried) oxide. The SOI microstructures are left suspended from the walls of the isolation trench. Given the substantial preprocessing, wafer acceptance by CMOS foundries is an issue [10].

Thin-film polysilicon microstructures can also be cofabricated with CMOS electronics using a MEMS-first strategy. By forming the microstructural and sacrificial layers within a trench, then filling the trench with deposited oxide and planarizing the wafer surface using chemical-mechanical polishing (CMP), electronic circuitry can be fabricated afterwards on the wafer surface [12]. The trench is sealed with a nitride film to protect the MEMS structures during CMOS fabrication. In a different approach, selective silicon epitaxial growth is used to planarize the wafer after completion of the polysilicon MEMS structural and sacrificial layers, prior to standard CMOS processing [13]. Each of these approaches requires protection of the transistor structures during the final step of microstructure release etch in hydrofluoric acid.

In order to achieve complete "MEMS-first" modularity, the microstructures should be released and encapsulated prior to transistor fabrication. This goal has been

achieved recently by using low-pressure chemical vapor deposition (LPCVD) oxide or polysilicon films to seal release-etch access holes in a microshell cavity containing the microstructure [14]. Resonators encapsulated using this process have proven to be extremely stable [15], which indicates the suitability of wafer-level encapsulated MEMS for timing and high-performance inertial sensor applications. Microshell encapsulation was first demonstrated in the late 1980s using epitaxial silicon growth to seal a microresonator in a vacuum ambient [16], and a variety of approaches have been explored. Fig. 3 is a cross-sectional scanning electron microscopy (SEM) image of the edge of the sealed cavity. The microshell is formed by deposition in a silicon epitaxial growth reactor, which results in the simultaneous formation of epipolysilicon over the planarized microstructure area and SCS growth in the adjacent regions. The cavity sealing process requires high temperatures of 1000 °C or higher. As a result, the microstructure is annealed sufficiently to be unaffected by the thermal cycles of a modern CMOS process. In contrast to earlier MEMS-first processes, the MEMS fabrication, encapsulation, and vertical feedthrough fabrication processes are completely finished prior to the CMOS processing.

III. MEMS-LAST PROCESSES

The second approach in which surface micromachining of the structural layers occurs after completion of the CMOS back-end-of-line (BEOL) process steps, also known as the MEMS-last approach, offers a number of significant advantages. First, it is truly modular, making it compatible with any integrated circuit (IC) fabrication process. The MEMS module can be considered as a process option, similar to an additional thick metal layer for integrated passive components. Ideally, it should have as negligible an impact on the CMOS front-end process as would any additional interconnect layer, so that the circuit designs (cell libraries and IP blocks) do not need to be modified, for greater design flexibility and shorter design cycles. From a performance standpoint, the capability to stack the MEMS components on top of the electronic circuitry allows for minimal parasitics, resulting in lower power consumption and better sensitivity. Also, because of monolithic integration, robust modeling of interconnects becomes a very important benefit for proper matching needed in radio-frequency (RF) circuits to maximize yield and minimize the number of design cycles. From an architectural standpoint, the stacked configuration is particularly advantageous for arrays of MEMS devices, such as those used for storage [17] and display [18] applications. If the materials are CMOS-compatible and 200- or 300-mm process tools are available, the MEMS fabrication can be done by an extension of the CMOS line.

Fig. 4 illustrates the steps in a post-CMOS process flow that uses a damascene process—common in CMOS BEOL processes—to fabricate integrated microresonators [19]. The damascene approach is a typical way to leverage standard semiconductor manufacturing techniques for MEMS purposes, which is desirable when consolidating a CMOS and MEMS cofabrication process into one single flow. In this example, the dielectric defining the mold for back-end metallization is replaced by a sacrificial material, while the MEMS structural material is similarly deposited and planarized by CMP in lieu of interconnect metals. IBM Research has demonstrated copper microstructures with custom damascene CMOS BEOL layers for RF switch applications [20]. Both plasma-enhanced CVD (PECVD) diamond-like carbon and amorphous Si materials were

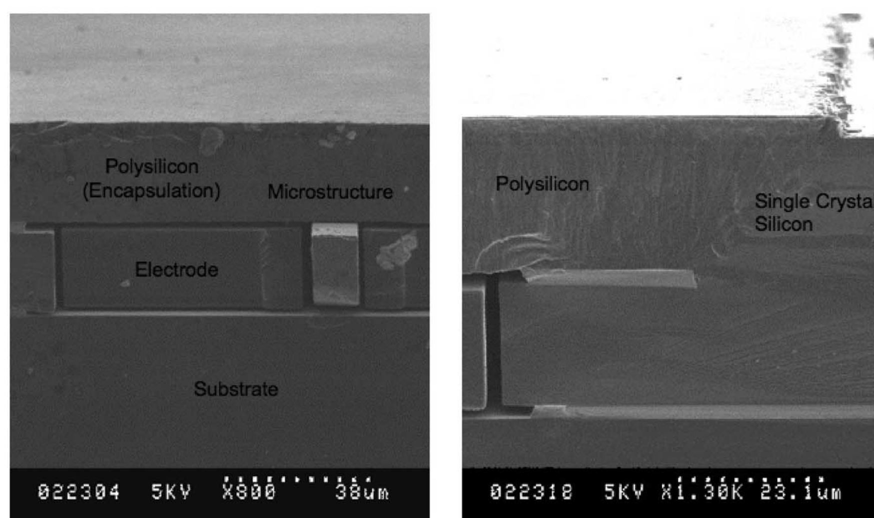


Fig. 3. ***Epipoly sealed microshell cavity cross section (courtesy of B. Kim and Prof. T. W. Kenny, Department of Mechanical Engineering, Stanford University).***

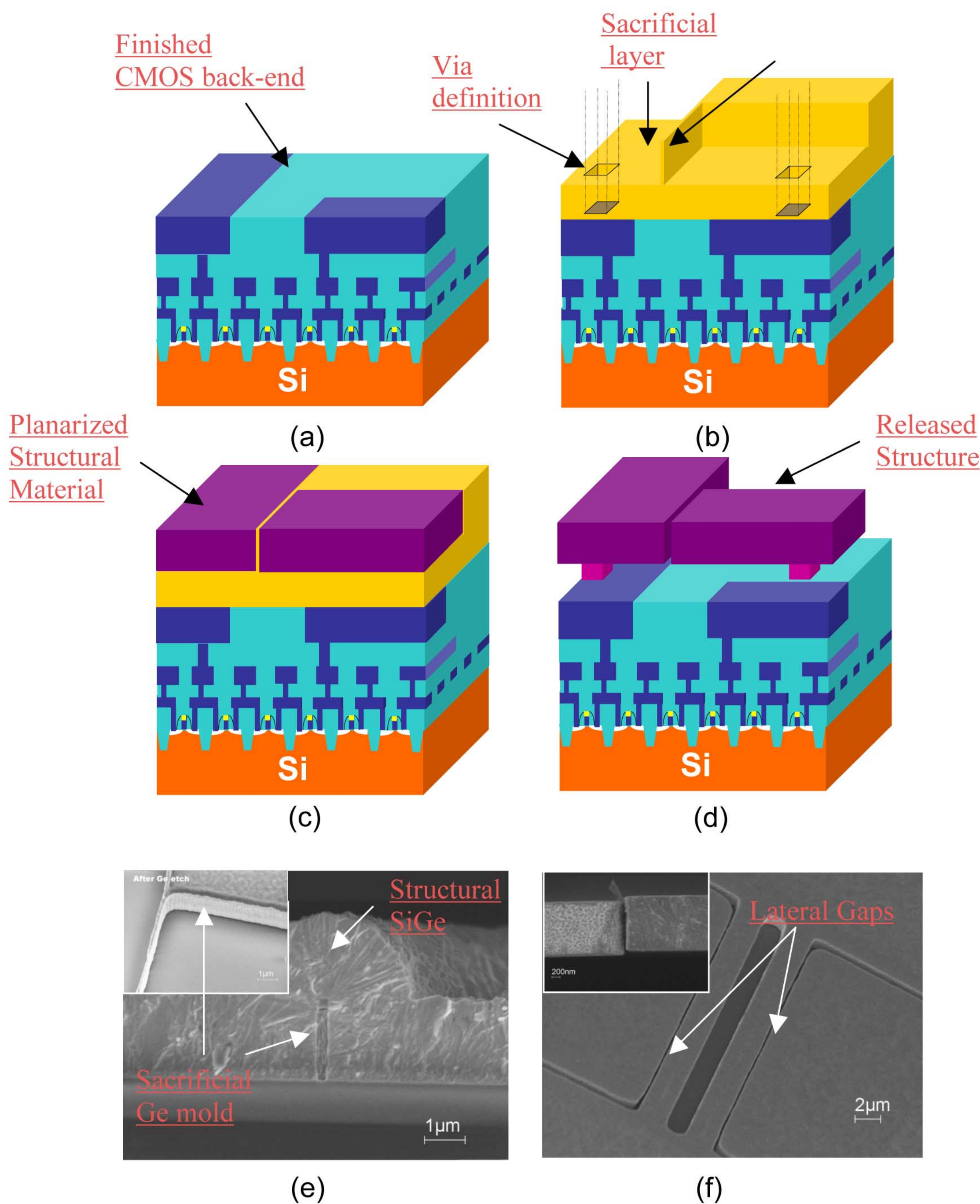


Fig. 4. ***(a)–(d) MEMS resonator fabrication based on dual-damascene process. (e) and (f) SEM pictures of poly-SiGe resonator fabricated using this process (from [19]).***

explored as sacrificial layers [21]. This approach minimizes surface topology and allows for many layers to be fabricated reliably, so long as stress in the accumulated layers is not problematic. For this reason, companies like MicroFabrica [22] are commercializing processes derived from the damascene approach for multilayered devices to enable cost-effective, modular prototyping of complex three-dimensional geometries using structural materials such as silver, copper, or nickel. The planar topology is also advantageous for microshell encapsulation of the microstructures.

The primary constraint for a post-CMOS MEMS process is the MEMS thermal process budget, which must be tolerated by the underlying electronic devices. This is a

challenging requirement, particularly if a modern CMOS process (technology node below 0.35 μm) is used. Although the transistors themselves can withstand significant thermal processing, the metal interconnects are impacted in terms of contact/via resistance and electromigration because of thermal stress and annealing effects. A thermal budget limit of 10 h at 425 °C for a standard 0.25-μm CMOS process has been demonstrated [23]; an earlier study showed that a 0.35-μm CMOS can tolerate up to 90 min at 525 °C [24]. In more advanced CMOS technologies, the low-permittivity dielectrics utilized in the metallization stack are less tolerant of postdeposition annealing. In the future, the divergence of CMOS technologies (mixed-signal processes using more standard dielectrics versus digital processes, where there is more aggressive use of low-k dielectrics to reduce parasitic capacitances) can pose very different thermal budget requirements for integration of MEMS.

Another constraint for a post-CMOS MEMS process stems from the fact that conventional CMOS passivation materials (PECVD SiN_x, polyimide) are etched by or are permeable to hydrofluoric acid, so that silicon dioxide is undesirable as a sacrificial material. Alternative sacrificial materials include photoresist, polyimide, germanium, and molybdenum, which can be selectively removed by an oxidizing agent, or molybdenum and amorphous silicon, which can be etched by xenon difluoride.

As is typically the case in MEMS, the choice of structural materials is dependent on the application. For example, inertial sensors require thick films with low strain gradients to minimize out-of-plane deflection upon release because of the large area required for the proof mass. Optical devices such as mirrors have stringent flatness specifications and, hence, require low-strain gradient structural layers with highly smooth surfaces. RF MEMS devices (movable capacitors, inductors, switches, and microresonators) require both high electrical conductivity and low residual tensile stress, among other properties. In the case of microresonators, a structural material with high intrinsic quality factor is highly desirable, meaning that thermoelastic damping and other losses should be low. Biological sensors having exposed surfaces must be fabricated from biocompatible materials. Because of these varied requirements, a variety of post-CMOS MEMS processes have been developed to meet the requirements of specific applications. From the perspective of defining a high-volume foundry post-CMOS MEMS integrated technology, however, it would be most cost-effective to develop a generic technology platform to support the maximum number of applications. Structural material requirements that are common to several applications are high fracture strength, resistance to creep, and low damping losses.

A. Metallic Structural Layers

Although they are considered inferior to silicon in terms of mechanical properties, metal-based structural materials present an attractive path for MEMS-last integration because of their low deposition temperature. Many metals are available in standard CMOS fabrication lines and are readily deposited at CMOS-compatible temperatures by sputtering, electrodeposition, or chemical vapor deposition. The most prominent example of a successfully commercialized MEMS-last technology is the digital light processor (DLP) technology developed by Texas Instruments.[2] The use of a large-scale-integrated array of addressable micromirror picture elements to project video images makes obvious the need for high-density interconnects and chip compactness; hence post-CMOS monolithic integration is highly desirable. For this application, the high optical reflectivity of aluminum is necessary for the reflecting surfaces of the deformable micromirrors [18]. A digital micromirror display (DMD) uses three layers of aluminum-based films for the mirror and its suspension system. The critical structural layers are specially developed amorphous aluminum alloys, which have demonstrated high reliability in long-term operation [25]. Polycrystalline alloys tried initially were found to suffer from long-term instabilities in their mechanical properties. Air-gap layers are formed between these metal layers when the sacrificial material is removed. The use of resist as a sacrificial layer is specific to metal surface-micromachining processes which employ very low deposition temperatures. Fig. 5 shows a closeup SEM view of the aluminum mirrors and underlying hinged yoke microstructure.

Among other examples of CMOS-compatible metal-based MEMS devices, electrodeposited nickel vibratory rate gyroscopes [26] and micromechanical resonators [27] are especially worthy of note. Nickel has a relatively high acoustic velocity, which is desirable for a microstructural material, and it can be electroplated at room temperature. When used for bulk-mode RF resonators, nickel has shown very high quality factors [27]. However, nickel was abandoned for the gyroscope application due to performance issues caused by the difference between its thermal expansion coefficient and that of the silicon substrate, as well as concerns about the long-term stability of its material properties [28]. As is true for all MEMS structural layers, the nickel deposition process must be highly reproducible and its effect on MEMS performance well understood for successful commercialization.

Gold has been used for RF-switch applications and has also been studied as a structural material for RF capacitors, inductors, and switches in duplexers and for frequency band switching.[3] Hard platinum alloys have been demonstrated as hysteresis-free flexural materials for micromirror suspensions [29]. Finally, although the material used has not been disclosed, Cavendish Kinetics is developing encapsulated metal switches for embedded

[2] http://www.dlp.com/.
[3] http://www.wispry.com/.

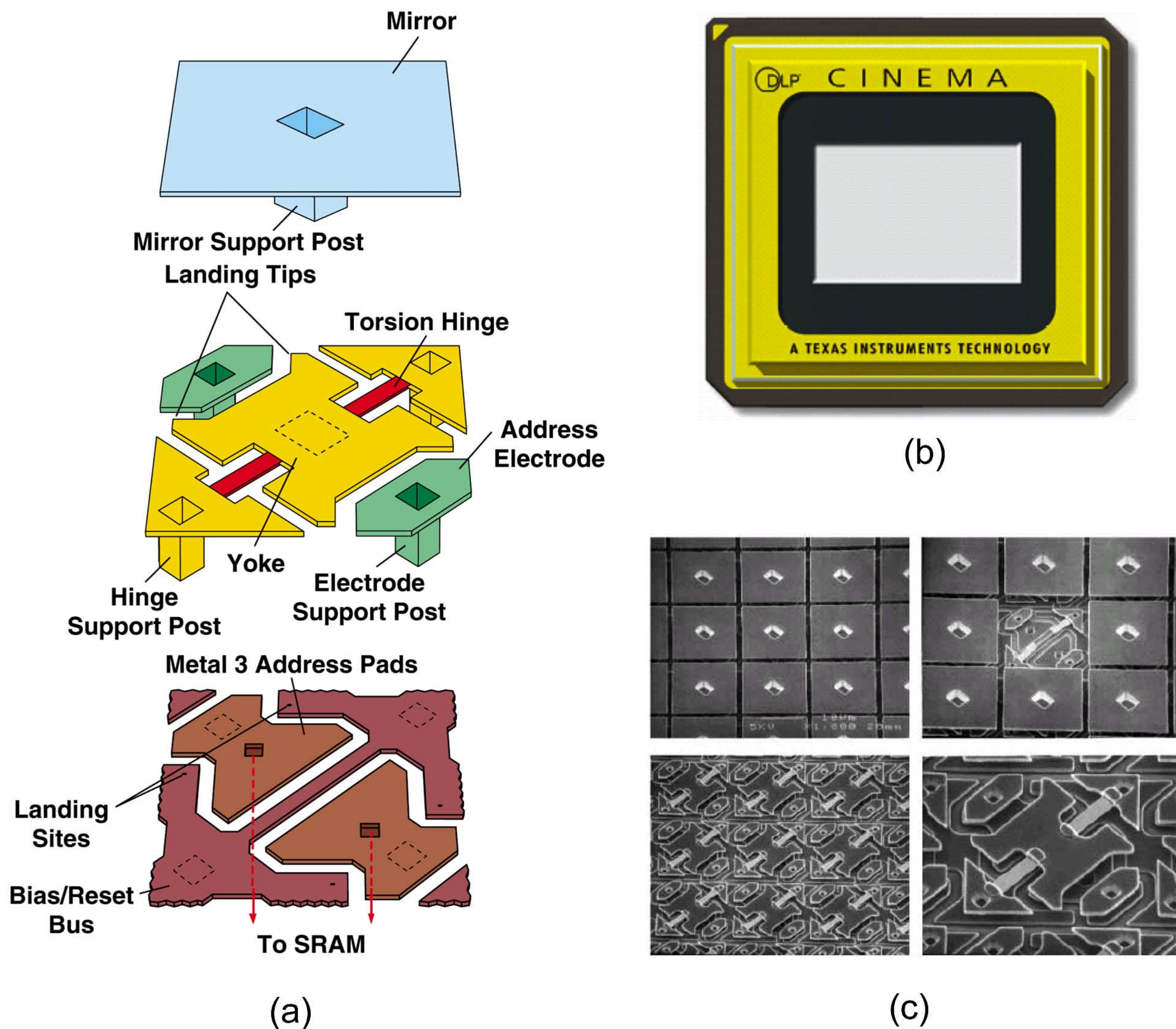


Fig. 5. ***(a) Schematic of the Texas Instruments DMD superstructure, (b) a packaged DLP, and (c) SEMs of a DMD structure (from http://www.dlp.com/).***

micromechanical memory devices[4] [30] (see Fig. 8). In this application, microcantilevers fabricated as a BEOL process on top of CMOS are used as memory elements. The "bits" are one-time programmable through the application of an electrostatic force pulling down the cantilever into a permanently adhered state.

B. Piezoelectric Materials

An emerging application for integrated MEMS technology is RF filters for transceiver front-ends. To replace quartz crystal and surface acoustic wave (SAW) mechanical filters, thin-film bulk acoustic resonators (FBARs), or bulk acoustic wave (BAW) resonators were introduced in the 1990s as standalone passive components. These devices utilize stacks of metal electrodes and piezoelectric material, such as aluminum nitride (AlN), to form vibrating mechanical elements with highly efficient transduction. The integration of BAW resonators directly on top of a SiGe BiCMOS stack to form a complete system-on-chip for wide-band code-division multiple-access applications was recently demonstrated [31]. The BAW was fabricated using ST Microelectronics' "above-IC" technology, in which AlN is integrated into the BEOL process. Fig. 6 shows a cross-sectional schematic view of an FBAR connected to the last (upper) metal layer (M5) on an IC chip [32]. The AlN is grown on an oriented platinum (Pt) electrode in order to achieve excellent piezoelectric properties. Zinc-oxide piezoelectric films are also compatible with CMOS processing, as demonstrated by an early integrated multisensor chip [33].

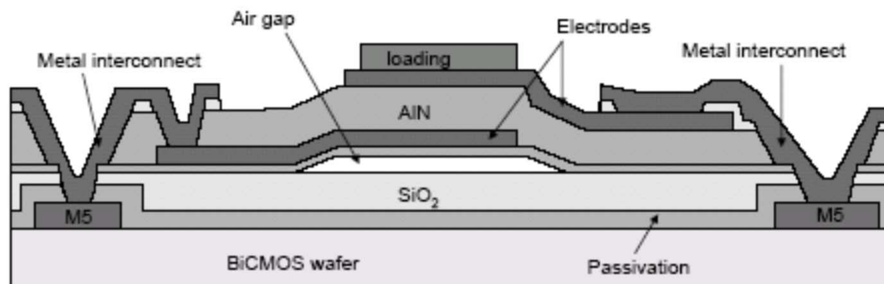
[4] http://www.cavendish-kinetics.com/.

C. Composite Amorphous Silicon-Metal Microstructures

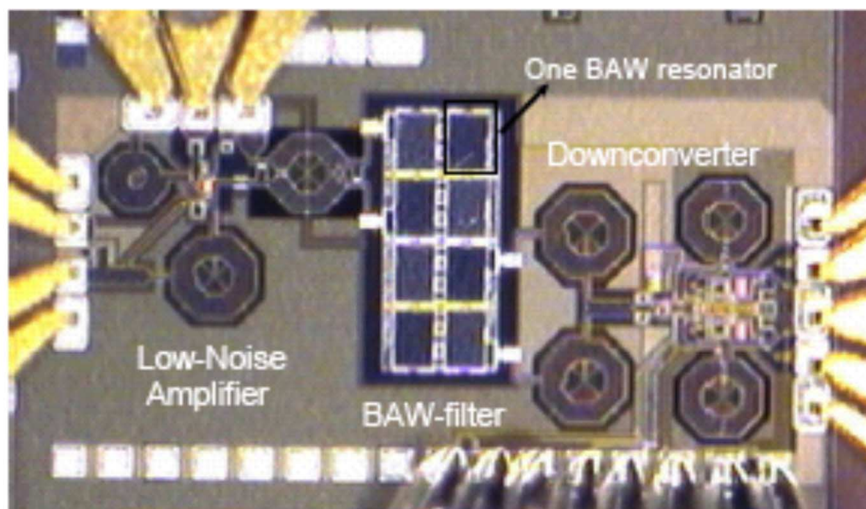
The first demonstration of integrated amorphous silicon microstructures was by Honer *et al.* in 2001 [34]. They showed that an amorphous silicon (a-Si) structural film with low tensile stress (<100 MPa) can be formed at low temperature (<350 °C, including postdeposition forming gas annealing) by optimizing the film deposition parameters. Because the sheet resistance of amorphous silicon is too high (in the tens of MΩ/square range), it was encapsulated with a thin layer of titanium-tungsten (TiW) for good electrical conductivity. The use of a metal/a-Si/metal stack for the structural layer dictates that the direction of actuation to be vertical (normal to the wafer surface). Integrated cantilevers and variable capacitors were successfully demonstrated (Fig. 7). Compatibility with silicon dioxide CMOS passivation was possible, due to the use of polyimide as the sacrificial material. The release etch was performed in oxygen plasma, which eliminates capillary-induced stiction. An alternative approach for low-temperature formation of amorphous silicon employs plasma-enhanced chemical vapor deposition (PECVD) [35], [36]. PECVD a-Si technology has been developed to fabricate thin-film transistors on plastic substrates at temperatures as low as 100 °C, making it very attractive for monolithic integration of MEMS with CMOS electronics. Phosphorus-doped hydrogenated a-Si (n+ a-Si:H) films are readily deposited using a mixture of the gaseous sources silane, hydrogen, and phosphine. The quality factor of amorphous silicon bending-mode resonators is high enough (up to 5000) that the material is potentially useful for timing applications [36].

D. Semiconducting Structural Materials

The experience and knowledge base for standalone surface-micromachined polycrystalline-silicon (poly-Si)



(a)



(b)

Fig. 6. *(a) Schematic of AlN resonator on top of CMOS and (b) micrograph of BiCMOS and above-IC BAW filter RF front-end (from [44]).*

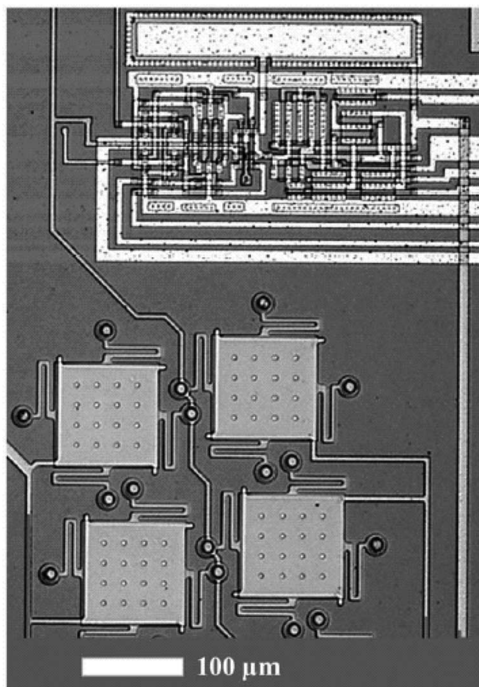


Fig. 7. *SEM picture of amorphous silicon variable capacitors with integrated detection circuitry [34].*

MEMS was an obvious target for modular integration. Due to its high deposition temperature, the CMOS back-end process was altered to withstand the high thermal budget required for poly-Si MEMS. Tungsten was extensively studied for interconnects because of its very high melting point, but it eventually proved to be problematic due to source/drain contact reliability [37], [38]. Also, the need for a customized CMOS process is a serious drawback to this integration approach. Another challenge for integration of polysilicon semiconductor layers into a CMOS backend process is forming low-resistance contacts to the underlying CMOS interconnect layers. Since the semiconductor layers are formed after the metal interconnects, techniques developed by the semiconductor industry, such as silicidation, which require moderately high process temperatures, cannot be readily employed to achieve low specific contact resistivity.

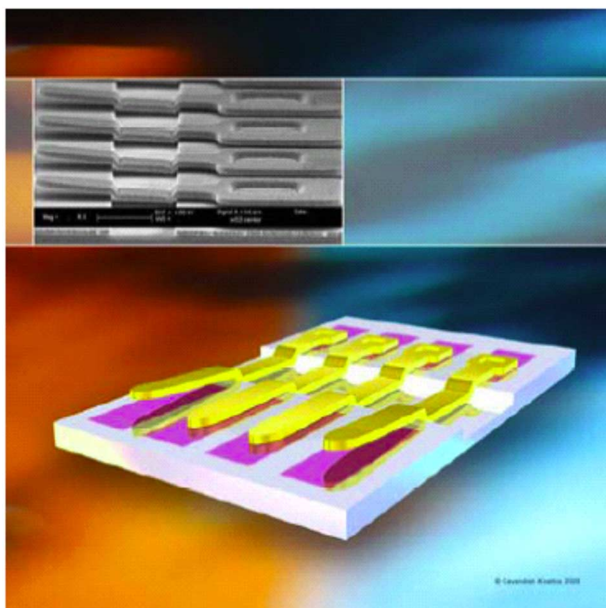


Fig. 8. *Cantilever device (microphotograph and schematic representation) for integrated nonvolatile memory (from [30]).*

E. Poly-Silicon-Germanium Alloys

Based on knowledge established by CMOS device researchers [39], polycrystalline germanium (poly-Ge) [40] and polycrystalline silicon-germanium (poly-SiGe) [41], [42] were introduced as MEMS structural materials in the late 1990s. Poly-SiGe has mechanical properties similar to those of poly-Si but can be formed with a much lower thermal process budget (below 450 °C for *in situ* p-type doped films with Ge content greater than 60%) so that it is compatible with standard CMOS processes. Work done at the University of California, Berkeley, focused on batch processing by conventional LPCVD of thin poly-SiGe films with thicknesses in the range from 1 to 5 μm. Germane (GeH_4) and silane (SiH_4) are the precursor gases of choice. *In-situ* boron doping is preferred because it enhances the deposition rate and can be achieved with diborane (B_2H_6) or boron tri-chloride (BCl_3) source gases. Integration of poly-SiGe microelectromechanical resonators on top of CMOS was soon demonstrated (see Fig. 9) [43]. Low-resistance contacts to the underlying CMOS interconnect layers can be achieved by optimizing the interconnect barrier layer material and predeposition cleaning process

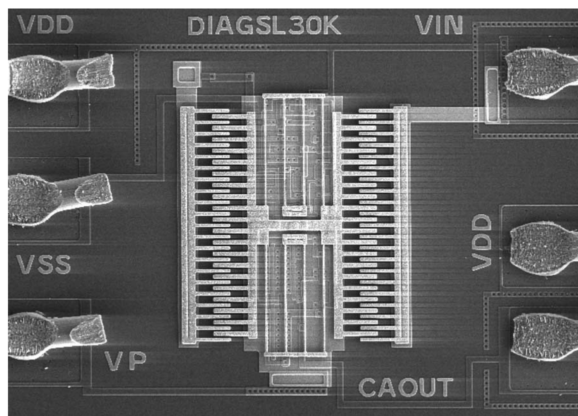


Fig. 9. *P+ poly-Si$_{0.35}$Ge$_{0.65}$ resonator fabricated on top of a CMOS amplifier with Al-Si(2%) metallization. Wires are bonded to the exposed Al-Si(2%) bond pads (from [43]).*

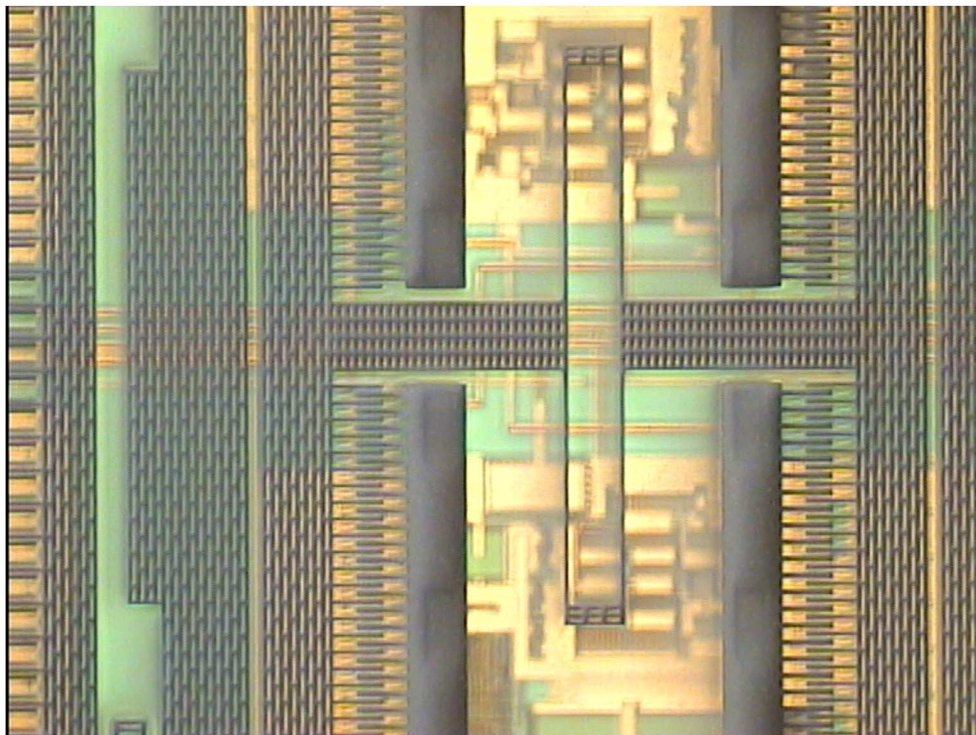


Fig. 10. ***Optical micrograph of an integrated gyroscope on top of 0.35 μm BiCMOS electronics (courtesy of A. Witrouw, IMEC).***

[44]. With a columnar grain structure and average grain size in the range of 200–500 nm (Fig. 9), LPCVD poly-SiGe shows great potential for RF high-Q resonator applications; $f - Q$ products well above 10^{12} were demonstrated [45].

An attractive feature of poly-SiGe is that its properties can be tuned by adjusting the Ge content. Germanium-rich films (>80% Ge) are readily etched in oxidizing solutions and plasmas. This makes pure germanium film the ideal sacrificial material because it can be selectively etched in hydrogen peroxide solution, leaving the CMOS passivation layers unaffected by the structural release step. Further optimization of LPCVD poly-SiGe processing is still needed to achieve the low residual stress and strain gradient required for display [46] and inertial sensors applications [47], however. Postdeposition annealing, ion implantation, and the use of a multilayered structural film are methods that can be used to reduce the overall strain gradient. Another option for achieving low strain gradient is simply to use a thicker structural film.

This approach was taken by researchers at IMEC who studied poly-SiGe films deposited by PECVD and successfully demonstrated the modular integration of a poly-SiGe MEMS gyroscope with 0.35-μm Philips BiCMOS technology [48] (see Fig. 10). The structural layer was a boron-doped poly-SiGe film, approximately 10 μm thick, grown at 450 °C and 2 torr for approximately 2 h. A silicon seed layer (~100 nm thick) was first deposited to eliminate the incubation time, followed by a CVD SiGe crystallization layer (~370 nm thick) to enhance the crystallinity of the PECVD layer, before the majority of the structural layer was grown by a high-deposition-rate PECVD process [49]. In an effort to further reduce the process thermal budget, PECVD SiGe films with deposition temperature of 210 °C and rate of 20 nm/min were recently demonstrated [50].

F. Other Structural Materials

An impressive early demonstration of MEMS-last integration was the 1000 element tactile sensing array demonstrated by researchers at Toyota Research in the late 1980s [51]. In order to release the silicon nitride touch-sensing membranes, a wet silicon anisotropic etch was used to remove a poly-Si sacrificial layer and form inverted pyramidal cavities in the substrate. Honeywell Research demonstrated an uncooled bolometer array in the 1990s using VO_x as the bolometric material deposited on thermal isolation microstructures fabricated after completion of the CMOS readout circuit [52].

Some applications require specific materials because of their unique mechanical or electronic transport properties, or their compatibility with fluids or biomaterials, as in the case of polymeric structural materials [53]. Another example is the use of carbon nanotube ribbons to form arrays of mechanical memory elements for embedded nonvolatile memory applications, due to their small size, resistance to wear and fatigue, and excellent electronic

transport properties. Nantero, Inc. has developed processes for positioning carbon nanotubes reliably on a large scale by treating them as a fabric that can be deposited using methods such as spin-coating, and then patterning them using conventional lithography and etching processes readily available in CMOS manufacturing lines [54]. The high-temperature synthesis of the carbon nanotubes is performed prior to spin-casting on the CMOS substrate. This strategy may be adaptable to other synthetic nanostructures with interesting electronic or electromechanical properties, such as nanowires and buckyballs.

IV. MEMS IN THE CMOS METALLIZATION STACK

A. MEMS in the BEOL CMOS Stack

Several different groups have developed MEMS made from the existing CMOS metal-dielectric interconnect stack. Early "integrated" MEMS for thermal sensing were made from metal-dielectric-polysilicon interconnect stacks similar to those used in CMOS [55]–[58]. The first true "CMOS MEMS" process flow of this genre was presented in 1988 [59], [60]. By stacking via-cuts and omitting the metal layer, openings in the dielectric stack were created down to the silicon substrate. A timed wet etch of the silicon resulted in released microstructures. Multiple electrically isolated metal layers, as well as gate and capacitor polysilicon, can be placed inside these microstructures. Applications included thermal micro-hotplates with embedded polysilicon heater resistors for chemical sensors [61], [62] and infrared detectors with polysilicon/aluminum thermopiles [63].

Via-cut stacking cannot be used to define etch pits in CMOS on wafers of diameter 8 in and greater, since such CMOS incorporates fixed-size tungsten plug vias. Post-CMOS reactive ion etching of the dielectric stack to define microstructures was introduced in 1996 [64]. This process, illustrated in Fig. 11(a), has been used on scaled CMOS down to the 0.18-μm technology node having both aluminum and copper interconnects [65]. By patterning with the union of all CMOS metal layers as the RIE mask, microstructures of different heights can be designed. Microstructures in this process can be made with lateral air gaps at the critical dimensions of the CMOS metallization. However, the dielectric RIE does have limitations with sidewall polymerization that needs to be controlled [66]. The low-gee accelerometer in Fig. 11(b) illustrates

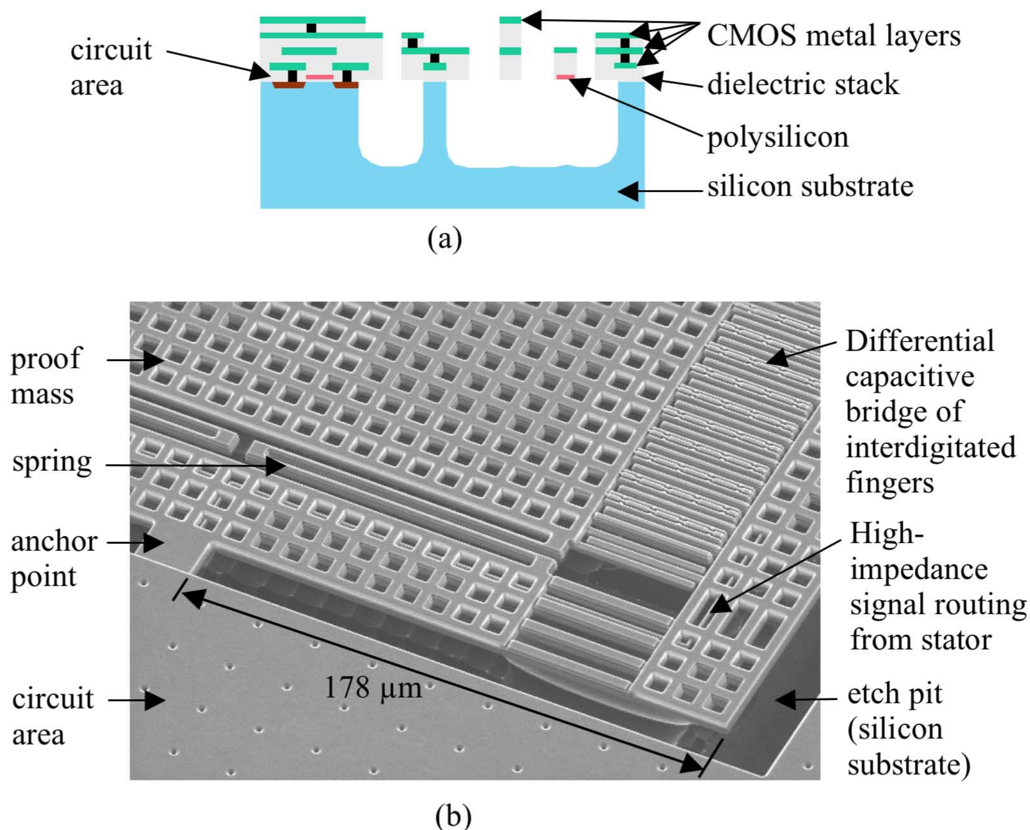


Fig. 11. *(a) Metal-masked CMOS MEMS cross-section. (b) A low-gee lateral-axis accelerometer micromachined after 0.35-μm CMOS fabrication [65].*

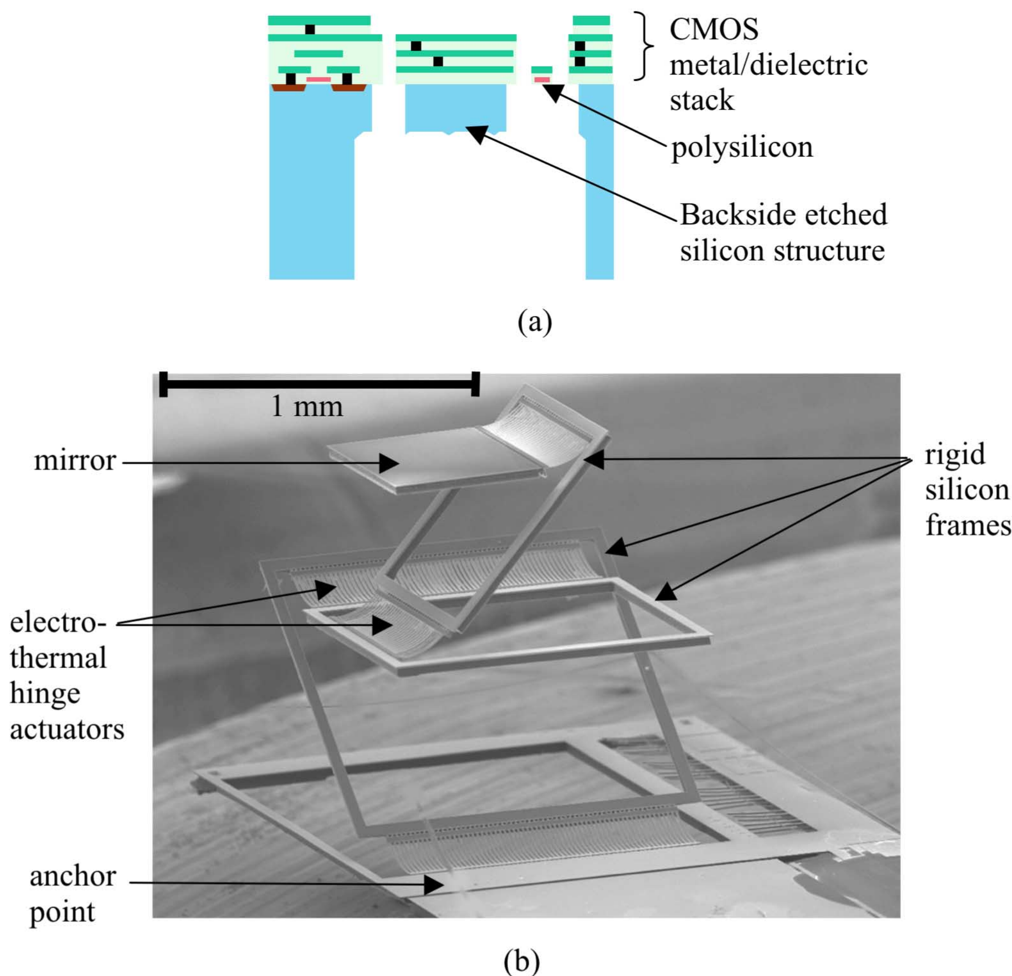


Fig. 12. *A bulk silicon CMOS-MEMS process. (a) Cross section. (b) Optical scanner example [79]. Four electrothermal hinge actuators provide piston and two-axis tilt motion of the mirror. (SEM courtesy of H. Xie, University of Florida).*

the reduction in out-of-plane curl achieved due to low residual stress gradients in 8-in wafer diameter CMOS processes [67]. A variation of this process uses a photoresist mask on 0.35-μm CMOS wafers. Similar processes are now offered by multiproject prototyping service providers[5] [68]. The MEMSIC thermal tilt sensor products are commercial examples of this kind of CMOS MEMS technology.

Several related processes have been developed that exploit other combinations of the CMOS BEOL layers. Microfluidic channels made in the BEOL dielectric layers were accomplished with a post-CMOS wet aluminum etch [69]. Microstructures were created out of the multiple aluminum layers while utilizing the vias as structural posts [70]. The sacrificial top oxide layers were etched in buffered hydrofluoric acid (HF) with isopropyl alcohol (IPA) as an additive to provide etch selectivity over the aluminum. Submicrometer-width cantilevers were made from the gate polysilicon by post-CMOS direct write laser lithography to pattern a metal liftoff pattern, followed by RIE of the polysilicon and released with a timed sacrificial oxide etch [71].

B. Bulk Silicon CMOS MEMS

The CMOS silicon substrate can also be incorporated into microstructures. Silicon n-well regions have been made into microstructures using a silicon electrochemical etch (ECE) stop. An initial use of front-side ECE in CMOS created a silicon n-well suspended by the aluminum interconnect [72]. Electrically and thermally isolated vertical bipolar transistors were located in the well and connected as p-n junctions to form temperature sensors. A more recent example of front-side ECE in CMOS resulted in a suspended thermally isolated resistor array for infrared detection [73]. Backside through-wafer ECE has also been used to create infrared imagers [74] and resonant cantilevers for gravimetric chemical sensing using electrothermal [75] and electromagnetic actuation [76]. The latter devices have been fully integrated into a series of systems

[5]See http://www.memscap.com; http://www.cmp.imag.fr/; http://www.cic.org.tw; http://www.memsic.com.

on chip with signal amplification, sampling, and analog-to-digital conversion [77].

Silicon DRIE was used more recently to make bulk silicon CMOS MEMS, as illustrated in Fig. 12(a) [78]. Front-side dielectric RIE defined etch pits to the substrate. A subsequent timed backside DRIE thinned the CMOS chip, in most cases to a 25-μm target thickness. The final front-side silicon RIE created high-aspect-ratio structures where the CMOS BEOL layers were used for routing. The most mature use for the process is in electrothermal micromirrors, such as the optical scanner in Fig. 12(b) [79]. Using a DRIE process flow, a silicon-on-glass in-plane capacitive accelerometer with CMOS interface circuitry was realized [80]. The front side of the CMOS substrate with transducer and electronics was aligned and bonded to a glass substrate patterned with recesses. The CMOS backside was then chem-mechanically polished to a 120-μm thickness followed by through-wafer silicon DRIE to form the proof mass, suspension, and capacitive comb fingers.

C. Adding Polymer Materials to BEOL CMOS MEMS

These various CMOS MEMS processes may be augmented by adding materials before or after the micromachining release steps while addressing the low-temperature constraint and issues with subsequent microstructural integrity. Gold or platinum electrode metallization with connection to the CMOS aluminum is important for biological and chemical sensing. This step can be accomplished through a series of intermediate zincation and nickel electroless plating steps [81] by direct electroless gold deposition without intermediate steps [82] or by sputtering of metal films. The latter method was used to create a DNA detector array of 8 × 16 biomodified gold electrodes integrated with capacitive measurement control circuitry, array decoding and analog-to-digital conversion [83]. Polymers to form chemically sensitive layers for gravimetric detection have been deposited onto cantilevers by spray coating with shadow masks [84] and drop casting [85]. In another approach, polymer dissolved in solvent may be ink-jetted into a delivery well adjacent to a grooved cantilever, as shown in Fig. 13 [86]. Through capillary action, the solvent wicks into the groove and leaves polymer deposited onto the cantilever without affecting neighboring air gaps used for electrostatic actuation and sensing.

Membranes for microphones and microspeakers have been made by first defining a suspended skeleton mesh made from the CMOS BEOL metal and dielectric layers [87]. Both PECVD and vapor-deposited polymer coatings were successfully applied to seal the mesh to form the membrane. Backside vent holes were etched with DRIE to improve acoustic system compliance. Fig. 14 is a single-chip microphone with signal conditioning circuitry from Akustica, Inc. that is made in this technology.[6] The SEM in Fig. 14(c) is a fractured cross-section that shows the skeletal mesh along with the air gap to the silicon backplate.

[6]http://www.akustica.com.

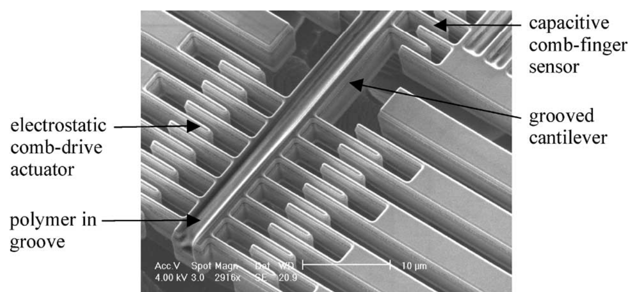


Fig. 13. *The end of a 120-μm-long 4-μm-wide 5-μm-tall CMOS-MEMS cantilever with a 2-μm-wide groove down its axis [85]. Polystyrene filled the groove by wicking up the cantilever axis starting at its base.*

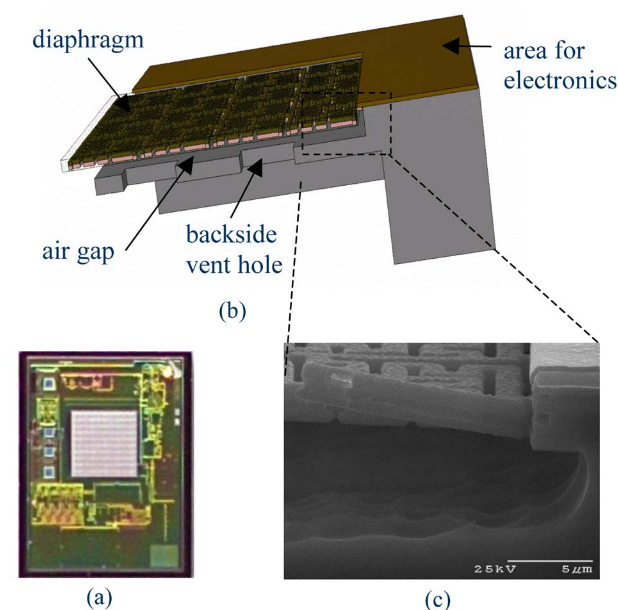


Fig. 14. *Single-chip CMOS-MEMS microphone. (a) Schematic cross section. (b) Die photo. (c) Cross-section of skeletal mesh (courtesy of K. J. Gabriel, Akustica, Inc.).*

V. CONCLUSIONS

Integration of MEMS and electronics is desirable for some applications. However, most successful MEMS products are currently not integrated on a single chip with electronics. For these products, multichip solutions represent an economically and technically viable solution. Such MEMS are usually made in a custom process flow, which has led to a so-called "MEMS law" of "one process, one product." Contrary to this dictum, a handful of manufacturers, such as Analog Devices, have made multiple integrated MEMS products with a single process. The

eventual maturation of modular CMOS MEMS processes is expected to widen the occurrence of multiple products from single processes and eventually make integrated MEMS a financially viable offering from foundries.

Integration is possible using various modular processing strategies, with complementary tradeoffs involving the overall fabrication cost and device quality. Overall manufacturing cost remains the driving factor in commercialization of integrated solutions. The large majority of MEMS applications today do not require integration with state-of-the-art CMOS electronics. The choice of CMOS technology node will be at the lowest cost that is available, reliable, and compatible with the chosen integration approach. Electronics foundry availability is problematic for bulk silicon MEMS pre-CMOS processing; the low-temperature constraint for above-CMOS MEMS films presents a challenge to obtaining high mechanical quality with good electrical contacts; and MEMS made in the CMOS BEOL metal/dielectric stack is constrained by the mechanical properties inherited from the electronics foundry. Nevertheless, each of these MEMS process options shows promise for making a commercial impact. Missing thus far is the adoption of one of these processes by a major foundry to establish it as a *de facto* standard. However, having the CMOS and MEMS processing done in a single foundry may not be necessary for emerging modular pre-CMOS and post-CMOS MEMS technologies. For example, some CMOS MEMS multiproject prototyping services use two foundries: first conventional CMOS, then a MEMS foundry. Currently, the most common technology nodes used for MEMS integration are 0.5-μm (6-in-diameter wafers) and 0.35-μm CMOS (8-in wafers). The continued obsolescence of older CMOS technology nodes may force CMOS integration efforts to migrate to more advanced nodes having substantial volume and lower cost. Tooling compatibility is a competing issue as more advanced CMOS is made on 8-in or larger diameter wafers, while current MEMS foundries are generally configured to handle 4- to 6-in-diameter wafers.

Overall, the MEMS-last approach may offer the greatest flexibility and reliability. University research efforts have proven the feasibility of this approach, and recent developments have been made by companies and large industrial laboratories. Several startup companies are relying on this approach to develop timing and embedded memory products, for which density and small chip size are economically desirable.

Integrated MEMS process flows will continue to evolve, with an increased emphasis on manufacturability and reliability. Concepts from above-CMOS processing, CMOS BEOL MEMS processing, and bulk silicon processing may be combined to form new kinds of structures and capabilities. Techniques evolving from the refinement of system-in-package processing, such as wafer thinning and through-wafer vias for chip stacking, are expected to commingle with MEMS processing to spawn new generations of integrated MEMS. Although beyond the scope of this paper, heterogeneous integration using batch transfer or self-assembly technologies may become a viable alternative to integration by cofabrication; however, more research and development is needed to establish the manufacturability of these processes. ■

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