EE214
Advanced Analog Integrated Circuit Design

- Winter 2011 -

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Table of Contents

Chapter 1	**Introduction**
Chapter 2	**BJT Devices**
Chapter 3	**MOS Devices and G_m/I_D-based Design**
Chapter 4	**Review of Elementary Circuit Configurations**
Chapter 5	**Two-Port Feedback Circuit Analysis**
Chapter 6	**Frequency Response of Feedback Circuits**
Chapter 7	**Wideband Amplifiers**
Chapter 8	**Noise Analysis**
Chapter 9	**Distortion Analysis**
Chapter 10	**Opamps and Output Stages**

Chapter 1

Introduction

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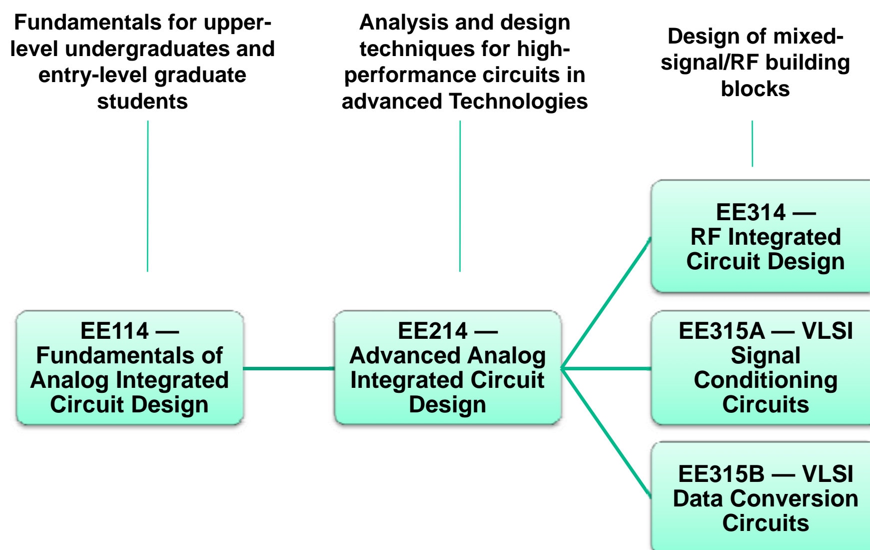
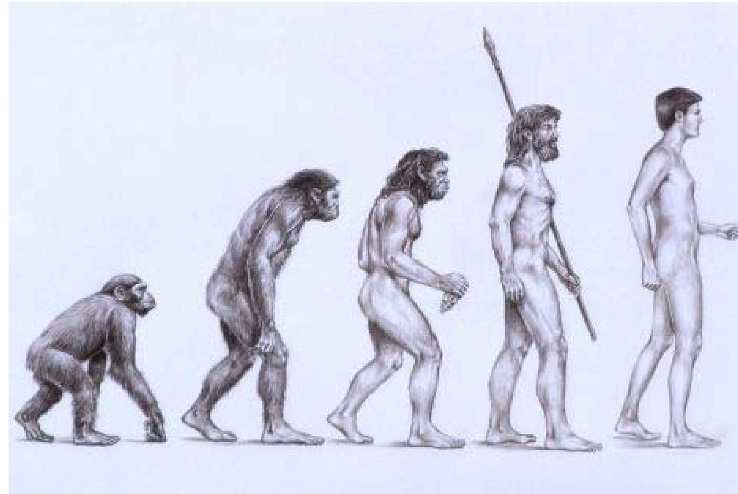
Analog Circuit Sequence

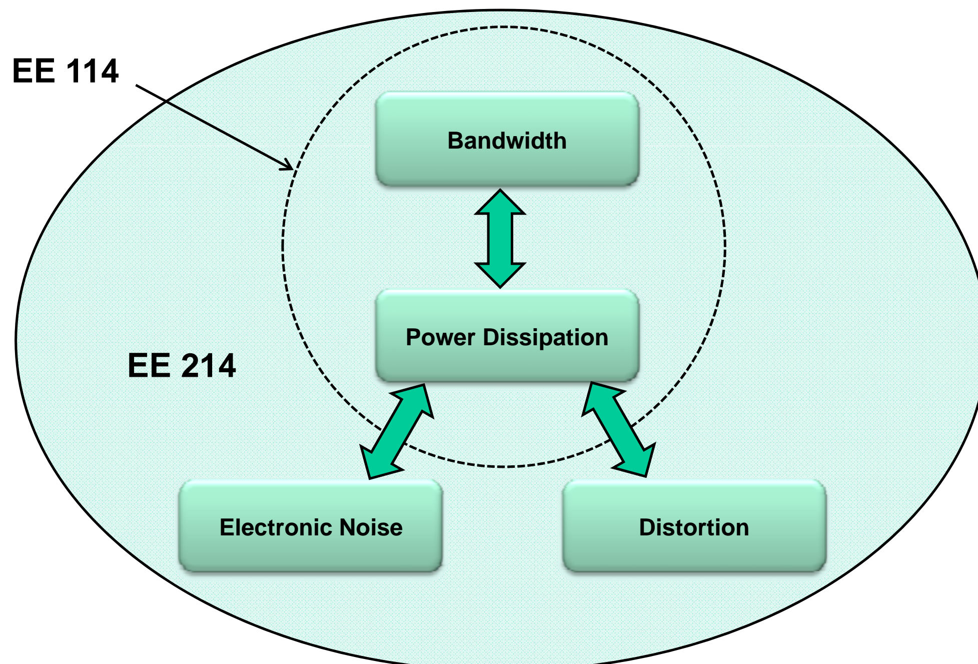


The Evolution of a Circuit Designer…

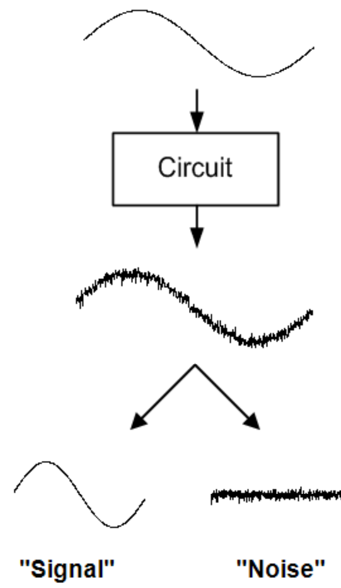


EE101A,B **EE114** **EE214** **EE314 EE315A,B**

Analog Design



Significance of Electronic Noise (1)



Signal-to-Noise Ratio

$$SNR = \frac{P_{signal}}{P_{noise}} \propto \frac{V_{signal}^2}{V_{noise}^2}$$

Significance of Electronic Noise (2)

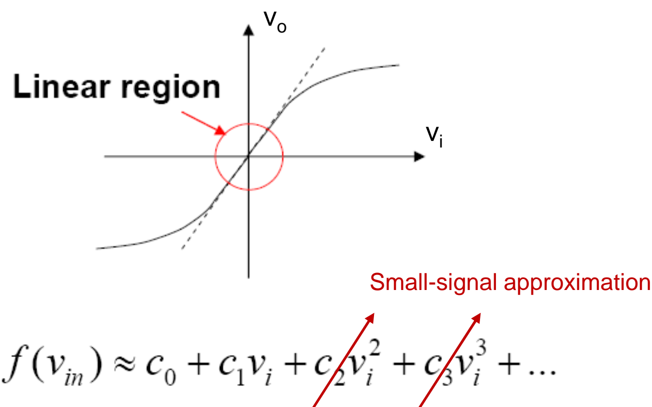
Example: Noisy image

http://www.soe.ucsc.edu/~htakeda/kernelreg/kernelreg.htm

Significance of Electronic Noise (3)

- The "fidelity" of electronic systems is often determined by their SNR
  - Examples
    - Audio systems
    - Imagers, cameras
    - Wireless and wireline transceivers
- Electronic noise directly trades with power dissipation and speed
  - In most circuits, low noise dictates large capacitors (and/or small R, large g_m), which means high power dissipation
- Noise has become increasingly important in modern technologies with reduced supply voltages
  - $SNR \sim V_{signal}^2/V_{noise}^2 \sim (\alpha V_{DD})^2/V_{noise}^2$
- Designing a low-power, high-SNR circuit requires good understanding of electronic noise

Distortion



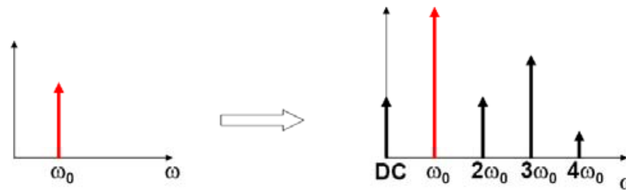
Small-signal approximation

$$v_o = f(v_{in}) \approx c_0 + c_1 v_i + c_2 v_i^2 + c_3 v_i^3 + \ldots$$

- All electronic circuits exhibit some level of nonlinear behavior
  - The resulting waveform distortion is not captured in linearized small-signal models
- The distortion analysis tools covered in EE214 will allow us to quantify the impact of nonlinearities on sinusoidal waveforms

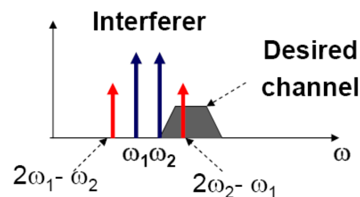
Significance of Distortion

- For a single tone input, the nonlinear terms in a circuit's transfer function primarily result in signal harmonics



- For a two-tone input, the nonlinear terms in a circuit's transfer function result in so-called "intermodulation products"

Example: Two interferer tones create an intermodulation product that corrupts the signal in a desired (radio-) channel

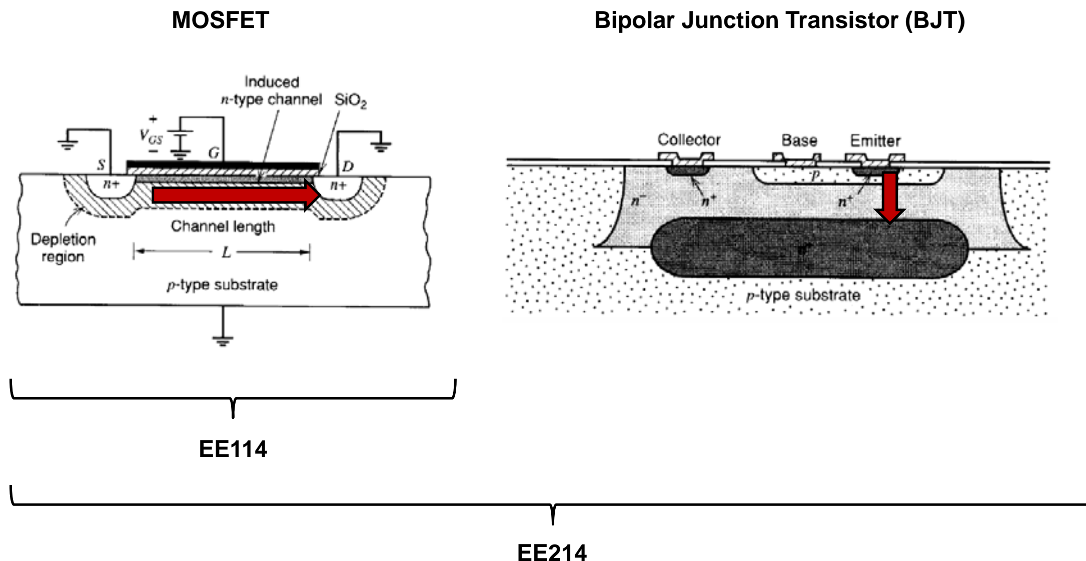


Noise and Distortion Analysis in EE214

- Main objective
  - Acquire the **basic** tools and intuition needed to analyze noise and distortion in electronic circuits
  - Look at a few specific circuit examples to "get a feel" for situations where noise and/or distortion may matter

- Leave application-specific examples for later
  - EE314: Noise and distortion in LNAs, mixers and power amplifiers
  - EE315A: Noise and distortion in filters and sensor interfaces
  - EE315B: Noise and distortion in samplers, A/D & D/A converters

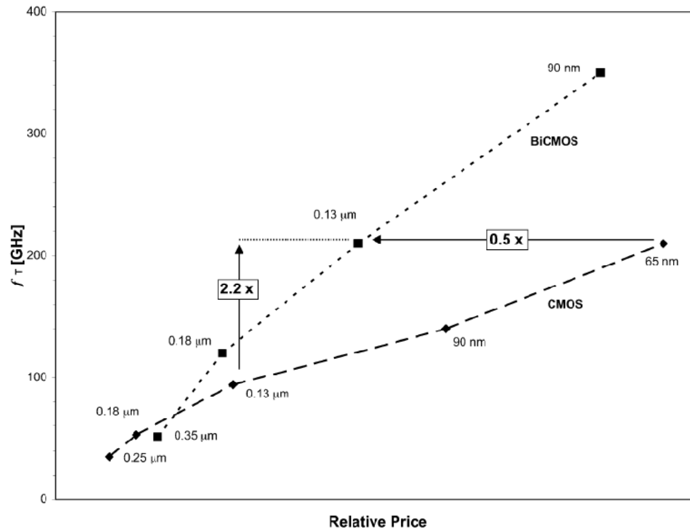
Technology



Bipolar vs. CMOS (1)

- Advantages of bipolar transistors
  - Lower parametric variance
  - Higher supply voltages
  - Higher intrinsic gain ($g_m r_o$)
  - Higher f_T for a given feature size/lithography
- Disadvantages of bipolar transistors
  - Lower integration density, larger features
  - Higher cost

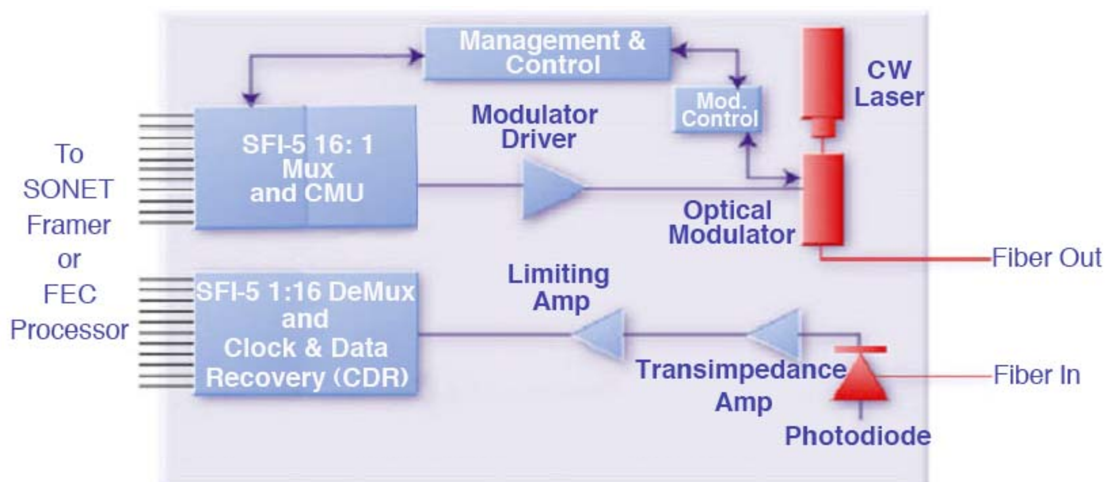
Bipolar vs. CMOS (2)



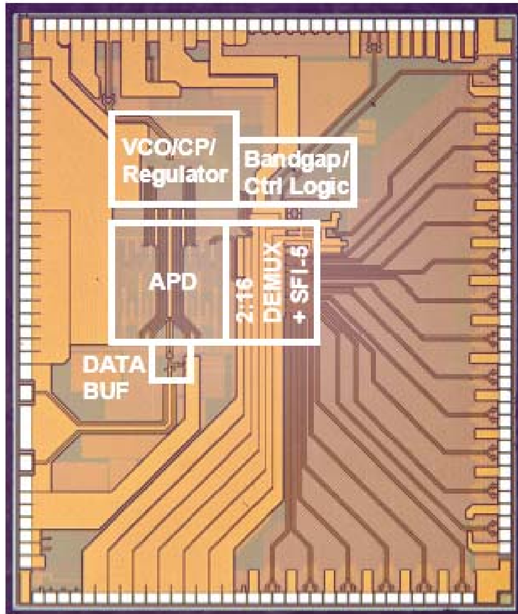
A.J. Joseph, et al., "Status and Direction of Communication Technologies - SiGe BiCMOS and RFCMOS," *Proceedings of the IEEE*, vol.93, no.9, pp.1539-1558, September 2005.

- CMOS tends to require finer lithography to achieve same speed as BiCMOS process with advanced BJT

Example that Leverages High-Speed BJTs: 40Gb/s Integrated Optical Transponder



Die Photo of 40Gb/s CDR Circuit *



- 120-GHz f_T / 100GHz f_{max} 0.18μm SiGe BiCMOS
- 144 pins
- 3.5mm x 4.2mm
- +1.8V and –5.2V supplies
- 7.5W power dissipation

* A. Ong, et al., ISSCC 2003

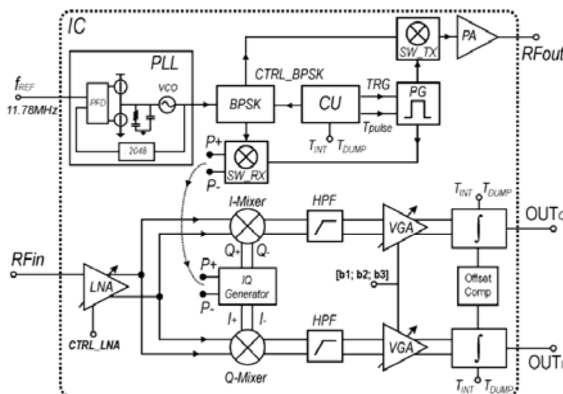
Radar Sensor

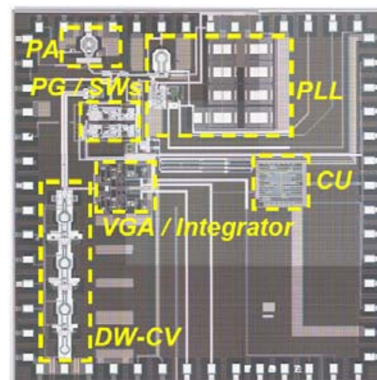
1. Collision warning and mitigation
2. Pre-crash sensing
3. Blind spot detection
4. Parking aid
5. Adaptive Cruise Control (ACC)

BiCMOS process

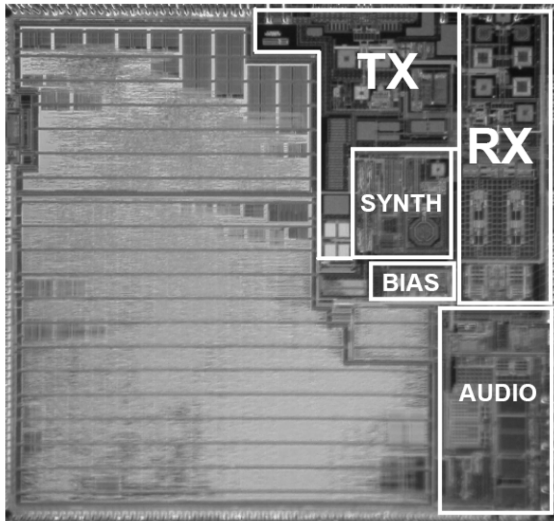
- 0.13-μm CMOS core (1.2/2.5V)
- 1.7V BV_{CEO} SiGe HBT
- 166/175GHz f_t/f_{max}
- 6 metal layers (1 thick)
- Capacitors MIM (2 fF/μm^2)
- Spiral PGS inductors

Ragonese et al., ISSCC 2009





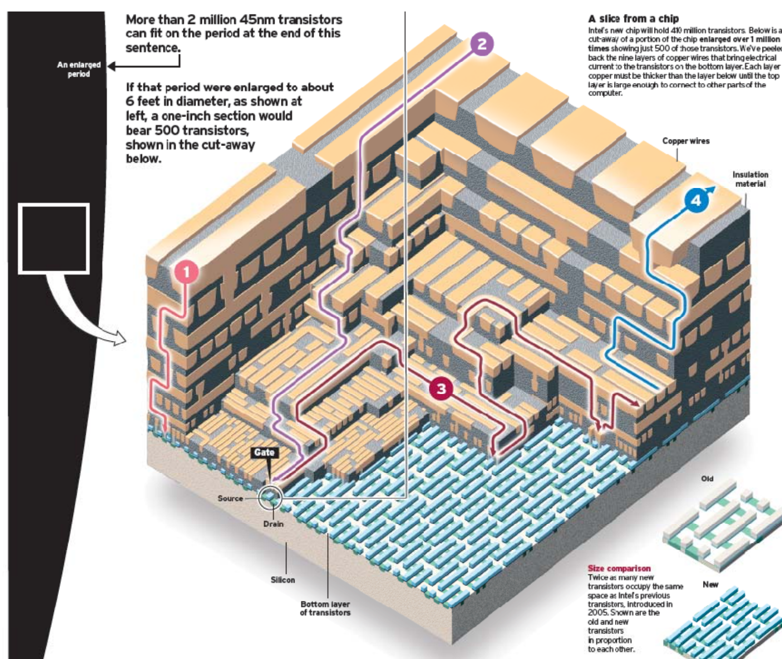
Example that Leverages Densely Integrated CMOS: RF Transceiver System-on-a-Chip (SoC)



Mehta et al., "A 1.9GHz Single-Chip CMOS PHS Cellphone," ISSCC 2006.

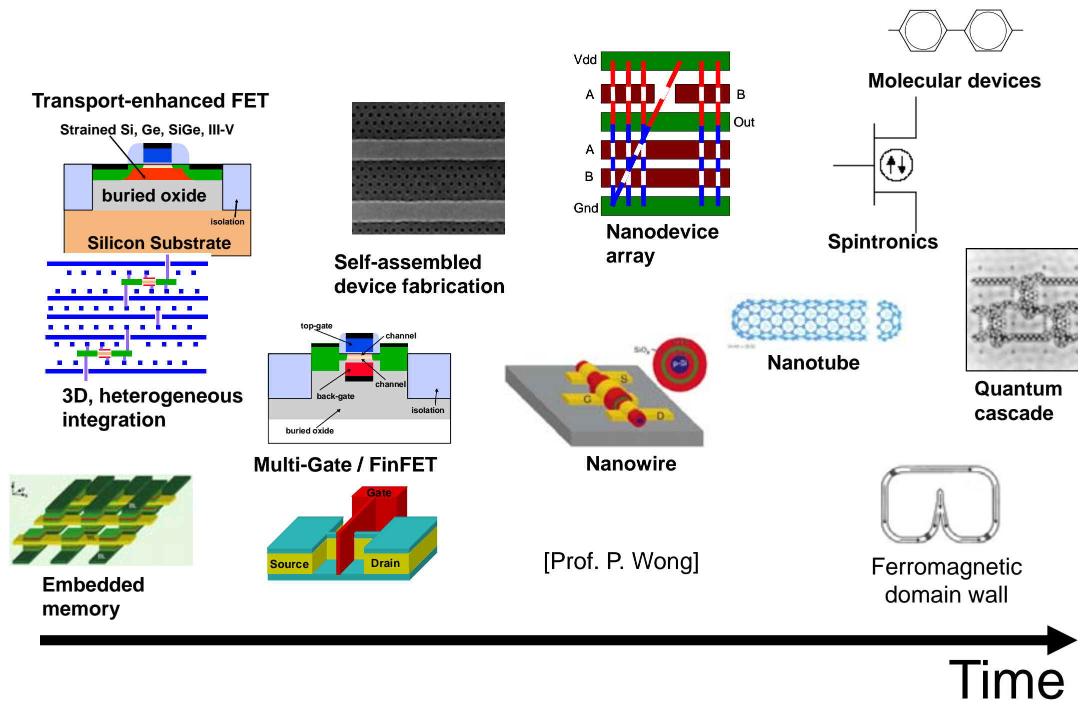
- In modern CMOS technology, millions of logic gates can be integrated on a chip
  - Together with moderate- to high performance analog blocks

45nm CMOS (Intel)



Steve Cowden
THE OREGONIAN
July 2007

Research in Device Technology



Thoughts on Device Technology

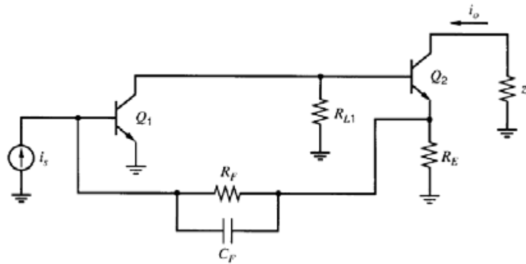
- In the future, innovative circuit designers must embrace "whichever" technology is most suitable (in terms of performance, cost, reliability, etc. for their specific problem
  - Regardless of the respective I-V law and associated nonidealities

- In EE214, we will use bipolar **and** MOS technology to illustrate the similarities and differences between two advanced technologies
- The device parameters and simulation models of the "EE214 technology" correspond to a modern 0.18-µm SiGe BiCMOS technology
  - See e.g. S. Wada, et al., "A manufacturable 0.18-um SiGe BiCMOS technology for 40-Gb/s optical communication LSIs," in *Proc. 2002 Bipolar/BiCMOS Circuits and Technology Meeting, pp. 84–87.*

Analysis of Feedback Circuits

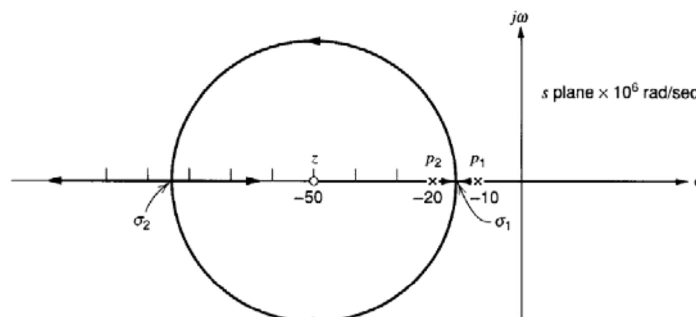
- Feedback circuits can be studied in several ways
  - Return ratio analysis (EE114)
  - Two-port analysis (EE214)
- Both methods have their own merits and demerits, and a good circuit designer should understand both approaches
- Two-port analysis nicely captures a number of practical scenarios in which the forward amplifier ("a") and feedback network ("f") can be intuitively identified and separated (while maintaining loading effects)
  - Shunt-shunt, shunt-series, series-shunt, series-series configurations

Example:
Shunt-series feedback circuit



Root Locus Techniques

- Provides intuitive guidance on "where the poles move" when the loop gain is varied
- Valuable for stability analysis and frequency compensation



Course Outline

- BJT & short channel MOS device models
- Review of elementary amplifier stages (BJT focus)
- Two-port feedback circuit analysis
- Root locus
- Wideband amplifiers
- Noise analysis
- Distortion analysis
- OpAmps and output stages

Summary of Learning Goals

- Understand device behavior and models for transistors available in advanced integrated circuit technologies
  - SiGe BJT, short channel MOS
- Acquire the basic intuition and models for
  - Distortion analysis
  - Noise analysis
  - Two-port feedback circuit analysis
  - Root locus techniques and their application to broadband amplifiers
- Solidify the above topics in a hands-on project involving the design and optimization of a broadband amplifier circuit

Staff and Website

- Instructors
  - Boris Murmann, Drew Hall
- Teaching assistants
  - Kamal Aggarwal, Pedram Lajevardi
- Administrative support
  - Ann Guerra, CIS 207
- Lectures are televised
  - But please come to class to keep the discussion interactive!
- Web page: http://ccnet.stanford.edu/ee214
  - Check regularly, especially bulletin board
  - Register for online access to grades and solutions

Text and Prerequisites

- EE214 Course reader
  - Hardcopies available at Stanford Bookstore (~1/3)
- Required textbook
  - Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., Wiley
- Reference text
  - B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2002
- Course prerequisite: EE114 or equivalent
  - Basic device physics and models
  - Frequency response, dominant pole approximation, ZVTC
  - Biasing, small-signal models
  - Common source, common gate, and common drain stages
  - Port impedance calculations
  - Feedback basics

Assignments

- Homework (20%)
  - Handed out on Wed, due following Wed in class
  - Lowest HW score will be dropped
  - Policy for off-campus students
    - Fax or email to SCPD before deadline stated on handout
- Midterm Exam (30%)
- Design Project (20%)
  - Design of an amplifier using HSpice (no layout)
  - Work in teams of two
  - OK to discuss your work with other teams, but no file exchange!
- Final Exam (30%)

Honor Code

- Please remember you are bound by the honor code
  - We will trust you not to cheat
  - We will try not to tempt you
- But if you are found cheating it is very serious
  - There is a formal hearing
  - You can be thrown out of Stanford
- Save yourself a huge hassle and be honest
- For more info
  - http://www.stanford.edu/dept/vpsa/judicialaffairs/guiding/pdf/honorcode.pdf

Chapter 2
Bipolar Junction Transistors

B. Murmann

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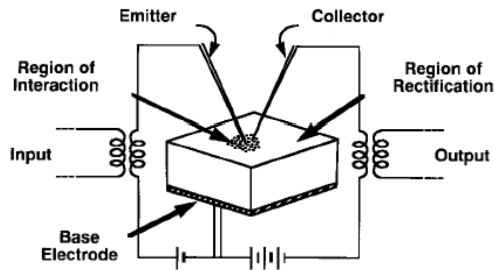
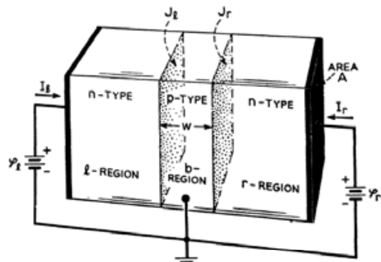
Reading Material: Sections 1.1, 1.2, 1.3, 1.4, 2.5, 2.6, 2.7, 2.11, 2.12

History

Bardeen, Brattain, and Shockley, 1947

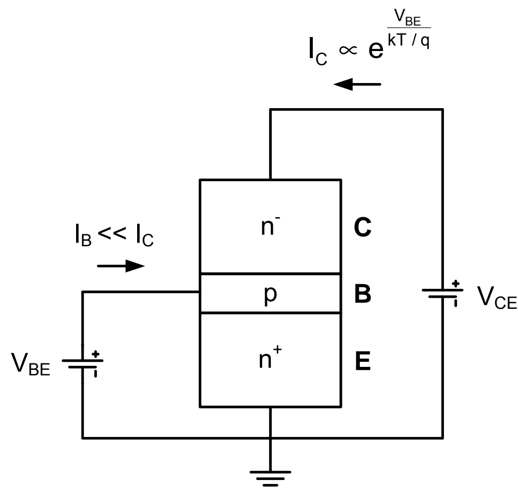


W. Brinkman, D. Haggan, and W. Troutman, “A history of the invention of the transistor and where it will lead us,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1858-1865, Dec. 1997.



W. Shockley, M. Sparks, and G. K. Teal, “P-N junction transistors,” *Phys. Rev. 83,* pp. 151–162, Jul. 1951.

Conceptual View of an NPN Bipolar Transistor (Active Mode)

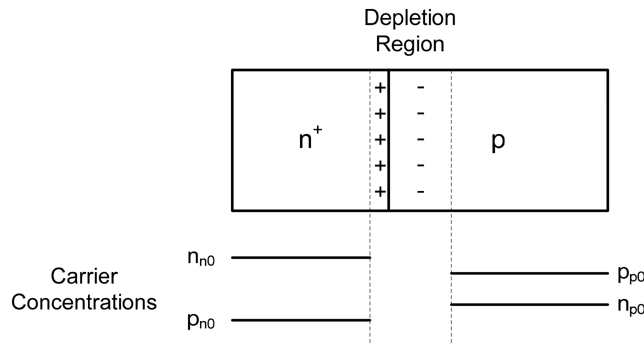


- Device acts as a voltage controlled current source
  - V_{BE} controls I_C
- The base-emitter junction is forward biased and the base-collector junction is reverse biased
- The device is built such that
  - The base region is very thin
  - The emitter doping is much higher than the base doping
  - The collector doping is much lower than the base doping

Outline of Discussion

- In order to understand the operation principle of a BJT, we will look at
  - The properties of a forward biased pn^+ junction
  - The properties of a reverse biased pn^- junction
  - And the idea of combining the two junctions such that they are joined by a very thin (p-type) base region
- The treatment in the following slides is meant to be short and qualitative
  - See any solid-state physics text for a more rigorous treatment (involving band diagrams, etc.)

pn+ Junction in Equilibrium (No Bias Applied)



$$n_{n0} \cong N_D \quad \text{(Donor concentration)}$$

$$p_{p0} \cong N_A \quad \text{(Acceptor concentration)}$$

$$n_{p0} = \frac{n_i^2}{p_{p0}} \cong \frac{n_i^2}{N_A}$$

$$p_{n0} = \frac{n_i^2}{n_{n0}} \cong \frac{n_i^2}{N_D}$$

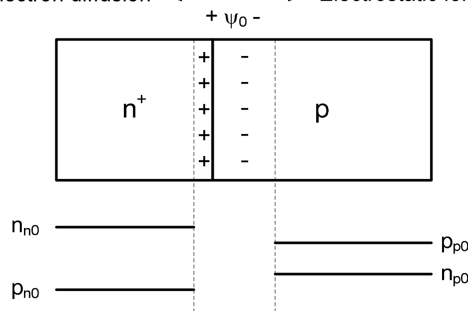
n_n Concentration of electrons on n side (majority carriers)
p_n Concentration of holes on n side (minority carriers)
n_p Concentration of electrons on p side (minority carriers)
p_p Concentration of holes on p side (majority carriers)

The subscript “0” in the carrier concentrations denotes equilibrium (no bias applied)

Built-in Potential

Electrons “want” to diffuse → ← Holes “want” to diffuse

Electrostatic force preventing electron diffusion ← → Electrostatic force preventing hole diffusion

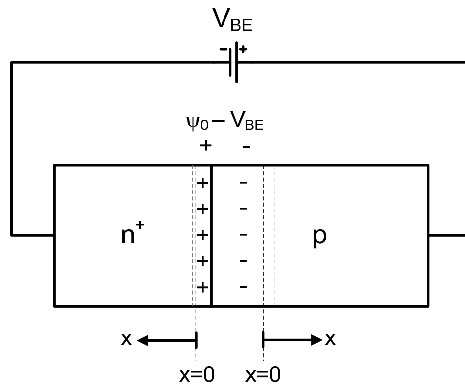


- The built in potential sets up an electric field that opposes the diffusion of mobile holes and electrons across the junction

$$\text{(Drift)} \quad q\mu_p pE = qD_p \frac{dp}{dx} \quad \text{(Diffusion)}$$

$$\Rightarrow \psi_0 = V_T \ln\left(\frac{p_{p0}}{p_{n0}}\right) = V_T \ln\left(\frac{n_{n0}}{n_{p0}}\right) \cong V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \qquad V_T = \frac{kT}{q}$$

pn⁺ Junction with Forward Bias (1)



- Depletion region narrows, diffusion processes are no longer balanced by electrostatic force
- At the edge of the depletion region (x=0), the concentration of minority carriers [$n_p(0)$] can be computed as follows

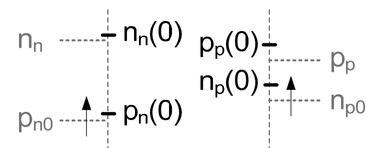
$$\psi_0 - V_{BE} = V_T \ln\left(\frac{n_n}{n_p(0)}\right) \cong V_T \ln\left(\frac{N_D}{n_p(0)}\right) \qquad \therefore n_p(0) = \frac{N_D}{e^{\frac{\psi_0}{V_T}}} \cdot e^{\frac{V_{BE}}{V_T}} = n_{p0} e^{\frac{V_{BE}}{V_T}} \cong \frac{n_i^2}{N_A} e^{\frac{V_{BE}}{V_T}}$$

pn+ Junction with Forward Bias (2)

- The result on the previous slide shows that forward biasing increases the concentration of electrons at the “right” edge of the depletion region by a factor of $\exp(V_{BE}/V_T)$
- The same holds for holes at the “left” edge of the depletion region

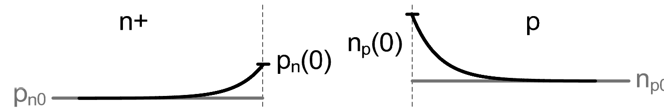
$$p_n(0) = p_{n0} \cdot e^{\frac{V_{BE}}{V_T}} \cong \frac{n_i^2}{N_D} \cdot e^{\frac{V_{BE}}{V_T}}$$

- Since $N_D >> N_A$, it follows that $p_n(0) << n_p(0)$, i.e. the concentration of minority carriers is much larger at the lightly doped edge
- Since there must be charge neutrality in the regions outside the depletion region, the concentration of the majority carriers at the edge of the depletion region must also increase
  - However, this increase is negligible when $n_p(0) << p_p \cong N_A$ (or $p_n(0) << n_n \cong N_D$)
  - These conditions are called “low-level injection”

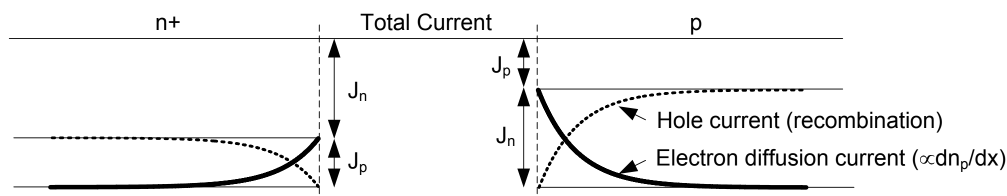


What Happens with the Injected Minority Carriers?

- The carriers would "like" to diffuse further into the neutral regions, but quickly fall victim to recombination
- The number of minority carriers decays exponentially, and drops to 1/e of the at the so-called diffusion length (L_p or L_n, on the order of microns)



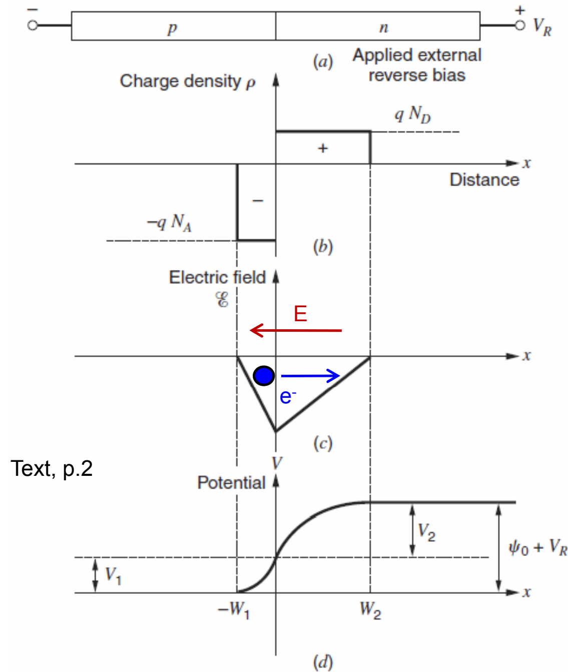
- In each region, there are now two types of currents
  - Diffusion of injected minority carriers due to non-zero dn_p/dx (or dp_n/dx)
  - Majority carrier currents for recombination



Summary – Forward Biased pn+ junction

- Lots of electrons being injected into the p-region, not all that many holes get injected into the n^+ region
  - The heavier n-side doping, the more pronounced this imbalance becomes
- The electrons injected in the p region cause a diffusion current that decays in the x-direction due to recombination
- The recombination necessitates a flow of holes to maintain charge neutrality; as the diffusion current decays, the hole current increases, yielding a constant current density along the device
- Near the edge of the depletion region, the electron diffusion current dominates over the hole current that supplies carriers for recombination
  - This is a very important aspect that we will come back to

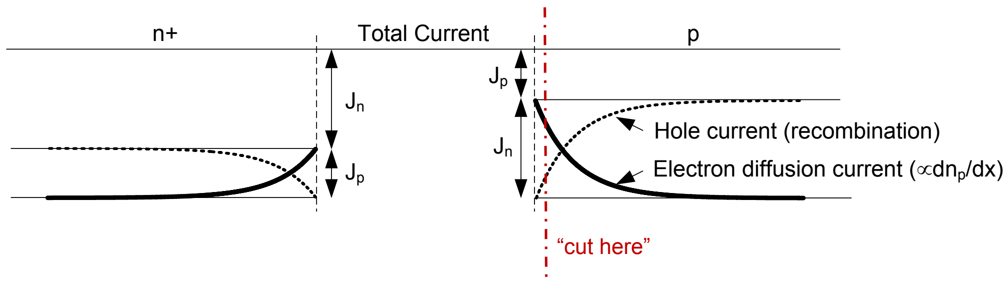
Reverse Biased pn^- Junction



Text, p.2

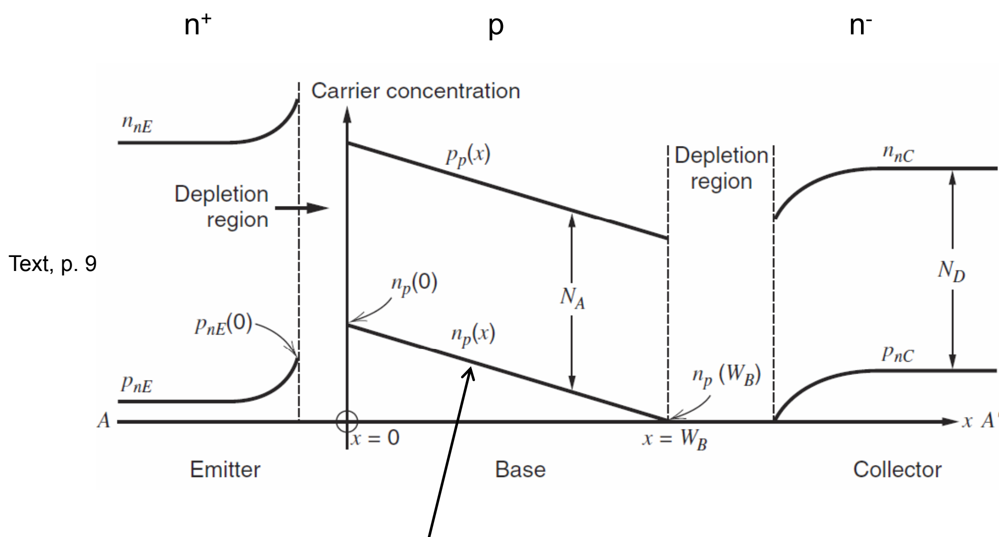
- Reverse bias increases the width of the depletion region and increases the electric field
- Depletion region extends mostly into n^- side
- Any electron that would "somehow" make it into the depletion region will be swept through, into the n-region
  - Due to electric field

Bipolar Junction Transistor – Main Idea



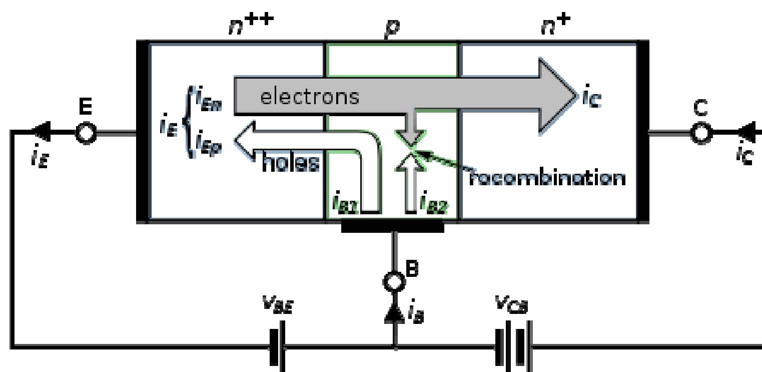
- Make the p-region of the pn^+ junction <u>very</u> thin
- Attach an n^- region that will "collect" and sweep across most of the electrons before there is a significant amount of recombination

Complete Picture



Straight line because base is thin; negligible recombination ("short base" electron profile)

BJT Currents



http://en.wikipedia.org/wiki/Bipolar_junction_transistor

- Primary current is due to electrons captured by the collector
- Two (undesired) base current components
  - Hole injection into emitter (→ 0 for infinite emitter doping)
  - Recombination in the base (→ 0 for base width approaching zero)

First-Order Collector Current Expression

$$J_n = qD_n \frac{dn_p(x)}{dx} \cong -qD_n \frac{n_p(0)}{W_B}$$ Current density

$$I_C \cong qAD_n \frac{n_p(0)}{W_B}$$ A is the cross-sectional area

W_B is the base width

$$n_p(0) \simeq \frac{n_i^2}{N_A} e^{\frac{V_{BE}}{V_T}}$$ Result from slide 7

$$\therefore I_C \cong \frac{qAD_n n_i^2}{W_B N_A} e^{\frac{V_{BE}}{V_T}}$$

$$\therefore I_C \cong I_S e^{\frac{V_{BE}}{V_T}} \qquad I_S = \frac{qAD_n n_i^2}{W_B N_A}$$

Base Current

$I_B = I_{B1} + I_{B2}$ where I_{B1} = Recombination in the base

I_{B2} = Injection into the emitter

I_{B1} follows from dividing the minority carrier charge in the base (Q_e) by its "lifetime" (τ_B)

$$I_{B1} = \frac{Q_e}{\tau_b} = \frac{\frac{1}{2} n_p(0) W_B qA}{\tau_b} = \frac{1}{2} \frac{W_B qA n_i^2}{\tau_b N_A} e^{\frac{V_{BE}}{V_T}}$$

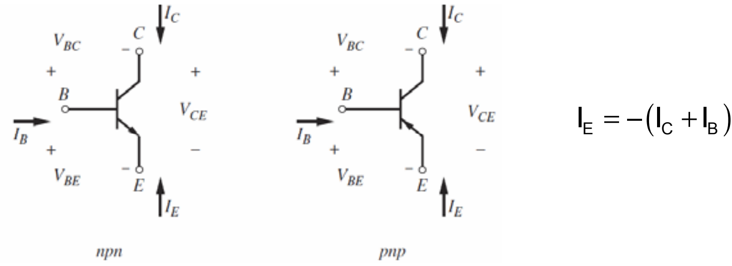
I_{B2} depends on the gradient of minority carriers (holes) in the emitter. For a "long" emitter (all minority carriers recombine)

$$I_{B2} = -qAD_p \left.\frac{dp_n(x)}{dx}\right|_{x=0} = -qAD_p \left[\frac{d}{dx} \left(\frac{n_i^2}{N_D} e^{\frac{V_{BE}}{V_T}} e^{-\frac{x}{L_p}} \right) \right]_{x=0} = \frac{qAD_p}{L_p} \frac{n_i^2}{N_D} e^{\frac{V_{BE}}{V_T}}$$

In modern narrow-base transistors $I_{B2} >> I_{B1}$.

Terminal Currents and Definition of α_F, β_F

Text, p. 9



$$I_E = -(I_C + I_B)$$

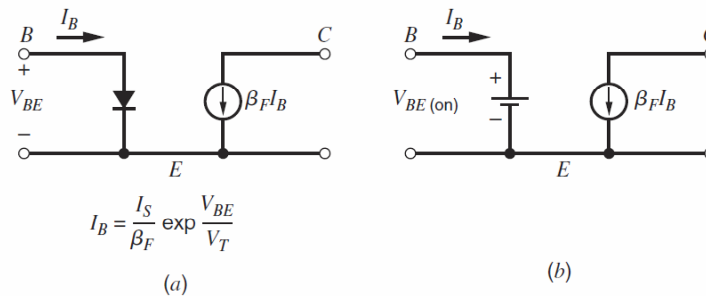
$$\beta_F \triangleq \frac{I_C}{I_B} \quad \text{(ideally infinite)}$$

$$\alpha_F \triangleq \frac{I_C}{(-I_E)} = \frac{\beta_F}{1+\beta_F} \quad \text{(ideally one)}$$

- The subscript “F” indicates that the device is assumed to operate in the forward active region (BE junction forward biased, BC reverse biased, as assumed so far)
  - More on other operating regions later…

Basic Transistor Model

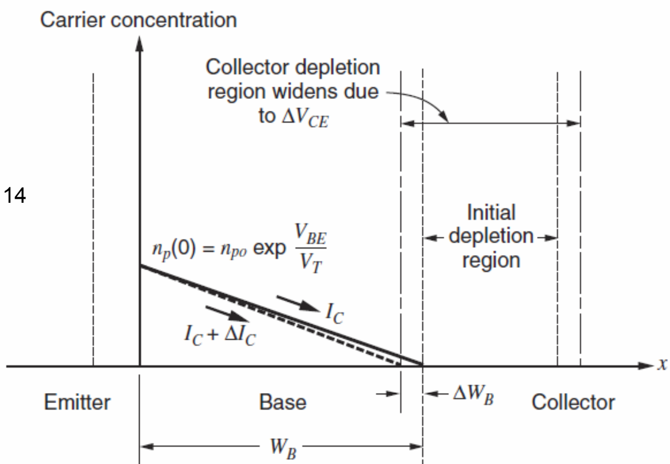
Text, p. 13



Simplified model; very useful for bias point calculations (assuming e.g. $V_{BE(on)}$ = 0.8V)

Basewidth Modulation (1)

Text, p. 14



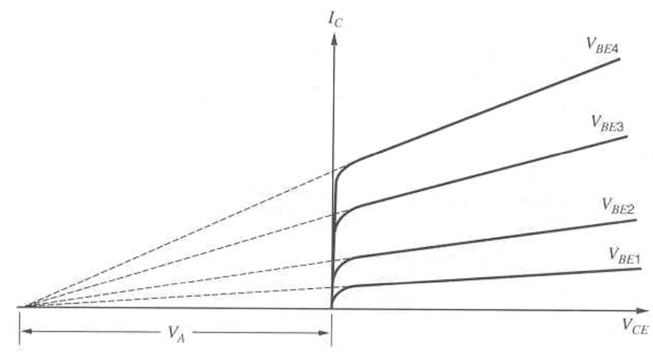
Side note:
BJT inherently has better (higher) r_o than MOS since lower doping on n-side (collector) has most of the depletion region inside the collector

$$\frac{\partial I_C}{\partial V_{CE}} = \frac{\partial}{\partial V_{CE}} \left(\frac{qAD_n n_i^2}{W_B(V_{CE}) \cdot N_A} e^{\frac{V_{BE}}{V_T}} \right) = -\frac{I_C}{W_B} \frac{dW_B}{dV_{CE}}$$

(See eq. (1.18) for dW_B/dV_{CE} term)

Early Voltage (V_A)

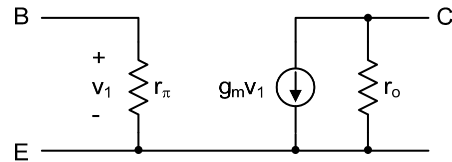
Text, p. 15



$$V_A \triangleq \frac{I_C}{\frac{\partial I_C}{\partial V_{CE}}} = -\frac{W_B}{\frac{dW_B}{dV_{CE}}} = \text{const.} \quad \text{(independent of } I_C\text{)}$$

$$\boxed{I_C \cong I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)}$$

Small-Signal Model



$$g_m = \frac{dI_C}{dV_{BE}} = \frac{d}{dV_{BE}} I_S e^{\frac{V_{BE}}{VT}} = \frac{I_C}{V_T}$$

$$g_\pi = \frac{1}{r_\pi} = \frac{dI_B}{dV_{BE}} = \frac{d\left(\frac{I_C}{\beta_F}\right)}{dV_{BE}} = \frac{1}{\beta_F}\frac{I_C}{V_T} = \frac{g_m}{\beta_F} \quad (\text{assuming } \beta_F = \text{const.})$$

$$g_o = \frac{1}{r_0} = \frac{dI_C}{dV_{CE}} = \frac{d}{dV_{CE}}\left[I_S e^{\frac{V_{BE}}{V_T}}\left(1 + \frac{V_{CE}}{V_A}\right)\right] \cong \frac{I_C}{V_A}$$

Intrinsic Gain

$$g_m r_o \cong \frac{I_C}{V_T} \cdot \frac{V_A}{I_C} = \frac{V_A}{V_T} \qquad V_T \cong 26\text{mV} \quad (\text{at room temperature})$$

- In the EE214 technology, the SiGe npn device has V_A = 90V, thus

$$g_m r_o \cong \frac{90\text{V}}{26\text{mV}} = 3460$$

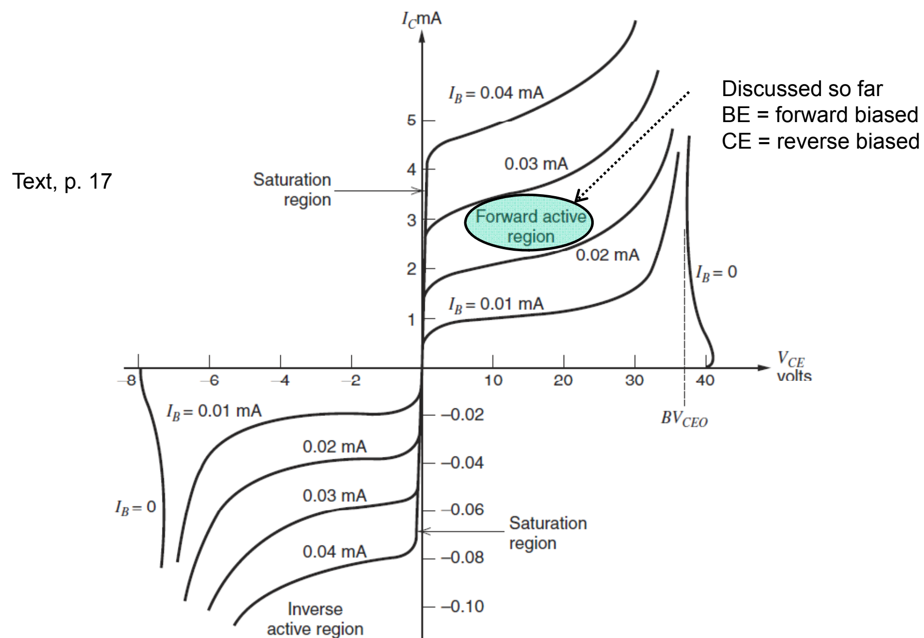
- Much larger than the intrinsic gain of typical MOSFET devices

Outline – Model Extensions and Technology

- Complete picture of BJT operating regions
- Dependence of β_F on operating conditions
- Device capacitances and resistances
- Technology
  - Junction isolated
  - Oxide isolated with polysilicon emitter
  - Heterojunction bipolar (SiGe base)
  - BiCMOS
  - Complementary bipolar

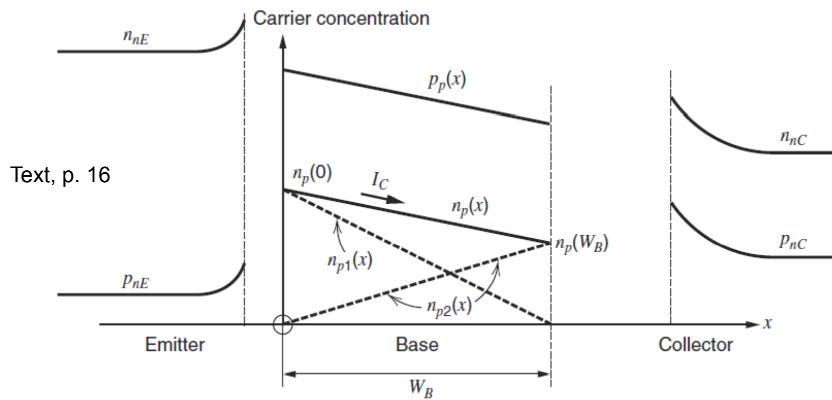
BJT Operating Regions

Text, p. 17



Carrier Concentrations in Saturation

Text, p. 16

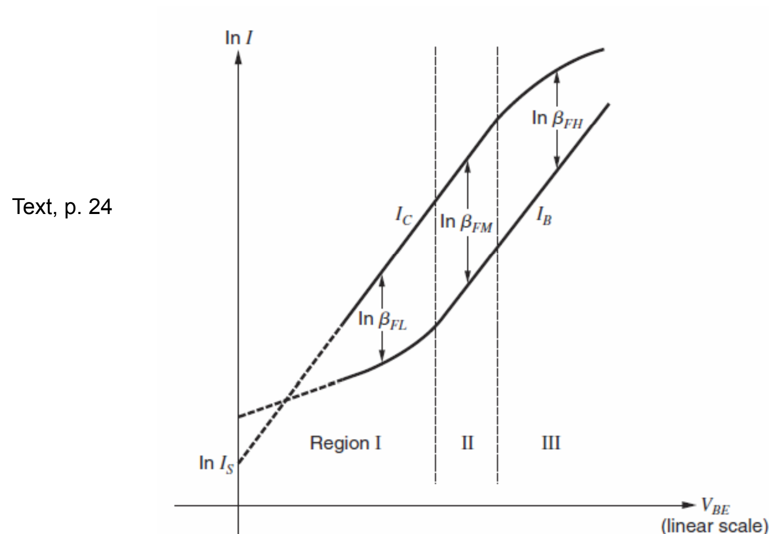


- Base-Collector junction is forward biased
- $n_p(W_B)$, and therefore also I_C, strongly depend on V_{BC}, V_{CE}
- $V_{CE(sat)}$ is the voltage at which the devices enters saturation
  - The difference between the two junction voltages, small ~0.05…0.3V

Gummel Plot

- A Gummel plot is a semi-log plot of I_C and I_B versus V_{BE} (linear scale)
- It reveals the regions for which high β_F is maintained (region II below)
- What happens in regions I and III?

Text, p. 24



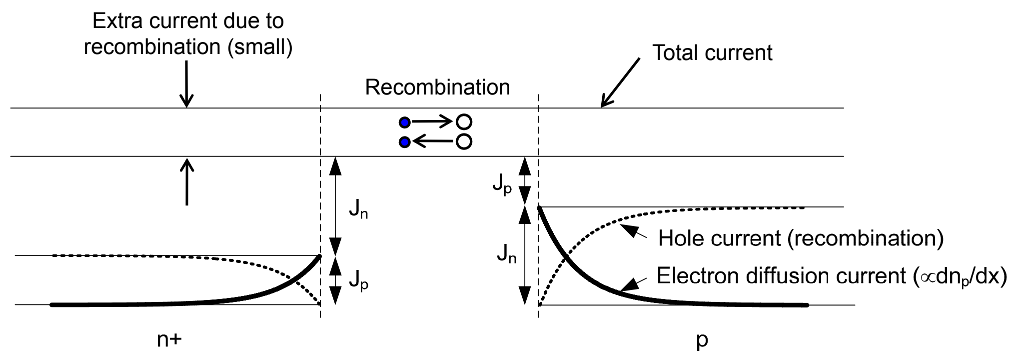
β_F Fall-Off

- Region III (high current density)
  - Injected electron charge in base region nears the level of doping ("high level injection")
  - For this case, it can be shown that the injected carrier concentration rises with a smaller exponent (cut in half) and therefore

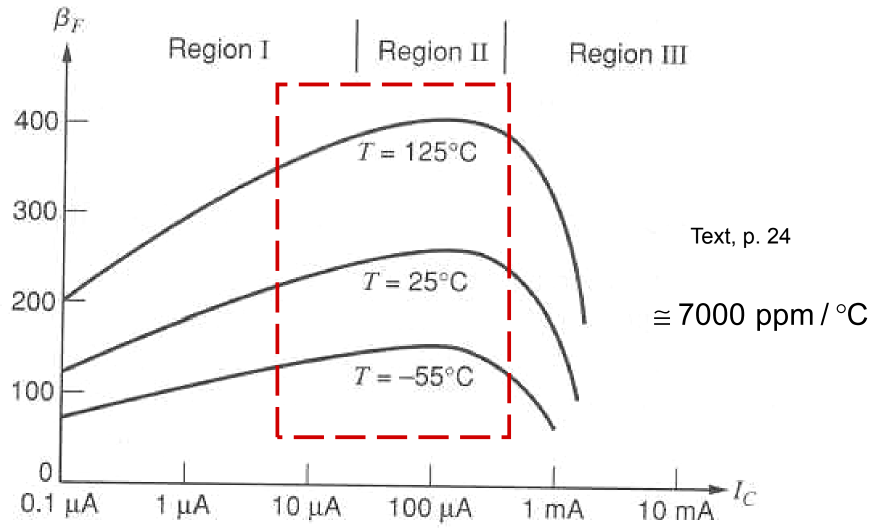
$$I_C = I_S e^{\frac{1}{2}\frac{V_{BE}}{V_T}}$$

- Region I (low current density)
  - There exists excess base current due to (unwanted) recombination in the depletion layer of the base-emitter junction
  - This current becomes significant at low current densities and sets a minimum for I_B

Current Profile of a Forward Biased Diode Revisited



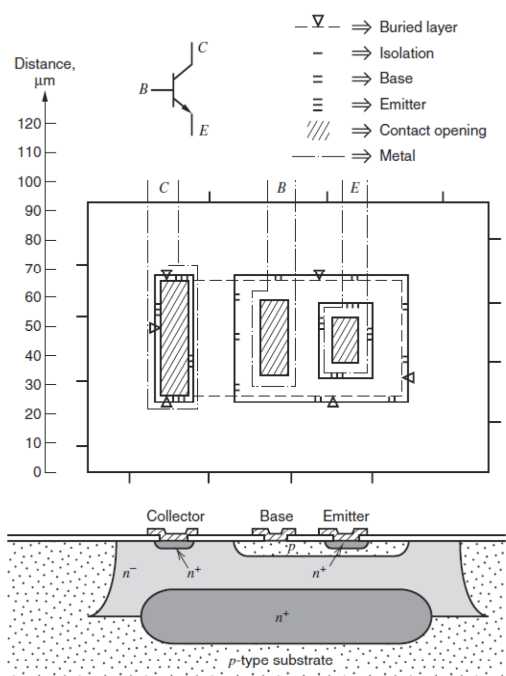
β_F vs. I_C and Temperature



Text, p. 24

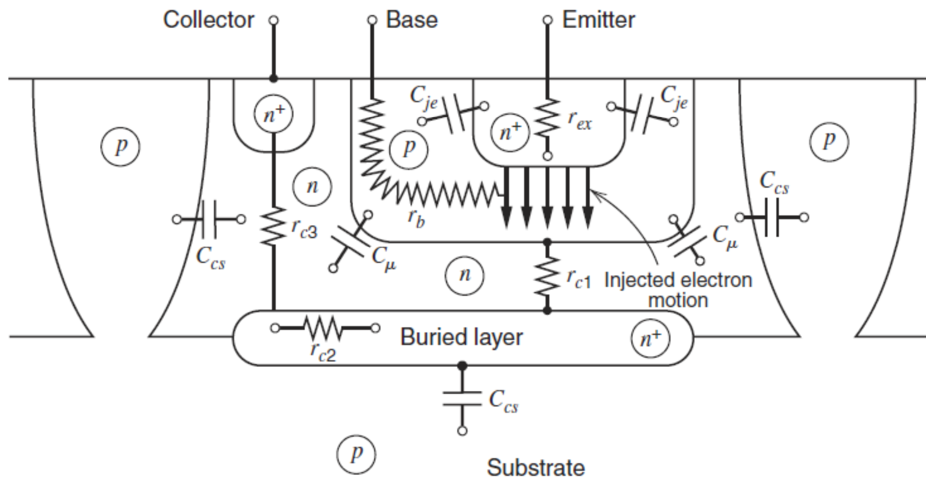
$\cong 7000\ \text{ppm} / °\text{C}$

Junction Isolated npn Transistor



Text, p. 97

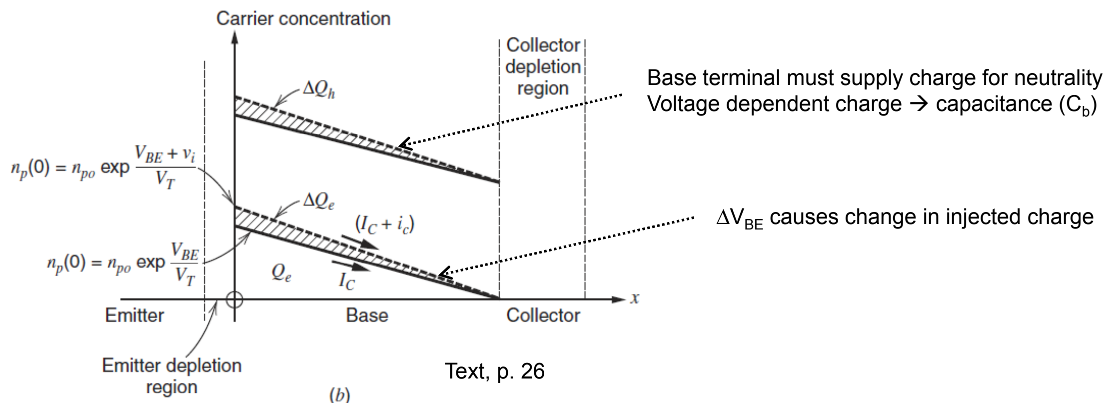
Device Capacitances and Resistances



- Big mess!
- First focus on intrinsic elements

Charge Storage

- In the intrinsic transistor, charge is stored in the junction capacitances, C_{je} and $C_{jc} = C_\mu$, and as minority carriers in the base and emitter
- Both minority carrier charge injected into the base and into the emitter, are proportional to $\exp(V_{BE}/V_T)$
  - But the charge in the base is much larger, as discussed previously



Text, p. 26

Base Charging Capacitance

$$C_b \triangleq \frac{\partial Q_e}{\partial V_{BE}} = \frac{\partial Q_e}{\partial I_C}\frac{\partial I_C}{\partial V_{BE}} = \tau_F g_m$$

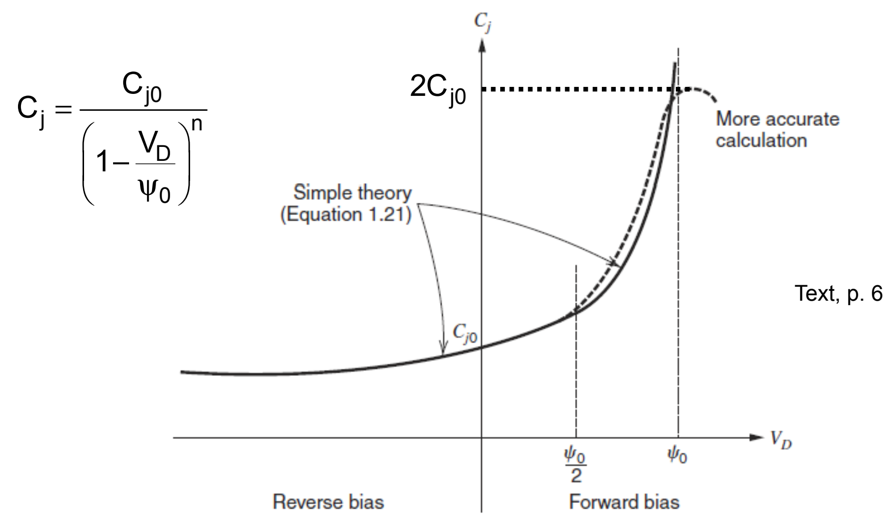
$$\tau_F = \frac{\partial Q_e}{\partial I_C} = \frac{\partial}{\partial I_C}\left(\frac{1}{2}n_p(0)W_B qA\right) \qquad I_C = \frac{qAD_n n_p(0)}{W_B}$$

$$\tau_F = \frac{\partial}{\partial I_C}\left(\frac{1}{2}\frac{W_B^2}{D_n}I_C\right) = \frac{1}{2}\frac{W_B^2}{D_n}$$

- τ_F is called the base transit time (in forward direction)
- Typical values for high-speed transistors are on the order of 1…100ps

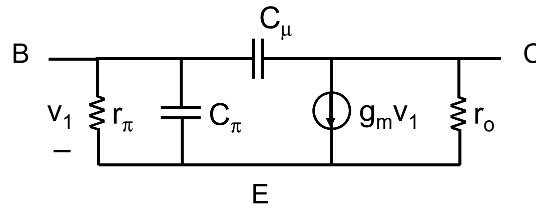
Junction Capacitance

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\psi_0}\right)^n}$$



Text, p. 6

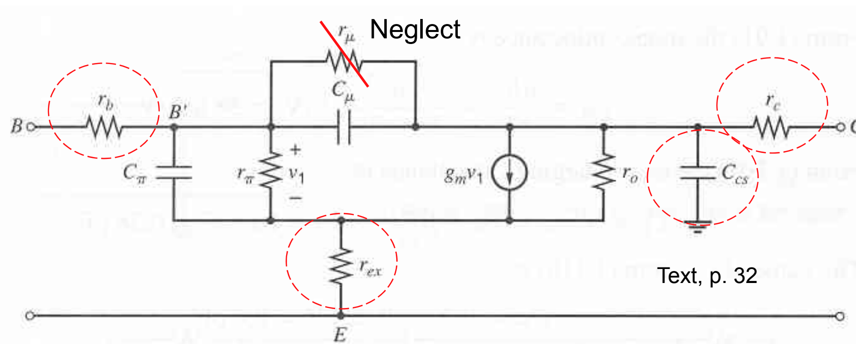
Small-Signal Model with Intrinsic Capacitances



$$C_\pi = C_b + C_{je} = C_b + 2C_{je0}$$

$$C_\mu = C_{jc} = \frac{C_{jc0}}{\left(1+\frac{V_{CB}}{\psi_{0c}}\right)^n}$$

Model with Additional Parasitics

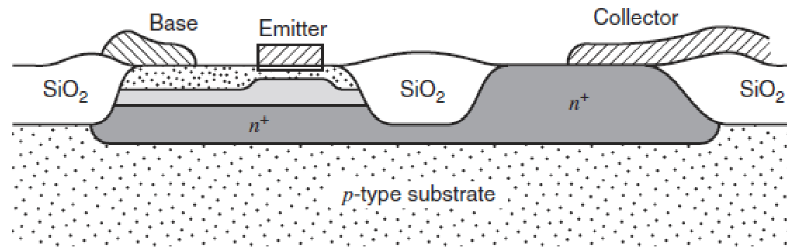


<u>Range of numbers</u>

- r_e ~1-3Ω
- r_b ~ 50-500Ω
- r_c ~ 20-500Ω
- C_{CS} ~ 3-200fF

Values at high end of these ranges may have large impact on performance → Try to minimize through advanced processing & technology

BJT in Advanced Technology



Text, p. 107

- Oxide isolated
- Self-aligned structure (base and emitter align automatically)
- Very thin base (~100nm or less) through ion implantation
- Reduced breakdown voltages compared to more traditional structures

SiGe Heterojunction Bipolar Technology

- A heterojunction is a pn junction formed with different materials for the n and p regions
- Germanium is added to the base of a silicon bipolar transistor to create a heterojunction bipolar transistor (HBT)
  - Base formed by growing a thin epitaxial layer of SiGe
  - Results in a lower bandgap (and higher intrinsic carrier concentration) in the base than emitter
- In “band diagram speak” the bandgap mismatch increases the barrier to the injection of holes (in an npn transistor) from the base into the emitter
- One way to enumerate the benefits of a SiGe base is to look at the current gain expression

HBT Current Gain

- Intrinsic carrier concentration in the SiGe base (n_{iB}) is larger than intrinsic carrier concentration in the Si emitter (n_{iE})

$$\beta_F = \frac{\dfrac{qAD_n n_{p0}}{W_B}}{\dfrac{1}{2}\dfrac{n_{p0} W_B qA}{\tau_b} + \dfrac{qAD_p n_{iE}^2}{L_p N_D}} \cong \frac{\dfrac{qAD_n n_{p0}}{W_B}}{\dfrac{qAD_p n_{iE}^2}{L_p N_D}} = \frac{\dfrac{qAD_n n_{iB}^2}{W_B N_A}}{\dfrac{qAD_p n_{iE}^2}{L_p N_D}} = \frac{D_n N_D L_p}{D_p N_A W_B} \cdot \boxed{\frac{n_{iB}^2}{n_{iE}^2}}$$

Added degree of freedom for HBT

- Base doping (N_A) can be increased while maintaining same β_F
  - Can reduce base width without affecting r_b
  - Larger r_o due to decrease in base width modulation

Device Parameter Comparison

Parameter	Vertical *npn* Transistor with 2 μm² Emitter Area	SiGe npn HBT Transistor with 0.7μm² = 0.22μm x 3.2μm Emitter Area
β_F	120	**300**
β_R	2	**2**
V_A	35 V	**90**
I_S	6×10^{-18}A	**3.2×10^{-17}A**
I_{CO}	1 pA	**1pA**
BV_{CEO}	8 V	**2.0V**
BV_{CBO}	18 V	**5.5V**
BV_{EBO}	6 V	**3.3V**
τ_F	10 ps	**0.56ps**
τ_R	5 ns	**10ps**
r_b	400 Ω	**25Ω**
r_c	100 Ω	**60Ω**
r_{ex}	40 Ω	**2.5Ω**
C_{je0}	5 fF	**6.26fF**
ψ_{0e}	0.8 V	**0.8V**
n_e	0.4	**0.4**
$C_{\mu0}$	5 fF	**3.42fF**
ψ_{0c}	0.6 V	**0.6V**
n_c	0.33	**0.33**
C_{cs0} (C_{bs0})	20 fF	**3.0fF**
ψ_{0s}	0.6 V	**0.6V**
n_s	0.33	**0.33**

3x smaller device, 5x bigger I_S (for I_S)

18x smaller τ_F (for τ_F)

16x smaller r_b (for r_b)

Oxide isolation vs. Junction isolation (for C_{cs0})

BiCMOS Technology

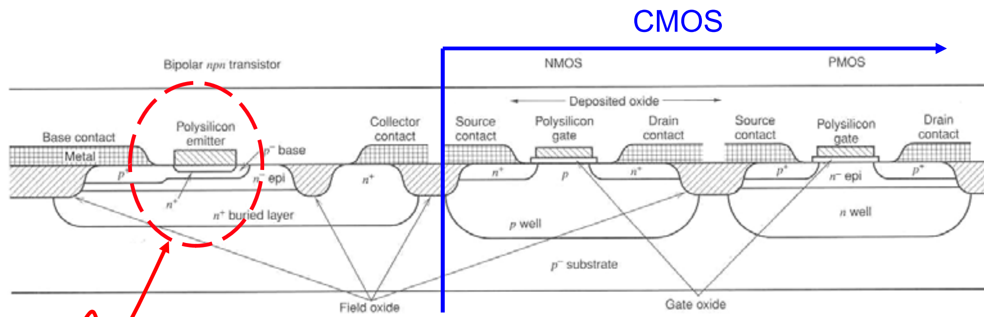


Figure 2.66 Cross section of a high-performance BiCMOS process.

Text, p. 154

Older BJTs used poly Si as “diffusion source” for emitter doping. Advanced (state-of-the-art) BJTs use epitaxial growth of both the SiGe base and Si emitter regions

Advanced Complementary Bipolar Technology

BiCom3x Overview

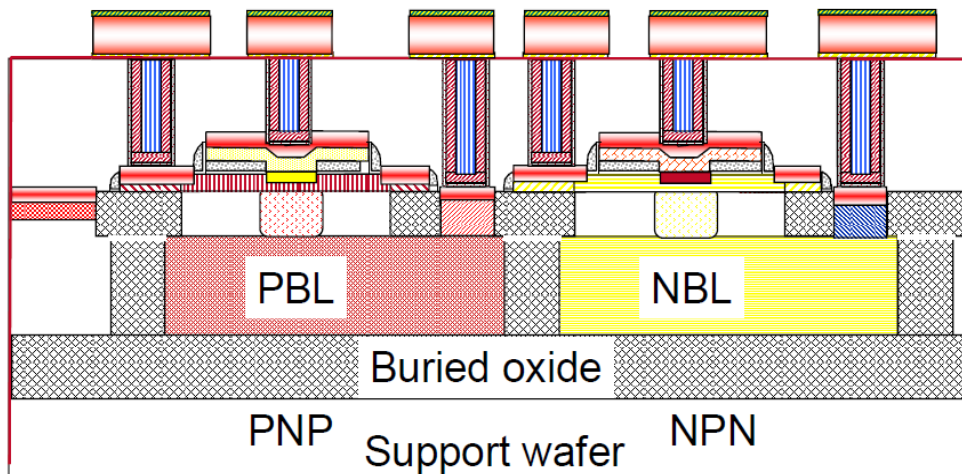
Technology Features:
- 200mm Wafers
- 0.35 um Features
- 5V Operation
- SOI Substrates
- Trench Isolation
- SiGe Bipolar (NPN & PNP)
- 115 A Gate Ox
- QLM (1.0 um Pitch)
- NiCrAl Thin Film Resistor
- Metal-Silicide Capacitor
- Cu Power Metal Option
- Laser Trimming
- 13K Gates/mm^2

- Qualified 1Q06
- In Production

Component Set:
- CMOS: 5V & 3.3V
- Isolated CMOS
- 5V NPN
- 5V PNP
- Poly Resistors
- Well Resistors
- Thin Film Resistor
- TiN-Polycide Capacitor
- Poly Fuse

[Texas Instruments]

Cross Section

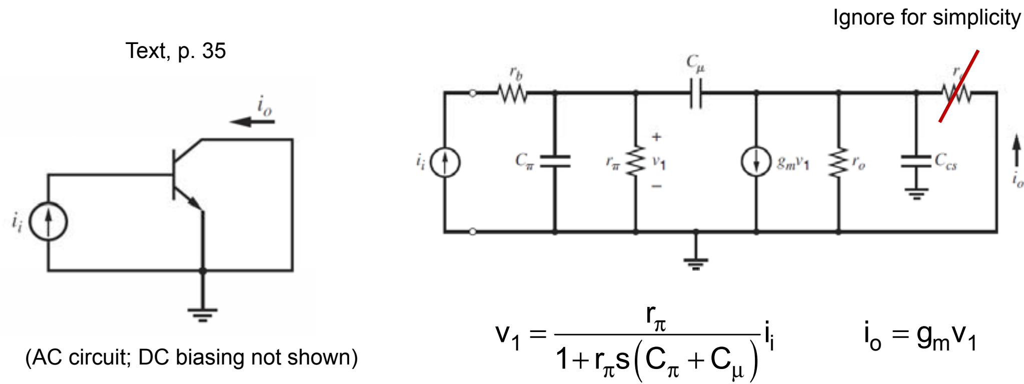


[Texas Instruments]

Figures of Merit for BJTs

- Product of current gain and Early voltage, $\beta \cdot V_A$
- Product of transit frequency and breakdown voltage, $f_T \cdot BV_{CEO}$
- Maximum frequency of oscillation, f_{max}
  - More in EE314
- Transit (or transition) frequency, f_T
  - Formally defined as the frequency for which the current gain of the device falls to unity
  - Important to keep in mind that the basic device model may fall apart altogether at this frequency
    - Lumped device models tend to be OK up to ~f_T/5
  - Therefore, f_T should be viewed as an extrapolated parameter, or simply as a proxy for device transconductance per capacitance

Transit Frequency Calculation (1)



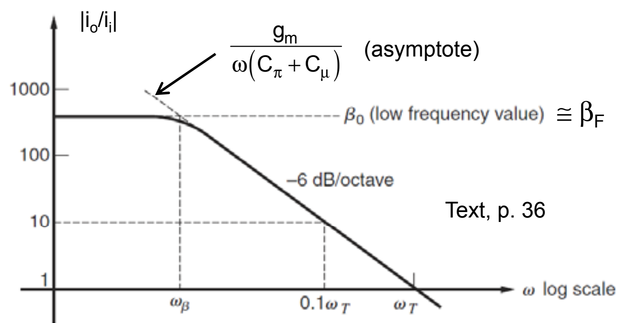
(AC circuit; DC biasing not shown)

$$v_1 = \frac{r_\pi}{1 + r_\pi s\left(C_\pi + C_\mu\right)} i_i \qquad i_o = g_m v_1$$

$$\frac{i_o}{i_i} = \frac{g_m r_\pi}{1 + r_\pi j\omega\left(C_\pi + C_\mu\right)} \cong g_m r_\pi = \beta_F \quad \text{for} \quad \omega << \frac{1}{r_\pi\left(C_\pi + C_\mu\right)} = \omega_\beta$$

$$\frac{i_o}{i_i} \cong \frac{g_m}{j\omega\left(C_\pi + C_\mu\right)} \quad \text{for} \quad \omega >> \omega_\beta$$

Transit Frequency Calculation (2)



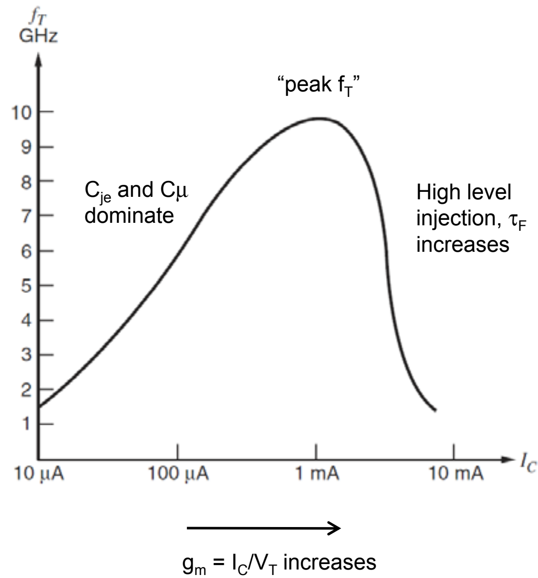
Text, p. 36

Note that r_π "matters" only for frequencies up to $\omega_\beta = \omega_T/\beta_F$

$$1 = \frac{g_m}{\omega_T\left(C_\pi + C_\mu\right)} \qquad \Rightarrow \omega_T = \frac{g_m}{C_\pi + C_\mu}$$

$$\tau_T = \frac{1}{\omega_T} = \frac{C_b}{g_m} + \frac{C_{je}}{g_m} + \frac{C_\mu}{g_m} = \tau_F + \frac{C_{je}}{g_m} + \frac{C_\mu}{g_m}$$

f_T versus I_C plot



Text, p. 37

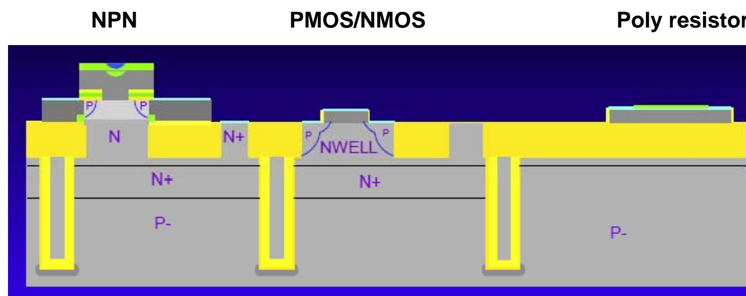
$g_m = I_C/V_T$ increases

- The particular current value at which f_T is maximized depends on the particular parameters of a technology and the emitter area of the BJT

EE214 Technology

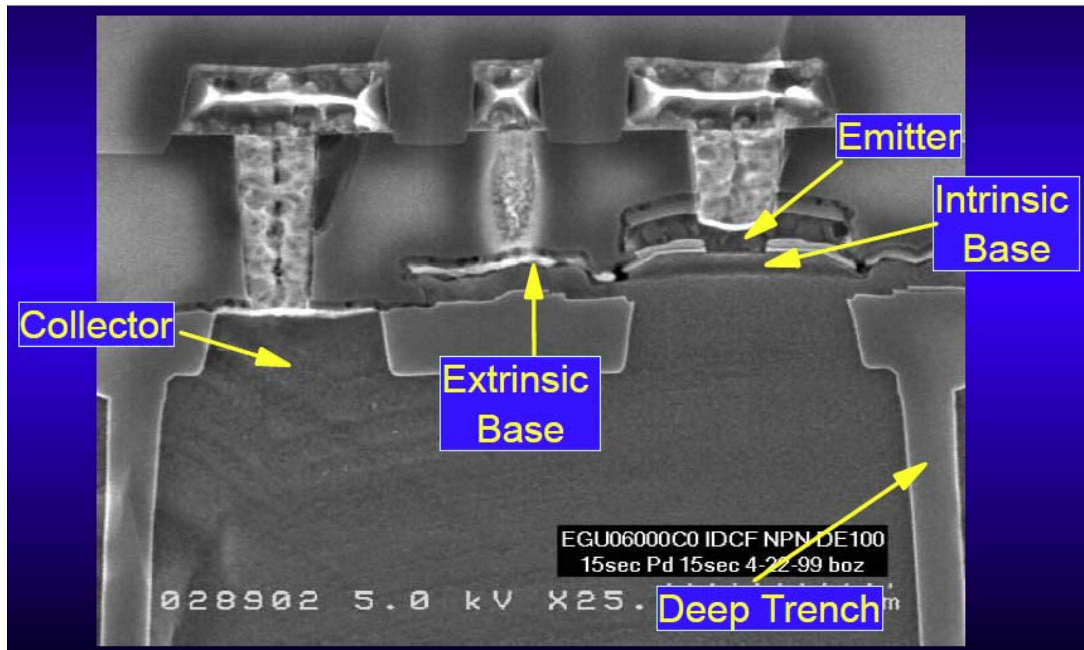
- Assumed to be similar to a 0.18-µm BiCMOS technology featuring a high-performance SiGe npn device
  - V_{CC} = 2.5V (BJT), V_{DD}=1.8V (MOS)
- See e.g.
  - Wada et al., BCTM 2002
  - Joseph et al., BCTM 2001
  - IBM 7HP documentation
    - https://www-01.ibm.com/chips/techlib/techlib.nsf/products/BiCMOS_7HP)

NPN **PMOS/NMOS** **Poly resistor**



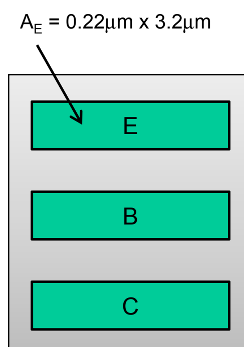
http://fuji.stanford.edu/events/spring01/slides/harameSlides.pdf

Cross Section of npn Device



EE214 npn Unit Device

A_E = 0.22µm x 3.2µm



- A technology typically comes with an optimized layout for a unit device of a certain size
- Great care is then taken to extract a Spice model for this particular layout using measured data
- Spice model (usr/class/ee214/hspice/ee214_hspice.sp)

```
.model npn214 npn
+ level=1 tref=25 is=.032f bf=300 br=2 vaf=90
+ cje=6.26f vje=.8 mje=.4 cjc=3.42f vjc=.6 mjc=.33
+ re=2.5 rb=25 rc=60 tf=563f tr=10p
+ xtf=200 itf=80m ikf=12m ikr=10.5m nkf=0.9
```

- Instantiation in a circuit netlist

```
*    C  B  E
q1   n1 n2 n3  npn214
```

BJT Model Parameters

Table 5-3 BJT Model Parameters

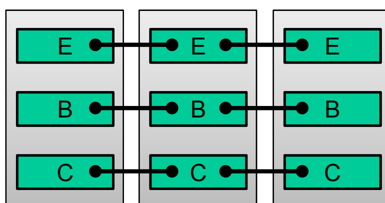
Parameter	Description
DC	BF, BR, IBC, IBE, IS, ISS, NF, NR, NS, VAF, VAR
beta degradation	ISC, ISE, NC, NE, IKF, IKR
geometric	SUBS, BULK
resistor	RB, RBM, RE, RC, IRB
junction capacitor	CJC, CJE, CJS, FC, MJC, MJE, MJS, VJC, VJE, VJS, XCJC
parasitic capacitance	CBCP, CBEP, CCSP
transit time	ITF, PTF, TF, VT, VTF, XTF
noise	KF, AF

- For more info consult the HSpice documentation under

/afs/ir.stanford.edu/class/ee/synopsys/B-2008.09-SP1/hspice/docs_help

```
PDF files:
home.pdf  hspice_cmdref.pdf  hspice_integ.pdf  hspice_relnote.pdf  hspice_sa.pdf
hspice_devmod.pdf  hspice_mosmod.pdf  hspice_rf.pdf  hspice_si.pdf
```


Adding Multiple Devices in Parallel

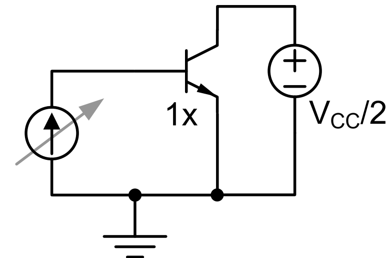


- For the unit device, there exists a practical upper bound for the collector current
  - Due to the onset of high level injection
- This means that the unit device can only deliver a certain maximum g_m
- If more g_m is needed, “m” unit devices can be connected in parallel
- Instantiation in a circuit netlist (m=3)

```
*    C  B  E
q1   n1 n2 n3  npn214   3
```

npn Unit Device Characterization

```
* ee214 npn device characterization

*    C B E
q1   c b 0   npn214
Vc   c 0     1.25
ib   0 b     1u

.op
.dc ib dec 10 10f 100u
.probe ib(q1) ic(q1) ie(q1)
.probe gm   =  par('gm(q1)')
.probe go   =  par('g0(q1)')
.probe cpi  =  par('cap_be(q1)')
.probe cmu  =  par('cap_ibc(q1)')
.probe beta =  par('beta(q1)')

.options dccap post brief
.inc '/usr/class/ee214/hspice/ee214_hspice.sp'
.end
```



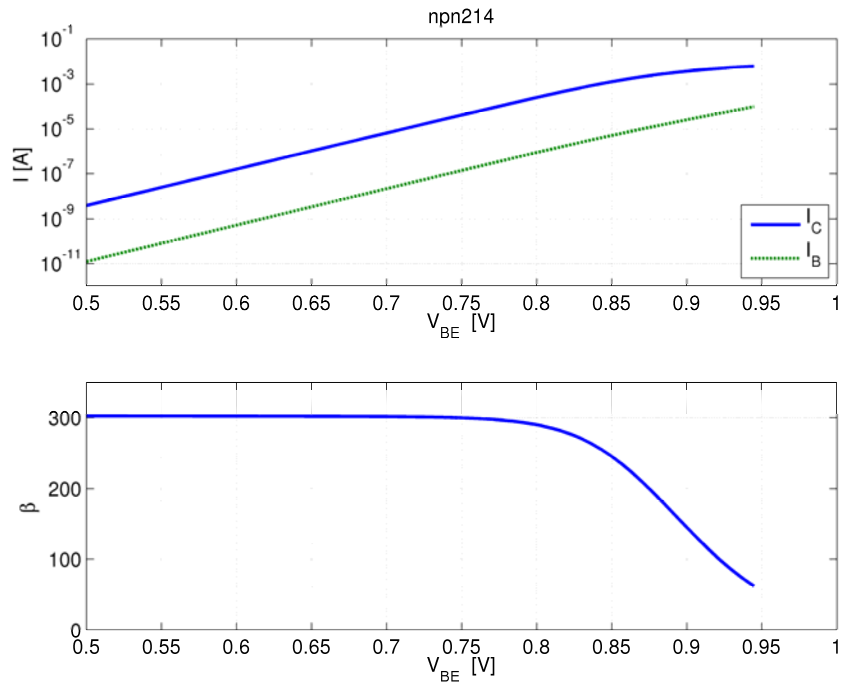
DC Operating Point Output

```
**** bipolar junction transistors
element  0:q1
 model    0:npn214
  ib       999.9996n
  ic       288.5105u
  vbe      803.4402m
  vce        1.2500
  vbc     -446.5598m
  vs        -1.2327
  power    361.4415u
  betad    288.5106
  gm        10.2746m
  rpi       26.8737k
  rx        25.0000
  ro       313.4350k
  cpi       14.6086f
  cmu        2.8621f
  cbx        0.
  ccs        0.
  betaac   276.1163
  ft        93.5999g
```

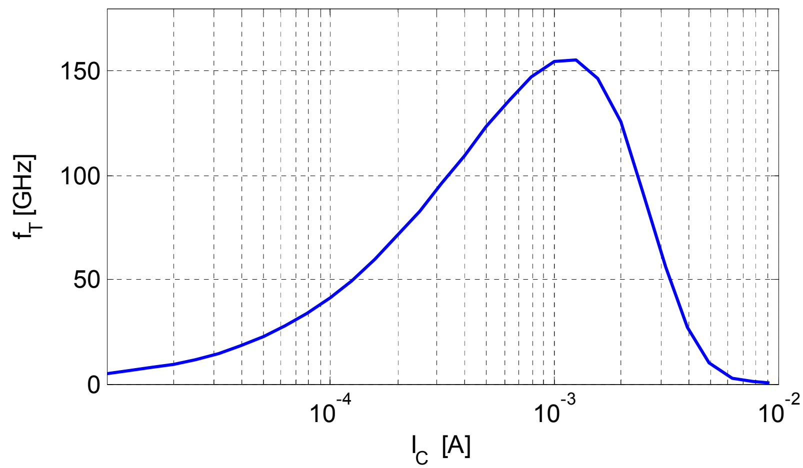
Table 5-18 BJT DC Operating Point Output

Quantities	Definitions
ib	base current
ic	collector current
is	substrate current
vbe	B-E voltage
vbc	B-C voltage
vcs	C-S voltage
vs	substrate voltage
power	power
betad(betadc)	beta for DC analysis
gm	transconductance
rpi	B-E input resistance
rmu(rmuv)	B-C input resistance
rx	base resistance
ro	collector resistance
cpi	internal B-E capacitance
cmu	internal B-C capacitance
cbx	external B-C capacitance
ccs	C-S capacitance
cbs	B-S capacitance
cxs	external substrate capacitance
betaac	beta for AC analysis
ft	unity gain bandwidth

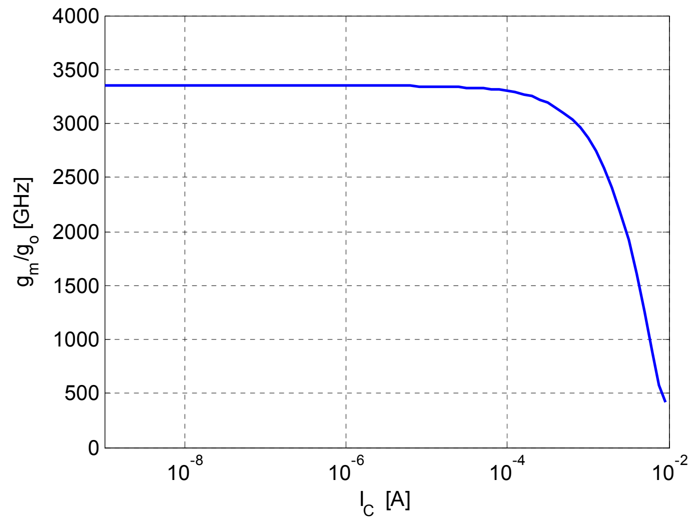
Gummel Plot



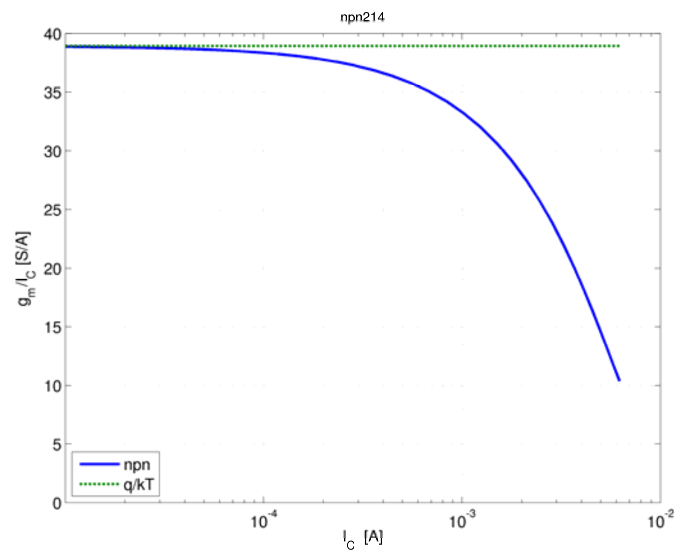
Transit Frequency



Intrinsic Gain

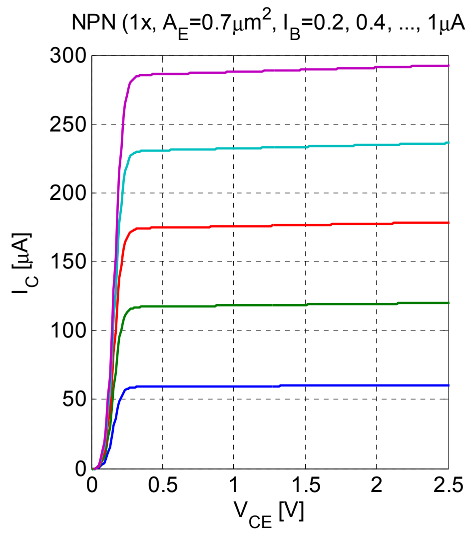


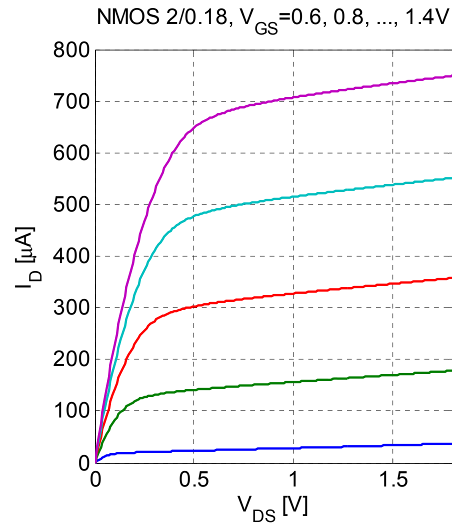
g_m/I_C



- Important to realize that g_m will not be exactly equal to I_C/V_T at high currents

I-V Curves





Passive Components (1)

Resistors	Rs (O/Sq)	TCR (ppm/C)
Subcollector	8.1	1430
N+ Diffusion	72	1910
P+ Diffusion	105	1430
P+ Polysilcon	270	50
P Polysilicon	1600	-1178
TaN	135	-750
Capacitors	**Cp (fF/um2)**	**VCR (+5/-5 ppm/V)**
MIM	1	<45
MOS	2.6	5
Inductor	**L (nH)**	**Max Q at 5 GHz**
Al - Spiral Inductor	>=0.7	21
Varactor	**Tuning Range**	**Q @0.5 GHz**
CB Junction	1.64:1	90
MOS Accumulation	3.1:1	300

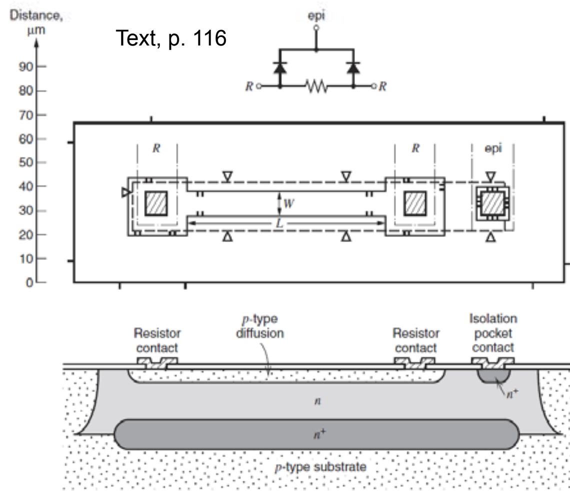
Joseph et al., BCTM 2001

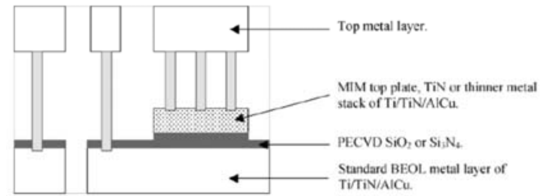
Passive Components (2)

Diffusion Resistor

MIM Capacitor

Text, p. 116





[Ng, Trans. Electron Dev. 7/2005]

Chapter 3

MOS Transistor Modeling

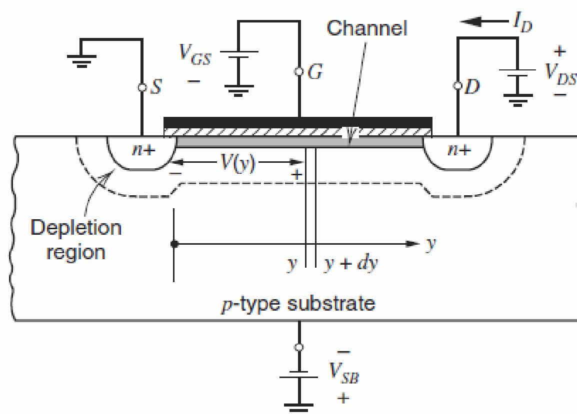
G_m/I_D-based Design

B. Murmann

Stanford University

Reading Material: Sections 1.5, 1.6, 1.7, 1.8

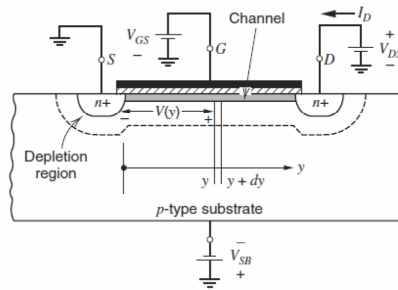
Basic MOSFET Operation (NMOS)



Text, p.41

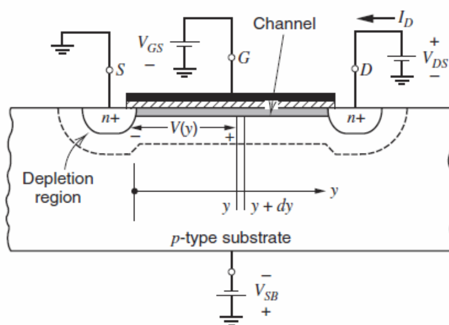
How to calculate drain current (I_D) current as a function of V_{GS}, V_{DS}?

Simplifying Assumptions



1) Current is controlled by the mobile charge in the channel. This is a very good approximation.
2) "Gradual Channel Assumption" - The vertical field sets channel charge, so we can approximate the available mobile charge through the voltage difference between the gate and the channel
3) The last and worst assumption (we will fix it later) is that the carrier velocity is proportional to lateral field ($v = \mu E$). This is equivalent to Ohm's law: velocity (current) is proportional to E-field (voltage)

Derivation of First Order IV Characteristics (1)



$$Q_n(y) = C_{ox}\left[V_{GS} - V(y) - V_t\right]$$

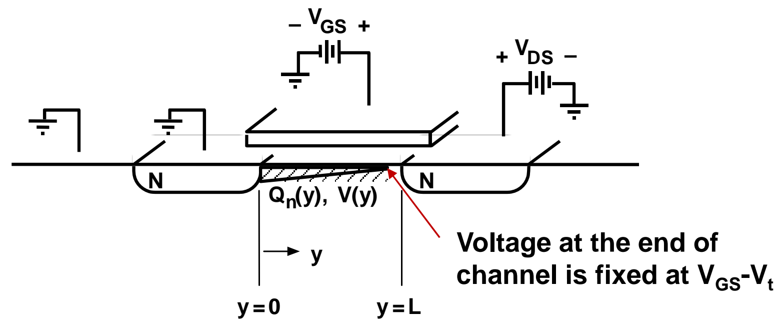
$$I_D = Q_n \cdot v \cdot W$$

$$v = \mu \cdot E$$

$$I_D = C_{ox}\left[V_{GS} - V(y) - V_t\right] \cdot \mu \cdot E \cdot W$$

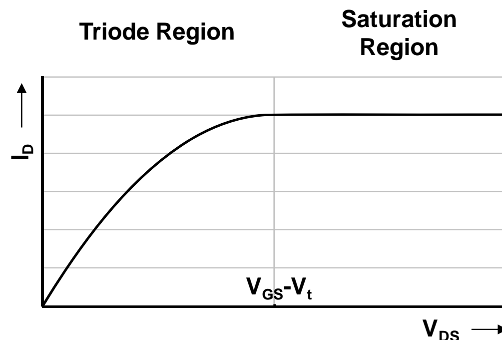
$$\boxed{I_D = \mu C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_t\right) - \frac{V_{DS}}{2}\right] \cdot V_{DS}}$$

Pinch-Off



- Effective voltage across channel is V_{GS}-V_t
  - At the point where channel charge goes to zero, there is a high lateral field that sweeps the carriers to the drain
    - Recall that electrons are minority carriers in the p-region of a pn junction; they are being swept toward the n-region
  - The extra drain voltage drops across depletion region
- To first order, the current becomes independent of V_{DS}

Plot of Output Characteristic



Triode Region:

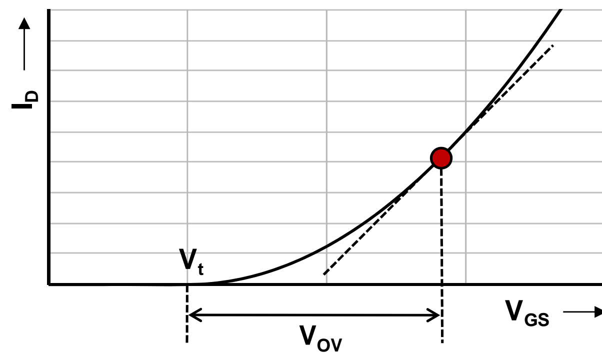
$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_t) - \frac{V_{DS}}{2}\right] \cdot V_{DS}$$

Saturation Region:

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_t) - \frac{(V_{GS} - V_t)}{2}\right] \cdot (V_{GS} - V_t)$$

$$= \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$$

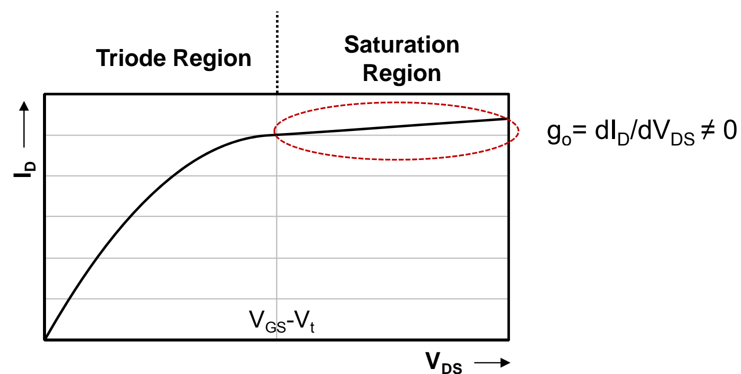
Plot of Transfer Characteristic (in Saturation)



$$g_m = \frac{dI_D}{dV_{GS}} = \mu C_{ox}\frac{W}{L}(V_{GS}-V_t) = \mu C_{ox}\frac{W}{L}V_{OV}$$

$$= \sqrt{2I_D\mu C_{ox}\frac{W}{L}} = \frac{2I_D}{V_{OV}}$$

Output Characteristic with "Channel Length Modulation"

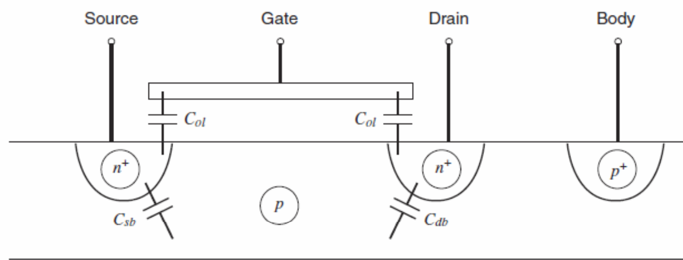


$g_o = dI_D/dV_{DS} \neq 0$

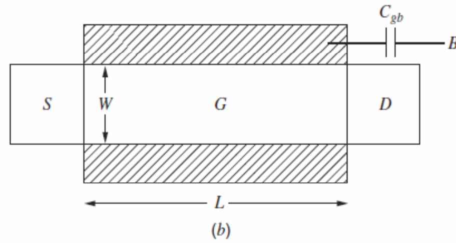
$$g_o = \frac{dI_D}{dV_{DS}} = \frac{d}{dV_{DS}}\left[\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{ds})\right]$$

$$= \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_t)^2 \cdot \lambda = \frac{\lambda I_D}{1+\lambda V_{DS}} \cong \lambda I_D$$

Capacitances



(a)



(b)

Text, p. 54

Gate Capacitance Summary

	Subthreshold	Triode	Saturation
C_{gs}	C_{ol}	$\frac{1}{2} WLC_{ox} + C_{ol}$	$\frac{2}{3} WLC_{ox} + C_{ol}$
C_{gd}	C_{ol}	$\frac{1}{2} WLC_{ox} + C_{ol}$	C_{ol}
C_{gb}	$\left(\frac{1}{C_{js}} + \frac{1}{WLC_{ox}}\right)^{-1}$	0	0

Capacitance Equations and Parameters

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{ol} = WC'_{ol}$$

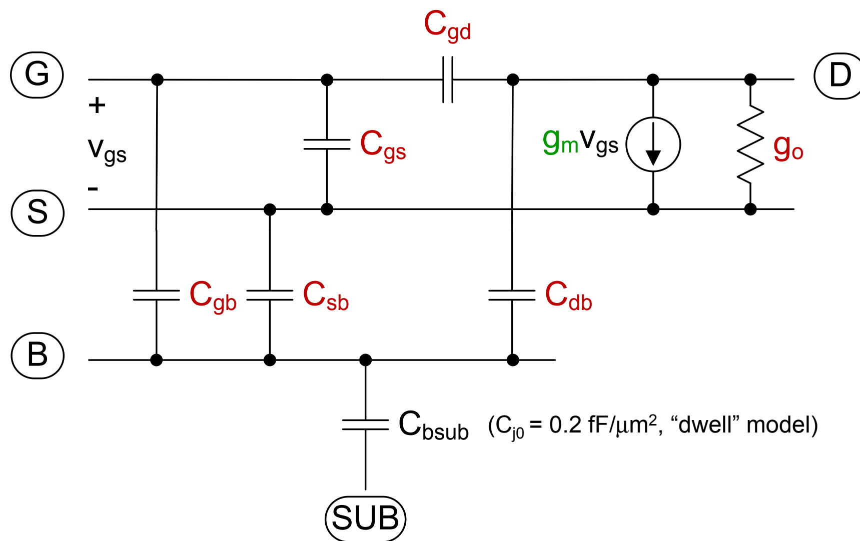
$$C_{db} = \frac{AD \cdot C_J}{\left(1+\frac{V_{DB}}{PB}\right)^{MJ}} + \frac{PD \cdot C_{JSW}}{\left(1+\frac{V_{DB}}{PB}\right)^{MJSW}}$$

$$AD = WL_{diff}$$

$$PD = W + 2L_{diff}$$

Parameter	EE 214 Technology (0.18μm)	
	NMOS	PMOS
C_{ox}	8.42 fF/μm²	8.42 fF/μm²
C'_{ol}	0.491 fF/μm	0.657 fF/μm
C_J	0.965 fF/μm²	1.19 fF/μm²
C_{JSW}	0.233 fF/μm	0.192 fF/μm
PB	0.8 V	0.8 V
MJ	0.38	0.40
MJSW	0.13	0.33
LDIF	0.64 μm	0.64 μm

Complete Small-Signal Model



$$C_{gg} \triangleq C_{gs} + C_{gb} + C_{gd} \qquad C_{dd} \triangleq C_{db} + C_{gd}$$

What are μC_{ox} ("KP") and λ ("LAMBDA") for our Technology?

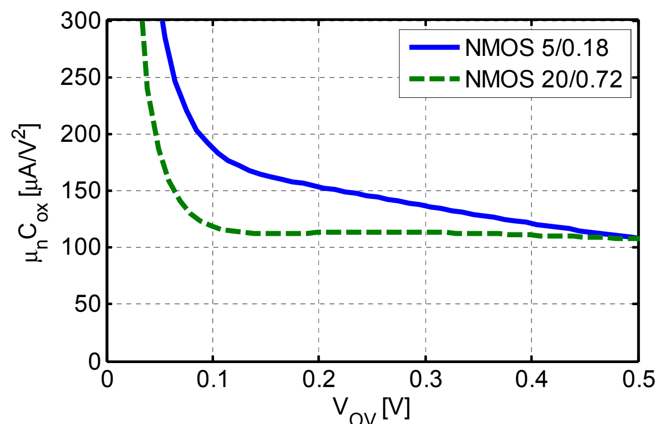
```
.MODEL nmos214 nmos
+acm     = 3            hdif     = 0.32e-6       LEVEL    = 49
+VERSION = 3.1          TNOM     = 27            TOX      = 4.1E-9
+XJ      = 1E-7         NCH      = 2.3549E17     VTH0     = 0.3618397
+K1      = 0.5916053    K2       = 3.225139E-3   K3       = 1E-3
+K3B     = 2.3938862    W0       = 1E-7          NLX      = 1.776268E-7
+DVT0W   = 0            DVT1W    = 0             DVT2W    = 0
+DVT0    = 1.3127368    DVT1     = 0.3876801     DVT2     = 0.0238708
+U0      = 256.74093    UA       = -1.585658E-9  UB       = 2.528203E-18
+UC      = 5.182125E-11 VSAT     = 1.003268E5    A0       = 1.981392
+AGS     = 0.4347252    B0       = 4.989266E-7   B1       = 5E-6
+KETA    = -9.888408E-3 A1       = 6.164533E-4   A2       = 0.9388917
+RDSW    = 128.705483   PRWG     = 0.5           PRWB     = -0.2
+WR      = 1            WINT     = 0             LINT     = 1.617316E-8
+XL      = 0            XW       = -1E-8         DWG      = -5.383413E-9
+DWB     = 9.111767E-9  VOFF     = -0.0854824    NFACTOR  = 2.2420572
+CIT     = 0            CDSC     = 2.4E-4        CDSCD    = 0
+CDSCB   = 0            ETA0     = 2.981159E-3   ETAB     = 9.289544E-6
+DSUB    = 0.0159753    PCLM     = 0.7245546     PDIBLC1  = 0.1568183
+PDIBLC2 = 2.543351E-3  PDIBLCB  = -0.1          DROUT    = 0.7445011
+PSCBE1  = 8E10         PSCBE2   = 1.876443E-9   PVAG     = 7.200284E-3
+DELTA   = 0.01         RSH      = 6.6           MOBMOD   = 1
+PRT     = 0            UTE      = -1.5          KT1      = -0.11
+KT1L    = 0            KT2      = 0.022         UA1      = 4.31E-9
+UB1     = -7.61E-18    UC1      = -5.6E-11      AT       = 3.3E4
+WL      = 0            WLN      = 1             WW       = 0
+WWN     = 1            WWL      = 0             LL       = 0
+LLN     = 1            LW       = 0             LWN      = 1
+LWL     = 0            CAPMOD   = 2             XPART    = 1
+CGDO    = 4.91E-10     CGSO     = 4.91E-10      CGBO     = 1E-12
+CJ      = 9.652028E-4  PB       = 0.8           MJ       = 0.3836899
+CJSW    = 2.326465E-10 PBSW     = 0.8           MJSW     = 0.1253131
+CJSWG   = 3.3E-10      PBSWG    = 0.8           MJSWG    = 0.1253131
+CF      = 0            PVTH0    = -7.714081E-4  PRDSW    = -2.5827257
+PK2     = 9.619963E-4  WKETA    = -1.060423E-4  LKETA    = -5.373522E-3
+PU0     = 4.5760891    PUA      = 1.469028E-14  PUB      = 1.783193E-23
+PVSAT   = 1.19774E3    PETA0    = 9.968409E-5   PKETA    = -2.51194E-3
+nlev    = 3            kf       = 0.5e-25
```

- The HSpice model for an NMOS device in our technology is shown to the left
- BSIM 3v3 model
- 110 parameters
- KP and LAMBDA nowhere to be found…

An Attempt to Extract μC_{ox}

- Bias MOSFET at constant $V_{DS}>V_{OV}$, sweep V_{GS} and plot μC_{ox} estimate

$$\mu C_{ox} = \frac{2I_D}{\frac{W}{L}V_{OV}^2}$$



- The extracted μC_{ox} depends on L and V_{OV} and cannot be viewed as a constant parameter

Questions

- Which physical effects explain the large deviation from the basic square law model?
- How can we design with such a device?
  - Is there another "simple" equation that describes its behavior?
- We will approach the above two questions by performing a systematic, simulation-based device characterization
  - And discuss the relevant physical phenomena that explain the observed behavior
- As a basis for this characterization, we consider three basic figures of merit that relate directly to circuit design

Figures of Merit for Device Characterization

Square Law

- Transconductance efficiency
  - Want large g_m, for as little current as possible

$$\frac{g_m}{I_D} = \frac{2}{V_{OV}}$$

- Transit frequency
  - Want large g_m, without large C_{gg}

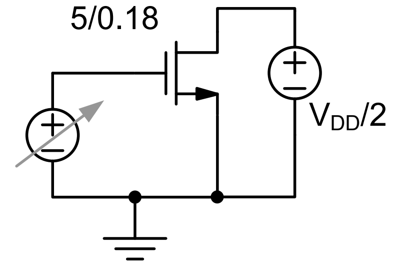
$$\frac{g_m}{C_{gg}} \cong \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

- Intrinsic gain
  - Want large g_m, but no g_o

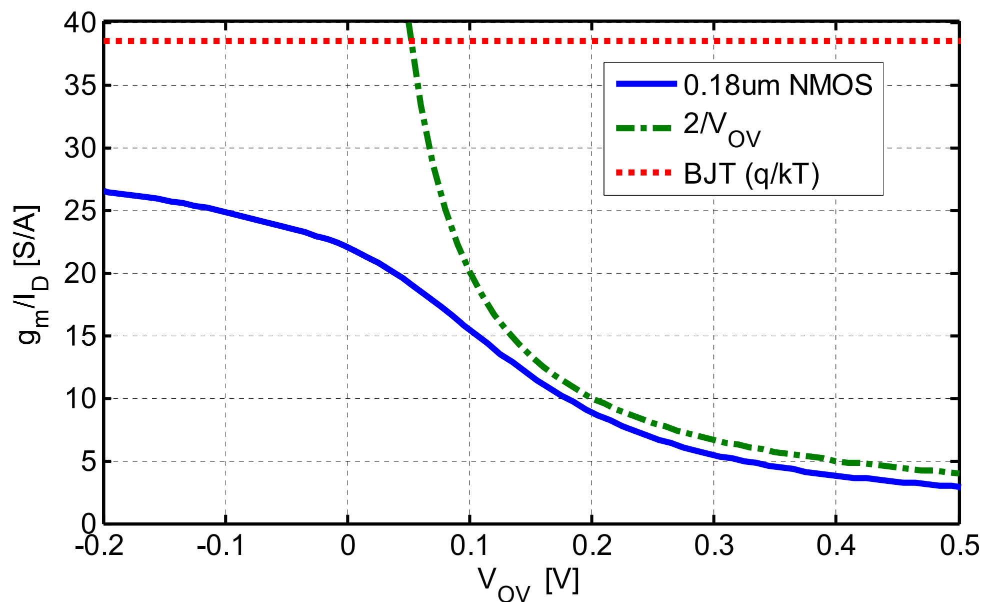
$$\frac{g_m}{g_o} \cong \frac{2}{\lambda V_{OV}}$$

Device Characterization

```
* NMOS characterization

.param  gs=0.7
.param  dd=1.8
vds     d 0       dc      'dd/2'
vgs     g 0       dc      'gs'
mn      d g 0 0   nmos214  L=0.18um  W=5um

.op
.dc gs 0.2V 1V 10mV
.probe ov     = par('gs-vth(mn)')
.probe gm_id  = par('gmo(mn)/i(mn)')
.probe ft     = par('1/6.28*gmo(mn)/cggbo(mn)')
.probe gm_gds = par('gmo(mn)/gdso(mn)')

.options post brief dccap
.inc /usr/class/ee214/hspice/ee214_hspice.sp
.end
```



g_m/I_D Plot

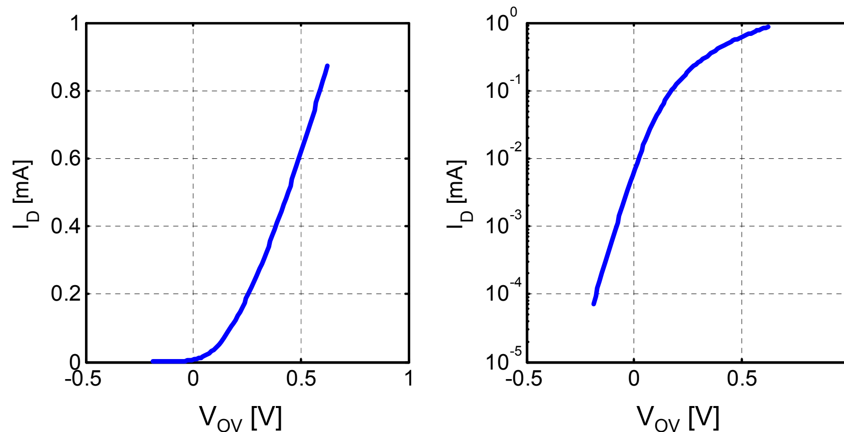


Observations

- Square law prediction is fairly close for $V_{OV} > 150mV$
- Unfortunately g_m/I_D does not approach infinity for $V_{OV} \rightarrow 0$
- It also seems that we cannot do better than a BJT, even though the square law equation would predict this for $0 < V_{OV} < 2kT/q \cong 52mV$
- For further analysis, it helps to identify three distinct operating regions
  - Strong inversion: $V_{OV} > 150mV$
    - Deviations due to short channel effects
  - Subthreshold: $V_{OV} < 0$
    - Behavior similar to a BJT, g_m/I_D nearly constant
  - Moderate Inversion: $0 < V_{OV} < 150mV$
    - Transition region, an interesting mix of the above

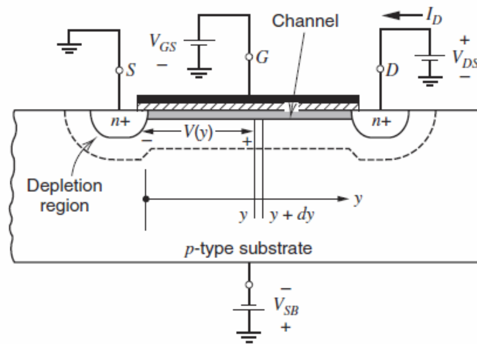
Subthreshold Operation

- A plot of the device current in our previous simulation



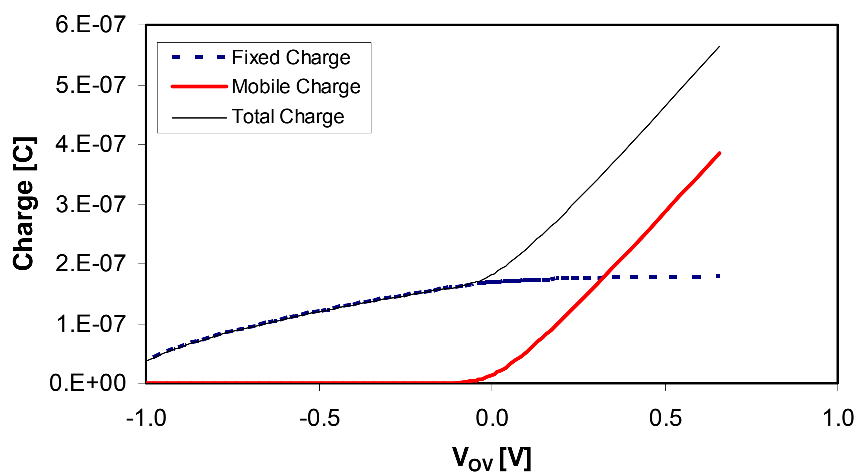
- Questions
  - What determines the current when V_{OV}< 0, i.e. V_{GS}< V_t?
  - What is the definition of V_t?

Definition of V_t



- V_t is defined as the V_{GS} at which the number of electrons at the surface equals the number of doping atoms
- Seems somewhat arbitrary, but makes sense in terms of surface charge control

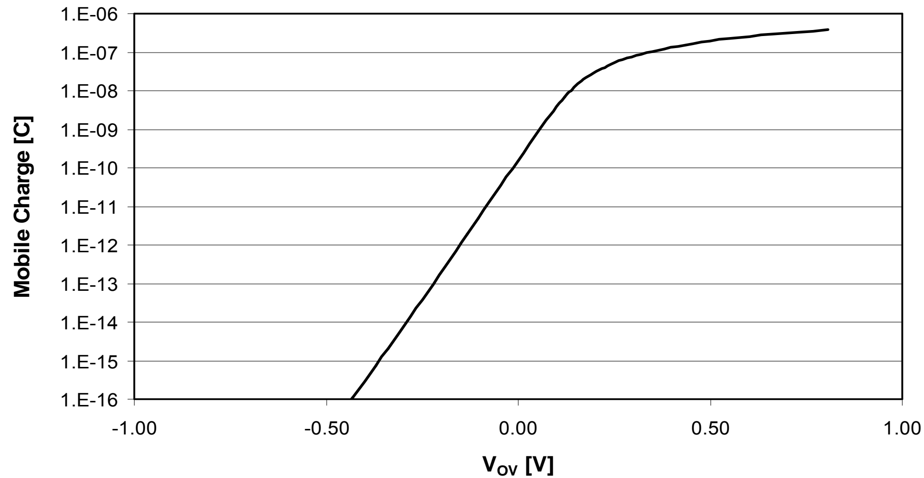
Mobile Charge versus V_{OV}



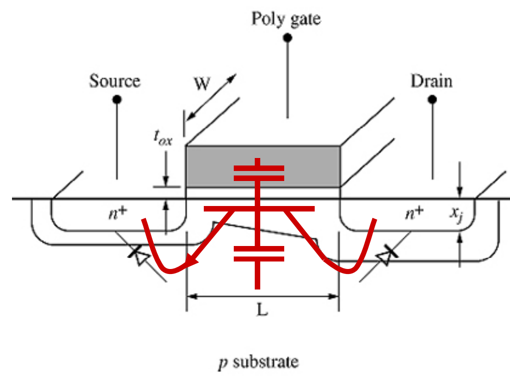
- Around $V_{GS}=V_t$ ($V_{OV}=0$), the relationship between mobile charge in the channel and gate voltage becomes linear ($Q_n \sim C_{ox}V_{OV}$)
  - Exactly what we assumed to derive the long channel model

Mobile Charge on a Log Scale

- On a log scale, we see that there are mobile charges **before** we reach the threshold voltage
  - Fundamental result of solid-state physics, not short channels



BJT Similarity



- We have
  - An NPN sandwich, mobile minority carriers in the P region
- This is a BJT!
  - Except that the base potential is here controlled through a capacitive divider, and not directly by an electrode

Subthreshold Current

- We know that for a BJT

$$I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \qquad V_T = \frac{kT}{q}$$

- For the MOSFET in subthreshold we have

$$I_D = I_0 \cdot e^{\frac{V_{GS}-V_t}{nV_T}}$$

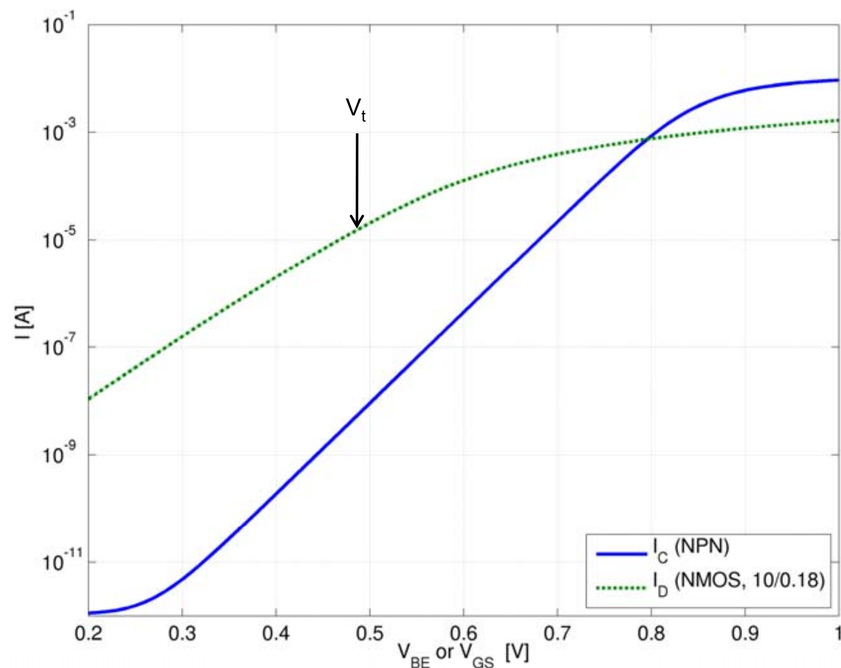
- n is given by the capacitive divider

$$n = \frac{C_{js} + C_{ox}}{C_{ox}} = 1 + \frac{C_{js}}{C_{ox}}$$

where C_{js} is the depletion layer capacitance

- In the EE214 technology $n \cong 1.5$

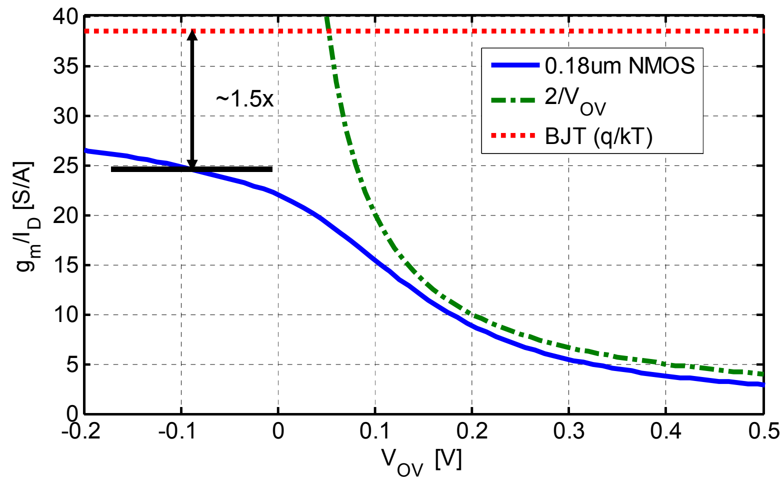
Comparison – NMOS versus NPN



Subthreshold Transconductance

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{1}{n}\frac{I_D}{V_T} \qquad \frac{g_m}{I_D} = \frac{1}{nV_T}$$

- Similar to BJT, but unfortunately n (≅1.5) times lower



Moderate Inversion

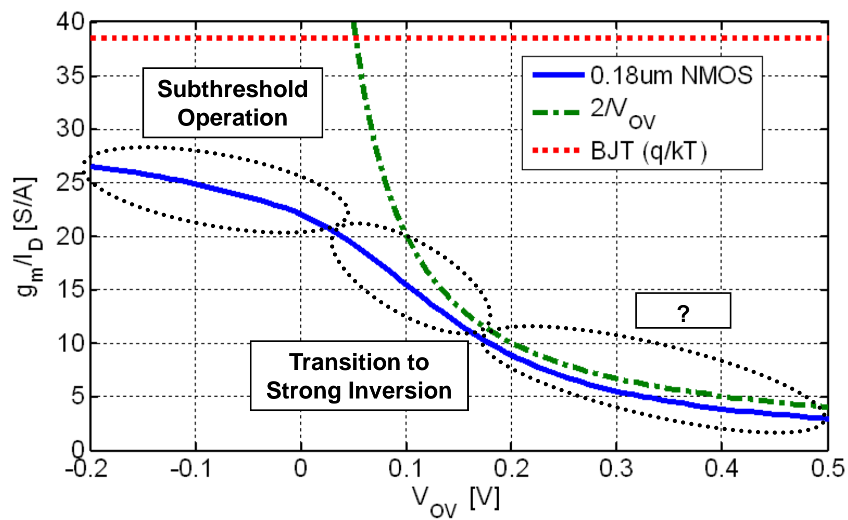
- In the transition region between subthreshold and strong inversion, we have two different current mechanisms

Drift (MOS) $\nu = \mu E$

Diffusion (BJT) $\nu = D\frac{dn}{dx} = \frac{kT}{q}\mu\frac{dn}{dx}$

- Both current components are always present
  - Neither one clearly dominates in moderate inversion
- Can show that ratio of drift/diffusion current ~$(V_{GS}-V_t)/(kT/q)$
  - MOS equation becomes dominant at several kT/q

Re-cap



- What causes the discrepancy between $2/V_{OV}$ and 0.18µm NMOS in strong inversion?

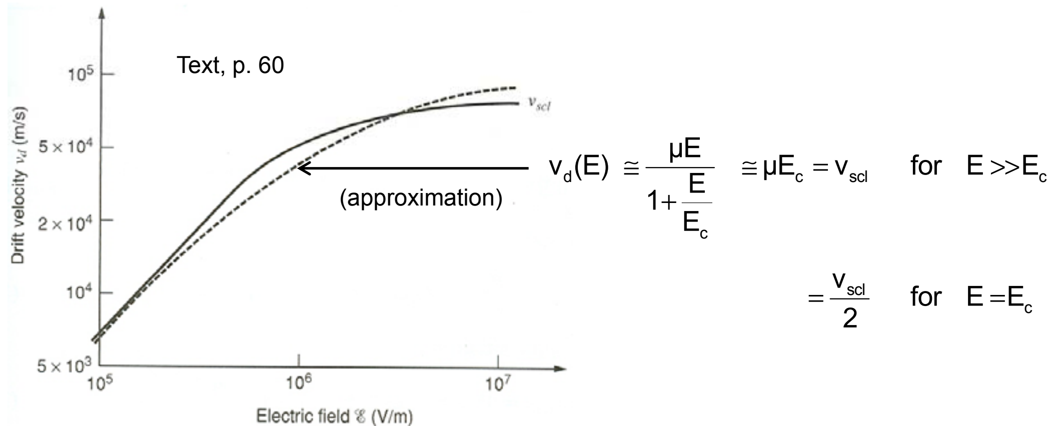
Short Channel Effects

- Velocity saturation due to high lateral field
- Mobility degradation due to high vertical field
- V_t dependence on channel length and width
- $V_t = f(V_{DS})$
- $r_o = f(V_{DS})$
- …

- We will limit the discussion in EE214 to the first two aspects of the above list, with a focus on qualitative understanding

Velocity Saturation (1)

- In the derivation of the square law model, it is assumed that the carrier velocity is proportional to the lateral E-field, $v=\mu E$
- Unfortunately, the speed of carriers in silicon is limited ($v_{scl} \cong 10^5$ m/s)
  - At very high fields (high voltage drop across the conductive channel), the carrier velocity saturates



Velocity Saturation (2)

- It is important to distinguish various regions in the above plot
  - Low field, the long channel equations still hold
  - Moderate field, the long channel equations become somewhat inaccurate
  - Very high field across the conducting channel – the velocity saturates completely and becomes essentially constant (v_{scl})
- To get some feel for latter two cases, let's first estimate the E field using simple long channel physics
- In saturation, the lateral field across the channel is

$$E = \frac{V_{OV}}{L} \quad \text{e.g.} \quad \frac{200\text{mV}}{0.18\mu\text{m}} = 1.11 \cdot 10^6 \frac{\text{V}}{\text{m}}$$

Field Estimates

- In our 0.18μm technology, we have for an NMOS device

$$E_c = \frac{v_{scl}}{\mu} \cong \frac{10^5 \frac{m}{s}}{150 \frac{cm^2}{Vs}} = 6.7 \cdot 10^6 \frac{V}{m}$$

Therefore

$$\frac{E}{E_c} = \frac{1.11 \cdot 10^6 \frac{V}{m}}{6.7 \cdot 10^6 \frac{V}{m}} \cong 0.16$$

- This means that for V_{OV} on the order of 0.2V, the carrier velocity is somewhat reduced, but the impairment is relatively small
- The situation changes when much larger V_{OV} are applied, e.g. as the case in digital circuits

Short Channel I_D Equation

- A simple equation that captures the moderate deviation from the long channel drain current can be written as (see text, p. 62)

$$I_D \cong \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OV}^2 \cdot \frac{1}{\left(1+\frac{V_{OV}}{E_cL}\right)}$$

$$\cong \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{OV} \cdot \underbrace{\frac{E_cL \cdot V_{OV}}{(E_cL + V_{OV})}}$$

Think of this as a “parallel combination"

Minimum-length NMOS: $E_cL = 6.7 \cdot 10^6 \frac{V}{m} \cdot 0.18\mu m = 1.2V$

Minimum-length PMOS: $E_cL = 16.75 \cdot 10^6 \frac{V}{m} \cdot 0.18\mu m = 3V$

Modified g_m/I_D Expression

- Assuming V_{OV} << E_cL, we can show that (see text, pp. 63-64)

$$\frac{g_m}{I_D} \cong \frac{2}{V_{OV}} \cdot \frac{1}{\left(1+\frac{V_{OV}}{E_cL}\right)}$$

- E.g. for an NMOS device with V_{OV}=200mV

$$\frac{g_m}{I_D} \cong \frac{2}{V_{OV}} \cdot \frac{1}{\left(1+\frac{0.2}{1.2}\right)} = \frac{2}{V_{OV}} \cdot 0.86$$

- Means that the square law model in strong inversion (at $V_{OV} \cong$ 200mV) should be off by about 15%
  - This prediction agrees well with the simulation data

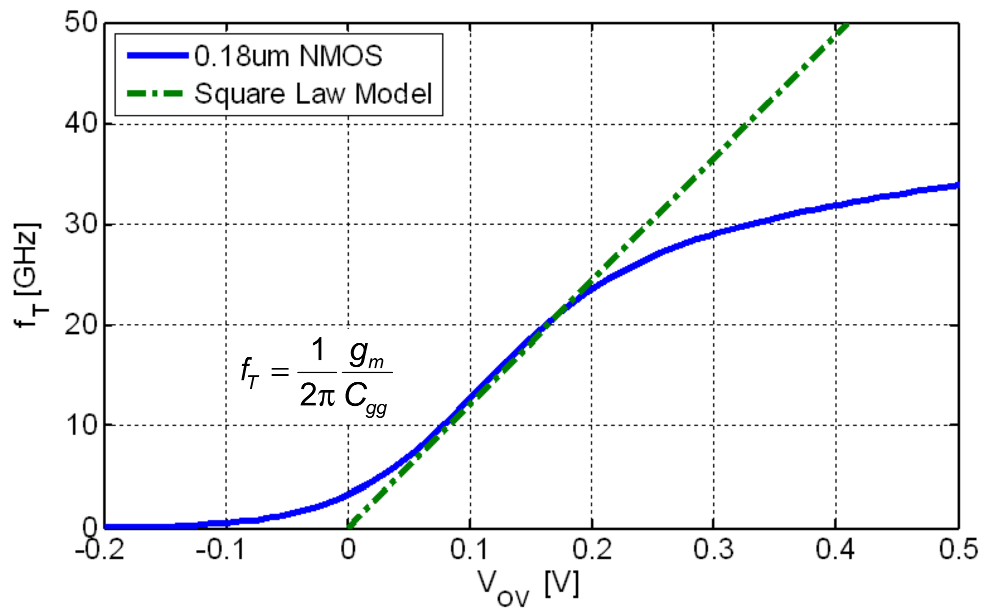
Mobility Degradation due to Vertical Field

- In MOS technology, the oxide thickness has been continuously scaled down with feature size
  – ~6.5nm in 0.35µm, ~4nm in 0.18µm, ~1.8nm in 90nm CMOS
- As a result, the vertical electric field in the device increases and tries to pull the carriers closer to the "dirty" silicon surface
  – Imperfections impede movement and thus mobility
- This effect can be included by replacing the mobility term with an "effective mobility"

$$\mu_{eff} \cong \frac{\mu}{(1+\theta V_{OV})} \qquad \theta = 0.1...0.4\frac{1}{V}$$

- Yet another "fudge factor"
  – Possible to lump with E_cL parameter, if desired

Transit Frequency Plot

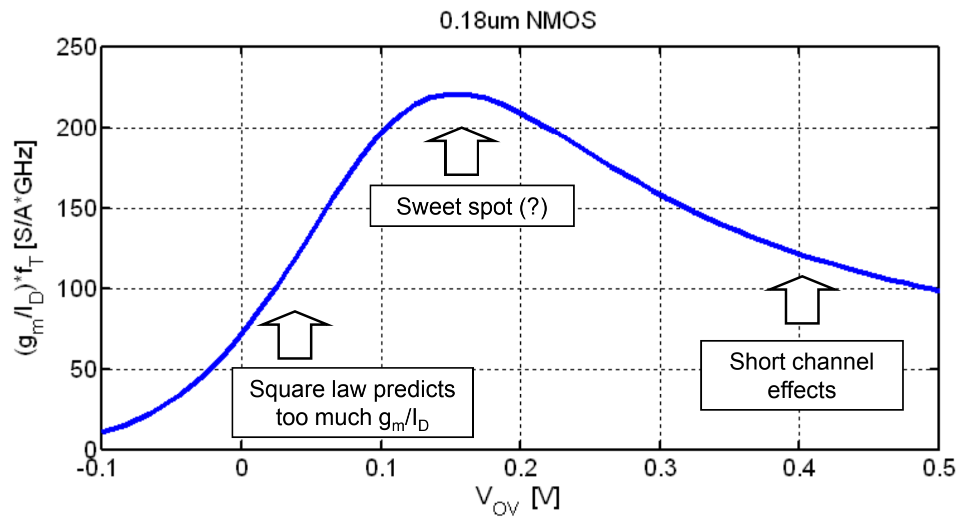


Observations - f_T

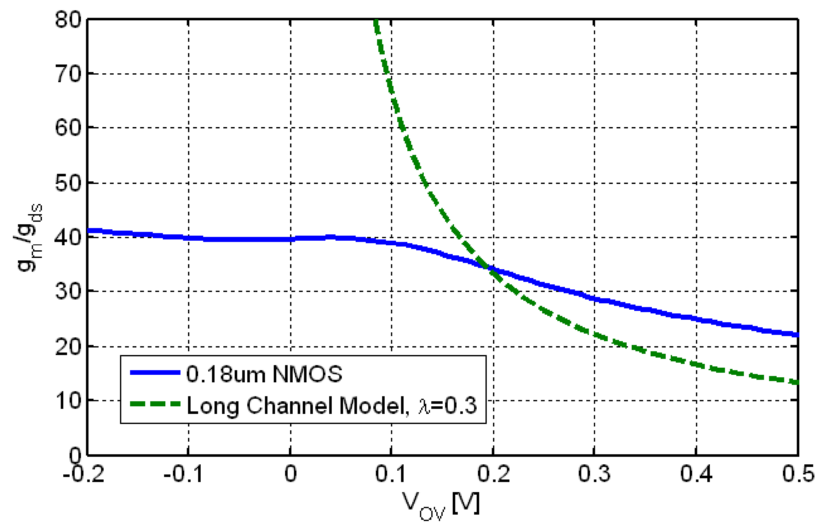
- Again the square-law model doesn't do a very good job
  - Large f_T discrepancy in subthreshold operation and in strong inversion (large V_{OV})
- The reasons for these discrepancies are exactly the same as the ones we came across when looking at g_m/I_D
  - Bipolar action in subthreshold operation and moderate inversion
  - Short channel effects at large V_{OV}
    - Less g_m, hence lower g_m/C_{gg}
- Same conclusion: we won't be able to make good predictions with a simple square law relationship

$g_m/I_D \cdot f_T$ Plot

Square Law: $$\frac{g_m}{I_D} \cdot f_T \cong \frac{1}{2\pi} \frac{3\mu}{L^2}$$

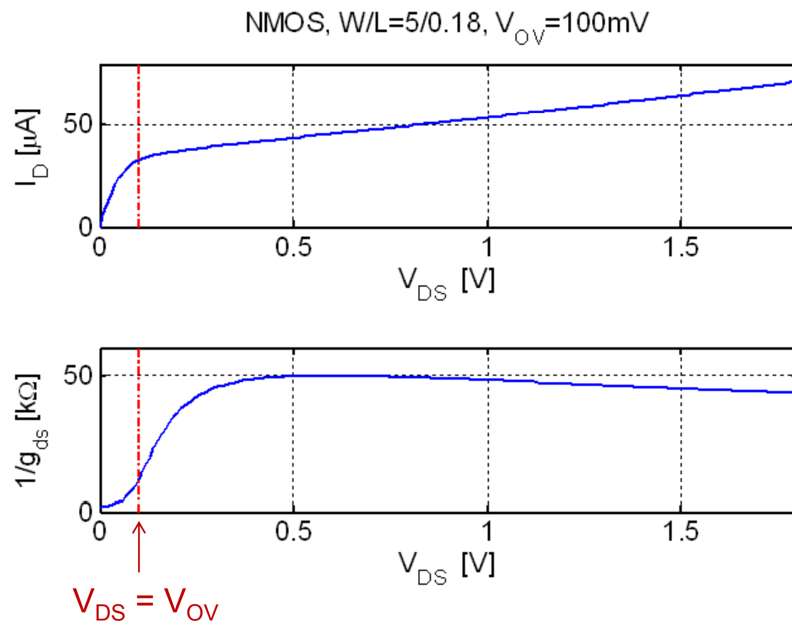


Intrinsic Gain Plot

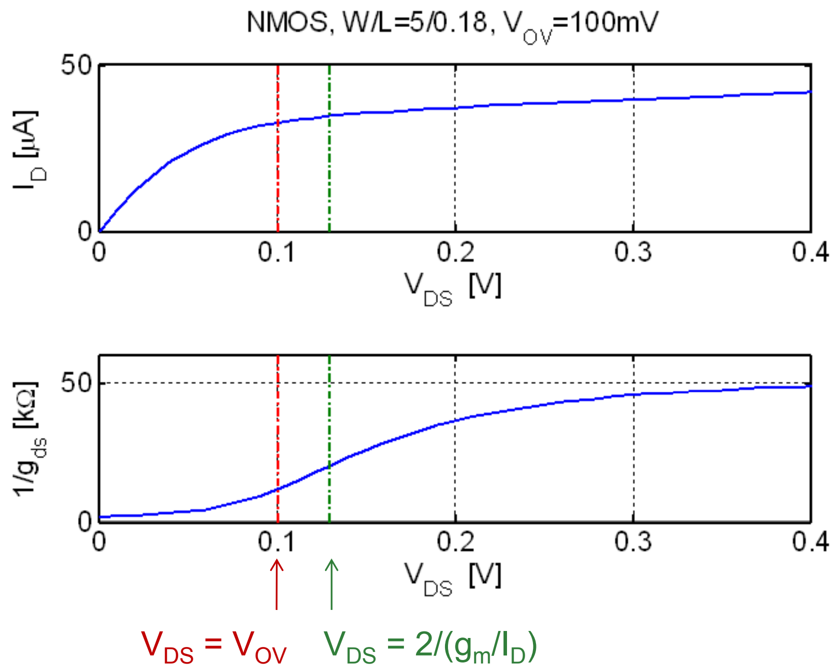


- Impossible to approximate with the "λ" model equation!

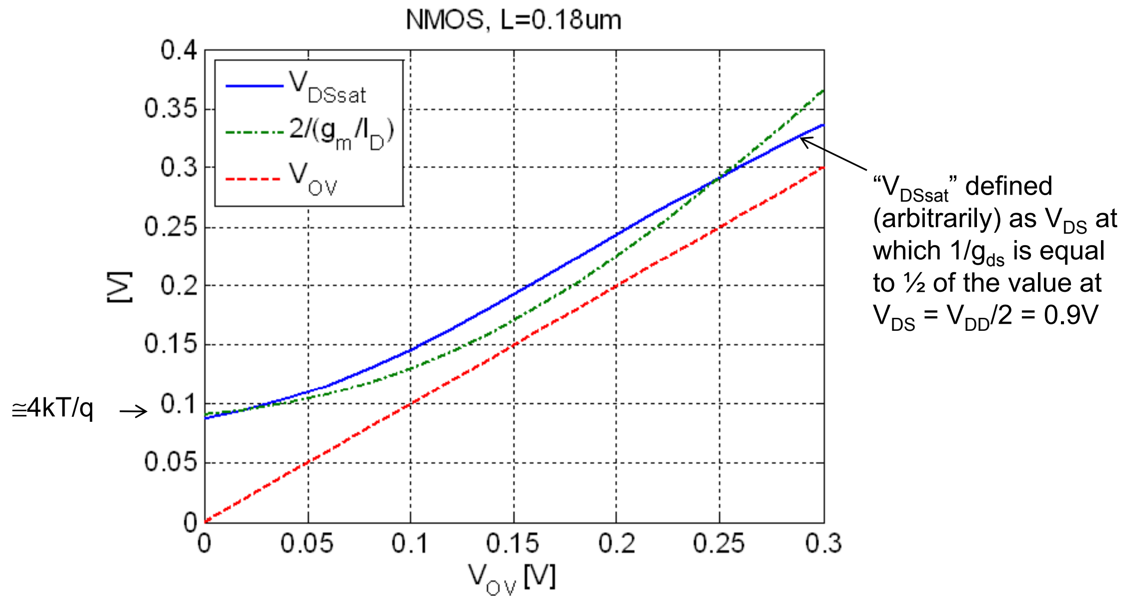
Gradual Onset of $1/g_{ds}$



Gradual Onset of $1/g_{ds}$ (Zoom)



"V_{DSsat}" Estimate Based on g_m/I_D



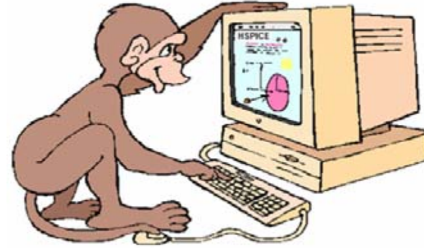
- $V^* = 2/(g_m/I_D)$ is a reasonable estimate of "V_{DSsat}"

Observations – Intrinsic Gain

- Device shows a rather gradual transition from triode to saturation
  - Square law predicts an abrupt change from small to large intrinsic gain at $V_{DS} = V_{OV}$
  - $V^* = 2/(g_m/I_D)$ provides a reasonable estimate for the minimum V_{DS} that is needed to extract gain from a device
    - Typically want to stay at least 100mV above this value in practical designs
- The physics that govern the behavior of $r_o=1/g_{ds}$ are complex
  - Channel length modulation
  - Drain induced barrier lowering (DIBL)
  - Substrate current induced body effect (SCBE)
    - Not present in all technologies and/or PMOS devices
- If you are interested in more details, please refer to EE316 or similar

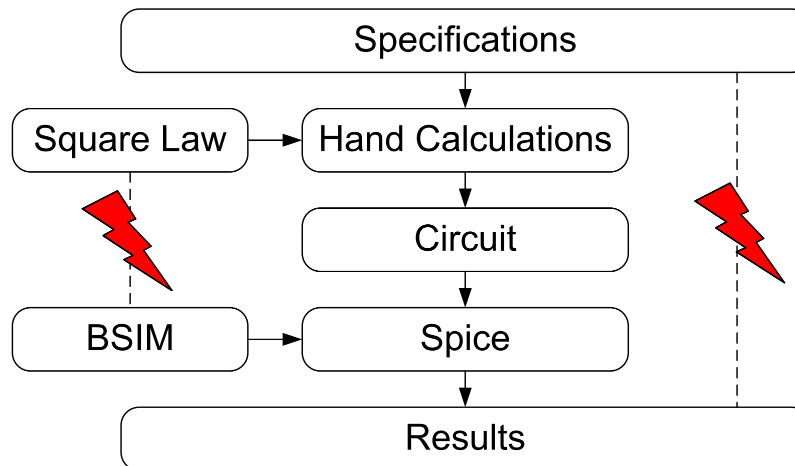
The Challenge

- Square-law model is inadequate for design in fine-line CMOS
  - But simulation models (BSIM, PSP, …) are too complex for hand-calculations
- This issue tends to drive many designers toward a "spice monkey" design methodology
  - No hand calculations, iterate in spice until the circuit "somehow" meets the specifications
  - Typically results in sub-optimal designs
- Our goal
  - Maintain a systematic design methodology in absence of a set of compact MOSFET equations
- Strategy
  - Design using look-up tables or charts

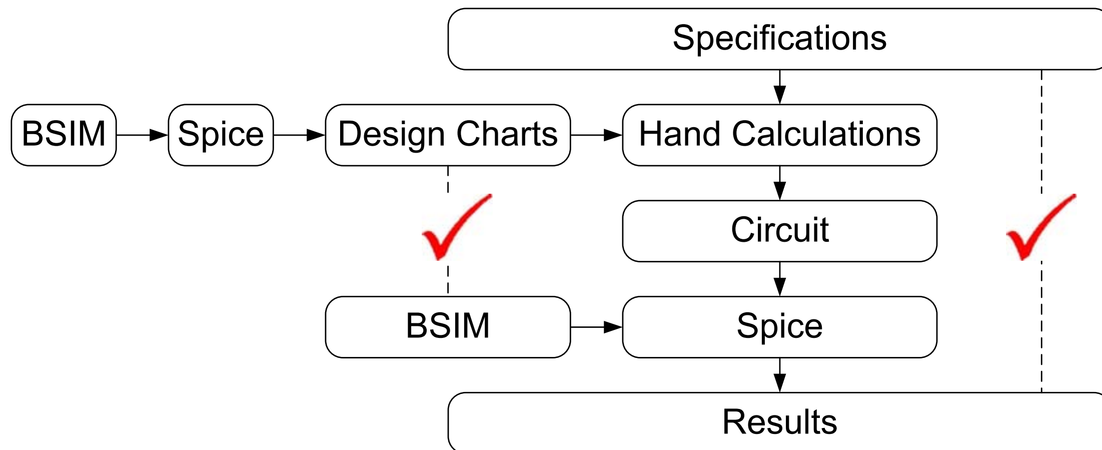


[Courtesy Isaac Martinez]

The Problem



The Solution

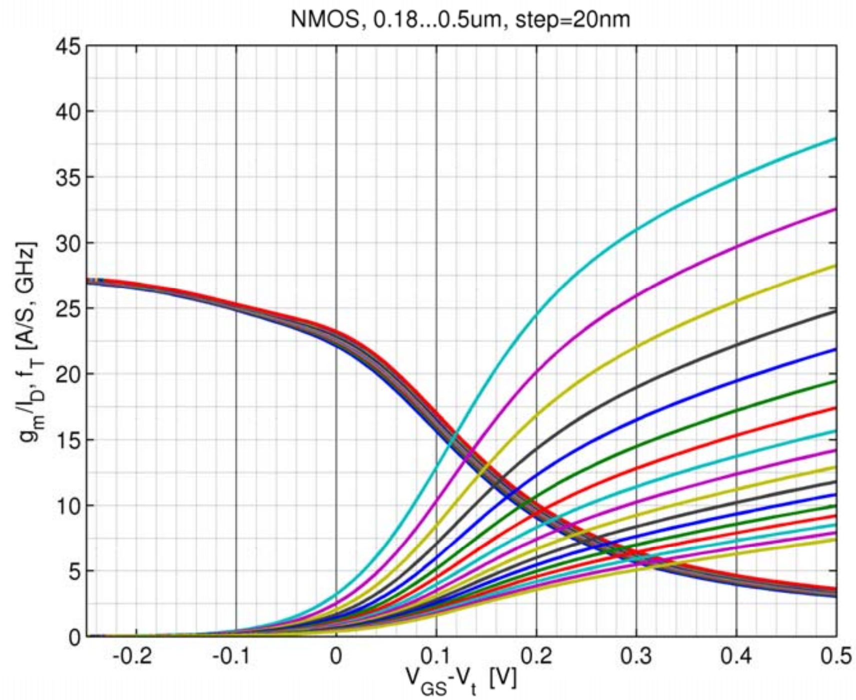


- Use pre-computed spice data in hand calculations

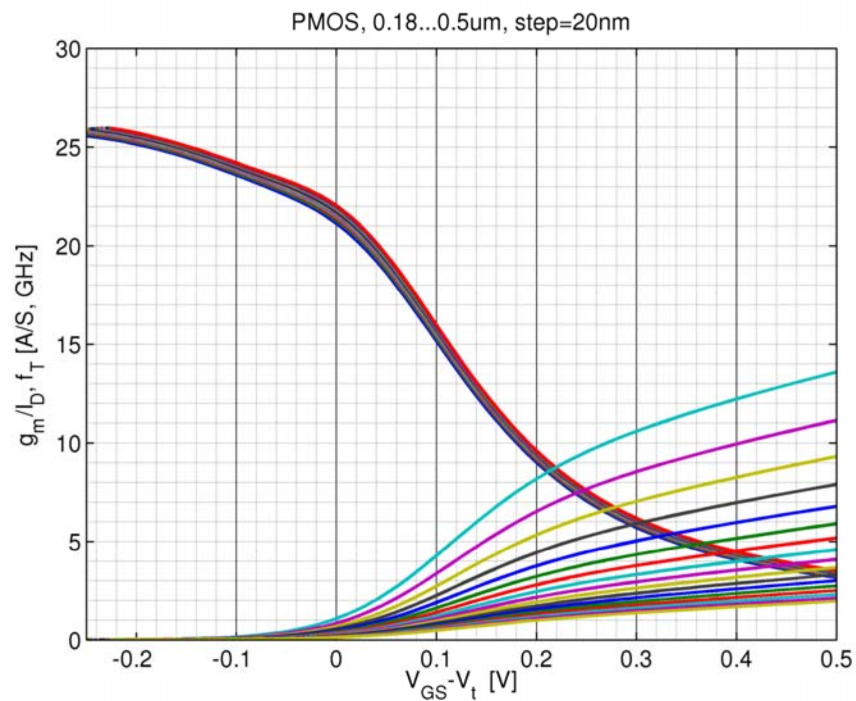
Technology Characterization for Design

- Plot the following parameters for a reasonable range of g_m/I_D and channel lengths
  - Transit frequency (f_T)
  - Intrinsic gain (g_m/g_{ds})
  - Current density (I_D/W)
- In addition, may want to tabulate relative estimates of extrinsic capacitances
  - C_{gd}/C_{gg} and C_{dd}/C_{gg}
- Parameters are (to first order) independent of device width
  - Enables "normalized design" and re-use of charts
  - Somewhat similar to filter design procedure using normalized coefficient tables
- Do hand calculations using the generated technology data
  - Can use Matlab functions to do table-look-up on pre-computed data

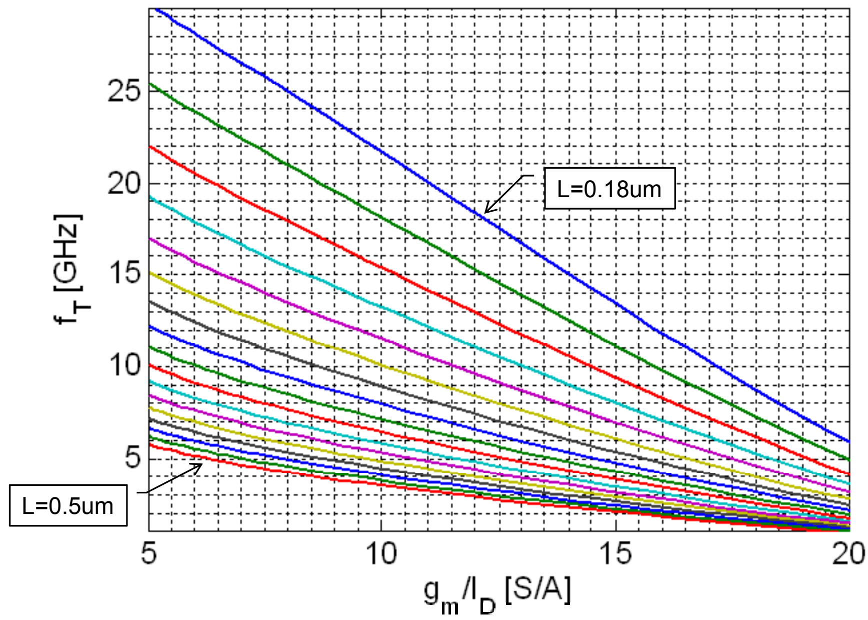
NMOS Simulation Data



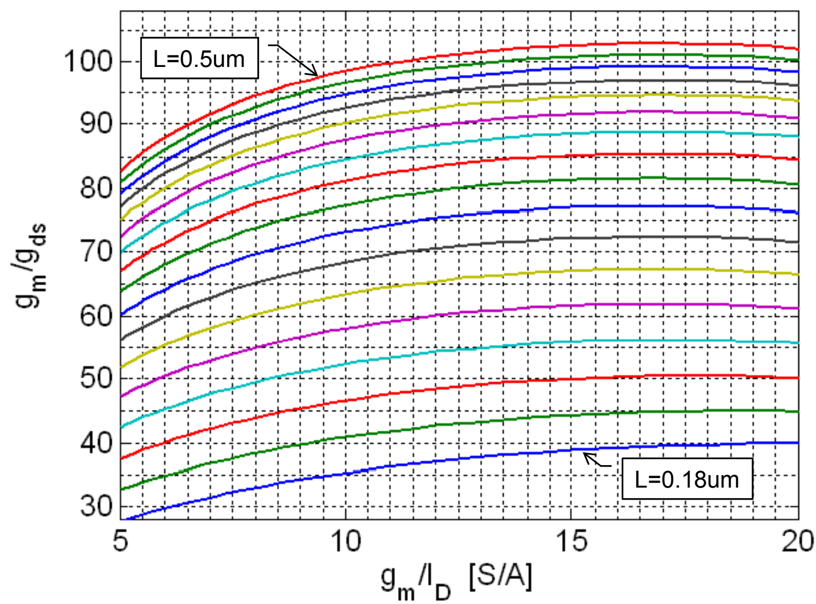
PMOS Simulation Data



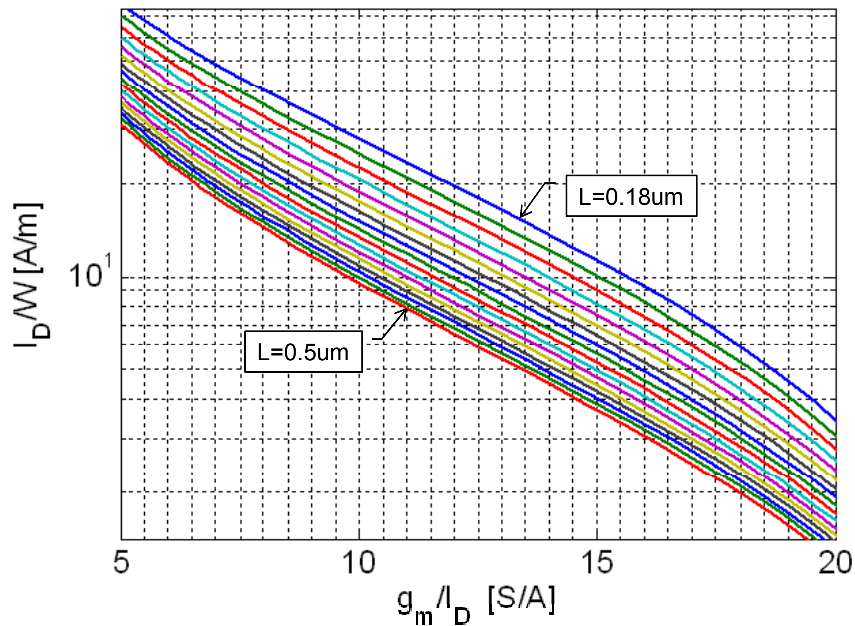
Transit Frequency Chart



Intrinsic Gain Chart



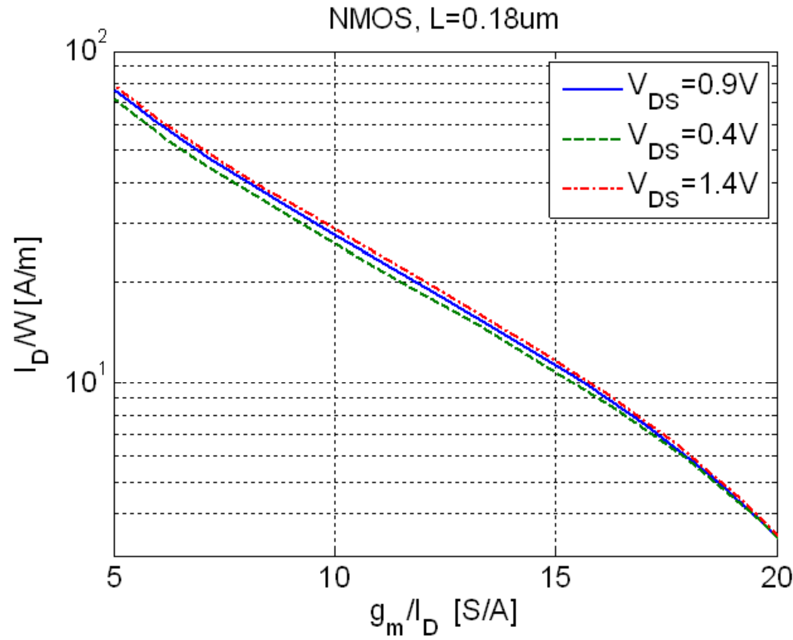
Current Density Chart



Lookup Functions in Matlab

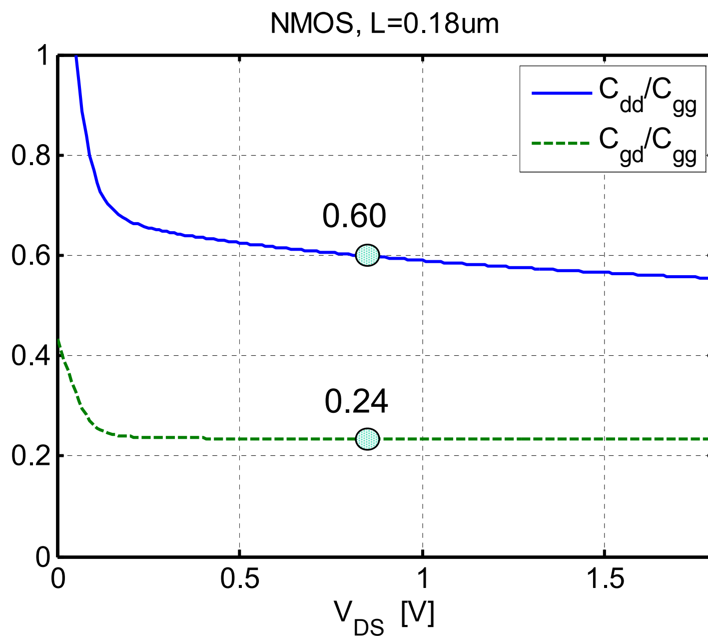
```
% Set up path and load simulation data (for VDS=0.9V)
addpath('/usr/class/ee214/matlab');
load techchar.mat;

% Lookup fT for NMOS, L=0.18um, at gm/ID=10S/A
lookup_ft(tech, 'n', 0.18e-6, 10)
ans =    2.2777e+10

% Lookup gm/ID for NMOS, L=0.18um, at fT=20GHz
lookup_gmid(tech, 'n', 0.18e-6, 20e9)
ans =    11.5367

% Lookup ID/W for NMOS, L=0.18um, at gm/ID=10S/A
lookup_idw(tech, 'n', 0.18e-6, 10)
ans =    29.3281
```

V_{DS} Dependence



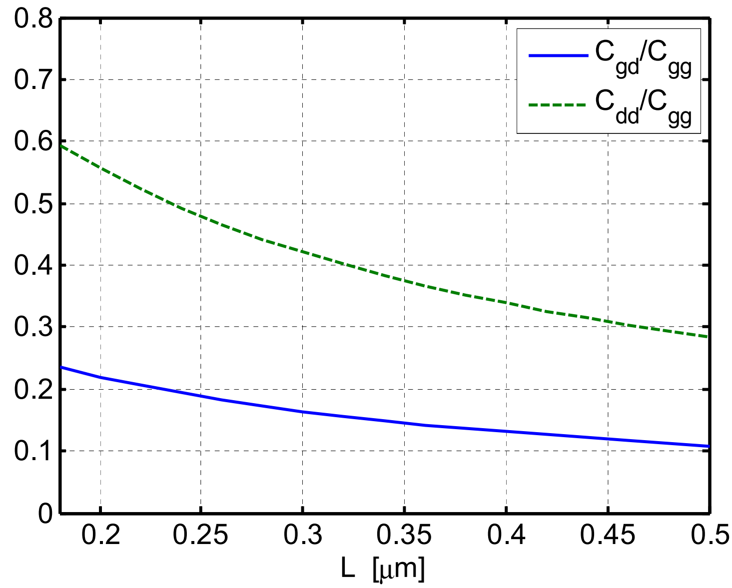
- V_{DS} dependence is relatively weak
- Typically OK to work with data generated for $V_{DD}/2$

Extrinsic Capacitances (1)

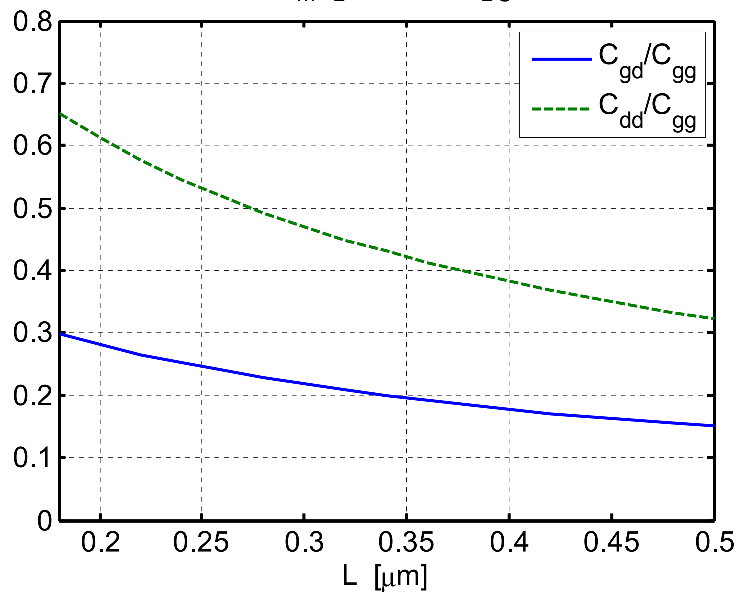


- Again, usually OK to work with estimates taken at $V_{DD}/2$

Extrinsic Capacitances (2)



Extrinsic Capacitances (3)

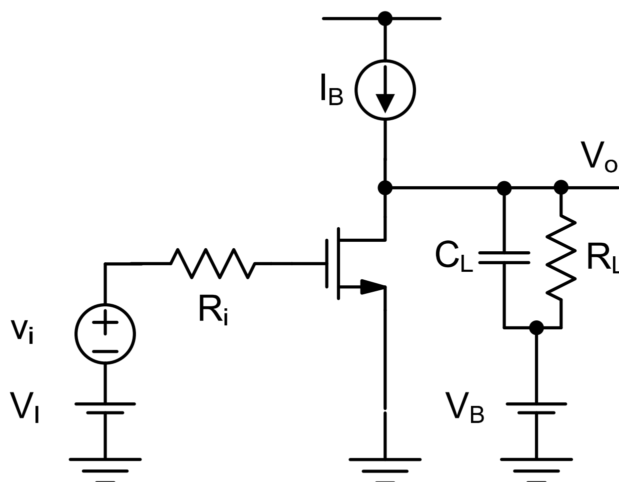


Generic Design Flow

1) Determine g_m (from design objectives)
2) Pick L
   - Short channel → high f_T (high speed)
   - Long channel → high intrinsic gain
3) Pick g_m/I_D (or f_T)
   - Large g_m/I_D → low power, large signal swing (low V_{DSsat})
   - Small g_m/I_D → high f_T (high speed)
4) Determine I_D (from g_m and g_m/I_D)
5) Determine W (from I_D/W, current density chart)

Many other possibilities exist (depending on circuit specifics, design constraints and objectives)

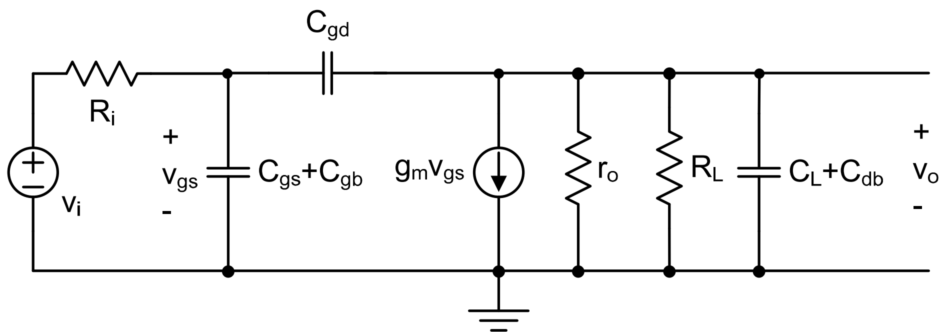
Basic Design Example



Given specifications and objectives

- 0.18µm technology
- DC gain = -4
- R_L=1k, C_L=50fF, R_i=10k
- Maximize bandwidth while keeping $I_B \leq$ 300uA
  - Implies $L=L_{min}$=0.18um
- Determine device width
- Estimate dominant and non-dominant pole

Small-Signal Model



Calculate g_m and g_m/I_D

$$\left|A_v(0)\right| \cong g_m R_L = 4 \quad \Rightarrow \quad g_m = \frac{4}{1k\Omega} = 4mS$$

$$\boxed{\frac{g_m}{I_D} = \frac{4mS}{300\mu A} = 13.3\frac{S}{A}}$$

Why can we Neglect r_o?

$$\left|A_v(0)\right| = g_m\left(R_L \,||\, r_o\right)$$

$$= g_m\left(\frac{1}{R_L} + \frac{1}{r_o}\right)^{-1}$$

$$\frac{1}{\left|A_v(0)\right|} = \frac{1}{g_m R_L} + \frac{1}{g_m r_o}$$

$$\frac{1}{4} = \frac{1}{g_m R_L} + \cancel{\frac{1}{g_m r_o}}$$

- Even at $L=L_{min}$= 0.18µm, we have $g_m r_o > 30$
- r_o will be negligible in this design problem

Zero and Pole Expressions

High frequency zero (negligible)

$$\omega_z \cong \frac{g_m}{C_{gd}} >> \omega_T$$

Dominant pole (see Chapter 4)

$$\omega_{p1} \cong \frac{1}{R_i\left[C_{gs}+C_{gb}+\left(1+g_mR_L\right)\cdot C_{gd}\right]}$$

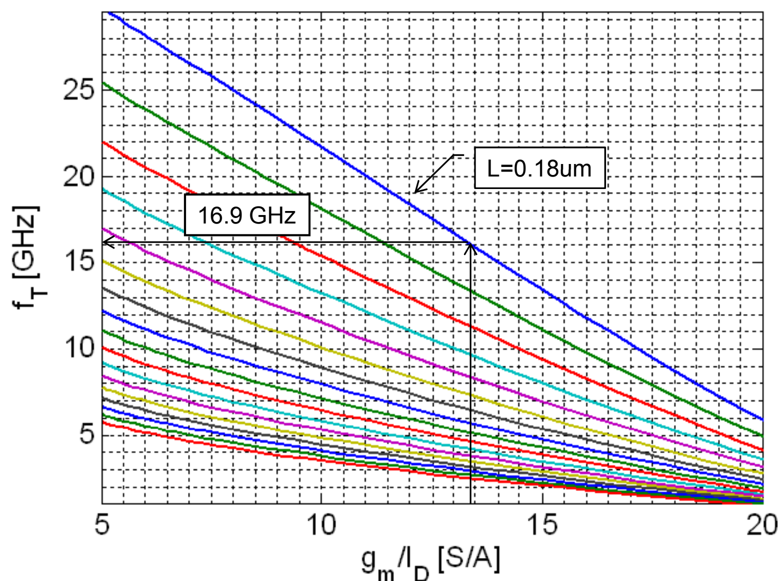
Nondominant pole (see Chapter 4)

$$\omega_{p2} \cong \frac{1}{\omega_{p1}}\frac{1}{R_iR_L\left(\left[C_{gs}+C_{gb}\right]C_L+\left[C_{gs}+C_{gd}\right]C_{db}+C_LC_{gd}\right)}$$

Calculation of capacitances from tabulated parameters:

$$C_{gs}+C_{gb}=C_{gg}-C_{gd} \qquad C_{db}=C_{dd}-C_{gd}$$

Determine C_{gg} via f_T Look-up



Find Capacitances and Plug in

$$C_{gg} = \frac{1}{2\pi}\frac{g_m}{f_T} = \frac{1}{2\pi}\frac{4mS}{16.9GHz} = 37.7fF$$

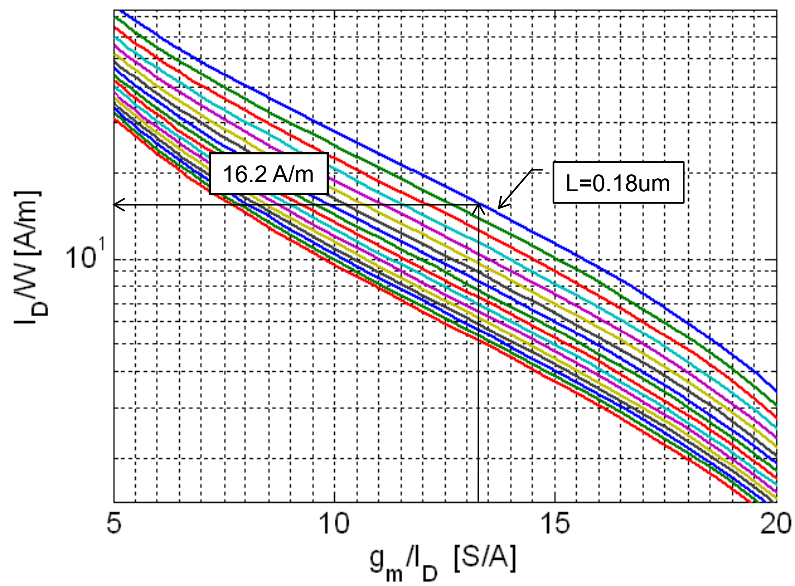
$$C_{gd} = \frac{C_{gd}}{C_{gg}}C_{gg} = 0.24 \cdot 37.7fF = 9.0fF$$

$$C_{dd} = \frac{C_{dd}}{C_{gg}}C_{gg} = 0.60 \cdot 39.4fF = 23.6fF$$

$\therefore f_{p1} \cong 196\ \text{MHz}$

$\therefore f_{p2} \cong 6.0\ \text{GHz}$

Device Sizing

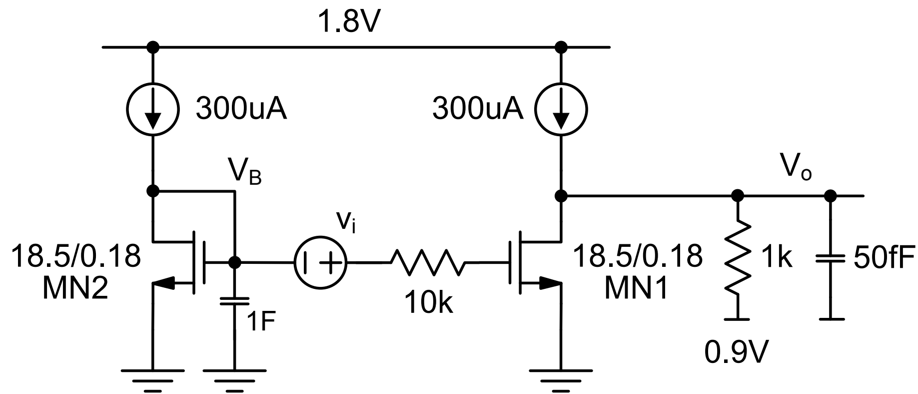


Circuit For Spice Verification

Device width

$$W = \frac{I_D}{\frac{I_D}{W}} = \frac{300\mu A}{16.2A/m} = 18.5\mu m$$

Simulation circuit



Simulated DC Operating Point

element	0:mn1	Calculation
region	Saturati	
id	326.8330u	300 uA
vgs	624.9116m	
vds	873.1670m	
vdsat	113.7463m	
vod	138.5878m	
gm	4.1668m	4 mS
gds	108.2225u	
...		
cdtot	21.8712f	23.6 fF
cgtot	37.6938f	37.7 fF
cgd	8.9163f	9.0 fF
...		
gm/ID	12.8	13.3 S/A

Good agreement!

HSpice .OP Capacitance Output Variables

HSpice (.OP)

```
cdtot    21.8712f
cgtot    37.6938f
cstot    44.2809f
cbtot    34.9251f
cgs      26.7303f
cgd       8.9163f
```

Corresponding Small Signal Model Elements

cdtot $\equiv C_{gd} + C_{db}$

cgtot $\equiv C_{gs} + C_{gd} + C_{gb}$

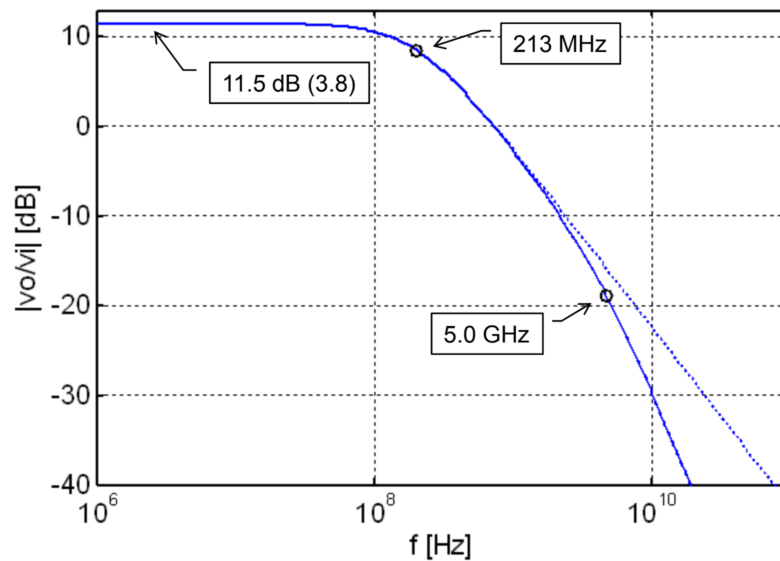
cstot $\equiv C_{gs} + C_{sb}$

cbtot $\equiv C_{gb} + C_{sb} + C_{db}$

cgs $\equiv C_{gs}$

cgd $\equiv C_{gd}$

Simulated AC Response



- Calculated values: $|A_v(0)|$=12 dB (4.0), f_{p1}=196 MHz, f_{p2}=6.0 GHz

Using .pz Analysis

Netlist statement

```
.pz v(vo) vi
```

Output

```
***************************************************
******   pole/zero analysis
input =  0:vi          output = v(vo)

       poles (rad/sec)                 poles ( hertz)
 real              imag              real              imag
 -1.34190g         0.                -213.569x         0.
 -31.4253g         0.                -5.00149g         0.

       zeros (rad/sec)                 zeros ( hertz)
 real              imag              real              imag
 458.247g          0.                72.9323g          0.
```


Observations

- The design and pole calculations essentially right on target!
  – Typical discrepancies are on the order of 10-20%, mostly due to V_{DS} dependencies, finite output resistance, etc.
- We accomplished this by using pre-computed spice data in the design process
- Even if discrepancies are more significant, there's always the possibility to track down the root causes
  – Hand calculations are based on parameters that also exist in Spice, e.g. g_m/I_D, f_T, etc.
  – Different from square law calculations using μC_{ox}, V_{OV}, etc.
    - Based on artificial parameters that do not exist or have no significance in the spice model

References

- F. Silveira et al. "A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, Sep. 1996, pp. 1314-1319.
- D. Foty, M. Bucher, D. Binkley, "Re-interpreting the MOS transistor via the inversion coefficient and the continuum of g_{ms}/I_d," *Proc. Int. Conf. on Electronics, Circuits and Systems*, pp. 1179-1182, Sep. 2002.
- B. E. Boser, "Analog Circuit Design with Submicron Transistors," IEEE SSCS Meeting, Santa Clara Valley, May 19, 2005, http://www.ewh.ieee.org/r6/scv/ssc/May1905.htm
- P. Jespers, *The g_m/I_D Methodology, a sizing tool for low-voltage analog CMOS Circuits*, Springer, 2010.
- T. Konishi, K. Inazu, J.G. Lee, M. Natsu, S. Masui, and B. Murmann, “Optimization of High-Speed and Low-Power Operational Transconductance Amplifier Using g_m/I_D Lookup Table Methodology,” IEICE Trans. Electronics, Vol. E94-C, No.3, Mar. 2011.

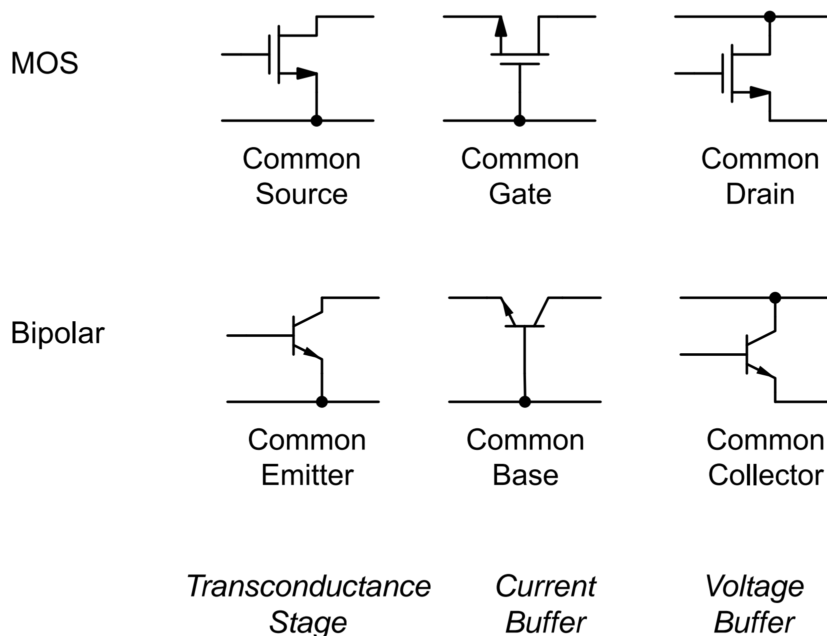
Chapter 4
Review of Elementary Circuit Configurations

B. Murmann

Stanford University

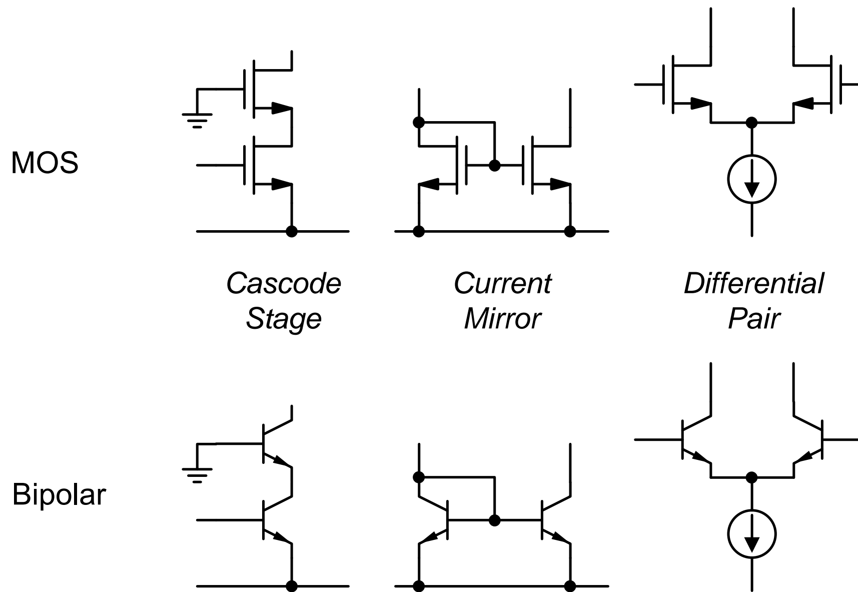
Reading Material: Sections 3.3.1, 3.3.3, 3.3.6, 3.3.8, 3.5, 7.2.3, 7.2.4.1, 7.3.2, 7.3.4, 4.2.2, 4.2.3, 4.2.4

Basic Single-Stage Amplifier Configurations



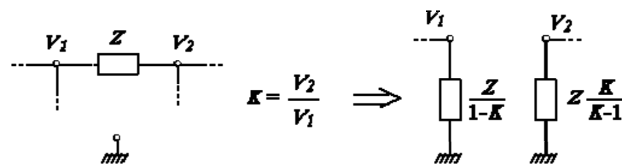
Transconductance Stage | *Current Buffer* | *Voltage Buffer*

Widely Used Two-Transistor Circuits



Analysis Techniques (1)

- Nodal analysis (KCL, KVL)
  - Write KCL for each node, solve for desired transfer function or port impedance
  - Most general method, but conveys limited qualitative insight and often yields high-entropy expressions
- Miller theorem



http://paginas.fe.up.pt/~fff/eBook/MDA/Teo_Miller.html

- Miller approximation
  - Approximate the gain across Z as frequency independent, i.e. K(s) ≅ K for the frequency range of interest
  - This approximation requires a check (or good intuition)

Analysis Techniques (2)

- Dominant pole approximation

$$\frac{1}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} = \frac{1}{1-\frac{s}{p_1}-\frac{s}{p_2}+\frac{s^2}{p_1p_2}} \cong \frac{1}{1-\frac{s}{p_1}+\frac{s^2}{p_1p_2}}$$

$$\text{Given} \quad \frac{1}{1+b_1s+b_2s^2} \Rightarrow p_1 \cong -\frac{1}{b_1}, \quad p_2 \cong -\frac{b_1}{b_2}$$

- Zero value time constant analysis
  - The coefficient b_1 can be found by summing all zero value time constants in the circuit

$$b_1 = \sum \tau_i$$

- Generalized time constant analysis
  - Can also find higher order terms (e.g. b_2) using a sum of time constant products
  - A. Hajimiri, "Generalized Time- and Transfer-Constant Circuit Analysis," IEEE Trans. Circuits Syst. I, pp. 1105-1121, June 2010.

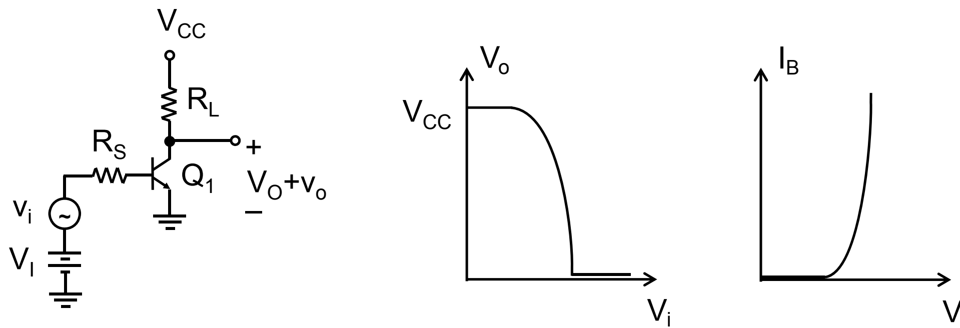
Analysis Techniques (3)

- Return ratio analysis
  - See text pp. 599-612
- Blackman's impedance formula
  - See text pp. 607-612
- Two-port feedback analysis
  - See text pp. 557-587
  - More later in this course

Chapter Overview

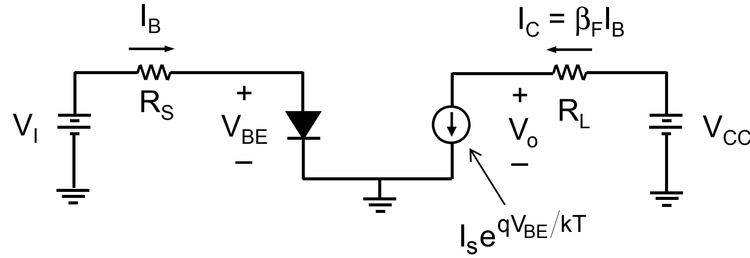
- BJT-centric review of elementary circuit configurations
  - Highlight differences to MOS circuits
- Single-stage amplifiers
  - Common emitter stage
  - Common emitter stage with source degeneration
  - Common collector stage
  - Common base stage
  - Common gate stage (discussion of bulk connection)
- BJT current mirrors
- BJT differential pair

Common-Emitter Stage



- DC input bias voltage (V_I) biases Q_1 in the forward active region
- Typically, want $V_O \cong V_{CC}/2$
- Main differences to consider versus common-source stage (MOS)
  - Bias point sensitivity
  - Finite input resistance (due to r_π)
  - Base resistance (r_b) often significant

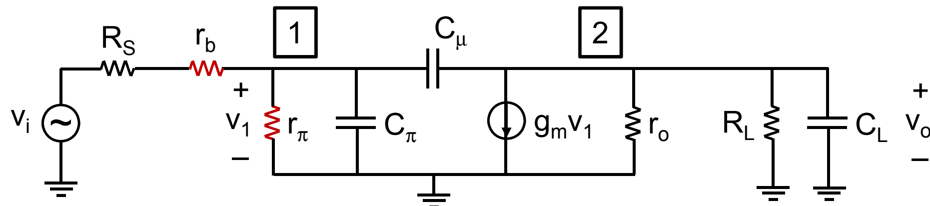
Bias Point Sensitivity



$$I_B \cong \frac{V_I - V_{BE(on)}}{R_S} \qquad V_O = V_{CC} - I_C R_L = V_{CC} - \beta_F I_B R_L = V_{CC} - \beta_F \frac{R_L}{R_S}\left(V_I - V_{BE(on)}\right)$$

- The dependence on β_F makes "direct voltage biasing" impractical
- How to generate V_I so as to control V_o?
- Practical configurations are usually based on feedback, replica biasing, ac coupling or differential circuits

Small-Signal Equivalent Circuit for CE Stage



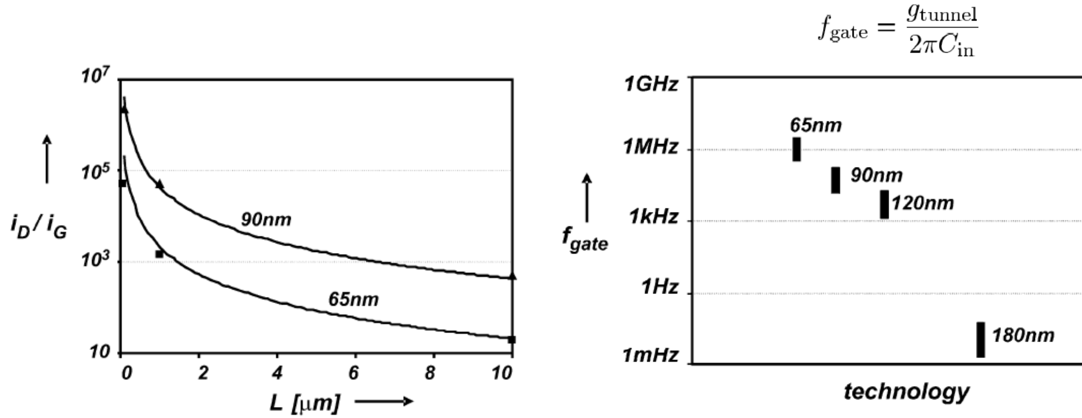
- For hand analysis, we will usually neglect r_c and r_e
- If significant, r_b can be included with R_S, i.e. $R_S^* = R_S + r_b$
- Resulting low-frequency gain

$$A_V(0) \triangleq \left.\frac{v_o}{v_i}\right|_{\omega=0} = -\underbrace{\left(\frac{r_\pi}{R_S^* + r_\pi}\right)}_{=1 \text{ for MOS}} \cdot g_m R_{Ltot} \qquad R_{Ltot} = r_o \,||\, R_L$$

Gate Tunnel Conductance for MOSFETS

- MOSFETs with extremely thin gate oxide draw a gate current due to direct tunneling
- This leads to a finite current gain and input resistance
  - Similar to BJT!

$$f_{\text{gate}} = \frac{g_{\text{tunnel}}}{2\pi C_{\text{in}}}$$



A. Annema, et al., "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits,* pp. 132-143, Jan. 2005.

Frequency Response

- Using nodal analysis, we find

$$\frac{v_o(s)}{v_i(s)} = -\left(\frac{r_\pi}{R_S^* + r_\pi}\right) \cdot g_m R_{Ltot} \frac{\left(1 - \frac{s}{z_1}\right)}{1 + b_1 s + b_2 s^2}$$

$$b_1 = R_S^*(C_\pi + C_\mu) + R_{Ltot}(C_L + C_\mu) + g_m R_S^* R_{Ltot} C_\mu$$

$$b_2 = R_S^* R_{Ltot}(C_\pi C_L + C_\pi C_\mu + C_L C_\mu)$$

$$z_1 = +\frac{g_m}{C_\mu}$$

- z_1 is a feedforward zero in the RHP. If $C_\pi >> C_\mu$, then

$$z_1 = +\frac{g_m}{C_\mu} >> \frac{g_m}{C_\pi + C_\mu} = \omega_T$$

Dominant Pole Approximation

- If a dominant pole condition exists, we can write

$$p_1 \cong -\frac{1}{b_1} = -\frac{1}{R_S^*(C_\pi + C_\mu) + R_{Ltot}(C_L + C_\mu) + g_m R_S^* R_{Ltot} C_\mu}$$

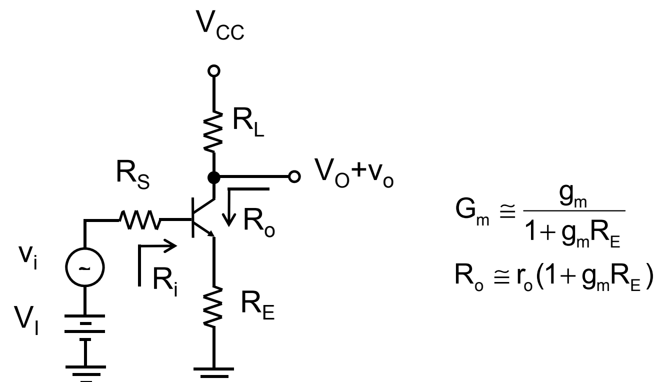
$$= -\frac{1}{R_S^*\left[C_\pi + (1+g_m R_{Ltot})C_\mu\right] + R_{Ltot}(C_L + C_\mu)}$$

$$p_2 \cong -\frac{b_1}{b_2} = -\frac{R_S^*(C_\pi + C_\mu) + R_{Ltot}(C_L + C_\mu) + g_m R_S^* R_{Ltot} C_\mu}{R_S^* R_{Ltot}(C_\pi C_L + C_\pi C_\mu + C_L C_\mu)}$$

- If $C_\mu << C_\pi$, C_L, then

$$p_2 \cong -\frac{R_S^* C_\pi + R_{Ltot} C_L + g_m R_S^* R_{Ltot} C_\mu}{R_S^* R_{Ltot} C_\pi C_L} = -\left(\frac{1}{R_S^* C_\pi} + \frac{1}{R_L C_L} + \frac{g_m}{C_L} \cdot \frac{C_\mu}{C_\pi}\right)$$

Emitter Degeneration



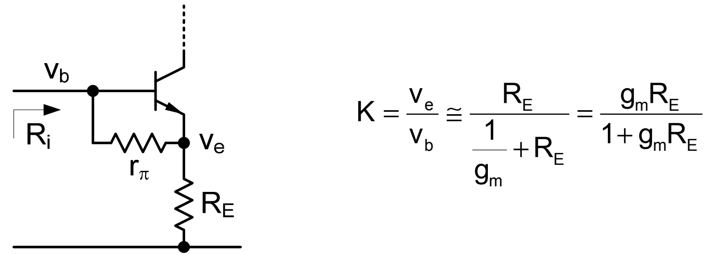
$$G_m \cong \frac{g_m}{1+g_m R_E}$$

$$R_o \cong r_o(1+g_m R_E)$$

- Degeneration resistor reduces the transconductance and increases the output resistance of the device
  - Same as in the MOSFET version of this circuit
- For the BJT version, R_E helps increase the input resistance

Calculation of R_i

- For the complete nodal analysis, see text p. 196
- A more intuitive way to find R_i is via the Miller theorem

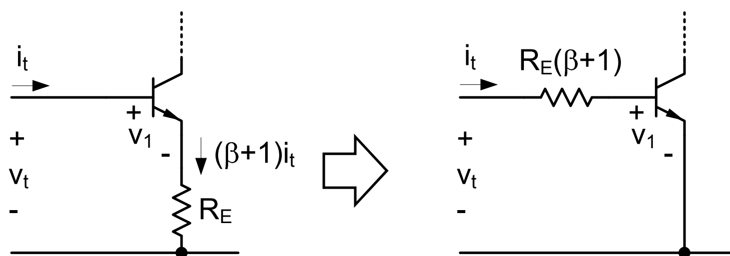


$$K = \frac{v_e}{v_b} \cong \frac{R_E}{\frac{1}{g_m} + R_E} = \frac{g_m R_E}{1 + g_m R_E}$$

$$R_i = \frac{r_\pi}{1-K} \cong \frac{r_\pi}{\left(1 - \frac{g_m R_E}{1+g_m R_E}\right)} = r_\pi\left(1+g_m R_E\right)$$

- The same "bootstrapping" effect applies to C_π, we see $C_\pi/(1+g_m R_E)$ looking into the input
  - Assuming K = constant in the frequency range of interest

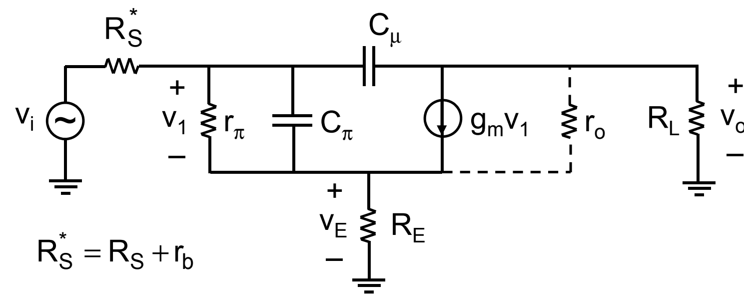
Alternative Calculation of R_i



$$R_i \cong r_\pi + R_E\left(1+\beta\right) = r_\pi + R_E\left(1+g_m r_\pi\right) \cong r_\pi\left(1+g_m R_E\right)$$

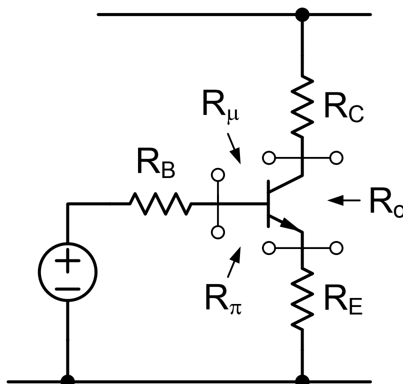
- Tricks of this kind are useful for reasoning about low frequency behavior
- More detailed analyses must be used be taken when investigating frequency dependence

Small-Signal Equivalent Circuit for Degenerated CE Stage



- Deriving the transfer function of this circuit requires solving a 3x3 system of equations
- In order to obtain an estimate of the circuit's bandwidth, it is more convenient (and intuitive) to perform a zero-value time constant analysis

Useful Expressions



$$R_o \cong r_o \| \frac{R_C + R_E}{1 + g_m R_E} \quad (\text{for } \beta \to \infty)$$

$$R_\pi \cong r_\pi \| \frac{R_B + R_E}{1 + g_m R_E}$$

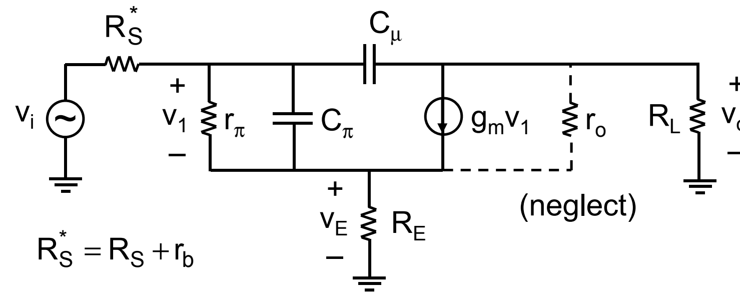
$$R_\mu = R_{left} + R_{right} + G_m R_{left} R_{right}$$

$$R_{left} \cong R_B \| r_\pi (1 + g_m R_E)$$

$$R_{right} \cong R_C$$

$$G_m = \frac{g_m}{1 + g_m R_E}$$

Bandwidth Estimate for Degenerated CE Stage (1)



$$R_S^* = R_S + r_b$$

$$R_\mu = R_S^* \| r_\pi(1+g_m R_E) + R_C + G_m\left[R_S^* \| r_\pi(1+g_m R_E)\right]R_C$$
$$\cong R_S^* + R_C + G_m R_C R_S^* = R_S^*\left(1+|A_v(0)|\right) + R_C$$

$$R_\pi \cong r_\pi \left\| \frac{R_S^* + R_E}{1+g_m R_E} \right. \cong \frac{R_S^* + R_E}{1+g_m R_E}$$

Bandwidth Estimate for Degenerated CE Stage (2)

$$\tau = \left[R_S^*\left(1+|A_v(0)|\right) + R_C\right]C_\mu + \frac{1+\frac{R_E}{R_S^*}}{1+g_m R_E} R_S^* C_\pi \qquad \omega_{-3dB} \cong \frac{1}{\tau}$$

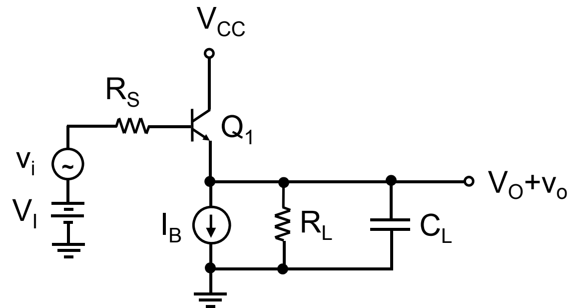
- Compare to the case of $R_E = 0$

$$\tau \cong \left[R_S^*\left(1+|A_v(0)|\right) + R_C\right]C_\mu + R_S^* C_\pi \qquad \omega_{-3dB} \cong \frac{1}{\tau}$$

- Adding R_E can help improve the bandwidth, provided that $g_m > 1/R_S^*$
  - Note, however, that g_m (and hence the power dissipation must be increased) to maintain the same $A_v(0)$
- Consider another special case where $g_m R_E >> 1$ and the time constant due to C_μ is negligible

$$\tau \cong \left(1+\frac{R_S^*}{R_E}\right)\frac{C_\pi}{g_m} \qquad \omega_{-3dB} \cong \omega_T\left(\frac{C_\pi + C_\mu}{C_\pi}\right)\left(\frac{R_E}{R_E + R_S^*}\right)$$

Common-Collector Stage (Emitter Follower)



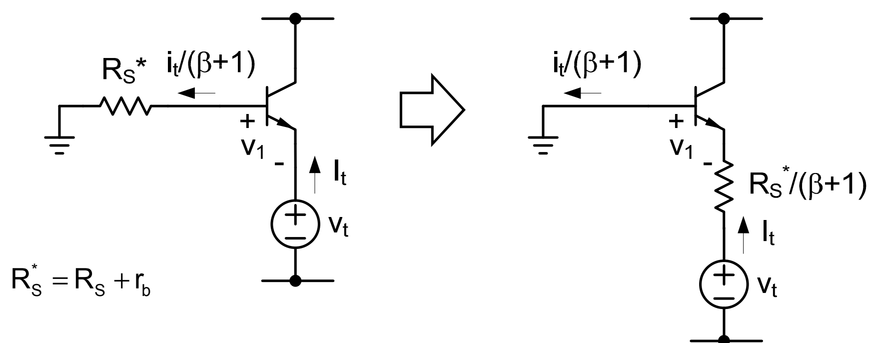
- Behavior is very similar to MOS common drain stage, except that
  - We do not need to worry about backgate effect
  - There is finite input resistance due to r_π
  - The output resistance depends on R_S (in addition to $1/g_m$)

Input and Output Resistance

- Input resistance (by inspection)

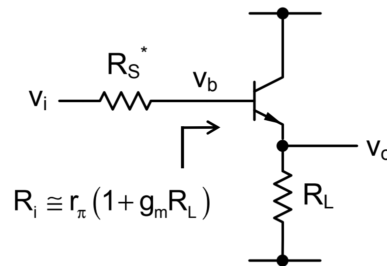
$$R_i \cong r_\pi (1 + g_m R_L)$$

- Output resistance (using push-through trick)



$$R_o \cong \frac{1}{g_m} + \frac{R_S^*}{\beta+1} \cong \frac{1}{g_m}\left(1 + \frac{R_S^*}{r_\pi}\right)$$

Low Frequency Voltage Gain

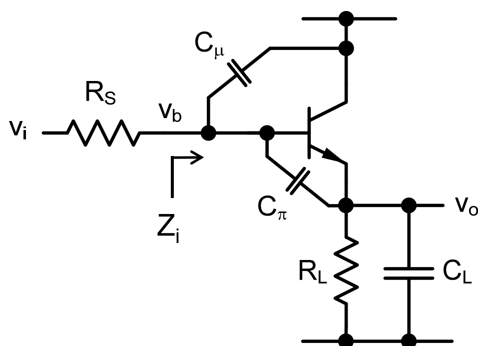


$$A_{v0} = \frac{v_o}{v_i} = \frac{v_b}{v_i}\frac{v_o}{v_b} \cong \frac{r_\pi(1+g_mR_L)}{r_\pi(1+g_mR_L)+R_s^*}\frac{g_mR_L}{1+g_mR_L}$$

$$\cong \frac{g_mR_L}{1+g_mR_L} \quad \text{for} \quad r_\pi(1+g_mR_L) >> R_s^*$$

$$\cong 1 \quad \text{for} \quad g_mR_L >> 1 \quad \text{and} \quad r_\pi(1+g_mR_L) >> R_s^*$$

Frequency Response



$$\frac{v_o}{v_i} = \frac{v_b}{v_i}\cdot\frac{v_o}{v_b} = \frac{Z_i}{Z_i+R_S}\cdot\frac{v_o}{v_b}$$

- Detailed analysis gives a very complex result for the general frequency response expression
- Must typically apply approximations based on given component values

Frequency Response

- Assuming that R_S is large (often the case, and the reason why the stage is used), we expect that the dominant pole is introduced at node v_b
- For the frequency range up until the dominant pole, we can therefore approximate

$$\frac{v_o}{v_b} \cong \frac{g_m R_L}{1+g_m R_L} = K \qquad Z_i \cong \frac{1}{s\left(C_\pi [1-K] + C_\mu\right)} = \frac{1}{sC_i}$$

$$\omega_p \cong \frac{1}{\left(R_s \| R_{in}\right) C_i}$$

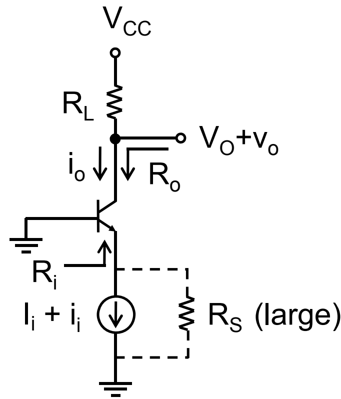
- See text, pp. 503 for a more detailed analysis, which also captures the feedforward zero introduced by C_π

Common Collector Output Impedance

- Detailed analysis of the common-collector output impedance shows potentially inductive behavior for large R_S
- The inductive behavior can lead to undesired “ringing” (or oscillations) during circuit transients
- In other cases, the inductive behavior is utilized for bandwidth extension (“inductive peaking”)
- The capacitance C_μ tends to reduce the inductive frequency range
  - C_μ appears in parallel with R_S, and creates a low impedance termination for high frequencies
  - Makes it difficult to use the circuit as a “good inductor”

- For a discussion on common collector output impedance and a detailed KCL-based analysis, see EE114 or section 7.2.3

Common-Base Stage



$$A_i = \frac{i_o}{i_i} \qquad A_i(0) = \frac{i_C}{i_E} = \frac{\beta}{\beta+1}$$

Neglecting r_b, r_c, r_e and r_π, we have

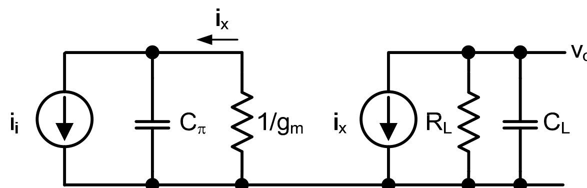
$$R_o \cong r_o(1+g_m R_S)$$

$$R_i \cong \frac{1}{g_m}\left(1+\frac{R_L}{r_o}\right) \cong \frac{1}{g_m}$$

Behavior is very similar to MOS common base stage, except that

- We do not need to worry about backgate effect
- The DC current gain is not exactly unity, due to finite β

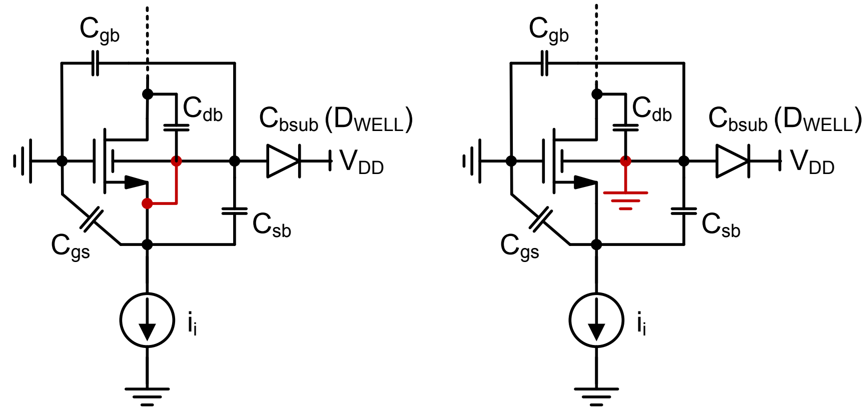
Simplified Small-Signal Model for High-Frequency Analysis



$$\frac{v_o}{i_i} = \frac{R_L}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \qquad \omega_{p2} = \frac{g_m}{C_\pi} = \frac{C_\pi + C_\mu}{C_\pi}\omega_T \qquad \omega_{p1} = \frac{1}{R_L C_L}$$

- The time constant associated with the load usually dominates the frequency response, i.e. $\omega_{p1} < \omega_{p2}$
- Note, however, that ω_{p2} can be important in feedback circuits (phase margin)

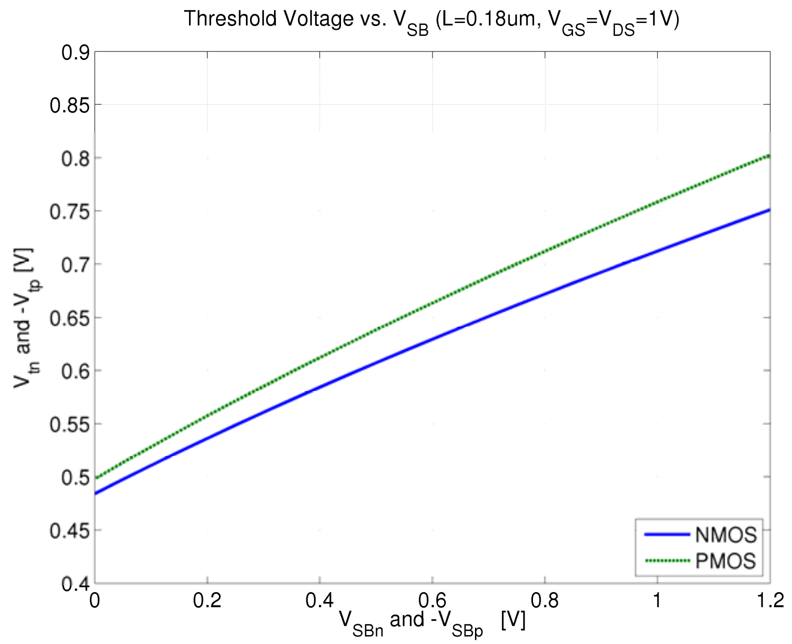
Common Gate Stage – Bulk Connection Scenarios



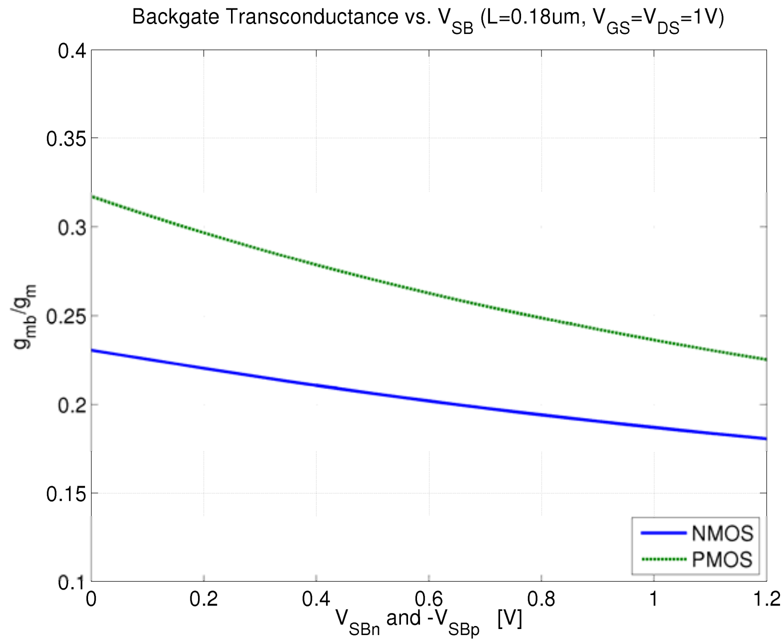
$$\omega_{p2,a} = \frac{g_m}{C_{gs} + C_{gb} + C_{bsub} + C_{db}\left[1 - K(s)\right]} \qquad \omega_{p2,b} = \frac{g_m + g_{mb}}{C_{gs} + C_{sb}}$$

- $\omega_{p2,a}$ is always less than $\omega_{p2,b}$ → Usually a bad idea to connect source to bulk in a common gate stage

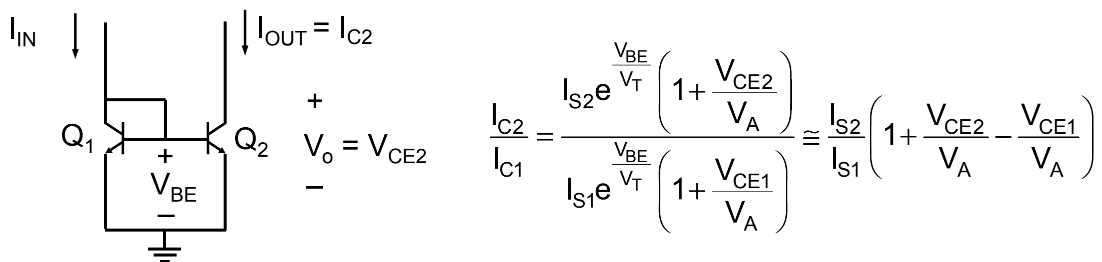
Backgate Effect in the EE214 Technology (1)



Backgate Effect in the EE214 Technology (2)



Basic BJT Current Mirror



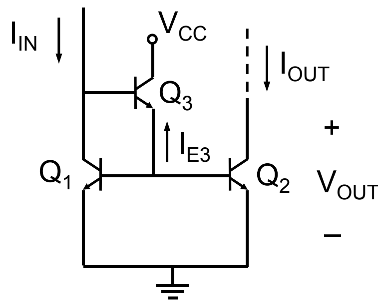
$$\frac{I_{C2}}{I_{C1}} = \frac{I_{S2} e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE2}}{V_A}\right)}{I_{S1} e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE1}}{V_A}\right)} \cong \frac{I_{S2}}{I_{S1}} \left(1 + \frac{V_{CE2}}{V_A} - \frac{V_{CE1}}{V_A}\right)$$

- Error due to base current

$$I_{IN} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} \cong I_{C2}\left(1 + 2\frac{I_{C2}}{\beta}\right) \quad \text{for} \quad I_{S1} = I_{S2}$$

$$\frac{I_{OUT}}{I_{IN}} \cong \frac{1}{\left(1 + \frac{2}{\beta}\right)} \cong 1 - \frac{2}{\beta}$$

BJT Current Mirror with "Beta Helper"

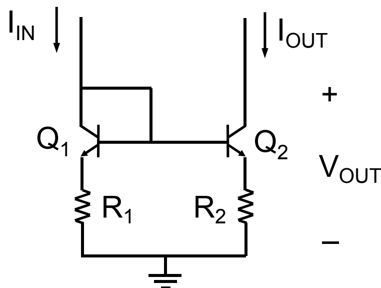


$$-I_{E3} = \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} \cong 2\frac{I_{C2}}{\beta} \quad \text{assuming} \quad I_{S1} = I_{S2}$$

$$I_{B3} = -\frac{I_{E3}}{\beta+1} \cong \frac{2I_{C2}}{\beta(\beta+1)} \qquad I_{IN} = I_{C1} + I_{B3} \cong I_{C1} + \frac{2I_{C2}}{\beta(\beta+1)} \cong I_{C2}\left[1 + \frac{2}{\beta(\beta+1)}\right]$$

$$\frac{I_{OUT}}{I_{IN}} \cong \frac{1}{1+\left(\dfrac{2}{\beta^2+\beta}\right)} \cong 1 - \frac{2}{\beta^2}$$

BJT Current Mirror with Degeneration



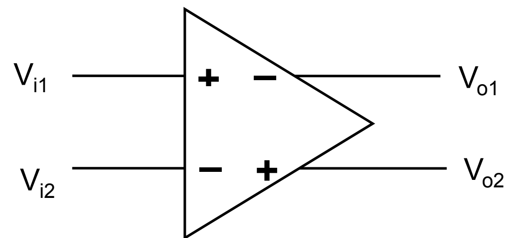
Neglecting base currents

$$V_{BE1} + I_{C1}R_1 = V_{BE2} + I_{C2}R_2$$

$$I_{C2} = \frac{1}{R_2}\left\{I_{C1}R_1 + V_T \ln\left[\left(\frac{I_{C1}}{I_{C2}}\right)\left(\frac{I_{S2}}{I_{S1}}\right)\right]\right\} \cong I_{C1}\frac{R_1}{R_2} \qquad \frac{I_{OUT}}{I_{IN}} \cong \frac{R_1}{R_2}$$

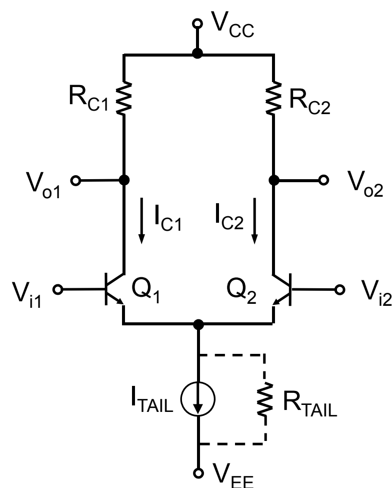
- Degeneration brings two benefits
  - Increased output resistance
  - Reduces sensitivity of mirror ratio to mismatches in I_S
- Minimum V_{OUT} for which Q_2 remains forward active is increased

Differential Circuits



- Enables straightforward biasing without AC coupling
- Information is carried in “differential” signals that are insensitive to “common-mode” perturbations, such as power supply noise
- Fully differential circuits are increasingly used for I/O and clock-and-data recovery (CDR) circuits to allow the use of small signals at high speeds

BJT Differential Pair



Differential Input Voltage

$$V_{id} \triangleq V_{i1} - V_{i2}$$

Differential Collector Current

$$I_{cd} \triangleq I_{c1} - I_{c2}$$

Differential Output Voltage

$$V_{od} \triangleq V_{o1} - V_{o2}$$

- The following large signal analysis neglects r_b, r_c, r_e, finite R_{EE} and assumes that the circuit is perfectly symmetric

Large Signal Analysis

$$V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0 \qquad I_{C1} \cong I_{S1} e^{\frac{V_{be1}}{V_T}} \qquad I_{C2} \cong I_{S2} e^{\frac{V_{be2}}{V_T}}$$

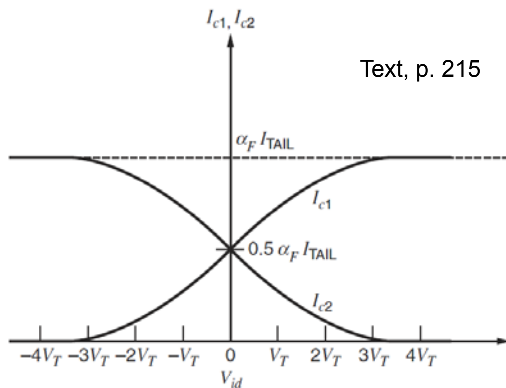
$$\Rightarrow \frac{I_{c1}}{I_{c2}} = e^{\frac{V_{be1}-V_{be2}}{V_T}} = e^{\frac{V_{i1}-V_{i2}}{V_T}} = e^{\frac{V_{id}}{V_T}}$$

$$I_{TAIL} = -(I_{e1}+I_{e2}) = \frac{1}{\alpha}(I_{c1}+I_{c2}) \qquad \Rightarrow I_{c1} = \frac{\alpha I_{TAIL}}{1+e^{-\frac{V_{id}}{V_T}}} \qquad I_{c2} = \frac{\alpha I_{TAIL}}{1+e^{+\frac{V_{id}}{V_T}}}$$

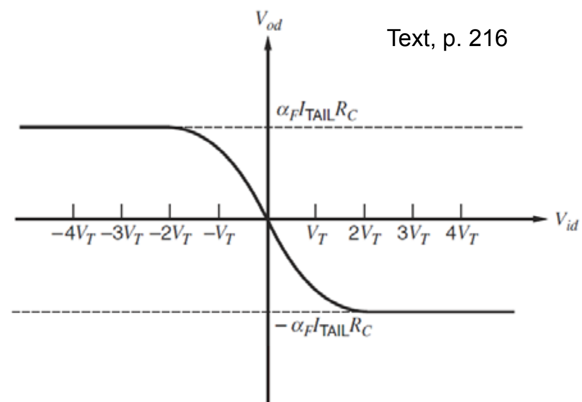
$$\boxed{I_{cd} = I_{c1} - I_{c2} = \alpha_F I_{TAIL}\left[\frac{1}{1+e^{-\frac{V_{id}}{V_T}}} - \frac{1}{1+e^{+\frac{V_{id}}{V_T}}}\right] = \alpha_F I_{TAIL} \tanh\left(\frac{V_{id}}{2V_T}\right)}$$

$$V_{od} = I_{od}R_L = \alpha I_{TAIL} R_L \tanh\left(\frac{V_{id}}{2V_T}\right)$$

Plot of Transfer Characteristics



Text, p. 215

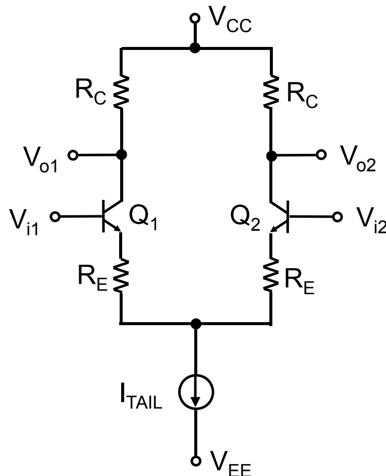


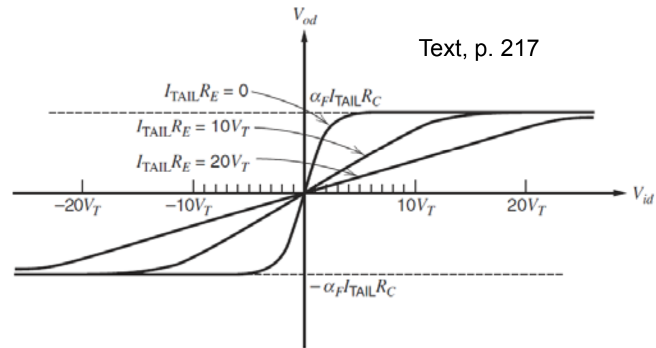
Text, p. 216

- Linear region in V_{od} vs. V_{id} characteristic is narrow compared to MOS
  - Recall that full steering in a MOS pair occurs for $V_{id} = \sqrt{2}V_{OV}$
- BJT differential pair is linear only for $|V_{id}| < V_T \cong 26$ mV

Emitter Degeneration

- Can use emitter degeneration resistors to increase the range of input voltage over which the transfer characteristic of the pair is linear
- For large R_E, linear range is approximately equal to $I_{TAIL}R_E$





Voltage Decomposition

Common-Mode Voltages

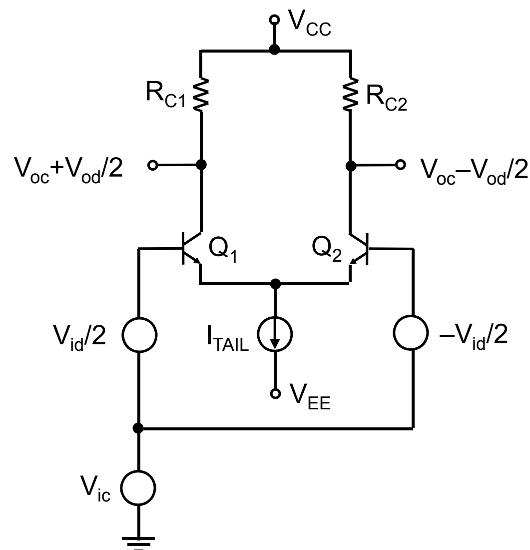
$$V_{ic} \triangleq \frac{1}{2}(V_{i1} + V_{i2})$$

$$V_{oc} \triangleq \frac{1}{2}(V_{o1} + V_{o2})$$

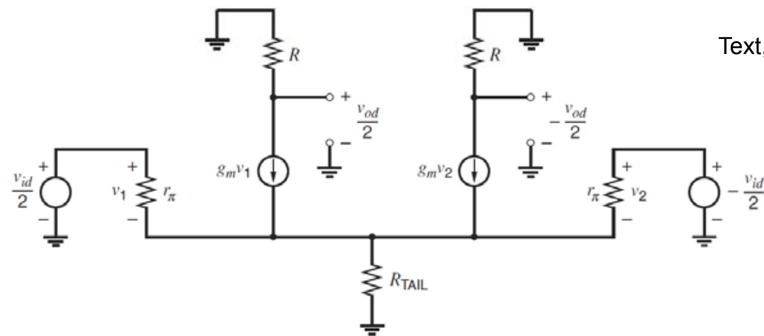
Inputs V_{i1} and V_{i2} can be decomposed into a combination of differential- and common-mode voltage sources

$$V_{i1} = V_{ic} + \frac{1}{2}V_{id}$$

$$V_{i2} = V_{ic} - \frac{1}{2}V_{id}$$



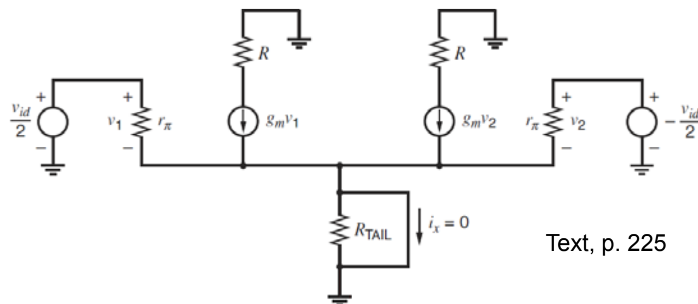
Small Signal Model for $v_{ic} = 0$



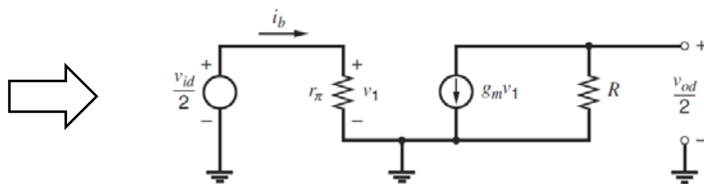
Text, p. 224

- Define differential mode gain as $$A_{dm} \triangleq \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0}$$

Differential Mode Half Circuit

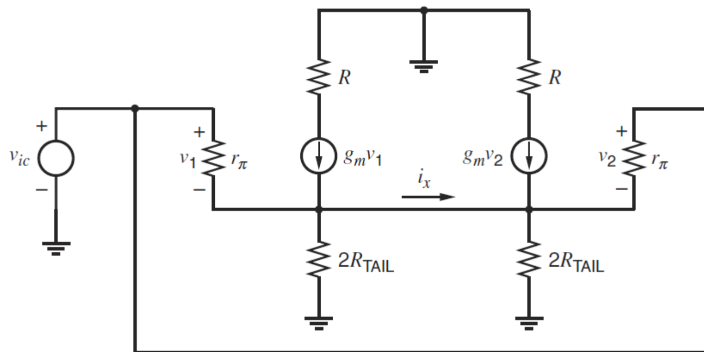


Text, p. 225



$$\frac{v_{od}}{2} = -g_m R \frac{v_{id}}{2} \qquad A_{dm} = \frac{v_{od}}{v_{id}} = -g_m R$$

Small Signal Model for $v_{id} = 0$

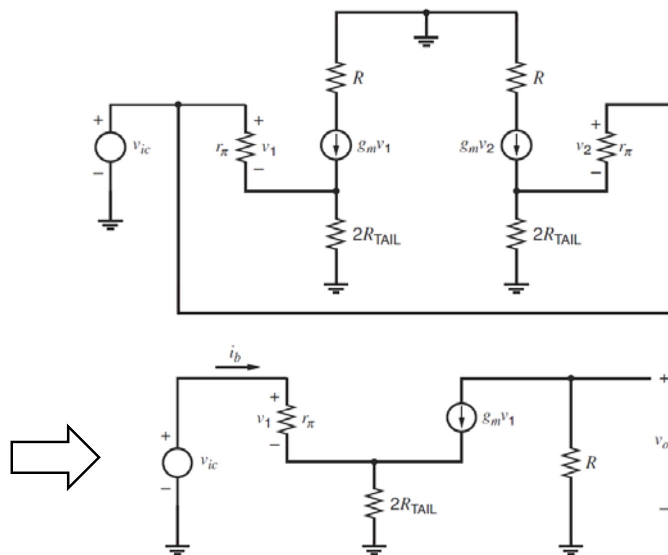


Text, p. 227

- Define common mode gain as

$$A_{cm} \triangleq \left.\frac{v_{od}}{v_{id}}\right|_{v_{id}=0}$$

Common Mode Half Circuit



Text, p. 227

$$v_{oc} = -G_m R v_{ic}$$

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = -G_m R = -\frac{g_m R}{1 + 2g_m R_{TAIL}}$$

Interaction of Common Mode and Differential Mode

$$A_{cdm} \triangleq \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \quad \text{and} \quad A_{dcm} \triangleq \left.\frac{v_{oc}}{v_{id}}\right|_{v_{ic}=0}$$

- In a perfectly balanced (symmetric) circuit, $A_{cdm} = A_{dcm} = 0$
- In practice, A_{cdm} and A_{dcm} are not zero because of component mismatch
- A_{cdm} is important because it indicates the extent to which a common-mode input will corrupt the differential output (which contains the actual signal information)
- See text, section 3.5.6.9 for a detailed analysis

Common-Mode Rejecton

For fully differential circuits, the common-mode rejection ratio (CMRR) is traditionally defined as

$$CMRR \triangleq \left|\frac{A_{dm}}{A_{cdm}}\right|$$

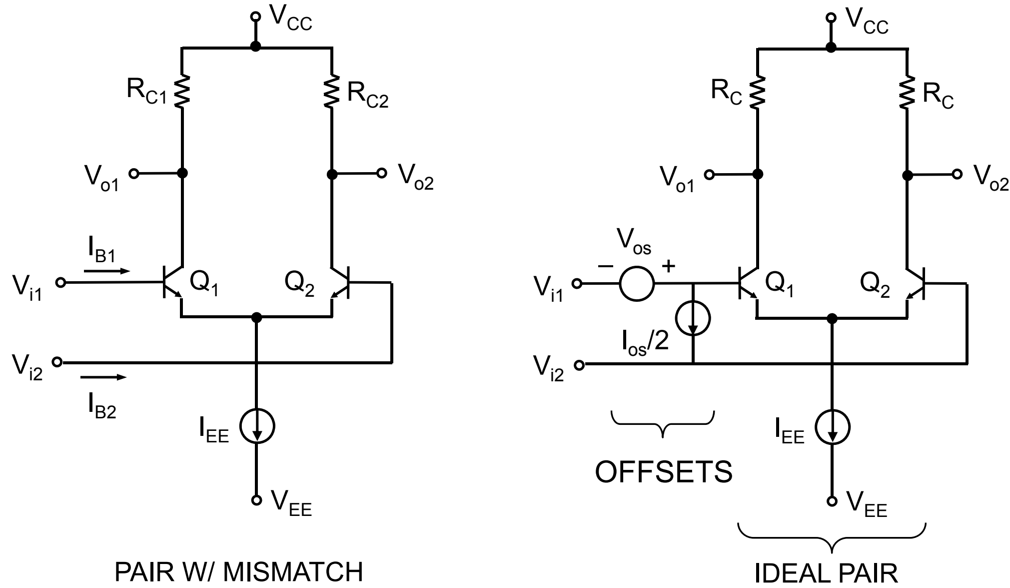
However, the text defines the ratio as

$$CMRR\big|_{Text} \triangleq \left|\frac{A_{dm}}{A_{cm}}\right|$$

This latter definition is appropriate for circuits with a differential input and single-ended output, such as operational amplifiers.

Input-Referred DC Offsets

- In a perfectly symmetric circuit, $V_{id} = 0$ yields $V_{od} = 0$
- Imbalances can be modeled as input referred offsets



Analysis

$$V_{os} - V_{BE1} + V_{BE2} = 0$$

$$\therefore \; V_{os} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$

$$= V_T \ln\left[\left(\frac{I_{C1}}{I_{C2}}\right)\left(\frac{I_{S2}}{I_{S1}}\right)\right], \qquad \text{where } V_T = \frac{kT}{q}$$

If $V_{od} = 0$, then

$$I_{C1}R_{C1} = I_{C2}R_{C2}$$

$$\therefore \; \frac{I_{C1}}{I_{C2}} = \frac{R_{C2}}{R_{C1}}$$

Thus

$$V_{os} = V_T \ln\left[\left(\frac{R_{C2}}{R_{C1}}\right)\left(\frac{I_{S2}}{I_{S1}}\right)\right]$$

Result

- For small mismatches $\Delta R_C << R_C$ and $\Delta I_S << I_S$, it follows that

$$V_{os} \cong V_T\left(-\frac{\Delta R_C}{R_C}-\frac{\Delta I_S}{I_S}\right)=\left(\frac{g_m}{I_D}\right)^{-1}\left(-\frac{\Delta R_C}{R_C}-\frac{\Delta I_S}{I_S}\right)$$

- And similarly

$$I_{os} \cong -\frac{I_C}{\beta}\left(\frac{\Delta R_C}{R_C}+\frac{\Delta \beta}{\beta}\right)$$

(see text, pp. 231)

- Mismatch in I_S results primarily from mismatches in the emitter areas and the base doping
- Mismatch in β results primarily from mismatches in the base width
- The standard deviations of device-to-device variations in I_S and β is typically on the order of 5%

Offset Voltage Drift

$$\frac{dV_{os}}{dT}=\frac{d}{dT}\left[\frac{kT}{q}\left(-\frac{\Delta R_C}{R_C}-\frac{\Delta I_S}{I_S}\right)\right]=\frac{V_{os}}{T}$$

- Example
  - V_{OS} was determined to be 2 mV through a measurement at 300°K
  - Means that the offset voltage will drift by 2 mV/300°K = 6.6 μV/°C
- For a MOS differential pair, the offset drift is less predictable and turns out to be a complex function of several process parameters

Comparison of V_{OS} for MOS and BJT Differential Pairs

$$V_{OS,BJT} \cong \left(\frac{g_m}{I_D}\right)^{-1}\left(-\frac{\Delta R}{R}-\frac{\Delta I_S}{I_S}\right)$$

$$V_{OS,MOS} \cong \underbrace{\Delta V_t}_{?} + \underbrace{\left(\frac{g_m}{I_D}\right)^{-1}}_{\text{Worse}}\underbrace{\left(-\frac{\Delta R}{R}-\frac{\Delta (W/L)}{(W/L)}\right)}_{\text{Similar to BJT}}$$

- The standard deviation of ΔV_t can be estimated using the following expression (Pelgrom, JSSC 10/1989)

$$\sigma_{\Delta V_t} \cong \frac{A_{Vt}}{\sqrt{WL}}$$

where $A_{vt} \cong 5\text{mV-}\mu\text{m}$ for a typical 0.18 μm process

Numerical Example

- Ignoring resistor mismatch for simplicity
- Assume $(g_m/I_D)_{MOS}$ = 10 S/A, W = 5 μm, L= 0.2 μm

$$\text{std}\left(V_{OS,BJT}\right) \cong \text{std}\left[\left(\frac{g_m}{I_D}\right)^{-1}\left(\frac{\Delta I_S}{I_S}\right)\right] = 26\text{mV}\cdot 5\% = 1.3\text{mV}$$

$$\text{std}\left(V_{OS,MOS}\right) \cong \text{std}\left[\Delta V_t + \left(\frac{g_m}{I_D}\right)^{-1}\left(\frac{\Delta (W/L)}{(W/L)}\right)\right]$$

$$\cong \sqrt{\left(\frac{5\text{mV}-\mu\text{m}}{\sqrt{5\mu\text{m}\cdot 0.2\mu\text{m}}}\right)^2 + \left(100\text{mV}\cdot 5\%\right)^2}$$

$$\cong \sqrt{\left(5\text{mV}\right)^2 + \left(5\text{mV}\right)^2} = 7.1\text{mV}$$

- MOS offset is typically 5-10 times worse than BJT

A_{Vt} Data

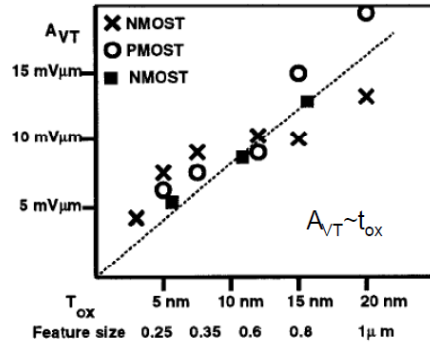
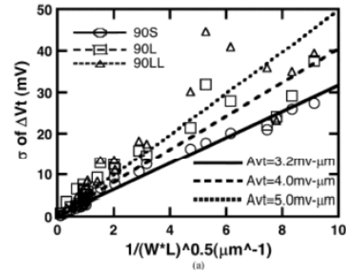
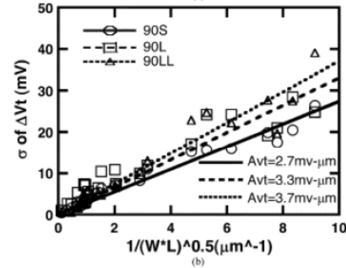


Fig. 3. Evolution of matching coefficient over process generation. Squares are derived from[4], the other measurements are by the authors.

[Pelgrom, IEDM 1998]





[Chang, TED 7/2005]

- A_{Vt} improves with technology scaling
- But, unfortunately, A_{Vt} scales not as fast as minimum device area
  - Hence V_t mismatch for minimum size devices worsens

Chapter 5

Two-Port Feedback Circuit Analysis

B. Murmann

Stanford University

Reading Material: Sections 8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.8

Benefits and Costs of Negative Feeback

Negative feedback provides a means of exchanging gain for improvements in other performance metrics

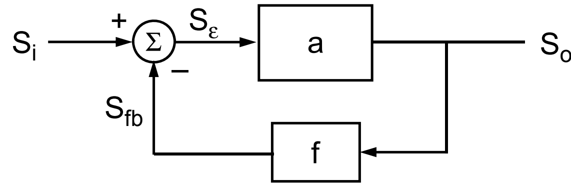
Benefits

- Reduced sensitivity (improved precision)
- Reduced distortion (more later)
- Scaling of impedance levels (up or down)
- Increased bandwidth

Costs

- Lower gain
- Potential instability

Ideal Feedback (1)



Assumptions for an ideal feedback system:

1. No loading
2. Unilateral transmission in both the forward amplifier and feedback network

$$\left.\begin{aligned} S_o &= a \cdot S_\varepsilon \\ S_{fb} &= f \cdot S_o \\ S_\varepsilon &= S_i - S_{fb} \end{aligned}\right\} \Rightarrow S_o = (S_i - S_{fb}) = a(S_i - f \cdot S_o)$$

Ideal Feedback (2)

$$\left.\begin{aligned} &\textbf{Closed-Loop Gain:} \quad A \triangleq \frac{S_o}{S_i} = \frac{a}{1+af} \\ &\textbf{Loop Gain:} \quad T \triangleq af = \frac{S_{fb}}{S_\varepsilon} \end{aligned}\right\} \Rightarrow A = \frac{a}{1+T}$$

If **T >> 1**, then

$$A \cong \frac{a}{T} = \frac{1}{f}$$

The feedback loop acts to minimize the error signal, S_ε, thus forcing S_{fb} to track S_i. In particular,

$$S_\varepsilon = S_i - f \cdot S_o = S_i - f \cdot \left(\frac{a}{1+af}\right) S_i = \left(1 - \frac{af}{1+af}\right) \cdot S_i$$

$$\therefore \quad \frac{S_\varepsilon}{S_i} = 1 - \frac{T}{1+T} = \frac{1}{1+T} \quad \text{and} \quad \frac{S_{fb}}{S_i} = a \cdot f\left(\frac{S_\varepsilon}{S_i}\right) = \frac{T}{1+T}$$

Gain Sensitivity

- The feedback network is typically a precision passive network with an insensitive, well-defined transfer function f. The forward amplifier gain is generally large, but not well controlled.
- Feedback acts to reduce not only the gain, but also the relative, or fractional, gain error by the factor 1+T

$$\frac{dA}{da} = \frac{d}{da}\left(\frac{a}{1+af}\right) = \frac{1}{1+af} + a\frac{d}{da}\left(\frac{1}{1+af}\right)$$
$$= \frac{(1+af)-af}{(1+af)^2} = \frac{1}{(1+af)^2} = \frac{1}{(1+T)^2}$$

- For a change δa in a

$$\delta a = \frac{dA}{da}\delta a = \frac{\delta a}{(1+T)^2}$$

$$\therefore \quad \frac{\delta A}{A} = \frac{\delta a}{(1+T)^2}\left(\frac{1+T}{a}\right) = \left(\frac{1}{1+T}\right)\frac{\delta a}{a}$$

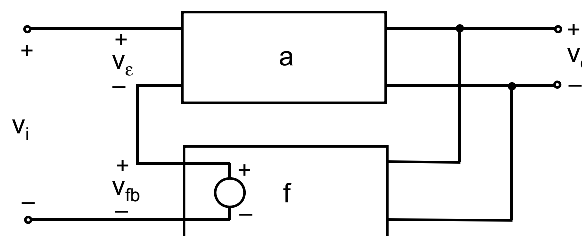
The Two-Port Approach to Feedback Amplifier Design

- A practical approach to feedback amplifier analysis and design is based on constructing two-port representations of the forward amplifier and feedback network
- The **two-port approach** relies on the following **assumptions**:
  - Loading effects can be incorporated in the two-port model for the forward amplifier
  - Transmission through the forward amplifier is nearly unilateral
  - Forward transmission through the feedback network is much less than that through the forward amplifier
- When the preceding assumptions break down, the two-port approach deviates from, and is less accurate than, the **return ratio** approach devised by Henrik Bode
- But, the two-port approach can provide better physical tuition, especially with respect to what happens in the frequency domain when the feedback loop is "closed"
  - It is basically an effort to model feedback amplifiers in the way that Harold Black conceived them

Feedback Configurations

- In the two-port approach to feedback amplifier analysis there are four possible amplifier configurations, depending on whether the two-port networks are connected in SHUNT or in SERIES at the input and output of the overall amplifier
- At the OUTPUT
  - A shunt connection senses the output voltage
  - A series connection senses the output current
- At the INPUT
  - A shunt connection feeds back a current in parallel with the input
  - A series connection feeds back a voltage in series with the input
- The four possible configurations are referred to as SERIES-SHUNT, SHUNT-SHUNT, SHUNT-SERIES, and SERIES-SERIES feedback
- The following pages illustrate these configurations using ideal two-port networks

Series-Shunt Feedback

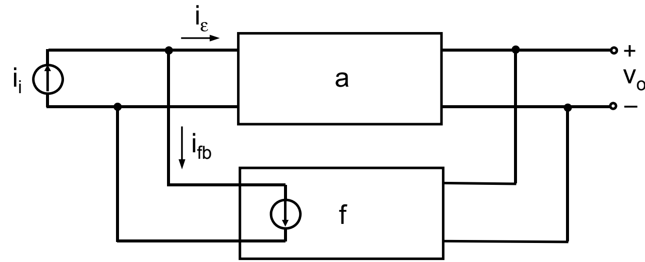


$$a = \frac{v_o}{v_\varepsilon}, \quad f = \frac{v_{fb}}{v_o}$$

$$A = \frac{v_o}{v_i} = \frac{a}{1+af} = \frac{a}{1+T}$$

In this case **a**, **A** and **f** are all **voltage gains**

Shunt-Shunt Feedback

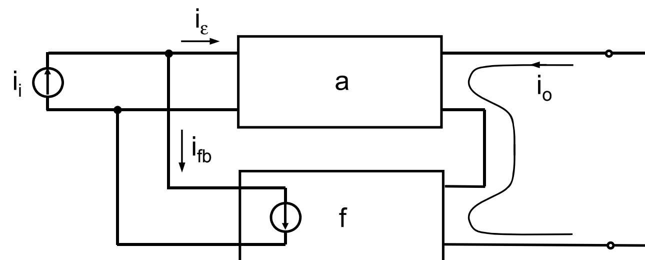


$$a = \frac{v_o}{i_\varepsilon}, \quad f = \frac{i_{fb}}{v_o}$$

$$A = \frac{v_o}{i_i} = \frac{a}{1+af} = \frac{a}{1+T}$$

a and **A** are **transimpedances**; **f** is a **transadmittance**

Shunt-Series Feedback

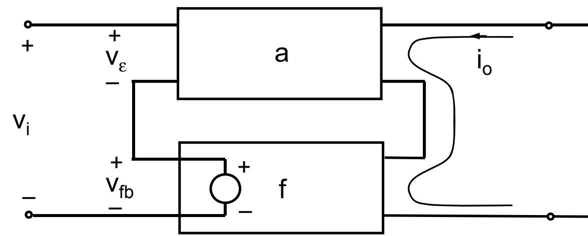


$$a = \frac{i_o}{i_\varepsilon}, \quad f = \frac{i_{fb}}{i_o}$$

$$A = \frac{i_o}{i_i} = \frac{a}{1+af} = \frac{a}{1+T}$$

a, **A**, and **f** are **current gains**

Series-Series Feedback



$$a = \frac{i_o}{v_\varepsilon}, \quad f = \frac{v_{fb}}{i_o}$$

$$A = \frac{i_o}{v_i} = \frac{a}{1+af} = \frac{a}{1+T}$$

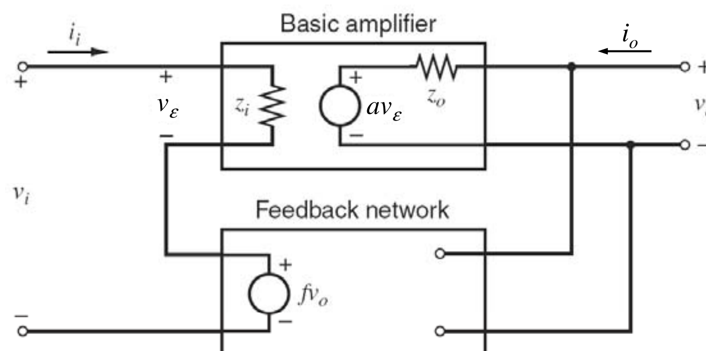
a and **A** are **transadmittances**; **f** is **transimpedance**

Note: T = af is always dimensionless

Closed Loop Impedances

- To illustrate the influence of feedback on the input and output impedances of an amplifier, consider the following:
  - Include finite input and output impedances in a simple, idealized two-port model of the forward amplifier
  - Assume that the feedback network has ideal input and output impedances so as not to load the forward amplifier
- Consider two examples, **series-shunt** and **shunt-series** amplifiers

SERIES-SHUNT



"Ideal" Series-Shunt Impedances

Input Impedance

$$Z_i \triangleq \left.\frac{v_i}{i_i}\right|_{i_o=0}$$

With $i_o = 0$

$$v_o = a v_\varepsilon$$
$$v_i = v_\varepsilon + f v_o = (1+af)v_\varepsilon$$
$$= (1+T)v_\varepsilon$$
$$i_i = \frac{v_\varepsilon}{z_i} = \frac{1}{z_i}\left(\frac{1}{1+T}\right)v_i$$

$$Z_i = \frac{v_i}{i_i} = (1+T)z_i$$

Output Impedance

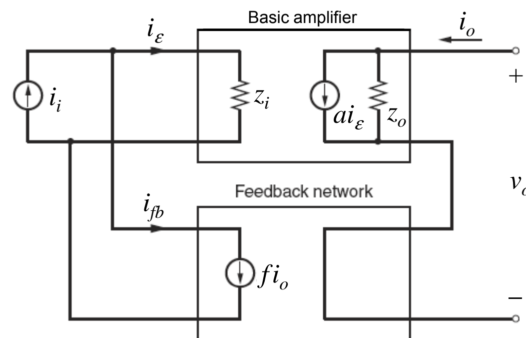
$$Z_o \triangleq \left.\frac{v_o}{i_o}\right|_{v_i=0}$$

With $v_i = 0$

$$v_\varepsilon + f v_o = v_i = 0$$
$$i_o = \frac{v_o - a v_\varepsilon}{z_o} = \frac{1}{z_o}(1+af)v_o$$
$$= \frac{1}{z_o}(1+T)v_o$$

$$Z_o = \frac{v_o}{i_o} = \frac{z_o}{1+T}$$

"Ideal" Shunt-Series Impedances



Input Impedance

$$Z_i \triangleq \left.\frac{v_i}{i_i}\right|_{v_o=0}$$

With $v_o = 0$

$$i_o = a i_\varepsilon$$
$$i_i = i_\varepsilon + f i_o = (1+af)i_\varepsilon = (1+T)i_\varepsilon$$
$$v_i = i_\varepsilon z_i = \left(\frac{i_i}{1+T}\right)z_i$$

$$\Rightarrow \quad Z_i = \frac{v_i}{i_i} = \frac{z_i}{(1+T)}$$

Output Impedance

$$Z_o \triangleq \left.\frac{v_o}{i_o}\right|_{i_i=0}$$

With $i_i = 0$

$$i_\varepsilon + f i_o = 0$$

$$v_o = (i_o + a i_\varepsilon) z_o = (i_o + a f i_o) z_o = i_o (1+T) z_o$$

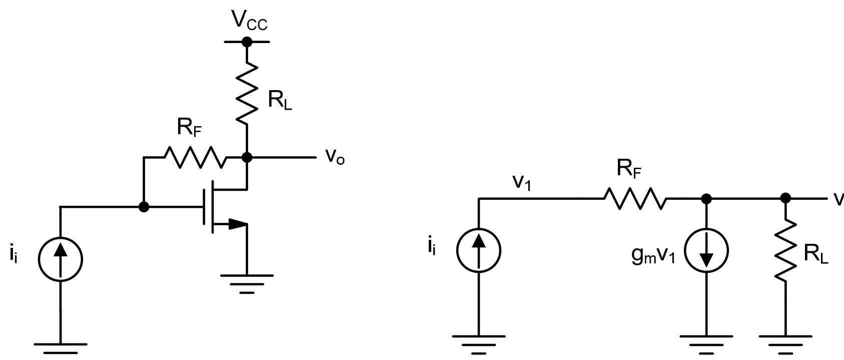
$$\Rightarrow \quad Z_o = \frac{v_o}{i_o} = (1+T) z_o$$

In general:

- Negative feedback connected in **series** **increases** the driving point impedance by (1+T)
- Negative feedback connected in **shunt** **reduces** the driving point impedance by (1+T)

Loading Effects – Introductory Example

- Consider the following feedback circuit



- Analysis methods
  - Closed loop transfer function using nodal analysis
  - Return ratio analysis (see EE114)
  - Two-port feedback circuit analysis

Nodal Analysis

Given

$$0 = \frac{v_1 - v_o}{R_F} - i_i$$

$$0 = \frac{v_o - v_1}{R_F} + g_m \cdot v_1 + \frac{v_o}{R_L}$$

$$\text{Find}(v_1, v_o) \rightarrow \begin{pmatrix} \dfrac{R_F \cdot i_i + R_L \cdot i_i}{R_L \cdot g_m + 1} \\ \dfrac{R_L \cdot i_i - R_F \cdot R_L \cdot g_m \cdot i_i}{R_L \cdot g_m + 1} \end{pmatrix} \qquad A = \frac{v_o}{i_i} = \frac{R_L - R_F \cdot R_L \cdot g_m}{R_L \cdot g_m + 1} = -R_F \cdot \left(\frac{1 - \dfrac{1}{g_m \cdot R_F}}{1 + \dfrac{1}{g_m \cdot R_L}} \right)$$

- No information about loop gain (which we need e.g. for stability analysis)

Return Ratio Analysis

$$A = A_{inf} \cdot \frac{RR}{1 + RR} + \frac{d}{1 + RR} \qquad A_{inf} = -R_F \qquad d = R_L \qquad RR = g_m \cdot R_L$$

$$A = -R_F \frac{g_m \cdot R_L}{1 + g_m \cdot R_L} + \frac{R_L}{1 + g_m \cdot R_L} = -R_F \left(\frac{g_m \cdot R_L - \dfrac{R_L}{R_F}}{1 + g_m \cdot R_L} \right) = -R_F \cdot \left(\frac{1 - \dfrac{1}{g_m \cdot R_F}}{1 + \dfrac{1}{g_m \cdot R_L}} \right)$$

- The result for the closed loop gain (A) matches the nodal analysis perfectly
- In addition, we have determined (along the way) the loop gain (RR)
  - This is useful for stability analysis
- The return ratio method is accurate and general
- The two-port method aims to sacrifice some of this accuracy and generality in exchange for better intuition and less computational effort
  - The involved approximations follow from the typical design intent for each of the four possible approximations