

# Area-Efficient Linear Regulator With Ultra-Fast Load Regulation

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**Abstract**—We demonstrate a fully integrated linear regulator for multisupply voltage microprocessors implemented in a 90 nm CMOS technology. Ultra-fast single-stage load regulation achieves a 0.54-ns response time at 94% current efficiency. For a 1.2-V input voltage and 0.9-V output voltage the regulator enables a 90 mV<sub>P-P</sub> output droop for a 100-mA load step with only a small on-chip decoupling capacitor of 0.6 nF. By using a PMOS pull-up transistor in the output stage we achieved a small regulator area of 0.008 mm<sup>2</sup> and a minimum dropout voltage of 0.2 V for 100 mA of output current. The area for the 0.6-nF MOS capacitor is 0.090 mm<sup>2</sup>.

**Index Terms**—Linear regulator, low-dropout regulator.

## I. INTRODUCTION

LOW-POWER low-voltage microprocessors implemented in a scaled CMOS technology often require multiple supply voltages. High voltage, e.g., 1.8 V, is used for I/O buffers for compatibility reasons, medium voltage of 1.2–1.4 V is used for analog circuits, e.g., phase-locked loops, or operational amplifiers that benefit from a larger voltage headroom, and low voltage of 0.6–1 V can be used for logic circuits to reduce active and leakage power. In dual-supply designs, speed-critical logic circuits can operate at a nominal voltage, e.g., 1.2 V, while noncritical circuits can meet their speed requirement at a lower voltage, e.g., 0.9 V, while saving power.

Active power of a CMOS circuit operating at a constant frequency reduces with the square of the supply voltage,  $V_{DD}$ . Leakage power decreases exponentially. For a 25% reduction in  $V_{DD}$ , the active power reduces by 44%. A high-efficiency switching dc–dc converter can achieve power efficiency of  $\sim 95\%$  [1], resulting in overall active power savings of 41%. However, such switching converters require off-chip inductors and capacitors. A linear regulator is easy to integrate on-chip within a small area. For 1.2–0.9 V conversion, the theoretical maximum power efficiency of a linear regulator is 75% and the resulting active power savings are 25%. For a realistic linear regulator with 95% current efficiency, the power efficiency is 71.25% and the power savings are 21.4%. Moreover, the battery life in handheld and other portable applications is often limited by leakage rather than active power. Linear regulators can

achieve low standby current due to the absence of switching. Therefore, a fully integrated linear regulator with no external components is attractive for applications with stringent volume and weight requirements and relatively small peak power of  $\sim 1$  W.

We demonstrate a linear regulator implemented in a 90-nm CMOS technology that converts from 1.2 to 0.9 V with 94% current efficiency. The regulator occupies an area of 0.008 mm<sup>2</sup> for a 100-mA rating. Fast load regulation is important when biasing digital CMOS circuits with rapidly changing supply current. The response time of 0.54 ns guarantees 10%<sub>P-P</sub> output voltage variations under a 100% load step with only a small decoupling capacitor of 0.6 nF. The capacitor was integrated on-chip in 0.090 mm<sup>2</sup> of area. The regulator features digital setting of output current rating that allows reduced bias current in the standby mode. The decoupling capacitor can be reduced from 0.6 to 0.3 nF, if a load circuit provides a control signal ahead of a rapid load current transient. This signal temporarily activates a turbo mode with two times faster load regulation compared to the active mode.

In Section II, we discuss various properties of existing regulator topologies and explain the benefits of the proposed topology. Section III describes in detail the implementation of the circuits used on the test chip. The dc and ac measurements are given in Section IV, and finally, we compare performance of this regulator with previously published results in Section V.

## II. LINEAR REGULATOR TOPOLOGY

Existing linear regulator topologies vary widely in their quiescent current, dc load regulation, transient response, decoupling capacitance and silicon area requirements. Since our goal was to fully integrate the regulator on the same chip with the load circuit, the available silicon area for  $\sim 100$ -mA rating limits the size of the output decoupling capacitor of the regulator to about 1 nF, if implemented as a thin gate oxide capacitor, which consumes die area and oxide leakage power. One of the main design requirements for a linear regulator is usually extremely small quiescent current, such as  $< 1\%$  of the load current. The problem is that small quiescent current slows down the transient response and results in a large output decoupling capacitor. In a 90-nm logic process, gate leakage of a 1-nF decoupling capacitor is on the order of milliamperes. The added leakage from even a small additional on-chip capacitor could easily erase any benefits of having high current efficiency. For our application, we need a regulator with a very fast transient response. Quiescent current of a few percent is acceptable if the regulator does

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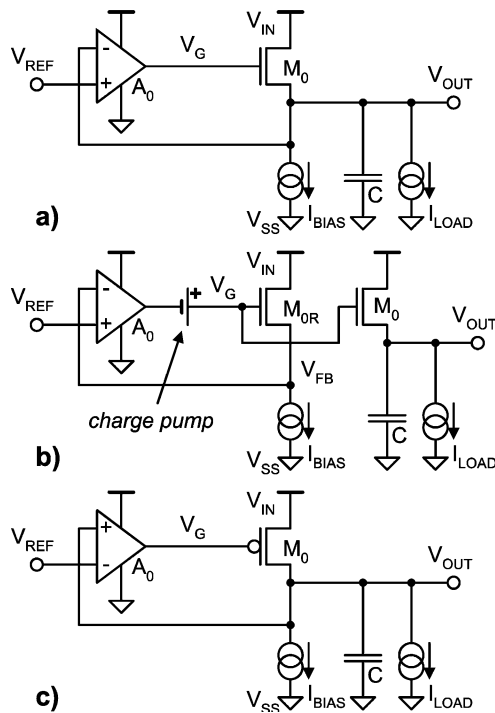


Fig. 1. Linear regulator with: (a) a source follower; (b) a replica-biased source follower; (c) a common-source driver.

not require additional decoupling. Some applications demand accurate load regulation within a few percent. For biasing of digital CMOS circuits, a 10%<sub>P-P</sub> variation across the line and load variations is acceptable. For clarity, we refer to the incoming line voltage as  $V_{IN}$  and the output voltage supplied to the digital load as  $V_{OUT}$ .

#### A. Regulator With Source Follower Output Stage

Fig. 1(a) shows a linear regulator topology with source follower output driver. This topology achieves fast load regulation due to low output impedance of the source follower  $M_0$ . With sufficient voltage headroom  $M_0$  will operate in saturation which results in very good high-frequency power supply noise rejection. Unfortunately, this topology is not suitable for our application. With input voltage  $V_{IN}$  of 1.2 V, output voltage  $V_{OUT}$  of 0.9 V, and a typical threshold voltage  $V_T$  of 300–400 mV, there is not enough headroom for the gate voltage of  $M_0$  to accommodate the variations on  $V_{IN}$ . In addition, relatively small  $V_{GS}$  of  $M_0$  results in large silicon area.

#### B. Source Follower With Gate Overdrive

A modified topology in Fig. 1(b) features gate overdrive to increase  $V_{GS}$  of  $M_0$  to provide additional regulation headroom as well as reduce silicon area [2], [3]. This topology also uses replica biasing to further improve load regulation. Since the feedback loop does not observe output  $V_{OUT}$ , load regulation is based only on the  $I$ - $V$  characteristic of transistor  $M_0$  [2]. For a 90-mV droop, source conductance of transistor  $M_0$  limits the ratio of the minimum to maximum output current to about 1:10. A source follower without replica-biasing [3] does not have such

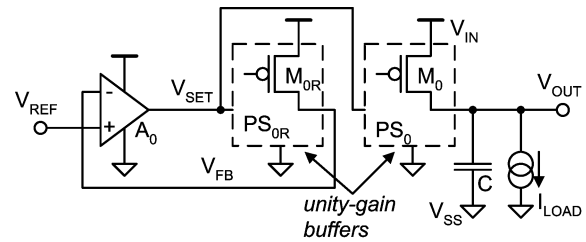


Fig. 2. Proposed low-dropout linear regulator topology with replica-biased common-source unity-gain buffer.

problem, but load regulation is limited by the bandwidth of the amplifier feedback loop.

#### C. Common-Source Output Stage

The topology in Fig. 1(c) achieves low dropout voltage without a need for gate overdrive [4], [5]. Also, since  $M_0$  can turn on with large  $V_{GS}$ , the silicon area required for the output stage is much smaller than for the regulator in Fig. 1(a). The main disadvantage is slow load regulation limited by the bandwidth of the amplifier feedback loop and poor supply noise rejection.

#### D. Proposed Topology

Obviously, none of the existing topologies offers low dropout voltage, small output droop, fast load regulation, and small silicon area. We realized that PMOS output driver operating with large  $V_{GS}$  is preferable for small dropout voltage and small silicon area. To understand the bottleneck of slow load regulation, we analyzed the operation of circuit in Fig. 1(c). The purpose of operational amplifier  $A_0$  is to guarantee that  $V_{OUT}$  tracks  $V_{REF}$  across variations of process, temperature,  $V_{IN}$ , and load current. Variations in process and temperature are slow while variations in  $V_{IN}$  and load current are very fast. The problem of tracking  $V_{REF}$  can be separated in two problems. First, for certain nominal conditions of process, temperature,  $V_{IN}$ , and load current the output voltage  $V_{OUT}$  should be equal to  $V_{REF}$ . Second, if any of the parameters deviates from the nominal conditions, the deviation of  $V_{OUT}$  from  $V_{REF}$  should be within the specified limit, e.g., 10%<sub>P-P</sub>. In order to solve the first problem, the control loop must have a sufficient open-loop gain, typically >40 dB, but the bandwidth is not critical. The second problem requires a much smaller gain, about 20 dB, but very high bandwidth is essential. Since the two problems have different requirements, they should be solved separately. In fact, the replica-biased source follower in Fig. 1(b) does just that by using a slow control loop to generate a gate bias voltage for the source follower  $M_0$  while fast load regulation is accomplished by the device  $I$ - $V$  characteristic.

We propose a linear regulator topology in Fig. 2 that emulates a replica-biased source follower. The NMOS driver  $M_0$  and its replica  $M_{0R}$  were replaced by unity gain P-stage buffers  $PS_0$  and  $PS_{0R}$  that utilize an internal PMOS driver transistor to achieve small dropout voltage and small area. Fast load regulation inherent to a source follower driver is not available in a common-source driver. Instead, load regulation is accomplished by a fast, single-stage feedback loop within the P-stage that



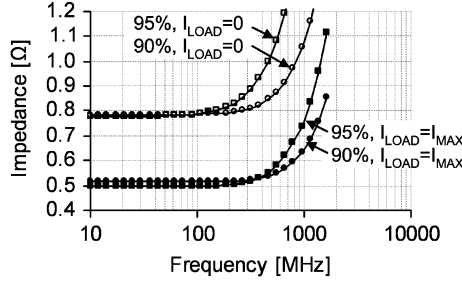


Fig. 6. Simulated output impedance (without  $C_{DIE}$ ) as a function of current efficiency and load current.

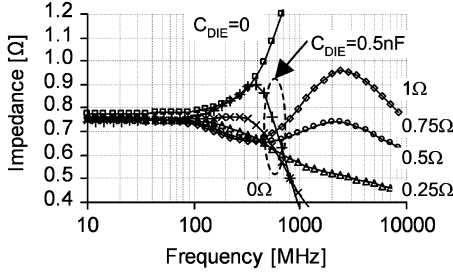


Fig. 7. Simulated output impedance without  $C_{DIE}$ , and with  $C_{DIE}$  of 0.5 nF and varying effective series resistance ESR.

decoupling capacitor  $C_{DIE}$  with a series resistance ESR adds a pole  $S_{P1}$  and two zeros  $S_{Z0}$  and  $S_{Z1}$ , where

$$S_{P1} = \frac{1}{ESR * C_{DIE}}$$

$$S_{Z0,1} = \frac{R + ESR}{2L} \left( 1 \pm 2\sqrt{1 - \frac{L}{(R + ESR)C_{DIE}}} \right).$$

Ideal response with voltage positioning is achieved when the zeros  $S_{Z0}$  and  $S_{Z1}$  cancel out the poles  $S_{P0}$  and  $S_{P1}$ , which happens for  $ESR = R$ , and  $C_{DIE} = L/R^2 = S_{P0}/R$ .

Fig. 7 shows the output impedance for  $C_{DIE}$  of 0.5 nF and ESR from 0 to 1  $\Omega$ . Impedance dependency on frequency is minimized for ESR of 0.75  $\Omega$ . Capacitor  $C_{DIE}$  is implemented as a PMOS inversion-mode gate capacitor. The ESR was tuned by adjusting the channel length. A larger droop  $\Delta V_{OUT}$  corresponds to a larger  $R$ . For a constant  $C_{DIE}$ , pole  $S_{P0}$  can move to a lower frequency which allows smaller bias current and improved current efficiency. Another option is to keep the quiescent current constant and reduce  $C_{DIE}$ . These tradeoffs between droop, decoupling capacitance and current efficiency are shown in Fig. 8. For a droop of 80 mV, the regulator achieves a 90% current efficiency with only 0.3 nF of decoupling. For higher current efficiency, e.g., 97%, the required decoupling capacitance increases to 0.8 nF.

Simple modifications in Fig. 9 provide a capability to digitally control the quiescent current. When  $TURBO = L$  transistors  $M_{1B}$ – $M_{3B}$  are off and the current efficiency improves but load regulation is slower. For  $STANDBY = H$ , the quiescent current is virtually zero and  $M_{3A}$  turns  $M_0$  off. The  $STANDBY$  signal can also be used to place some of the output buffers into a standby mode.

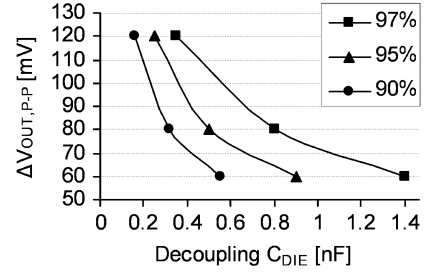


Fig. 8. Tradeoff between decoupling capacitance  $C_{DIE}$  and output variation  $\Delta V_{OUT}$  for current efficiencies 90%–97%.

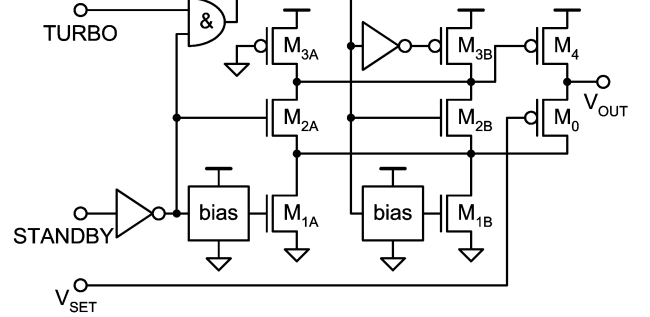


Fig. 9. P-stage unity-gain buffer with power-management.

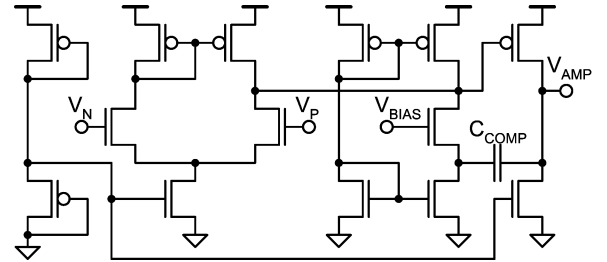


Fig. 10. Operational amplifier with cascode compensation.

## B. Operational Amplifier

The operational amplifier  $A_0$  utilizes cascode feedback compensation [8], which helps reduce the size of the compensation capacitor  $C_{COMP}$  to 120 fF (Fig. 10). The amplifier has an open-loop dc gain of 43 dB, phase margin of 86°, and unity gain frequency of 330 MHz.

## C. Pre-Driver (N-Stage)

The pre-driver, N-stage, shown in Fig. 11, was implemented as a complementary circuit of P-stage in Fig. 5(a). The main difference is that P-stage was sized for pull-up operation while N-stage was optimized for push-pull operation in order to reject the AC noise coupled to  $V_{SET}$  from  $V_{OUT}$  via the gate-source capacitance of P-stage transistor  $M_4$ . The N-stage shifts voltage  $V_{AMP}$  down by one  $V_T$  while the output stage shifts  $V_{SET}$  up by one  $V_T$  so that the overall shift from  $V_{AMP}$  to  $V_{OUT}$  is negligible. As we discovered in simulations, cascoding the N-stage and P-stage improved line regulation at high frequency because the supply noise coupled by the N-stage cancels out with the noise coupled by the P-stage. For example, if  $V_{IN}$  drops,  $V_{SET}$  rises due to negative gain through N-stage and  $V_{OUT0}$  drops due to positive gain through P-stage. However, the rise in  $V_{SET}$  will also cause  $V_{OUT0}$  to rise due to positive gain through P-stage.

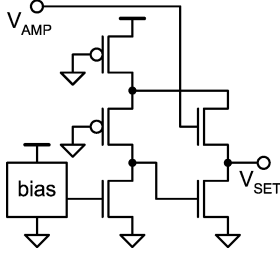


Fig. 11. N-stage pre-driver is a dual circuit of P-stage.

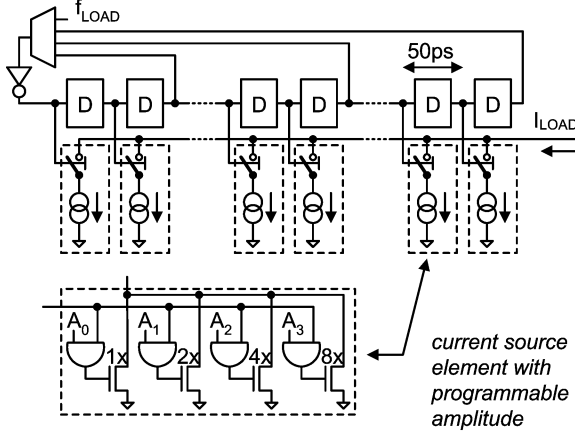


Fig. 12. On-die emulated transient load with programmable amplitude and rise time.

The two opposite effects cancel out supply noise at  $V_{OUT0}$  and hence  $V_{OUT}$ . The resulting high-frequency supply noise gain from  $V_{IN}$  to  $V_{OUT}$  is  $-16$  dB.

#### D. On-Die Programmable Load

Testing load response at gigahertz frequencies requires a circuit that can generate load transients with controlled ramp time of about 100 ps. Due to series inductance of the external leads, it is difficult to apply such current from outside of the regulator chip. Therefore, we implemented a programmable on-die transient load with adjustable amplitude, ramp time, and frequency (Fig. 12). The load can be triggered either by an external trigger connected to  $f_{LOAD}$  or by an internal ring oscillator with a loop delay selected by a multiplexer. The rising and falling edges are generated by accumulating the current supplied by ten current source elements staggered by 50 ps.

#### E. Layout of the Test Chip

The test chip was implemented in a 90-nm CMOS process [7] and laid out to match an available wafer probe card with a  $15 \times 2$  pad arrangement (see Fig. 13). The linear regulator was divided into two blocks to emulate a distributed regulator. Each block was rated at 50 mA and had an adjacent 50-mA load and a 0.3-nF decoupling capacitor. The blocks were located on the opposite ends of the power grid about 1 mm from each other. One P-stage is rated at 5 mA and occupied area of  $200 \mu\text{m}^2$ , which translates into output current density of  $25 \text{ A/mm}^2$ . Fig. 13 shows that the output transistor  $M_0$  occupies only about 25% of the P-stage area. The remaining space was occupied by the bias circuit. With higher current rating per P-stage, output current density as much as  $100 \text{ A/mm}^2$  is achievable.

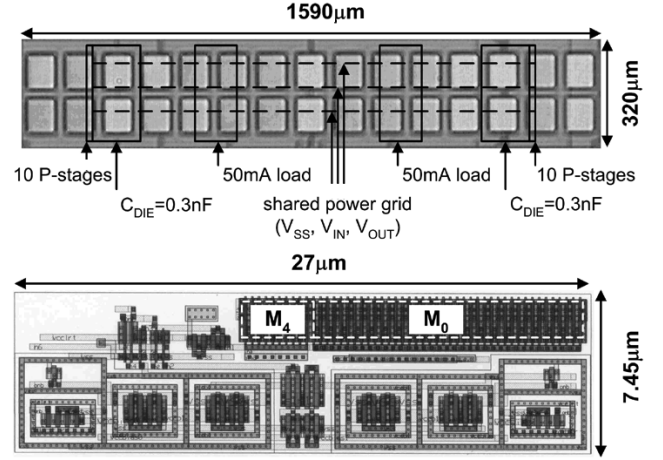


Fig. 13. Die micrograph of the linear regulator test chip and layout capture of a 5-mA P-stage buffer.

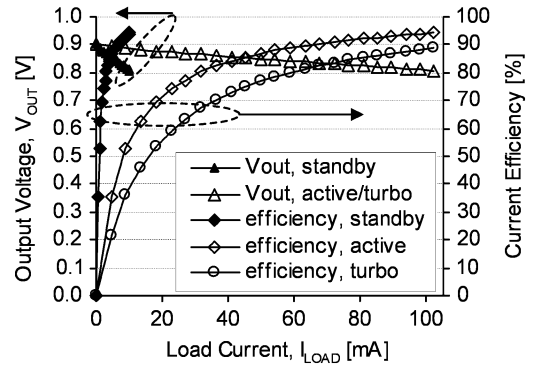


Fig. 14. Measured dc output characteristic and current efficiency in the standby, active, and turbo modes.

## IV. MEASUREMENT RESULTS

The chip was wafer-probed using a Cascade MicroTech probe card. The on-die voltages  $V_{IN}$ ,  $V_{OUT}$ , and  $V_{SS}$  were connected to three 50- $\Omega$  RF probes with a 20-GHz bandwidth. The dc voltages were tapped from each RF trace via a 4.7-k $\Omega$  series resistor and measured by a precision voltmeter.

#### A. DC Characteristic

Fig. 14 shows output  $V_{OUT}$  and current efficiency as a function of load current in the active mode with the output rating of 100 mA and current efficiency of 94%, in the turbo mode with the rating of 100 mA and current efficiency of 89%, and in the standby mode with the rating reduced to 10 mA by keeping only two P-stages active. Because of voltage positioning, the dc output droop at  $I_{MAX}$  is intentionally 10% below  $V_{REF}$  (refer to Fig. 4 and Section II-E).

#### B. Transient Response to a Load Step

Verification of the load response requires load transients with sub-nanosecond rise times and predictable amplitude was accomplished by the on-die programmable load circuit. The rise time and amplitude were determined from calibration measurements. Fig. 15 shows the transient measurements with an external 30-MHz load clock with a 50% duty cycle. The rise and fall times of the load current were 100 ps, and the amplitude

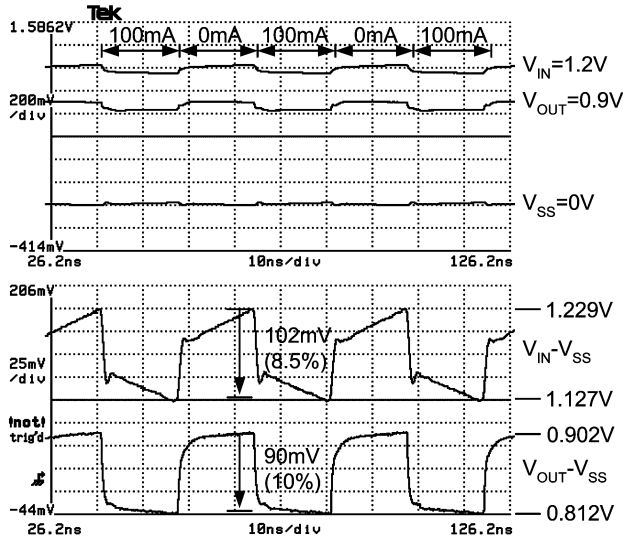


Fig. 15. Measured response to load step of 100 mA at 30 MHz with rise time of 100 ps in the active mode. Voltages  $V_{IN}$ ,  $V_{OUT}$ , and  $V_{SS}$  were probed simultaneously. Ground bounce was subtracted to produce on-die voltages.

changed between 0 and 100 mA according to the intervals overlaid in Fig. 14. The upper graticule shows the probed on-die voltages  $V_{IN}$ ,  $V_{OUT}$ , and  $V_{SS}$ . A load current applied at  $V_{OUT}$  causes a change in the regulator input current that leads to a droop on  $V_{IN}$  and bounce on  $V_{SS}$  primarily due to the series inductance of the probe card. The regulator perceives a sudden increase in the load current from 0 mA to  $I_{MAX}$  accompanied by a sudden decrease in its input voltage  $V_{IN} - V_{SS}$ , as shown in the lower graticule. Yet, the output voltage  $V_{OUT} - V_{SS}$  remains within a 10%<sub>P-P</sub> window with no signs of overshoot or undershoot. This measurement demonstrates successful voltage positioning and optimum transient response as described in Fig. 4.

According to Fig. 7, the output impedance should decrease to  $0.65 \Omega$  at 500 MHz, resulting in  $\Delta V_{OUT}$  of 65 mV for a 100-mA load current. Although the load current is trapezoidal rather than sinusoidal, the peak-to-peak droop in Fig. 16 is about 60 mV, which is much less than the 90-mV droop in Fig. 15. Changing ramp time from 100 to 500 ps had little effect on the droop waveform, which is likely due to the bandwidth limitation of the ac-termination and the oscilloscope.

We performed a frequency sweep of the load current from 1 to 600 MHz (Fig. 16). The upper and lower bounds of  $V_{IN} - V_{SS}$  and  $V_{OUT} - V_{SS}$  at each frequency are shown in Fig. 16. There is an anomaly at 10 MHz caused by resonance of the probe card series inductance with the probe card decoupling capacitance. Despite the excessive (out of specification) input noise, the regulator manages to reject the noise with minimal degradation.

## V. PERFORMANCE COMPARISON

The proposed low-dropout linear regulator was implemented in a 90-nm CMOS technology. For a 100-mA rating, the total regulator area is  $0.008 \text{ mm}^2$ , where  $0.004 \text{ mm}^2$  of area is consumed by the output stages. The 0.6-nF on-chip decoupling capacitor occupies  $0.090 \text{ mm}^2$ . The response time,  $T_R$ , is found from the required  $C_{DIE}$  for a specified  $I_{MAX}$  and  $\Delta V_{OUT}$

$$T_R = \frac{C * \Delta V_{OUT}}{I_{MAX}} = \frac{0.6 \text{ nF} * 90 \text{ mV}}{100 \text{ mA}} = 0.54 \text{ ns.}$$

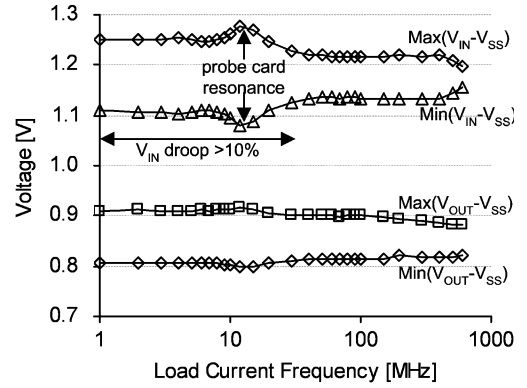


Fig. 16. Measured dependency of input/output voltage limits on the frequency of load current.

TABLE I  
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED  
LOW-DROPOUT LINEAR REGULATORS

|                                       | [4]  | [2]     | [3]    | [5]   | this work |
|---------------------------------------|------|---------|--------|-------|-----------|
| Year                                  | 1998 | 1998    | 2001   | 2003  | 2004      |
| Technology [ $\mu\text{m}$ ]          | 2    | 0.5     | 0.6    | 0.6   | 0.09      |
| $V_{IN}$ [V]                          | 1.2  | 5       | 2      | 1.5   | 1.2       |
| $V_{OUT}$ [V]                         | 0.9  | 3.3     | 1.8    | 1.3   | 0.9       |
| $I_{MAX}$ [mA]                        | 50   | 300     | 4000   | 100   | 100       |
| $I_Q$ [mA]                            | 0.23 | 0.75    | 0.2    | 0.038 | 6         |
| Current efficiency $\eta$ [%]         | 99.5 | 99.8    | 99.995 | 99.96 | 94.3      |
| $\Delta V_{OUT}$ [mV]                 | 19   | 400     | 220    | 130   | 90        |
| Response time $T_R$ [ $\mu\text{s}$ ] | 1.8  | 0       | 8      | 2     | 0.00054   |
| Decoupling $C$ [ $\mu\text{F}$ ]      | 4.7  | 0.00018 | 100    | 10    | 0.00060   |
| Scalable $\Delta V_{OUT}$             | yes  | no      | yes    | yes   | yes       |
| $C$ integrated on-die                 | no   | yes     | no     | no    | yes       |
| $FOM_1$ [ns]                          | 8.2  | 0.00060 | 0.28   | 4.9   | 0.032     |
| FO4 delay [ns]                        | 0.51 | 0.13    | 0.15   | 0.15  | 0.023     |
| $FOM_2$ []                            | 16   | 0.0047  | 1.8    | 32    | 1.4       |

For the purpose of comparison with other regulators designed to different specifications of droop, decoupling  $C$ , quiescent current  $I_Q$ , and current rating  $I_{MAX}$ , we define a figure of merit,  $FOM_1$ , as

$$FOM_1 = T_R \frac{I_Q}{I_{MAX}} = \frac{C * \Delta V_{OUT}}{I_{MAX}} * \frac{I_Q}{I_{MAX}} \text{ [ns].}$$

The smaller the  $FOM_1$ , the better the regulator. For example, two identical regulators operating in parallel with two times higher  $I_{MAX}$ ,  $I_Q$ , and  $C$  have the same  $FOM_1$  as each regulator operating standalone. Also, a reduction in the quiescent current by 50% and doubling of the capacitance does not affect  $FOM_1$ . According to Table I, the proposed regulator achieves smaller  $FOM_1$  than all other designs, with the exception of the replica-biased NMOS source follower with gate voltage overdrive [2]. Owing to a very fast load response, this is also the only other regulator with integrated capacitor. As mentioned in Section II-B, the problem with a replica-biased source follower is that the droop and current efficiency cannot be chosen independently. Therefore, this design is not suitable for a 90-mV

droop as it would lead to a current efficiency of <90%. The next closest competitor [3] with about  $8\times$  worse  $FOM_1$  is a source-follower-based regulator with gate overdrive. It could be argued that the  $8.7\times$  improvement in  $FOM_1$  is mostly due to the process scaling ( $0.6\ \mu\text{m}/90\ \text{nm} = 6.7\times$ ). Therefore, we defined  $FOM_2$ , which normalizes the regulator speed given by  $FOM_1$  by an estimated fan-out of four delay, FO4, of the process to remove the process dependence

$$FOM_2 = \frac{FOM_1}{T_G} = \frac{T_R}{T_G} \frac{I_Q}{I_{MAX}} = \frac{C * \Delta V_{OUT,DRP}}{T_G I_{MAX}} * \frac{I_Q}{I_{MAX}}$$

The proposed linear regulator and the source follower regulator [3] achieve comparable  $FOM_2$ . This means that in a given process, both topologies are equally efficient in utilizing the available quiescent current for load regulation. However, since our regulator makes use of a single-stage load regulation while the source-follower regulator requires at least two stages, we expect that ultimately our topology should be about two times faster than the source follower [3]. In other words, if the quiescent current  $I_Q$  of the source-follower regulator is increased to reduce  $T_R$ , at some point the decrease in  $T_R$  will not offset the increase in  $I_Q$  and  $FOM_2$  will degrade. It should be pointed out that the source follower [3] utilized a BiCMOS process which has an advantage in driving of high fan-out capacitive load, e.g., the gate capacitance of the pull-up driver.

## VI. CONCLUSION

We have demonstrated a low-dropout linear regulator for multi- $V_{DD}$  microprocessors in a 90-nm CMOS technology. Compared to other designs suitable for 1.2–0.9 V conversion, the proposed regulator achieves a very fast response time of 0.54 ns, and best figure of merit which accounts for the decoupling capacitance, output droop, current efficiency, and current rating. The regulator occupies  $0.008\ \text{mm}^2$  of silicon area and is fully integrated with a 0.6-nF decoupling capacitor that consumes  $0.090\ \text{mm}^2$ . The regulator combines single-stage load regulation with voltage positioning and replica biasing to achieve optimum load regulation. Output current density of  $100\ \text{A}/\text{mm}^2$  is achievable for output rating larger than 1 A.

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