A Wide-Range Delay-Locked Loop With a Fixed Latency of One Clock Cycle

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***Abstract*—A delay-locked loop (DLL) with wide-range operation and fixed latency of one clock cycle is proposed. This DLL uses a phase selection circuit and a start-controlled circuit to enlarge the operating frequency range and eliminate harmonic locking problems. Theoretically, the operating frequency range of the DLL can be from $1/(N \times T_{D\max})$ to $1/(3T_{D\min})$, where $T_{D\min}$ and $T_{D\max}$ are the minimum and maximum delay of a delay cell, respectively, and N is the number of delay cells used in the delay line. Fabricated in a 0.35-μm single-poly triple-metal CMOS process, the measurement results show that the proposed DLL can operate from 6 to 130 MHz, and the total delay time between input and output of this DLL is just one clock cycle. From the entire operating frequency range, the maximum rms jitter does not exceed 25 ps. The DLL occupies an active area of 880 μm $\times$ 515 μm and consumes a maximum power of 132 mW at 130 MHz.**

***Index Terms*—Delay-locked loops, latency, phase-locked loops, wide range.**

I. Introduction

With THE evolution and continuing scaling of CMOS technologies, the demand for high-speed and high integration density VLSI systems has recently grown exponentially. However, the important synchronization problem among IC modules is becoming one of the bottlenecks for high-performance systems.

Phase-locked loops (PLLs) [1]–[3] and delay-locked loops (DLLs) [4]–[7] have been typically employed for the purpose of synchronization. Due to the difference of their configuration, the DLLs are preferred for their unconditional stability and faster locking time than the PLLs. Additionally, a DLL offers better jitter performance than a PLL because noise in the voltage-controlled delay line (VCDL) does not accumulate over many clock cycles.

Conventional DLLs may suffer from harmonic locking over wide operating range. If the DLLs are to operate at lower frequency without harmonic locking, the number of delay stages must be increased to let the maximum delay of the delay line be equal to the period of the lowest frequency. However, the maximum operating frequency of a DLL will be limited by the minimum delay of the delay line.

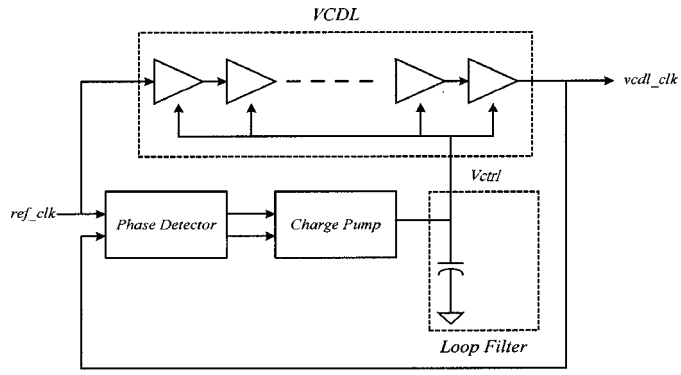

Fig. 1. Block diagram of the conventional analog DLL.

In this paper, a DLL with wide-range operation and fixed latency of one clock cycle is proposed by using the phase selection circuit and the start-controlled circuit. The proposed DLL not only locks the delay equal to one clock cycle but also operates without the restrictions stated above. The operating frequency range of the proposed DLL can also be increased.

The range problem of conventional DLLs will be discussed in Section II. The architecture of the proposed DLL will be introduced in Section III and the building blocks in this DLL will be described in Section IV. Measurement results are given in Section V. Conclusions are given in Section VI.

II. Range Problem of Conventional DLLs

A conventional DLL, as shown in Fig. 1, consists of four major blocks: the phase detector (PD), the charge-pump circuit, the loop filter, and the VCDL. In the DLL, the reference clock, ref_clk, is propagated through VCDL. The output signal, vcdl_clk, at the end of the delay line is compared with the reference input. If delay different from integer multiples of clock period is detected, the closed loop will automatically correct it by changing the delay time of the VCDL. However, the conventional DLL will fail to lock or falsely lock to two or more periods, $T_{\rm clk}$, of the input signal if the initial delay of the VCDL is shorter than 0.5 $T_{\rm clk}$ or longer than 1.5 $T_{\rm clk}$, as shown in Fig. 2. Therefore, if the DLL is required to lock the delay to one clock cycle of the input reference signal, the initial delay of the VCDL needs to be located between 0.5 $T_{\rm ref}$ and 1.5 $T_{\rm ref}$ [7], regardless of the initial voltage of the loop filter. Assume that the maximum and the minimum delay of the VCDL are $T_{\rm VCDL\_max}$

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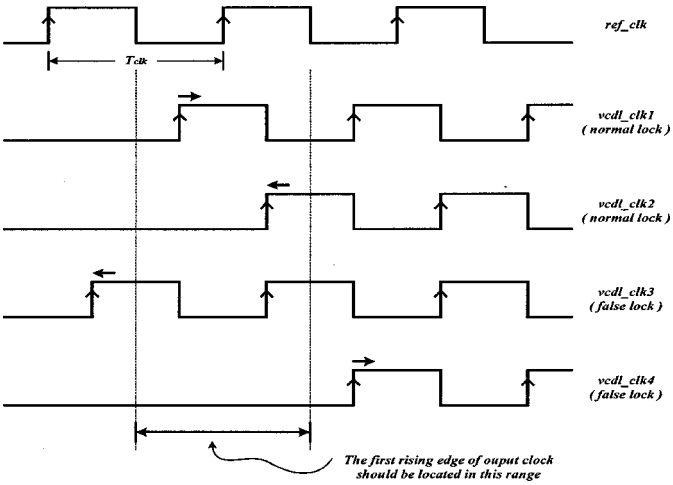

Fig. 2. DLL in normal lock and false lock conditions.

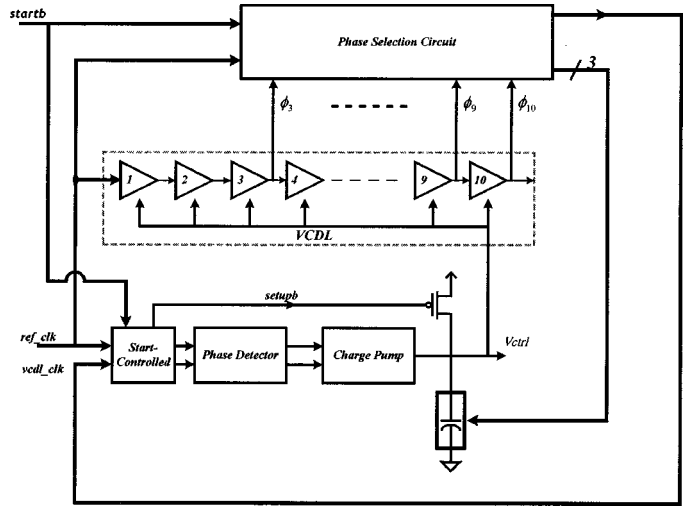

Fig. 3. System architecture of the proposed DLL.

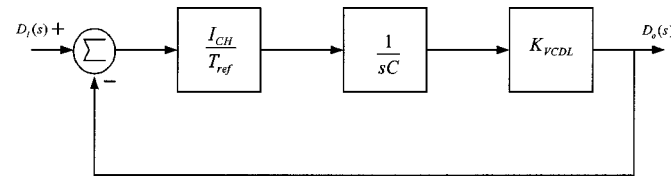

Fig. 4. Small-signal model of the conventional analog DLL.

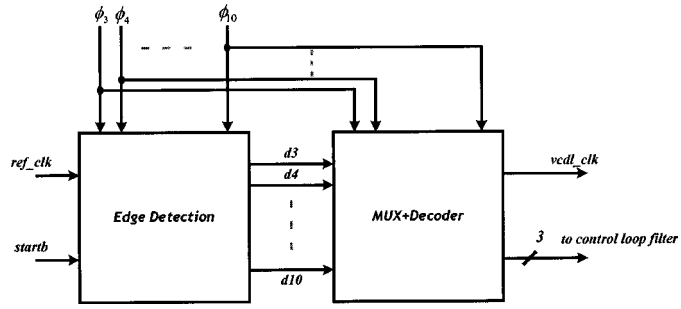

Fig. 5. Block diagram of the phase selection circuit.

and $T_{\mathrm{VCDL\_min}}$, respectively. As a result, the period of the input signal should satisfy the following inequality [7]:

$$\mathrm{Max}\left(T_{\mathrm{VCDL\_min}}, \frac{2}{3}\times T_{\mathrm{VCDL\_max}}\right) < T_{\mathrm{CLK}} < \mathrm{Min}\left(T_{\mathrm{VCDL\_max}}, 2\times T_{\mathrm{VCDL\_min}}\right) \quad (1)$$

Equation (1) shows that the DLL is prone to the false locking problem when process variations are taken into account [7]. Therefore, some solutions [6]–[10] are proposed to overcome this problem. They are described as follows.

First, the basic idea is to use a phase-frequency detector (PFD) [5], because it has a capture range of $(-2\pi, +2\pi)$ wider than other phase detectors. So, the PFD is a better choice for wide range operation. However, the PFD cannot be used in the DLL alone without any control circuit because the DLL will try to lock a zero delay. A PFD combined with a control circuit is presented in [6]. Nevertheless, in some cases, especially for high-frequency operations, the initial delay between ref_clk and vcdl_clk, as shown in Fig. 1, may be larger than two clock cycles and harmonic locking will occur.

Second, a solution called an all-analog DLL using a replica delay line [7] has been developed to solve the narrow frequency range problem of a conventional DLL. If the delay range of the VCDL satisfies the relation $T_{\mathrm{VCDL\,min}} < 1/7 \times T_{\mathrm{VCDL\,max}}$, the DLL will have a maximum operation range of 7:1.

Third, a digital-controlled DLL called the self-correcting DLL is proposed in [8]. The problem of false locking is solved by the addition of a lock-detect circuit and the modified phase detector. Although this self-correcting DLL avoids false locking, the outputs of the VCDL are required to have an exact 50% duty cycle.

The DLL developed in [9] uses a stage selector for fast-locked and wide-range operations, but the DLL requires an additional VCDL, which increases the area. A similar DLL can automatically change its lock mode to extend the operation range, but the latency of the DLL will be larger than one clock cycle [10].

The approach presented in this work uses a phase selection circuit to automatically decide what number of delay cells should be used. This can enable the DLL to operate in the wide-frequency range. A new start-controlled circuit is also presented for the DLL to solve false locking problems and keep the latency of one clock cycle. The exact 50% duty cycle is not necessary.

III. Architecture of the Proposed DLL

The architecture of the proposed DLL is shown in Fig. 3. It is composed of a conventional analog DLL, a phase selection circuit, and a start-controlled circuit. Before the DLL begins to lock, the phase selection circuit will choose an appropriate delay cell to be a feedback signal (vcdl_clk) according to different frequencies of input signal. In other words, the number of the delay cells may change at different input frequencies. The minimum delay $T_{D\,\mathrm{min}}$ of the delay line is determined by one unit-delay cell. The maximum delay can be decided as $N \times T_{D\,\mathrm{max}}$ where N is the number of unit-delay cells. Thus, the operating frequency range of the DLL can be from $1/(3T_{D\,\mathrm{min}})$ to $1/(N \times T_{D\,\mathrm{max}})$.

The linear model of the DLL is shown in Fig. 4, where the summer stands for a phase detector, I_{cp} is the charge-pump cur-

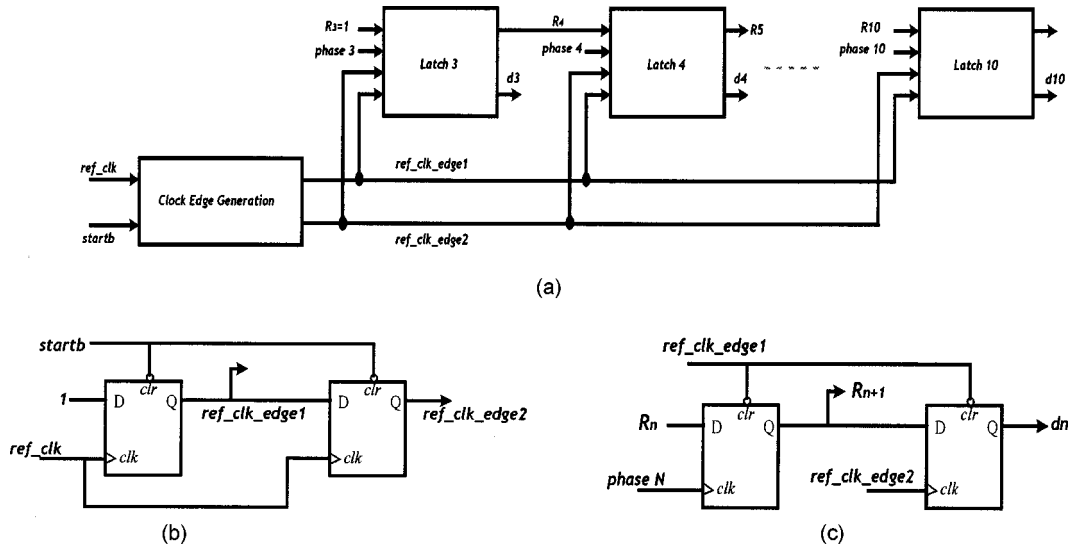

Fig. 6. Schematic of edge detection circuit. (a) Edge detection circuits. (b) Clock edge generation. (c) Latch N.

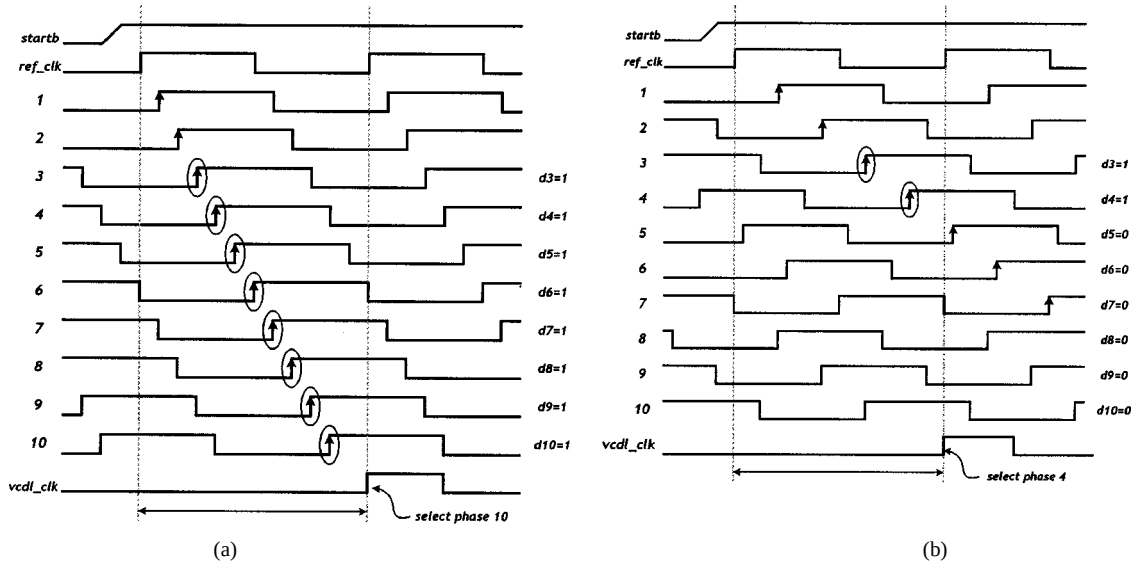

Fig. 7. Timing diagram of edge detection circuit.

rent, T_{REF} is the period of the input reference clock, C is the capacitor value in the loop filter, and K_{VCDL} is the gain of the VCDL which is proportional to the number of delay cells. In the steady-state locked condition, the s-domain transfer function can be expressed as [11]

$$\frac{Do(s)}{D_I(s)} = \frac{1}{1+\dfrac{s}{\omega_N}} \tag{2}$$

where D_I is the input delay time and D_O is the output delay time. The loop bandwidth ω_N can be expressed as [11]

$$\omega_N = \frac{I_{\mathrm{CH}} \cdot K_{\mathrm{VCDL}}}{T_{\mathrm{REF}} \cdot C} \tag{3}$$

Since the transfer function is inherently stable, a wider loop bandwidth can be used to achieve fast acquisition time, but the jitter performance will be degraded. Hence, the following tradeoff design guideline was suggested in [12]:

$$\frac{\omega_N}{\omega_{\mathrm{REF}}} = \frac{I_{\mathrm{CH}} \cdot K_{\mathrm{VCDL}}}{2\pi \cdot C} \leq \frac{1}{10} \tag{4}$$

where $\omega_{\mathrm{REF}} = 2\pi/T_{\mathrm{REF}}$.

When the input frequency is higher, the phase selection circuit will select the smaller number of delay cells and K_{VCDL} will become smaller. In order to have an adequate loop bandwidth for the DLL, the capacitances used in the loop filter must become smaller. In this work, the 3-bit control signals generated from the phase selection circuit will switch the number of capacitors in the loop filter depending on the selected phase.

After the vcdl_clk is decided, the DLL will start the locking process, which is controlled by the start-controlled circuit. First, the delay between input and output of the VCDL is initially set to the minimum value and then allows the *down* signal of the PFD output activate, supposing that the VCDL's delay increases with control voltage decreasing. Therefore, the delay between

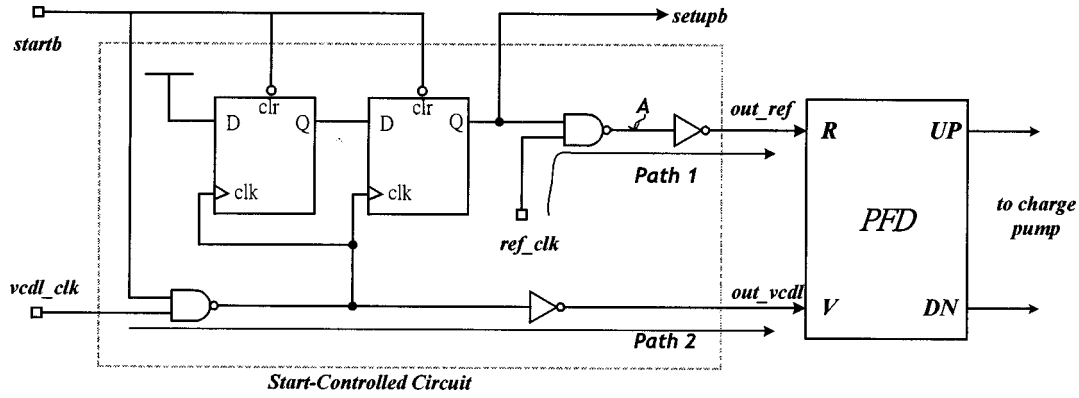

Fig. 8. Schematic of start-controlled circuit associated with PFD.

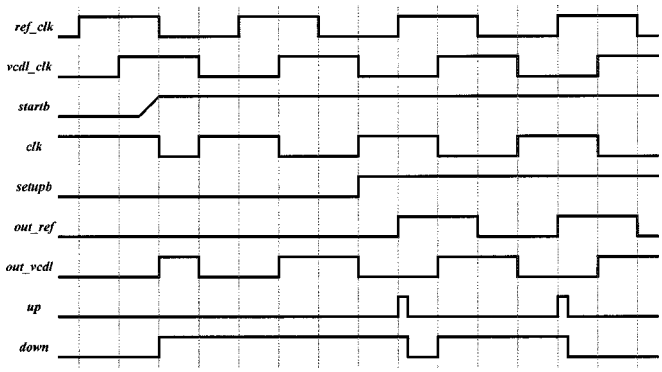

Fig. 9. Timing diagram of start-controlled circuit.

input and output of the VCDL will increase until it reaches one clock period of the input signal. Thus, the DLL will not fall into false locking and the latency is fixed to one clock cycle no matter how long a delay the VCDL provides.

IV. Circuit Description

A. Phase Selection Circuit

The phase selection circuit consists of two blocks: an edge detector and a multiplexer with a decoder, as shown in Fig. 5. The schematic and timing diagram of the edge detector are shown in Figs. 6 and 7, respectively. To guarantee that the latency of the DLL is just one clock cycle, the first two clock phases in Fig. 6 are reserved for measurement. In practice, the first two clock phases could be included in the phase selection circuit to improve the operating frequency range of the DLL. At the initial state, the signal *startb* is set to low to reset the edge detector outputs (i.e., d3 $\sim$ d10) and the delay of the VCDL is set to its minimum value. When the signal *startb* goes high, the edge detector will detect the rising edge of input signals in sequence during the next two rising edges of ref_clk. Referring to Fig. 7(a), suppose that the signals all have rising edges in sequence during one clock cycle, therefore, the outputs (d3 $\sim$ d10) are all high and the multiplexer will select phase 10 as the output signal, vcdl_clk. However, if the input frequency is higher, suppose that the timing diagram is similar to Fig. 7(b). All the inputs have rising edges during one clock cycle, but only the rising edges of phases 1 $\sim$ 4 in sequence lead the selected phase to be 4. The vcdl_clk will be low until the selected phase is chosen. After

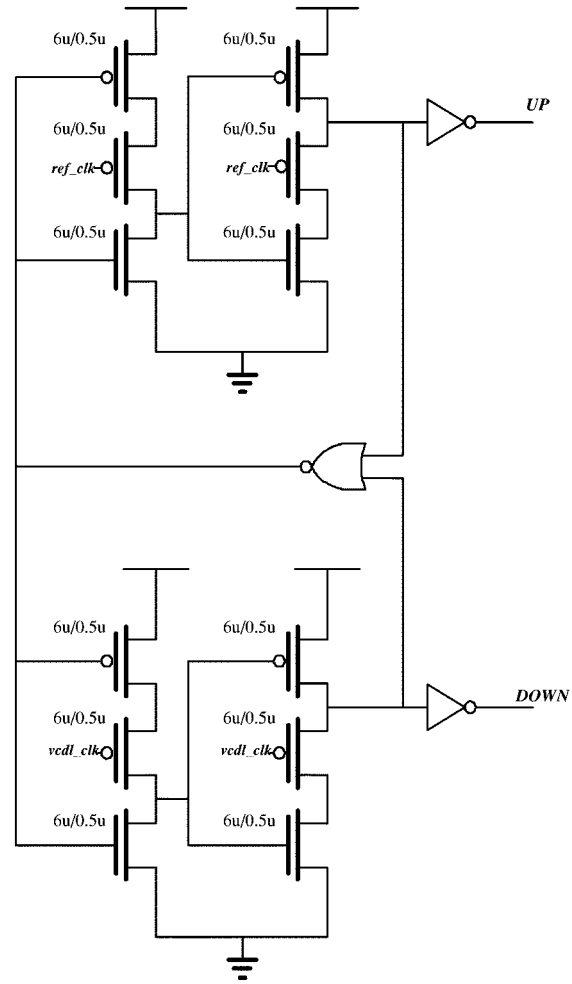

Fig. 10. Schematic of the PFD circuit [12].

the vcdl_clk is decided, the DLL will start the locking process, which will be explained later. By the decoder, signals (d3 $\sim$ d10) are decoded to generate 3-bit control signals, which switch the number of capacitors used in the loop filter for tuning the loop bandwidth.

B. Start-Controlled Circuit

The schematic of the start-controlled circuit and the associated PFD are shown in Fig. 8. It is composed of only two rising-edge trigger D-flip-flops (DFFs), two NAND gates, and

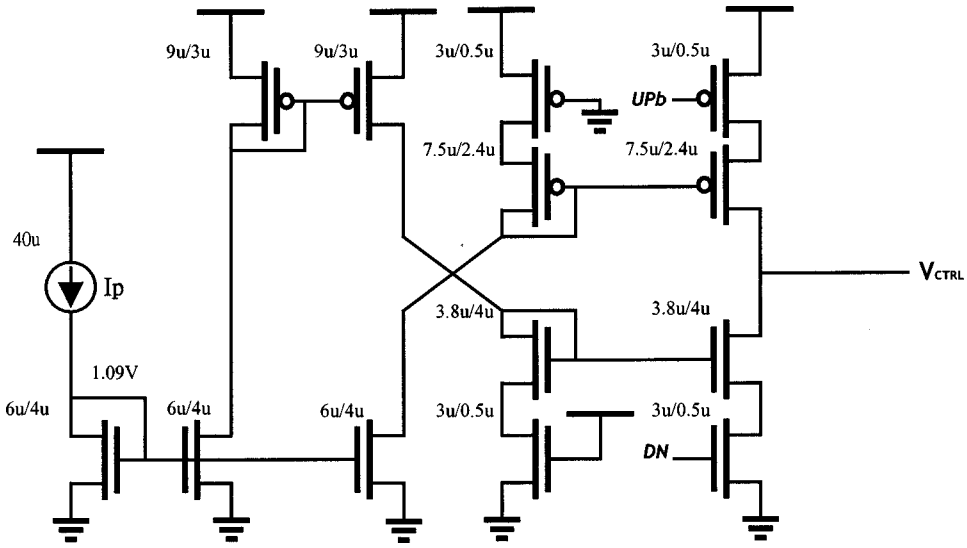

Fig. 11. Schematic of the charge-pump circuit [11].

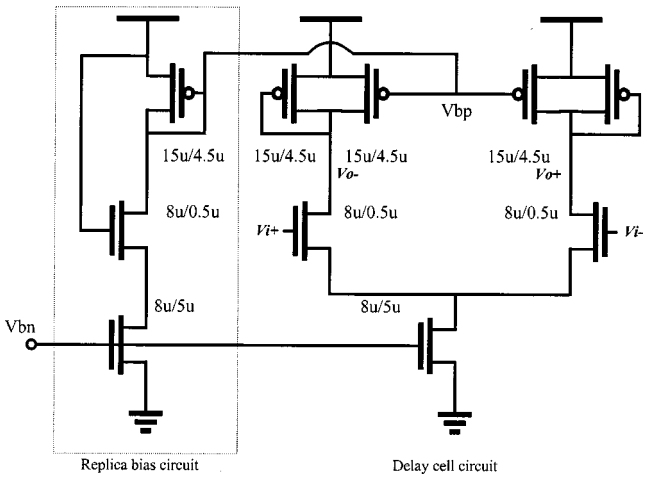

Fig. 12. Schematic of the delay cell with replica bias [12].

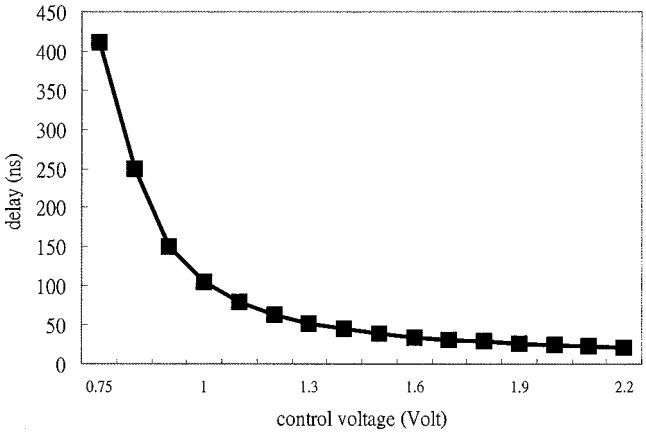

Fig. 13. Simulated transfer curve of the VCDL.

two inverters. The timing diagram of this start-controlled circuit is shown in Fig. 9. Initially, *startb* is set to low in order to clear the two DFF's outputs. Therefore, *setupb* is low and pulls the control voltage to V_{DD}, as shown in Fig. 3 (i.e., set the VCDL delay to its minimum value). In this way, the two inputs of the

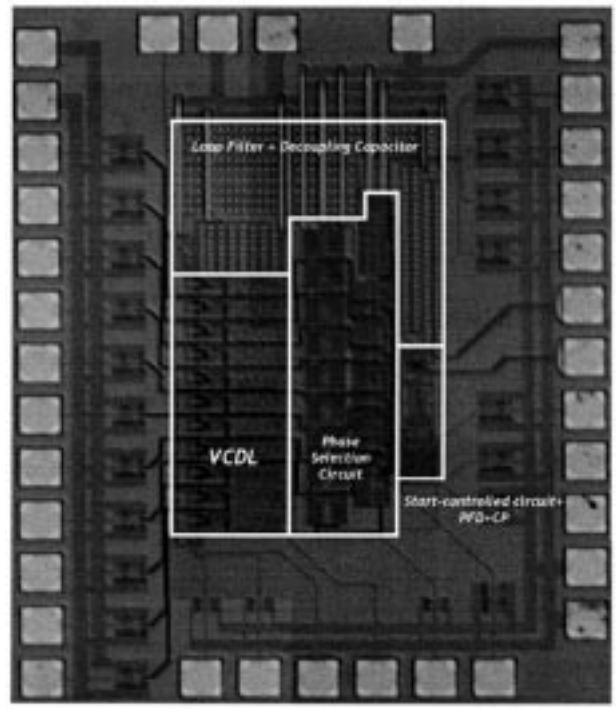

Fig. 14. Microphotograph of the chip.

PFD are in low level. When *startb* goes to high, *setupb* will also go to high. After two consecutive falling edges of vcdl_clk trigger the DFFs, the down signal of the PFD will be activated and let the delay of the VCDL increase. The delay of the VCDL will increase until it is equal to one clock period of the input signal due to the nature of negative feedback architecture. Since the start-controlled circuit forces the delay of the VCDL to its minimum value and controls the delay of the VCDL to increase until its delay is equal to one clock period, the DLL will not fall into false locking even when $10\,T_{D\min} < 0.5T$. In order to get equal delays for path1 and path2, dummy loads should be added in point A. In comparison with [6], this start-controlled circuit

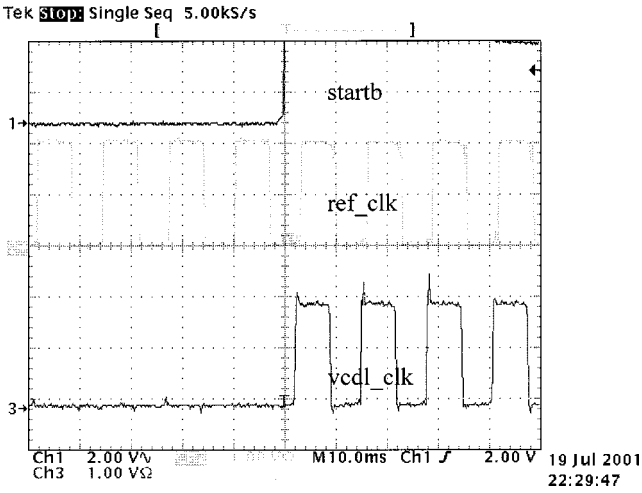

Fig. 15. DLL at initial state when operating frequency is 6 MHz.

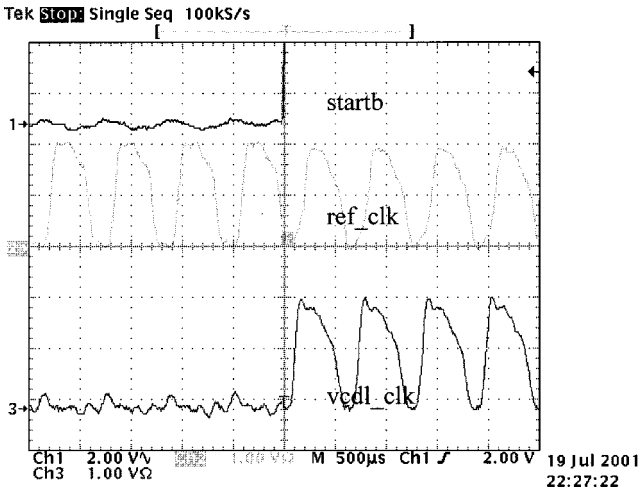

Fig. 16. DLL at initial state when operating frequency is 130 MHz.

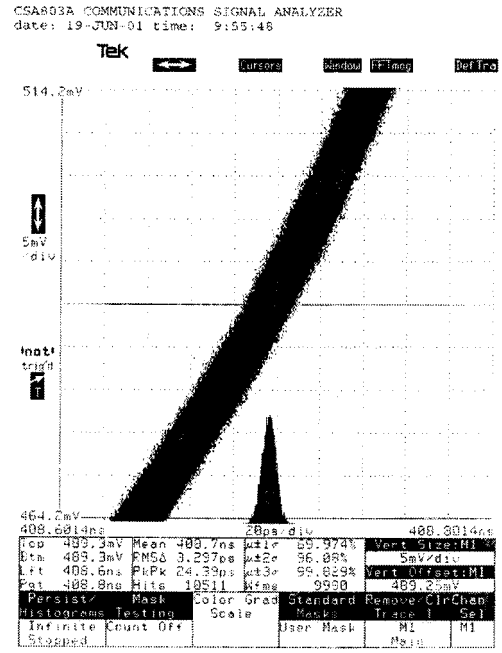

Fig. 17. Jitter histogram when DLL operates at 130 MHz.

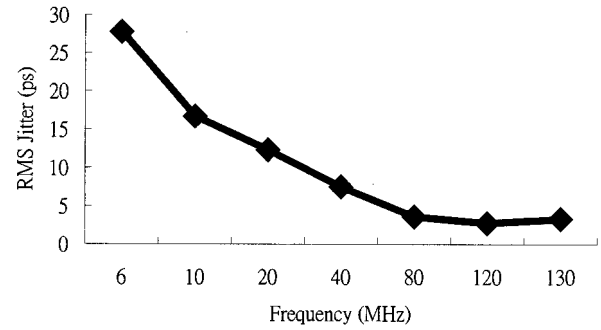

Fig. 18. Measurement results of rms jitter over different frequencies.

has two advantages: the proposed circuit is simple, and the duty cycle of ref_clk and vcdl_clk is not required to be exactly 50%.

C. Other Circuits

In this work, the dynamic logic style PFD [13] is adopted to avoid the dead-zone problem and improve the operating speed. To mitigate charge injection errors induced by the parasitic capacitors of the switches and current source transistors, the charge-pump circuit developed in [11] is used here. The delay cell circuit is similar to [11]. The schematics of these circuits are shown in Figs. 10–12. The control voltage of the loop filter is directly connected to nMOS rather than pMOS. Therefore, the transfer curve of delay versus control voltage is monotonic decreasing, as shown in Fig. 13.

V. Experimental Results

The prototype chip is fabricated in a 0.35-μm single-poly triple-metal standard CMOS process. The microphotograph of the chip is shown in Fig. 14. The capacitors used in the loop filter are integrated in the chip and formed by metal-to-metal capacitors. The experimental results show that the DLL can operate in the frequency range of 6–130 MHz. Figs. 15 and 16 show the first four cycles of the DLL in the locking process when the operating frequency is 6 and 130 MHz, respectively. After the signal *startb* is high, the phase selection circuit will select one of the outputs of the VCDL as close as possible to the next rising edge of the input clock, ref_clk. Figs. 15 and 16 also show that after the signal *startb* is high, the first rising edge of

TABLE I
Performance Summary

Process	0.35-µm 1P3M TSMC CMOS process
Operating Voltage	3.3 V
Operating Frequency Range	6 MHz ~ 130 MHz
RMS Jitter	24.77 ps @ 6 MHz 3.297 ps @ 130 MHz
Peak-to-Peak Jitter	210 ps @ 6 MHz 24.3 ps @ 130 MHz
Lock time	~1130 clock cycles (simulated)
Power Dissipation	132 mW @ 130 MHz
Active Area	880-µm×515-µm @ without pads

the output clock of the VCDL, vcdl_clk, leads that of the input clock, ref_clk. Since the signal *startb* will set the control voltage $V_{\rm ctrl}$ in Fig. 3 to V_{DD}, the proposed phase detector and the current-pump circuit will discharge the loop filter to increase the delay of the VCDL. It will align the phases between the input clock and output clock of the VCDL. Fig. 17 shows the jitter histogram when the DLL operates at 130 MHz. Fig. 18 shows the measurement results of rms jitter over different frequencies. Table I gives the performance summary. The proposed DLL can be seen to have a wide-operational range and a fixed latency of one clock cycle.

VI. Conclusion

A DLL with wide-range operation and fixed latency of one clock cycle is proposed. First, the multiphase outputs of the VCDL are all sent to the phase selection circuit. Then the phase selection circuit will automatically select one of the delayed outputs to feedback. As a result, this DLL can operate over a wide range without suffering from harmonic locking problems. Ideally, this DLL can operate from $1/(N \times T_{D\,\max})$ to $1/(3T_{D\,\min})$. The experimental results also demonstrate the functionality of the proposed DLL. Moreover, at different operating frequencies, the jitter performances are all in an acceptable range and the latency is just one clock cycle. Since the speed of the proposed circuits can be increased if the more advanced process is used, the performance of the DLL such as the operating frequency range can be improved with a little hardware and design effort. The power consumption of the digital part in the DLL and the total die area will also be reduced.

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