Analysis on LDO Design

LDO Design for RF circuits

Jacob Jia

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1. Introduction on LDO Design

Low dropout regulator (LDO) is a linear voltage regulator. It is featured by a clean output voltage with the low noise, low ripple.

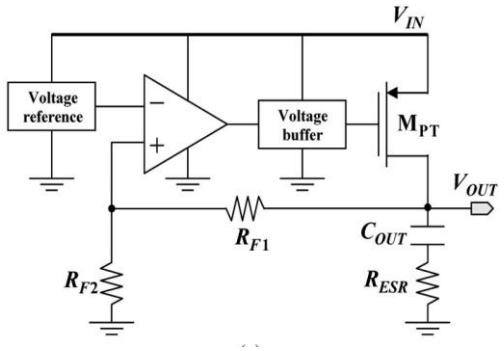


Fig. 1 The circuit diagram of LDO

Normally, a typical LDO consists of a op-amp to control output voltage, a buffer to drive the Power/Pass transistor, the power transistor (PMOSFET or NMOSFET) to provide a stable voltage with a strong driving capability.

1. Types of LDOs

Based on the output filter capacitor - C_{out}, LDOs can be classified the one with an external off-chip capacitor on PCB and the one without external capacitor which is also called capless or cap-free LDO.

For LDO with an external capacitor, the external large capacitor like a water pool can store and release the extra chargers caused by the loading current transient variation. Therefore, it can be used to reduce the spike (overshoot and undershoot) due to a large dynamic transient load variation. So this kind of LDO is used for the high dynamic load current block such as the large digital circuit. The larger external capacitor also can improve the PSR at high frequency. However, the LDO with off-chip capacitor needs an extra pad and pin on chip and package respectively, also, the external capacitor is used. **In addition, due to the bonding wire, it will introduce a spike voltage in the chip when the load current has a large transient variation**.

Now the capless LDO becomes popular which can save one output pad, pin and off-chip capacitor. Because there is no large external capacitor(which can be used to reduce the voltage spike due to the fast transient load variation and improve PSR at high frequency), the unit-gain bandwidth of cap-less LDO normally should be large to improve PSR and transient response (Wide UBGW is not the only way to improve the PSR and reduce the spike, it can be also realized by improving the architecture of LDO design. It will be mentioned in the followed contents).

2. Critical Design Performance/SPEC

The key design performance of LDO includes high PSRR, low noise, low ripple, fast transient response, low quiescent no-load current, good line regulation and load regulation. For RF system, the high PSRR (to isolate the interference from power supply), low noise/ripple are very important. Besides the above requirement, the stability is always necessary for LDO.

2. LDOs design in Reference Circuit

1. PMU Topology

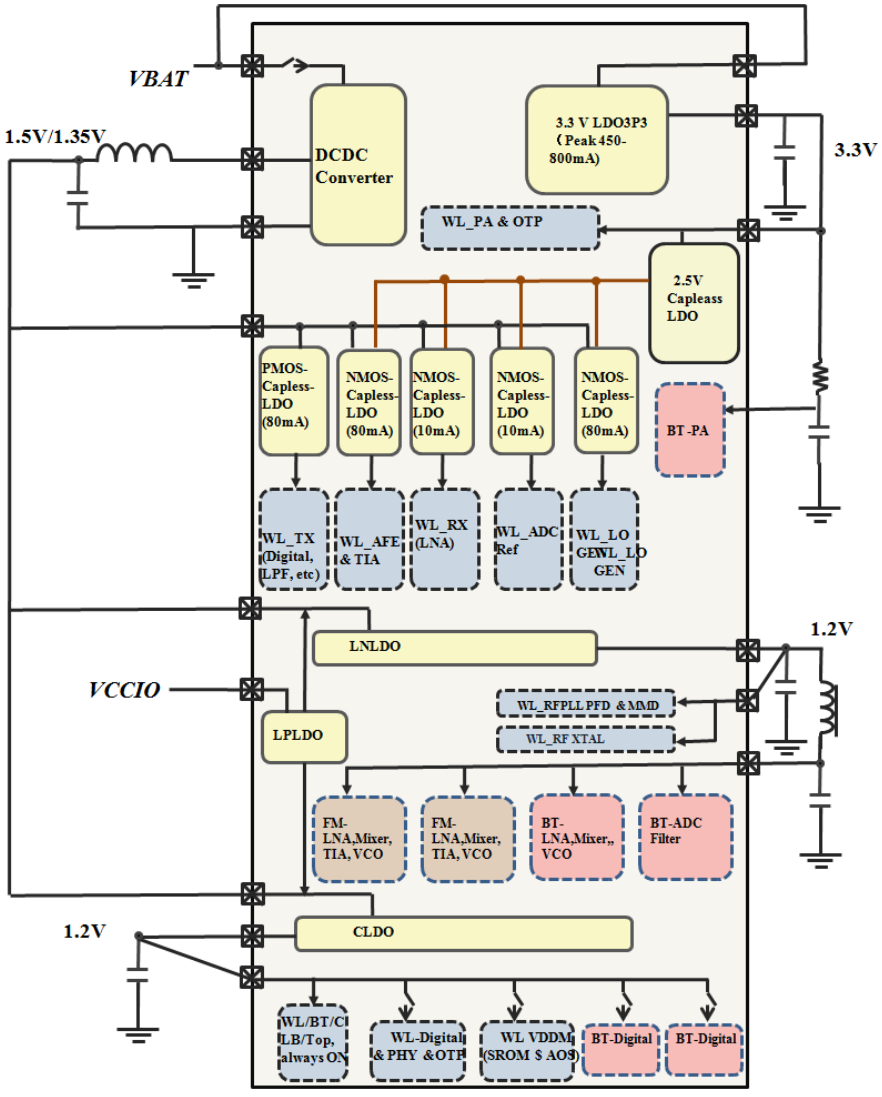


Fig. 2 PMU Topology

2. PMU Introduction

In the reference circuit, the PMU (power management unit) consists of the following regulators.

1. One BUCK DCDC converter (VBAT to 1.35V/1.5V, Avg_Iout=170mA), it can provide 1.5/1.35V power supply for on-chip LDOs.

2. LDO3P3(VBAT to 3.3V, Avg_Iout=200mA), it can provide 3.3V power supply for WL-RF-PA, Bluetooth PA and other blocks.

3. CLDO (Core LDO, 1.5/1.35V to 1.2V, Avg_Iout=80mA), which can provide 1.35V-0.95V power supply to digital blocks. A pass function is included.

4. LNLDO (Low noise LDO, 1.5/1.35V to 1.2V, Iout=100mA), through a magnetic bead filter, it can provide a 1.2V low noise power supply for WL, BT and FM block such as BT & FM ‘s VCO, LNA etc.

5. A mini PMU for Wireless Radio including 5 LDOs (1.5/1.35V to 1.2V), it can provide low noise, low ripple, high PSRR 1.2V output voltage for WL’s LNA, LOGEN, and ADC’s reference etc.

6. Low noise LDO (3.3V to 2.5V/1.8V, Iout=10mA), it can provide low noise power supply for WL’s ADC, AFE, LOGEN and other blocks.

7. LPLDO (VCCIO, 18V/3.3V to 1.35V/1.5V, Iout=40mA), it will be turned on to provide 1.35V/1.5V power supply when CBUCK is disable.

Regulator	Power conversion domain	Output Current (mA)	Circuit Blocks (provide power supply for)	Type of regulators
CBUCK (Core BUCK DCDC converter)	VBAT (2.4V - 4.8V) to 1.35V/1.5V	Ipeak=370mA; Iavg = 170mA	WL-mini PMU (LDOs), LNLDO,CLDO	Switching Power supply
LDO3P3	VBAT (2.4V - 4.8V) to 3.3V	Ipeak=800mA; Iavg=200mA	WL-OTP, WL-RFPA, BT-PA and 2.5VLDO	Linear regulator with external Capacitor
CLDO (Core LDO)	1.5V/1.35V to 1.2V	Ipeak=200mA; Iavg=80mA	Digital Core ,PHY, VDDM etc.	Linear, with external Cap
LNLDO (Low-noise LDO)	1.5V/1.35V to 1.2V	100mA	FM&BT VCO,LNA,Mixer and WL_RF_PFD	Linear, with external Cap, magnetic bead
Mini-PMU-LDOs (5 Low-noise WL_RF_LDOs)	1.5V/1.35V to 1.2V	10mA/80mA	WL_RF_LOGEN,LNA, ADC reference, TIA,TX etc.	Linear, capless
LNLDO (Low-noise LDO)	3.3V to 2.5V/1.8V	10mA	WL-RF ADC,AFE, LOGEN, LNA and NMOS（power transistor）@ mini-PMU-LDOs	Linear, capless
LPLDO1	3.3V/1.8V to 1.5V/1.35V	40mA	Active when CBUCK off.	Linear, External cap

Table. 1 Summry on regulators of PMU

3. Analysis on LDOs

1. Design on LNLDO with Off-Chip Capacitor

1. Design requirement

For the Low Noise LDO with off-chip capacitor, it requires the output noise, ripple of LDO as small as possible to satisfy the requirement of RF blocks. Also, the stability of LDO must be guaranteed within a large load current range.

2. Circuit diagram of LNLDO with off-chip capacitor

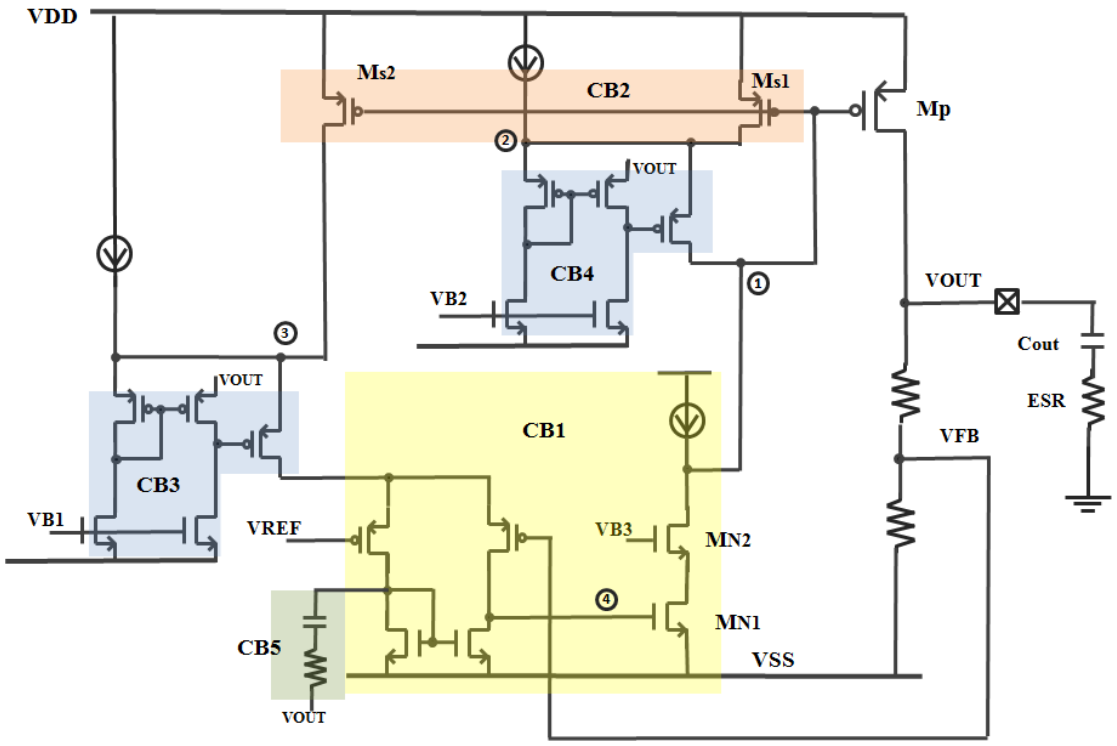


Fig. 3 The circuit diagram of LNLDO

LNLDO mainly includes several important circuit blocks – CB1(Core amplifier), CB2- the sensing transistors , CB3 and CB4,(amplifier help to force the drain of sensing transistor equal to drain voltage of the sensed power transistor), CB5 (transient spike feedback path from VOUT).

3. Analysis on function of different circuit blocks

Generally, for a LDO with an off-chip capacitor, the dominant pole is located at the output stage because of the huge capacitor on PCB. However, the frequency of dominant pole will change dramatically due to the wide load variation as shown in the followed Fig.3, then, the phase margin of the system should become less even unstable with two close poles.

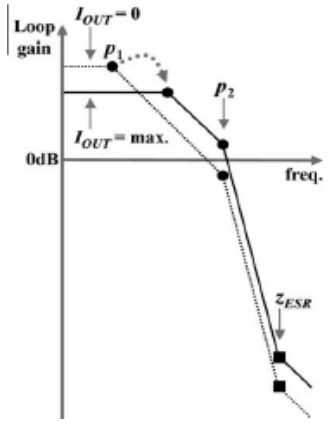


Fig. 4 The bode plot of the conventional LDO

So, a **load-tracking technique** [1] is used in this LDO by sensing the load current. In CB2, both Ms1 and Ms2 can be used to sense the current of Mp (the power transistor of LDO). Also, Ms1 can be used to reduce the impedance at node 1 to $1/gm_{\_Ms1}$ and the pole at this node is pushed to further frequency than the dominant pole at output of LDO. Compared with the conventional sensing method (only the Ms1/Ms2 sensing transistor), an amplifier (CB3/CB4) is added to force the drain voltage of Ms1/Ms2 equal to Mp, so that Ms1/Ms2 can work in the same operational region with Mp to realize an accurate sensing. The impedance at node 1 ($1/gm_{\_Ms1}$) will be changed following the load current proportionally and the pole at node 1 will also move with the dominant pole changing as shown in Fig. 4. (If there is no CB3/CB4, the Ms1/Ms2 will operate in a saturation region, and Mp operates in a linear region. The sensed current is not a linear ratio to load current.)

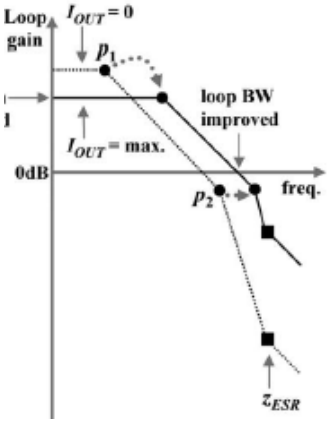


Fig. 5 The bode plot of the conventional LDO with load tracking.

For CB3/CB4, VOUT is connected with the inverting input, the output and non-inverting input is shorted like a voltage follower to force output of opamp is equal to inverting input voltage [2]. The

drains of Ms1 and Ms1- node 2 and node 3 are equal to VOUT respectively.

CB1 is a typical two stage amplifier, MN2 is used for two targets, 1- to increase the effective channel length by cascade; 2- to remove the miller cap effect on node 4 by Cgd of MN1 then push the pole at node 4 to a higher frequency.

CB5 is transient spike feedback loop from VOUT of LDO to reduce the spike voltage at VOUT.

A large capacitor – Cout can improve the PSRR at high frequency and reduce the spike/ripple at the output stage.

2. Design on CLDO with Off-Chip Capacitor

CLDO (Core-LDO) is similar with LNLDO. One bypass function is included.

3. Design on LPLDO with Off-Chip Capacitor

LPLDO is a low power LDO with off-chip capacitor to provide a 1.35V/1.5V instead of CBUCK when CBUCK is disable.

1. Circuit diagram of LPLDO

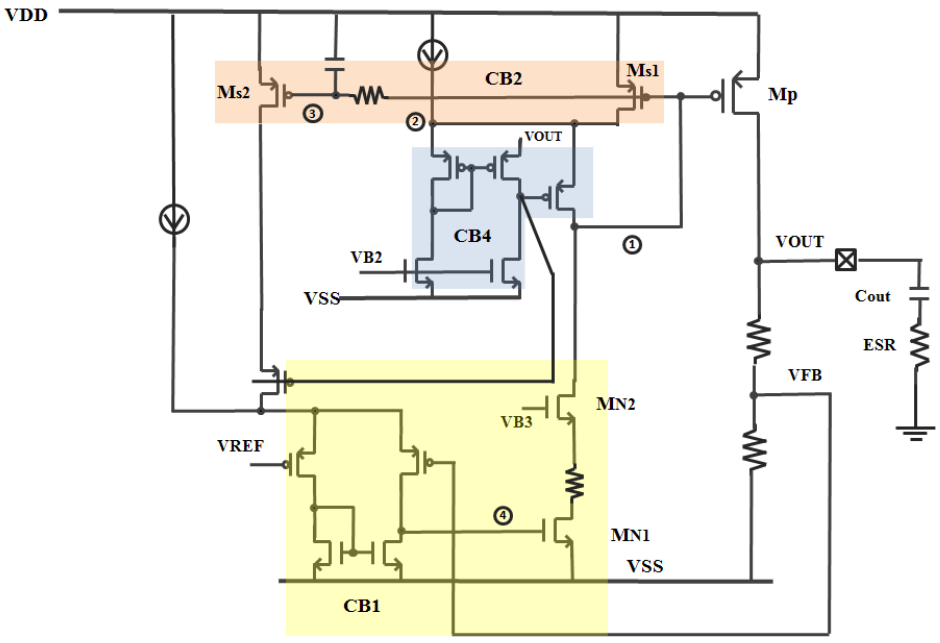


Fig. 6 The circuit diagram of LPLDO

The structure of LPLDO is similar with LNLDO/CLDO. The different point is that one current sensing opamp is removed and the other one is re-used for two current sensing PMOSFETs to save the power of LDO itself. CB1 is the control opamp to control the output voltage of LDO. in CB2, there is RC filter to improve the PSR of control opamp- CB1.

4. Design on LDO3P3 with Off-Chip Capacitor

LDO3P3 is used to directly convert the battery power supply to a 3.3V output voltage supply.

1. Circuit diagram of LDO3P3

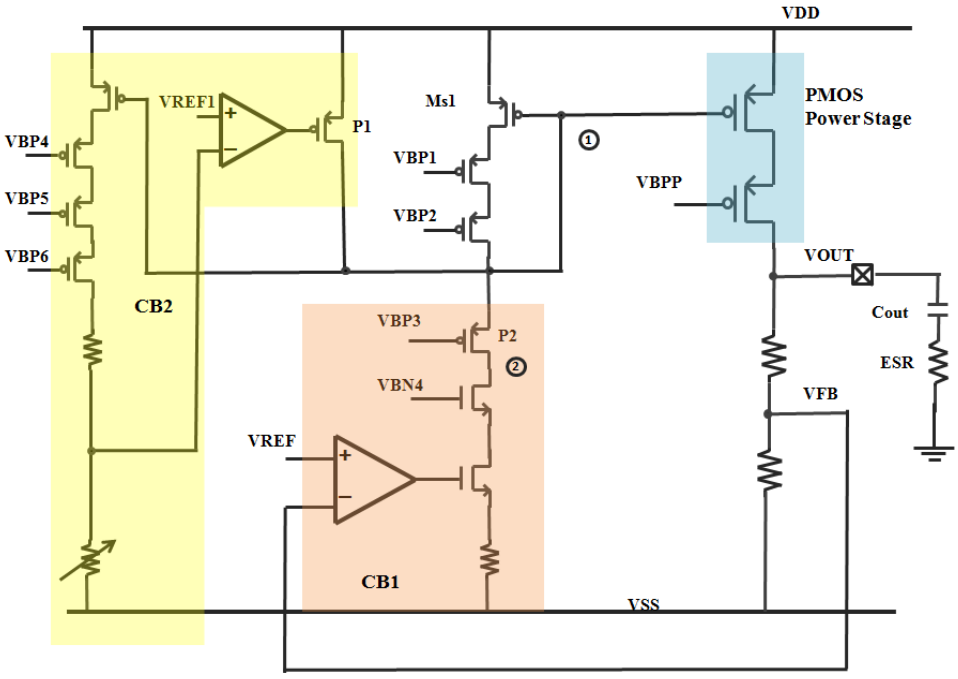


Fig. 7 The circuit diagram of LDO3P3

CB1 is the main LDO control block. CB2 is the peak output current control block.

2. Analysis on function of different circuit blocks

Different with the other LDOs (their power supplies are connected with the internal power such as CBUCK or LDOs), LDO3P3's power supply is directly from battery. To reduce the effect on the other systems which are connected with the same battery, the large /start-up/transient/DC current of LDO3P3 must be limited.

Therefore, CB2 is included which is used to define the peak output current of LDO3P3. At the light load case, the voltage on node 1 is high and P1 is turned off at the power stage of LDO. So, there is no current from P1 to the node 1. The voltage on the node1 is controlled by the control opamp- CB1. When the load current becomes large enough, the voltage on node 1 becomes lower, then, P1 is turned on to control the voltage on node 1 together with CB1. The voltage on node 1 is clamped to set the maximum output current of LDO.

The PMOSFET – P2 is used to guarantee the voltage on node 1 is not too low at a extreme heavy load case, then to protect the Ms1and Power PMOSFET on the output stage from a breakdown by a high Vgs .

5. Design on Capless LDO without Off-Chip Capacitor

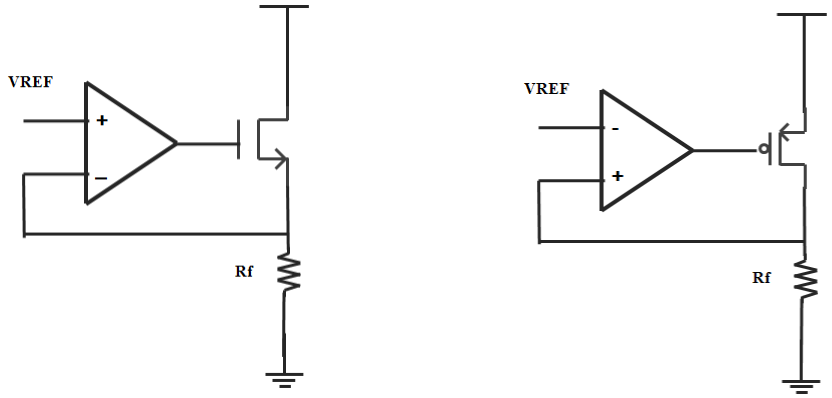
1. Design on capless LDO with NMOS pass transistor

For RF LDO, the low noise, low spike/ripple and high PSRR are necessary to the noise-sensitive RF circuit. In this design, a NMOSFET is used at output power stage.

1. Advantage of LDO with NMOSFET as pass transistor

First, the dominant pole of the capless LDO is located in the opamp not at the output of LDO that is different with off-chip cap LDO where the dominant pole is located at output stage of LDO. For the LDO with NMOS pass transistor, the pole of output stage can be further with different loads due to low impedance at NMOSFET output stage. The phase margin can be compensated easily.

Second, the NMOS LDO has a low spike/ripple at output of LDO. The comparison on LDOs with NMOS and PMOS power stage is given by the following.



(a) (b)

Fig. 8 (a) The LDO circuit diagram with NMOS (b) The LDO circuit diagram with PMOS

The Output impedance of LDO with NMOS and PMOS pass transistor is given by

$$R_{out\_NMOS} = \frac{1}{(A(s)+1)g_{mn}} // R_o \qquad \text{Eq - 1}$$

$$R_{out\_PMOS} = \frac{1}{A(s)g_{mp}} // R_o \qquad \text{Eq - 2}$$

where A(s) is transfer function of the Opamp, and $R_o = R_{ds} // R_f$

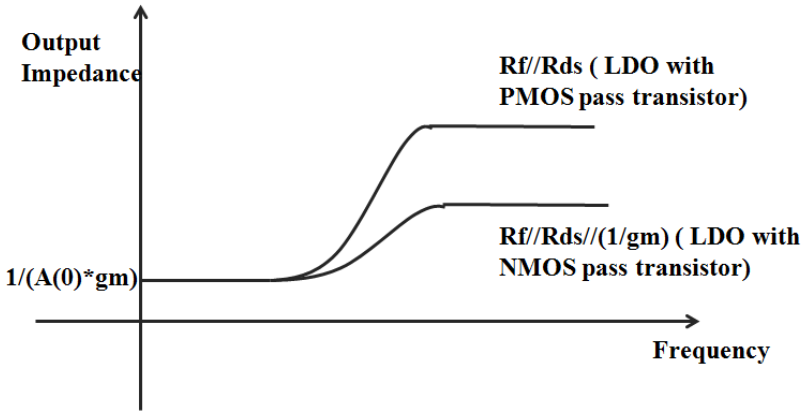


Fig. 9 Output Impedance of LDO with NMOS and PMOS respectively.

Because 1/gm < R_o, so for LDO with the NMOSFET pass transistor, it's output impedance ($\frac{1}{g_{mn}} // R_o$) is much smaller than the impedance of PMOS LDO at high frequency where the gain of opamp $A(s) \approx 0$. Since the ripple/spike at output is depending on the output impedance and load current variation ($V_{out\_spike} = I_{load\_tran} R_{out}$), the ripple/spike on the output of NMOS LDO is much smaller

than the PMOS LDO at high frequency.

Third, the NMOS LDO can be used to realize the low noise output. Because it is not like PMOS LDO which needs a much wider UGBW to reduce the output ripple/spike, the NMOS LDO can add a large capacitor on the output of opamp to filter the noise at output of opamp.

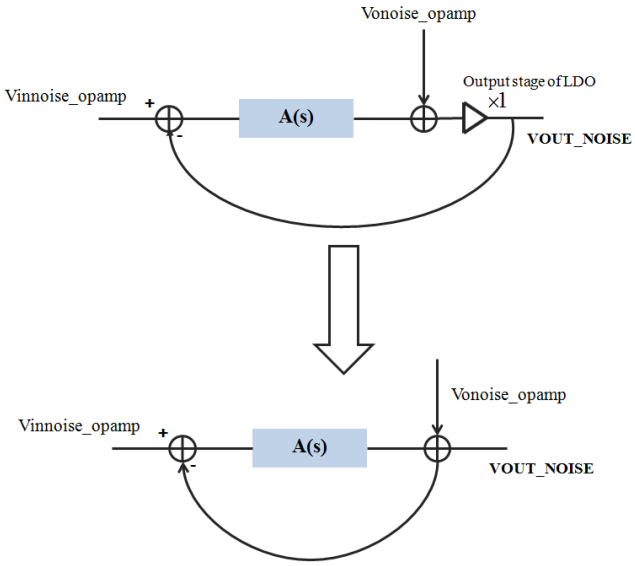


Fig. 10 SFG on LDO noise.

Based on the above signal-flow-graphic on LDO noise, the final noise output of LDO can be given by

$$V_{OUT\_N} = \frac{A(s)}{1+A(s)}\left(\frac{V_{ON}}{A(s)} + V_{INN}\right) \qquad \text{Eq - 3}$$

where, A(s) is the transfer function of opamp, V_{ON} is the noise of opamp's output stage, V_{INN} is the noise of opamp's input stage. For NMOS LDO, the V_{ON} can be filtered by a capacitor. So, the NMOS LDO has a lower noise than the noise of PMOS LDO at high frequency where $A(s) \le 1$.
The disadvantage of NMOS LDO is that two different power supplies are necessary. The high voltage power supply should be higher than VOUT_max by at least one threshold voltage.

Fourth, compared with the LDO with PMOS pass transistor, the LDO with NMOS pass transistor has a better PSR performance on the output power stage at the high frequency.

2. Circuit diagram of the Capless LDO

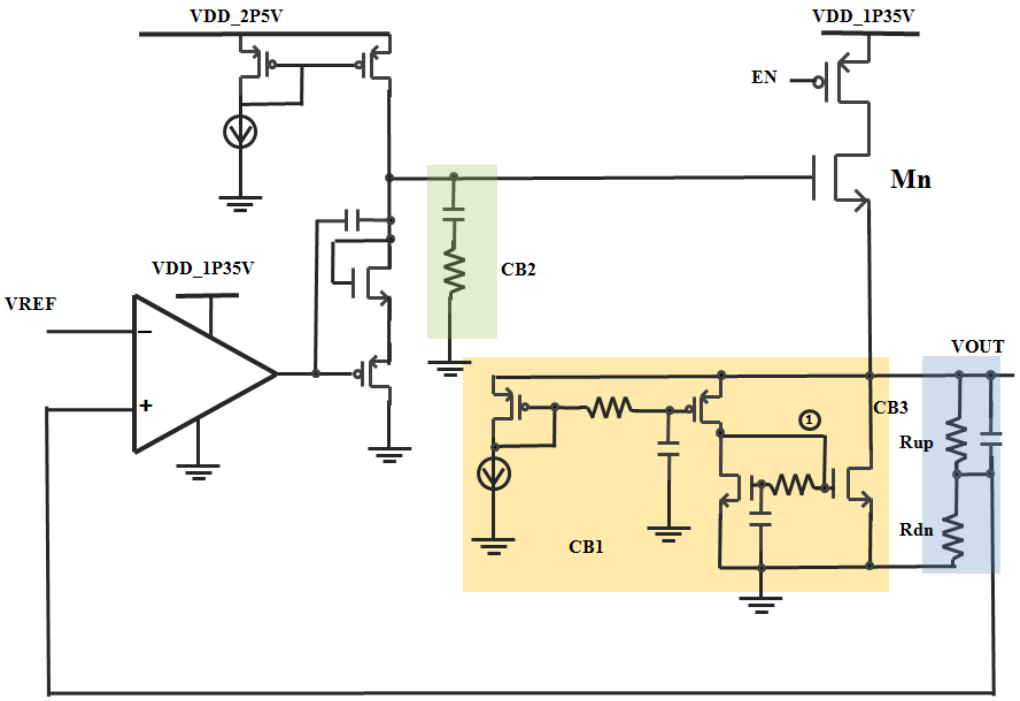


Fig. 11 Circuit diagram of NMOS Capless LDO

3. Analysis on function different circuit blocks

In the capless LDO, the block cell CB1 is a fast transient spike/ripple response loop to reduce the transient spike/ripple caused by a dynamic load current variation. When VOUT has a spike, the node 1 will follow the VOUT variation to eliminate the VOUT spike/ripple.

CB2 is used to filter the output noise of the opamp to reduce the output noise at output of LDO.

CB3 is used to improve phase margin by a lead compensation $\frac{s+z}{s+p}$ where $z=\frac{1}{CR_{up}}$,

$p=\frac{1}{C(R_{up}\,//\,R_{dn})}$. Z < P.

2. Design on capless LDO with PMOS pass transistor

1. Circuit diagram of capless LDO with PMOS power transistor

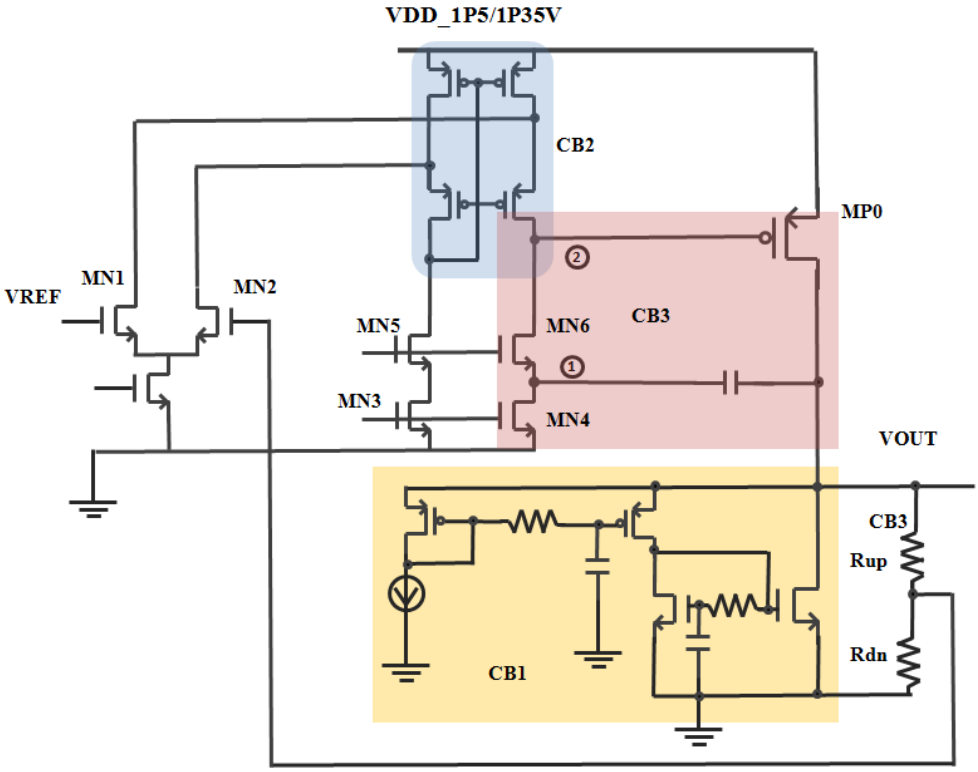


Fig. 12 Circuit diagram of PMOS Capless LDO

2. Analysis on circuit block function

1. Block cell CB1 is same with the previous design for improving transient response to reduce output spike.

CB2 is a self bias cascade To improve PSRR of PMOS LDO, the self-bias should be at up-side (PMOS side), so that node 2 can follow the voltage variation on VDD to cancel the variation of Vgs of the power pass transistor.

To enlarge the UGBW, the current buffer compensation is used in CB3 [6,7]. For the conventional miller compensation in a two-stage opamp, the poles and zero are

$$p_1 = -(R_{o1} C_C g_{m\_O} R_{o2})^{-1} \qquad \text{Eq - 4}$$

$$p_2 = -(C_L / g_{mo})^{-1} \quad \text{Eq - 5}$$

$$z_1 = C_C / g_{mo} \quad \text{Eq - 6}$$

where R_{o1} and R_{o2} are the output resistance of 1st and 2nd stages respectively, C_C and C_L are the miller capacitor (between the outputs of 1st and 2nd stages) and the load capacitor at output stage. g_{mo} is the transconduction of the output stage. z_1 is a RHP zero.

With the current buffer compensation (also called Ahuja compensation which was proposed by B.K.Ahujia firstly [6]), the poles and zero of the LDO are given by

$$p_1 = -\frac{1}{R_{o1} C_C g_{MP0} R_{o2}} \quad \text{Eq - 7}$$

$$p_2 = -\frac{g_{MP0} C_C}{C_2 C_L} \quad \text{Eq - 8}$$

$$p_3 = -\frac{g_{MN6}}{C_C + C_{gs\_MN6}} \quad \text{Eq - 9}$$

$$z_1 = -\frac{g_{MN6}}{C_C + C_{gs\_MN6}} \quad \text{Eq - 10}$$

R_{o1} and R_{o2} are the output resistance of 1st and 2nd stages respectively, C_2 is the capacitance at the node 2. P_3 and Z_1 can be cancelled by each other.

6. Summary on LDO Design

1. Summary on Spike Reduce Technique

Wider UGBW, smaller output impedance, fast transient spike feedback loop and enhanced slew rate of gate of power transistor can be used to reduce the spike on the output of LDO. [3,4].

As aforementioned NMOSFET Pass transistor can be used to reduce the spike due to the small output impedance, Also, a shunt feedback can be used to reduce the output impedance with PMOSFET pass transistor as shown in the followed figure.

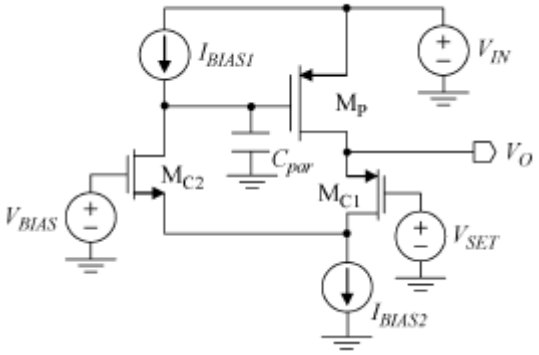


Fig. 13 Circuit diagram of with follower shunt feedback

With the shunt-feedback , the output impedance of VO is reduced dramatically especially with a light load.

Some kinds of fast transient spike feedback loop or spike detection circuit [3] is also used to reduce to spike voltage at output as in Fig.8 CB5 and Fig.9 CB1.

2. Summary on High PSRR Design

LDO's PSRR is determined by Opamp's AC gain, conductance of power pass transistor, the output impedance (load impedance) and the parasitic capacitance of the power pass transistor. At the low and middle frequency, PSR is determined by conductance of power pass transistor and opamp's AC gain. At high frequency, PSR is determined by the parasitic capacitance of the power pass transistor and the impedance of the output (load).

For LDO with an external capacitor, the large cap has low impedance at high frequency which can improve PSRR at high frequency. However, due to the parasitic bonding wire's inductance and ESR of capacitor, the PSR cannot be reduced infinitely.

SFG of LDO's PSR is given by

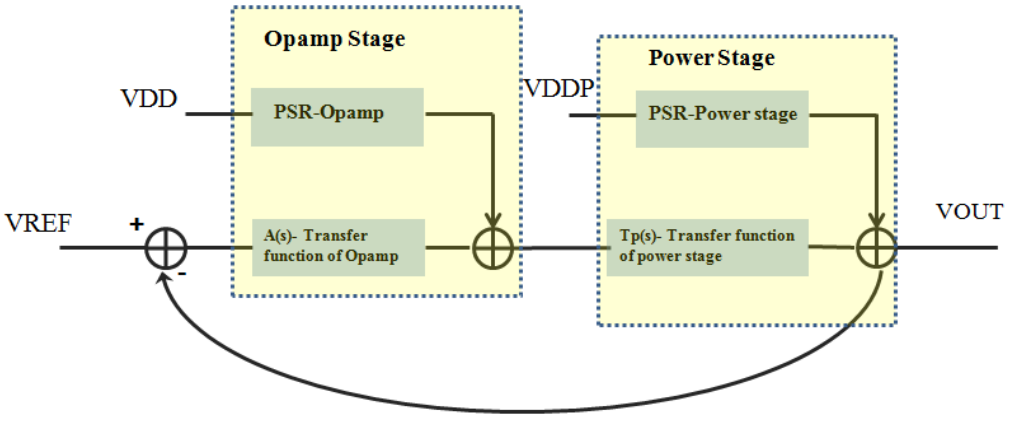


Fig. 14 PSR SFG of LDO

when VDD=VDDP, the transfer function of PSR can be given by

$$PSR = \frac{VOUT}{VDD} = \frac{PSR_{OPAMP}T_P(s) + PSR_{Powerstage}}{1 + A(s)T_P(s)} \qquad \text{Eq - 11}$$

For LDO, if the power pass transistor is a PMOSFET, the gain polarity of $PSR_{OPAMP}T_P(s)$ and $PSR_{Powerstage}$ is opposite. Meanwhile $T_P(s)$ and $PSR_{Powerstage}$ have the similar AC gain (The polarity is opposite). If the variation on the output of opamp can follow the variation of VDD, then the output of opamp which is connected with the gate of power pass transistor can cancel the variation on the power supply to improve the PSR performance. So, the load current mirror of the opamp should be at PMOS side as shown Fig.9 CB2. Also, with a buffer stage, the power PMOSFET is biased by a PMOSFET diode connection.

A new technique is used to improve PSR of LDO. A feed-forward path is used to feed the voltage variation on VDD to the power PMOSFET gate to cancel the VGS variation as shown the following Fig.11 [5].

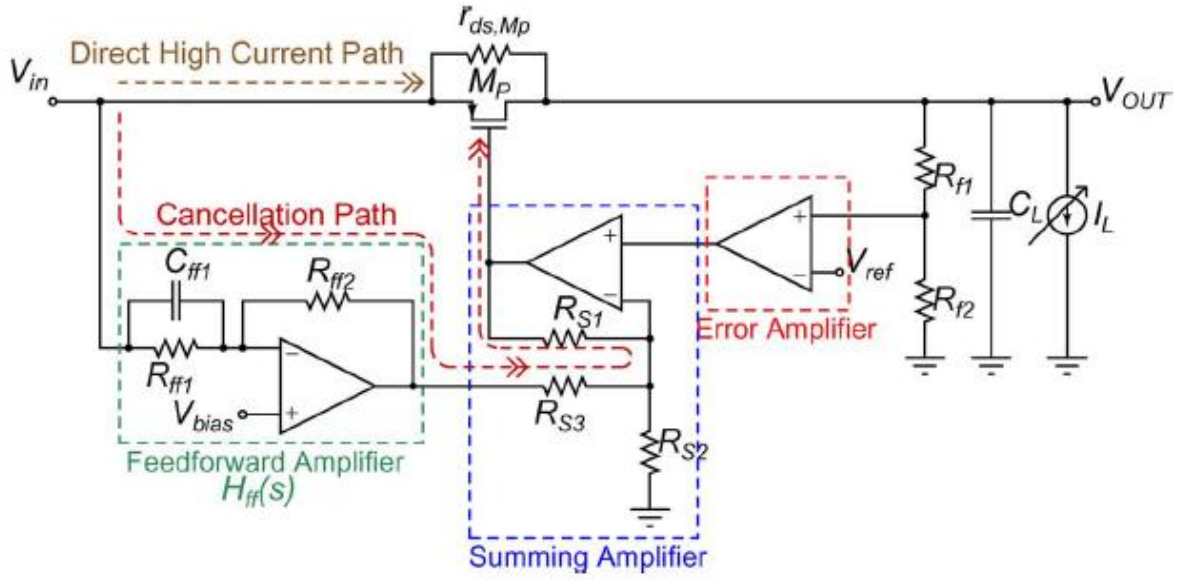


Fig. 15 Circuit diagram of LDO with feed-forward ripple cancellation

For the capless LDO with NMOSFET power pass transistor, the gain polarity of $PSR_{OPAMP}T_P(s)$ and $PSR_{Powerstage}$ is same. They cannot cancel each other. So, it requires that the opamp of the LDO with an NMOSFET power transistor has a better PSR performance than the PSR of LDO with PMOS power pass transistor. To realize a good PSR of opamp,. a cascade opamp like the followed is used to drive NMOSFET power transistor.

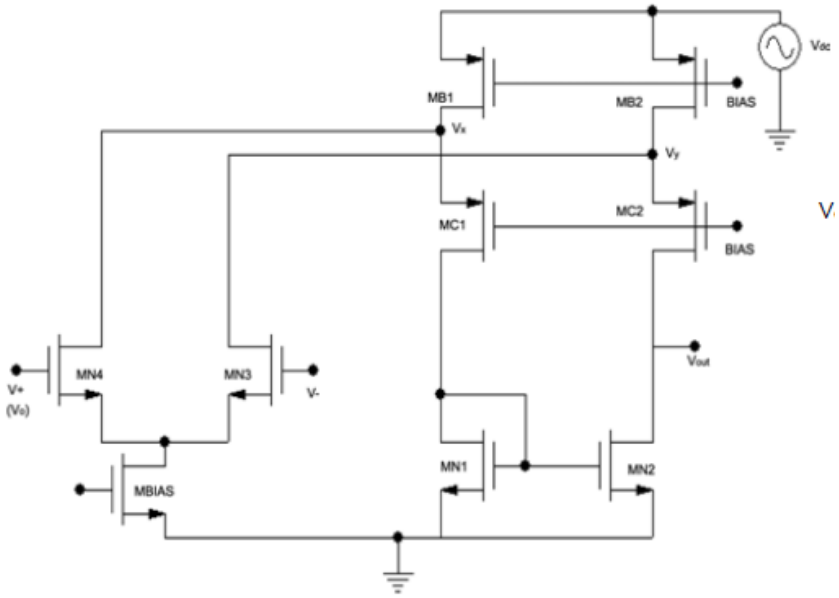


Fig. 16 Circuit diagram of the opamp for the capless LDO with NMOSFET

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