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Analytical comparison of frequency compensation techniques in three-stage amplifiers

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SUMMARY

In this paper, design equations of the most common Nested Miller topologies are derived. Moreover, a coherent and comprehensive analytical comparison among the different topologies is also presented. In particular, after deriving design equations, following the approach previously proposed by the authors that have the phase margin as the main design parameter, the different solutions are compared by evaluating a novel figure of merit that expresses a trade-off between gain-bandwidth product, load capacitance and total transconductance, for equal values of phase margin. It is shown that there is no unique optimal solution as this depends on the load condition and the relative magnitude of the transconductance of each stage. From this point of view, the proposed comparison also provides useful design guidelines for the optimization of small-signal performance. Simulations confirming the effectiveness of the comparison are also given. Copyright © 2006 John Wiley & Sons, Ltd.

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1. INTRODUCTION

In the analogue design domain, amplifiers with three stages are often encountered. We can find them in audio power amplifiers [1, 2], in integrated power amplifiers [3–5] (realized with two or more gain stages and a class AB output stage [5–8]), in integrated voltage regulators [9, 10], and recently also to implement low-voltage high-gain operational transconductance amplifiers (OTAs).

To stabilize the frequency and transient response of a three-stage amplifier, where the second stage is non-inverting and the last is inverting, the nested Miller compensation (NMC) topology can be used [1, 2, 10, 11]. This technique employs two compensation capacitors which exploit the Miller effect to split low-frequency poles and achieve the desired phase margin and transient

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response. However, this topology results in bandwidth reduction (gain bandwidth product (GBW) is one-quarter of that achievable by a single-stage amplifier [12]) and in high-power consumption.

Recently, many researchers have proposed different compensation topologies to overcome the inherent limits of NMC. Many of these topologies use a passive capacitive–resistive compensation network [13–17] and one or two additional transconductance stages to form feed-forward paths [18–21]. To improve both the GBW product and the slew rate, other solutions exploit only one Miller capacitor and a damping-factor control stage [22], an active-feedback stage [23, 24] or an AC boosting amplifier [25].

The performance achieved by some of the proposed topologies seems really interesting. Indeed, they are going to be applied even in contests where other compensation strategies are traditionally used, such as that of integrated voltage regulators [9, 10], where discrete components are used to provide circuit compensation.

It is worth noting that for many of the proposed topologies, a clear and defined design strategy which allows to dimension the compensation capacitances involved is not provided, and when it is given it is based on the proposed methodology in [12] which cannot allow the designer to arbitrarily set the phase margin. Indeed, the approach in [12] uses, as frequency response target of the amplifier in unity-gain configuration, a third-order Butterworth frequency response, which means to design the amplifier with a phase margin almost equal to 60°.

Moreover, up to now each compensation technique is usually compared to the others only using experimental data, while analytical comparison is carried out solely for the counterpart of NMC. This type of evaluation may lead to imprecise results, as it strongly depends upon the technology used to implement each amplifier as well as on the supply voltage and current consumption. And, from the designer's point of view, a comparison based only on the experimental results cannot indicate the real advantages of a particular compensation topology as it only allows a ranking based on the specific design conditions of different amplifiers.

Hence, an analytical comparison among the most common solutions presented in the literature is necessary. Indeed, only this type of evaluation can highlight the real benefits of a compensation network independently of the specific topology of the three gain stages, the transistor aspect ratio and the particular technology adopted to implement the amplifier. Moreover, an analytical comparison between different design solutions can help the designer to choose the compensation strategy which best satisfies a given set of design constraints.

This paper is organized as follows. In Section 2, design equations for the most common compensation topologies of three-stage amplifiers, with only the last stage inverting, are carried out.

In particular, the design methodology proposed by authors in [13, 16], which allows to arbitrarily set the amplifier phase margin, has been applied for each topology, thus achieving for each topology analytical design equations to size the network compensation capacitances. Moreover, the initial assumptions, transfer functions, stability criteria and design factors are also given. In Section 3 a figure of merit that weights the trade-off between gain-bandwidth product, load capacitance and the sum of all the transconductances, including those from the compensation network requiring additional bias current, is introduced and discussed. In Section 4 the small-signal performance for equal values of the phase margin is compared by analytically evaluating the figure of merit introduced. And the effectiveness of the proposed design methodology as well as the analytical figure of merit is confirmed by SPICE simulations. Finally, in Section 5, the conclusions are given.

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2. PROPOSED DESIGN METHODOLOGY

In this section a design strategy, first proposed by Palumbo and Pennisi [13, 16], is extended to 10 different compensation strategies. Figure 1 shows the block diagram of a three-stage amplifier and its equivalent small-signal model, where parameters g_{mi}, r_{oi} and C_{oi} represent the ith stage transconductance, resistance and equivalent output capacitance, respectively. Unless and otherwise stated, in the following the open-loop transfer functions of the topologies considered are carried out by neglecting the effect of the parasitic capacitances C_{oi} and output resistances r_{oi} and assuming for each stage a DC gain $A_{Vi} = g_{mi} r_{oi}$ which is much greater than one. These approximations hold for most amplifiers and allow us to develop a simpler transfer function while maintaining accuracy. The gain-bandwidth product of all the compensation techniques considered is equal to

$$\omega_{\mathrm{GBW}} = \frac{g_{m1}}{C_{C1}} \tag{1}$$

In addition, since in general the output stage significantly affects the performance of the whole amplifier in terms of power dissipation, linearity and bandwidth [26], we develop design equations by normalizing transconductances with respect to the transconductance of the last stage g_{m3}, thus introducing the variables

$$G_{Nm1} = \frac{g_{m1}}{g_{m3}} \tag{2}$$

$$G_{Nm2} = \frac{g_{m2}}{g_{m3}} \tag{3}$$

Design equations giving the values of the compensation network components are usually carried out by neglecting the effect of zeroes and assuming a Butterworth unity-feedback frequency response. However, by following this procedure, the designer cannot set the compensation network for the desired phase margin. To this end, we extend an alternative design strategy initially proposed

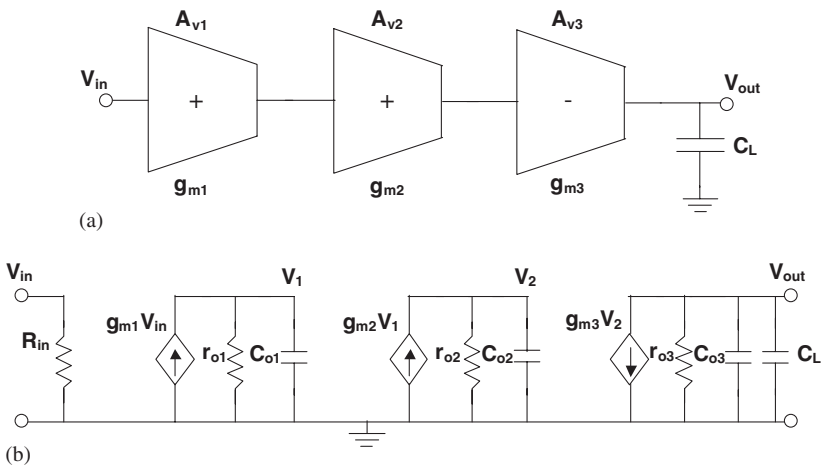

Figure 1. (a) Block diagram of a three-stage amplifier; and (b) equivalent small-signal model.

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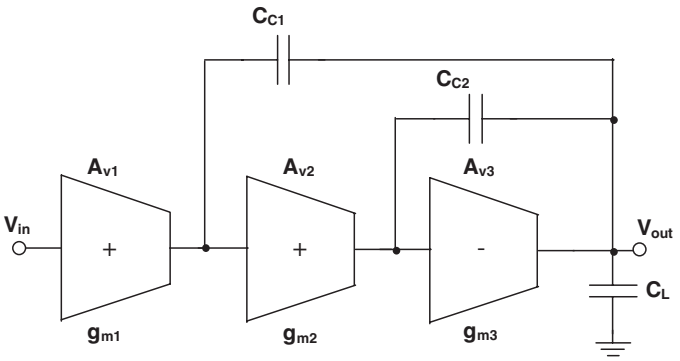

Figure 2. Block diagram of a three-stage NM compensated amplifier.

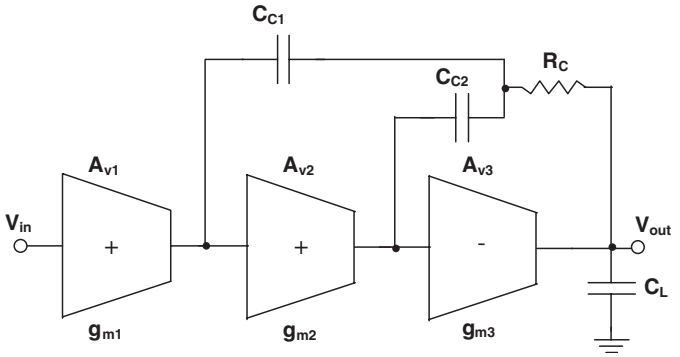

Figure 3. Block diagram of NMCNR [15].

by Palumbo and Pennisi [13, 16] for NMC and NMCNR (nested Miller compensation with nulling resistor), which introduces the phase margin as an additional design parameter, and apply it to all the compensation topologies studied.

2.1. Nested Miller compensation (NMC) and NMC with nulling resistor (NMCNR)

The high-level schematic of a three-stage NMC amplifier is shown in Figure 2. This topology has been extensively studied [12–14] assuming that $g_{m3} \gg g_{m2}$, g_{m1} with the purpose of neglecting the effect of the two zeroes (one left half plane (LHP) zero and one right half plane (RHP) zero located at a lower frequency) due to the feed-forward current through the two compensation capacitors. Nevertheless, in low-power CMOS design condition $g_{m3} \gg g_{m2}$, g_{m1}, which is equivalent to G_{Nm1}, $G_{Nm2} \ll 1$, is not easy to achieve and consequently, the design equations carried out can lead to wrong results. To cancel the RHP zero, while maintaining the LHP, which enhances phase margin, the NMCNR topology shown in Figure 3 was proposed [15].

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For the sake of conciseness we did not study the NMC core directly but derived it by setting $R_C = 0$ from the NMCNR topology shown in Figure 3. The transfer function of the equivalent small-signal circuit of the block diagram in Figure 3, evaluated under the assumptions introduced at the beginning of this section, is given by

$$A_{v\mathrm{NMCNR}}(s) = A_0 \frac{1 + s\left[R_C C_{C1} + \left(R_C - \frac{1}{g_{m3}}\right) C_{C2}\right] + s^2 \frac{g_{m3} R_C - 1}{g_{m3} g_{m2}} C_{C1} C_{C2}}{\left(1 + \frac{s}{\omega_{P1}}\right)\left[1 + s\left(\frac{1}{g_{m2}} - \frac{1}{g_{m3}}\right) C_{C2} + s^2 \frac{1 - g_{m2} R_C}{g_{m3} g_{m2}} C_{C2} C_L\right]} \tag{4}$$

where ω_{P1} is the dominant pole expressed by

$$\omega_{P1} \cong \frac{1}{r_{o1} C_{C1} g_{m2} r_{o2} g_{m3} r_{o3}} \tag{5}$$

and A_0 is the DC voltage gain given by

$$A_0 = -g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} \tag{6}$$

Equation (3) also includes two other (higher) poles and two zeroes.

Now let us develop the design conditions for C_{C1} and C_{C2} as a function of R_C. The second-order polynomial at the denominator of (4) is equal to the denominator of the open-loop gain of the second and third stages alone (which we also refer to as the *inner* amplifier) and can be rewritten as

$$D_{\mathrm{inner}} = 1 + \frac{s}{\omega_{\mathrm{GBW}i}} + \frac{s^2}{\omega_{\mathrm{GBW}i}^2 K_i} \tag{7}$$

where $\omega_{\mathrm{GBW}i}$ is the gain-bandwidth product (almost equal to the transition frequency) of the inner amplifier, given by

$$\omega_{\mathrm{GBW}i} = \frac{g_{m2}}{(1 - G_{Nm2}) C_{C2}} \tag{8}$$

and K_i is the ratio between the inner amplifier second pole and $\omega_{\mathrm{GBW}i}$, called separation factor (which is almost equal to the tangent of the phase margin of the inner amplifier [13]). To avoid overshoot in the inner amplifier frequency response module, a proper value of the separation factor K_i must be set. In particular, assuming $K_i = 2$ (which is the minimum value guaranteeing a monotonic module frequency response and corresponding to a phase margin of about 64°)[‡] and comparing the coefficients of Equation (7) with those of a second-order polynomial at the denominator of Equation (4), after some algebra we get

$$C_{C2} = 2 \frac{g_{m2} g_{m3} (1 - g_{m2} R_C)}{(g_{m3} - g_{m2})^2} C_L \tag{9}$$

[‡]This by representing the denominator of the inner amplifier, using pole frequency ω_n and damping factor ξ, $D_{\mathrm{inner}} = 1 + (2\xi/\omega_n)s + (1/\omega_n^2)s^2$. Such a condition is achieved by setting $\xi = 1/\sqrt{2}$.

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Now let us introduce phase margin Φ as design parameter of the global amplifier. Neglecting, for the moment, the effect of the zeroes, the following relation holds:

$$\tan\Phi = \tan\left(90^\circ - \tan^{-1}\frac{\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i}}{1-\frac{1}{2}(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2}\right) = \frac{1-\frac{1}{2}(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2}{\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i}} \tag{10}$$

where ω_{GBW} is the unity-gain frequency of the global amplifier expressed by Equation (1). Solving Equation (10) using Equations (1), (8) and (9) we get the expression of C_{C1}

$$C_{C1} = \left[\tan\Phi + \sqrt{\tan^2\Phi + 2}\right]\frac{g_{m1}(1-g_{m2}R_C)}{(g_{m3}-g_{m2})}C_L \tag{11}$$

Now, setting $R_C = 0$, we obtain the design equations for NMC topology

$$C_{C1} = \left[\tan\Phi + \sqrt{\tan^2\Phi + 2}\right]\frac{G_{Nm1}}{1-G_{Nm2}}C_L \tag{12a}$$

$$C_{C2} = 2\frac{G_{Nm2}}{(1-G_{Nm2})^2}C_L \tag{12b}$$

and the constraint $G_{Nm2}<1$ is required to obtain LHP poles.

The above equations are valid if we neglect the effect of the zeroes on the phase margin (i.e. if condition $G_{Nm1}, G_{Nm2} \ll 1$ holds). It should be noted that this condition is mandatory if we want to achieve feasible values for the compensation capacitors. Indeed, to get values of C_{C2} smaller than C_L, constraint $G_{Nm2}<2-\sqrt{3}\cong 0.27$ must be satisfied. In the same way, to satisfy constraint $C_{C1}<C_L$ we set an upper limit on the value of G_{Nm1}, which can be found using Equation (12a) and is expressed by $G_{Nm1}<(1-G_{Nm2})/[\tan\Phi + \sqrt{\tan^2\Phi+2}]$.

In contrast, setting $R_C = 1/g_{m3}$ the s^2 term in the numerator of Equation (1) is set equal to zero, yielding only an LHP zero $\omega_z = g_{m3}/C_{C1}$ as proposed by Leung and Mok [20] and called NMCNR topology. Taking into account the LHP zero, the phase margin is given by

$$\begin{aligned}\tan\Phi &= \tan\left(90^\circ - \tan^{-1}\frac{\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i}}{1-\frac{1}{2}(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2} + \tan^{-1}\frac{\omega_{\mathrm{GBW}}}{\omega_Z}\right)\\ &= \frac{2\omega_{\mathrm{GBW}i}(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2 + \omega_Z(2-(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2)}{\frac{\omega_{\mathrm{GBW}}}{\omega_{\mathrm{GBW}i}}[\omega_{\mathrm{GBW}i}((\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2-2)+2\omega_Z]}\end{aligned} \tag{13}$$

or equivalently, introducing the angle Φ_B as the contribution of the zero to the phase margin

$$\tan(\Phi-\Phi_B) = \tan\left(90^\circ - \tan^{-1}\frac{\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i}}{1-\frac{1}{2}(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2}\right) = \frac{1-\frac{1}{2}(\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i})^2}{\omega_{\mathrm{GBW}}/\omega_{\mathrm{GBW}i}} \tag{14a}$$

where

$$\Phi_B = \tan^{-1}\left(\frac{\omega_{\mathrm{GBW}}}{\omega_Z}\right) = \tan^{-1}(G_{Nm1}) \tag{14b}$$

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It should be noted that Equation (14a) is formally similar to Equation (10). Thus, setting $R_C = 1/g_{m3}$ in Equations (11) and (9), we obtain the following design equations:

$$C_{C1} = \left[\tan(\Phi - \Phi_B) + \sqrt{\tan^2(\Phi - \Phi_B) + 2}\right] G_{Nm1} C_L \tag{15a}$$

$$C_{C2} = 2\frac{G_{Nm2}}{1 - G_{Nm2}} C_L \tag{15b}$$

Again, in order to get LHP poles and to have a zero at a frequency greater than the ω_{GBW}, we must guarantee constraints $G_{Nm2}<1$ and $G_{Nm1}<1$, respectively. However a value of G_{Nm1} and G_{Nm2} which is much lower than 1 must be chosen to obtain compensation capacitances lower than load capacitance. Indeed, from Equation (15a), neglecting the effect of zero, we get $G_{Nm1}<[\tan\Phi + \sqrt{\tan^2\Phi + 2}]^{-1}$, and from Equation (15b) we get $G_{Nm2}<\frac{1}{3}$.

2.2. *Double pole-zero cancellation (DPZC)*

Compared to NMCNR, the DPZC compensation topology, proposed by Palumbo and Pennisi [16] and Grasso *et al.* [17], exploits an additional resistor R_{C2} in the compensation network, as shown in Figure 4, with the aim of extending the bandwidth through a pole-zero cancellation. The transfer function of the small-signal equivalent circuit of Figure 4 is equal to

$$A_{v\mathrm{DPZC}}(s) = A_0 \frac{1 + s\left[R_C C_{C1} + \left(R_{C2} + R_C - \dfrac{1}{g_{m3}}\right) C_{C2}\right] + s^2 \dfrac{(1 + g_{m2} R_{C2}) g_{m3} R_C - 1}{g_{m2} g_{m3}} C_{C1} C_{C2}}{\left(1 + \dfrac{s}{\omega_{P1}}\right)\left[1 + s\left(R_{C2} + \dfrac{1}{g_{m2}} - \dfrac{1}{g_{m3}}\right) C_{C2} + s^2 \dfrac{1 - g_{m2} R_C}{g_{m2} g_{m3}} C_{C2} C_L\right]} \tag{16}$$

By inspection of Equation (16), it can be seen that the zeroes can both be made negative and their values can be adjusted to exactly cancel the two higher poles. By setting $R_C = 1/g_{m3}$ and equating

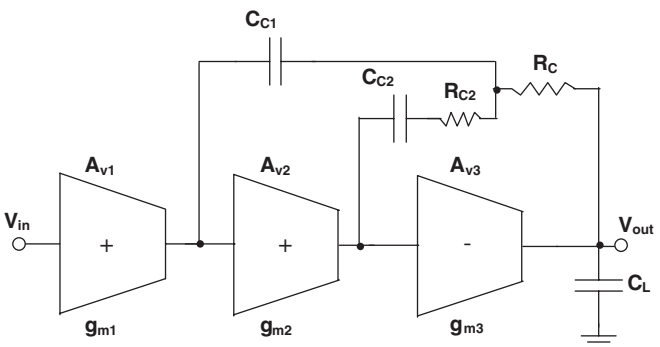

Figure 4. Block diagram of DPZC [16, 17].

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the coefficients of the second-order polynomials, we get

$$R_{C2} = \frac{C_L}{g_{m3} C_{C2}} \tag{17a}$$

$$C_{C1} = \frac{1 - G_{Nm2}}{G_{Nm2}} C_{C2} \tag{17b}$$

By substituting Equation (17a) in Equation (17b), we find that the transfer function frequency response of the amplifier is now a single-pole function. Setting the inner phase margin to over 64° yields $G_{Nm2} < \frac{1}{2}$. Under this condition, any value of C_{C2} lower than C_L ideally ensures that the inner amplifier is stable. In reality, the minimum value of C_{C2} is imposed by parasitic capacitances. Indeed, after pole-zero cancellation, a parasitic pole remains which is approximately expressed by $\omega_{\text{par}} = (g_{m3} - g_{m2})/C_{o2}$. Making the parasitic pole much higher than the gain-bandwidth product yields condition $C_{C2} \gg C_{o2}[G_{Nm1} G_{Nm2}/(1 - G_{Nm2})^2]$. From Equations (1) and (17b), it is clear that the lower the value of C_{C2} the better the gain-bandwidth product of the amplifier. Thus, this technique shows good performance for capacitive loads greater than 100 pF. In this case, as a rule of thumb we can set $C_{C2} = 0.05$–$0.1\ C_L$ in a first design step.

A final remark concerns the effects of process and temperature variations. These do not allow perfect pole-zero cancellation and two pole-zero doublets arise which could deteriorate the amplifier's stability, especially if the lower doublet appears to the left of the transition frequency. This drawback is common to all the pole-zero cancelling approaches and can be alleviated by using pole-zero tracking biasing schemes.

2.3. Multi-path nested Miller compensation (MNMC)

To improve the bandwidth of the basic NMC solution, MNMC exploits an additional feed-forward path, as shown in Figure 5. Assuming constraint $g_{m3} \gg g_{m1}, g_{m2}$, the transfer function is given by

$$A_{v\text{MNMC}}(s) = A_0 \frac{1 + s\dfrac{C_{C1} g_{mf1}}{g_{m1} g_{m2}}}{\left(1 + \dfrac{s}{\omega_{P1}}\right)\left(1 + s\dfrac{C_{C2}}{g_{m2}} + s^2 \dfrac{C_L C_{C2}}{g_{m2} g_{m3}}\right)} \tag{18}$$

Neglecting the high-frequency zeroes, MNMC introduces an additional LHP zero compared to the NMC solution. As proposed by Eschauzier and Huijsing [18], the multi-path LHP zero can be used to cancel out the second non-dominant pole of the amplifier, thus enhancing ω_{GBW}. The transfer function (18) can be rewritten as

$$A_{v\text{MNMC}}(s) \cong A_0 \frac{\left(1 + \dfrac{s}{\omega_Z}\right)}{\left(1 + \dfrac{s}{\omega_{P1}}\right)\left(1 + \dfrac{s}{\omega_{P2}}\right)\left(1 + \dfrac{s}{\omega_{P3}}\right)} \tag{19}$$

where $\omega_Z = g_{m1} g_{m2}/g_{mf1} C_{C1}$, $\omega_{P1} = g_{m1}/C_{C1}$, $\omega_{P2} = g_{m3}/2C_L(1 - \sqrt{1 - 4\alpha})$, $\omega_{P3} = (g_{m3}/2C_L)(1 + \sqrt{1 - 4\alpha})$, $\alpha = (g_{m2}/C_{C2}) C_L/g_{m3}$.

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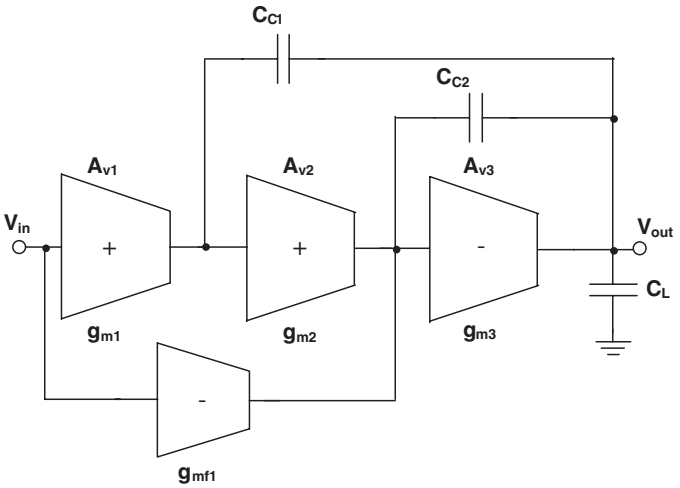

Figure 5. Block diagram of MNMC [18].

Setting $\omega_{P2} = \omega_Z$ and $\alpha = 0.1$ [14], so that the third pole moves at high frequency, we get

$$C_{C2} = 10 G_{Nm2} C_L \tag{20}$$

$$\tan \Phi = \tan\left(90^\circ - \tan^{-1} \frac{\omega_{\mathrm{GBW}}}{\omega_{P3}}\right) = \frac{\omega_{P3}}{\omega_{\mathrm{GBW}}} \tag{21}$$

$$C_{C1} = 2 \frac{\tan \Phi}{1 + \sqrt{0.6}} G_{Nm1} C_L \tag{22}$$

It is worth noting that the proposed compensation is effective only when $G_{Nm1}, G_{Nm2} \ll 1$ otherwise the expression of the feed-forward zero is different and, additionally, an RHP zero appears.

Compared to NMCNR, this technique enhances GBW, albeit at the expense of extra circuitry, increased power dissipation ($g_{mf1} = 4.54\ g_{m2}$ for $\Phi = 60^\circ$) and very high values of C_{C2}, which greatly affect slew rate and area occupation, especially when the capacitive load is high.

2.4. Nested G_m-C compensation (NGCC)

The NGCC solution [19] exploits two additional transconductance stages to implement the compensation network, as shown in Figure 6. Although this compensation strategy can be profitably extended to an N-stage amplifier, here we analyse only the three-stage case which represents a good compromise between DC gain, power dissipation and circuit complexity. The transfer function of a three-stage NGCC topology is given by

$$A_{v\mathrm{NGCC}}(s) = A_0 \frac{1 + s \dfrac{C_{C2}(g_{mf2} - g_{m2})}{g_{m2} g_{m3}} + s^2 \dfrac{C_{C1} C_{C2} (g_{mf1} - g_{m1})}{g_{m1} g_{m2} g_{m3}}}{\left(1 + \dfrac{s}{\omega_{P1}}\right)\left[1 + s \dfrac{C_{C2}(g_{mf2} - g_{m2} + g_{m3})}{g_{m2} g_{m3}} + s^2 \dfrac{C_L C_{C2}}{g_{m2} g_{m3}}\right]} \tag{23}$$

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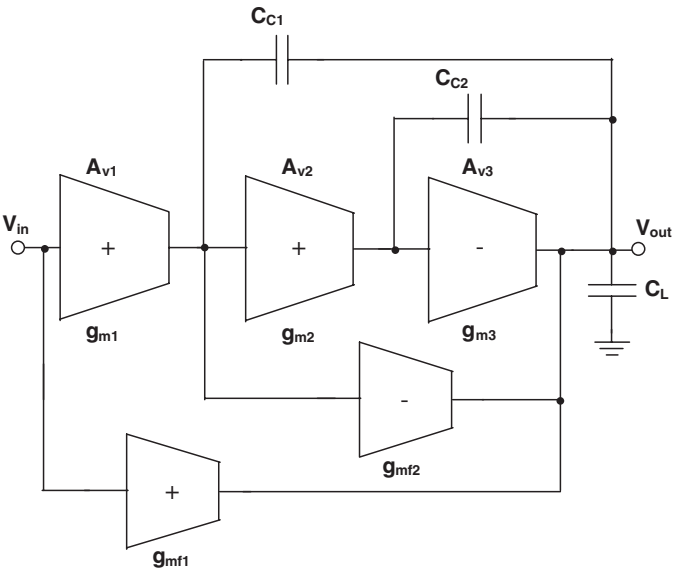

Figure 6. Block diagram of NGCC [19].

From the numerator of Equation (23), it can be seen that the zeroes can be easily eliminated by setting $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$. Thus, the phase margin is exactly expressed by Equation (10), where $\omega_{\mathrm{GBW}i} = g_{m2}/C_{C2}$. Following the same procedure shown in Section 2.1, we obtain the following design equations:

$$C_{C1} = \left[\tan\Phi + \sqrt{\tan^2\Phi + 2}\right] G_{Nm1} C_L \tag{24}$$

$$C_{C2} = 2G_{Nm2} C_L \tag{25}$$

Although condition $G_{Nm1}, G_{Nm2} \ll 1$ is not required to derive the above equations, to get practical values for C_{C1} and C_{C2}, i.e. values at least smaller than C_L, we must satisfy constraints $G_{Nm2} < \frac{1}{2}$ and $G_{Nm1} < [\tan\Phi + \sqrt{\tan^2\Phi + 2}]^{-1}$, respectively. It should be noted that the NGCC topology requires extra circuitry merely to implement g_{mf1}. Indeed, implementing the feed-forward transconductance g_{mf2} does not entail extra transistors, since it can be realized by simply changing the connection of the active-load transistor in the last stage. Moreover, given that the load is driven by a push–pull structure, the slew rate is only limited to internal nodes.

2.5. Nested Miller compensation feed-forward (NMCF) and NMCF with nulling resistor (NMCFNR)

Cancelling both the RHP and LHP zeroes from the transfer function of the basic NMC amplifier to obtain a stable amplifier as occurs in NGCC topology is unnecessary. Indeed, the LHP zero can be used to enhance phase margin, allowing, in turn, the use of smaller compensation capacitors to be used. To this aim, solutions NMCF [14] and NMCFNR [20, 21] were proposed. In particular, both exploit one feed-forward transconductance, with NMCFNR also using a compensation resistor,

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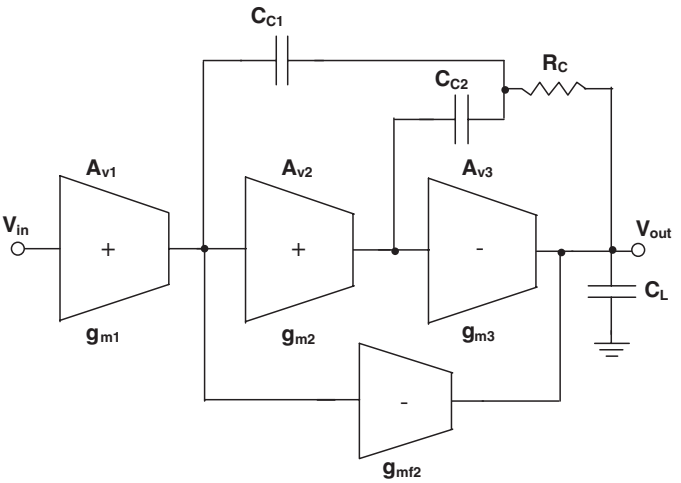

Figure 7. Block diagram of NMCFNR [21] and NMCF ($R_C = 0$) [20].

as shown in Figure 7. The transfer function of the small-signal equivalent circuit of Figure 6 is equal to

$$A_{v\mathrm{NMCFNR}}(s) = A_0 \frac{\left\{1+s\left[(C_{C1}+C_{C2})R_C+\dfrac{(g_{mf2}-g_{m2})}{g_{m2}g_{m3}}C_{C2}\right]+s^2\dfrac{(g_{mf2}+g_{m3})R_C-1}{g_{m2}g_{m3}}C_{C1}C_{C2}\right\}}{\left(1+\dfrac{s}{\omega_{P1}}\right)\left(1+s\dfrac{g_{m3}+g_{mf2}-g_{m2}}{g_{m2}g_{m3}}C_{C2}+s^2\dfrac{1-R_C g_{m2}}{g_{m2}g_{m3}}C_{C2}C_L\right)} \tag{26}$$

The feed-forward transconductance g_{mf2} can be set equal to g_{m3} to obtain a symmetrical push–pull output stage which enhances slew rate performance. Setting $R_C = 0$ we get NMCF topology. Following the same strategy as in the previous subsections and considering that the phase margin can again be expressed using Equation (14a), where $\omega_{\mathrm{GBW}i} = g_{m2}/(2 - G_{Nm2})C_{C2}$, we obtain the following design equations:

$$C_{C2} = \frac{2G_{Nm2}}{(2-G_{Nm2})^2}C_L \tag{27}$$

$$C_{C1} = \left[\tan(\Phi-\Phi_B)+\sqrt{\tan^2(\Phi-\Phi_B)+2}\right]\frac{G_{Nm1}}{2-G_{Nm2}}C_L \tag{28}$$

$$\Phi_B = \tan^{-1}\left(\frac{\omega_{\mathrm{GBW}}}{\omega_Z}\right) = \tan^{-1}\left(2\frac{1-G_{Nm2}}{(2-G_{Nm2})\left(\tan\Phi+\sqrt{\tan^2\Phi+2}\right)}\right) \tag{29}$$

The term Φ_B takes into account the effect of the lower frequency zero which is LHP. NMCF topology is characterized by two zeroes whose expression can be found by equating the

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numerator of Equation (26) to zero after setting $R_C = 0$. However, we can approximate the expression of the LHP zero to the reciprocal of the s term coefficient, if condition $g_{m2}g_{m3}/(g_{m3}-g_{m2})$ $C_{C2} \gg C_{C1}/(g_{m3}-g_{m2})$ is satisfied, since in this case the numerator of Equation (27) can be rewritten as

$$1 + s\frac{g_{m3} - g_{m2}}{g_{m2}g_{m3}}C_{C2} - s^2\frac{C_{C1}C_{C2}}{g_{m2}g_{m3}} \cong \left(1 + s\frac{g_{m3} - g_{m2}}{g_{m2}g_{m3}}C_{C2}\right)\left(1 - s\frac{C_{C1}}{g_{m3} - g_{m2}}\right) \tag{30}$$

Neglecting Φ_B, the above condition is verified with good approximation when $G_{Nm1} < 2(1 - G_{Nm2})^2/[(\tan\Phi + \sqrt{\tan^2\Phi + 2})(2 - G_{Nm2})]$, that is to say for all the values of G_{Nm1} and G_{Nm2} which in turn yield the values of the compensation capacitors smaller than C_L. Indeed, to satisfy conditions $C_{C2} < C_L$, $C_{C1} < C_L$, we must guarantee that $G_{Nm2} < 3 - \sqrt{5} \cong 0.76$ and, neglecting the effect of the zero, $G_{Nm2} < 2(2 - G_{Nm2})/(\tan\Phi + \sqrt{\tan^2\Phi + 2})$, respectively.

The NMCFNR topology is obtained by setting $g_{mf2} = g_{m3}$ and $R_C = \frac{1}{2}g_{m3}$. In this case, the s^2 term in the numerator of Equation (26) is set to zero and only the LHP zero $\omega_z = [C_{C1} + C_{C2}/2g_{m3} + (g_{m3} - g_{m2}/g_{m2}g_{m3})C_{C2}]^{-1}$ remains. Compared to NMCF, the compensation resistor R_C allows smaller compensation capacitors to be obtained. Indeed, using Equation (14a) with $\omega_{\mathrm{GBW}i} = g_{m2}/(2 - G_{Nm2})C_{C2}$ and following the same procedure, we get the following design equations:

$$C_{C1} = \left[\tan(\Phi - \Phi_B) + \sqrt{\tan^2(\Phi - \Phi_B) + 2}\right]\frac{G_{Nm1}}{2}C_L \tag{31}$$

$$C_{C2} = \frac{G_{Nm2}}{2 - G_{Nm2}}C_L \tag{32}$$

$$\Phi_B = \tan^{-1}\left(\frac{\omega_{\mathrm{GBW}}}{\omega_Z}\right) = \tan^{-1}\left(\frac{G_{Nm1}}{2} + \frac{1}{\tan\Phi + \sqrt{\tan^2\Phi + 2}}\right) \tag{33}$$

In order to satisfy conditions $C_{C2} < C_L$, $C_{C1} < C_L$, we must guarantee that $G_{Nm2} < 1$ and, neglecting Φ_B, $G_{Nm1} < 2/(\tan\Phi + \sqrt{\tan^2\Phi + 2})$, respectively.

2.6. Damping-factor control frequency compensation (DFCFC)

Since $\omega_{\mathrm{GBW}} = g_{m1}/C_{C1}$, and considering the expressions of C_{C1}, it can be seen that for all the compensation strategies analysed until now, ω_{GBW} is proportional to the ratio g_{m3}/C_L. Thus, high values of g_{m3} (i.e. high power consumption) are needed to increase bandwidth, especially when driving a large capacitive load. This characteristic is inherited from the nesting of the two compensation capacitors C_{C1} and C_{C2}. In particular, C_{C2} limits bandwidth since it is directly connected to the output. Including C_{C2}, however, is mandatory if we want to ensure a proper phase margin for the inner amplifier (i.e. a proper damping factor), avoiding undesired peaks in the frequency response of the amplifier.

As shown in Figure 8, DFCFC topology [22] only uses the compensation capacitor C_{C1} connected between two nodes in the direct path and introduces a damping-factor control stage involving C_{C2} to guarantee an appropriate phase margin for the inner amplifier. Setting for simplicity

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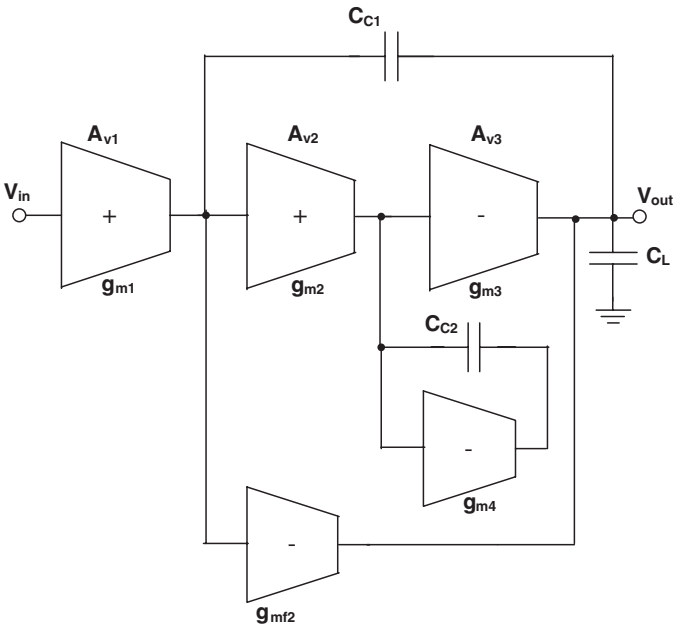

Figure 8. Block diagram of DFCFC [22].

$C_{C1} = C_{C2}$ and assuming that $g_{m4} r_{o4} > 1$ and C_{o1}, C_{o4} are smaller than C_{C1}, C_{o2} and C_L, respectively, the open-loop transfer function of the DFCFC topology is expressed by the three-pole and two-zero function

$$A_{v\mathrm{DFCFC}}(s) = A_0 \frac{1 + s\dfrac{C_{o2}g_{mf2} - C_{C1}g_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} - s^2\dfrac{C_{o2}C_{C1}}{g_{m2}g_{m3} + g_{mf2}g_{m4}}}{\left(1 + \dfrac{s}{\omega_{P1}}\right)\left(1 + s\dfrac{C_L g_{m4}}{g_{m2}g_{m3} + g_{mf2}g_{m4}} + s^2\dfrac{C_{o2}C_L}{g_{m2}g_{m3} + g_{mf2}g_{m4}}\right)} \tag{34}$$

Unlike previous compensation topologies where the poles are a function of C_{C2}, the non-dominant poles depend on the parasitic capacitance at the output of the second stage C_{o2}. Thus, the bandwidth is significantly extended. As for the other topologies employing the feed-forward stage g_{mf2}, we can set $g_{mf2} = g_{m3}$ so as to obtain a symmetrical push–pull output stage.

Imposing a phase margin of about 64° for the inner amplifier (i.e. damping factor of $1/\sqrt{2}$), we carry out the required value for g_{m4}

$$g_{m4} = c_{No2} g_{m3} \left(1 + \sqrt{1 + 2\frac{G_{Nm2}}{c_{No2}}}\right) \tag{35}$$

where

$$c_{No2} = \frac{C_{o2}}{C_L} \tag{36}$$

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Neglecting the effect of the zeroes, the phase margin can be derived from Equation (10), where $\omega_{\mathrm{GBW}i} = (g_{m2}g_{m3} + g_{mf2}g_{m4})/C_L g_{m4}$. Solving for C_{C1} using Equation (35) yields

$$C_{C1} = C_{C2} = \frac{c_{No2}\left(1+\sqrt{1+2G_{Nm2}/c_{No2}}\right)}{2\left[G_{Nm2}+c_{No2}\left(1+\sqrt{1+2G_{Nm2}/c_{No2}}\right)\right]}\left(\tan\Phi+\sqrt{\tan^2\Phi+2}\right)G_{Nm1}C_L \tag{37}$$

As stated in [14, 22], it is always possible to neglect the effect of the zeroes since they depend on C_{C1} and C_{o2}, while the non-dominant poles depend on C_L and C_{o2} and $C_{C1}<C_L$. It is worth noting that in this topology the value of the compensation capacitor is always much smaller than the load capacitance.

2.7. Active-feedback frequency compensation (AFFC)

AFFC [23, 24] eliminates capacitive nesting exploiting an active-capacitive-feedback network, as shown in Figure 9. As a result, only C_{C2} is directly connected to the output. Setting $C_{C1} = C_{C2}$ and assuming that $g_{m4}\,r_{o4} \gg 1$, and $C_{o1}, C_{o2} \ll C_{C1}, C_L$, the transfer function is given by

$$A_{v\mathrm{AFFC}}(s) = A_0 \frac{1 + s\dfrac{C_{C1}}{g_{m4}}}{\left(1+\dfrac{s}{\omega_{P1}}\right)\left(1+\dfrac{C_{o1}C_L}{C_{C1}(g_{mf2}-g_{m2})}s+\dfrac{C_{o1}C_L}{g_{m4}(g_{mf2}-g_{m2})}s^2\right)} \tag{38}$$

As in the previous subsections, g_{mf2} is set equal to g_{m3}. Setting a phase margin equal to 64° for the inner amplifier yields

$$g_{m4} = g_{m1}\left[\tan(\Phi-\Phi_B)+\sqrt{\tan^2(\Phi-\Phi_B)+2}\right] \tag{39}$$

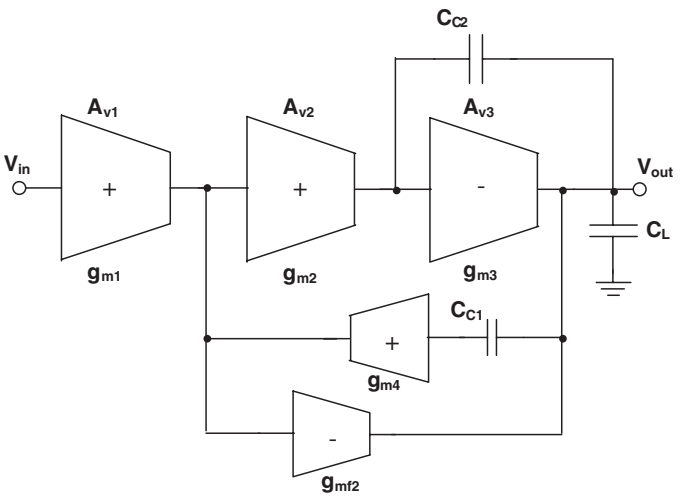

Figure 9. Block diagram of AFFC [23, 24].

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The phase margin of the global amplifier can be derived from Equation (14), where $\omega_{\mathrm{GBW}i} = C_{C1}(g_{m3} - g_{m2})/C_{o1}C_L$ and

$$\Phi_B = \tan^{-1}\frac{\omega_{\mathrm{GBW}}}{\omega_Z} = \tan^{-1}\left(\frac{1}{\tan\Phi + \sqrt{\tan^2\Phi + 2}}\right) \tag{40}$$

Solving for C_{C1}, using Equation (39), results in

$$C_{C1} = \sqrt{\frac{c_{No1}G_{Nm1}\left[\tan(\Phi - \Phi_B) + \sqrt{\tan^2(\Phi - \Phi_B) + 2}\right]}{2(1 - G_{Nm2})}}C_L \tag{41}$$

where

$$c_{No1} = \frac{C_{o1}}{C_L} \tag{42}$$

It is worth noting that the equation obtained includes the low-power strategy proposed by Leung and Mok [14], since setting $\Phi = 60°$ yields $g_{m4} \cong 2.78g_{m1}$ which is much lower than value $g_{m4} \cong 4g_{m1}$ that we obtain by applying the classical approach.

2.8. AC boosting compensation (ACBC)

As shown in Figure 10, ACBC strategy introduces an additional AC amplifier in parallel with the second stage to enhance high-frequency gain. Assuming $r_{o2} \gg r_{o4}$ and $C_{o1}, C_{o2} \ll C_{C1}$, C_L, an inherent pole-zero cancellation occurs [25] and the simplified small-signal transfer function can

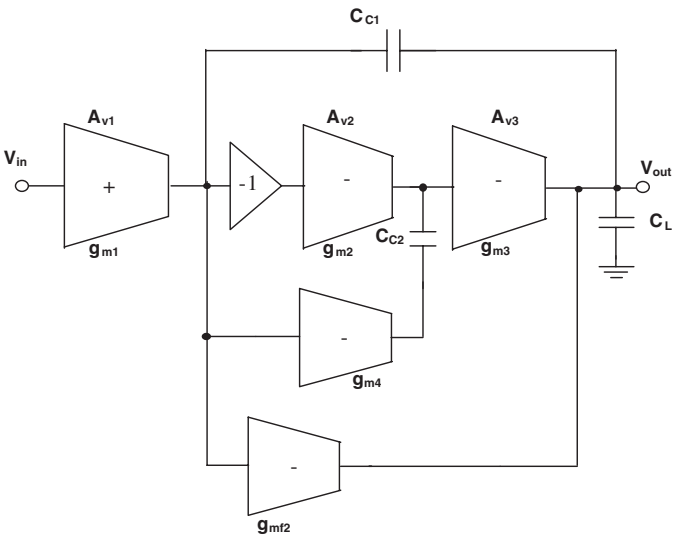

Figure 10. Block diagram of ACBC [25].

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be written as

$$A_{v\mathrm{ACBC}}(s) \approx A_0 \frac{1}{\left(1+\dfrac{s}{\omega_{P1}}\right)\left(1+\dfrac{C_L}{g_{m3}\left(A_{2h}+\dfrac{g_{mf2}}{g_{m3}}\right)}s\right)} \tag{43}$$

where

$$A_{2h} = (g_{m2} + g_{m4}) r_{o4} \tag{44}$$

To obtain a symmetrical push–pull output stage, g_{mf2} is set equal to g_{m3}. Since only one non-dominant pole can be considered, compensation is straightforward. Indeed, naming ω_{ND} as the non-dominant pole, we can write

$$\Phi = \tan^{-1} \frac{\omega_{\mathrm{ND}}}{\omega_{\mathrm{GBW}}} \tag{45}$$

and, given that $\omega_{\mathrm{GBW}} = g_{m1}/C_{C1}$,

$$C_{C1} = \tan\Phi \frac{G_{Nm1}}{A_{2h}+1} C_L \tag{46}$$

Compensation capacitor C_{C2} can be set equal to C_{C1} in a first design step, but can be smaller provided that it is greater than the parasitic capacitances.

As will be shown in the subsequent sections, ACBC is a very efficient compensation strategy. Indeed, the additional g_{m4} transconductance stage can be implemented using a simple transistor. Moreover, the A_{2h} factor can be easily controlled by using a diode-connected transistor [15].

3. THE FIGURE OF MERIT

Hitherto, the performance achieved by a new compensation technique has been analytically compared to the original NMC topology, while comparison of performance with the other approaches has usually been done using only experimental results, adopting two figures of merit suitable to evaluate the small-signal and large-signal performance of amplifiers.

In particular, in [22] to show the advantage of the proposed compensation network the two figures of merit below were used

$$\mathrm{FOM}_S = \frac{\omega_{\mathrm{GBW}} \cdot C_L}{\mathrm{Power}} \tag{47}$$

$$\mathrm{FOM}_L = \frac{\mathrm{SR} \cdot C_L}{\mathrm{Power}} \tag{48}$$

where SR is the slew rate and Power is the DC power consumption. The higher the value of Equations (47) and (48) the better the amplifier. These figures of merit, however, may lead to imprecise results because they depend upon the supply voltage. A more precise figure of merit,

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which used the total bias current, I_{dd}, in the denominator of Equations (47) and (48), was proposed by Peng and Sensen [25]

$$\text{IFOM}_S = \frac{\omega_{\text{GBW}} \cdot C_L}{I_{dd}} \tag{49}$$

$$\text{IFOM}_L = \frac{\text{SR} \cdot C_L}{I_{dd}} \tag{50}$$

To evaluate the amplifier efficiency, the figures of merit (49) and (50) are certainly much useful. Indeed, they allow to quantify the speed performance in the small and large signal domains, respectively, after a load condition and a total bias current (i.e. the power consumption assuming the power supply to be set) have been defined. Of course, the compensation network adopted in an amplifier affects its final speed performance, but it is not the only element to define that performance. Indeed, both the circuit topology of each single stage, which composes the amplifier and the fabrication technology, impacts the amplifier efficiency. As an example, consider that for a defined value of g_{m1} the use of a folded cascode topology requires twice the bias current needed by a differential pair with a current mirror active load topology.

Thus, unless the same amplifier topology and technology is used, a comparison of different compensation networks based on the above figures of merit from data obtained either experimentally or by simulation, cannot provide general information about the real benefits of a particular compensation technique, and only allows the considered amplifiers to be ranked as designed by the original authors.

To perform a general comparison among the many compensation approaches independently of their particular amplifier topology, design choices and technology, we introduce a novel figure of merit (FOM). It relates load capacitance, gain-bandwidth product and the total transconductance of the amplifier, g_{mT},

$$\text{FOM} = \frac{\omega_{\text{GBW}} \cdot C_L}{g_{mT}} \tag{51a}$$

Several considerations lead to define the figure of merit in Equation (51a). The transconductance is not only a key design parameter in the small-signal domain, but it is also strictly related to other significant design aspects such as power consumption and silicon area. Indeed, the transconductance shows the trade-off between transistor area and bias current. On the other hand, remembering that for a CMOS transistor operating in saturation $g_m = 2I_{\text{BIAS}}/V_{DSsat}$ and assuming an almost equal V_{DSsat} for the transistors of the amplifiers being analysed, the transconductance represents an assessment of power dissipation only. Moreover, perhaps the most relevant consideration is that the FOM can be analytically evaluated, starting from the design equations derived in the previous section, regardless of amplifier topology, technology and other design choices. For each compensation topology, we get a function whose independent variables are the phase margin and the transconductances of each stage (defined by design considerations which also include silicon area and power consumption). Thus, the comparison among the compensation topologies can be carried out through the behaviour of their FOMs. Moreover, for each compensation network, the FOM function gives information on the topology efficiency due to a variation of the transconductances distribution among the three stages.

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Table I. FOM expressions.

NMC	$\frac{(1-G_{Nm2})}{(G_{Nm1}+G_{Nm2}+1)(\tan\Phi+\sqrt{\tan^2\Phi+2})}$
NMCNR [15]	$\frac{1}{(G_{Nm1}+G_{Nm2}+1)(\tan(\Phi-\tan^{-1}G_{Nm1})+\sqrt{\tan^2(\Phi-\tan^{-1}G_{Nm1})+2})}$
DPZC [16, 17]	$\frac{G_{Nm2}G_{Nm1}}{(G_{Nm1}+G_{Nm2}+1)(1-G_{Nm2})}\frac{C_L}{C_{C2}}$
MNMC [18]	$\frac{1+\sqrt{0.6}}{2\tan\Phi(G_{Nm1}+G_{Nm2}\frac{1+\sqrt{0.6}}{\tan\Phi(1-\sqrt{0.6})}+1)}$
NGCC [19]	$\frac{1}{(G_{Nm1}+2G_{Nm2}+1)(\tan\Phi+\sqrt{\tan^2\Phi+2})}$
NMCF [20]	$\frac{(2-G_{Nm2})}{(G_{Nm1}+G_{Nm2}+1)\left(\tan\left(\Phi-\tan^{-1}\left(\frac{2(1-G_{Nm2})}{(2-G_{Nm2})(\tan\Phi+\sqrt{\tan^2\Phi+2})}\right)\right)+\sqrt{\tan^2\left(\Phi-\tan^{-1}\left(\frac{2(1-G_{Nm2})}{(2-G_{Nm2})\left(\tan\Phi+\sqrt{\tan^2\Phi+2}\right)}\right)\right)+2}\right)}$
NMCFNR [21]	$\frac{2}{(G_{Nm1}+G_{Nm2}+1)\left(\tan\left(\Phi-\tan^{-1}\left(\frac{G_{Nm1}}{2}+\frac{1}{\tan\Phi+\sqrt{\tan^2\Phi+2}}\right)\right)+\sqrt{\tan^2\left(\Phi-\tan^{-1}\left(\frac{G_{Nm1}}{2}+\frac{1}{\tan\Phi+\sqrt{\tan^2\Phi+2}}\right)\right)+2}\right)}$
DFCFC [22]	$\frac{2\left(G_{Nm2}+c_{N02}\left(1+\sqrt{1+\frac{G_{Nm2}}{c_{N02}}}\right)\right)}{c_{N02}\left(1+\sqrt{1+\frac{G_{Nm2}}{c_{N02}}}\right)\left(G_{Nm1}+G_{Nm2}+c_{N02}\left(1+\sqrt{1+\frac{G_{Nm2}}{c_{N02}}}\right)+1\right)(\tan\Phi+\sqrt{\tan^2\Phi+2})}$
AFFC [23, 24]	$\frac{\sqrt{2(1-G_{Nm2})G_{Nm1}}}{\sqrt{c_{No1}(\tan(\Phi-\Phi_B)+\sqrt{\tan^2(\Phi-\Phi_B)+2})}(G_{Nm1}(1+\tan(\Phi-\Phi_B)+\sqrt{\tan^2(\Phi-\Phi_B)+2})+G_{Nm2}+1)}$
	$\Phi_B=\tan^{-1}\left(\frac{1}{\tan\Phi+\sqrt{\tan^2\Phi+2}}\right)$
ACBC [25]	$\frac{1+A_{2h}}{\tan\Phi(G_{Nm1}+2G_{Nm2}+1)}$

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Exploiting Equation (51a) for a three-stage amplifier with a specific compensation network, we get

$$\mathrm{FOM} = \frac{\omega_{\mathrm{GBW}} \cdot C_L}{g_{m1} + g_{m2} + g_{m3} + g_{m\mathrm{COMP}}} = \frac{G_{Nm1}}{G_{Nm1} + G_{Nm2} + 1 + \dfrac{g_{m\mathrm{COMP}}}{g_{m3}}} \frac{C_L}{C_{C1}} \tag{51b}$$

where $g_{m\mathrm{COMP}}$ represents the sum of the compensation network transconductances, if any, which require additional bias current (i.e. more power dissipation) for their implementation.

The FOM (51) evaluated using the developed design equations *versus* the phase margin, Φ, and parameters, G_{Nm1}, G_{Nm2}, are summarized in Table I.

A fair comparison between different compensation techniques can now be achieved by assuming the same phase margin value. Note that this was almost impossible to obtain by following the traditional design equations based on a Butterworth response for the unity-gain closed-loop amplifier. Indeed, the resulting phase margin is substantially different from the expected value of 60° because the parasitic zeroes in the real transfer function are usually neglected.

Finally, it is worth noting that the proposed FOM represents the ratio between the gain-bandwidth product of the amplifier under consideration and the gain-bandwidth product of a pure single-stage amplifier under the same load and having transconductance equal to the total one of the three-stage amplifier.

4. ANALYTICAL COMPARISON

4.1. Analysis and discussion

Without loss of generality, we make the comparison assuming a phase margin equal to 70°, because this value allows us to optimize the 1% settling time [13, 27]. Nevertheless, almost the same results can be found for different phase margin values.

Let us start by analysing the compensation topologies whose FOM depends only on the phase margin, Φ, and parameters, G_{Nm1}, G_{Nm2}. Hence, we do not consider the topologies DFCFC, AFFC (whose FOM depends also on the ratio between parasitic capacitances and load capacitance, c_{No1} or c_{No2}) and ACBC (whose FOM depends also on A_{2h}). Moreover, we do not consider the DPZC for the moment, which is the only technique showing an inherent phase margin of 90°.

The FOM of NMC, NMCNR, NGCC, MNMC, NMCF and NMCFNR, are plotted in Figures 11–13 *versus* G_{Nm1}, for three typical values of G_{Nm2}. We see by inspection that the basic NMC always exhibits the lowest FOM. NGCC shows a FOM comparable to NMC for low values of G_{Nm2} (Figures 11 and 12) and is better than NMC only for higher values of G_{Nm2}. Indeed, as shown in Figure 13, for $G_{Nm2} = 0.5$ the FOM is about 1.5 times NMC, even though this requires compensation capacitor values comparable to C_L, as stated in Section 2.4. MNMC exhibits a FOM higher than NMCNR only for very low values of G_{Nm1} and G_{Nm2}. Finally, NMCFNR and NMCF topologies generally have the best FOM. In particular, NMCFNR is always the best choice, as the FOM is always 2–6 times higher than NMC. As regards NMCF, its FOM is always lower than NMCFNR, but higher than the other topologies (except for NMCNR so long as the condition $G_{Nm1} > -G_{Nm2} + 0.9$ can be met, which unfortunately yields compensation capacitances much higher than NMCF).

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From Figures 11–13 it can be seen that for all compensation strategies considered, the lower the value of G_{Nm2} the higher the FOM. Considering the dependence of FOM on G_{Nm1} we have different cases. The FOM increases reducing G_{Nm21} for topologies NMC, MNMC, NGCC and NMCF. For the NMCFNR topology, we observe a similar behaviour only for low values of

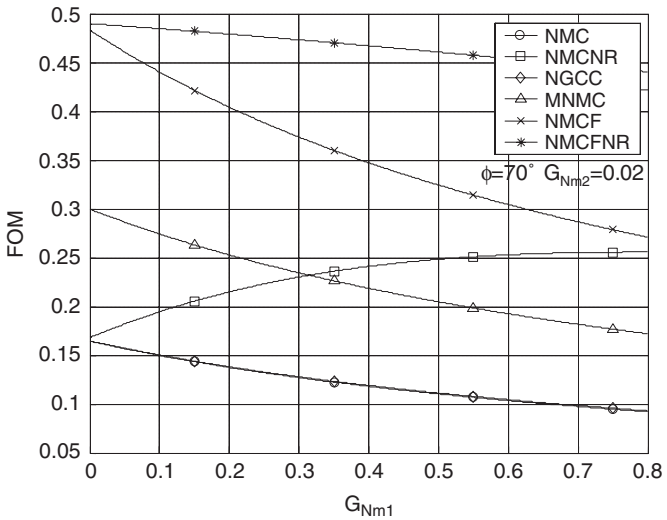

Figure 11. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.02$, $\phi = 70°$.

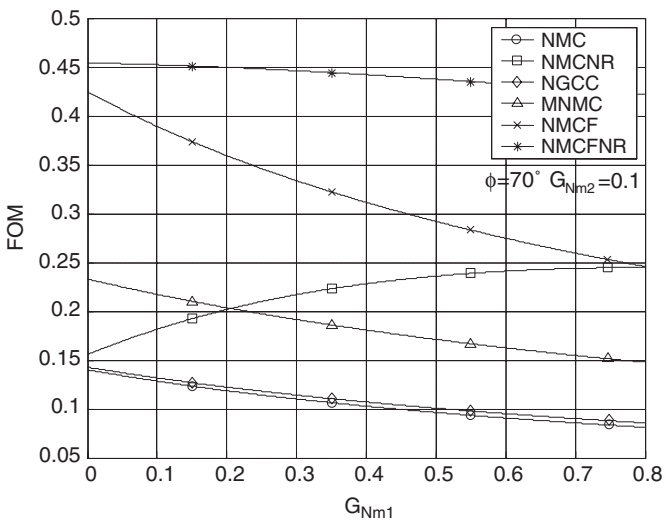

Figure 12. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.1$, $\phi = 70°$.

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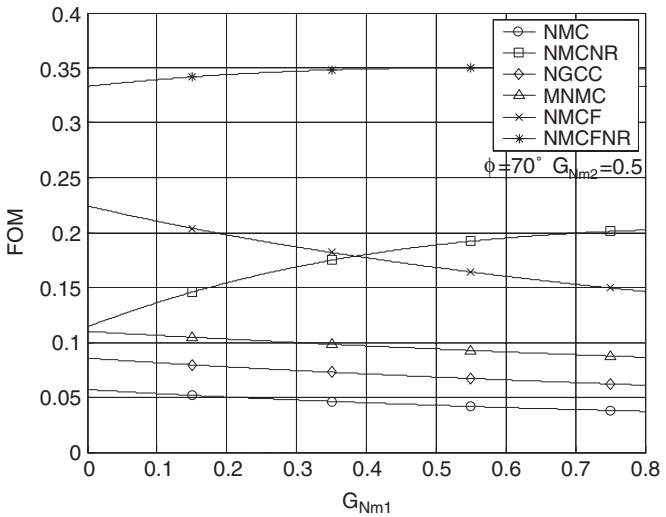

Figure 13. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.5$, $\phi = 70°$.

G_{Nm2}, whereas the FOM slightly increases increasing G_{Nm1} for value of G_{Nm2} approaching 0.5. Finally, in contrast with the previous cases, the FOM of NMCNR increases increasing G_{Nm1}.

Now, let us consider the DFCFC, AFFC and ACBC topologies which are the only structures whose FOM depends upon parasitic parameters c_{No1}, c_{No2} and A_{2h}. Their FOM are plotted against G_{Nm1} in Figures 14–16 for two values of c_{No1}, c_{No2} and A_{2h} and for three typical values of G_{Nm2}. In particular, we chose the value of 0.002 and 0.02 for c_{No1} and c_{No2}, which correspond approximately to a load capacitance ranging from 800 to 1 nF and from 80 to 100 pF, respectively. In order to compare DFCFC, AFFC and ACBC with the other previously analysed topologies, in the same figures we plot the FOM of NMCFNR, which has already appeared as the best solution. By inspection of Figures 14–16, it can be seen that for DFCFC and AFFC, the lower the value of c_{No1}, c_{No2} (i.e. the higher the value of load capacitance C_L) the higher the FOM. In particular, AFFC shows better performance than DFCFC, except for high values of G_{Nm2}, for which, as shown in Figure 16, DFCFC is the best choice. ACBC represents the best solution for low values of G_{Nm1}. For heavy capacitive loads and $G_{Nm1} > 0.1$, however, AFFC shows better performance.

It should be noted that for a given load capacitance C_L, parameters c_{No1} and c_{No2} cannot be set by the designer. In particular, for low/medium values of C_L (1–40 pF) DFCFC and AFFC always show a lower FOM than NMCFNR (even lower than NMCF and DFCFC), as shown in Figure 17 where the FOM is plotted for $c_{No1} = 0.1$. The FOM of ACBC, in contrast, does not depend upon C_L but on parameter A_{2h} whose value can be freely set by the designer to boost the GBW (see Equation (46)). Consequently, the FOM of ACBC is *always* much higher than that of NMCFNR, irrespective of the capacitive load. Thus, we can assert that ACBC is generally the best choice, while AFFC is a viable alternative only for heavy capacitive loads (>80–100 pF).

From Figures 14–16 it can be seen that for all compensation strategies except AFFC, the lower the value of G_{Nm2} the higher the FOM. For the topologies DFCFC and AFFC, the FOM also

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increases for higher load capacitance, which means a lower ratio between parasitic and load capacitances. For the ACBC it is advantageous to have a high value of A_{2h}. Moreover, for all compensation strategies except AFFC, the lower the value of G_{Nm1} the higher the FOM.

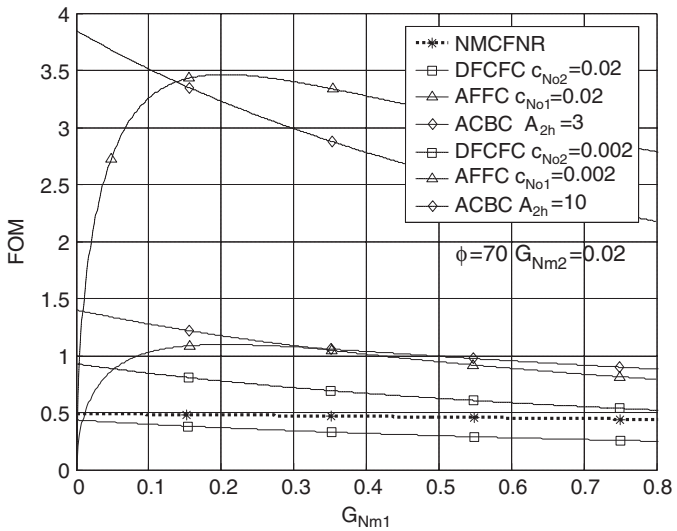

Figure 14. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.02$, $\phi = 70°$.

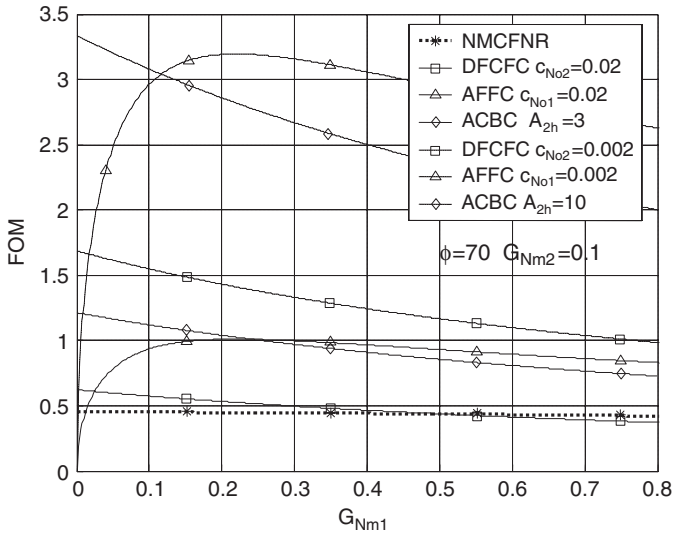

Figure 15. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.1$, $\phi = 70°$.

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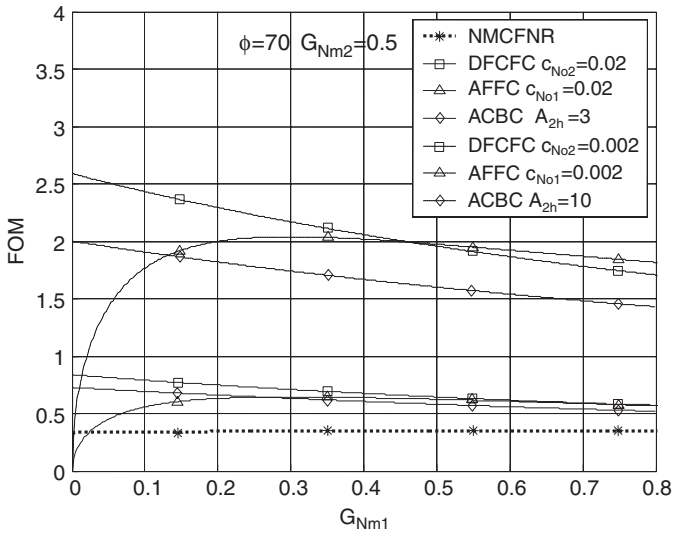

Figure 16. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.5$, $\phi = 70°$.

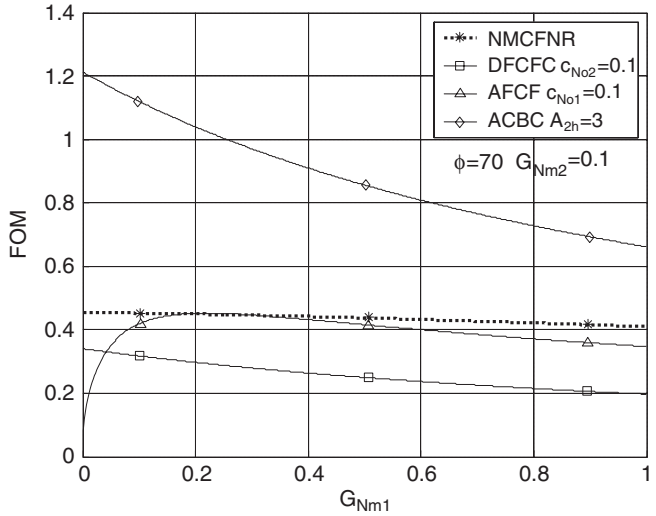

Figure 17. FOM *versus* normalized transconductance G_{Nm1} for $G_{Nm2} = 0.1$, $\phi = 70°$.

For AFFC, in contrast, there is a maximum value for the FOM. In particular, for a given value of G_{Nm2}, the optimum value $G_{Nm1,\text{opt}}$ can be found by setting the derivative of the FOM to zero with respect to G_{Nm1}. Although an analytical expression can be found, this equation is still too complex for hand calculations, but it can be approximated with an error lower than 5% for

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Φ ranging from 55 to 75° by

$$G_{Nm1,\text{opt}} = \frac{1}{50}[(-3\tan\Phi + 18)G_{Nm2} - 3\tan\Phi + 18] \tag{52}$$

Now, let us consider DPZC. By inspection of Table I it can be seen that the FOM of this compensation technique is proportional to G_{Nm2} and ratio C_L/C_{C2}. In particular, for a capacitive load of 100 pF and $C_{C2} = 0.05C_L$, the value of the FOM can be 2–3 times higher than the other previously analysed solutions for values of G_{Nm2} that range from 0.3 to 0.4, even though the phase margin is equal to 90°. For heavy capacitive loads (>500 pF), DPZC outperforms the other solutions [17], since its FOM can be as high as 7 for $G_{Nm2} = 0.3$, $G_{Nm1} = 0.4$ and $C_{C2}/C_L = 0.02$.

Finally, it is worth noting that, in contrast to the common knowledge, the adoption of the compensation topologies DPZC, DFCF, AFFC and ACBC, under some specific conditions, can lead to a three-stage amplifier with gain-bandwidth product higher than that of a single-stage amplifier having the same total transconductance (in other words the FOM is higher than 1).

4.2. Simulation results

To further confirm the obtained results, the three-stage amplifier whose schematic is shown in Figure 18 was compensated using the compensation networks illustrated in Figure 19 and was simulated with SPICE, adopting a 0.35-μm technology and a 2-V supply voltage. As already stated in the previous sections, the feed-forward transconductance stage g_{mf2} (in NGCC, NMCF, NMCFNR, DFCFC, AFFC and ACBC) can be implemented simply by connecting the gate of M13 to V_{out1}. It is worth noting that the schematics in Figure 19 are simplified. In particular, to properly bias the transistors of the compensation networks of DFCFC and AFFC and avoid DC offsets, an appropriate bias circuit should be used, as shown in [22, 23]. We designed all the amplifiers for a phase margin of 70° and a load capacitance of 100 pF, setting $g_{m1} = 112$ μA/V, $g_{m2} = 86.2$ μA/V, and $g_{m3} = 853$ μA/V, corresponding to $G_{Nm1} = 0.13$ and $G_{Nm2} = 0.1$. Moreover, for ACBC, parameter A_{2h} was set equal to 3, while for DFCFC and AFFC a value of 0.02 was considered for both parameters c_{No1} and c_{No2}, while for DPZC C_{C2} was set equal

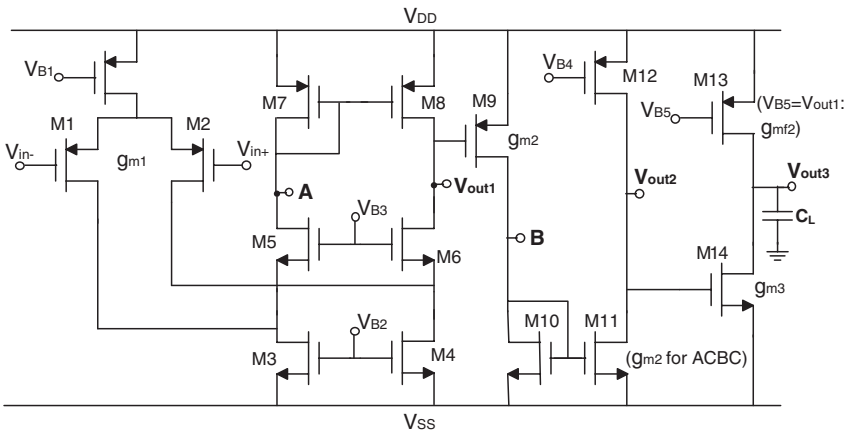

Figure 18. Schematic of the simulated three-stage amplifier.

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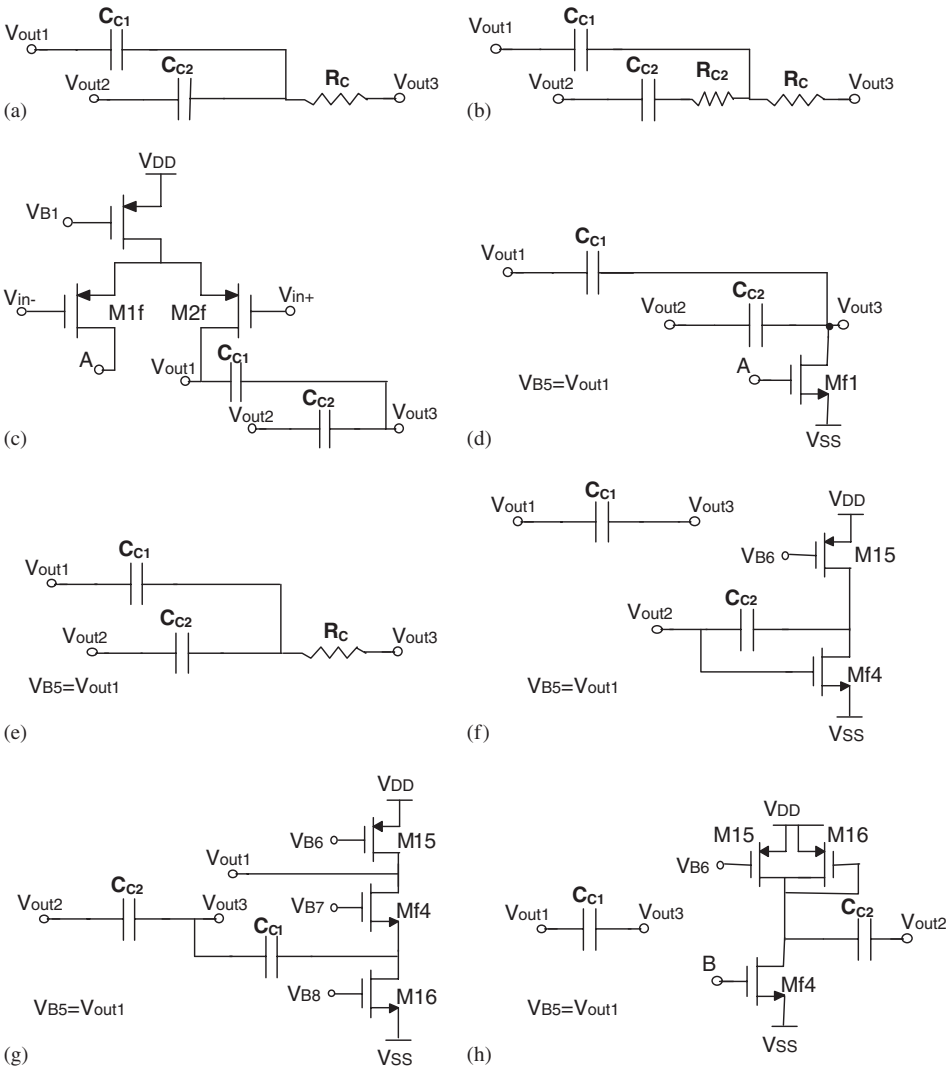

Figure 19. Schematics of the studied compensation networks: (a) NMC ($R_C = 0$) and NMCNR; (b) DPZC; (c) MNMC; (d) NGCC; (e) NMCF ($R_C = 0$) and NMCFNR; (f) DFCFC; (g) AFFC; and (h) ACBC.

to $0.05C_L$. The simulation results obtained are summarized in Table II and are found in good agreement with the design equations carried out in the previous sections, with the exception of the MNMC, given that condition $G_{Nm1}, G_{Nm2} \ll 1$, utilized for the calculations, was not met. Thus, as stated in Section 2.3, the expression of the feed-forward zero changes and RHP zero appears, causing a much lower phase margin than expected. After simulating MNMC with $G_{Nm1} = 0.02$ and $G_{Nm2} = 0.02$ (but with a power dissipation of about 1 mW), we obtained a phase margin of 67°, confirming that condition $G_{Nm1}, G_{Nm2} \ll 1$ is stringent and essential for this compensation strategy.

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Table II. Simulation results for $g_{m1} = 112\,\mu A/V$, $g_{m2} = 86.2\,\mu A/V$, $g_{m3} = 853\,\mu A/V$, $\Phi = 70°$ and $C_L = 100\,pF$.

	Phase margin (deg.)	GBW (MHz)	C_{C1}/C_{C2} (pF)	SR^+/SR^- (V/μs)	T_S^+/T_S^- 1% (μs)	CMRR (dB)/−3 dB (MHz)	PSRR (dB)/−3 dB (Hz)	Power (μW)	FOM	
									Analysis	Measure-ment
NMC	68.3	0.22	85/25	0.25/0.20	2.09/1.54	72/0.15	72/58	345	0.12	0.12
NMCNR	70.5	0.32	56/22	0.30/0.24	1.41/1.08	72/0.15	72/38	345	0.19	0.19
DPZC	90.5	0.40	44.5/5	0.39/0.36	1.28/1.26	72/0.16	72/73	345	0.24	0.24
MNMC	40	0.54	41/100	0.35/0.45	2.5/1.32	72/0.16	72/40	431	0.21	0.19
NGCC	69.1	0.25	76/20	0.33/0.24	1.94/1.44	72/0.11	71/45	365	0.13	0.13
NMCF	69.6	0.67	28/6	0.57/0.56	0.52/0.51	72/0.16	72/115	345	0.39	0.40
NMCFNR	72.1	0.80	23.4/5.3	0.63/0.62	0.45/0.44	72/0.15	72/140	345	0.45	0.48
DFCFC	66.6	0.96	17.5/17.5	0.8/0.75	0.34/0.35	72/0.14	72/184	372	0.56	0.54
AFFC	70.4	2.60	7.5/7.5	12/9	0.25/0.31	69/0.25	68/200k	424	0.98	1.12
ACBC	69.6	2.06	9/9	1.22/1.88	0.33/0.17	71/0.14	71/370	365	1.09	1.14

The value of compensation capacitors C_{C1} and C_{C2} is reported in the third column of Table II. It should be noted that for DFCFC, AFFC and ACBC we set C_{C2} equal to C_{C1}. Nevertheless, C_{C2} can be set even smaller without changing the phase margin, provided that it is higher than the parasitic capacitances.

To prove that DPZC can achieve better FOM than the other compensation strategies, we simulated the amplifier by setting $g_{m1} = 156\,\mu A/V$, $g_{m2} = 174\,\mu A/V$, and $g_{m3} = 512\,\mu A/V$ and $C_{C2} = 0.05C_L$; $C_L = 100$ pF. The measured FOM was 2.16 (1.91 from the analytical model) which by inspection of Figures 14–16 was about 2.5 higher than that of the other compensation techniques, for an equal capacitive load.

5. CONCLUSIONS

In this paper, a design methodology which, unlike traditional ones, also adds the phase margin as design parameter, was developed and applied to the most widely adopted compensation techniques for three-stage CMOS amplifiers with only last stage inverting. The design equations obtained were used to analytically compare the analysed solutions. In addition, we introduced a novel figure of merit which evaluated the trade-off between gain-bandwidth product, load capacitance and total transconductance, for equal values of phase margin. Although it was proved that there is no specific optimal strategy, the best compensation technique depends basically on the value of load capacitance. In particular, for low-medium capacitive loads (10–500 pF), ACBC provides the best FOM, whereas for heavy capacitive loads (>500 pF) DPZC achieves better performance. The DPZC technique also represents a good alternative to ACBC for loads around 100 pF. However, ACBC generally represents the best choice since its FOM does not depend upon load capacitance. In addition, it is characterized by relatively low circuit complexity. For all the compensation strategies, excepting AFFC, the higher the transconductance of the last stage the higher the FOM.

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For AFFC, in contrast, an optimal value of the ratio of the transconductance of the first stage to that of the last stage was found.

It is worth noting that, under some conditions, four of the analysed compensation techniques, namely DPZC, DFCF, AFFC and ACBC, may have a FOM higher than one. This means that the resulting three-stage amplifier has a frequency performance better than that of a single-stage amplifier with the same total transconductance.

SPICE simulations on a three-stage amplifier compensated by the analysed compensation techniques confirmed the validity of the design strategy as well as the analytical comparison proposed.

The proposed performance comparison was independent of the particular technology used, allowed a better understanding of the real benefits of a specific compensation strategy and gave further design guidelines. Indeed, the inspection of the FOM expressions can help the designer to choose the best values of the transconductances for optimizing an amplifier compensated with a given compensation technique.

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