A 950-MHz Rectifier Circuit for Sensor Network Tags With 10-m Distance

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***Abstract*—This paper presents a 950-MHz wireless power transmission system and a high-sensitivity rectifier circuit for ubiquitous sensor network tags. The wireless power transmission offers a battery-life-free sensor tag by recharging the output power of a base station into a secondary battery implemented with the tag. For realizing the system, a high-sensitivity rectifier with dynamic gate-drain biasing has been developed in a 0.3-μm CMOS process. The measurement results show that the proposed rectifier can recharge a 1.2-V secondary battery over −14-dBm input RF power at a power conversion efficiency of 1.2%. In the proposed wireless system, this sensitivity corresponds to 10-m distance communication at 4-W output power from a base station.**

***Index Terms*—Bias voltage distributor, effective threshold voltage, high-sensitivity rectifier, radio-frequency identification (RFID), wireless power transmission.**

I. Introduction

MANY sensor networks have been proposed to realize the vision of the ubiquitous computing society [1]–[3]. These networks require not only a small, simple, and low-cost RF terminal with sensing devices, but also a long-distance communication RF terminal in order to acquire diverse information. A communication distance of more than 10 m between the terminal and a base station is desired for indoor sensing network applications to minimize the number of base stations required in a room of an office or in a home [1]. In various kinds of radio systems, radio-frequency identification (RFID) tags are one of the most appropriate RF terminals for sensor networks from the point of view of small size, simplicity, and low cost.

RFID tags can be classified into the following three types: an active tag, a semi-passive tag, and a passive tag. The active tag has some external components such as a battery and a crystal, and transmits ID data of the tag using the battery. The active tag supports long-distance communication and can supply power to sensors. However, the active tag has several disadvantages such as finite battery life, large volume, and high cost.

In contrast, the passive tag can communicate to the base station without a battery by using transmitted power from a base station. In view of this mechanism, low-power operation is required for the passive tag. The passive tag communicates to the base station using a backscatter method, in which the antenna impedance of the tag is modulated according to the data bit stream. This method is suitable for low power consumption because it does not require large transmission power. However, the communication distance of a passive tag is generally about 1–5 m because the received power is not sufficient for activating the tag over a greater distance [4]. In addition, no sensors can be included in the passive tags. With a view to extending communication distance, many studies of passive tags have recently been reported [5], [6]. These papers used Schottky diodes in the rectifiers with a low forward voltage of 200 mV to communicate over long distances from small input RF signals. However, the forward voltage of 200 mV needs to be further reduced in order to increase the communication distance.

TABLE I
COMPARISON OF ACTIVE TAG, SEMI-PASSIVE TAG, AND PASSIVE TAG

	Active tag	Semi-passive tag	Passive tag
Communication distance	Long	Moderate	Short
Incorporation of sensor	Easy	Possible	Difficult
Necessity of Battery	Need	Need	No need
Cost	High	Moderate	Low

The semi-passive tag has a battery and communicates to the base station using a backscatter method. This means that the semi-passive tag has the merits of both the active tag and the passive tag. Table I shows a comparison of the tags. The communication distance of the semi-passive tag is over 10 m since it operates with the battery, and some sensors can be included. Although the semi-passive tag must have a battery, since other expensive components such as a crystal are unnecessary, the cost is not excessive. From the comparison of these tags shown in Table I, the performance of the semi-passive tag is the most appropriate for sensor networks. However, the drawbacks of the limited battery life need to be overcome.

Wireless power transmission that supplies power to a tag is one of the solutions to overcome the drawbacks of the limited battery life for the semi-passive tag. Studies of wireless power transmission, notably of high-power transmission such as solar power satellites, have been reported [7]. However, low-power transmission and rectification technologies required for a sensor network tag have not been considered.

This paper describes a 950-MHz high-sensitivity CMOS rectifier with a secondary battery for sensor network systems and a low-power wireless transmission system using the rectifier. In

Manuscript received April 18, 2005; revised July 25, 2005.

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Digital Object Identifier 10.1109/JSSC.2005.858620

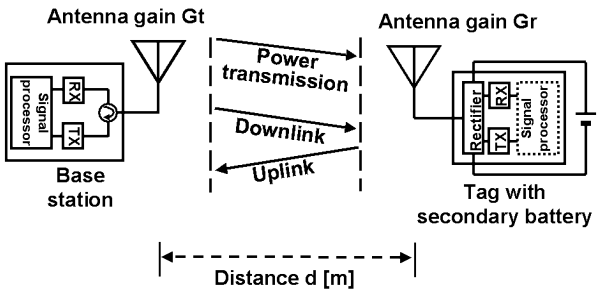

Fig. 1. Tag system including base station and tag with wireless power transmission.

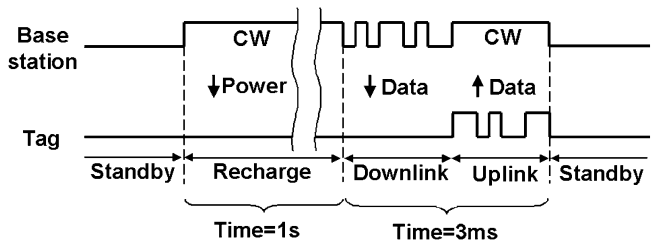

Fig. 2. Timing chart for the tag system considering the signal of base station and tag.

Section II, we propose the wireless power transmission system and estimate the required rectification efficiency to realize long-distance communication of over 10 m. In Section III, the design objectives of a rectifier in the RFID tag are specified and circuit design of the proposed high-sensitivity rectifier for long-distance wireless power transmission is described. IC fabrication is described in Section IV. Measured performance of the rectifier IC and measured results of wireless communication using the tag module are shown in Section V. Section VI summarizes the rectifier IC and the power transmission system with the rectifier.

II. Wireless Power Transmission System

Fig. 1 shows the proposed wireless power transmission system between a base station and a semi-passive tag with a secondary battery. In this system, the base station first transmits wireless power to the tag in order to charge the secondary battery with sufficient energy for data communication. After that, data communication, that is, downlink and uplink, is performed in the same manner as in the case of the conventional passive tag system.

The loss of RF power L is expressed by the Friis equation as follows [8]:

$$L\,[\mathrm{dB}] = 20\log\left(\frac{4\pi f d}{c}\right) - 10\log Gt - 10\log Gr \quad (1)$$

where the communication distance between the base station and the tag is d, frequency is f, antenna gains of the base station and the tag are Gt and Gr, respectively, and c is the speed of light. Assuming the RF frequency f is 950 MHz, the distance d is 10 m, and the antenna gain Gr of the tag is 2 dBi, the loss L is calculated to be 50 dB. When the effective isotropic radiated RF power of the base station is $4\mathrm{W}_{\mathrm{EIRP}}$, which is the maximum possible output power complying with U.S. and Japanese RFID regulations of the UHF band, the received power at the tag for 10-m distance is 40 μW.

Fig. 2 shows a timing chart of the tag system between the base station and the tag. A continuous wave (CW) from the base station activates the tag from standby mode and the power is transmitted from the base station to the tag during the power transmission time of one second. Next, data transmissions from the base station to the tag (downlink) and from the tag to the base station (uplink) are performed in 3 ms at a data rate of about 100 kb/s. In this period, the base station and the tag can communicate about 100 bits of data, that is, the amount of ID data of typical tags.

TABLE II
Specifications of the Tag System

Output power of base station	$4\mathrm{W}_{\mathrm{EIRP}}$ (36dBm)
Frequency	950MHz
Distance	10m
Antenna gain of base station	0dBi
Antenna gain of tag	2dBi
Power transmission time	1s
Data communication time	3ms (Up & Down link)
Data rate	100kb/s
Tag power consumption	< 0.1mW
Rectification efficiency	> 0.75%

In the power transmission period, the tag is supplied energy of over 40 μWs within the communication distance of 10 m. Assuming that the power consumption of the tag while transmitting data is 0.1 mW, which is a typical value for RFID tags, the energy consumed by the tag is 0.3 μWs. From the relationship between the supplied energy and the energy consumed, the rectification efficiency needs to be more than 0.75%. The specifications of the wireless transmission system are summarized in Table II.

III. Circuit Design

A. High-Sensitivity Rectifier Circuit

In RFID tag chips, generally there is a rectifier circuit to generate DC power from received RF power from a base station as shown in Fig. 1. The rectifier converts RF power to DC power when its rectified voltage surpasses the voltage of a secondary battery. Hence, the rectified voltage and input signal voltage are discussed in the following. Fig. 3 shows a conventional full-wave rectifier circuit composed of NMOS transistors connected in series [4]. The gate and drain terminals of the NMOS are directly connected. The relationship between an input signal voltage V_{rf} and an input RF power P_{rf} is expressed as follows:

$$V_{\mathrm{rf}} = \sqrt{P_{\mathrm{rf}}/\mathrm{Re}(Y_{\mathrm{in}})} \quad (2)$$

where Y_{in} is the input admittance of the rectifier. When the input RF signal $\mathrm{RF_{in}}$ is in its negative phase and $V_{\mathrm{rf}} > V_{\mathrm{th}}$, the transistor M_2 turns on and the current I_{M2} flows from ground to capacitor C_1, where V_{th} is threshold voltage of the NMOS transistor. In negative phase, the terminal A has the potential of $-V_{\mathrm{th}}$ and C_1 holds $V_{\mathrm{rf}} - V_{\mathrm{th}}$. In positive phase and $V_{\mathrm{rf}} > V_{\mathrm{th}}$, the transistor M_1 turns on and current I_{M1} flows from C_1 to C_2.

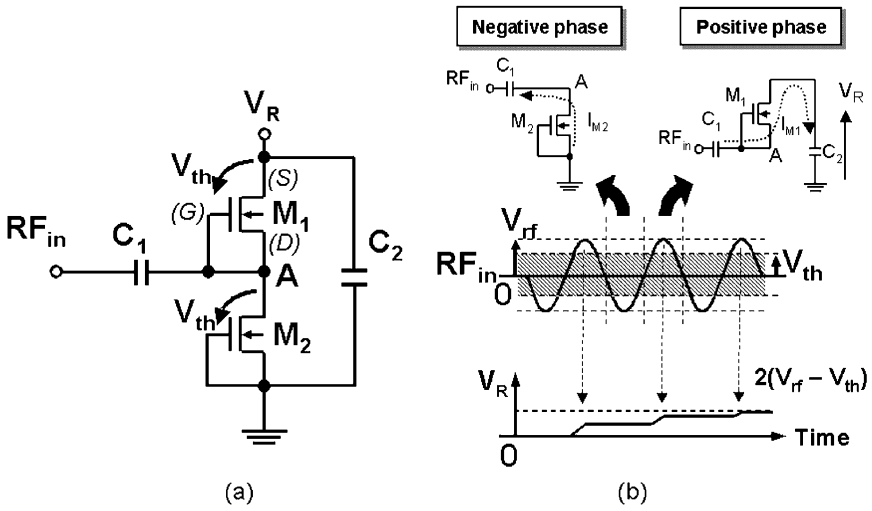

Fig. 3. (a) Conventional NMOS-type rectifier circuit and (b) illustration of the rectification mechanism.

Since the change of the RF signal voltage is $2V_{\rm rf}$ in one cycle, the potential of the terminal A rises to $2V_{\rm rf} - V_{\rm th}$, assuming that $C_1 >> C_2$. Considering $V_{\rm th}$ of $\rm M_1$, the rectification voltage V_R is

$$V_R = 2(V_{\rm rf} - V_{\rm th}). \tag{3}$$

From (3), the maximum of V_R is obtained when $V_{\rm th}$ is minimized, i.e., $V_{\rm th} = 0$. However, considering MOS transistors generally have $V_{\rm th}$ absolute variation of about ± 100 mV, the MOS rectifier using $V_{\rm th}$ below 100 mV is unsuitable because both $\rm M_1$ and $\rm M_2$ become on-state simultaneously and off-leak current occurs.

The unit cell of the proposed rectifier is shown in Fig. 4. A bias voltage $V_{\rm bth}$ is connected between the gate G and drain D terminals of each transistor. Since $V_{\rm th}$ is equivalently changed to $V_{\rm th} - V_{\rm bth}$, (3) is rewritten as follows:

$$V_R = 2(V_{\rm rf} - V_{\rm th} + V_{\rm bth}). \tag{4}$$

On the condition that $V_{\rm bth}$ is nearly equal to $V_{\rm th}$ and keeps $V_{\rm th} > V_{\rm bth}$, (4) can be approximated as

$$V_R \approx 2V_{\rm rf}. \tag{5}$$

Equation (5) indicates the input RF signal is converted to DC voltage without influence of $V_{\rm th}$. Since the drain–source voltage $V_{\rm DS}$ is always equal to gate–source voltage $V_{\rm GS}$ on the condition of (5), the transistors in the proposed rectifier are maintained in the saturation region. As illustrated in Fig. 4(b), the effective threshold voltage decreases from $V_{\rm th}$ to $V_{\rm th} - V_{\rm bth} \approx 0$ and the rectified voltage V_R generates a maximum voltage of $2V_{\rm rf}$. In view of these studies, the proposed rectifier is expected to be effective for small RF signals, and hence the tag using the rectifier is expected to be suitable for long-distance communication. The $V_{\rm bth}$ generator is discussed later.

B. Stacked Configuration of Unit Rectifier

For proper operation, the rectifier must output a voltage of at least 1.5 V to a secondary battery. To obtain this voltage from the small RF signal power of 40 μW, the units of the rectifier must be stacked [9]. Fig. 5 shows a simulation result of rectifier unit dependence of rectified voltage under the condition that a load of the rectifier is omitted. From Fig. 5, it is clear that the total rectifier voltage has a maximum value of 2.4 V at 6 units, whereas the input voltage $V_{\rm rf}$ is reduced with increasing rectifier units. When the rectifier has more than 6 units, increasing transistor parasitic losses reduce the total rectified voltage. Hence, the total rectified voltage is dependent on the number of the stacked cells. From the simulation results, we designed units consisting of 6-stacked rectifiers, that is, 12 transistors in series to obtain a supply voltage of at least 1.5 V under the condition of the finite load of the rectifier.

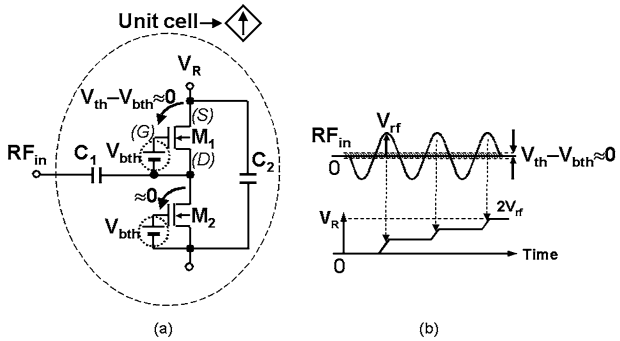

Fig. 4. (a) Unit cell of proposed NMOS-type rectifier and (b) illustration of the rectification state of the rectifier.

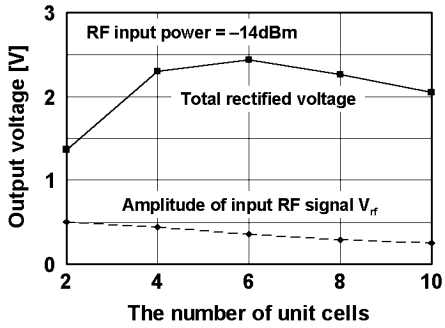

Fig. 5. Simulated results of the rectified voltage as a function of the number of unit cells of the rectifier.

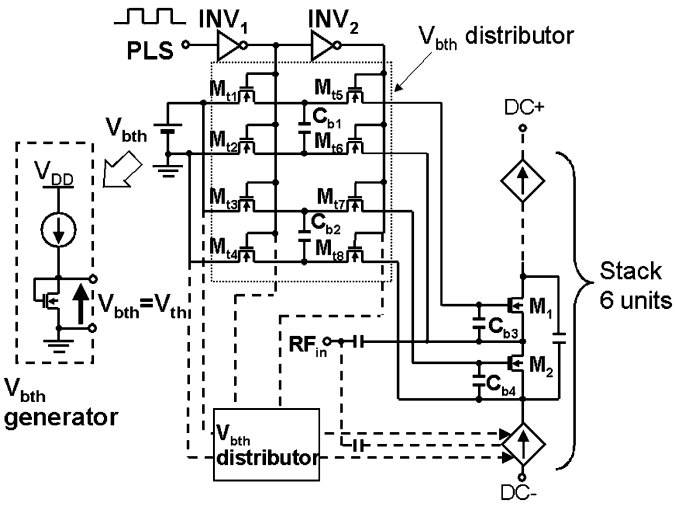

Fig. 6. Implementation of the proposed circuit with $V_{\rm bth}$ distributor.

Since the stacked transistors operate with different potential, $V_{\rm bth}$ needs to be supplied individually. Fig. 6 shows the implementation of the rectifier circuit with $V_{\rm bth}$ distributors, which can distribute a reference voltage of $V_{\rm bth}$ to each rectifier transistor. The distributor consists of two pairs of pass transistors ($\rm M_{t1}, M_{t2}$, and $\rm M_{t5}, M_{t6}$) for each rectifier transistor. The pass transistors are driven by a pulse signal (PLS) via inverter $\rm INV_1$ and $\rm INV_2$. When PLS is low, the voltage of $V_{\rm bth}$ is transferred to capacitor $C_{\rm b1}$ and $C_{\rm b2}$ through $\rm M_{t1}$–$\rm M_{t4}$. At that time, the potentials of rectification transistors are not affected because $\rm M_{t5}$–$\rm M_{t8}$ are in off-state. Next, when PLS is high, the voltages of $C_{\rm b1}$ and $C_{\rm b2}$ are transferred to $C_{\rm b3}$ and $C_{\rm b4}$, respectively, via $\rm M_{t5}$–$\rm M_{t8,}$ and the potentials of rectifier transistors are not affected from the voltage source of $V_{\rm bth}$ because $\rm M_{t1}$–$\rm M_{t4}$ are in off-state. In this way, gate–drain voltage of each rectifier MOS transistor maintains $V_{\rm bth}$ while these terminals have different potential. Capacitors $C_{\rm b1}, C_{\rm b2}, C_{\rm b3}$, and $C_{\rm b4}$ have capacitance of 1 pF to satisfy $C_{\rm b3} >> C_{\rm GSM1} + C_{\rm DBMt5} + C_{\rm b3p}$, where $C_{\rm GSM1}, C_{\rm DBMt5}$, and $C_{\rm b3p}$ are the gate–source capacitance of $\rm M_1$, the drain–body capacitance of $\rm M_{t5}$, and the parasitic capacitance of $C_{\rm b3}$, respectively. $C_{\rm GSM1}$ and $C_{\rm DBMt5}$ affect the performance of $C_{\rm b3}$ when $C_{\rm b3}$ is too small, while $C_{\rm b3}$ affects the chip area when $C_{\rm b3}$ is too large. By the trade-off between these conditions, the optimum capacitance of 1 pF is chosen. The capacitances of the other capacitors $C_{\rm b1}, C_{\rm b2}$, and $C_{\rm b4}$ are decided in the same manner as $C_{\rm b3}$.

Since the pass transistors $\rm M_{t5}$–$\rm M_{t8}$ have off-leakage current when they are in off-state, PLS switches $\rm INV_1$ and $\rm INV_2$ cyclically to compensate voltage drop due to the off-leakage current.

The reference voltage $V_{\rm bth}$ can be produced from a $V_{\rm th}$ generator with a reference NMOS transistor in the IC. Consequently, $V_{\rm bth}$ can be set to equal $V_{\rm th}$, irrespective of the absolute variation of $V_{\rm th}$ among the IC chips.

C. The Other Circuit

The entire rectifier IC shown in Fig. 7 comprises the 6-stacked units of the rectifier, TX circuit, and a passive filter for RX. The TX circuit is composed of a switch transistor and a resistor corresponding to a backscatter communication system.

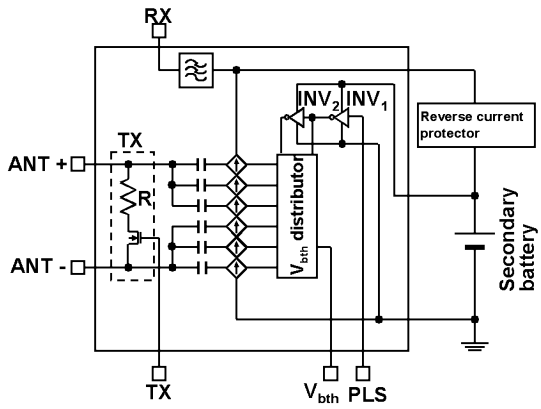

Fig. 7. Entire circuit with rectifier, TX circuit, and filter for RX.

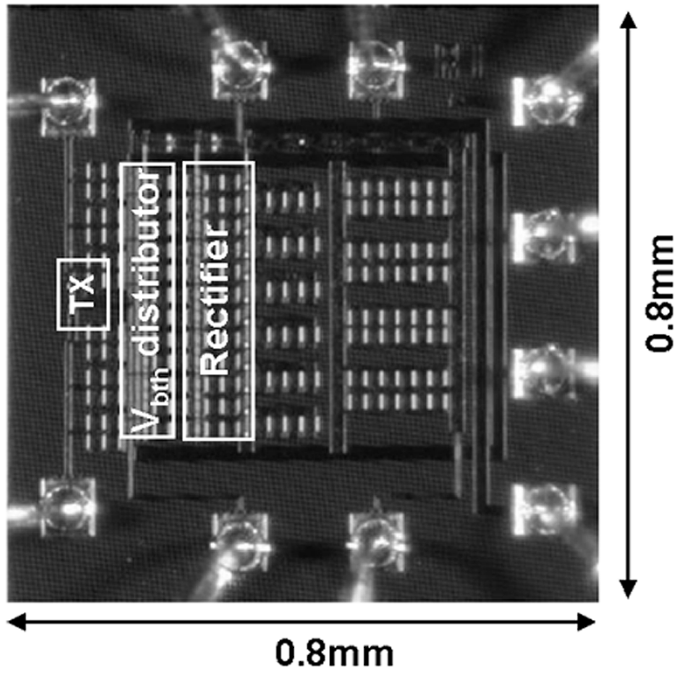

Fig. 8. Chip microphotograph.

RX signal components are detected from the envelope of the rectified signal. The rectified current recharges a secondary battery via a reverse current protection. The battery supplies the power supply voltage of $\rm INV_1$ and $\rm INV_2$.

IV. IC Fabrication

Fig. 8 shows the microphotograph of the IC fabricated in 0.3-μm gate length CMOS technology with 30 GHz f_T. The NMOS transistor with a triple-well structure is adopted for the rectifier and the back gate of the transistor is connected to the drain terminal of the transistor. Due to this structure, $V_{\rm th}$ is not influenced by DC voltage of the rectifier and the high-frequency characteristics of the rectifier are improved since parasitic capacitance is decreased. The gate width of each rectifier transistor is 10.4 μm. This size is chosen in view of the trade-off between producing the highest voltage and the largest current at -14 dBm input. The chip size is 0.8 mm $\times$ 0.8 mm. The actual chip area for the rectifier is less than a quarter of the chip

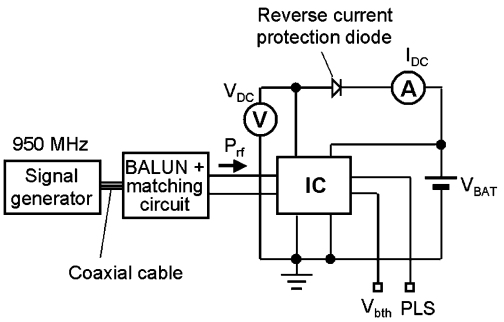

Fig. 9. Block diagram of recharge measurement setup.

area. The size of the rectifier block and $V_{\rm bth}$ distributor block are 0.16 mm $\times$ 0.4 mm and 0.1 mm $\times$ 0.4 mm, respectively.

V. Measurement Results

Fig. 9 shows the block diagram of the recharge measurement setup. In this setup, a 950-MHz RF signal is applied to the rectifier IC from an RF signal generator via a coaxial cable, a balanced-to-unbalanced transformer (BALUN) and matching networks. A commercially available 1.2-V secondary battery is used for the recharge measurement. RF input power $P_{\rm rf}$ is defined as the input power at the IC terminal. Output voltage $V_{\rm DC}$ and output current $I_{\rm DC}$ are measured at DC output terminal of the IC and DC output current from the IC, respectively. An external pulse generator and a DC voltage generator are used to supply PLS and $V_{\rm bth}$, respectively, in order to compare the performance of the proposed and the conventional rectifier. For the proposed circuit, the frequency of PLS is set to 100 Hz and $V_{\rm bth}$ is set to 0.53 V. For the conventional circuit, the frequency of PLS is set to 100 Hz and $V_{\rm bth}$ is set to 0 V. $V_{\rm th}$ of NMOS transistor for a wafer that is used for the rectifier IC is measured to be 0.529$\pm$0.025 V. From this result, it is clear that $V_{\rm bth}$ is set to almost the same value as $V_{\rm th}$.

Fig. 10 shows results of the recharge measurement. The output voltage of 1.5 V is obtained for the proposed circuit at $-$14-dBm RF power, whereas the voltage of the conventional rectifier does not reach 0.2 V. The proposed rectifier requires 10 dB less input power than the conventional circuit at the objective output voltage of 1.5 V. The output current is 0.4 μA at $-$14-dBm RF power. Above $-$15 dBm, the voltage of the proposed circuit exceeds the sum of the battery voltage and the forward voltage of the reverse current protection diode and the current of the proposed circuit outputs to the battery. The rectification efficiency for the proposed and the conventional circuits is shown in Fig. 11. The rectification efficiency E is defined as

$$E\,[\%] = \frac{V_{\rm BAT} \cdot I_{\rm DC}}{P_{\rm rf}} \cdot 100 \tag{6}$$

where $V_{\rm BAT}$ is the battery voltage of 1.2 V. The rectification efficiency of 1.2% is obtained at $-$14-dBm input power for the proposed circuit. The transistor gate width of 10.4 μm of the rectifier was designed to obtain high-rectified voltage at the input signal of $-$14 dBm. The measurement result indicates the gate width is suitable for the small power rectification since

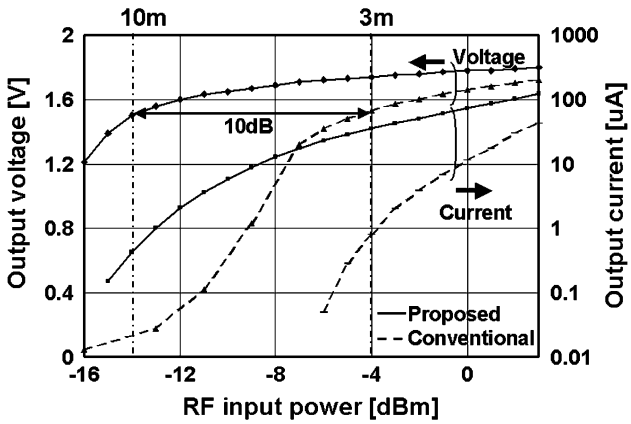

Fig. 10. Recharge characteristics of the proposed and the conventional circuits.

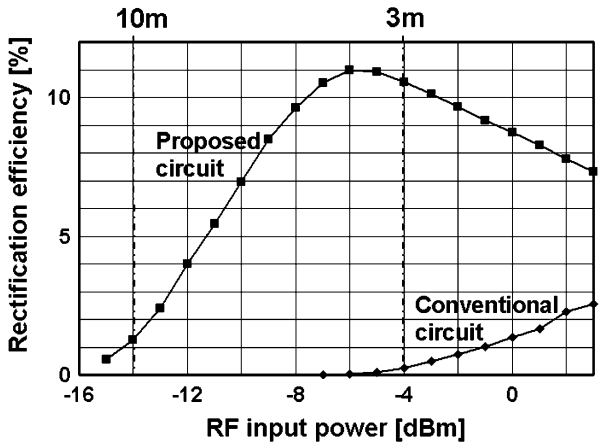

Fig. 11. Rectification efficiency of the proposed and the conventional circuits.

high-rectified voltage is obtained from the low input admittance as shown in (2). The maximum rectification efficiency of 11% is measured at RF input power of $-$6 dBm. Above the RF input power of $-$6 dBm, the efficiency decreases with increasing the RF input power. When large RF power is input, the large rectified current is generated. The power consumption of the rectifier transistors themselves and the reverse current protection diode increase with increasing rectified current, thereby reducing overall efficiency. The rectification efficiency of the conventional rectifier is below 3% in the measured RF input region. The characteristics of the proposed and conventional rectifier show that the bias voltage $V_{\rm bth}$ is especially effective for the rectification at low input power. In the evaluation, we ignore the power consumption of $V_{\rm bth}$ and PLS generators. When the power consumptions of the generators are taken into account, the rectification efficiency is reduced. The current consumption of the generators needs to be less than 0.15 μA to satisfy the specification that the efficiency be more than 0.75%.

Fig. 12 shows the $V_{\rm bth}$ dependence of the rectified current at $-$13-dBm input RF power. The rectified current increases with the bias voltage up to 0.53 V. Beyond 0.53 V, the rectified current rapidly decreases due to significant off-leakage of the rectifier.

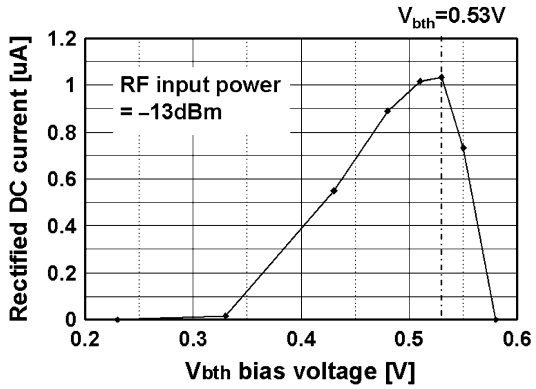

Fig. 12. $V_{\rm bth}$ dependence of rectified DC current.

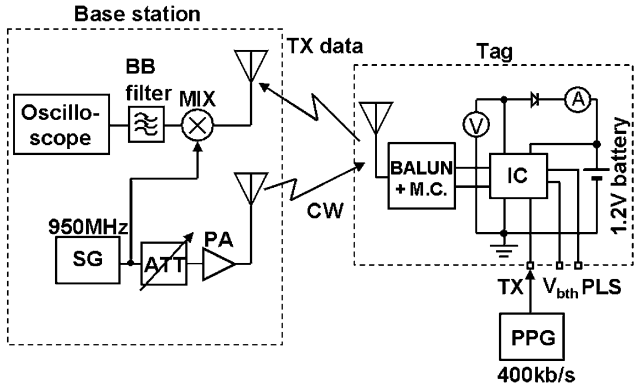

Fig. 13. Measurement setup of wireless data transmission.

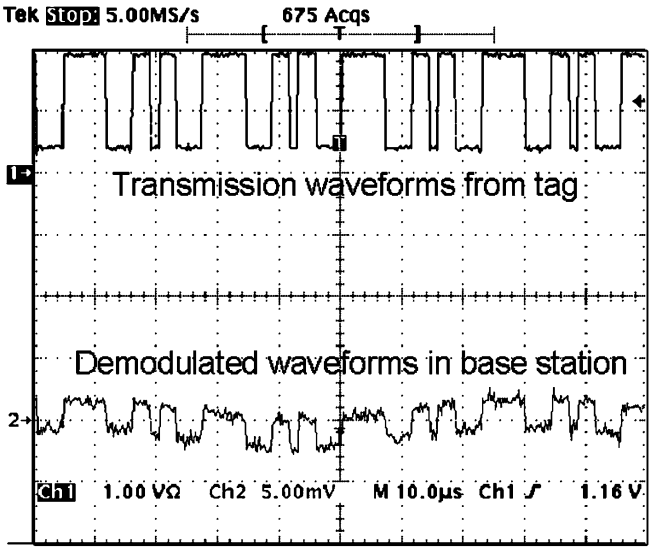

Fig. 14. Waveforms for transmitted and received data.

This result indicates that 0-V $V_{\rm th}$ transistor is unsuitable for rectifier, considering the absolute variation of $V_{\rm th}$ of 100 mV.

Fig. 13 shows the block diagrams for wireless data transmission measurement. The rectifier IC on the evaluation board is connected with an external dipole antenna. Transmission NRZ data of 400 kb/s generated by a pulse pattern generator is input from the TX terminal. A 950-MHz CW signal is used for backscattering communication and recharge. Received TX data is demodulated to a baseband signal by the 950-MHz CW signal. Fig. 14 shows measured transient waveforms for the 400-kb/s wireless data transmission. The upper waveforms are TX data of the tag and the lower ones are demodulated waveforms in the base station. The received waveforms are correctly demodulated at 2-m distances with CW power of 4 dBm. 1.5-V DC voltage is obtained at 2-m distances with CW power of 20 dBm. These results correspond to more than 10-m communication distance in the case that CW power is 4 $\rm W_{EIRP}$.

TABLE III
SUMMARY OF IC PERFORMANCE

IC size	0.8mm x 0.8mm
Input admittance	0.29mS + j1.4mS
PLS pulse frequency	100Hz
V_{bth} voltage	0.53V
Output DC voltage	1.5V @Pin = –14dBm
Output DC current	0.4µA @Pin = –14dBm
Sensitivity improvement	10dB @DC output voltage = 1.5V
Rectification efficiency	1.2% @Pin = –14dBm
Current consumption	0.2nA

Table III summarizes the performance of the IC. From recharge measurements, the IC achieved operation at −14-dBm input power corresponding to a 10-m communication distance.

VI. CONCLUSION

We have proposed a wireless power transmission tag system with a recharge period using a secondary battery for ubiquitous sensor networks. For realizing the system, a high-sensitivity rectifier circuit has been proposed in which a bias voltage almost equal to the threshold voltage is applied between the drain and gate terminals to enhance the sensitivity. A $V_{\rm bth}$ distributor has also been proposed to distribute the appropriate bias voltage from a single voltage source to each rectifier. The rectifier achieves a power conversion efficiency of 1.2% at an input RF power of −14 dBm, corresponding to a 10-m communication distance at 4-W output power from a base station. The measurement result meets the specification of the proposed system.

ACKNOWLEDGMENT

The authors would like to thank T. Iida for test chip fabrication. They are also grateful to K. Kawabata and H. Tsurumi for valuable discussion.

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