A 60GHz Power Amplifier with 14.5dBm saturation power and 25% peak PAE in CMOS 65nm SOI

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***Abstract*—A 60GHz wideband power amplifier (PA) is fabricated in standard CMOS SOI 65nm process. The PA is constituted by two cascode stages. Input, output and inter-stage matching use coplanar wave guide (CPW) transmission lines that have low losses thanks to the high resistivity SOI substrate. The PA measurements are carried out for supply voltages V_{DD} going from 1.2V to 2.6V and achieve a saturation power of 10dBm to 16.5dBm respectively. The peak power added efficiency is higher than 20% for all applied V_{DD} values.**

I. INTRODUCTION

Much effort has been carried out in order to develop millimeter wave circuits for wireless communication systems at the unlicensed 9GHz band around 60GHz. One of the most important elements in transceivers is the PA, which is crucial for the transmission range of a wireless link. Most PAs at 60 GHz are fabricated in III-V technologies or in BiCMOS bulk technology (bipolar SiGe) thanks to their high active performances. However, fabrication of millimeter-wave (mmW) PA in CMOS technologies remains attractive for integration with baseband, for high volume production and low cost reasons. Recently, numerous PAs in CMOS were reported at 60GHz, with output power up to 16dBm but power added efficiency (PAE) lower than 15% [1-6].

This paper describes the design of a power amplifier in the V-band that uses a CMOS 65nm SOI process. The main advantage of SOI CMOS technology versus classical bulk Si is the isolation between the substrate and active region. High resistivity SOI substrates inherently have lower dielectric attenuation for passive elements (transmission lines, inductors). Thanks to that, the 2-stages PA achieves 16dB gain and 14.5dBm output power with a peak PAE of 25%.

II. CMOS 65NM SOI TECHNOLOGY AND MM-W MODELS

The PA is fabricated in an industrial CMOS65nm SOI process provided by *STMicroelectronics*. The PA uses floating body transistors with 180GHz f_{max} and 150GHz f_t. The transistor model (BSIM3 SOI) that is provided in the design kit is not suited for mmW applications. For that reason, we used an empirical model which suited for high frequency circuit design and describes accurately the transistor's characteristics. The model is not described here, but details can be found in [7, 8].

The process uses a standard back-end that features six copper metal layers and an aluminum cap-layer on the top. The sixth metal layer is thicker than the lower ones. The CMOS65nm process is fabricated on a high resistivity substrate which is located underneath the buried-oxide (BOX). The high resistivity silicon substrate offers low dielectric losses. Therefore, the substrate does not need to be screened by a metal plane and CPW transmission lines are applicable.

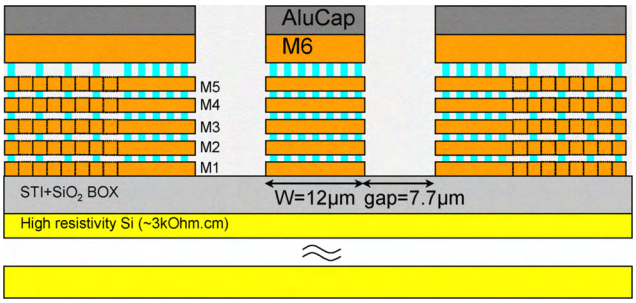

Figure 1. CPW transmission line cross section schematic.

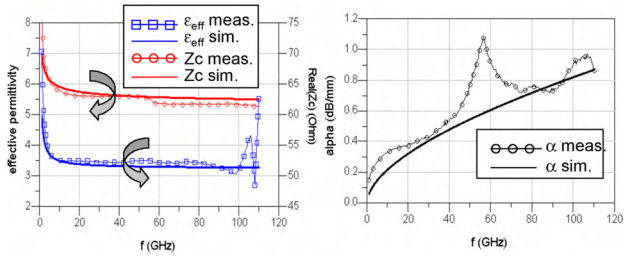

Figure 2. Measured and simulated characteristics of a 50Ohm CPW line versus frequency

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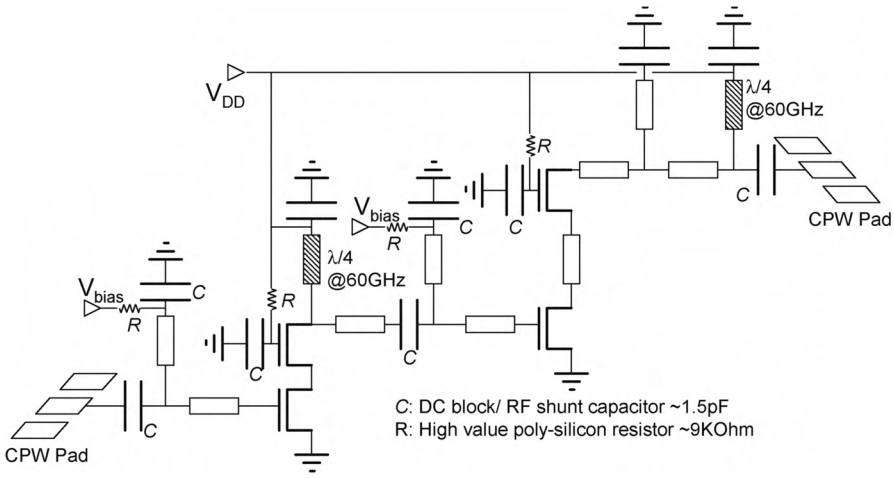

Figure 3. Electrical schematic of the 60 GHz power amplifier.

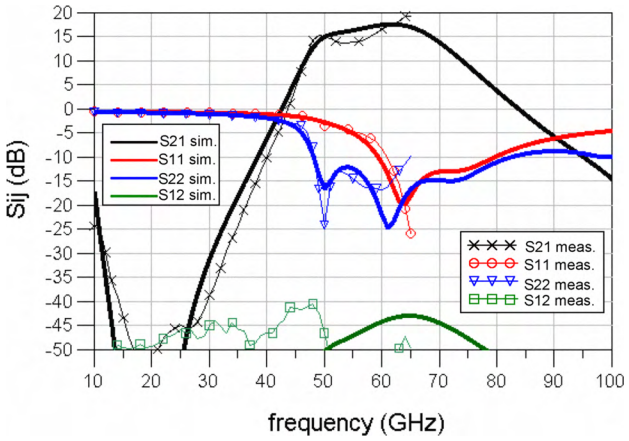

Figure 4. Measured and simulated S parameters of the PA versus frequency. V_{DD}=1.8V, I_{DC}=43mA.

Indeed, the signal attenuation in CPW lines on high resistivity substrate is mainly constituted by metallic losses. Fig.1 shows the cross section schematic of a CPW line in which all metal layers are stacked. As a result the metallic losses are reduced compared to a CPW line in which only the top metal is used for the central conductor. Furthermore, because of electro-migration reliability rules, conductor stacking increases the maximum current that is allowed to pass through the line. For applications like PA the current passing through a line can be several tens of milli-Amperes. Fig.2 shows the measured up to 110GHz effective permittivity, the characteristic impedance and the attenuation of a 50Ohm CPW stacked line. We observe that the losses of the line remain into acceptable values i.e. ~0.6dB/mm at 60GHz. In order to model CPW transmission lines and discontinuities (ex. Bends and Tee junctions), 3-dimensional full wave electromagnetic simulation are performed with the help of *HFSS* (*Ansoft*) simulator. Then, electrical models of transmission lines and discontinuities are extracted and implemented into computer aided design simulators. The high frequency modeling method of passive elements on SOI technology is described in reference [9].

III. CIRCUIT DESIGN

The PA contains two cascode stages with input, inter-stage and output matching networks. Fig.3 illustrates the electrical schematic of the PA. Matching networks use stacked CPW lines that are put in series and in parallel to the input or to the output of a cascode stage. The inter-stage matching network consists of two serial lines and one parallel stub and it is optimized for maximum power transfer between both stages. The output matching network is designed for maximum power transfer to a 50Ohm load at compression. Finally, the input matching network is designed for minimum return loss and maximum small signal gain. In order to optimize gain and output power, the second stage's transistors are larger than the first stage's ones. Indeed, the first cascode stage is constituted by two transistors of 63 fingers (1µm per gate finger), while the second cascode stage contains two transistors of 150 gate fingers (1µm per gate finger). In addition, a transmission line of 50µm length is put between the transistors of the second cascode stage, in order to increase the gain of the stage as shown in fig.3. The layout of the cascode transistors is carefully designed so that the metallic connection from top metal to the transistor tolerates high current values. All parasitics due to layout around the transistors were taken into account with the help of electromagnetic simulations. The V_{DD} supply bias is applied at the end of a quarter wave (at 60GHz) short-ended stub. Quarter wave stubs are employed because they ensure a good signal rejection at high frequency on the V_{DD} supply rail. The last prevents from eventual feed-back between the second and the first stage, therefore eventual instabilities. The common source transistors are biased through external bias on the gate. For that purpose high value poly-silicon resistors (~9KOhm) are placed between the gate and the bias pad. The common gate transistors gate bias is set to the V_{DD} supply voltage in order to benefit the maximum gain. The decoupling between the two stages and the RF shunts at the end of the line stubs are realized with high density, high quality metal-oxide-metal (MOM) capacitors. Typically, 1.5 Pico-Farads capacitors of 25x25µm² area are used.

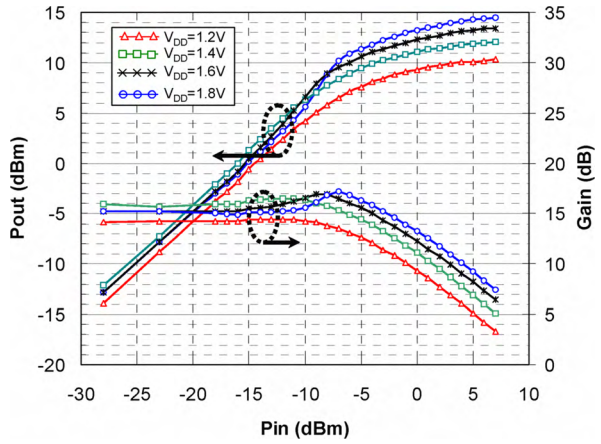

Figure 5. Measured output and power gain versus the input power at 60GHz for various supply voltages.

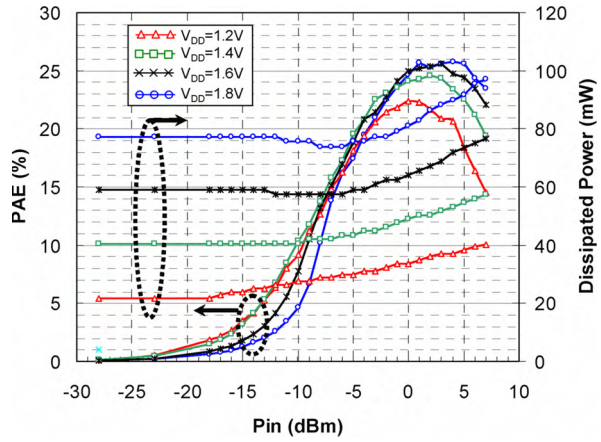

Figure 6. Measured power added efficiency and power consumption versus the input power at 60GHz for various supply voltages.

IV. Measurement Results

The circuit was measured on wafer with the helps of probe tips. Two V-band coplanar wave ground-signal-ground (GSG) probe tips were used for input and output high frequency measurements. For DC biasing a GSGSGS low frequency probe tip was applied to the circuit. All measurements were calibrated at the probe tips planes with respect to 50Ohm reference impedance. In fig.4 are reported the measured and the simulated small signal S parameters of the PA. The measurements were performed up to 65 GHz, though we reported the simulated S parameters up to 100GHz. The PA has a gain larger than 15dB from 50GHz to frequencies higher than the maximum measured one (65GHz). The measured peak gain is 19dB at 65GHz. This measurement was achieved under a power supply of 1.8V and a total DC current of 43mA (77.4mW).

Fig.5 shows the measured output power and the measured power gain versus the input power at 60GHz. The measurements are shown for various V_{DD} supply voltages going from 1.2V to 1.8V. We observe that the small signal power gain varies from 14dB to 16dB when the supply voltage varies from 1.2V to 1.8V. The output saturation power (P_{sat}) shows values that go from 10.5dBm to 14.5dBm, respectively. The output power at 1dB compression point (P_{1dB}) is between 7.1dBm and 12.7dBm, respectively. The gain and power curves of fig.5 show that the PA behaves as a class A amplifier when supplied by 1.2V voltage and trends to a class AB amplifier when the supply voltage increases to 1.8V. Fig.6 shows the PAE and the dissipated power versus the input power at 60GHz for the same previously applied supply voltages. The PAE is defined in (1).

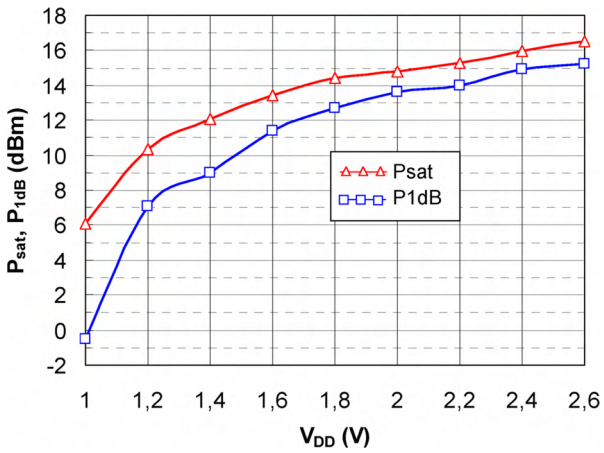

Figure 7. Measured output saturation power and output 1dB compression point power at 60GHz versus the supply voltage V_{DD}.

$$PAE = 100\% \cdot \frac{P_{out}^{mW} - P_{in}^{mW}}{P_{diss}^{mW}} \qquad (1)$$

We observe that the peak values of the PAE are larger than 25% when the circuit operates in class AB, and larger than 22% when operating in class A. The small signal dissipated power of the PA varies from 22mW to 77.4mW when V_{DD} supply is moved from 1.2V to 1.8V. At saturation, the dissipated power varies from 40mW to 97mW respectively.

In order to highlight the output power improvement when V_{DD} supply is increased, we proceeded to power measurements versus V_{DD} at 60GHz. Fig.7 illustrates the P_{sat} P_{sat} and the P_{1dB} at 60GHz versus the supply voltage V_{DD}. We observe that the output power values increase for V_{DD} up to 2.6V voltage supply. P_{sat} and P_{1dB} achieve 16.5dBm and 15.2dBm values when biased at 2.6V, respectively. Table I summarizes the performances of the power amplifier and compares them to recently published PA at 60GHz in CMOS. Note that this PA exhibits the best P_{sat} and PAE ever measured in the 60GHz band for CMOS technologies [1-6].

The micro-photograph of the circuit is shown in fig.8. The die size is 0.94x0.61mm² including pads. The inset of fig.8 shows a zoom on the second cascode stage, in which the 150µm large transistors can be clearly distinguished.

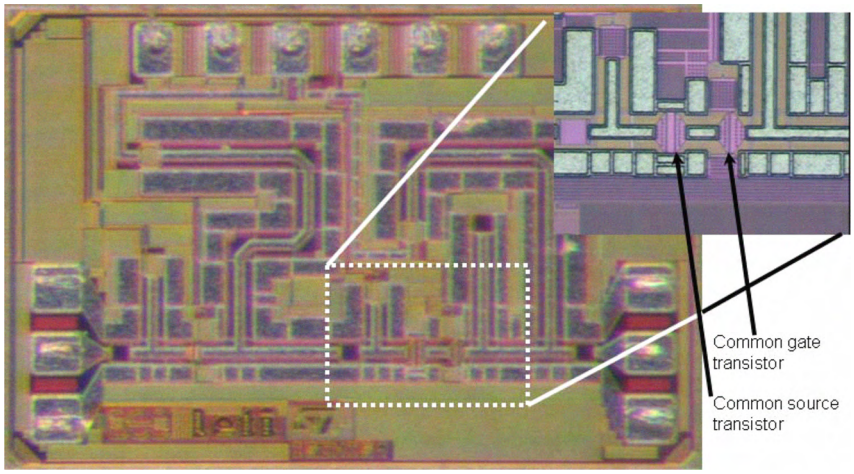

Figure 8. Chip micro-photograph. Chip size: 0.94x0.61mm² including pads. Inset: Zoom on the second stage cascode

V. CONCLUSION

A 60GHz large band power amplifier in SOI CMOS 65nm is described. The PA is made of two cascode stages of different size for power and gain optimization. The matching networks use coplanar wave transmission lines that benefit from the low losses of the high resistivity SOI substrate. The power gain around 60GHz is 16dB and 19dB at 65GHz. The amplifier demonstrates the highest output power and PAE ever reported in CMOS technologies around 60GHz. The output saturation power achieves 14.5dBm, the P_{1dB} 12.7dBm and the peak PAE 25% when the PA is supplied by 1.8V.

TABLE I. SUMMARY OF 60GHZ PA PERFORMANCES IN CMOS

Ref.	*Gain (dB)*	*OP_{1dB} (dBm)*	*P_{sat} (dBm)*	*Peak PAE (%)*	*Diss. Power (mW)*	*Diss. Power at peak PAE*	*V_{DD} (V)*
[1]	25	5	8	7	109.5	N/A	1.5
[2]	8.3	8.2	10	5	228.6	N/A	1
[3]	15.2	10	11	8.2	150	N/A	1
[4]	5.5	9	12.3	8.8	N/A	N/A	1
[5]	16	2.5	11.5	11	43.5	N/A	1
[6]	30	10.3	13.8	12.6	178	180	1.8
This Work	**14**	**7.1**	**10.5**	**22.3**	**21.6**	**33.6**	**1.2**
This Work	**16**	**12.7**	**14.5**	**25.7**	**77.4**	**90**	**1.8**
This Work	**15**	**15.2**	**16.5**	**18.2**	**169**	**202**	**2.6**

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