Reconfigurable Dual-Channel Multiband RF Receiver for GPS/Galileo/BD-2 Systems

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***Abstract*—A fully integrated dual-channel multiband RF receiver is designed and implemented for next-generation global navigation satellite systems (GNSSs) in a 0.18-μm CMOS process. Its two reconfigurable signal channels can simultaneously process any two types of 2-, 4-, or 20-MHz bandwidth signals mainly located around the RF bands of 1.2 and 1.57 GHz for GPS, Galileo, and BD-2 (aka Compass) systems, while achieving better performance (die area, noise figure, gain dynamic range) than other state-of-the-art GNSS receivers. A digital automatic gain control loop consisting of a variable gain amplifier and nonuniform 4-bit ADC is utilized to improve the receiver's robustness and performance in the presence of interferences. While drawing 25-mA current per channel from a 1.8-V supply, this RF receiver achieves a total noise figure of 2.5 dB/2.7 dB at 1.2/1.57 GHz, an image rejection of 28 dB, a maximum voltage gain of 110 dB, a gain dynamic range of 73 dB, and an input-referred 1-dB compression point of -58 dBm, with an active die area of 2.4 mm^2 for single channel.**

***Index Terms*—Automatic gain control (AGC), global navigation satellite systems (GNSSs), multiband, reconfigurable RF receiver.**

I. Introduction

GLOBAL navigation satellite systems (GNSS) have provided the fundamental physical quantities of the absolute position, velocity, and time information to users in a variety of civilian applications [1], [2]. Until now, the global positioning system (GPS) developed by the U.S. is the only fully operational GNSS. The European Union's Galileo positioning system, however, a GNSS in the initial deployment phase, is scheduled to be available in 2013 [3]. China has launched eight navigation satellites (as of June 2011) to construct the next-generation GNSS "BeiDou-2 (BD-2)" (also known as COMPASS), and the systems will be expanded into a fully operational GNSS by 2020 [4].

In order to improve the position accuracy and the operational capability in multipath and jamming environments, the new civil navigation signals called L2C and L5 will be added into the next-generation GPS [5]. For the same motivations as the GPS modernization plan, BD-2 and Galileo systems employ dual bands at B1/B2 and E1/E5, respectively [3], [4]. As summarized in Table I, these GNSS signals are mainly located at the RF bands of 1.2 and 1.57 GHz with 2-, 4-, or 20-MHz bandwidth (BW).

TABLE I
List of GNSS Signals

System	Band	Center Freq. (MHz)	Bandwidth (MHz)
GPS	L1 C/A	1575.42	2.046
	L2 C	1227.6	2.046
	L5	1176.45	20.46
Galileo	E1	1575.42	4.092
	E5a	1176.45	20.46
	E5b	1207.14	20.46
BD-2	B1	1561.098	4.092
	B2	1207.14	20.46

Most reported GNSS RF receivers focus on the GPS L1 band and some of them have been integrated into a system-on-chip (SoC) [7]–[13]. The applications of GNSS receivers in extreme environments, however, usually need cooperating from several GNSS bands, or even multiple navigation systems. Recently, some efforts have been made to design multimode and multiband GNSS receivers in [5], [6], [14], and [19], but these RF receivers lack sufficient flexibility for processing all of the GNSS signals. This paper presents the design and implementation of a dual-channel multiband RF receiver for GPS/Galileo/BD-2 systems. The reconfigurable receiver can simultaneously process any two types of GNSS signals listed in Table I, and for antijamming purposes, a digital automatic gain control (AGC) loop is implemented to suppress unwanted interference and to achieve constant optimal signal amplitude at the input of the analog-to-digital converter (ADC), and thus better ADC performance. To further improve the receiver's robustness, a 4-bit nonuniform adaptive ADC, which has the capability of reducing the degradation of signal-to-noise ratio (SNR) resulted from continuous wave interference (CWI), pulsed wave interference (PWI), and Gaussian interference [17]–[20], is adopted. This GNSS RF receiver enhances the system's robustness and position accuracy of next-generation the GNSS's receiving terminal.

This paper is organized as follows. Section II describes the GNSS fundamentals and the advantages of dual-channel and multiband reception. Section III discusses the architecture considerations and system performance of the dual-channel multiband GNSS receiver. Section IV presents the detailed circuit implementations. Section V shows the experimental results of the fabricated GNSS receiver. Section VI concludes this paper.

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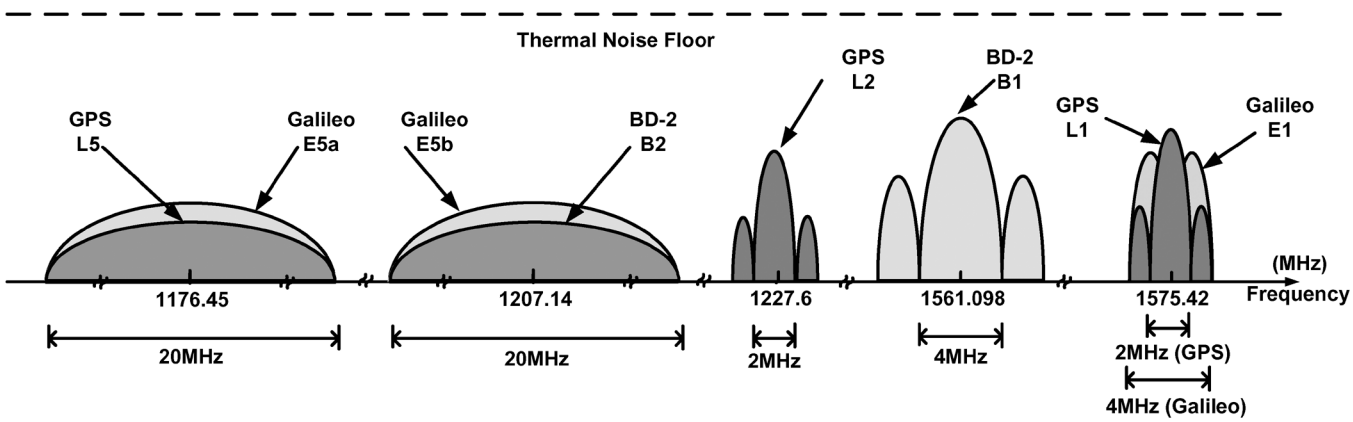

Fig. 1. Band spectrum of the GNSS signals.

II. Next-Generation GNSS

A. New GNSS signals

1) GPS: The GPS L1 signal is allocated at 1575.42 MHz using binary phase-shift keying (BPSK) modulation, the main lobe of which occupies a BW of 2 MHz [1]. The main drawback of current civil GPS is poor position accuracy, especially in multipath and jamming environments [1], [5].

To overcome those weaknesses, the new civil navigation signal called L2C and L5 will be added into next-generation GPS. The L2C signal with BW of 2 MHz is located at the L2 band (centered at 1227.6 MHz) [5]. The L5 signal is centered at 1176.45 MHz with a BW of 20 MHz [6].

2) Galileo: The Galileo project is an alternative and complementary to the GPS and is intended to provide more precise position measurements than current civil GPS. As shown in Fig. 1, the Galileo E1 signal is also centered at 1575.42 MHz, but with binary offset carrier (BOC) spreading modulation, occupying a signal BW of 4 MHz. The other Galileo signals, as listed in Table I, i.e., E5a and E5b, are both located near the band of 1.2 GHz and have a signal BW of 20 MHz [3].

3) BD-2: The first BeiDou system, officially called the BD-1 Satellite Navigation Experimental System, has been offering navigation services mainly for customers in China and its neighboring regions since 2000. The next-generation system, BD-2 System (aka the Compass System), shall be a global satellite navigation system consisting of 35 satellites and is still under construction. Also shown in Fig. 1, the BD-2 B1 band is centered at 1561.098 MHz using quadrature phase-shift keying (QPSK) modulation, which has a signal BW of 4 MHz [4]. Same as the Galileo E5b, another signal of BD-2, the B2, is also using the band of 1207.14 MHz and has a BW of 20 MHz.

B. Features of GNSS Signals

As shown in Fig. 1, all GNSS signals have the following common characteristics. First, GNSS signals mainly use two RF bands: 1.2 and 1.57 GHz, and the center frequencies of the GNSS signals are concentrated in the tens of megahertz at these RF bands. Based on this feature, a reconfigurable RF front-end can simultaneously process all of the GNSS signals. Secondly, all of the GNSS systems adopt the technology of a direct sequence spread spectrum (DSSS), which provides processing gain for the receiver [1]–[4]. Generally, the thermal noise with Gaussian distribution dominates the received power strength. In other words, all of the GNSS signals are buried under thermal noise, and the input SNR can go down to about −25 dB [5]. Finally, for achieving larger processing gain, the new GNSS signals usually have wider BW than the existing GPS L1 signals.

C. Why Dual-Channel and Multiband in GNSS Receiver

The sensitivity and position accuracy of a current GPS system could be extremely deteriorated in some special environments, such as wooded areas, building insides, and under tunnels [5]. In addition, multipath effect and polluted electromagnetic environment are usually present to the GNSS receivers. The simple GPS receiver with single band reception simply cannot provide sufficient availability and navigation accuracy. Employing multiband in GNSS receivers, as stated previously, should be an efficient way to achieve better acquiring and tracking performance [5], [6], [14], [15].

With the dual-channel architecture, the GNSS receivers can simultaneously process the signals from the different GNSS, for example, GPS and BD-2. Consequently, this dual-channel scheme will increase the number of visible satellites for the GNSS receiver and improve the navigation accuracy and availability [15].

D. Design Challenges for Dual-Channel and Multiband GNSS Receivers

Based on the characteristics of GNSS signals, some design challenges must be taken in the implementation of dual-channel and multiband GNSS receivers.

- The RF front-end must be reconfigurable for the two main RF bands: 1.2 and 1.57 GHz. Meanwhile, the noise figure (NF) and linearity performance of the RF front-end must meet the stringent specifications.
- The analog baseband (ABB) should be capable of processing all of the GNSS signals with different BW. In addition, gain control, image rejection, and variable IF should be realized as well.
- Traditionally, a 2-bit ADC that uses a buffered temperature compensated X'tal (crystal) oscillator (TCXO) signal as the sampling clock is good enough for the GPS L1 band

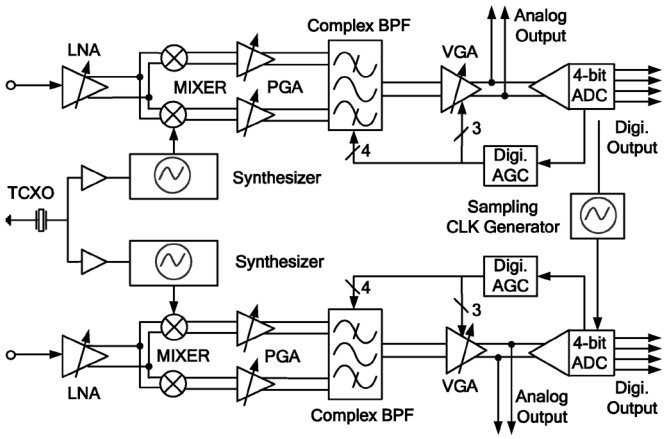

Fig. 2. Block diagram of the GNSS receiver.

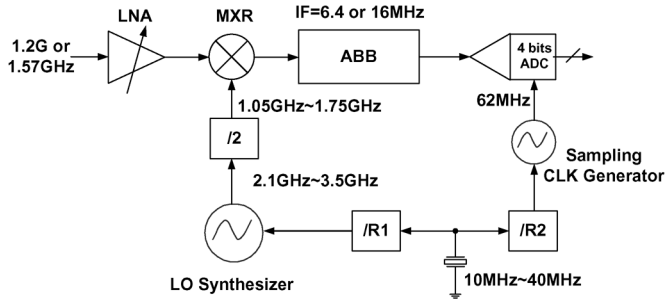

Fig. 3. Frequency plan of the proposed GNSS RF receiver.

[10], [11]. However, in the case of GNSS signals with 20-MHz BW, a 4-bit ADC with a faster sampling clock is demanded. Compared with the 2-bit ADC, the 4-bit ADC has better SNR, and thus, better sensitivity [1].

- Antijamming techniques have to be employed to improve the GNSS receivers' performance and robustness in the presence of polluted electromagnetic environment, especially in the case where the GNSS receivers coexist with other wireless transmitters, such as mobile phone transceivers.

III. Receiver Architecture

A. Receiver Architecture

The purpose of this research is to design and implement an RF receiver that can simultaneously process all of the GNSS's signals, as listed in Table I. Dual-channel and low IF architecture [15], as shown in Fig. 2, is proposed to realize a tri-mode (GPS, Galileo, and BD-2) and multiband GNSS RF receiver. The low-IF architecture not only improves the receiver integration level, but avoids the problem of flicker noise [5], [13].

The RF receiver consists of two separate and independent signal channels for simultaneous reception of any two GNSS signals, e.g., GPS L1 and GPS L5, or GPS L2 and BD-2 B1, and so on. Furthermore, most of the building circuit blocks in the receiver are reconfigurable and reusable in both channels to achieve the tri-mode and multiband functionality and lower the design and applications complexity.

Each signal channel of the RF receiver is composed of a low-noise amplifier (LNA), a down-conversion mixer (MXR) followed by a programmable gain amplifier (PGA), a complex bandpass filter (BPF), a variable-gain amplifier (VGA) with a digital AGC loop, a 4-bit nonuniform adaptive ADC, along with an integer-N phase-locked loop (PLL) and a wideband voltage-controlled oscillator (VCO). The output of each channel can be taken after the ADC (in the digital domain) or before the ADC (in the analog domain) for testing and application flexibility.

The RF signals around 1.2 or 1.57 GHz would be first amplified by the LNA and then down-converted to the IF by the quadrature mixer. The following reconfigurable complex BPF provides channel selection, image rejection, and antialiasing, as well as gain control for the down-converted GNSS signals. It also provides multiple operational modes for processing various GNSS signals. For GNSS signals with 2- or 4-MHz BW, the complex BPF can be configured with a center frequency of 6 MHz and a BW of 2, 4, 6, or 8 MHz; for GNSS signals with 20-MHz BW, the complex BPF can be configured with a center frequency of 16 MHz and a BW of 5, 10, 15, or 20 MHz. This configurability of the complex BPF enables the RF receiver to process all types of GNSS signals with different BW.

B. IF Selection and Frequency Plan

The low-IF architecture is more suitable for the GNSS's receiver than the zero-IF architecture because the zero-IF architecture would suffer from the problems of dc offset and flicker noise from MOS transistors. The IF should be high enough for easy removal of the dc offset and flicker noise. However, a lower IF is desirable for low-power ADC design, and more importantly, for relaxing the image-rejection requirement by moving the image band into the protected GNSS's guard band, and across these bands, the GNSS signals are dominated by the thermal noise and no other signal is present. In addition, the IF should be reconfigurable to accommodate various GNSS signal BW.

The frequency plan for this RF receiver is outlined in Fig. 3 (only one channel shown). Two independent frequency synthesizers based on an integer-N PLL provide wideband LO frequencies for each channel with the tuning range from 1.05 to 1.75 GHz, which covers all of the RF bands used by GNSS satellites.

Different from mostly reported architectures [5]–[14], the clock signals for the digital AGC loops and ADC blocks, as well as the digital baseband chip, are generated by the third frequency synthesizer with a tiny digital ring oscillator rather than the divided-down local oscillator (LO) signal. Traditionally, the ADC of GPS receivers use a buffered TCXO signal or a clock from the divided LO signals as the sampling clock. However, the LO signals are reconfigurable and should be changed for different operational modes in the case of a multimode and multiband GNSS receiver. In addition, for the GNSS signals with 20-MHz BW, higher sample frequency must be adopted. Based on these reasons, an independent PLL loop with a ring oscillator is designed to provide more flexible clock signals for the ADC and digital AGC loop in this study.

This clock generation scheme can save power consumption and increase clocking flexibility. A 62-MHz clock signal is

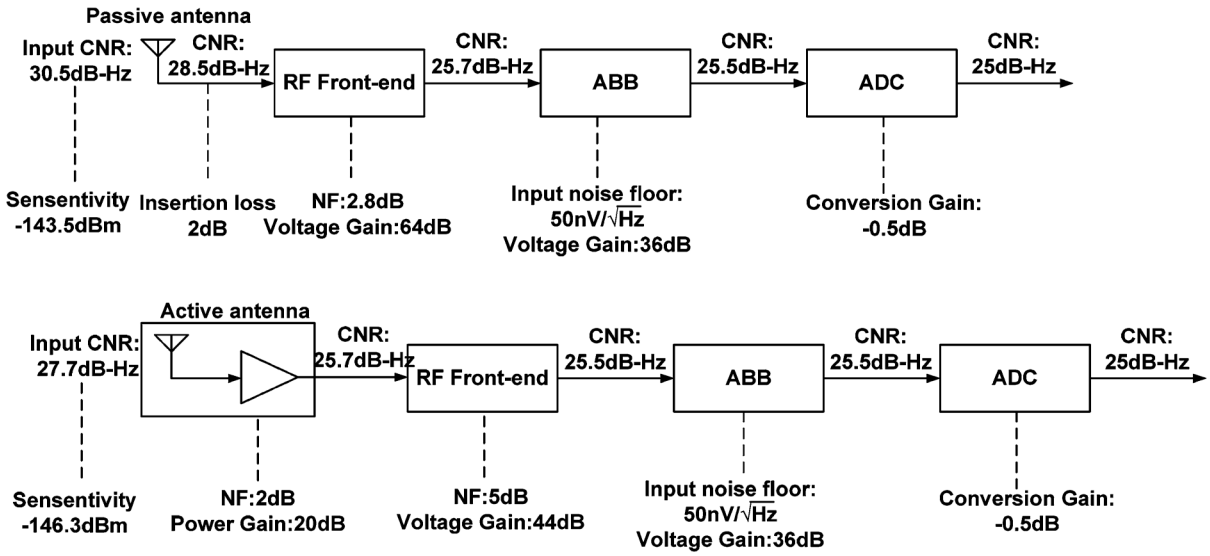

Fig. 4. Noise and gain lineup of the proposed RF receiver in the case of a passive or an active antenna.

chosen as the sampling clock for the AGC loops and ADCs in both channels.

C. Noise and Gain

In consideration of various BW of GNSS signals, the carrier-to-noise ratio (CNR) is more appropriate to quantify noise performance of GNSS RF receivers than SNR. The minimum required CNR for the digital correlator to acquire and track the satellite signals and then to obtain correct navigation messages is 25 dB · Hz [5]. In the entire GNSS RF receiver chain, the antenna, RF front-end, and ADC all contribute major noise degradation. Usually the LO signals with average phase noise of −80 dBc/Hz will cause about 0.1-dB loss in the CNR and the image signals will corrupt the down-converted spectrum and degrade the CNR by about 0.1 dB with an image rejection ratio (IMRR) of 16 dB [5].

Gain controls are implemented along the signal channel to optimize the noise and antiinterference performance in the GNSS receiver. To achieve better receiver performance in the presence of interferences, a 73-dB gain dynamic range was implemented in the signal channel. The gain control in the LNA, PGA and BPF, and VGA provides 8-, 18-, and 47-dB gain dynamic range, respectively. The LNA and PGA gain controls are programmable through digital controls from the serial peripheral interface (SPI) to achieve a better tradeoff between the noise and linearity performance in the RF front-end. The gain controls in the BPF and VGA are realized using a digital AGC loop to achieve a constant signal magnitude at the ADC input for optimized ADC performance.

Fig. 4 depicts the noise and gain lineup of the entire GNSS RF receiver in the case of a passive or an active antenna. If a passive antenna is adopted, the required NF is 2.8 dB for receiver sensitivity of −143.5 dBm, as shown in Fig. 4. With an active antenna, the receiver sensitivity will be improved and the required NF could be relaxed (e.g., 5-dB NF and −146.3-dBm receiver sensitivity, as shown in Fig. 4.

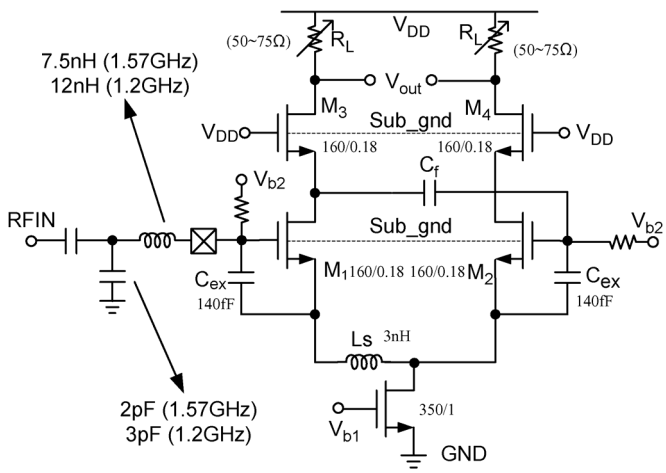

Fig. 5. Schematic of the dual-band LNA and matching network.

An external SAW filter should be placed in the front of the receiver to suppress the out-of-band jammer resulted from other wireless systems, and to relax the linearity requirement of RF front-end. The in-band third-order intermodulation intercept point (IIP3) specifications of the LNA and MXR are −10 and −5 dBm, respectively. Reference [16] presents a detailed discussion about the interference and linearity of the GNSS receiver.

D. Adaptive ADC and Digital AGC for antiJamming

Antijamming techniques have rarely been used in civil GNSS receivers because the application of the spectral spreading technique provides additional process gain for the receiver [17]. Nevertheless, due to the polluted electromagnetic environment and coexistence of a GNSS receiver together with other RF transceivers on the same silicon die or printed circuit board (PCB), it is desirable for the GNSS receivers to have sufficient robustness against occasional or intentional jammers [18], [19]. A nonuniform ADC can be adaptively adjusted based on the

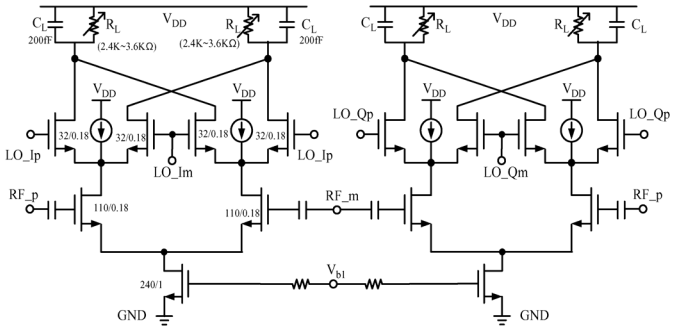

Fig. 6. Schematic of the mixer.

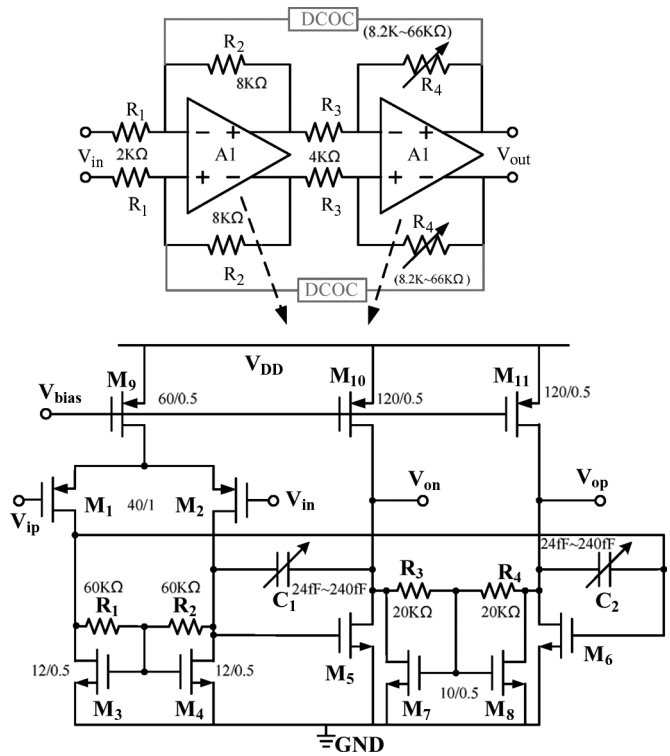

Fig. 7. Schematic of the PGA.

power strength of CWI jamming to achieve an optimized conversion gain of the ADC (i.e., the SNR loss in ADC) and thus better receiver performance [18]–[21]. In this proposed GNSS receiver, a 4-bit nonuniform ADC adaptively controlled by a digital AGC is designed for antijamming and performance optimization.

IV. Circuit Implementations

A. Reconfigurable RF Front-End

The reconfigurable RF front-end consists of an LNA, a double-balanced mixer, and a PGA. As shown in Fig. 5, the LNA is a pseudodifferential amplifier with an inductive degeneration. With a wideband resistive loading, the LNA can be operating at either 1.2 or 1.57 GHz for GNSS signals shown in Table I. To support either a passive or an active antenna, the LNA has two programmable gain states with a gain step of 8 dB, realized through a switching resistive load.

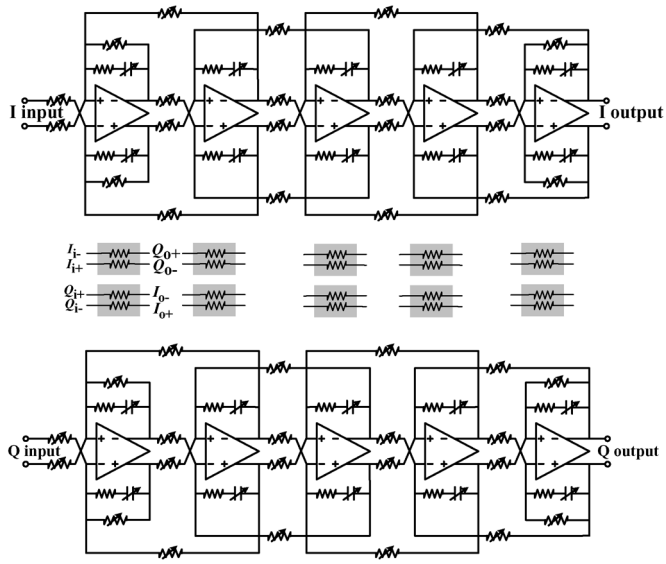

Fig. 8. Schematic of the complex BPF.

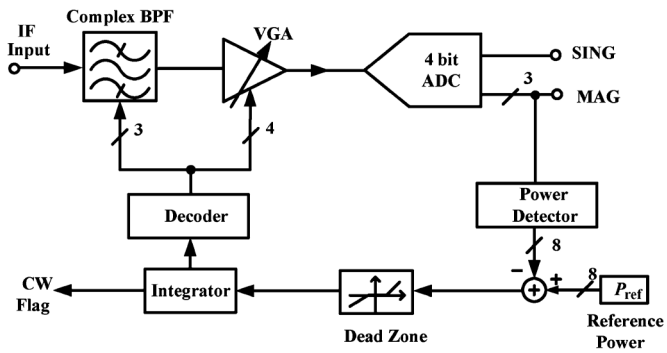

Fig. 9. Block diagram of the digital AGC.

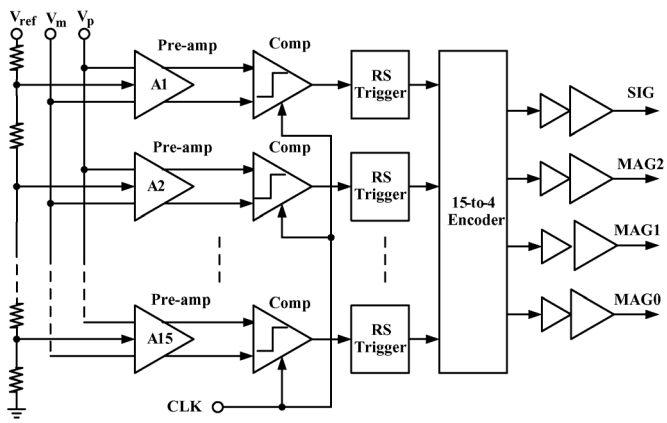

Fig. 10. Block diagram of the 4-bit flash ADC.

A single-ended-to-differential conversion circuitry is incorporated in the LNA to provide differential operation for the subsequent circuit blocks and increase the LNA gain by 6 dB. The tail current source along with the compensation feedback capacitor C_f improves the phase and amplitude imbalance of the single-ended-to-differential conversion [22]. In order to easily obtain simultaneous noise and input matching for dual band (1.2 and 1.57 GHz), extra capacitors $C_{\rm ex}$ are placed across

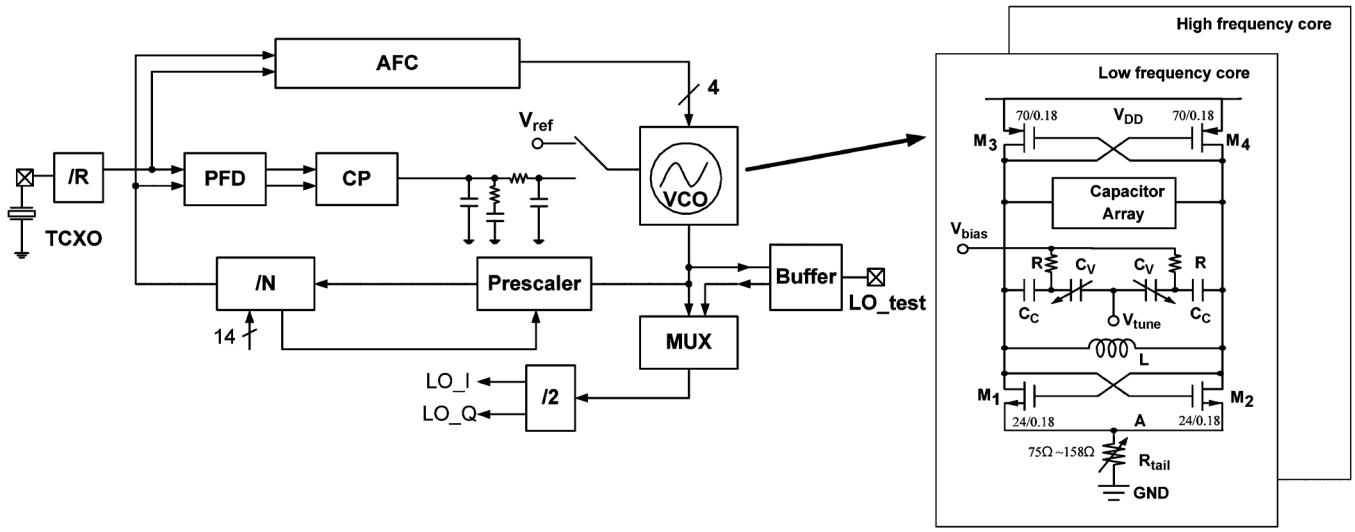

Fig. 11. Block diagram of the integer-N PLL and schematic of the dual-core VCO.

the gate and source of input stage [22]. The added $C_{\rm ex}$ slightly degrades the noise performance, but that makes input matching easier. If the size and bias of transistor M1 is given, appropriate noise performance and input matching can be achieved for both the 1.2- and 1.57-GHz bands with proper values of inductance L_s and $C_{\rm ex}$. The optimized transistor size of M1 and M2 is 160 μm/0.18 μm, and $C_{\rm ex}$ is 140 fF.

The simulated gain of this LNA is 23 and 20 dB at 1.2 and 1.57 GHz, respectively, adequate to suppress the noise contribution from the subsequent stages. The simulated IIP3 is -5.7 and -3.9 dBm and the NF is 2.1 and 2.3 dB at 1.2 and 1.57 GHz, respectively.

The double-balanced mixer based on Gilbert's topology is shown in Fig. 6. The current bleeding technique is adopted in the mixer to reduce the flicker noise contributed from switching pairs while improving the linearity of the mixer at the same time [22]. The dc-bias current and load resistor R_L in the mixer are programmable to provide a slight adjustment of the mixer's conversion gain.

The in-phase and quadrature outputs of the mixer are fed into the PGA, which is implemented between the RF front-end and the baseband complex BPF to relax the noise requirement for the complex BPF and optimize the linearity performance. As shown in Fig. 7, a fully differential Opamp with resistive feedback is utilized to realize the PGA for low noise and high linearity. In the Opamp, as shown at the bottom of Fig. 7, two tunable compensation capacitors (C_1 and C_2) are used to obtain constant BW. Moreover, an integrated dc-offset cancellation (DCOC) circuit based on a low-pass filter (LPF) is incorporated to suppress the dc component of the output signals. The PGA's 3-dB BW is set to be 145 MHz and the ripple of the PGA output is kept less than 0.2 dB across all interested GNSS bands (2 $\sim$ 30 MHz). The PGA achieves a third-order input intercept voltage point (IIV3) of 1.78 V and an input-referred noise of 14.5 nV/$\sqrt{\rm Hz}$.

B. Reconfigurable Complex BPF

A fifth-order Chebyshev-I complex BPF based on fully differential Opamp-RC integrators, as shown in Fig. 8, is implemented to achieve not only the channel selection, but also the image rejection, gain control, and DCOC [13], [15], [23]. The complex BPF selects the GNSS signal and rejects the image and out-of-band spurious signals and noise. It is implemented by means of two real LPFs quadrature coupled to achieve the frequency shift at the IF frequency $\omega_{\rm IF}$. All of the frequency-dependent elements in the LPF should be transformed into a function of $s - j\omega_{\rm IF}$ from s. Therefore, the output of the complex filter (CF) is given by

$$X_{\rm out} = \frac{A \cdot \omega_0}{\omega_0 + s - j\omega_{\rm IF}} X_{\rm in} \tag{1}$$

where A is the gain of the LPF, and ω_0 is the cutoff frequency of the LPF. In general, the desired signal in the I-branch leads the Q-branch by 90° and the output of each branch can be written as

$$I_{\rm out} = \frac{A \cdot \omega_0}{s + \omega_0} \left(I_{\rm in} - \frac{\omega_{\rm IF}}{A \cdot \omega_0} Q_{\rm out} \right) \tag{2}$$

$$Q_{\rm out} = \frac{A \cdot \omega_0}{s + \omega_0} \left(Q_{\rm in} + \frac{\omega_{\rm IF}}{A \cdot \omega_0} I_{\rm out} \right). \tag{3}$$

Equations (2) and (3) are implemented through the quadrature-coupled resistors (highlighted in Fig. 8), which set the frequency shift.

In order to reconfigure the center frequency or IF, BW, and gain, all the capacitors and resistors in the filter are implemented as binary arrays that are set to provide two operational modes: the first is IF $\approx$ 6 MHz and BW $= 2, 4, 6,$ or 8 MHz, while the second is IF $\approx$ 16 MHz and BW $= 5, 10, 15,$ or 20 MHz. To save power, this filter is also designed to realize the large gain programmability (from 0 to 42 dB at 6 dB per step) and play the role of the VGA block through five variable-gain stages. Followed by a very simple VGA with a small gain step (from 0 to 5.5 dB at 0.5 dB per step), this programmable complex BPF is part of the digital AGC loop to achieve constant power strength at the ADC input.

Due to the PGA placed between the mixer and the complex BPF, the noise requirement for the filter is relaxed, and as a

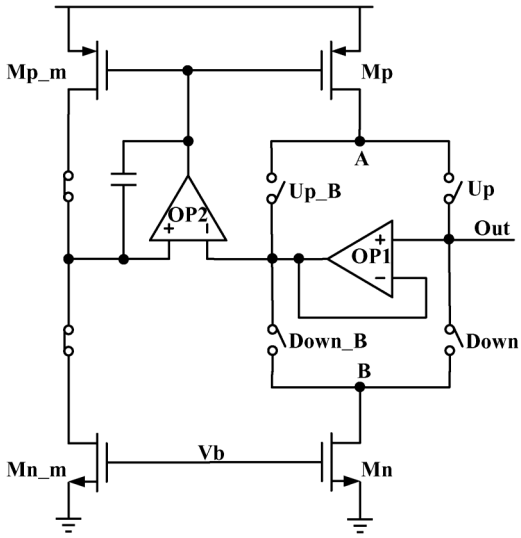

Fig. 12. Schematic of the CP.

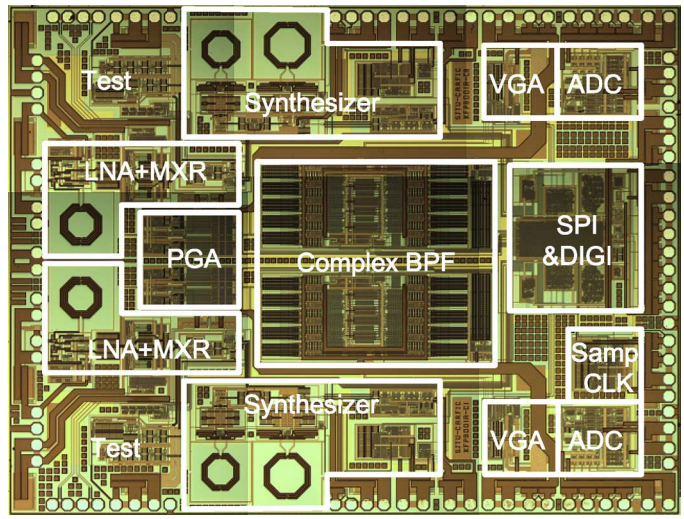

Fig. 13. Chip microphotograph of the dual-channel GNSS receiver.

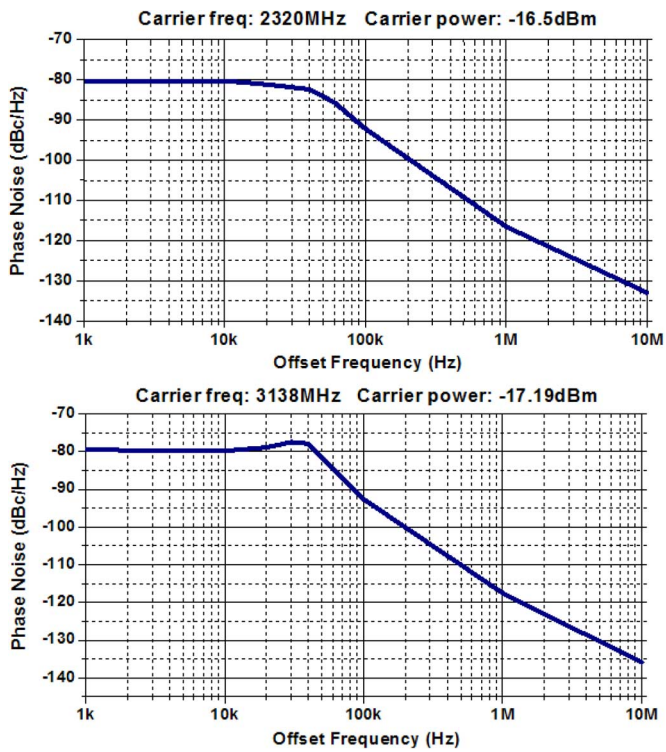

Fig. 14. Measured phase noise (frequency $= 2 \times$ LO).

consequence, it provides substantial design margin for linearity and silicon area. Moreover, an automatic digital *RC* tuning block guarantees the frequency accuracy of the set IF and BW.

C. Digital AGC and 4-bit Flash ADC

As shown in Fig. 9, the complete digital AGC loop is composed of the complex BPF, a digital VGA [20], a digital AGC feedback control loop, and a nonuniform 4-bit flash ADC. Gain controls are realized using this digital AGC loop to achieve constant optimal signal amplitude at the ADC input, and thus, better ADC performance. A 47-dB gain control range is provided by the complex BPF and the digital VGA, which has a linear-in-decibel characteristic and is tunable from 0 to 47 dB with a 0.5-dB gain step. Furthermore, in the presence of jammers, the digital AGC loop generates the signal of a continuous wave (CW) flag if the ADC saturates. With the notification from the CW flag signal, the digital baseband can adaptively adjust the reference signal P_{ref}, which determines the threshold of the ADC, and thus an optimum ADC conversion gain is achieved. In other words, the digital AGC loop, which is adaptively controlled by the digital baseband, can effectively suppress the jamming of CW interference and Gaussian interference [19], [21]. Finally, the digital AGC is more area efficient compared with a traditional analog counterpart since the digital AGC loop is free of huge loop capacitors.

Fig. 10 shows the block diagram of the proposed 4-bit flash ADC. The fully differential input and reference signals are fed into 15 parallel pre-amplifiers followed by comparators and RS triggers, and then the relevant 15-bit thermometer code generated by the comparators will be converted to a 4-bit binary code in the 15-to-4 encoder block [18], [24].

D. Synthesizer

There are two independent signal channels in this chip, and two separate PLLs provide the wideband quadrature LO signals for each channel. The complete integer-N PLL, including the dual-core VCO, the dual-mode prescaler, the phase frequency detector (PFD), the charge pump (CP), the programmable divider, the automatic frequency calibration (AFC), and the buffers, as shown in Fig. 11, is fully integrated. The VCO oscillates at twice the LO frequency and its output is divided by 2 for the quadrature LO signals.

A dual-core *LC*-VCO, as shown on the left-hand side of Fig. 11, is adopted in the PLL [6]. The quality factor of the *LC* tank is optimized by using top metal inductors and metal–insulator–metal (MIM) capacitors. The VCO gain (K_{VCO}) is set to be around 60 MHz/V to ensure good phase-noise performance. A 4-bit digitally controlled capacitor bank is used to obtain a large VCO tuning range. The capacitor bank is controlled by the AFC using a binary search algorithm. The optimized Q factor of *LC* tank is 9.3.

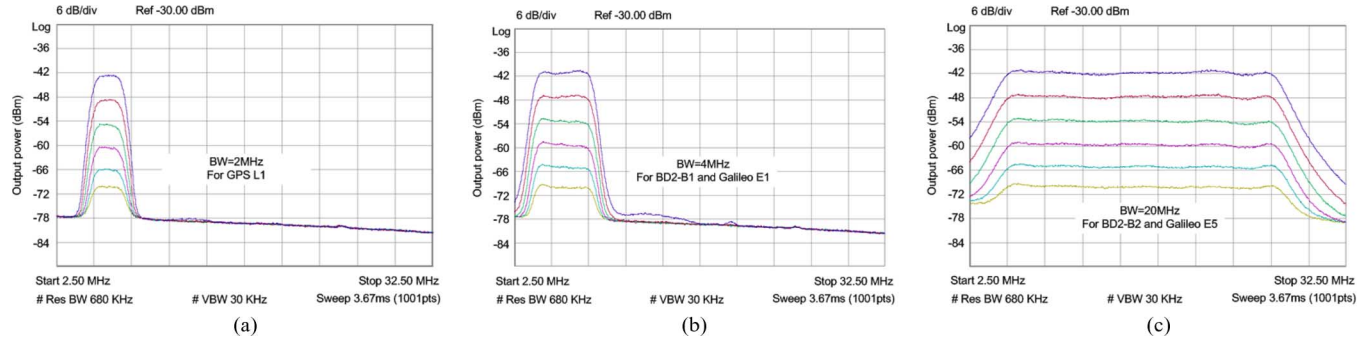

Fig. 15. Measured output spectrum of ABB with the tuning of IF, BW and gain. (a) GPS L1 mode. (b) BD-2 B1 or Galileo E1 mode. (c) BD-2 B2 and Galileo E5 mode.

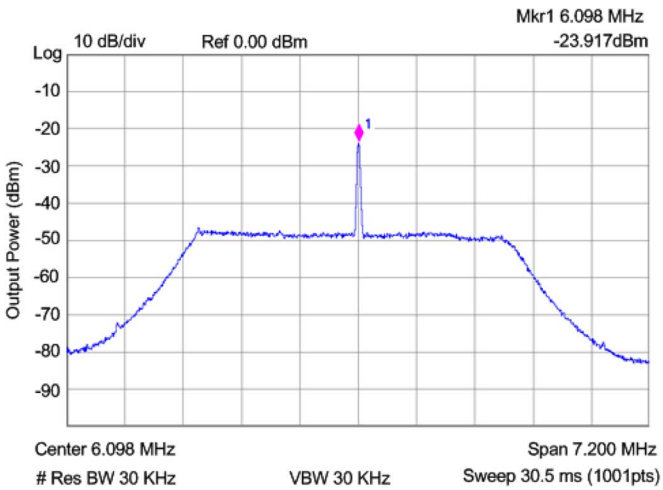

Fig. 16. Measured IF output spectrum of the GNSS RF receiver with −100-dBm RF input signal in BD-2 B1 mode.

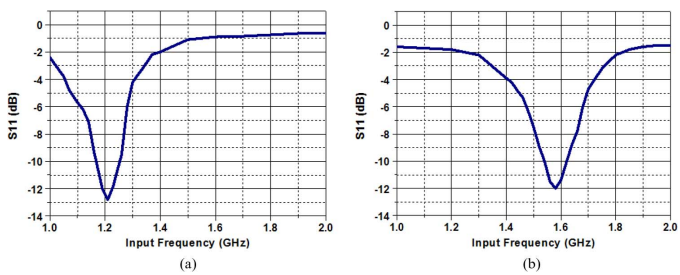

Fig. 17. Measured input $S11$. (a) 1.2-GHz band. (b) 1.57-GHz band.

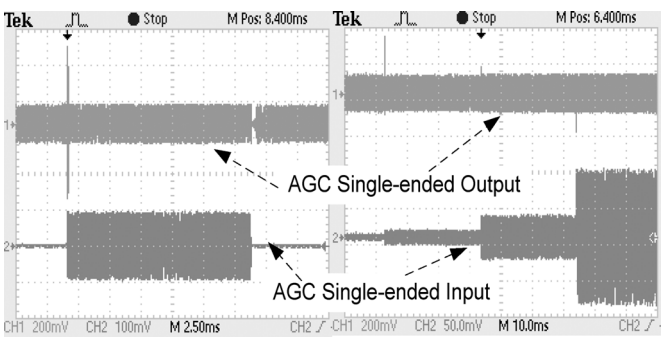

Fig. 18. Measured transient response of the digital AGC loop.

The proposed CP, which employs two Opamps to solve problems of current mismatch and charge sharing, is shown in Fig. 12. Opamp 1 working as a voltage follower is applied to settle the charge sharing problem [25]. The voltages on parasitic

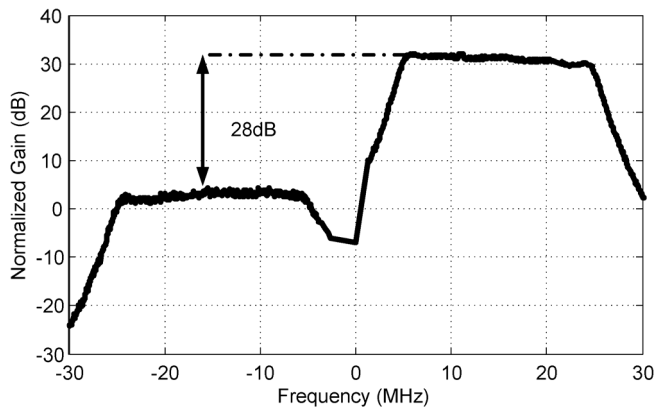

Fig. 19. Measured IMRR at BW of 20 MHz.

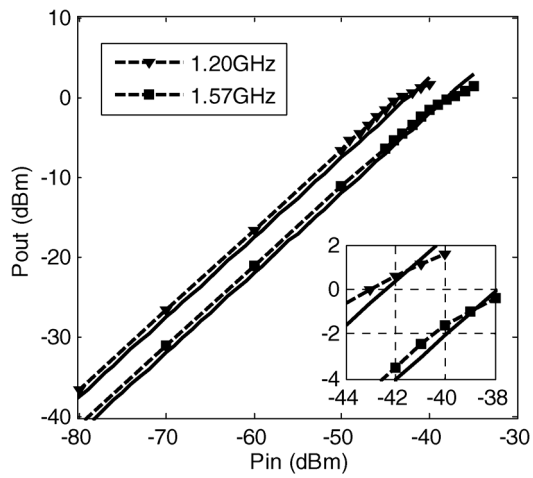

Fig. 20. Input-referred 1-dB compression point at minimum gain setting.

capacitors at nodes A and B are clamped so no charge transfer would occur. To remove current mismatches, the pMOS current sources are biased by Opamp 2 using the self-bias technique to force them to copy the nMOS sink currents precisely [26].

For power saving, flexibility, and low-cost considerations, a third individual PLL frequency synthesizer based on a ring oscillator is implemented to generate a 62-MHz clock signal for the ADC and AGC loop.

V. Experimental Results and Discussions

The reconfigurable dual-channel multiband GNSS RF receiver is fabricated in a 0.18-μm CMOS process and packaged in a standard 48-pin quad-flat no-leads (QFN) package. The

TABLE II
PERFORMANCE COMPARISON WITH STATES-OF-THE-ART

	This Work Single channel	**[14] TMTT2009**	**[13] JSSC2007**	**[7] ISSCC2010**	**[8] ISSCC2009**	**[5] JSSC 2005**	**Unit**
Technology	0.18um CMOS	0.18um CMOS	0.18um CMOS	65nm CMOS	0.11um CMOS	0.18um CMOS	
Mode and Band	GPS L1, L2 Galileo E1, E5a, E5b BD-2 B1, B2	L1, E1	L1	L1	L1	L1, L2	
NF	1.2 GHz 2.5 1.57 GHz 2.7	4.5	5	2.3	3.2	1.2 GHz 7.5 1.57GHz 8.5	dB
Channel BW	2, 4 or 20	2 or 4	2	2	2	2	MHz
Maximum Voltage Gain	110	108	NA	90	99	95	dB
Gain dynamic range	73	NA	40	42	48	70	dB
IMRR	28	34	23	30	40	20	dB
LO Phase noise @1MHz offset	1.2 GHz -122 1.57 GHz -124	-126	-108	-114	-115	-113	dBc/Hz
Active area (single channel)	2.4	5.2	2.5	2.5	2.4	2.6	mm^2
Supply current (single channel)	25	23	11.5	12.7	13	10.5	mA
Supply voltage	1.8	1.8	1.8	1.8	1.2	1.8	V

chip microphotograph is shown in Fig. 13. The active die area for a single channel of the receiver is 2.4 mm^2, while the whole chip, including two independent signal channels, the test circuits, electrostatic discharge (ESD) circuitry, and the I/O pads, occupies a die area of 2.4×3 mm^2.

The measured phase noise at 1-MHz frequency offset is about -122 dBc/Hz for 1.2-GHz LO and -124 dBc/Hz for 1.57-GHz LO. The measured frequency tuning range of the VCO is from 2.1 to 3.7 GHz. Fig. 14 shows the measured phase noise for the 1.2-GHz band (up) and 1.57-GHz band (down).

The measured frequency response of the ABB for various modes (i.e., various IF frequencies, BW, and gain settings) is shown in Fig. 15. The measurements demonstrate the reconfigurable RF receiver's capability of processing all of the GNSS signals with BW of 2, 4, or 20 MHz. Fig. 16 shows the IF output spectrum of the whole receiver at the moderate gain setting with a -100-dBm RF input signal when reconfiguring IF ≈ 6 MHz and BW $= 4$ MHz for BD-2 B1 band.

As shown in Fig. 16, the measured output CNR is about 25.08 dB, the NF of the GNSS could be obtained by the following equation:

$$\begin{aligned} \mathrm{NF} &= \mathrm{CNR_{in}} - \mathrm{CNR_{out}} - \mathrm{IL} \\ &= [-100\ \mathrm{dBm} - (-174\ \mathrm{dBm/Hz})] \\ &\quad - [25.08\ \mathrm{dB} + 10\log(30\ \mathrm{kHz})] - 1.4\ \mathrm{dB} \\ &= 2.7\ \mathrm{dB} \end{aligned} \tag{4}$$

where the IL is the measured insertion loss that resulted from the input SMA cable and connectors. The measured NF of the entire receiver is 2.5 dB at 1.2 GHz or 2.7 dB at 1.57 GHz. The measured maximum voltage gain is 110 dB with a dynamic range of 73 dB.

The measured input $S11$, as shown in Fig. 17, is about -12 and -11 dB at 1.2 and 1.57 GHz, respectively. The transient response of the digital AGC loop is presented in Fig. 18. As shown, the AGC can maintain constant output power (i.e., input power to the ADC) for optimized ADC performance when the input power to the AGC changes with either a small or large step. The measured IMRR is 28 dB for the 20-MHz BW signal, as plotted in Fig. 19. It is slightly less than the simulation results due to I/Q mismatch in the signal chain and LO path. The input-referred 1-dB compression point (1-dB CP) is -42 dBm/ -39 dBm at the 1.2- and 1.57-GHz band with minimum gain setting, as shown in Fig. 20.

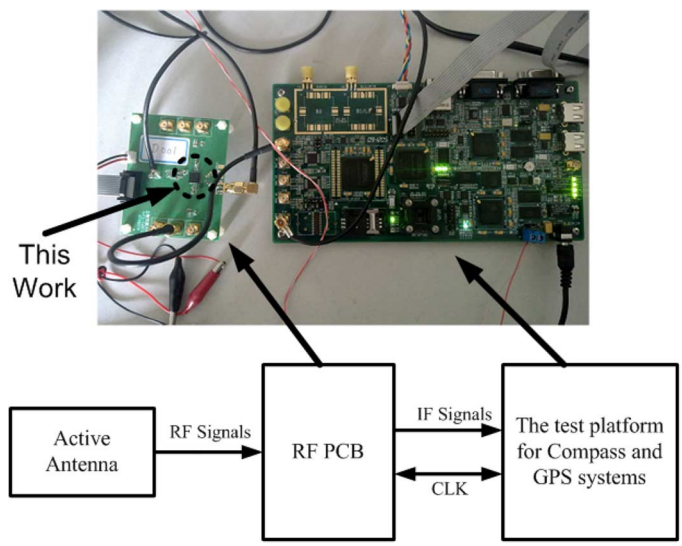

Fig. 21. Test bench of the GNSS RF receiver.

The performance comparison with the states-of-the-art is summarized in Table II. As can be seen, most performance of our proposed dual-channel multiband GNSS RF receiver is better than or as good as the state-of-the-art and it occupies the smallest active silicon area. The worse power consumption is partially because the CF is designed to provide 20-MHz BW,

TABLE III
SUMMARY OF RESULTS OF THE GNSS RECEIVER WITH THE PROPOSED CHIP

Mode	Band	Sat. Num.	IF/BW (MHz)	CNR (dB)	Pseudo Range (Meter)
GPS	L1	1	6.42/2	47.1	3001615 708
	L1	3	6.42/2	49.7	2622081 580
	L1	6	6.42/2	49.0	2705037 888
	L1	13	6.42/2	50.6	2786257 804
BD-2	B1	1	6.098/4	43.8	2585989 043
	B2	1	16.14/20	46.1	2584832 275

which needs larger gain BW of the Opamps, and thus, more power consumption. In addition, the 4-bit flash ADC and the wideband PLL and VCO also need more power consumption than the 2-bit ADC and the narrowband frequency synthesizer used in previous studies.

As shown in Fig. 21, a test-bench, which is composed of an active antenna, RF PCB, and GPS/compass test platform has been constructed to verify the systemic performances of the proposed RF chip. Due to the restricted platform, only the signals of GPS-L1, Compass-B1, and Compass-B2 can be processed in this test bench. The test results, as presented in Table III, indicated that the proposed RF chip can cooperate with the digital baseband to process GNSS signals very well.

VI. CONCLUSIONS

A dual-channel multiband RF receiver has been implemented for the next-generation GNSS in a 0.18-μm CMOS process. The RF receiver exhibits two independent signal channels for simultaneous reception of tri-mode all-band GNSS signals due to the reconfigurable RF front-end, complex BPF, and wideband frequency synthesizers. While drawing 25-mA current for a single channel from a 1.8-V supply, this RF receiver achieves a total NF of 2.5/2.7 dB at 1.2/1.57 GHz, an image rejection of 28 dB, a maximum voltage gain of 110 dB, a gain dynamic range of 73 dB, and an input-referred 1-dB CP of -58 dBm. The active die area for single channel of the receiver is 2.4 mm^2.

The proposed dual-channel multiband RF receiver can accommodate simultaneous reception of any two types of GNSS signals listed in Table I, which is desirable for better GNSS navigation accuracy and availability, while achieving better performance (die area, NF, gain dynamic range) than other state-of-the-art GNSS receivers. Moreover, some design efforts have been made to improve the receiver's robustness and position accuracy in the presence of interferences by utilizing the nonuniform 4-bit ADC and digital AGC loop to provide antijamming capability and optimized performance for the receiver.

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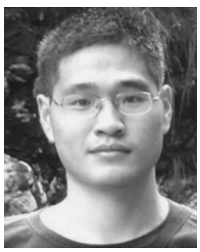

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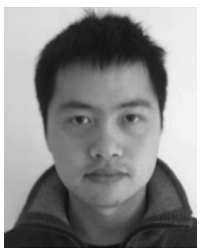

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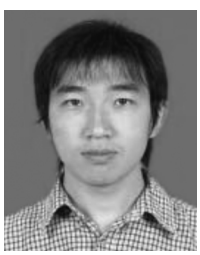

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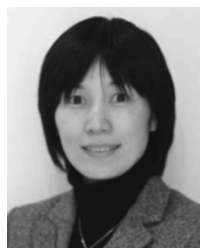

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