Design of Oversampled Sigma-Delta Data Converters

Chun-Hsien Su

中央大學電機系　蘇純賢

chunsu@ee.ncu.edu.tw

July, 2006

國立中央大學 電機工程學系
NATIONAL CENTRAL UNIVERSITY
DEPARTMENT OF ELECTRICAL ENGINEERING

OUTLINE

1. Fundamental of Data Conversion
2. Fundamentals of Sigma-Delta Data Converters
3. Switched-Capacitor Circuits
4. Circuit Implementation of ΣΔ Modulators
5. Design of High-Order Sigma-Delta Modulators
6. Design of ΣΔ Digital-to-Analog Converters
7. Conclusions

Data Converter Fundamentals

Chun-Hsien Su

中央大學電機系　蘇純賢

chunsu@ee.ncu.edu.tw

July, 2006

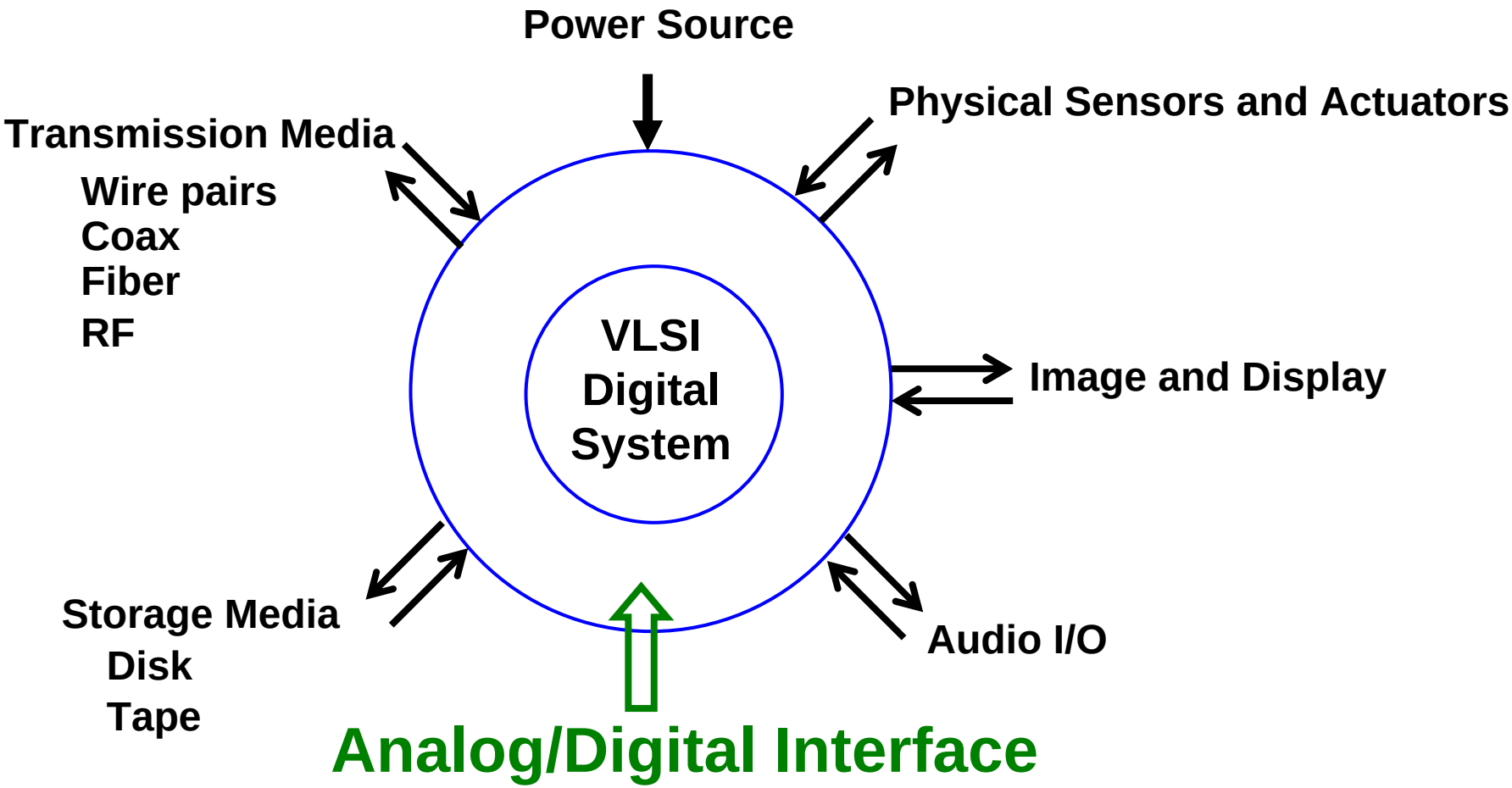
國立中央大學 電機工程學系
NATIONAL CENTRAL UNIVERSITY
DEPARTMENT OF ELECTRICAL ENGINEERING

Data Converter Fundamentals

1. Analog Signal Processing
2. Quantization Noise
3. Oversampling
4. Types of A/D Converters
5. Performance Metrics – Static and Dynamic
6. Sampling-Time Uncertainty

Analog Signal Processing

[Paul Gray, 1996]



Analog Signal Processing Functions

- **Amplification (Class-AB, audio amplifiers)**
- **Filtering (Switched-capacitor filters)**

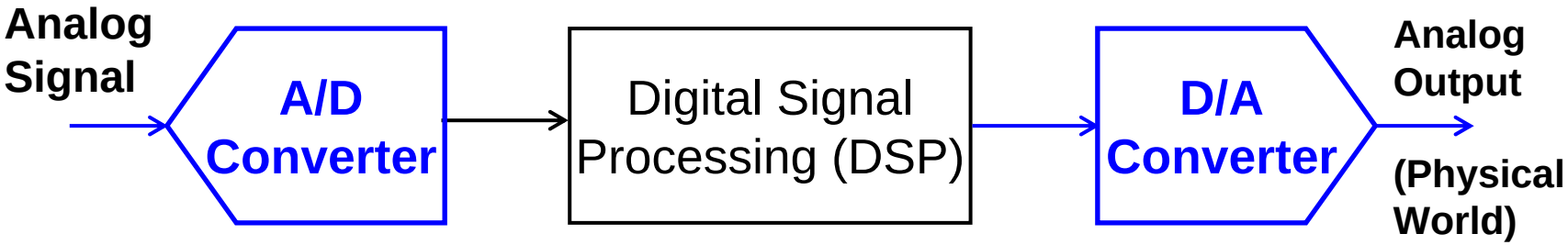
⇒ **Analog-to-digital conversion (serial, parallel, etc.)**

⇒ **Digital-to-analog conversion (serial, parallel, etc.)**

- **Power supply conditioning (Switching regulators)**

Modern Signal Processing Systems

Data Conversion in a DSP System:



Challenges in data converter design:

⇒ **Increased demand in resolution and bandwidth.**

⇒ **Performance limited by VLSI processes.**

Types of Data Converters

(1). Nyquist-Rate Data Converters

⇒ **Input–output one on one base on Nyquist Rate.**

⇒ **Problems: Difficulty in realizing anti-aliasing and reconstruction filters.**

⇒ **Practical: Operates at 1.5×~10× Nyquist Rate.**

(2). Oversampling Converters

⇒ **Output is much faster than input. (20× ~512×)**

⇒ **Signal-to-noise ratio (SNR) improved.**

⇒ **Anti-aliasing filter specs are relaxed.**

⇒ **Delta-Sigma = Oversampling + Noise shaping.**

ADC Categories

Amplitude conversion
- Integrating
- Successive Approximation
- Flash
- Algorithmic (or cyclic)
- Interpolation
- Folding
- Pipelined

Implementation
- Integrating
- Voltage Division
- Charge Redistribution
- Time-interleave

Frequency conversion
- Nyquist-rate
- Oversampled
- Sigma-Delta

Low-to-Medium Speed High Accuracy	**Medium Speed, Medium Accuracy**	**High Speed, Low-to-Medium Accuracy**
Integrating Oversampling	Successive approximation Algorithmic	Flash Two-step Interpolating Folding Pipelined Time-interleaved

DAC Categories

Implementation
- R-2R Ladder
- Voltage Division
- Charge Redistribution
- Current Steering

Frequency conversion
- Nyquist-rate
- Oversampled
- Sigma-Delta

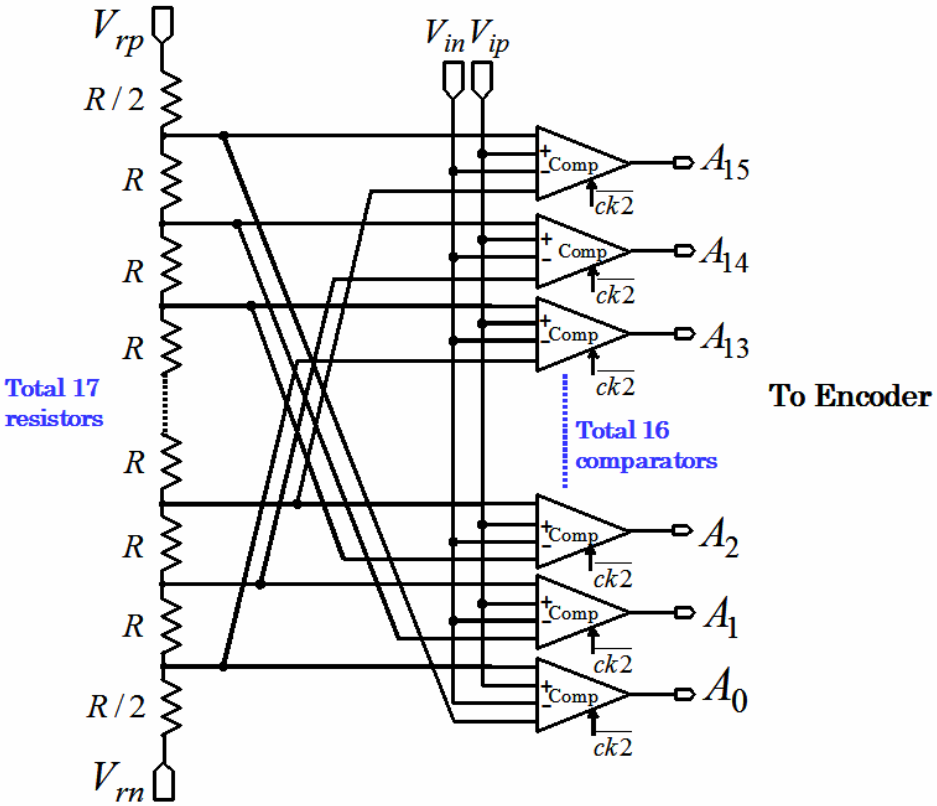
Amplitude conversion
- Flash
- Algorithmic (or cyclic)
- Pipelined

Coding scheme
- Binary
- Thermometer
- Segmented

DAC linearization technique
1. Trimming
2. Dynamic Element Matching
3. Pulse-Width Modulation
4. Self-Calibration

Types of ADCs – Nyquist-Rate ADCs

Flash ADC

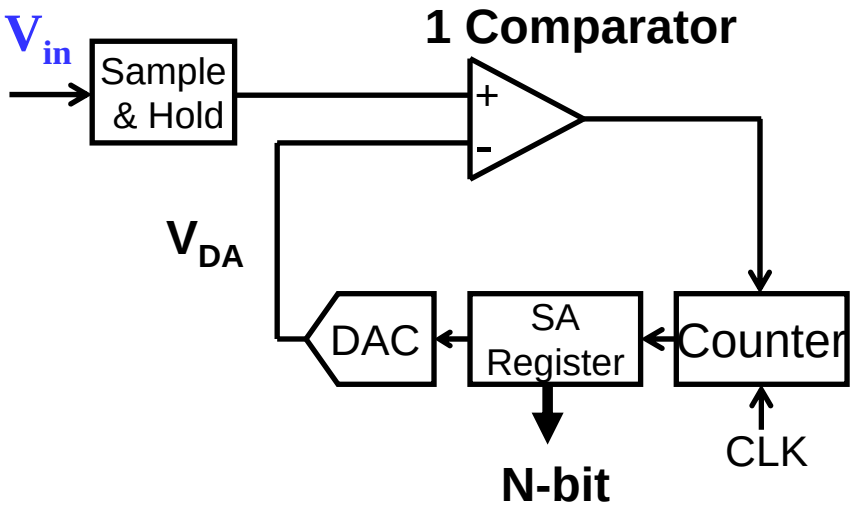


High Speed: 100's of MHz

Moderate resolution: 8-bit

Large circuit area

Successive Approximation (SA) ADC



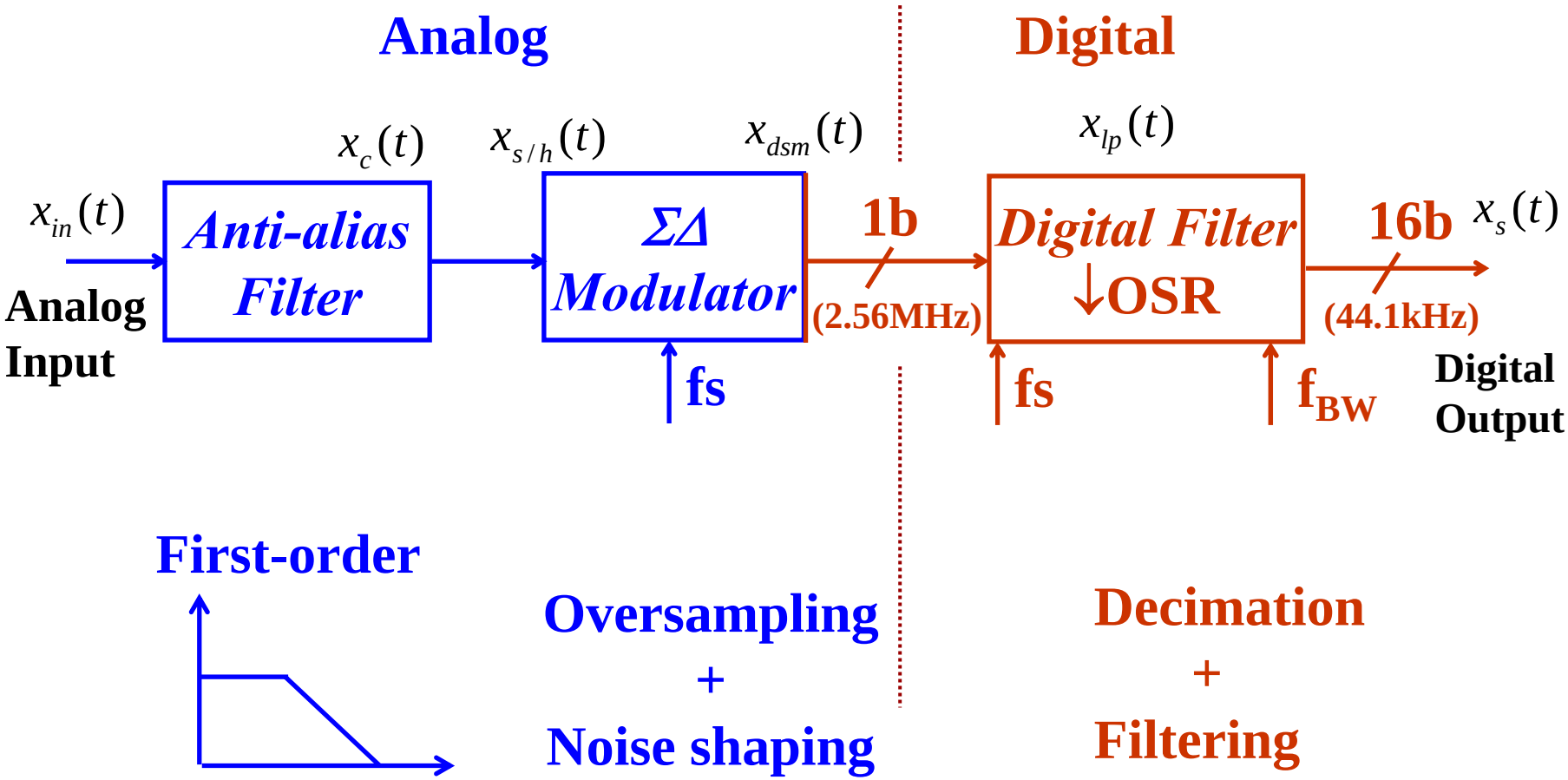
Low Speed: ~ kHz

High resolution: 14-bit

Small circuit area

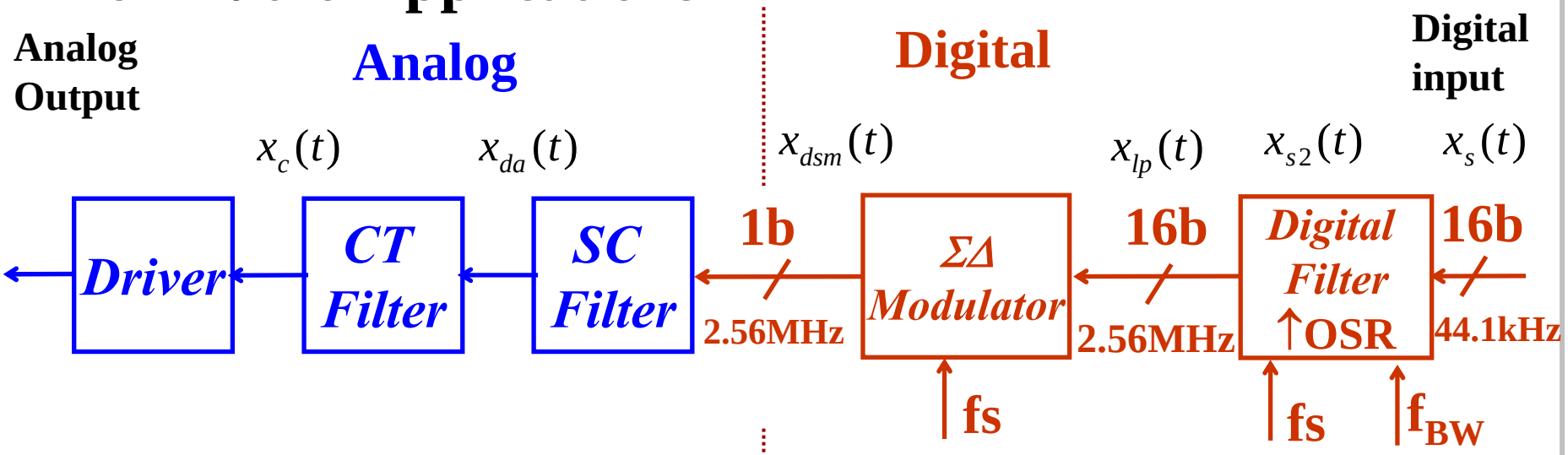
Oversampled Sigma-Delta ADC

For Audio Applications



Oversampled Sigma-Delta DAC

For Audio Applications



Class AB
Class D

SC Buffer (Direct Charge Transfer, DCT)

SC LPF

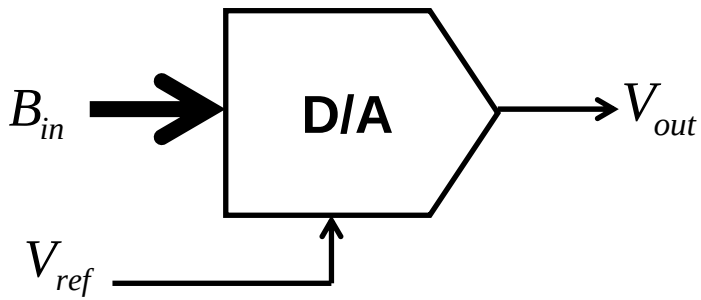
Oversampling + Noise shaping

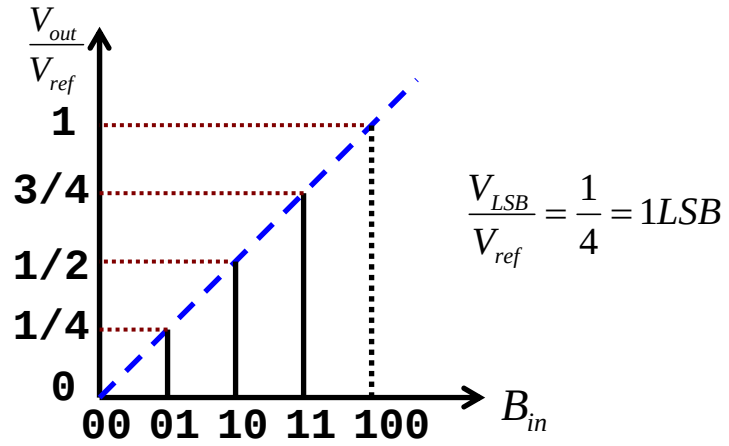
Intepolation + Filtering

⇒ Duality with ΣΔ ADC

Ideal D/A Converter

D/A Block





N-bit Input $B_{in} = \underline{b_1}2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + \underline{b_N} 2^{-N}$

MSB **LSB**

- **Unsigned: unipolar**
- **Signed**

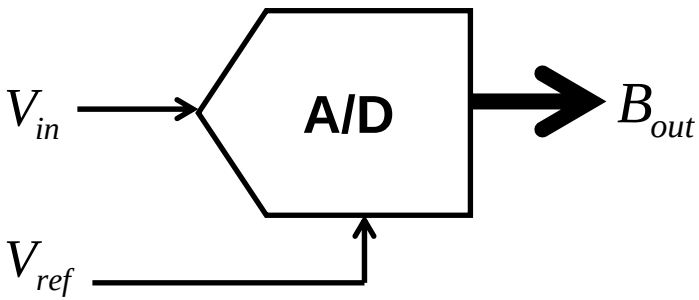
Output $V_{out} = \underline{V_{ref}}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + b_N 2^{-N}) = V_{ref} B_{in}$

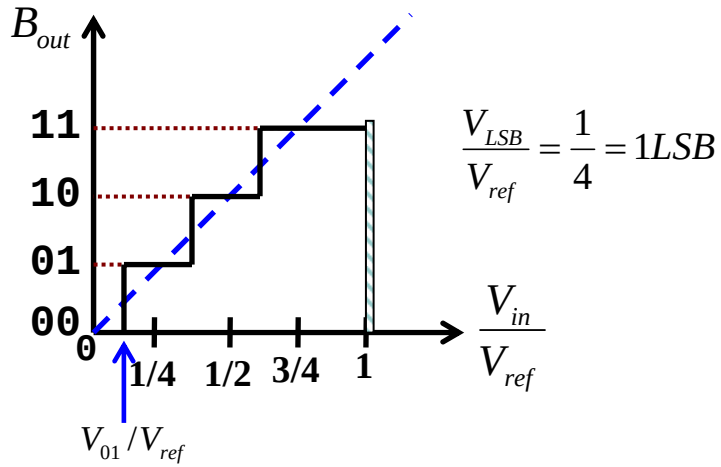
Reference voltage

$$\Rightarrow 1LSB = \frac{1}{2^N} \quad \Rightarrow V_{LSB} = \frac{V_{ref}}{2^N} \quad \Rightarrow V_{out} \begin{cases} \textbf{max} & V_{ref}(1 - \frac{1}{2^N}) \ (or\, V_{ref} - V_{LSB}) \\ \textbf{min} & 0 \end{cases}$$

Ideal A/D Converter

A/D Block





$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + b_N 2^{-N}) = V_{in} \pm V_X$$

$$\Rightarrow \quad -\frac{1}{2}V_{LSB} \le V_X \le \frac{1}{2}V_{LSB} \qquad \Rightarrow \quad V_X : \textbf{Quantization Error}$$

$\Rightarrow$ D/A no quantization error since output signals are well defined.

$\Rightarrow$ Transition voltage V_{ij} voltage that code changes from I to j.

$\Rightarrow$ Overload $V_X \ge \frac{1}{2}V_{LSB}$

ADC/DAC Performance Metrics

ADC:

Static Performance
- Gain
- Offset
- INL
- DNL
- Missing Code

Dynamic Performance
- SNR/SNDR/SFDR
- DR/SFDR
- THD
- Settling errors
- Sparking
- Sampling jitter
- Clock feedthrough

DAC:

Static Performance
- Gain
- Offset
- INL
- DNL
- Monotonicity

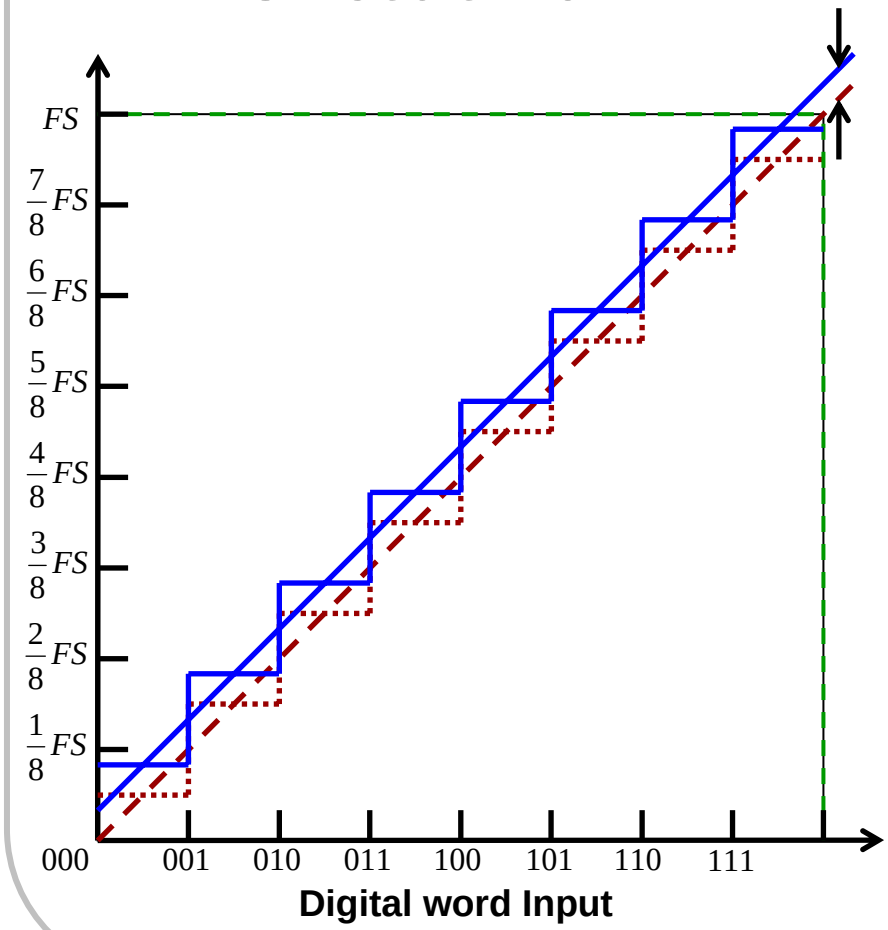
Dynamic Performance
- SNR/SNDR/SFDR
- DR
- THD
- Settling errors
- Code glitches
- Sampling jitter
- Clock feedthrough

ADC/DAC Performance Metrics – Static (I)

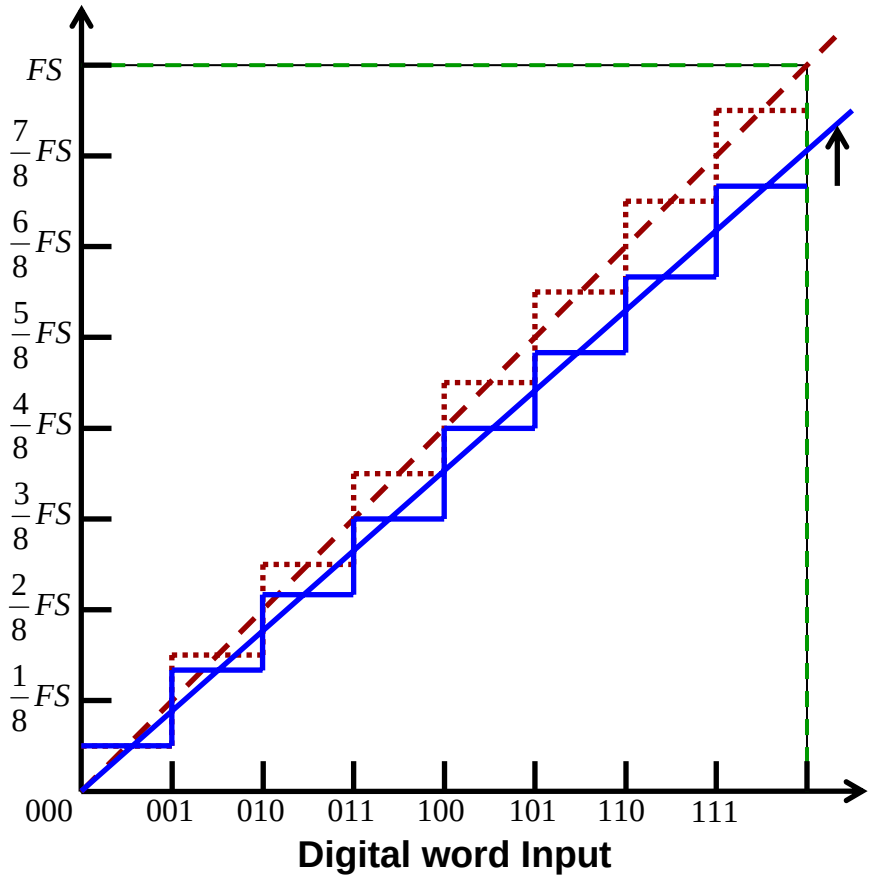
(1). Absolute Accuracy

[Allen, VLSI textbook, 1990]

- Offset error



- Gain error



Gain and Offset Errors Calculations

(1). DA Offset Error:

$$E_{offset(D/A)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0}$$

(2). AD Offset Error:

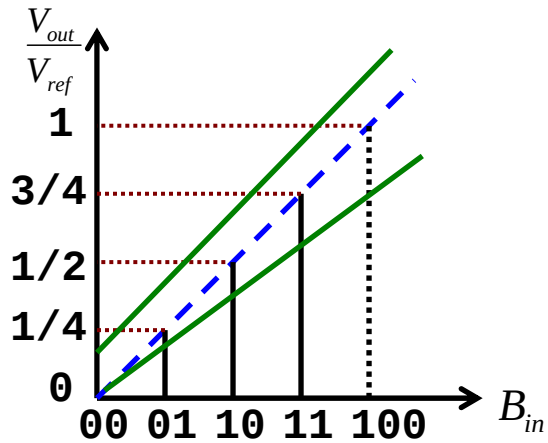
$$E_{offset(A/D)} = \frac{V_{0\ldots01}}{V_{LSB}} - \frac{1}{2}LSB$$

(3). DA Gain Error:

$$E_{gain(D/A)} = \left(\left.\frac{V_{out}}{V_{LSB}}\right|_{1\ldots1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0} \right) - \left(2^N - 1\right)$$

(4). AD Gain Error:

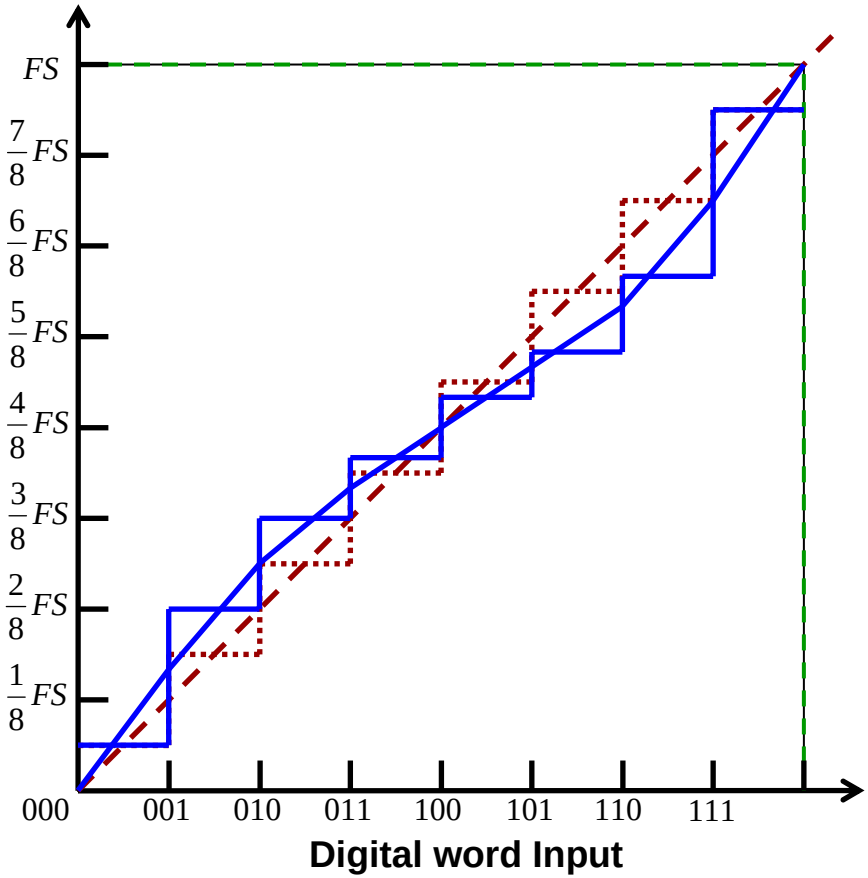
$$E_{gain(A/D)} = \left(\frac{V_{1\ldots1}}{V_{LSB}} - \frac{V_{0\ldots0}}{V_{LSB}} \right) - \left(2^N - 2\right)$$



ADC/DAC Performance Metrics – Static (II)

(2). Relative Accuracy - Nonlinearity

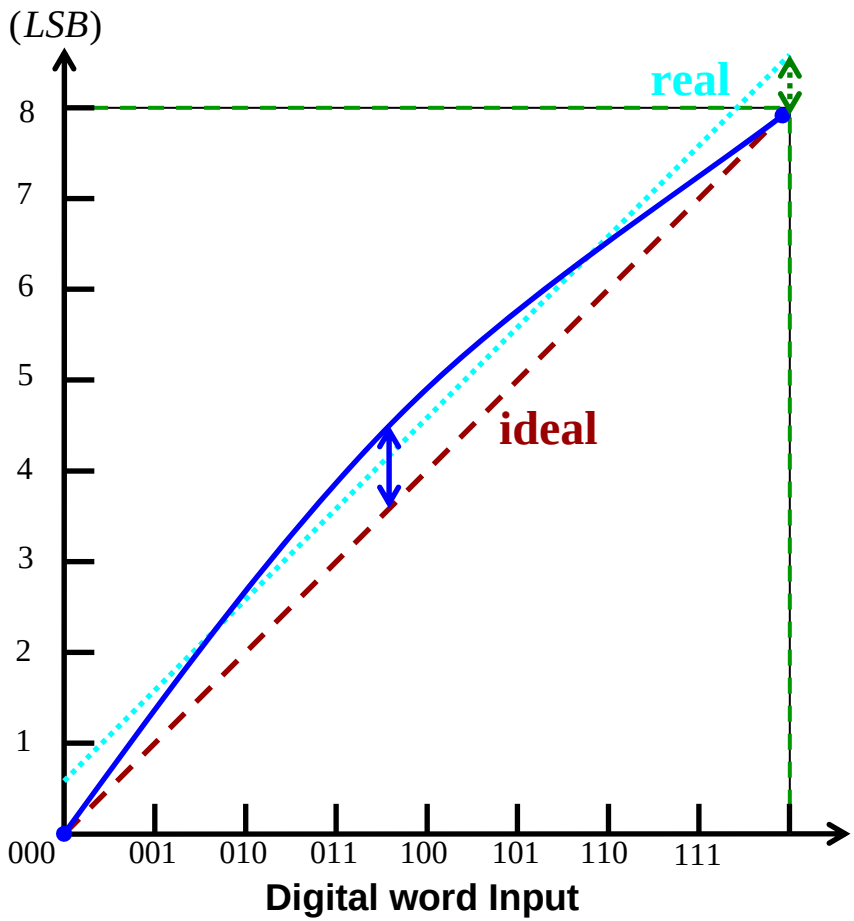
- INL error (represented in LSB)
- DNL error



Integral Nonlinearity (INL):
maximum deviation from the ideal transfer curve.

Differential Nonlinearity (DNL):
maximum deviation in analog step sizes away from 1LSB.

Best-Fit and Endpoint INLs



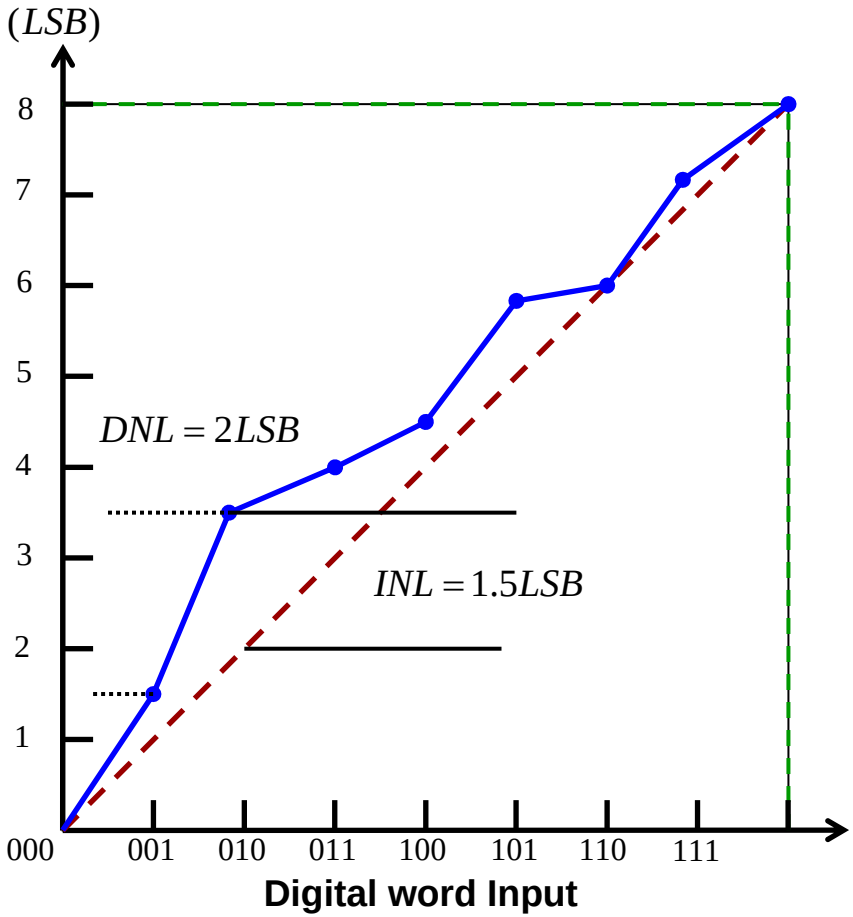
⟷ Endpoint INL

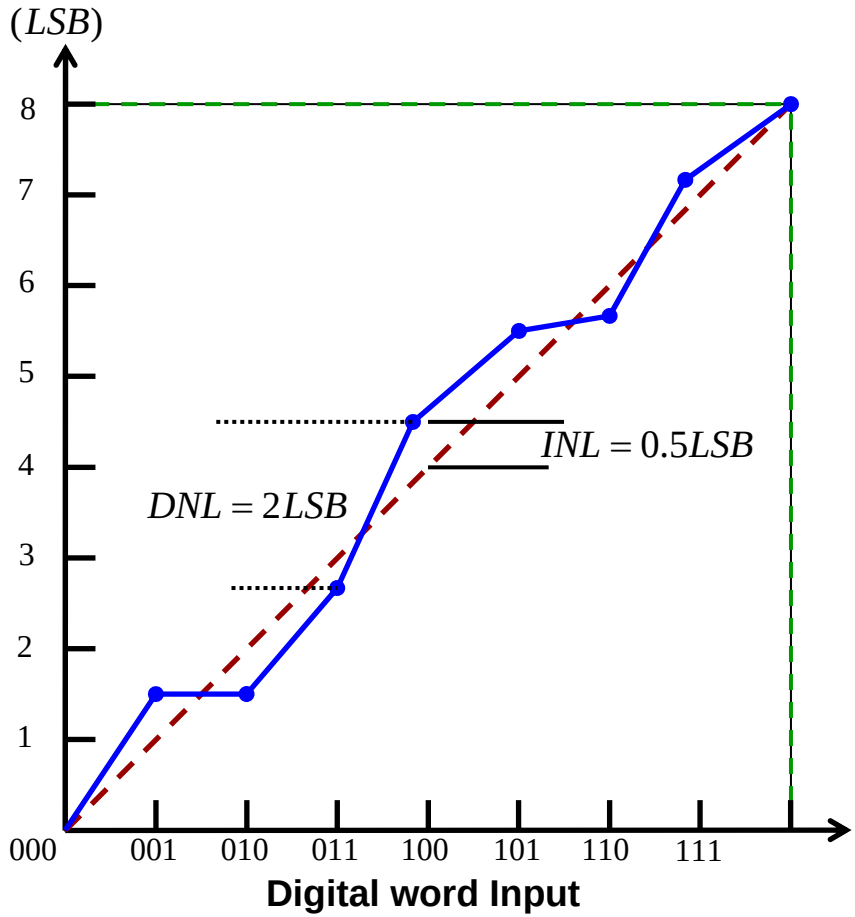
⇒ After remove the gain and offset error of the real transfer curve, find the max. difference from the ideal one.

⟷ Best-fit INL

⇒ Obtain the best-fit straight line of the real curve and then find its max. distance to the ideal one. We may use root-mean-square to fit the line.

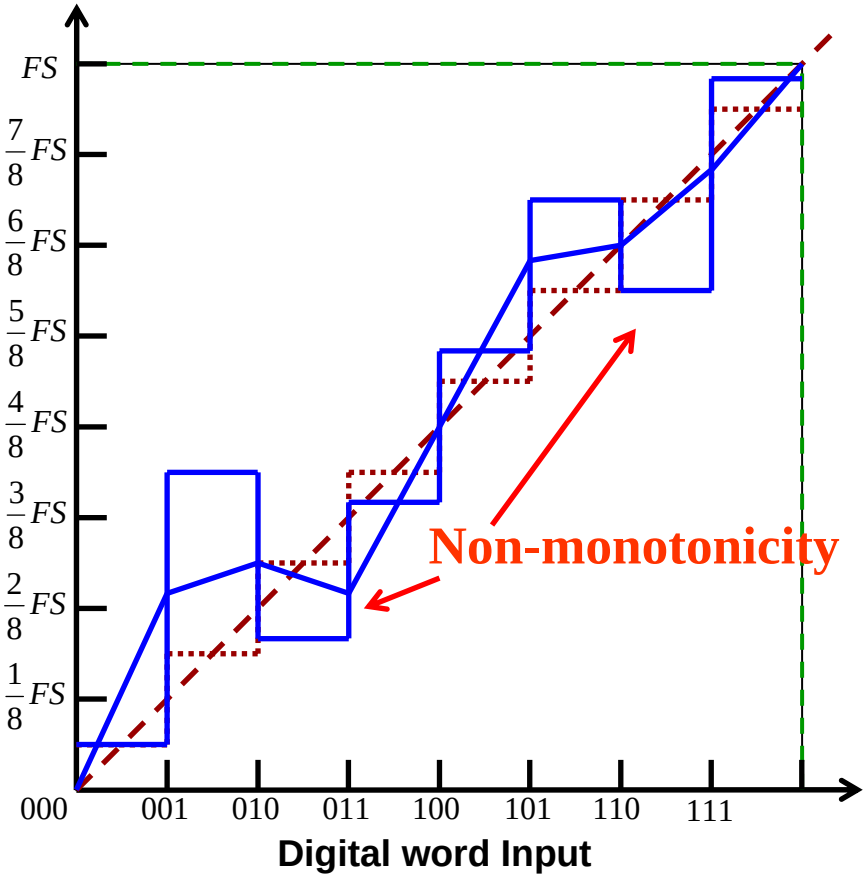
INL & DNL Examples





ADC/DAC Performance Metrics – Static (III)

(2). Relative Accuracy - Monotonicity



Monotonic: output increases as the input increases. ⇒ Real transfer curve slope ≥ 0.

DNL < 1LSB : monotonic

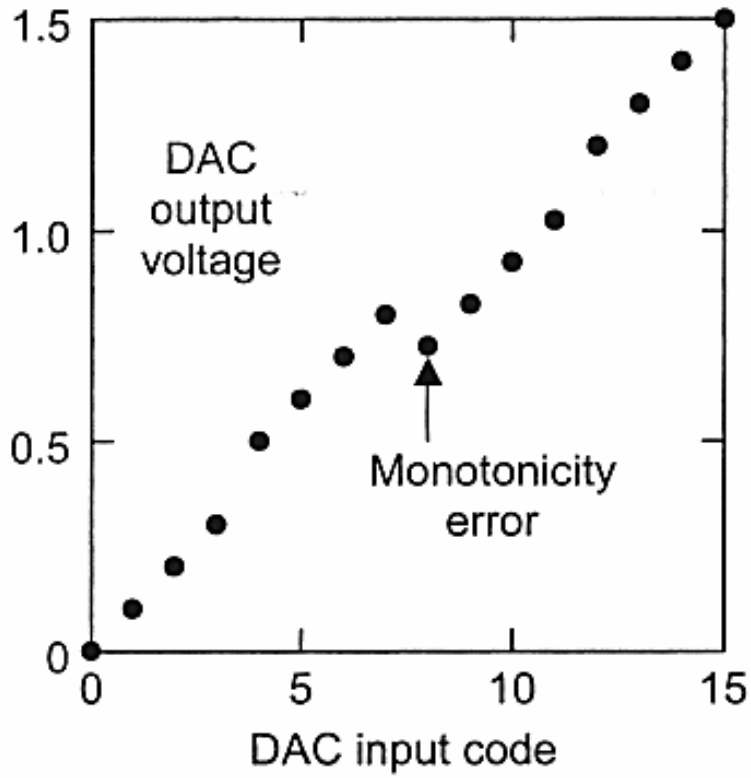
DNL >1LSB, INL <0.5LSB : monotonic (?)

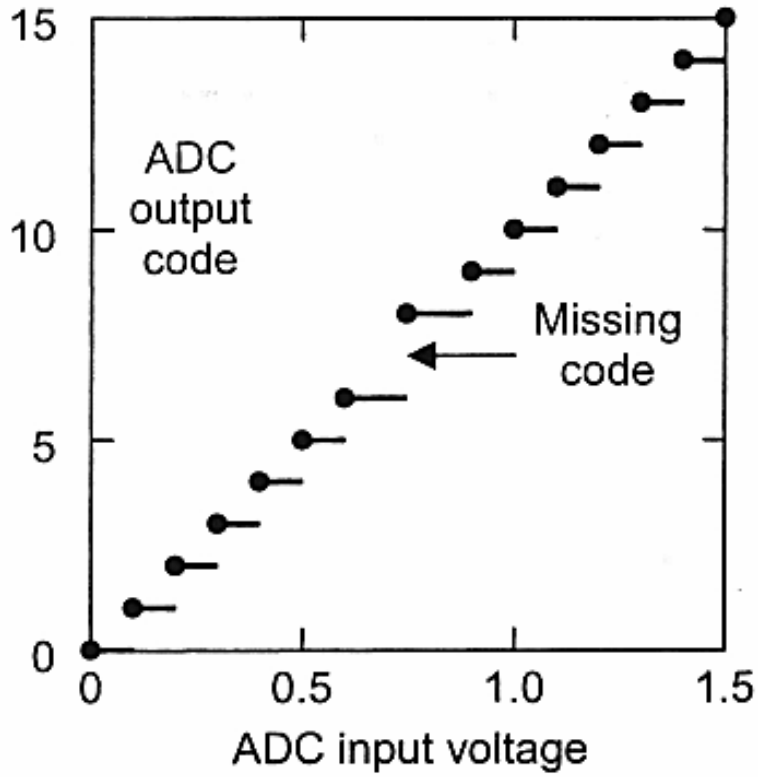
Monotonic: For D/A

Missing code: For A/D

Monotonicity and Missing Code

Monotonicity Errors in DACs and Missing Codes in ADCs





Example

Consider a 3-bit D/A converter in which Vref=4V, with the following measured voltage values:

{0.011 : 0.507 : 1.002 : 1.501 : 1.996 : 2.495 : 2.996 : 3.491}

1. 1LSB $V_{ref} / 2^3 = 0.5V$

2. Offset error $E_{offset(D/A)} = \frac{11mV}{0.5V} = 0.022LSB$

Gain error $E_{gain(D/A)} = \left(\frac{3.491}{0.5} - \frac{0.011}{0.5} \right) - \left(2^3 - 1\right) = -0.04LSB$

3. Remove gain and offset errors

{0.0 : 0.998 : 1.993 : 2.997 : 3.993 : 4.997 : 6.004 : 7}

INL error {0 : -0.002 : -0.007 : -0.003 : -0.007 : -0.003 : 0.004 : 0}

DNL error {-0.002 : -0.005 : 0.004 : -0.004 : 0.007 : -0.004}

4. Relative accuracy: max INL=0.007LSB=3.5mV $\Rightarrow$ N=10.2bit

ADC/DAC Performance Metrics – Dynamic (I)

Distortion Metric	Expression	
	(V/V)	(dB)
Signal to 2nd Harmonic Distortion (S/2nd)	$\frac{S}{H_2}$	$20\ \log_{10}\left(\frac{S}{H_2}\right)$
Signal to 3rd Harmonic Distortion (S/3rd)	$\frac{S}{H_3}$	$20\ \log_{10}\left(\frac{S}{H_3}\right)$
Signal to Total Harmonic Distortion (S/THD)	$\frac{S}{\sqrt{H_2^2+H_3^2+H_4^2+H_5^2+\cdots}}$	$20\ \log_{10}\left(\frac{S}{\sqrt{H_2^2+H_3^2+H_4^2+H_5^2+\cdots}}\right)$
Signal-to-noise (S/N)	$\frac{S}{N}$	$20\ \log_{10}\left(\frac{S}{N}\right)$
Signal to Total Harmonic Distortion plus Noise (S/THD+N)	$\frac{S}{\sqrt{H_2^2+H_3^2+H_4^2+H_5^2+\cdots+N^2}}$ or $\frac{S}{\sqrt{(\text{total signal RMS})^2-S^2}}$	$20\ \log_{10}\left(\frac{S}{\sqrt{H_2^2+H_3^2+H_4^2+H_5^2+\cdots+N^2}}\right)$ or $20\ \log_{10}\left(\frac{S}{\sqrt{(\text{total signal RMS})^2-S^2}}\right)$

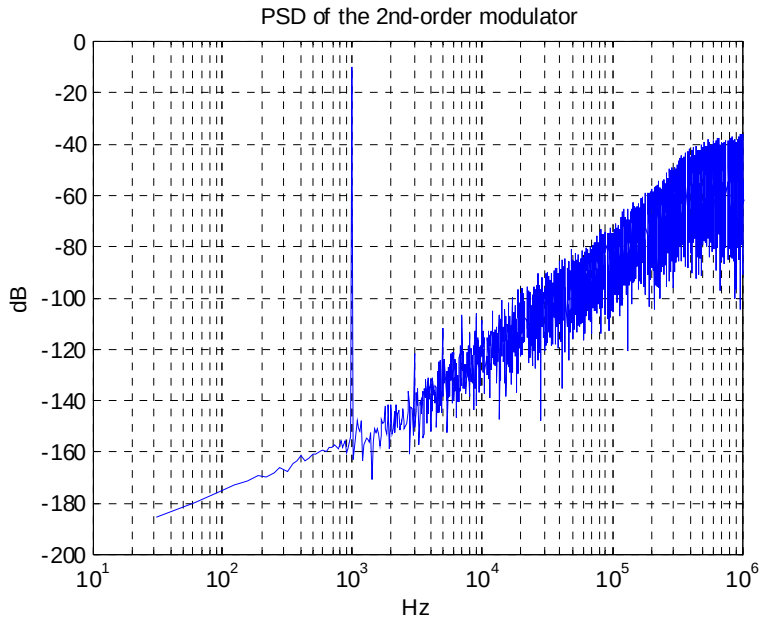
SNR

S(N+THD)R

ADC/DAC Performance Metrics – Dynamic (II)

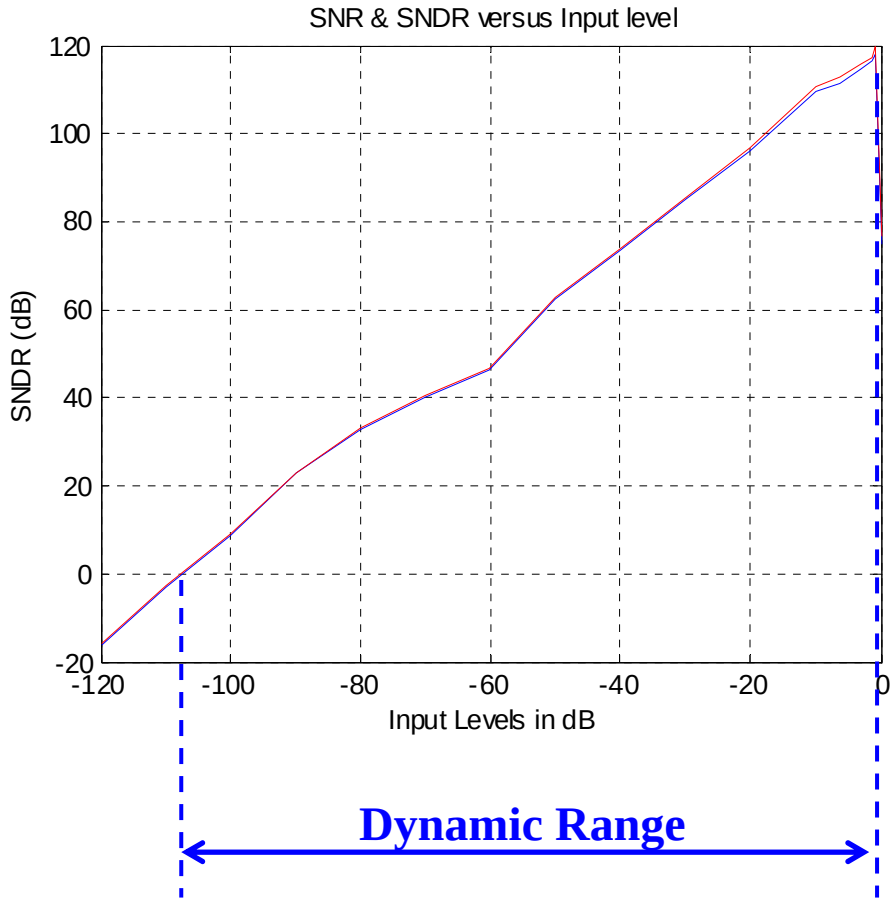
SNR and Dynamic Range (DR)

Power spectrum Density



SNR, SNDR, THD, SFDR

Input level versus SNR plot



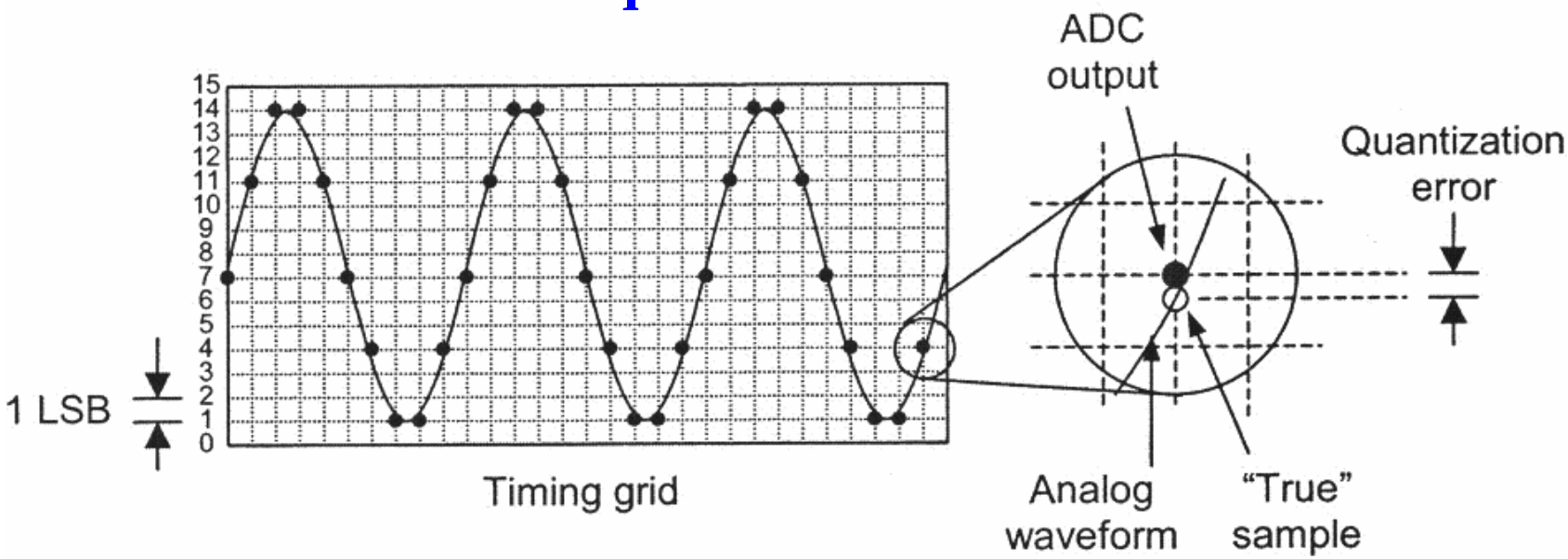
Quantization Effects (I)

– Noise introduced by an ADC

(1). Quantization noises

(2). Circuit related noise (thermal noise, shot noise,…)

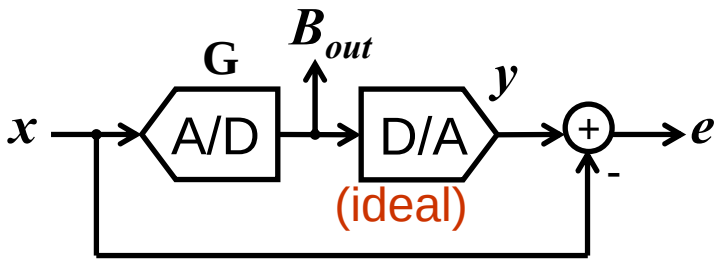
– In a perfectly designed and manufactured ADC, the majority of the noise will be the quantization noises.



– A N-bit ADC with full-scale analog input range of FS has a corresponding LSB step size of $V_{LSB}=FS/(2^N-1)$.

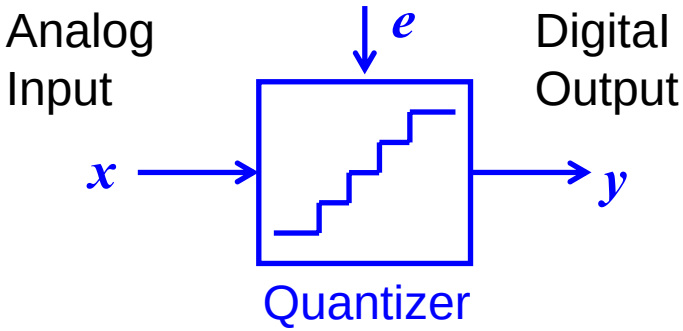
Quantization Effects (II)

Quantization Noise Model



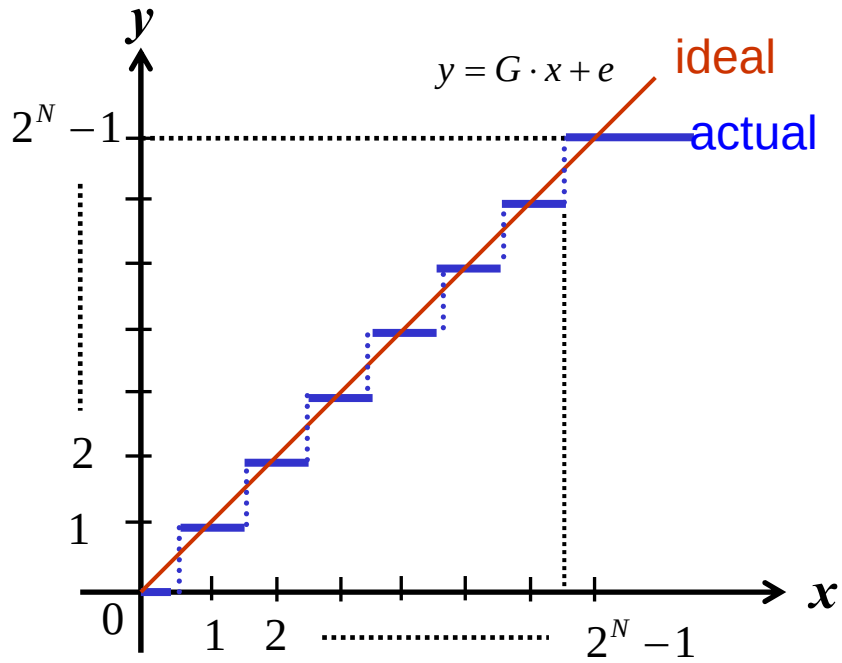
$$\Rightarrow V_e = V_y - V_x$$

$$\Rightarrow V_y = V_x + V_e$$



Output = Input + quantization noise

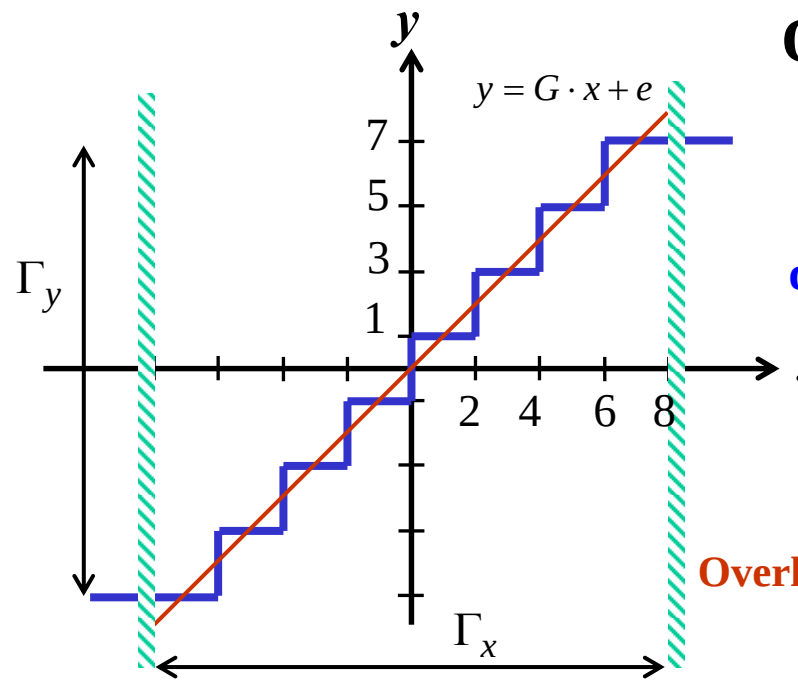
Transfer Curve



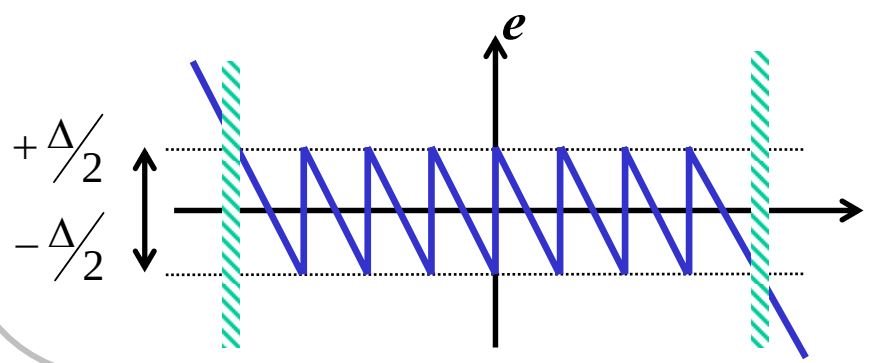
Definition of Quantization

N-bit Uniform quantization

[IEEE, 1992]



Overload



Quantization characteristics curve

$$y = G \cdot x + e$$

quantization gain　　quantization error

Quantization bit number N

Quantization space $\Delta = \dfrac{\Gamma_y}{2^N - 1}$

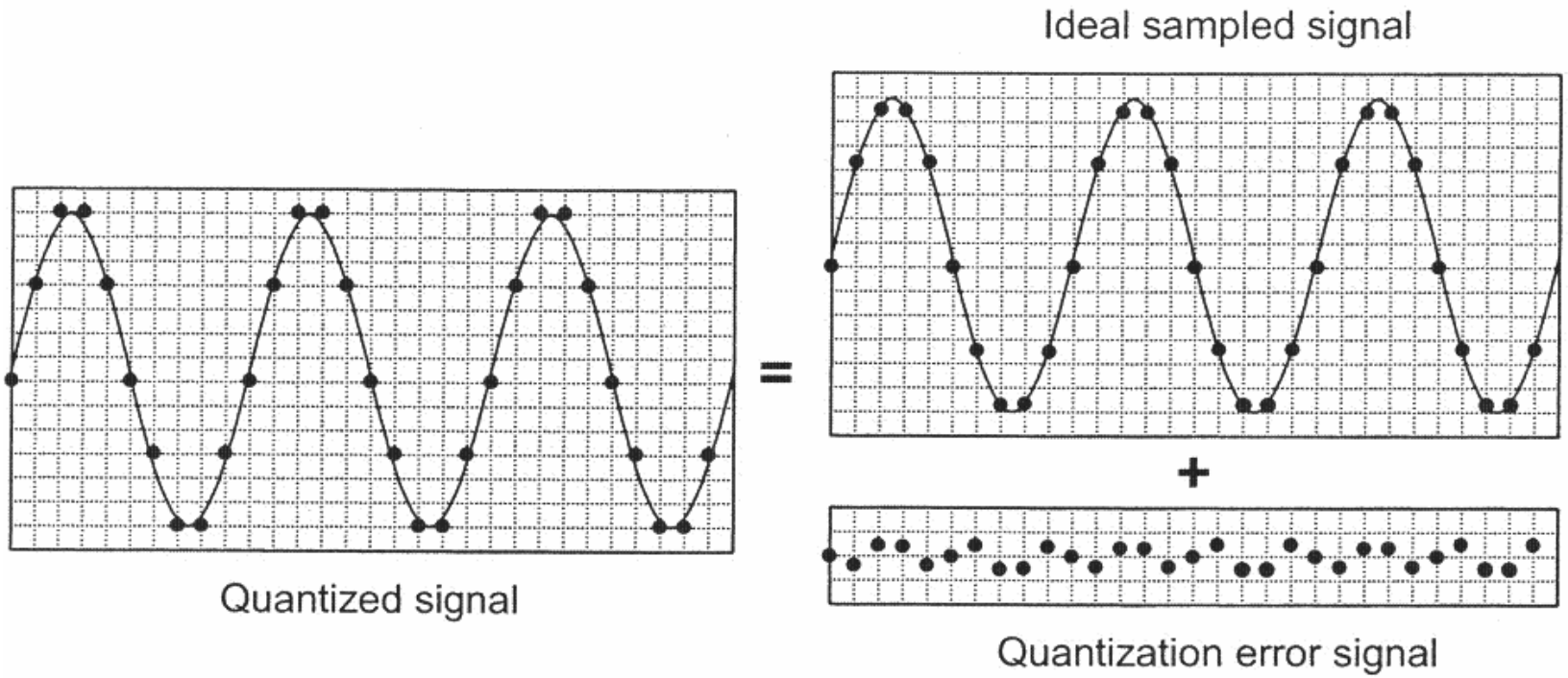
Least significant bit (LSB) $V_{LSB} = \Gamma_x / 2^N$

Quantization gain $G = \dfrac{\Delta}{LSB} = \dfrac{\Gamma_y \cdot (2^N)}{\Gamma_x \cdot (2^N - 1)}$

Quantization error boundary $\pm \Delta/2$

Quantization Effects (III)

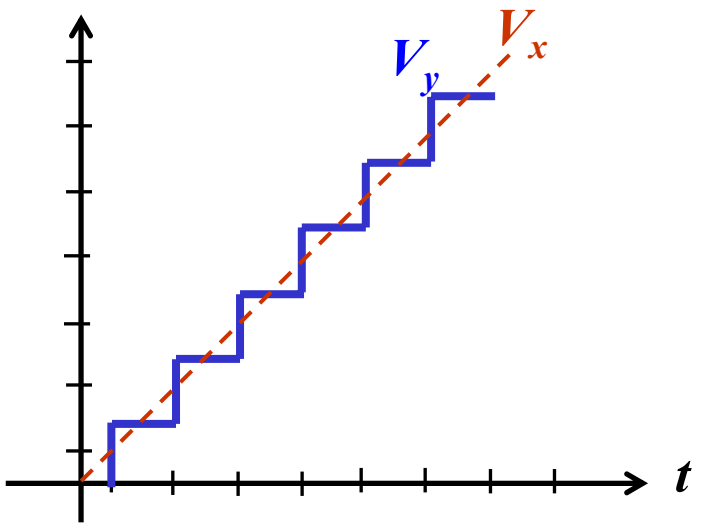
Quantized signal = Ideal sampled signal+ Quantization error signal

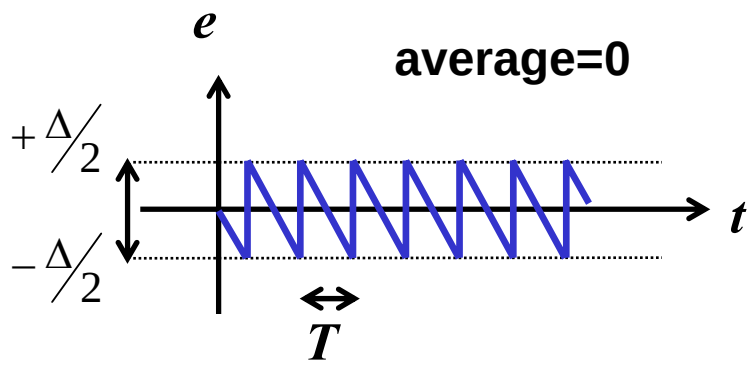


- **Quantization error of a random input signal exhibits a uniform probability density over ±½LSB.**
- **The ideal quantization error sequence v_q resembles random sequence having: $v_{q\text{-}average} = 0$ and $v_{q-RMS} = V_{LSB} / \sqrt{12}$**

Determine Quantization Noise (I)

Deterministic Approach: Input as a ramp function





$\Rightarrow$ **Quantization noise power (rms value)**

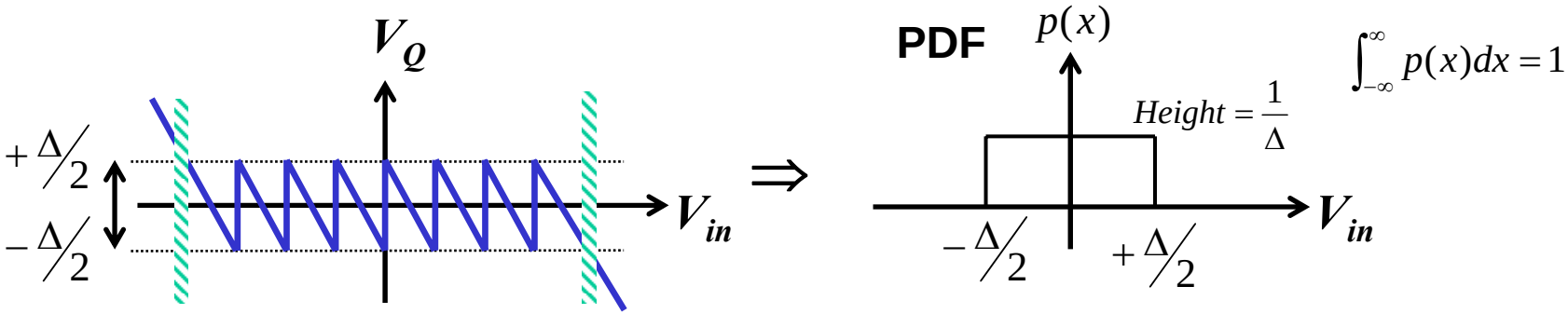
$$V_{Q(rms)}^2 = \frac{1}{T}\int_{-T/2}^{T/2} V_Q^2 dt = \frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2 \left(\frac{-t}{T}\right)^2 dt = \frac{\Delta^3}{T^3}\left(\frac{t^3}{3}\right)_{-T/2}^{T/2} = \frac{\Delta^2}{12}$$

$$\frac{V_{LSB}^2}{12}$$

Determine Quantization Noise (II)

Stochastic Approach: Input as a random variable

White noise approximation : if the quantizer input keeps busy and changes randomly between samples, the quantization error can be treated as an additive white noise. Under such conditions the generated white noise (quantization noise) has a uniformly-distributed probability density function (pdf) lying in the range of $\pm V_{LSB}/2$ statistically.

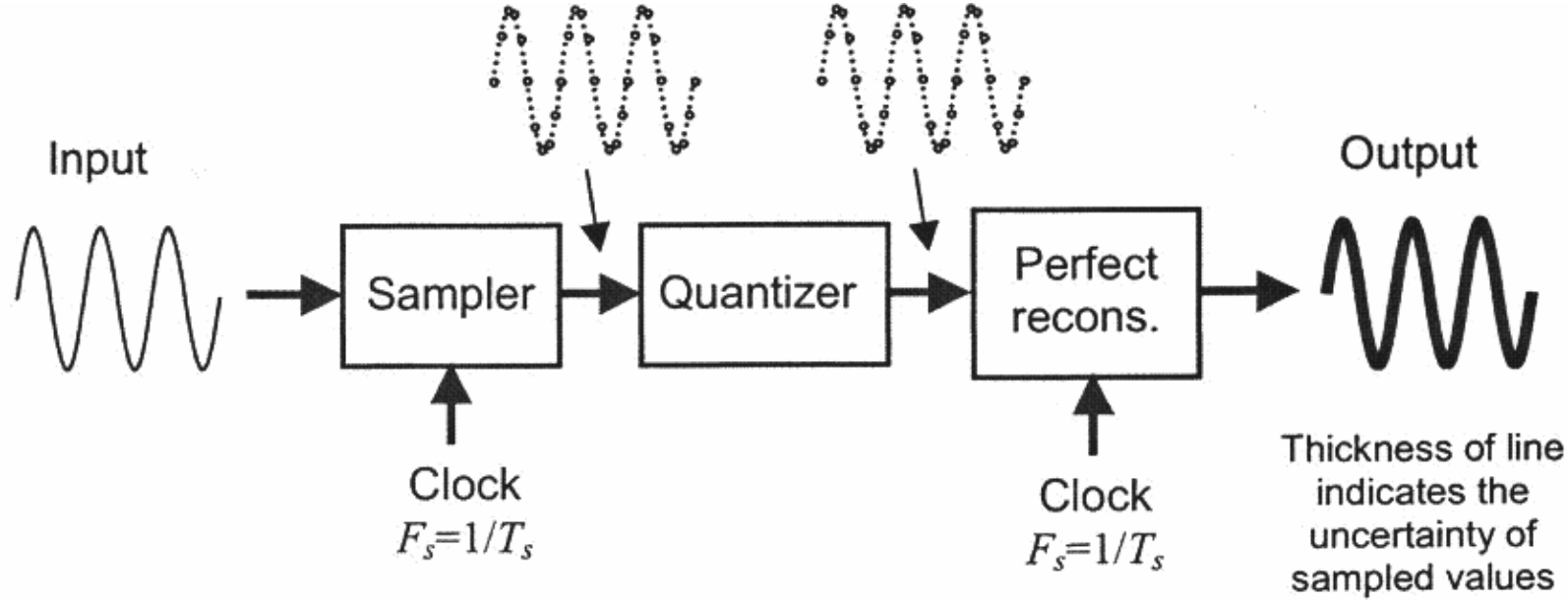


$$\Rightarrow V_{Q(avg)}^2 = \int_{-\infty}^{\infty} x \cdot p(x)dx = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} x dx = 0 \qquad (\Rightarrow \textbf{avergae=0})$$

$$\Rightarrow V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot p(x)dx = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} x^2 dx = \frac{\Delta^2}{12} \qquad [\Rightarrow \textbf{same as (I)}]$$

Performance Enhancement

– **Signal processing with a quantization operation**



– **Quantization error can be reduced using an ADC with more bits of resolution.**

⇒ **Adding an extra bit of ADC resolution reduces the size of each LSB by ½.**

⇒ **Reducing the RMS value by a factor 2 (or 6dB).**

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) Definition:

(With white input)

$$SNR = 10\log\left(\frac{P_{in}}{P_Q}\right) = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(2^N\right) = 6.02N(dB)$$

For a sinusoidal input signal $x(t)=A\sin(\omega t)$ to be quantized by a b-bit quantizer. Assume A is the full scale amplitude of the system, what is its SNR?

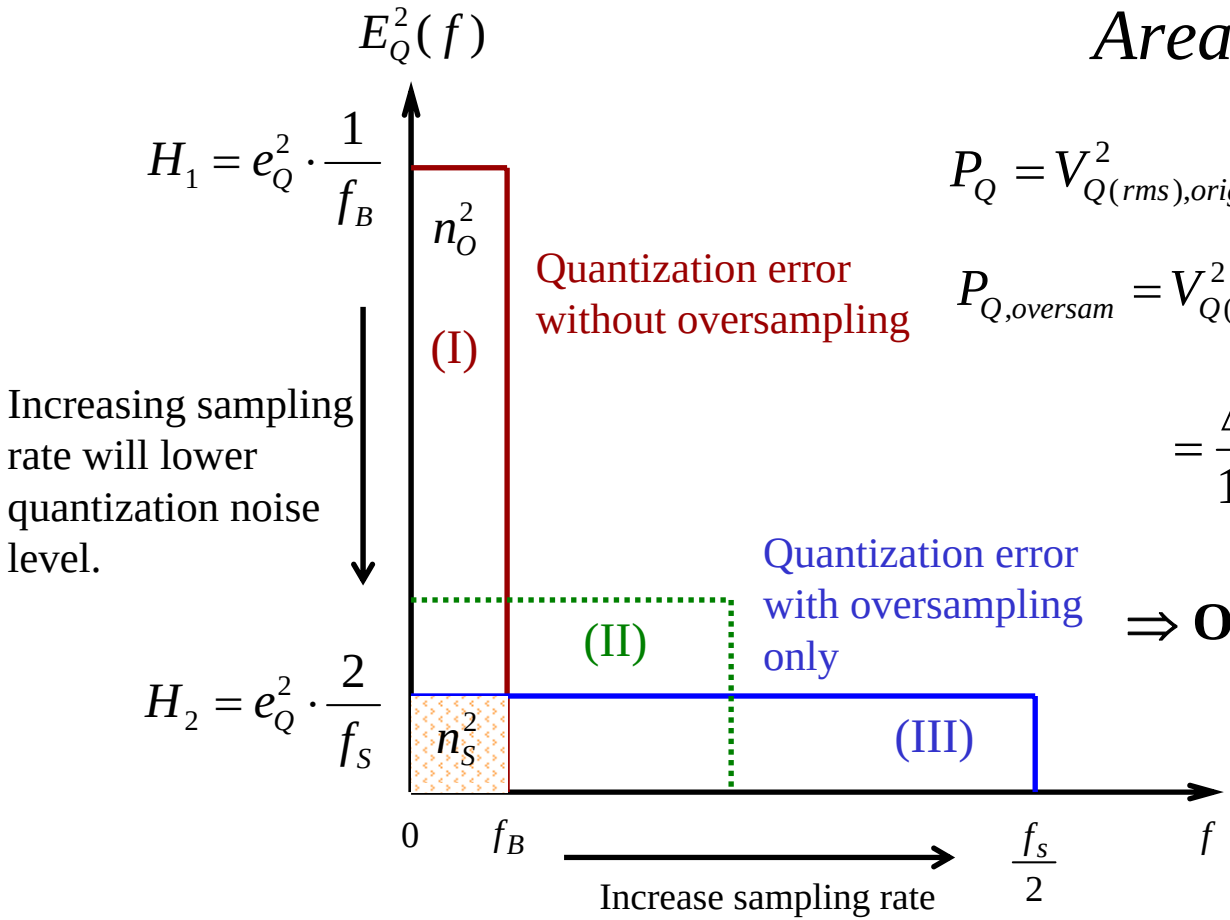
(1). Input signal power: $P_{in(rms)} = \frac{A^2}{2}$

(2). Quantization space: $V_{LSB} = \frac{2 \cdot A}{2^b}$

(3). Quantization noise power: $P_{Q(rms)} = V_{Q,(rms)}^2 = \frac{V_{LSB}^2}{12}$

$$SNR = 10\log\left(\frac{P_{in}}{P_Q}\right) = 10\log\left(\frac{A^2/2}{\Delta^2/12}\right) = 10\log\left(3 \cdot 2^{2b-1}\right) = 6.02b + 1.761(dB)$$

Oversampling to Increase SNR



$$Area_I = Area_{III}$$

$$P_Q = V_{Q(rms),orig}^2 = \frac{\Delta^2}{12}$$

$$P_{Q,oversam} = V_{Q(rms),orig}^2 \cdot \frac{2f_B}{f_S} = \frac{\Delta^2}{12} \cdot \frac{2f_B}{f_S}$$

$$= \frac{\Delta^2}{12} \cdot \frac{1}{OSR}$$

$\Rightarrow$ **Oversampling ratio (OSR)**

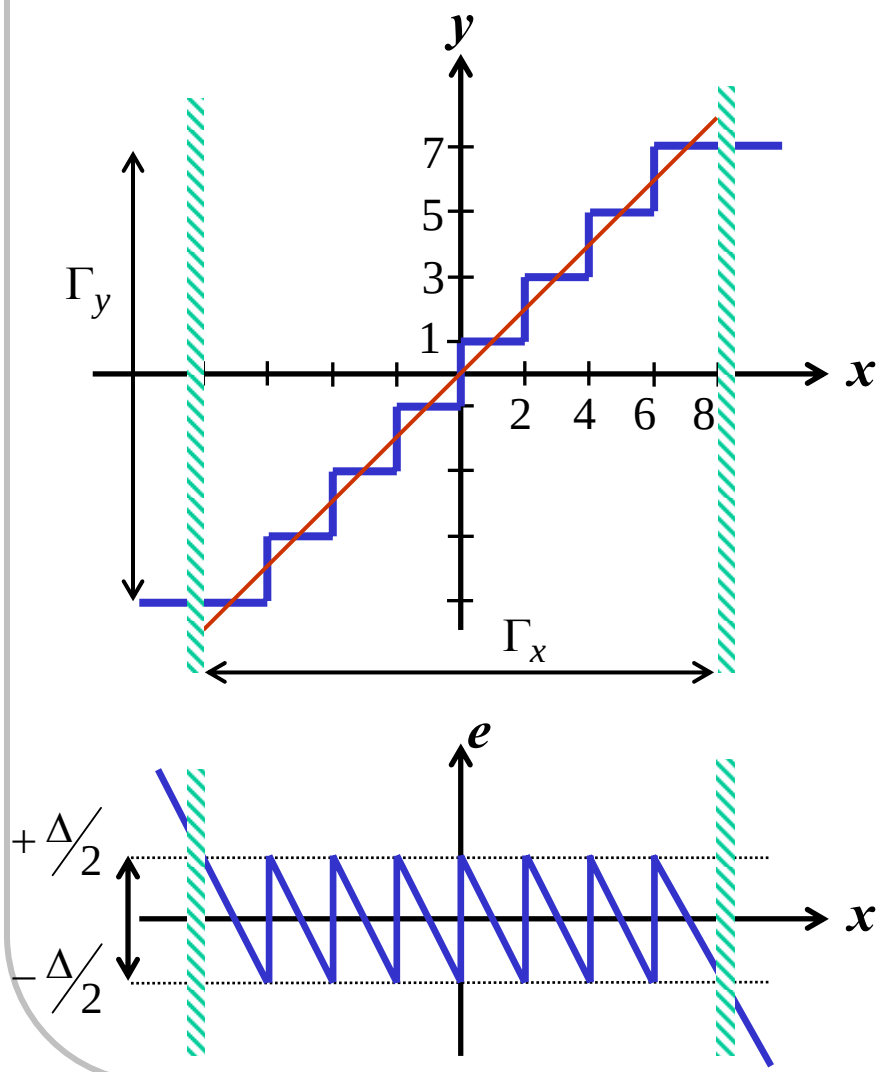
$$OSR = \frac{n_O^2}{n_S^2} = \frac{f_S}{2f_B}$$

$$SNR = 10\log\left(\frac{P_{in}}{P_Q}\right) = 6.02b + 1.761 + 10\log(OSR)$$

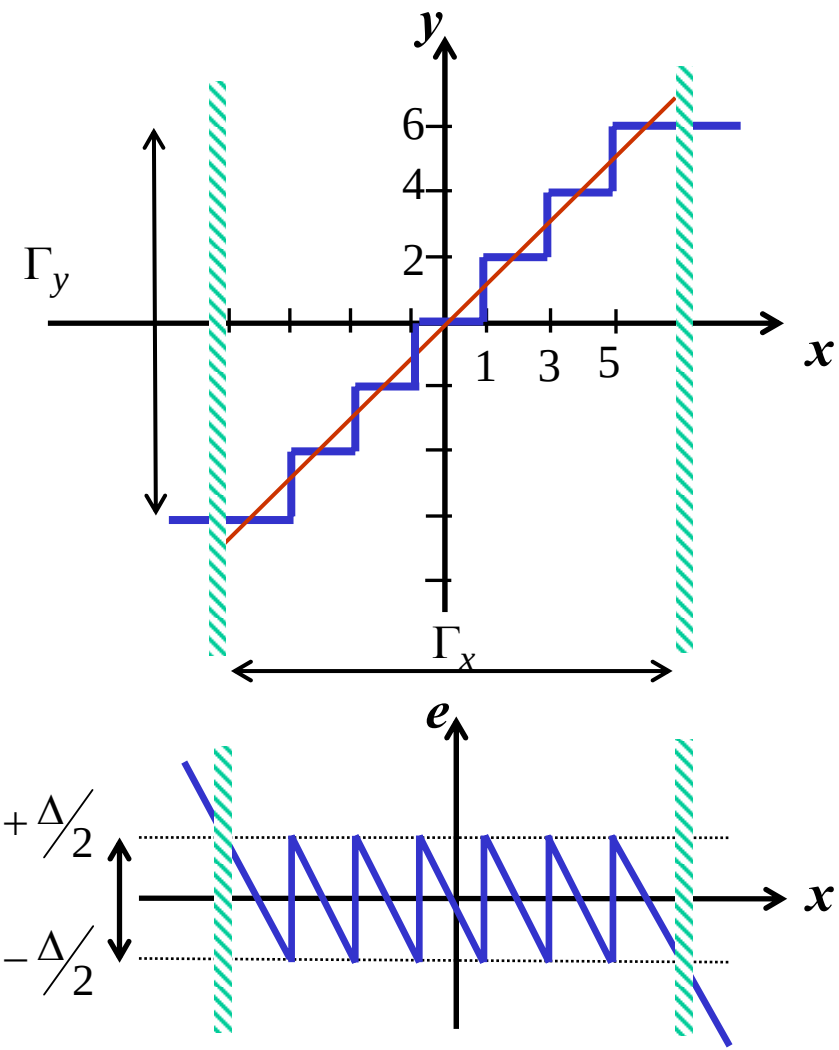
$\Rightarrow$ Each doubling OSR increases SNR by 3dB.

Midrise and Midtread Quantizers

M-step Midrise (M:even)

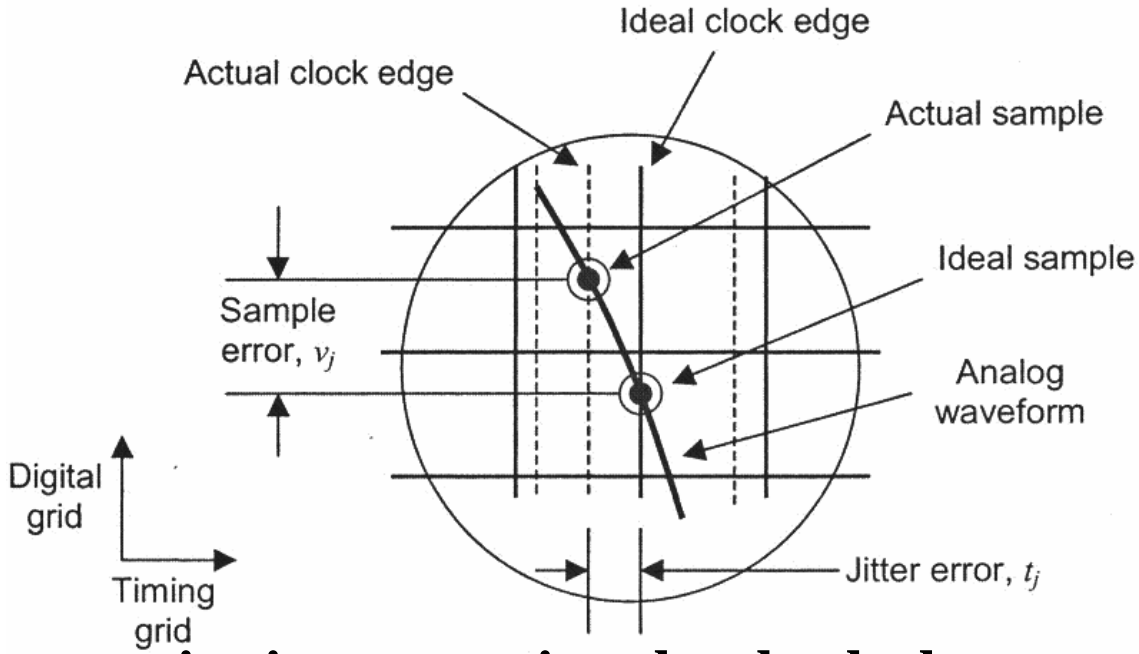


M-step Midtread (M:odd)



Sampling Jitter (I)

– **Jitter is the error in the placement of each clock edge controlling the timing of each ADC or DAC.**



– **The jitter noise is proportional to both the magnitude of the jitter and the slope of the signal at each sampled point.**

⇒ The RMS value of the jitter induced error is

$$v_{j-RMS} = \sqrt{2}\pi A_0 f_0 t_{j-RMS}$$

t_{j-RMS} : **Timing jitter**

Sampling Jitter (II)

Mathematical deduction:

– Let t_j be a random timing variable

Due to the nature of t_j, $v[n]$ is now a random variable as well

– Assume $v(t) = A\sin(2\pi f_0 nT_s)$

$$v[n] = v(t)\big|_{t=nT_s} = A_0 \sin(2\pi f_0 (nT_s + t_j))$$

$$= A_0 \sin(2\pi f_0 nT_s)\cos(2\pi f_0 t_j) + A_0 \cos(2\pi f_0 nT_s)\sin(2\pi f_0 t_j)$$

$$\approx A_0 \sin(2\pi f_0 nT_s) + A_0 2\pi f_0 t_j \cdot \cos(2\pi f_0 nT_s)$$

$$[\because t_j << T_s, \text{ and when } x \text{ is small}, \sin(x) = x, \cos(x) = 1]$$

– The error in the sample due to jitter, denoted as v_j , is

$$v_j[n] = A_0 2\pi f_0 t_j \cdot \cos(2\pi f_0 nT_s) = \left[\frac{dv(t)}{dt}\bigg|_{t=nT_s}\right] \cdot t_j$$

Jitter-induced error $\Rightarrow$ $v_{j-RMS} = \frac{1}{\sqrt{2}} 2\pi A_0 f_0 t_{j-RMS} = \sqrt{2}\pi A_0 f_0 t_{j-RMS}$

Sampling Jitter Effects for ADC

– **What is the maximum tolerable jitter allowable based on the ADC's speed and resolution?**

⇒ **Assume 1-LSB upper limit of jitter-induced noise**

$$v_{j-RMS} = \sqrt{2}\pi A_0 f_0 t_{j-RMS} < 1\,LSB = \frac{FS}{2^D - 1} \quad \Rightarrow t_{j-RMS} < \frac{FS}{\sqrt{2}\pi A_0 f_0 (2^D - 1)}$$

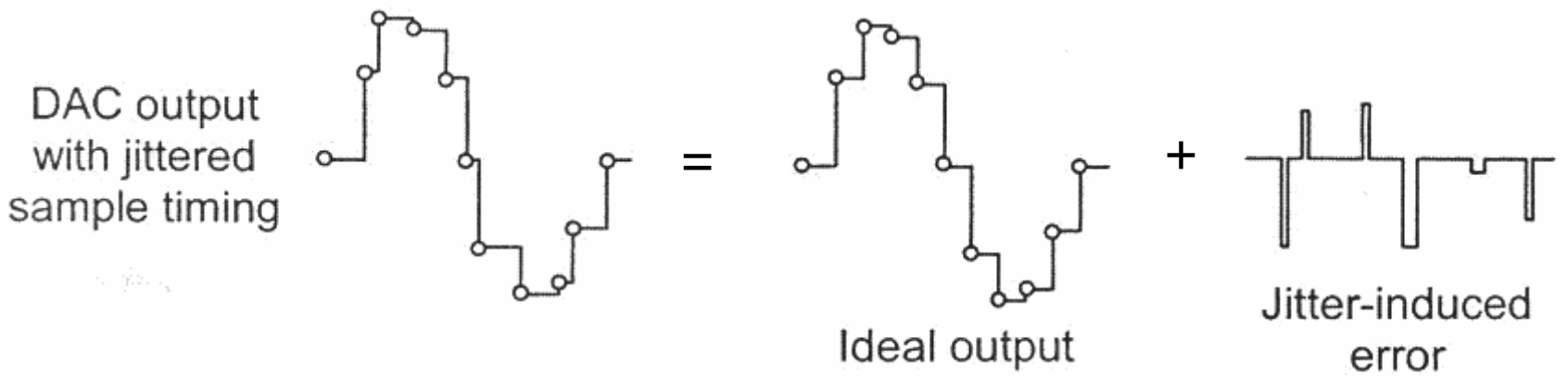
⇒ **Assume** $FS = 2A_0 \Rightarrow t_{j-RMS} < \dfrac{\sqrt{2}}{\pi f_0 (2^D - 1)}$

– **Conversely, if a *D*-bit ADC having an RMS jitter $t_{j\text{-}RMS}$, the maximum sampling frequency (i.e., $F_{s\text{-}MAX}=2f_{0\text{-}MAX}$) is**

$$F_{s-MAX} < \frac{2\sqrt{2}}{\pi t_{j-RMS} (2^D - 1)}$$

– **The maximum conversion resolution available with a $F_{s\text{-}MAX}$ and $t_{j\text{-}RMS}$ is** $D_{MAX} < \log_2\left(\dfrac{2\sqrt{2}}{\pi t_{j-RMS} F_{s-MAX}} + 1\right)$

Sampling Jitter Effects for DAC



$$v_j(t) = \left[v(nT_s) - v((n-1)T_s)\right] \cdot \left[\quad t - nT_s)\right]$$

$$\Rightarrow e_p[n] = \left(v[n] - v[n-1]\right)^2 \cdot \frac{t}{T_s}$$

$$\Rightarrow v_j[n] = \left(v[n] - v[n-1]\right) \cdot \sqrt{\frac{t_j}{T_s}} \approx \left[\left.\frac{dv(t)}{dt}\right|_{t=nT_s}\right] \cdot \sqrt{t_j T_s}$$

– **The maximum conversion resolution available with a maximum sampling frequency $F_{s\text{-}MAX}$ and RMS sampling jitter $t_{j\text{-}RMS}$ is**

$$D_{MAX} < \log_2\left(\frac{2}{\pi} \cdot \sqrt{\frac{2}{t_{j-RMS} F_{s-MAX}}} + 1\right)$$

← **A bit different from ADC's**

Sampling Jitter Effects for ADC/DAC

- In both DAC or ADC cases, doubling the timing jitter doubles the noise level.
- Also, doubling the frequency or amplitude doubles the jitter induced noise.

  $\Rightarrow$ SNR is not improved.

- If extremely low noise circuits are required, the designer should understand which sampling rates provide the least jitter for both design and testing environments.

Sampling-Time Uncertainty

Aperture Jitter

⇒ **For a full-scale sinusoidal signal V_{in} applied to an N-bit, signed, ADC**

$$V_{in} = \frac{V_{ref}}{2} \cdot \sin(2\pi f_{in} t)$$

⇒ **Maximum input change respect to time**

$$V_{in}^{'} = \left.\frac{\Delta V_{in}}{\Delta t}\right|_{\max} = \pi f_{in} V_{ref} \cdot \cos(2\pi f_{in} t)\Big|_{t=0} = \pi f_{in} V_{ref}$$

⇒ **If Δt represents the sampling-time uncertainty and let Δt < 1LSB**

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

8-bit, 250MHz, 5ps

16-bit, 1MHz, 5ps

References

Sigma-Delta Techniques

[1]. R. Schreier, and G. Temes, Understanding *Delta-Sigma Data Converters*, IEEE Press, New York, NY, 2005.

[2]. S. Norsworthy, R. Schreier, and G. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, New York, NY, 1997.

[3]. J. Candy and G. Temes, *Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, New York, NY, 1992.

[4]. R. Carley, R. Schreier, and G. Temes, “Delta-sigma ADCs with multi-bit internal converters,”: *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, New York, NY, 1997.

Data Converters

[5]. David Johns and Ken Martin, “Analog CMOS Integrated Circuit Design,” John Wiley and Sons, 1997.

[6]. R. Geiger, P. Allen, and N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, Chapter 8. McGraw-Hill Publishing Inc., New York, NY, 1990.

[7]. Mark Burns and Gordon W. Roberts, “An Introduction to Mixed-Signal IC Test and Measurement,” Oxford University Press, 2001.