WA 20.3 A 90dB SNR, 2.5MHz Output Rate ADC using Cascaded Multibit ΔΣ Modulation at 8x Oversampling Ratio

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This 16b, 2.5MHz output rate ADC is intended for xDSL and high-speed instrumentation applications. A fourth-order cascaded ΔΣ modulator (ΔΣM) operating at 20MHz employs multibit quantization and dynamic element matching (DEM) to make all quantization noise contributions negligible at an oversampling ratio (OSR) of eight. The ADC achieves 90dB signal-to-noise ratio (SNR) in a 1.25MHz bandwidth, and 102dB spurious free dynamic range (SFDR) with 270mW dissipation.

Cascaded ΔΣM structures realize high-order noise shaping without instability, and are suited for high-speed converters with low OSR [1][2][3]. A 2-1-1 cascade ΔΣM with 1b quantizers can reduce the inband power of theoretical quantization noise (TQN) to -90dBFS at 24x OSR. The resulting oversampling clock of 60MHz increases analog speed requirements, and makes decimation filter switching noise more difficult to manage in single-chip integration. The use of a multibit quantizer in the last stage further reduces the TQN, but the quantization noise leakage (QNL) due to analog circuit imperfections limit the OSR to 16x [2]. The cascaded pipeline approach is feasible at 8x OSR, but the extra complexity in the pipeline converter increases analog power [3].

This architecture overcomes the limitation of conventional 2-1-1 cascaded ΔΣMs by using multibit quantizers in the first two stages (Figure 20.3.1). This simple extension has several advantages that make low (8x) OSR feasible, and reduce power. Use of multibit quantizers in the first and second stage does not directly reduce TQN, because its quantization noise is cancelled by the noise cancellation logic (NCL). However, the smaller quantizer error extracted from the preceding stage allows the interstage gain to be larger than one to utilize the full dynamic range of the following stage. In case of 4b quantizers, interstage gain smaller than 15 will not cause overload. For this design, a three-stage implementation allows use of interstage gains 4 (hc1) and 8 (hc2). Since the quantization noise of the last stage is scaled by the inverse of hc1 and hc2 in the NCL, the TQN is reduced by the same amount. Figure 20.3.2a illustrates the division of the three factors for the signal-to-quantization-noise ratio (SQNR) set by TQN. At 8x OSR, fourth-order noise shaping gives 54dB SQNR. Four-bit quantization in the last stage gives another 24dB. Total interstage gain of 32 provides the final 30dB, totaling in 108dB. Unlike conventional ΔΣMs, noise shaping provides only half of the total SQNR.

Another advantage of multibit quantization in the earlier stages is the reduced QNL. The dominant source is the first stage QNL caused by integrator pole errors due to finite opamp dc gain, because its effect is only first-order noise-shaped. Figure 20.3.2b shows SQNR by QNL for opamps with 80dB dc gain. Use of 1b quantizers in the first two stages requires 32x OSR to keep QNL negligible. The proposed architecture achieves 110dB SQNR at 8x OSR. Note that a larger interstage gain increases the pole error. Thus, hc2 is made larger than hc1 because the pole error of latter stages has smaller effect. The architecture makes both TQN and QNL negligible in the overall SNR, leaving the entire noise budget to analog (kT/C) noise. In addition, the insertion of interstage gain reduces the kT/C noise contributions of the latter stages, which otherwise would be significant with limited noise-shaping at 8x OSR.

The nonlinearity of the first-stage multibit DAC directly affects the performance without suppression by noise shaping. However, improvement of capacitor mismatch in modern process technology and development of DEM algorithms has made this a viable choice. A common DEM algorithm, data weighted averaging (DWA) achieves first-order mismatch shaping, but can introduce signal-dependent tones [4]. This degrades SFDR and makes the inband mismatch-induced noise power dependent on signal level [5]. The bi-directional DWA (Bi-DWA) algorithm shown in Figure 20.3.3a switches the direction of rotation every sample with a separate index pointer for the odd samples (right rotation) and the even samples (left rotation). This simple modification to DWA randomizes the sequence to eliminate tones while preserving the noise shaping. Figure 20.3.3b demonstrates this by comparing simulations of DWA and Bi-DWA with 0.1% mismatch. The cost of Bi-DWA is the slight increase in mismatch noise. With capacitor mismatch of this design, the increase is 1dB compared to the worst-case of DWA, keeping mismatch noise contribution minor in the noise budget. Applying Bi-DWA to all three stages allows capacitor sizes in the latter stages to be optimized for kT/C noise instead of mismatch, which reduces power.

Fully-differential switched-capacitor circuits are used for the ΔΣM implementation. In the integrator stage, a common set of capacitors is shared by input sampling and the 4b DAC [3]. Eliminating one set of switched-capacitors results in 3dB reduction of kT/C noise, smaller ac load, and smaller integrator pole error. The advantage for use in the first integrator is the relaxed ADC input drive requirement. The full-scale input range is ±2.0V differential. Capacitors are pre-charged to the previous quantizer output level, which closely tracks the input in a oversampled multibit ΔΣM. The use of low-threshold CMOS transfer gates for input switches reduces resistance voltage dependency, hence sampling distortion. For the first integrator opamp, dc gain higher than the QNL requirement is implemented to avoid distortion caused by gain dependency to voltage. Settling requirements for QNL and distortion prevention are greatly relaxed by multibit quantization. A folded-cascode topology with gain boost achieves high dc gain with the necessary bandwidth (Figure 20.3.4). A single low-threshold transistor gain boost has the minimum current overhead, with swing reduction of only 0.3V compared to a cascode load biased in high-swing condition. The simulated dc gain is 96dB. The closed-loop dominant pole is 90MHz, which is only 4.5 times the sampling frequency.

The 4.6x5.4mm² chip is fabricated using triple-metal, double-poly, 0.5μm CMOS (Figure 20.3.5). The decimation low-pass filter consists of three half-band FIR stages. The stopband attenuation is 85dB and the passband ripple is ±0.004dB. All measurements are with 5V analog and 3V digital power supplies. Power dissipation of the ΔΣM is 105mW. The 270mW total power is less than half that of a previously-reported ADC with comparable performance [3]. Figure 20.3.6 shows signal-to-(noise + distortion) ratio (SNDR) and SFDR vs. input level for 100kHz and 500kHz signals. The SNR at 500kHz is 90dB. The SFDR is 110dB at -10dBFS, and 102dB at -0.1dBFS. Figure 20.3.7 shows the FFT spectrum for a -0.1dBFS, 100kHz sine-wave input. The total harmonic distortion is 98dB.

References:

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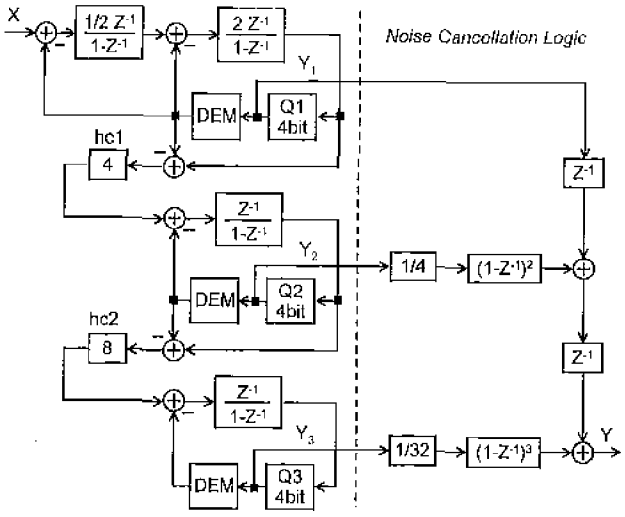

Figure 20.3.1: ΔΣ modulator block diagram.

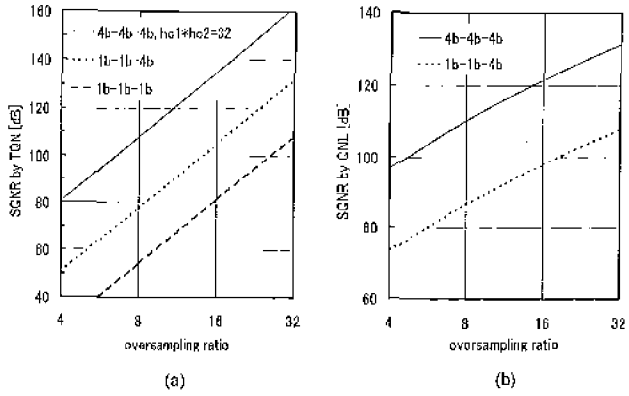

Figure 20.3.2: Multibit quantizers in a 2-1-1 cascade: (a) TQN vs. OSR, (b) QNL vs. OSR.

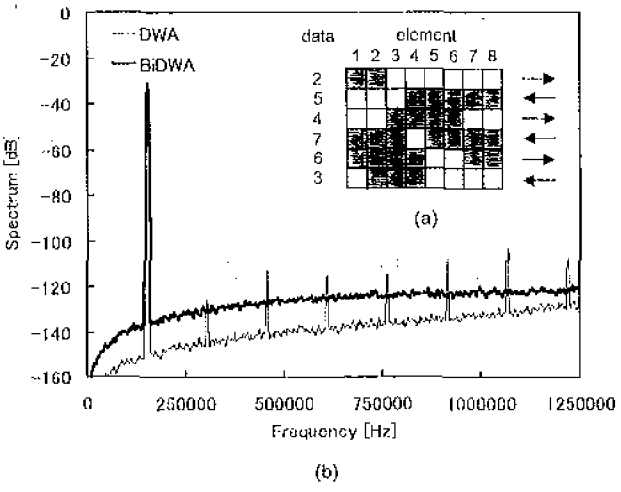

Figure 20.3.3: (a) Concept of Bi-DWA, (b) Simulated FFT with 0.1% DAC mismatch (average of 50sets).

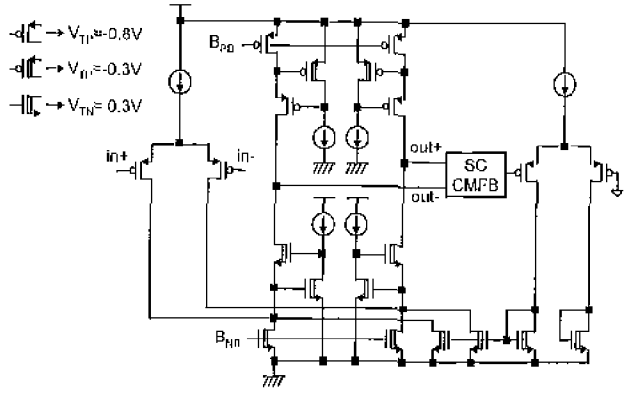

Figure 20.3.4: Opamp circuit diagram.

Figure 20.3.5: See page 468.

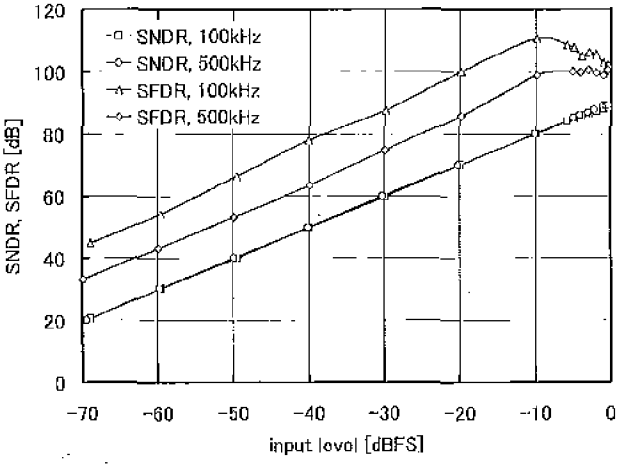

Figure 20.3.6: Measured SNDR and SFDR vs. input level.

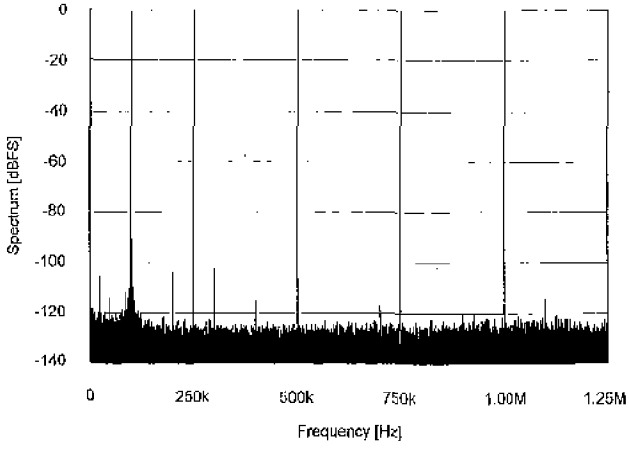

Figure 20.3.7: Measured FFT of a -0.1dBFS, 100kHz signal.