A High-Efficiency CMOS +22-dBm Linear Power Amplifier

Yongwang Ding and Ramesh Harjani, *Senior Member, IEEE*

***Abstract*—Modern wireless communication systems require power amplifiers with high efficiency and high linearity. CMOS is the technology of choice for complete systems on a chip due to its lower costs and high integration levels. However, it has always been difficult to integrate high-efficiency power amplifiers in CMOS. In this paper, we present a new class of operation (parallel A&B) for power amplifiers that improves both their dynamic range and power efficiency. A prototype design of the new amplifier was fabricated in a 0.18-μm CMOS technology. Measurement results show a PAE that is over 44% and the measured output power is +22 dBm. In comparison to a normal class A amplifier, this new design increases the 1-dB compression point (P1dB) by over 3 dB and reduces dc power consumption by over 50% within the linear operating range.**

***Index Terms*—Class A, class AB, CMOS, power amplifier.**

I. Introduction

CMOS power amplifiers (PAs) are used in modern radios for their low cost and the ability of integration with digital circuits. Many linear PAs have been designed for integrated radios [1]–[10]. Class A amplifiers are used where linear operation and high gain is critical. However, to maintain class A operation throughout the input signal range, such amplifiers need to be biased at a relatively high overdrive level. With the result that class A amplifiers consume significantly higher dc power than other amplifier topologies even for low-level input signals, class AB amplifiers have a drain current duty cycle that lies in between class A and class B amplifiers. With a fixed dc bias (current or voltage), a class AB amplifier is essentially a class A amplifier when the input signal is small. However, it starts to operate in the class AB mode when the input signal level is sufficiently high.

Most CMOS power amplifiers are operated in class AB mode for higher output power and better power-added efficiency (PAE) [1], [3]–[5], [7]–[11]. It is possible to achieve close to 40% PAE at the maximum output power for real-life CMOS class AB amplifiers. However, as the dc power consumption of such amplifiers is relatively constant over the entire operating range, its PAE reduces significantly when the output power is lower than the maximum level. This becomes a serious problem for systems that have large dynamic range (i.e., high peak-to-average ratio), such as multicarrier OFDM (802.11a/802.11g) systems. The output for such systems show a remarkable similarity to band-limited Gaussian white noise. Not unlike a Gaussian signal, the majority of the signals are small while a small percentage of the signals can be of large magnitude with the result that the average (rms) power is smaller than what might be reflected by the peak amplitude. Therefore, in order not to saturate the larger signals, the power amplifier needs to be backed off. For example, for the 802.11a standard 54-Mb/s operation (64 QAM), the power amplifier needs to be backed off by 8–10 dB from its output 1-dB compression point (P1dB) with the result that, during normal operation, the PAE effectively reduces to the 5% range.

The bias current increases with the input signal level for a CMOS class B amplifier, i.e., the dc power consumption self-adjusts depending on the input power level. Therefore, the PAE of a CMOS class B amplifier is much higher than that of a class A or class AB amplifier for small input levels. However, the gain of such amplifiers also changes with the input signal level, due to an increase in the effective transconductance, resulting in higher distortion than either class A or class AB amplifiers.

In this paper, we present a new power amplifier with a parallel combination of a class A/AB amplifier and a class B amplifier. This amplifier provides the higher linearity of a class A amplifier while providing a PAE that is closer to that of a class B amplifier over the entire operating range.

II. Traditional CMOS Linear Power Amplifiers

Linear PAs can be categorized as class A, class B, class AB, class C, etc., depending on the duty cycle of the their drain currents [12].

Fig. 1 shows a simplified circuit diagram for a CMOS cascode PA. We have shown a single-ended design but, in general, differential designs are often preferred for their improved power supply rejection ratio (PSRR) and the suppression of even-order harmonics. The input transistor M1 is biased to a fixed voltage $V\mathrm{in}_{\mathrm{DC}}$ through a pair of large valued resistors $R\mathrm{in}_{\mathrm{DC}}$. The cascode transistor M2 provides isolation between the input and output nodes. Capacitors C_{ac} are ac coupling capacitors, *RFC* is the RF choke, and the matching network is used for output impedance matching. This basic topology can be made to operate in different modes, e.g., class A mode and class B mode, by altering the input dc bias voltage V_{indc} to this amplifier.

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Y. Ding is with Silicon Laboratories, Inc., Austin, TX 78745 USA (e-mail: yongwang.ding@silabs.com).

R. Harjani is with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: harjani@ece.umn.edu).

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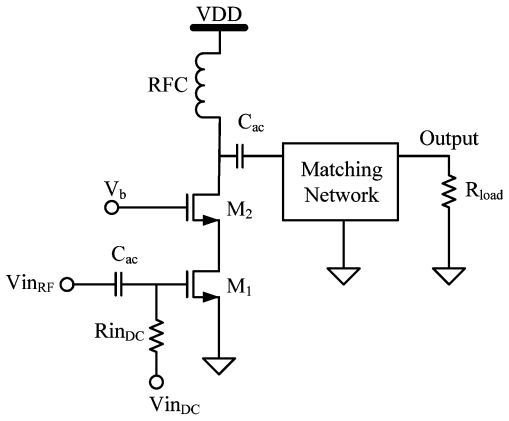

Fig. 1. General CMOS PA circuit.

A. Class A/AB Amplifier

When the input signal is small, the fundamental-signal transconductance for a class A or a class AB amplifier is given by

$$g_{mA} = \frac{I_{Ad,\text{fund}}}{V_{\text{in}}} = \mu_n C_{\text{ox}} \frac{W}{L} V_{od} \frac{1+\frac{1}{2}\rho_a}{(1+\rho_a)^2}\left(1+\alpha_A v_{\text{in}}^2\right) \tag{1}$$

where W and L are the channel width and length of the input transistor, respectively, $V_{\text{od}} = V_{\text{indc}} - V_{\text{th}}$ is the overdrive voltage, ρ_a is a measure of velocity saturation effect, and E_{sat} is the saturation field strength. It can be seen that the transconductance of the class A/AB amplifier decreases with the input signal level where

$$v_{\text{in}} = \frac{V_{\text{in}}}{V_{\text{od}}}$$

and

$$\alpha_A = -\frac{3\rho_a}{4(1+\rho_a)^2(2+\rho_a)}$$
$$\rho_a = \frac{V_{\text{od}}}{L \cdot E_{\text{sat}}}. \tag{2}$$

The dc current through a class A/AB amplifier is given by (3). Once again, the expression within the square brackets in (3) models the impact of short channel effects. As the class A amplifier needs to be biased at a sufficiently high dc voltage so as to be on during the entire period of the input signal, its drain current is practically constant over its entire operating range such that it consumes significant dc current even for small input signals

$$I_{\text{DCA}} = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L} V_{\text{od}}^2 \left[\frac{1}{1+\rho_a}\right]. \tag{3}$$

B. Class B Amplifier

The drain current for a class B amplifier is only on for half of the period of a sinusoidal input. As the drain current is not constant during the input cycle, large-signal analysis has to be applied to generate an expression for the fundamental-signal transconductance. The drain current at the fundamental frequency, $I_{Bd,\text{fund}}$, of a CMOS class B amplifier with a sinusoid input of $V_{\text{in}} \cdot \sin(\omega t)$ is given by

$$I_{Bd,\text{fund}} = \frac{2}{T}\int_0^{T/2} I_d(t)\sin(\omega t)dt = \frac{2}{T}\int_0^{T/2} \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L} V_{\text{in}}^2 \frac{\sin^2(\omega t)}{1+\rho_b \sin(\omega t)} \cdot \sin(\omega t)dt \tag{4}$$

where ρ_b is given by

$$\rho_b = \frac{V_{\text{in}}}{L \cdot E_{\text{sat}}}.$$

The fundamental-signal transconductance for a class B amplifier can be derived as shown by

$$g_{mB} = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L} V_{\text{in}} \left[\frac{1}{2\rho_b} - \frac{2}{\pi}\frac{1}{\rho_b^2} + \frac{1}{\rho_b^3} - \frac{4}{\pi}\frac{1}{\rho_b^3\sqrt{1-\rho_b^2}} \arctan\left(\sqrt{\frac{1-\rho_b}{1+\rho_b}}\right)\right]. \tag{5}$$

As ρ_b is proportional to V_{in}, we note that the fundamental-signal transconductance increases with the input signal level. This is true until the amplifier compresses due to signal swing limitations at the output

For small inputs, the fundamental-signal transconductance for the class B amplifier can be approximated by

$$g_{mB}\,|_{V_{\text{in}}\to 0} = \frac{2}{3\pi}\mu_n C_{\text{ox}} \frac{W}{L} V_{\text{in}}. \tag{6}$$

As can be seen from this expression, for small inputs the transconductance of a class B amplifier increases with the input signal level

Likewise, the dc current for a class B amplifier is given by

$$I_{DCB} = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L} V_{od}^2 \cdot \left[\frac{2}{\pi\rho_b} - \frac{1}{\rho_b^2} + \frac{4}{\pi\rho_b^3} \cdot \frac{1}{\sqrt{1-\rho_b^2}} \arctan\left(\sqrt{\frac{1-\rho_b}{1+\rho_b}}\right)\right] \tag{7}$$

and can be approximated by

$$I_{DCB}\,|_{V_{\text{in}}\to 0} = \frac{1}{8}\mu_n C_{\text{ox}} \frac{W}{L} V_{\text{in}}^2 \tag{8}$$

when the input is very small. We note that the dc current increases quadratically with the input signal level. This is not surprising given the quadratic large signal relationship between the gate voltage and drain current for a long-channel MOS device. As will be seen in Fig. 5, a class B amplifier consumes significantly lower dc current for small inputs in comparison to either a class A or class AB amplifier.

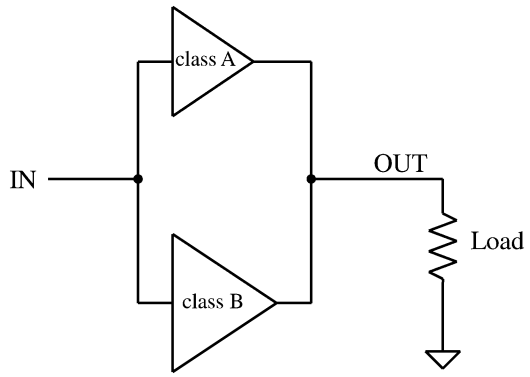

Fig. 2. Conceptual block diagram for the new amplifier.

III. CMOS Parallel Class A&B Amplifiers

A parallel combination of a class A and a class B amplifier can be used to improve both the linear operation range and the power efficiency. A conceptual block diagram for such an amplifier is shown in Fig. 2. As will be shown later, the outputs from both the amplifiers are combined in the current domain with little overhead. Our circuit architecture uses two differently biased transistors to provide a more linear transconductance and is a variation of the derivative superposition approach [13]–[18]. In our case, two amplifiers operate in parallel, a class A and a class B, so we call this a *parallel class A&B amplifier*.

The transconductance of the parallel class A&B amplifier is a combination of a class A transconductance and a class B transconductance, as is given by

$$g_{mA\&B} = g_{mA} + g_{mB} \tag{9}$$

where g_{mA} and g_{mB} are given by (1) and (5), respectively.

From (5) and (6), it is clear that the effective transconductance and resulting power gain of a class B amplifier increases with increased input amplitude. However, class A and/or class AB amplifiers start to compress rapidly as the input signal levels increase. So, in a parallel class A&B amplifier, the class A amplifier is the primary transconductance contributor at low signal levels; however, the class B amplifier is the primary contributor at high signal levels, with the result that the class B amplifier can compensate for the compression of the class A amplifier when they are combined with the appropriate ratio.

For example, Fig. 3 shows the simulated input–output power transfer function for the parallel class A&B amplifier. This design uses parameters for the UMC 0.18-μm CMOS process. With an overdrive voltage of 0.5 V for the class A transistors, the class B transistors need to be four times larger in order to linearize the transconductance. In this figure, the solid line with the solid circles shows the input–output power transfer function for the parallel class A&B amplifier. The dashed line with the +'s shows the contribution from the class A amplifier while the dashed line with the solid diamonds shows the contribution from the class B amplifier. As can be seen, at low input levels, the class A amplifier contributes the majority of the gain as the gain of the class B is very low. As the input level increases, the gain of the class B amplifier increases and its contribution to the overall gain increases proportionately. When the input level is

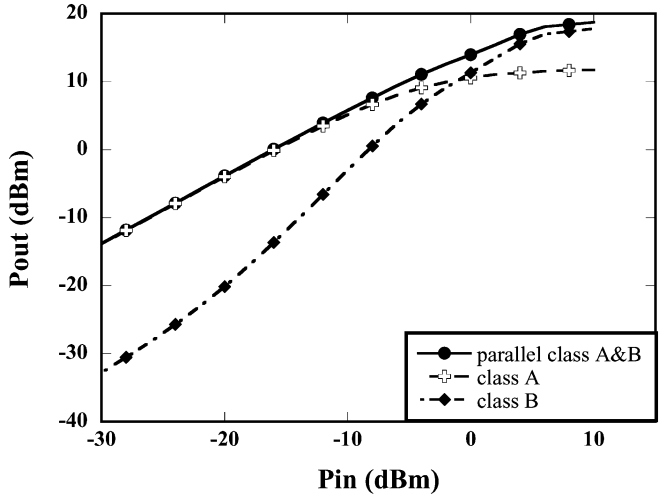

Fig. 3. Parallel class A&B amplifier transfer characteristics (simulation results).

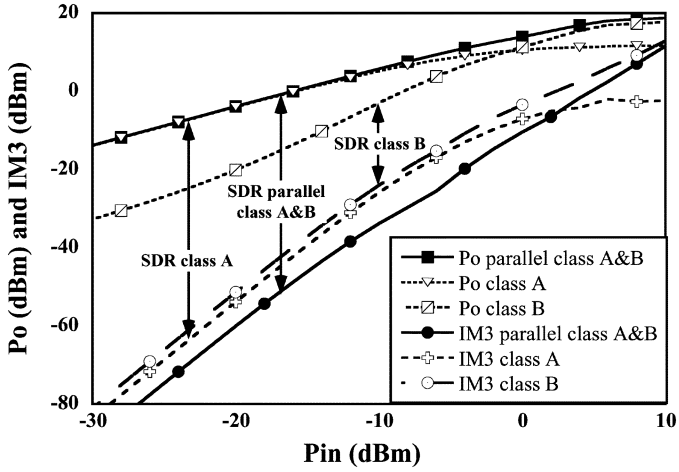

Fig. 4. Comparison of intermodulation products (simulation results).

sufficiently high, the class B amplifier provides the majority of the power gain and compensates for the gain compression of the class A amplifier.

In Fig. 3, we see that the class B amplifier compensates for the gain compression of the class A amplifier, so we expect a higher 1-dB compression point for the parallel class A&B amplifier in comparison to a class A amplifier. Additionally, since the class A amplifier does not have to provide significant power gain at larger inputs, it can be designed to be smaller and biased at a lower power level, i.e., resulting in an improved PAE. To evaluate both the PAE and the linearity characteristics, we have designed and simulated three amplifiers, class A, class B, and parallel class A&B, all of which drive low impedance loads so that gain compression occurs at the inputs rather than at the outputs.

The linearity characteristics are shown in Fig. 4 with both the fundamental and intermodulation signals (IM3) for the three amplifiers. Also marked on the figure is the signal-to-distortion ratio (SDR) for all three amplifiers. In the parallel class A&B amplifier, the class A contributes to the majority of the gain at low signal levels so we expect the linearity to be similar to a class A. Interestingly, we find that the IM3 products are 5–7 dB

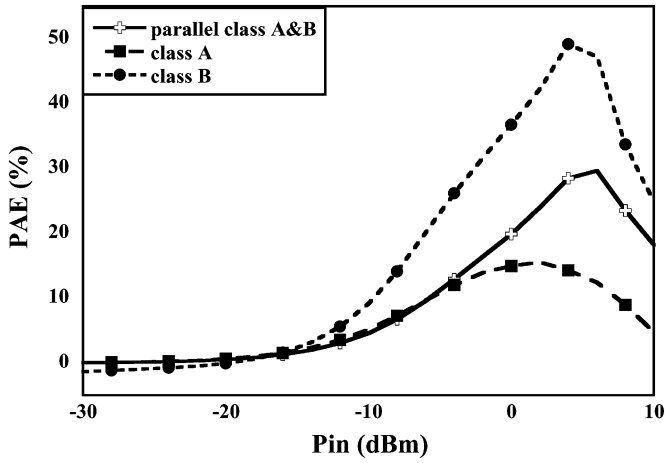

Fig. 5. Comparison of PAE (simulation results).

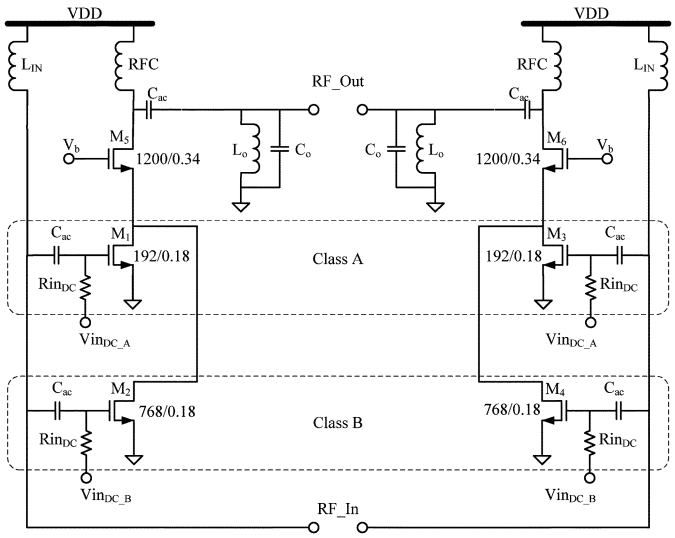

Fig. 6. Circuit schematic for the CMOS parallel class A&B amplifier.

lower than even those for the class A amplifier. This is because the class B amplifier, in the parallel A&B amplifier, partially compensates for the distortion caused by the class A amplifier. At high signal levels, the class B amplifier contributes the majority of the output power, at which point the total distortion of the parallel class A&B amplifier is dominated by the class B part and is larger than that of the class A amplifier. Multicarrier systems such as 802.11a/802.11g are very sensitive to power amplifier distortion. In particular, 54-Mb/s operation for either of these standards requires a minimum SDR of 25 dB (often measured as EVM). The higher linearity of the parallel class A&B PA allows it to transmit 54-Mb/s signals at 10-dBm output power while the class A amplifier with a SDR of 19 dB would only be able to support a 36-Mb/s stream at the same output power [19].

The dc current consumed by the parallel class A&B amplifier is given by

$$I_{\mathrm{DCA\&B}} = I_{\mathrm{DCA}} + I_{\mathrm{DCB}}. \tag{10}$$

where I_{DCA} and I_{DCB} are given by (3) and (7), respectively. The class A transconductors consumes the majority of the dc current at the small inputs and the power consumption of the class B transconductors dominates the dc current for large inputs.

Fig. 5 shows the PAE for the three power amplifiers (class A, class B, and parallel class A&B) versus input signal power. We see that the PAE of the class A amplifier is lower than both the class B amplifier and the parallel class A&B amplifier due to the higher dc bias. Because the class A part and the class B part of the parallel class A&B amplifier contribute to the majority of the gain and the dc current at different input power ranges, the PAE of the parallel class A&B is almost the same as that for a class A amplifier at low inputs and closer to that of a class B at high inputs. The parallel class A&B amplifier provides an excellent compromise between gain, output power, and PAE.

For these graphs, we have used a cascaded design so that the input has been well isolated from the output, which greatly reduces the intermodulation caused by the second-order interaction. Further, low linear output impedance has been used to ensure the linearity at the output. Therefore, the PA compresses at the input rather than at the output. However, in practice, PAs are usually limited at both the input and output. If compression occurs at the output, then the mode of operation of the transistor will have limited impact on the performance. Furthermore, there is the distortion caused by the nonlinear gate capacitance of the class B amplifier. Fortunately, that can be compensated by a dummy PMOS in parallel [20]. Therefore, in practice, the difference between the parallel class A&B amplifier and the class A/AB amplifiers maybe not be as large as shown in Figs. 4 and 5. However, the improvements offered by the combined structure is still significant, as will be seen in Section IV.

IV. Experimental Results

In this section, we present a prototype design of the parallel class A&B amplifier in the UMC 0.18-μm RF CMOS technology and compare its measured performance with other state-of-the-art CMOS power amplifiers. A simplified circuit diagram of the differential parallel class A&B power amplifier design is shown in Fig. 6.

Shunt inductors L_{in} are used to impedance match the inputs, and the inductors RFC are used as RF chokes to prevent coupling of the RF signal to the power supplies. An additional pair of inductors L_o is used to match the output port. The input transistors M2 and M4 have an aspect ratio of (768/0.18) and are biased at the edge of the threshold voltage via the two large value resistors, i.e., $V_{indcB} \sim V_{\mathrm{th}}$. These two transistors form the transconductors for the class B amplifier. The other two input transistors M1 and M3 have an aspect ratio of (192/0.18) and are biased well above the threshold voltage so that they operate in saturation for the majority of the input range, i.e., $V_{\mathrm{indcA}} \sim V_{\mathrm{th}} + V_{\mathrm{od,max}}$. These two transistors form the trasconductors for the class A amplifier. The size of the class A transistors M2 and M4 are only one quarter the size of the class B transistors M1 and M3. This forces the class B transistors to provide the majority of the power at large input signals. The cascode transistors have an aspect ratio of (1200/0.34). These transistors have a thicker gate oxide with a higher breakdown voltage than the input transistors and are able to handle the large

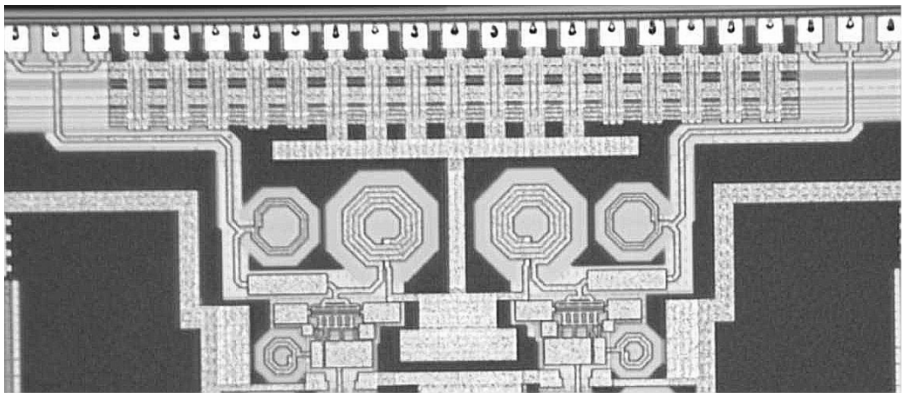

Fig. 7. Die microphotograph of the CMOS parallel class A&B amplifier.

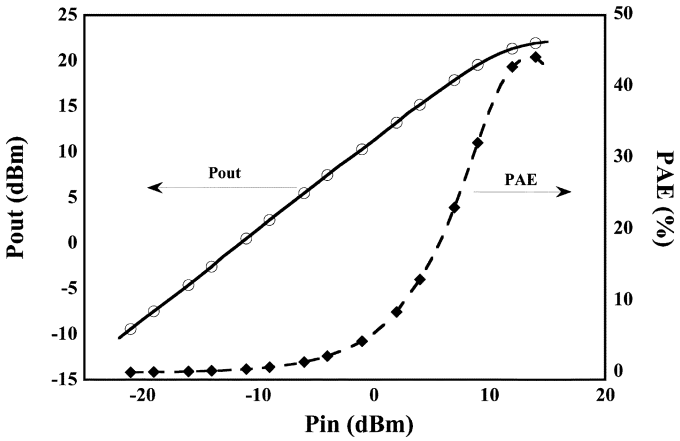

Fig. 8. CMOS parallel class A&B amplifier measurement results.

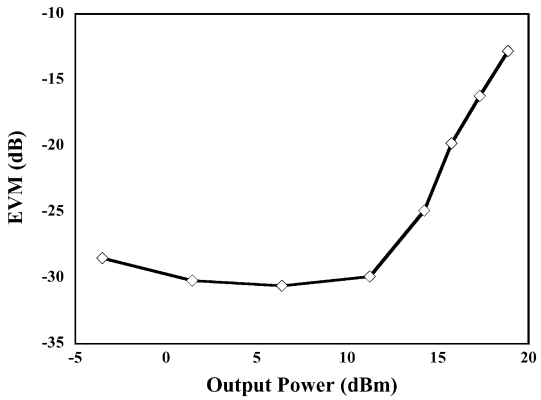

Fig. 9. Measured EVM versus output power for the CMOS parallel class A&B amplifier.

voltage swings at the outputs. A microphotograph of the fabricated PA is shown in Fig. 7.

The output power and PAE results for the parallel class A&B amplifier are shown in Fig. 8. The power gain within the linear operating range is 12 dB, the maximum output power is over +22 dBm and the maximum PAE is over 44%. The amplifier reaches its 1-dB compression point at an output level of +20.5 dBm and the PAE at P1dB is 36%.

Fig. 9 shows the measured EVM versus the output power. To achieve a −25-dB EVM, which is required by 54-Mb/s OFDM signals, the output power can be as high as 14.5 dBm, which corresponds to a 6-dB back-off from the 1-dB compression point.

TABLE I
COMPARISON OF MEASURED RESULTS

Design	Technology (μm)	A_p (dB)	$Pout_{max}$ (dBm)	PAE (%) @			
				$Pout_{max}$	P1dB	Back-off 4dB	Back-off 8dB
Ballweber	0.60 [3]	5	19	30	26	14	6
Giry	0.35 [4]	24.6	23.5	35	24	13	6
Sowlati	0.18 [10]	36	23	42	18	8	4
This work	0.18	12	22	44	36	18	8

The measured EVM at lower powers range is limited by a combination of the instrumentation resolution and noise floor.

In Table I we provide the measured results for a prototype class A&B amplifier and compare it with other CMOS class AB power amplifiers [3], [4], [10]. The new amplifier has a higher PAE. This is particularly visible when the amplifiers are operated in their linear operating range, i.e., 4–8 dB back-off, that is usually mandated by system requirements. For example, at 8-dB back-off, the PAE of the parallel class A&B amplifier is over 50% higher than that for the other designs. This can result in significant reduction in dc power consumption for similar RF output power levels.

V. CONCLUSION

In this paper, we have presented a design for a new PA with a parallel class A&B structure. This new amplifier provides superior performance in terms of both linearity and power efficiency in comparison to previous designs. Measurement results shows a 12-dB power gain (single stage), 22-dBm output power, and more than 44% PAE. More importantly, this circuit uses significantly lower dc power at 4–8 dB back-off in comparison to other class AB amplifiers.

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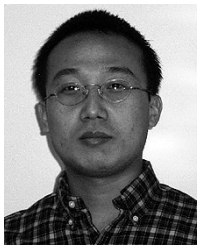

Yongwang Ding received the B.S. degree in physics from Peking University, Beiing, China, in 1996 and the M.S. degree in electrical engineering and the Ph.D. degree from the University of Minnesota, Minneapolis, in 1999 and 2004, respectively.

From May 2001 to September 2004, he was with Bermai, Inc., as an RF IC Design Engineer. He is now with Silicon Laboratories, Inc., Austin, TX. His research interests include RF front-end ICs for wireless communications and high-speed high-linearity circuits in CMOS. He is also the coinventor of four pending U.S. patents.

Ramesh Harjani (S'87–M'89–SM'00) received the B.S. degree from the Birla Institute of Technology and Science, Pilani, India, in 1982, the M.S. degree from the Indian Institute of Technology, New Delhi, in 1984, and the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, in 1989, all in electrical engineering.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering and a Member of the graduate faculty of the Department of Biomedical Engineering at the University of Minnesota, Minneapolis. Prior to joining the University of Minnesota, he was with Mentor Graphics Corporation, San Jose, CA, where he was involved with CAD tools for analog synthesis and power electronics. He has had a number of short stints as a Member of the Technical Staff at Lucent Technologies, Allentown, PA, and worked on data converters for DSL. He cofounded Bermai, Inc., Palo Alto, CA, a startup company developing CMOS chips for wireless LAN applications in 2001. His research interests include analog/RF circuits for wired and wireless circuits, low-power analog design, sensor interface electronics, and analog and mixed-signal circuit tests. He is a coauthor of the books *Design of Modulators for Oversampled Converters* (New York: Kluwer, 1998), *Design of High-Performance CMOS Voltage-Controlled Oscillators* (New York: Kluwer, 2002), and *High-Linearity CMOS RF Frontend Circuits* (Berlin, Germany: Springer-Verlag, 2004).

Dr. Harjani was the recipient of the National Science Foundation Research Initiation Award in 1991. He was also the recipient of the Best Paper Award at the 1987 IEEE/ACM Design Automation Conference and the 1989 International Conference on Computer-Aided Design and an Outstanding Paper Award at the 1998 GOMAC. His research group was the winner of the SRC Copper Design Challenge in 2000 and the winner of the SRC SiGe challenge in 2003. He was an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1995 to 1997 and was a Guest Editor for the special issue on "High-Speed Mixed-Signal Integrated Circuits" of the *International Journal of High-Speed Electronics and Systems* (2004) and a Guest Editor for the Special International Symposium on Circuits and Systems, Analog Integrated Circuits and Signal Processing (2004). He was the Chair of the IEEE Circuits and Systems Society Technical Committee on Analog Signal Processing from 1999 to 2000 and a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2001 to 2002.