# High-Speed Communication Circuits & Systems

## Limiting Amplifiers

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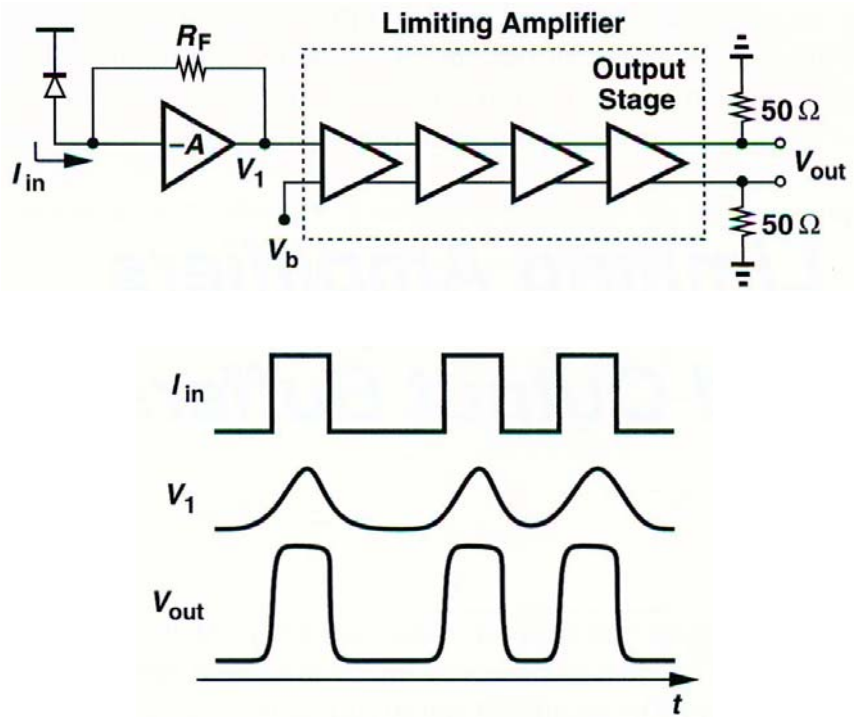
## Introduction to TIA & LA

- The signal produced by TIA suffers from small amplitude.
- The TIA must be followed by LA that boosts the signal swing to logical levels.
- LA provides both a high voltage gain and large output swings.
- Design issues:
  - Low noise
  - Broadband

## Role of s Limiting Amplifier in a Receiver Front End






## Aspects of LA (1/2)

- Input Capacitance

  The LA must exhibit a sufficiently low input capacitance so that it does not reduce the TIA bandwidth significantly.

- Bandwidth

  The data transitions at the output of the TIA ate relatively slow, but the LA must amplify and clip the signal such that $V_{out}$ exhibits a high slew rate and short rise and fall times.

- Noise
  - Input-referred noise of LA is critical for two reasons:
    - Their large bandwidth yields a greater integrated noise;
    - Design of TIAs with a high transimpedance gain becomes increasingly more difficult at high speeds, making the contribution of the LA noise significant.
  - Overall input-referred noise current of TIA/LA cascade:

$$\overline{I_{n,in,tot}^2} = \overline{I_{n,T}^2} B_T + \frac{\overline{V_{n,L}^2} B_L}{R_T^2}$$

Noise BW of TIA and LA are $B_T$ and $B_L$.

## Aspects of LA (2/2)

- Gain
  - The first stage of a limiting amplifier must provide enough gain so as to minimize the noise contributed by the following stages.
  - LA typically employ only 3 to 4 stages.
- Output Drive Capability

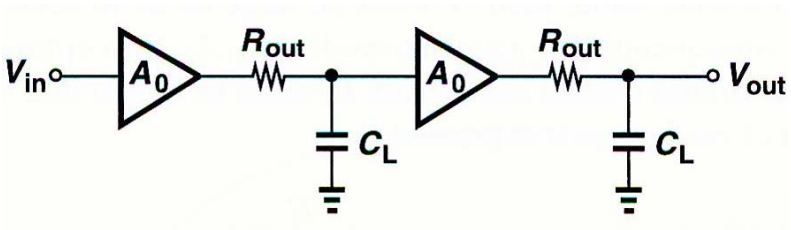
  The output stage must deliver large current to the 50-Ω loads.
- Jitter

  It is desirable to maintain the limiter jitter below a few percent of the bit period.
- Offset Voltage

  LA usually incorporates offset cancellation.



## Cascade Gain Stages




Overall transfer function: $H(s) = \left( \frac{A_0}{1 + \frac{s}{\omega_0}} \right)^2$ $\omega_0 = \frac{1}{R_{out} C_L}$ the $-3$dB BW of each stage

–3dB BW of the overall circuit:

$$\left( \frac{A_0}{\sqrt{1 + \left( \frac{\omega_{-3dB}}{\omega_0} \right)^2}} \right)^2 = \frac{A_0^2}{\sqrt{2}} \Rightarrow \omega_{-3dB} = \omega_0 \sqrt{\sqrt{2} - 1} \approx 0.644 \omega_0$$

Cascading two identical stages decreases the BW by about 36%.

Similarly, for N identical stages, the –3dB BW is:

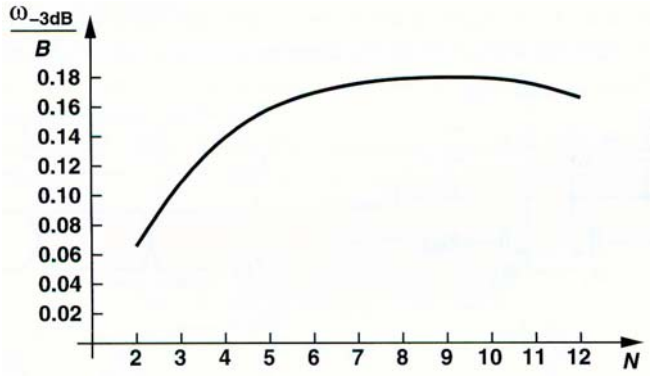
$$\left( \frac{A_0}{\sqrt{1 + \left( \frac{\omega_{-3dB}}{\omega_0} \right)^2}} \right)^n = \frac{A_0^n}{\sqrt{2}} \Rightarrow \omega_{-3dB} = \omega_0 \sqrt{\sqrt[n]{2} - 1} \Rightarrow \omega_{-3dB} \approx \omega_0 \frac{0.9}{\sqrt{N}} \text{ for } N \geq 2.$$

## Gain-Bandwidth Trade-off in Cascade Gain Stages

$$\omega_{-3dB} = \omega_0 \sqrt{\sqrt[n]{2} - 1}$$

- If N = 4 and choose $\omega_{-3dB} = 2\pi \times R_b$, then $\omega_0 \approx 2.3 \times 2\pi \times R_b$.
  ➡ The BW of each stage must exceed $2.3R_b$.
- If each stage provides a small gain and a wide band, then N must be large so as to achieve the required gain and vice versa.
- For a given overall gain ($A_{tot}$), an optimum value of N exists that yields the maximum overall BW.

  Normalized bandwidth as a function of N for $A_{tot}$ = 100 (40dB):






## Find an optimum value of N

Assume TF of each stage is expressed as: $H(s) = \dfrac{\dfrac{B}{\omega_0}}{1 + \dfrac{s}{\omega_0}}$ ← B: Gain-BW product

For N identical stages, $A_{tot} = \left( \dfrac{B}{\omega_0} \right)^n$ and hence $\omega_0 = \dfrac{B}{\sqrt[n]{A_{tot}}}$.

➡ $\omega_{-3dB} = \omega_0 \sqrt{\sqrt[n]{2} - 1} = B \dfrac{\sqrt{\sqrt[n]{2} - 1}}{\sqrt[n]{A_{tot}}} \approx B \dfrac{0.9}{\sqrt{N} \sqrt[n]{A_{tot}}}$

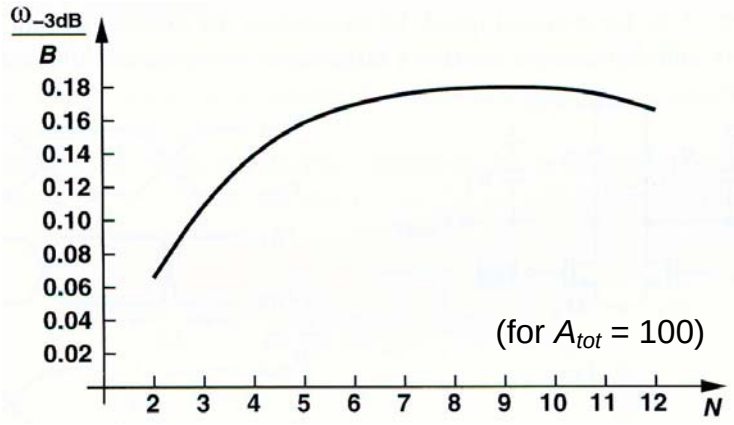
To minimize the denominator, we take its natural logarithm: $\ln D = \dfrac{\ln N}{2} + \dfrac{\ln A_{tot}}{N}$

Differentiate with respect to N ➡ $\dfrac{1}{D} \dfrac{\partial D}{\partial N} = \dfrac{1}{2N} - \dfrac{1}{N^2} \ln A_{tot}$

- The derivative vanishes at $N_{opt} = 2 \ln A_{tot}$, independent of B.
- The corresponding BW is

$$\omega_{\max} = \frac{0.9B}{\sqrt{2 \ln A_{tot}}} A_{tot}^{-\frac{1}{2 \ln A_{tot}}} \approx \frac{0.636B}{\sqrt{\ln A_{tot}}} A_{tot}^{-\frac{1}{2 \ln A_{tot}}}$$

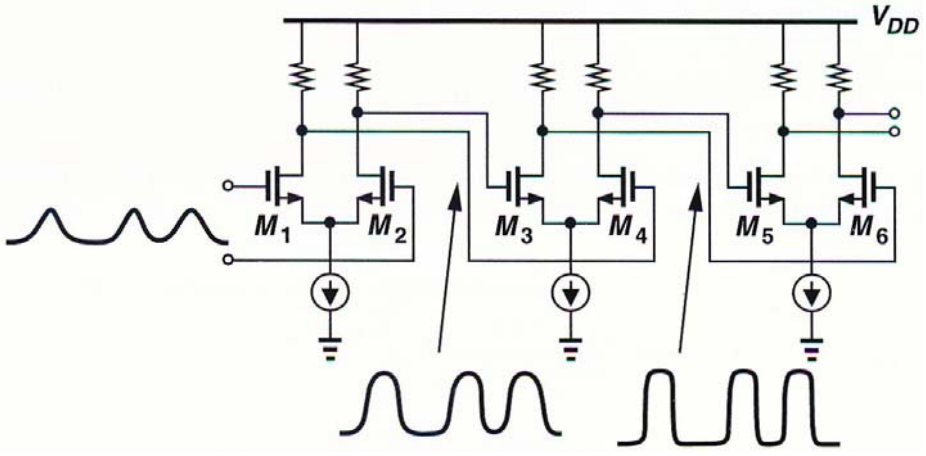
## Normalized bandwidth as a function of N




- $N_{opt} = 2\ln A_{tot}$ the BW reaches a maximum at N ≈ 10.
  However, the plot also reveals only an incremental change in $\omega_{-3dB}$/B for N > 5.
  - As N goes from 5 to 10, the BW increases by less than 15%.
  - With N = 10, the gain per stage is small, making the noise contributed by all of the stages significant.
- Typical high-gain LA employs no more than **five** gain stages.

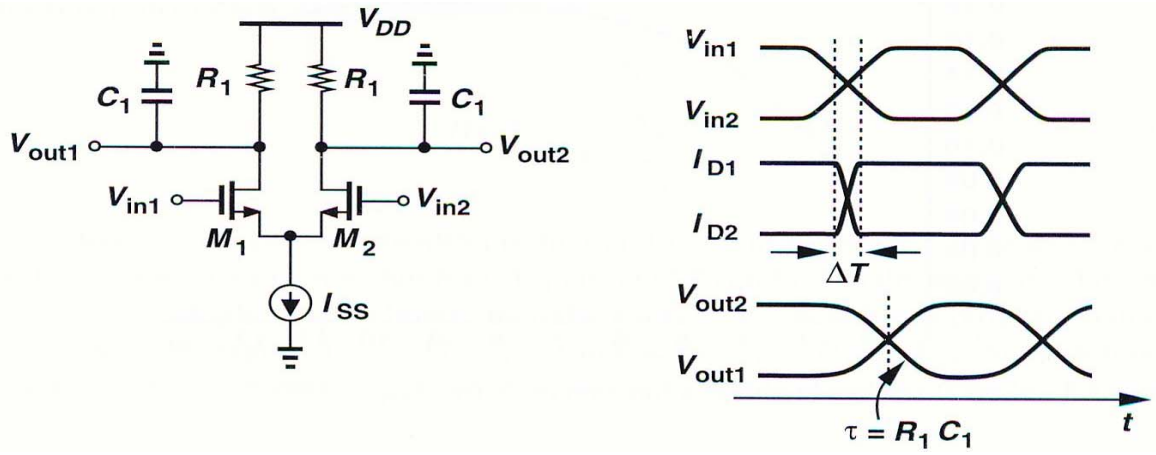


## Effect of limiting on bandwidth




- Owing to relatively complete switching of the tail current and the finite delay of each stage, the last two differential pairs process the zero crossings of the data at different times, violating the assumptions behind prior work.
- Small-signal BW of limiting stage provides a conservative measure of the large-signal speed.

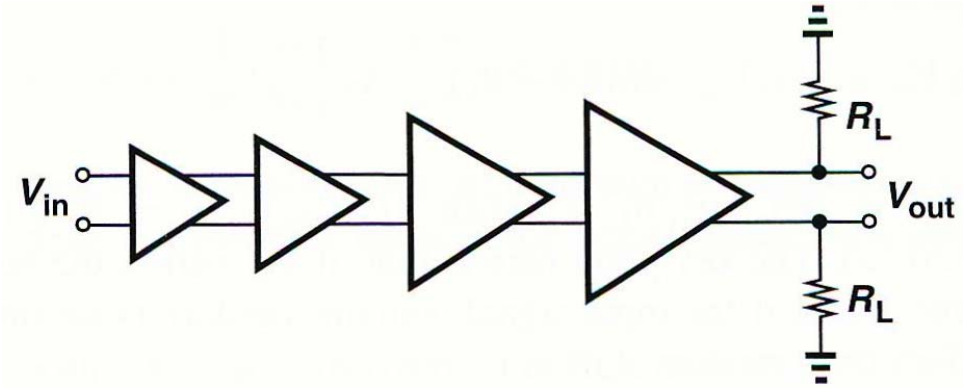
## Delay through a differential pair




- Assume $M_1$&$M_2$ sense a relatively large input swing and exhibit a high small-signal $g_m$ in equilibrium.
  - With long transition time of $V_{in}$, high $g_m$ enables $M_1$&$M_2$ to steer $I_{SS}$ during $\Delta T$.
  - Upon flowing through the loads, $I_{D1}$&$I_{D2}$ generate output waveforms with a time constant of $R_1C_1$. (As if the input had nearly zero transition times)
- In a cascade of identical stages operating with sufficiently large signals, the speed is only that of one stage.
  ➡ a common effect in cascade digital gates



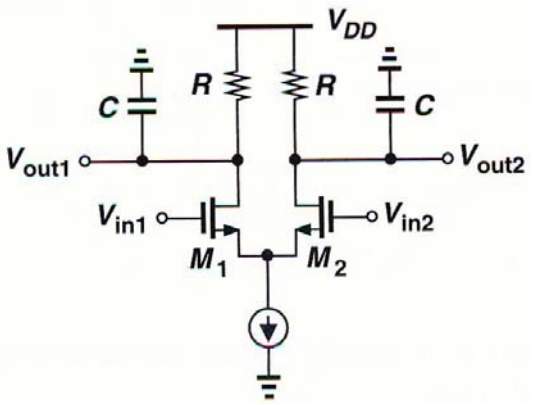
## Tapered output buffer




For 50-Ω loads, it must employ high currents and large output transistors in the last stage. ➡ Large input capacitance

➡ The cascade is tapered in device dimensions and bias currents from the first stage to the last so as to maintain a wide band while delivering high output current

## AM/PM conversion in a differential pair (1/2)




For moderate input swings, the V-to-I characteristic of the differential pair is:

$$I_{out} \approx \alpha_1 V_{in} + \alpha_3 V_{in}^3$$

Suppose $V_{in} = V_m \sin\omega t$ :

$$I_{out} = \alpha_1 V_m \sin\omega t + \alpha_3 V_m^3 \sin^3 \omega t$$
$$= \left(\alpha_1 V_m + \tfrac{3}{4}\alpha_3 V_m^3\right)\sin\omega t - \tfrac{3}{4}\alpha_3 V_m^3 \sin 3\omega t$$

Considering RC loads:

$$V_{out}(t) = A_1\left(\alpha_1 V_m + \tfrac{3}{4}\alpha_3 V_m^3\right)\sin(\omega t + \theta_1) - A_3 \tfrac{3}{4}\alpha_3 V_m^3 \sin(3\omega t + \theta_2)$$

where $A_1 = R/\sqrt{1+R^2C^2\omega^2}$, $\theta_1 = -\tan^{-1}(RC\omega)$, $A_3 = R/\sqrt{1+9R^2C^2\omega^2}$, $\theta_2 = -\tan^{-1}(3RC\omega)$.

- Despite harmonic distortion, $I_{out}$ still crosses zero at $t = n\pi/\omega$.
- If $V_m$ varies, the output zero-crossing points shift in time.
  - ➡ If $V_{in}$ contains random noise on its amplitude, $V_{out}$ suffers from random shift in its zero crossings, i.e., **jitter**.



## AM/PM conversion in a differential pair (2/2)

Estimate the jitter resulting from AM/PM conversion:

If the output zero crossings deviate from their ideal points in time by $\Delta t$

➡ $t = n\pi/\omega + \Delta t$

$$V_{out}\left(\tfrac{n\pi}{\omega} + \Delta t\right) = A_1\left(\alpha_1 V_m + \tfrac{3}{4}\alpha_3 V_m^3\right)(\sin\theta_1 + \omega\cdot\Delta t\cos\theta_1) - A_3\tfrac{3}{4}\alpha_3 V_m^3(\sin\theta_2 + 3\omega\cdot\Delta t\cos\theta_2)$$

Setting the right-hand side to zero, we have

$$\Delta t = \frac{-A_1\left(\alpha_1 V_m + \tfrac{3}{4}\alpha_3 V_m^3\right)\sin\theta_1 + A_3\tfrac{3}{4}\alpha_3 V_m^3 \sin\theta_2}{A_1\left(\alpha_1 + \tfrac{3}{4}\alpha_3 V_m^3\right)\omega\cdot\cos\theta_1 - A_3\tfrac{3}{4}\alpha_3 V_m^3(3\omega)\cos\theta_2}$$

➡ $$\Delta t \approx -\frac{\tan\theta_1}{\omega} + \frac{1}{\omega}\frac{A_3}{A_1}\frac{\tfrac{3}{4}\alpha_3 V_m^3}{\alpha_1 + \tfrac{3}{4}\alpha_3 V_m^3}\frac{\sin\theta_2}{\cos\theta_1} \approx -\frac{\tan\theta_1}{\omega} + \frac{3}{4}\frac{1}{\omega}\frac{A_3}{A_1}\frac{\alpha_3}{\alpha_1}V_m^3\frac{\sin\theta_2}{\cos\theta_1}$$

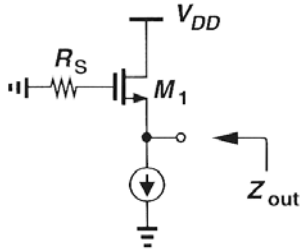
- The 1st term corresponds to the RC delay in the absence of nonlinearity, i.e., if $\alpha_3$ or $V_m$ are very small.
- The 2nd term reveals the dependence of $\Delta t$ upon nonlinearity and the signal amplitude. For example, if the delay variation < 5% of the period, then we have $\frac{A_3}{A_1}\frac{\alpha_3}{\alpha_1}V_m^3\frac{\sin\theta_2}{\cos\theta_1} < 0.419$

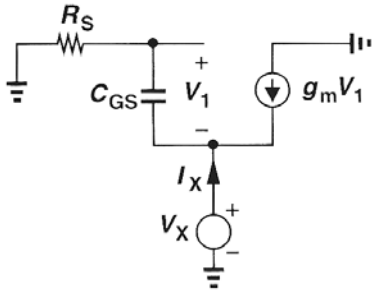
## Broadband Techniques

- Inductive peaking
  - Passive device
  - Active device
- Capacitive degeneration
- Cherry-Hooper amplifier
- $f_T$ doubler



## Source follower providing an inductive output (1/2)



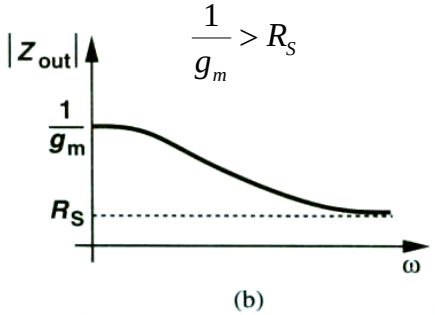




$C_{GD}$ is neglected,

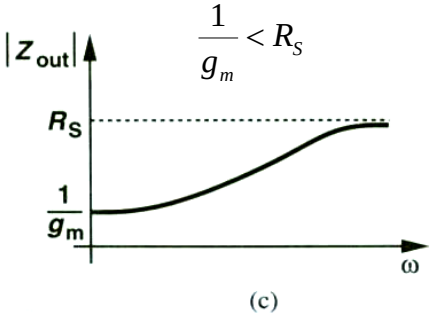
$$V_1 C_{GS} s + g_m V_1 = -I_X$$
$$V_1 C_{GS} s R_S + V_1 = -V_X$$

$$\Rightarrow Z_{out} = \frac{V_X}{I_X} = \frac{R_S C_{GS} s + 1}{g_m + C_{GS} s}$$

- At low frequencies, $Z_{out} \approx 1/g_m$.
- At very high frequencies, $Z_{out} \approx R_S$, because $C_{GS}$ shorts the gate and source.




(b)



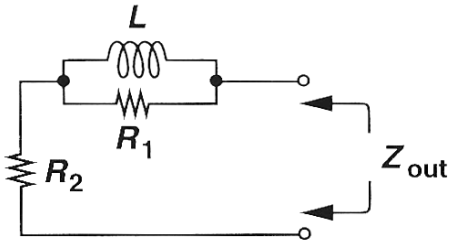

(c)

## Source follower providing an inductive output (2/2)

Equivalent output impedance of a source follower

If $Z_1 = Z_{out}$, find $R_1$, $R_2$ and $L$:

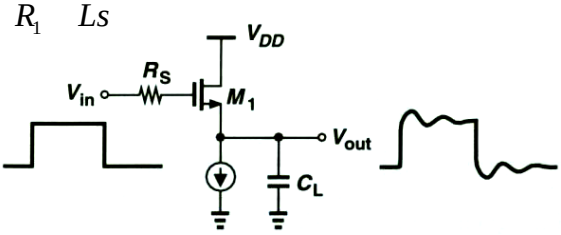
Take $R_2 = 1/g_m$, $R_1 = R_S - 1/g_m$, then




$$Z_{out} - \frac{1}{g_m} = \frac{C_{GS}s\left(R_S - \frac{1}{g_m}\right)}{g_m + C_{GS}s}$$

$$\Rightarrow \quad \frac{1}{Z_{out} - \frac{1}{g_m}} = \frac{1}{R_S - \frac{1}{g_m}} + \frac{1}{\frac{C_{GS}s}{g_m}\left(R_S - \frac{1}{g_m}\right)} = \frac{1}{R_1} + \frac{1}{Ls}$$

$$\Rightarrow \quad L = \frac{C_{GS}}{g_m}\left(R_S - \frac{1}{g_m}\right)$$

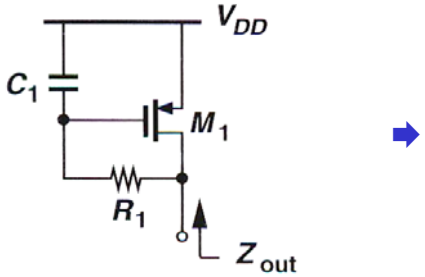


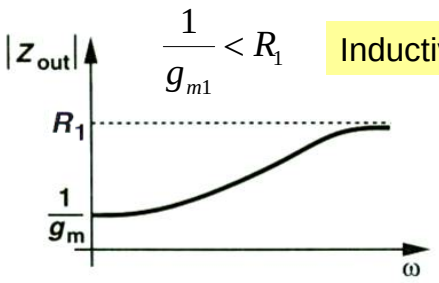

Drawback: Large voltage headroom consumption

L ↓ ➡ $g_m$ ↑ ➡ bias current ↑ ➡ $V_{GS}$ ↑



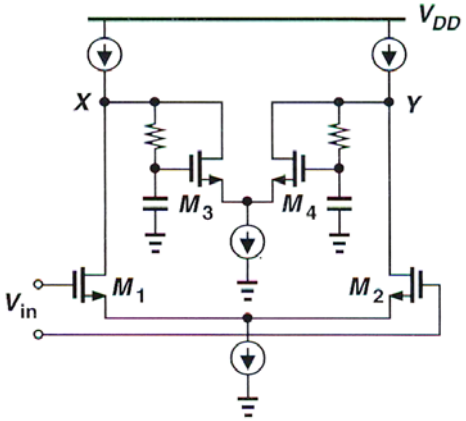
## MOS device configured as active inductor



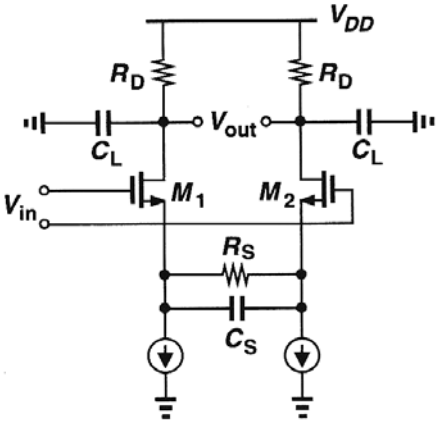

Inductive behavior

Differential amplifier with inductive load:



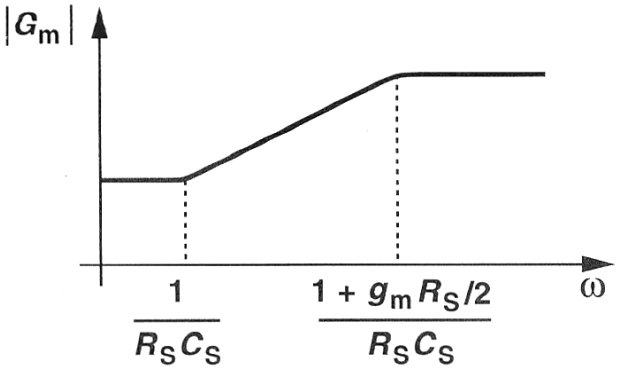

- NMOS active inductor
- Allow low-voltage operation
- Narrowband response:
  Large capacitances introduced at X&Y by the load current sources and $M_3$-$M_4$ limit the bandwidth to well below that achievable with passive inductors.

## Differential pair with capacitive degeneration (1/2)

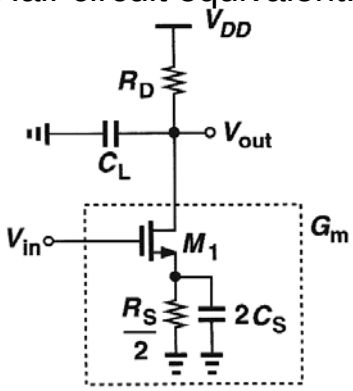



$$G_m = \frac{g_m}{1 + g_m\left(\frac{R_S}{2} \| \frac{1}{2C_S s}\right)} = \frac{g_m(R_S C_S s + 1)}{R_S C_S s + 1 + \frac{g_m R_S}{2}}$$

$$\omega_z = \frac{1}{R_S C_S} \qquad \omega_p = \frac{1 + \frac{g_m R_S}{2}}{R_S C_S}$$




Half-circuit equivalent:

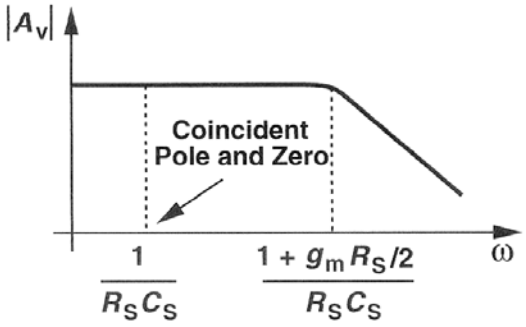





## Differential pair with capacitive degeneration (2/2)

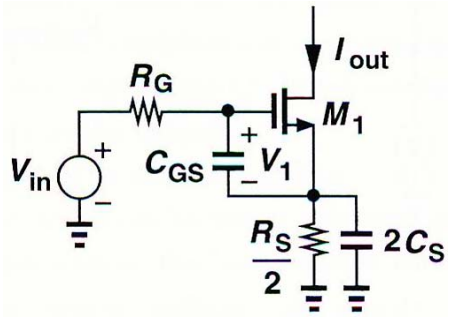
If the zero cancels the pole at the drain ➡ $R_S C_S = R_D C_L$

then the amplifier's bandwidth is extended to $\left(1 + \frac{g_m R_S}{2}\right)\frac{2}{R_S C_S} = \left(1 + \frac{g_m R_S}{2}\right)\frac{2}{R_D C_L}$.




- The speed is increased by a factor of $1+g_m R_S/2$.
- Reduced gain: $A_v = \frac{g_m R_D}{1 + \frac{g_m R_S}{2}}$.
- The thermal noise of $R_S$ may also pose difficulties.
- Benefit on input pole magnitude (See next)

## Input capacitance of a capacitively-degenerated stage




$$V_1 = \frac{I_{out}}{g_m}$$

$$\frac{I_{out}}{g_m} C_{GS} s R_G + \frac{I_{out}}{g_m} + \left( \frac{I_{out}}{g_m} C_{GS} s + I_{out} \right) \frac{R_S / 2}{R_S C_S s + 1} = V_{in}$$

$$\Rightarrow \quad \frac{I_{out}}{V_{in}} = \frac{g_m (R_S C_{GS} s + 1)}{R_G C_{GS} R_S C_S s^2 + (R_G C_{GS} + R_S C_S + R_S C_{GS} / 2) s + 1 + g_m R_S / 2}$$

Find poles (assuming $\omega_{p1} \ll \omega_{p2}$):

$$\omega_{p1} \approx \frac{1 + g_m R_S / 2}{R_G C_{GS} + R_S C_S + R_S C_{GS} / 2} \quad \Rightarrow \quad \omega_{p1} \approx \frac{1 + g_m R_S / 2}{R_G C_{GS}}$$

for $R_G C_{GS} \gg R_S (C_S + C_{GS} / 2)$

$$\omega_{p2} \approx \frac{1}{R_S C_S} + \frac{1}{R_G C_{GS}} + \frac{1}{2 R_G C_S}$$

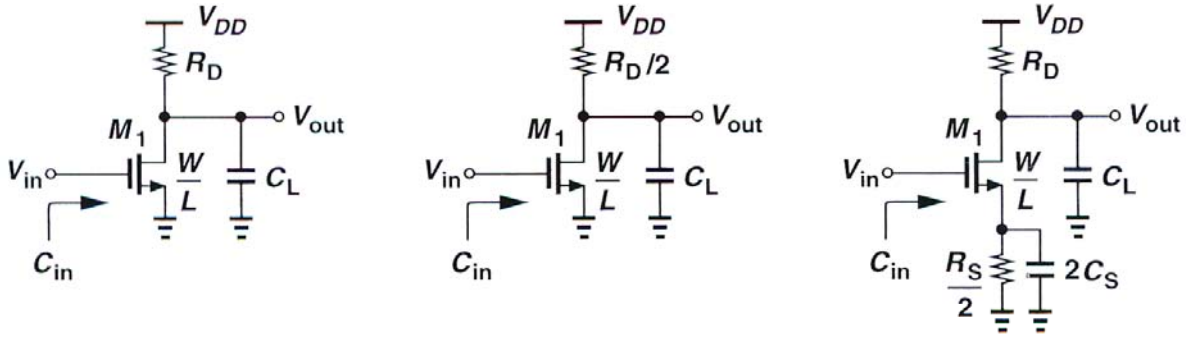
The input pole magnitude is increased by a factor of $1+g_mR_S/2$.

The zero: $\omega_z \approx \frac{1}{R_S C_S}$



## Three stages with & without capacitive degeneration

Assuming $g_mR_S$ of 2, equal bias current, and negligible Miller effect:




(a)

$$C_{in} \approx C_{GS}$$

$$|A_v| \approx g_m R_D$$

$$BW \approx \frac{1}{2\pi R_D C_L}$$

(b)

$$C_{in} \approx C_{GS}$$

$$|A_v| \approx g_m R_D / 2$$

$$BW \approx \frac{2}{2\pi R_D C_L}$$

(c)

$$C_{in} \approx C_{GS} / 2$$

$$|A_v| \approx g_m R_D / 2$$

$$BW \approx \frac{2}{2\pi R_D C_L}$$

## Cascade of differential pairs with capacitive degeneration

It is possible to allow the zero resulting from capacitive degeneration to cancel the pole $\omega_{p1}$. ➡ $\omega_z = \omega_{p1}$

$$\frac{1+g_m R_S/2}{R_G C_{GS} + R_S C_S + R_S C_{GS}/2} = \frac{1}{R_S C_S}$$

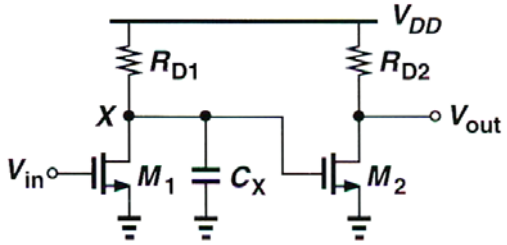
➡ $$\frac{C_S}{C_{GS}} = \frac{1}{g_m R_S}\left(\frac{2R_G}{R_S}+1\right)$$

Under this condition, $\omega_{p2}$ and the drain-substrate capacitance limit the bandwidth.



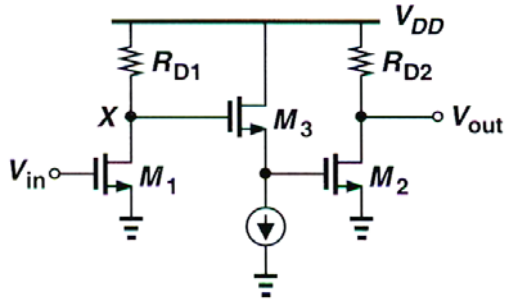
## Cascade & feedback for two-stage circuit (1/2)

- Cascade of two CS stages:




  - $|A_v| = g_{m1}R_{D1}$ and $\omega_{p,X} = \frac{1}{R_{D1}C_X}$.
  - 2nd stage:
    - $M_2$ must be wide enough to allow a reasonable gain.
    - $C_{GS2}$ and the Miller effect of $C_{CD2}$ may severely limit the bandwidth at node X.

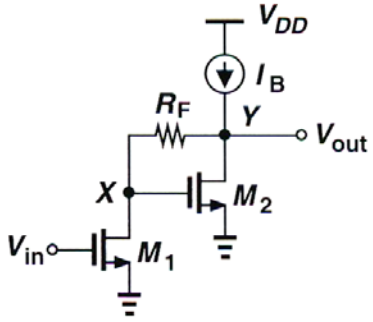
- Use of source follower as buffer:



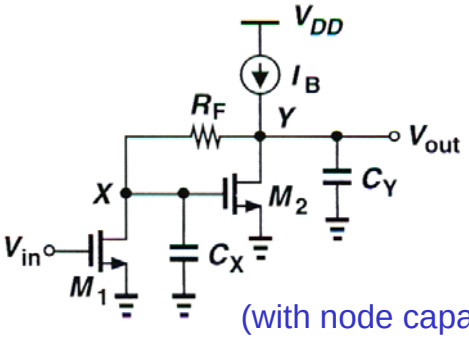

  - Interpose source follower to isolate node X from the input capacitance of the 2nd CS stage.
  - The follower consumes substantial voltage headroom, limiting
    - The allowable bias voltage across $R_{D1}$
    - The voltage gain
  - Attenuation by the follower if body effect and channel-length modulation.

## Cascade & feedback for two-stage circuit (2/2)

- Two stages with feedback:




➡




(with node capacitances)

Calculate low-frequency gain:

$$V_{out} - g_{m1}V_{in}R_F = V_X$$

$$g_{m2}V_X = -g_{m1}V_{in}$$

➡ $$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}}$$

If $R_F \gg g_{m2}^{-1}$, then the gain is equal to that of a simple CS stage.

Small-signal analysis:

- Small resistance at X and Y
- High-frequency poles:

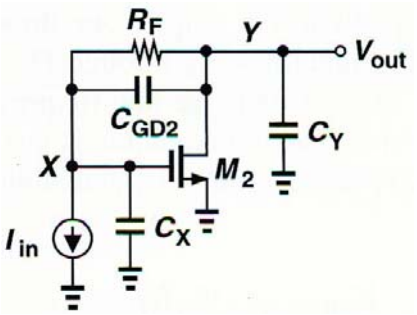
$$\omega_{p,X} \approx \frac{g_{m2}}{C_X} \text{ and } \omega_{p,Y} \approx \frac{g_{m2}}{C_Y}$$

(inaccurate)

- Cherry-Hooper amplifier, used in broadband applications.



## Equivalent circuit of Cherry-Hooper amplifier




$I_{in} = g_{m1}V_{in}$

$$(I_{in} + V_X C_X s)\left(R_F \parallel \frac{1}{C_{GD2}s}\right) + V_X = V_{out} \text{ and } -V_{out}C_Y s - g_{m2}V_X = I_{in} + V_X C_X s$$

➡ $$\frac{V_{out}}{I_{in}} = \frac{R_F^2 C_X C_{GD2} s^2 + (g_{m2}R_F C_{GD2} + C_X - C_{GD2})R_F s + g_{m2}R_F - 1}{R_F(C_X C_Y + C_{GD2}C_Y + C_{GD2}C_X)s^2 + (C_X + C_Y + g_{m2}R_F C_{GD2})s + g_{m2}}$$

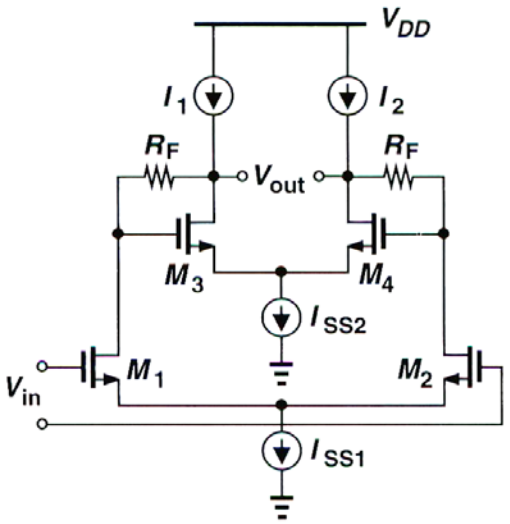
Suppose the two poles are **equal**:

$$\omega_{p1} = \omega_{p2} = \frac{2g_{m2}}{C_X + C_Y + g_{m2}R_F C_{GD2}} \approx \frac{g_{m2}}{\frac{C_X + C_Y}{2}}$$

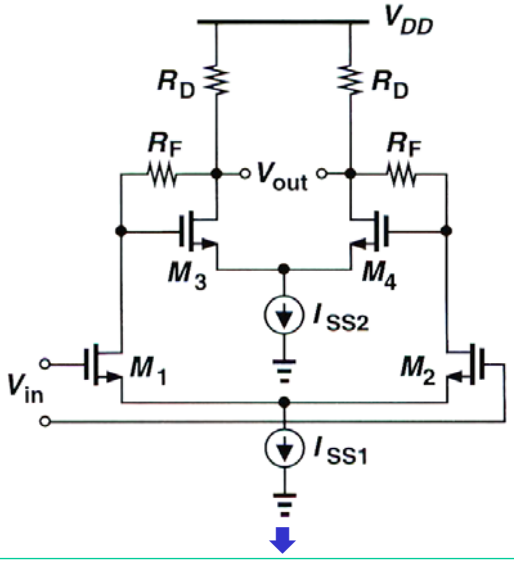
Much higher than those without feedback, e.g., $(R_F C_X)^{-1}$ or $(R_F C_Y)^{-1}$.

## Differential Cherry-Hooper amplifier

With current-source loads:




With resistive loads:



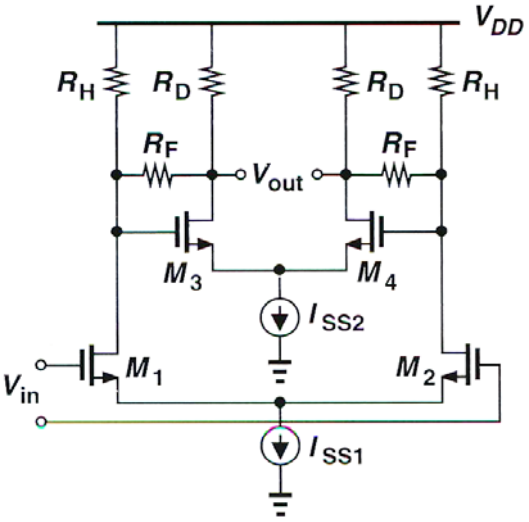

$$V_{DD,\min} = \frac{I_{SS1} + I_{SS2}}{2} R_D + \frac{I_{SS1}}{2} R_F + V_{GS3,4} + V_{ISS2}$$

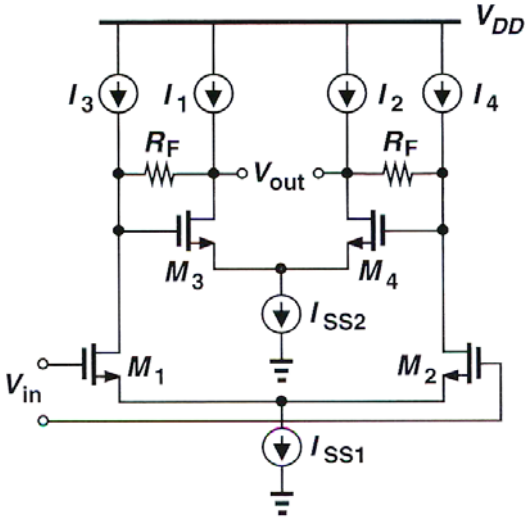
This constraint limits the voltage gain of the circuit.



## Modified Cherry-Hooper amplifier

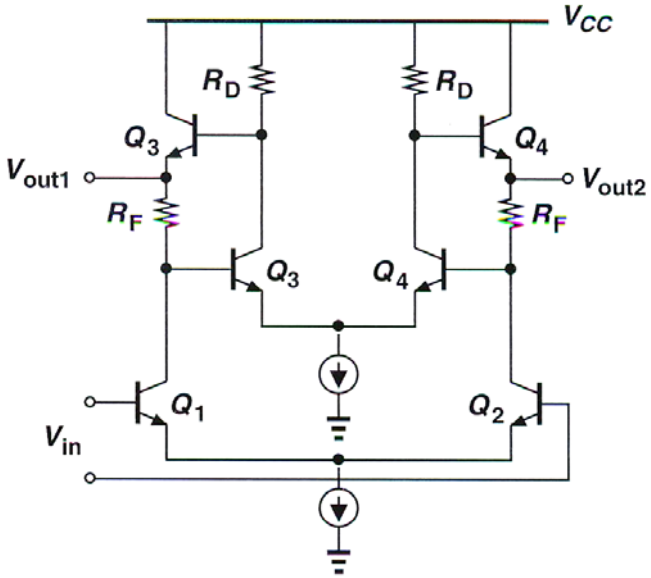
To alleviate the gain-headroom trade-off, the resistors or current sources provide part or all of the bias current of the input differential pair.




- $R_H$ must be much greater than the input resistance of 2nd stage (≈ $1/g_{m2}$ if $R_D$ is large) to avoid degrading the gain.
- Current sources $I_{1\text{-}4}$ (PMOS) may introduce substantial capacitance.

## Cherry-Hooper amplifier with emitter follower in FB loop



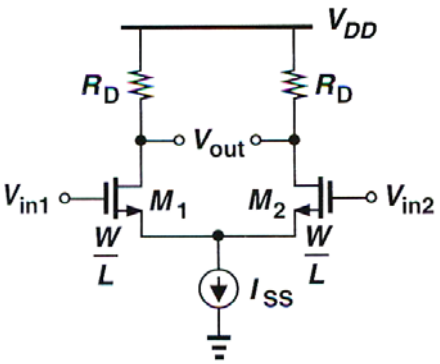

- Emitter followers are inserted in FB path so as to drive the load capacitance.
  - Isolate collectors of $Q_{3,4}$ from the load
  - Lower o/p impedance
  - High voltage headroom

- C.-H. amplifier proves more useful in the first few stages of LA than in the last few.
  - Benefits of FB: diminish as the signal amplitude increases
  - Differential pair experiences large signal operation



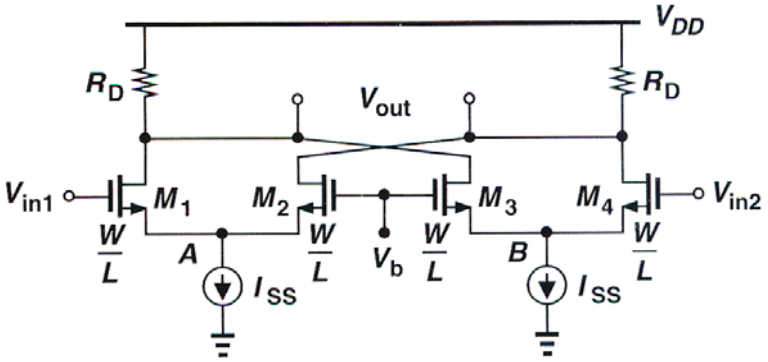
## $f_T$ doubler (1/2)

Simple differential stage:



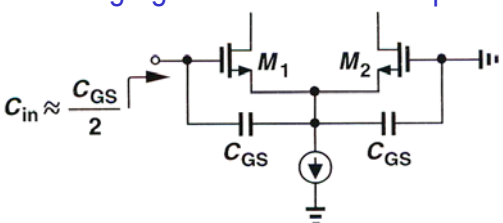

$$V_{out} = g_m(V_{in1} - V_{in2})R_D$$

$f_T$ doubler:




$$V_{out} = g_m(V_{in1} - V_{in2})R_D$$

The same voltage gain but with lower input capacitance!




(parasitic capacitance at A,B is negligible)

## $f_T$ doubler (2/2)

Drawbacks:

- Power dissipation is doubled.
- Total current flowing through $R_D$ is doubled, possibly driving the transistors into the triode region.
- Total capacitance contributed to the output is double, lowering the output pole.
- If the source-bulk junction capacitance of the transistors and the capacitance introduced by the tail current sources is not negligible, the input capacitance is higher than $C_{GS}/2$.