BSIM4.5.0 MOSFET Model

- User's Manual

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Web Sites:

BSIM4 web site with BSIM source code and documents:

http://www-device.eecs.berkeley.edu/bsim3/~bsim4.html

Compact Model Council: **http://www.eigroup.org/~CMC**

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Chapter 1: Effective Oxide Thickness, Channel Length and Channel Width

BSIM4, as the extension of BSIM3 model, addresses the MOSFET physical effects into sub-100nm regime. The continuous scaling of minimum feature size brought challenges to compact modeling in two ways: One is that to push the barriers in making transistors with shorter gate length, advanced process technologies are used such as non-uniform substrate doping. The second is its opportunities to RF applications.

To meet these challenges, BSIM4 has the following major improvements and additions over BSIM3v3: (1) an accurate new model of the intrinsic input resistance for both RF, high-frequency analog and high-speed digital applications; (2) flexible substrate resistance network for RF modeling; (3) a new accurate channel thermal noise model and a noise partition model for the induced gate noise; (4) a non-quasi-static (NQS) model that is consistent with the Rg-based RF model and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances. (5) an accurate gate direct tunneling model for multiple layer gate dielectrics; (6) a comprehensive and versatile geometry-dependent parasitics model for various source/drain connections and multi-finger devices; (7) improved model for steep vertical retrograde doping profiles; (8) better model for pocket-implanted devices in Vth, bulk charge effect model, and Rout; (9) asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET at the user's discretion; (10) acceptance of either the electrical or physical gate oxide thickness as the model input at the user's

choice in a physically accurate maner; (11) the quantum mechanical charge-layer-thickness model for both IV and CV; (12) a more accurate mobility model for predictive modeling; (13) a gate-induced drain/source leakage (GIDL/GISL) current model, available in BSIM for the first time; (14) an improved unified flicker (1/f) noise model, which is smooth over all bias regions and considers the bulk charge effect; (15) different diode IV and CV charatistics for source and drain junctions; (16) junction diode breakdown with or without current limiting; (17) dielectric constant of the gate dielectric as a model parameter; (18) A new scalable stress effect model for process induced stress effect; device performance becoming thus a function of the active area geometry and the location of the device in the active area; (19) A unified current-saturation model that includes all mechanisms of current saturation- velocity saturation, velocity overshoot and source end velocity limit; (20) A new temperature model format that allows convenient prediction of temperature effects on saturation velocity, mobility, and S/D resistances.

1.1Gate Dielectric Model

As the gate oxide thickness is vigorously scaled down, the finite charge-layer thickness can not be ignored [1]. BSIM4 models this effect in both IV and CV. For this purpose, BSM4 accepts two of the following three as the model inputs: the electrical gate oxide thickness *TOXE*[1], the physical gate oxide thickness *TOXP*, and their difference *DTOX* = *TOXE* - *TOXP*. Based on these parameters, the effect of effective gate oxide capacitance C_{oxeff} on IV and CV is modeled [2].

1. Capital and italic alphanumericals in this manual are model parameters.

High-*k* gate dielectric can be modeled as SiO_2 (relative permittivity: 3.9) with an equivalent SiO_2 thickness. For example, 3nm gate dielectric with a dielectric constant of 7.8 would have an equivalent oxide thickness of 1.5nm.

BSIM4 also allows the user to specify a gate dielectric constant (*EPSROX*) different from 3.9 (SiO_2) as an alternative approach to modeling high-*k* dielectrics.

Figure 1-1 illustrates the algorithm and options for specifying the gate dielectric thickness and calculation of the gate dielectric capacitance for BSIM4 model evaluation.

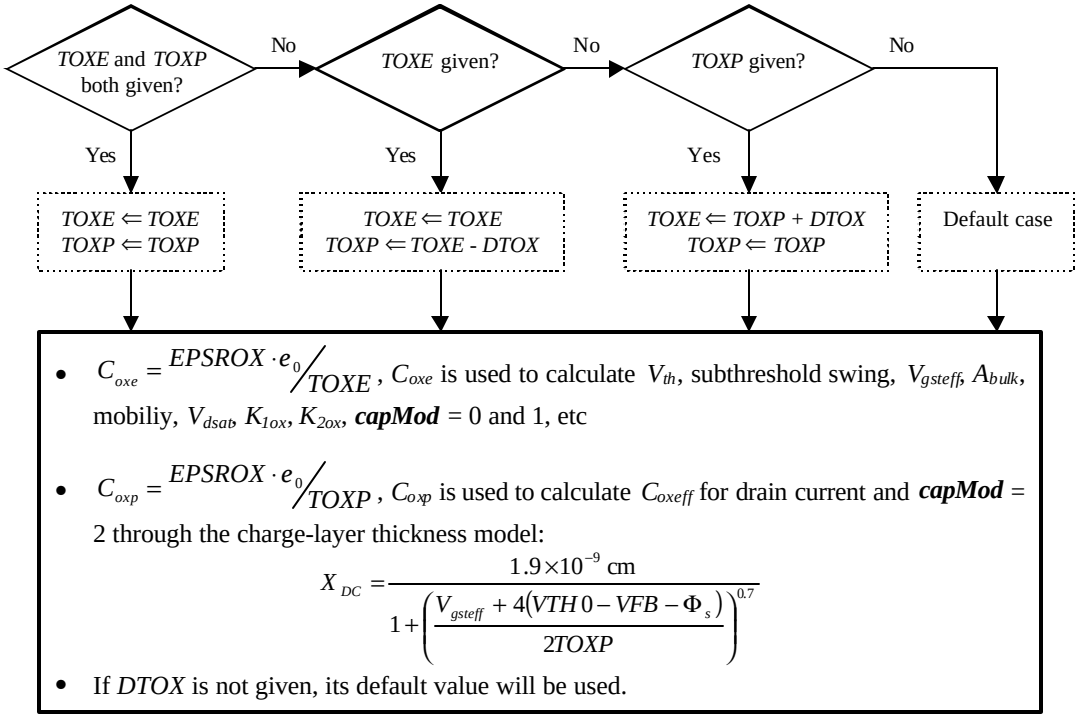


Figure 1-1. Algorithm for BSIM4 gate dielectric model.

1.2 Poly-Silicon Gate Depletion

When a gate voltage is applied to the poly-silicon gate, e.g. NMOS with n^+ poly-silicon gate, a thin depletion layer will be formed at the interface between the poly-silicon and the gate oxide. Although this depletion layer is very thin due to the high doping concentration of the poly-silicon gate, its effect cannot be ignored since the gate oxide thickness is small.

Figure 1-2 shows an NMOSFET with a depletion region in the n^+ poly-silicon gate. The doping concentration in the n^+ poly-silicon gate is *NGATE* and the doping concentration in the substrate is *NSUB*. The depletion width in the poly gate is X_p. The depletion width in the substrate is X_d. The positive charge near the interface of the poly-silicon gate and the gate oxide is distributed over a finite depletion region with thickness X_p. In the presence of the depletion region, the voltage drop across the gate oxide and the substrate will be reduced, because part of the gate voltage will be dropped across the depletion region in the gate. That means the effective gate voltage will be reduced.

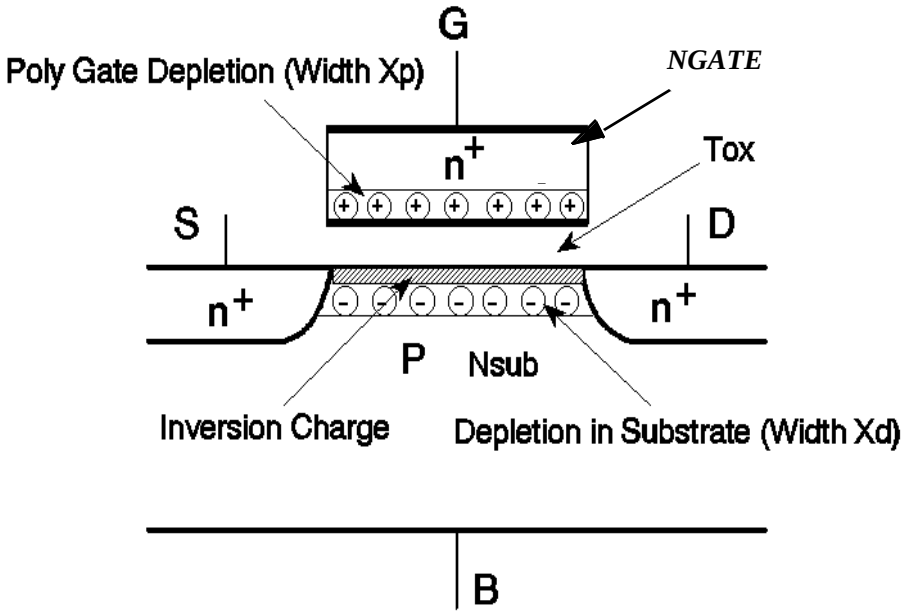


Figure 1-2. Charge distribution in a MOSFET with the poly gate depletion effect. The device is in the strong inversion region.

The effective gate voltage can be calculated in the following manner. Assume the doping concentration in the poly gate is uniform. The voltage drop in the poly gate V_{poly} can be calculated as

(1.2.1)

$$V_{poly} = 0.5 X_{poly} E_{poly} = \frac{qNGATE \cdot X_{poly}^2}{2e_{si}}$$

where E_{poly} is the maximum electrical field in the poly gate. The boundary condition at the interface of poly gate and the gate oxide is

(1.2.2)

$$EPSROX \cdot E_{ox} = e_{si} E_{poly} = \sqrt{2qe_{si} NGATE \cdot V_{poly}}$$

where E_{ox} is the electric field in the gate oxide. The gate voltage satisfies

(1.2.3)

$$V_{gs} - V_{FB} - \Phi_s = V_{poly} + V_{ox}$$

where V_{ox} is the voltage drop across the gate oxide and satisfies $V_{ox} = E_{ox}TOXE$.

From (1.2.1) and (1.2.2), we can obtain

(1.2.4)

$$a\left(V_{gs} - V_{FB} - \Phi_s - V_{poly}\right)^2 - V_{poly} = 0$$

where

(1.2.5)

$$a = \frac{EPSROX^2}{2qe_{si} NGATE \cdot TOXE^2}$$

By solving (1.2.4), we get the effective gate voltage V_{gse} which is equal to

(1.2.6)

$$V_{gse} = VFB + \Phi_s + \frac{qe_{si} NGATE \cdot TOXE^2}{EPSROX^2}\left(\sqrt{1 + \frac{2EPSROX^2\left(V_{gs} - VFB - \Phi_s\right)}{qe_{si} NGATE \cdot TOXE^2}} - 1\right)$$

1.3 Effective Channel Length and Width

The effective channel length and width used in the drain current model are given below where XL and XW are parameters to account the channel length/width offset due to mask/etch effect

(1.3.1)

$$L_{eff} = L_{drawn} + XL - 2dL$$

(1.3.2a)

$$W_{eff} = \frac{W_{drawn}}{NF} + XW - 2dW$$

(1.3.2b)

$$W_{eff}' = \frac{W_{drawn}}{NF} + XW - 2dW'$$

The difference between (1.3.2a) and (1.3.2b) is that the former includes bias dependencies. *NF* is the number of device fingers. *dW* and *dL* are modeled by

(1.3.3)

$$dW = dW' + DWG \cdot V_{gsteff} + DWB\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right)$$
$$dW' = WINT + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WWN}} + \frac{WWL}{L^{WLN} W^{WWN}}$$

(1.3.4)

$$dL = LINT + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN} W^{LWN}}$$

WINT represents the traditional manner from which "delta *W*" is extracted (from the intercept of straight lines on a $1/R_{ds}$~W_{drawn} plot). The parameters *DWG* and *DWB* are used to account for the contribution of both gate and substrate bias effects. For *dL*, *LINT* represents the traditional manner from which "delta *L*" is extracted from the intercept of lines on a R_{ds}~L_{drawn} plot).

The remaining terms in *dW* and *dL* are provided for the convenience of the user. They are meant to allow the user to model each parameter as a function of W_{drawn}, L_{drawn} and their product term. By default, the above geometrical dependencies for *dW* and *dL* are turned off.

MOSFET capacitances can be divided into intrinsic and extrinsic components. The intrinsic capacitance is associated with the region between the metallurgical source and drain junction, which is defined by the effective length (L_{active}) and width (W_{active}) when the gate to source/drain regions are under flat-band condition. L_{active} and W_{active} are defined as

$$L_{active} = L_{drawn} + XL - 2dL \tag{1.3.5}$$

$$W_{active} = \frac{W_{drawn}}{NF} + XW - 2dW \tag{1.3.6}$$

$$dL = DLC + \frac{LLC}{L^{LLN}} + \frac{LWC}{W^{LWN}} + \frac{LWLC}{L^{LLN} W^{LWN}} \tag{1.3.7}$$

$$dW = DWC + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN}W^{WWN}} \tag{1.3.8}$$

The meanings of *DWC* and *DLC* are different from those of *WINT* and *LINT* in the I-V model. Unlike the case of I-V, we assume that these dimensions are bias-dependent. The parameter dL_{eff} is equal to the source/drain to gate overlap length plus the difference between drawn and actual POLY CD due to processing (gate patterning, etching and oxidation) on one side.

The effective channel length L_{eff} for the I-V model does not necessarily carry a physical meaning. It is just a parameter used in the I-V formulation. This L_{eff} is therefore very sensitive to the I-V equations and also to the conduction characteristics of the LDD region relative to the channel region. A device with a large L_{eff} and a small parasitic resistance can have a similar current drive as another with a smaller L_{eff} but larger R_{ds}.

The L_{active} parameter extracted from capacitance is a closer representation of the metallurgical junction length (physical length). Due to the graded source/drain junction profile, the source to drain length can have a very strong bias dependence. We therefore define L_{active} to be that measured at flat-band voltage between gate to source/drain. If *DWC*, *DLC* and the length/width dependence parameters (*LLC*, *LWC*, *LWLC*, *WLC*, *WWC* and *WWLC*) are not specified in technology files, BSIM4 assumes that the DC bias-independent L_{eff} and W_{eff} will be used for the capacitnace models, and *DWC*, *DLC*, *LLC*, *LWC*, *LWLC*, *WLC*, *WWC* and *WWLC* will be set to the values of their DC counterparts.

BSIM4 uses the effective source/drain diffusion width W_{effcj} for modeling parasitics, such as source/drain resistance, gate electrode resistance, and gate-induced drain leakage (GIDL) current. W_{effcj} is defined as

$$W_{effcj} = \frac{W_{drawn}}{NF} - 2 \cdot \left(DWJ + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN} W^{WWN}} \right) \tag{1.3.9}$$

Note: Any compact model has its validation limitation, so does BSIM4. BSIM4 is its own valid designation limit which is larger than the warning limit, shown in following table. For users' reference, the fatal limitation in BSIM4 is also shown.

Parameter name	Designed Limitation(m)	Warning Limitation(m)	Fatal Limitation(m)
Leff	1e-8	1e-9	0
LeffCV	1e-8	1e-9	0
Weff	1e-7	1e-9	0
WeffCV	1e-7	1e-9	0
Toxe	5e-10	1e-10	0
Toxp	5e-10	1e-10	0
Toxm	5e-10	1e-10	0

Table 1-1. BSIM4.5.0 Geometry Limitation

Chapter 2: Threshold Voltage Model

2.1 Long-Channel Model With Uniform Doping

Accurate modeling of threshold voltage V_{th} is important for precise description of device electrical characteristics. V_{th} for long and wide MOSFETs with uniform substrate doping is given by

$$V_{th} = VFB + \Phi_s + g\sqrt{\Phi_s - V_{bs}} = VTH0 + g\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) \tag{2.1.1}$$

where *VFB* is the flat band voltage, *VTH0* is the threshold voltage of the long channel device at zero substrate bias, and γ is the body bias coefficient given by

$$g = \frac{\sqrt{2qe_{si}N_{substrate}}}{C_{oxe}} \tag{2.1.2}$$

where $N_{substrate}$ is the uniform substrate doping concentration.

Equation (2.1.1) assumes that the channel doping is constant and the channel length and width are large enough. Modifications have to be made when the substrate doping concentration is not constant and/or when the channel is short, or narrow.

Consider process variation, a new instance parameter DELVTO is added to VTH0 as:

(a) If VTH0 is given,

(2.1.3)

$$VTH0 = VTH0 + DELVTO$$

(a) If VTH0 isn't given,

(2.1.4)

$$VFB = VFB + DELVTO$$
$$VTH0 = VFB + \Phi_s + \gamma\sqrt{\Phi_s}$$

2.2 Non-Uniform Vertical Doping

The substrate doping profile is not uniform in the vertical direction and therefore γ in (2.1.2) is a function of both the depth from the interface and the substrate bias. If $N_{substrate}$ is defined to be the doping concentration (*NDEP*) at X_{dep0} (the depletion edge at V_{bs} = 0), V_{th} for non-uniform vertical doping is

(2.2.1)

$$V_{th} = V_{th,NDEP} + \frac{qD_0}{C_{oxe}} + K1_{NDEP}\left(\sqrt{\phi_s - V_{bs} - \frac{qD_1}{\varepsilon_{si}}} - \sqrt{\phi_s - V_{bs}}\right)$$

where $K1_{NDEP}$ is the body-bias coefficient for $N_{substrate}$ = *NDEP*,

(2.2.2)

$$V_{th,NDEP} = VTH0 + K1_{NDEP}\left(\sqrt{j_s - V_{bs}} - \sqrt{j_s}\right)$$

with a definition of

(2.2.3)

$$j_s = 0.4 + \frac{k_B T}{q}\ln\left(\frac{NDEP}{n_i}\right)$$

where n_i is the intrinsic carrier concentration in the channel region. The zero-th and 1st moments of the vertical doping profile in (2.2.1) are given by (2.2.4) and (2.2.5), respectively, as

(2.2.4)

$$D_0 = D_{00} + D_{01} = \int_0^{X_{dep0}} \left(N(x) - NDEP\right)dx + \int_{X_{dep0}}^{X_{dep}} \left(N(x) - NDEP\right)dx$$

(2.2.5)

$$D_1 = D_{10} + D_{11} = \int_0^{X_{dep0}} \left(N(x) - NDEP\right)xdx + \int_{X_{dep0}}^{X_{dep}} \left(N(x) - NDEP\right)xdx$$

By assuming the doping profile is a steep retrograde, it can be shown that D_{01} is approximately equal to -$C_{01}V_{bs}$ and that D_{10} dominates D_{11}; C_{01} represents the profile of the retrograde. Combining (2.2.1) through (2.2.5), we obtain

(2.2.6)

$$V_{th} = VTH0 + K1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) - K2 \cdot V_{bs}$$

where $K2 = qC_{01} / C_{oxe}$, and the surface potential is defined as

$$\Phi_s = 0.4 + \frac{k_B T}{q} \ln\left(\frac{NDEP}{n_i}\right) + PHIN \tag{2.2.7}$$

where

$$PHIN = -qD_{10}/e_{si}$$

*VTH*0, *K*1, *K*2, and *PHIN* are implemented as model parameters for model flexibility. Appendix A lists the model selectors and parameters.

Detail information on the doping profile is often available for predictive modeling. Like BSIM3v3, BSIM4 allows *K*1 and *K*2 to be calculated based on such details as *NSUB*, *XT*, *VBX*, *VBM*, etc. (with the same meanings as in BSIM3v3):

$$K1 = g_2 - 2K2\sqrt{\Phi_s - VBM} \tag{2.2.8}$$

$$K2 = \frac{(g_1 - g_2)\left(\sqrt{\Phi_s - VBX} - \sqrt{\Phi_s}\right)}{2\sqrt{\Phi_s}\left(\sqrt{\Phi_s - VBM} - \sqrt{\Phi_s}\right) + VBM} \tag{2.2.9}$$

where γ_1 and γ_2 are the body bias coefficients when the substrate doping concentration are equal to *NDEP* and *NSUB*, respectively:

(2.2.10)

$$g_1 = \frac{\sqrt{2qe_{si}NDEP}}{C_{oxe}}$$

(2.2.11)

$$g_2 = \frac{\sqrt{2qe_{si}NSUB}}{C_{oxe}}$$

VBX is the body bias when the depletion width is equal to *XT*, and is determined by

(2.2.12)

$$\frac{qNDEP \cdot XT^2}{2e_{si}} = \Phi_s - VBX$$

2.3 Non-Uniform Lateral Doping: Pocket (Halo) Implant

In this case, the doping concentration near the source/drain junctions is higher than that in the middle of the channel. Therefore, as channel length becomes shorter, a V_{th} roll-up will usually result since the effective channel doping concentration gets higher, which changes the body bias effect as well. To consider these effects, V_{th} is written as

(2.3.1)

$$V_{th} = VTH0 + K1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right)\cdot\sqrt{1+\frac{LPEB}{L_{eff}}} - K2\cdot V_{bs} + K1\left(\sqrt{1+\frac{LPE0}{L_{eff}}} - 1\right)\sqrt{\Phi_s}$$

In addition, pocket implant can cause significant drain-induced threshold shift (DITS) in long-channel devices [3]:

(2.3.2)

$$\Delta V_{th}(DITS) = -nv_t \cdot \ln\left(\frac{\left(1-e^{-V_{ds}/v_t}\right)\cdot L_{eff}}{L_{eff} + DVTP0\cdot\left(1+e^{-DVTP1\cdot V_{ds}}\right)}\right)$$

For V_{ds} of interest, the above equation is simplified and implemented as

for tempMod = 1:

(2.3.3a)

$$\Delta V_{th}(DITS) = -nv_t \times \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \times \left(1 + e^{-DVTP1\times V_{ds}}\right)}\right)$$

for tempMod = 2:

(2.3.3b)

$$\Delta V_{th}(DITS) = -nv_{tnom} \times \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \times \left(1 + e^{-DVTP1\times V_{ds}}\right)}\right)$$

Note: when tempMod =2, drain-induced threshold voltage shift (DITS) due to pocket implant has no temperature dependence, so nominal temperature (TNOM) is used as equation(2.3.4). when tempMod=0 or 1, equation(2.3.3) is used.

(2.3.4)

$$\Delta V_{th}(DITS) = -n v_{tnom} \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot \left(1 + e^{-DVTP1 \cdot V_{ds}}\right)}\right)$$

2.4 Short-Channel and DIBL Effects

As channel length becomes shorter, V_{th} shows a greater dependence on channel length (SCE: short-channel effect) and drain bias (DIBL: drain-induced barrier lowering). V_{th} dependence on the body bias becomes weaker as channel length becomes shorter, because the body bias has weaker control of the depletion region. Based on the quasi 2D solution of the Poisson equation, V_{th} change due to SCE and DIBL is modeled [4]

(2.4.1)

$$\Delta V_{th}(SCE, DIBL) = -q_{th}(L_{eff}) \cdot [2(V_{bi} - \Phi_s) + V_{ds}]$$

where V_{bi}, known as the built-in voltage of the source/drain junctions, is given by

(2.4.2)

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{NDEP \cdot NSD}{n_i^2}\right)$$

where *NSD* is the doping concentration of source/drain diffusions. The short-channel effect coefficient $\theta_{th}(L_{eff})$ in (2.4.1) has a strong dependence on the channel length given by

(2.4.3)

$$q_{th}(L_{eff}) = \frac{0.5}{\cosh\left(\frac{L_{eff}}{l_t}\right) - 1}$$

l_t is referred to as the characteristic length and is given by

(2.4.4)

$$l_t = \sqrt{\frac{e_{si} \cdot TOXE \cdot X_{dep}}{EPSROX \cdot h}}$$

with the depletion width X_{dep} equal to

(2.4.5)

$$X_{dep} = \sqrt{\frac{2e_{si}(\Phi_s - V_{bs})}{qNDEP}}$$

X_{dep} is larger near the drain due to the drain voltage. X_{dep} / η represents the average depletion width along the channel.

Note that in BSIM3v3 and [4], $\theta_{th}(L_{eff})$ is approximated with the form of

(2.4.6)

$$q_{th}(L_{eff}) = \exp\left(-\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-\frac{L_{eff}}{l_t}\right)$$

which results in a phantom second V_{th} roll-up when L_{eff} becomes very small (e.g. L_{eff} < *LMIN*). In BSIM4, the function form of (2.4.3) is implemented with no approximation.

To increase the model flexibility for different technologies, several parameters such as *DVT*0, *DVT*1, *DVT*2, *DSUB*, *ETA*0, and *ETAB* are introduced, and SCE and DIBL are modeled separately.

To model SCE, we use

$$q_{th}(\mathrm{SCE}) = \frac{0.5 \cdot DVT0}{\cosh\left(DVT1 \cdot \frac{L_{eff}}{l_t}\right) - 1} \tag{2.4.7}$$

$$\Delta V_{th}(\mathrm{SCE}) = -q_{th}(\mathrm{SCE}) \cdot (V_{bi} - \Phi_s) \tag{2.4.8}$$

with l_t changed to

$$l_t = \sqrt{\frac{e_{si} \cdot TOXE \cdot X_{dep}}{EPSROX}} \cdot (1 + DVT2 \cdot V_{bs}) \tag{2.4.9}$$

To model DIBL, we use

$$q_{th}(\mathrm{DIBL}) = \frac{0.5}{\cosh\left(DSUB \cdot \frac{L_{eff}}{l_{t0}}\right) - 1} \tag{2.4.10}$$

(2.4.11)

$$\Delta V_{th}(\text{DIBL}) = -q_{th}(\text{DIBL})\cdot(ETA0 + ETAB\cdot V_{bs})\cdot V_{ds}$$

and l_{t0} is calculated by

(2.4.12)

$$l_{t0} = \sqrt{\frac{e_{si}\cdot TOXE\cdot X_{dep0}}{EPSROX}}$$

with

(2.4.13)

$$X_{dep0} = \sqrt{\frac{2e_{si}\Phi_s}{qNDEP}}$$

*DVT*1 is basically equal to $1/(\eta)^{1/2}$. *DVT*2 and *ETAB* account for substrate bias effects on SCE and DIBL, respectively.

2.5 Narrow-Width Effect

The actual depletion region in the channel is always larger than what is usually assumed under the one-dimensional analysis due to the existence of fringing fields. This effect becomes very substantial as the channel width decreases and the depletion region underneath the fringing field becomes comparable to the "classical" depletion layer formed from the vertical field. The net result is an increase in V_{th}. This increase can be modeled as

(2.5.1)

$$\frac{pqNDEP \cdot X_{dep,\max}^{\ 2}}{2C_{oxe}W_{eff}} = 3p\ \frac{TOXE}{W_{eff}}\Phi_s$$

This formulation includes but is not limited to the inverse of channel width due to the fact that the overall narrow width effect is dependent on process (i.e. isolation technology). V_{th} change is given by

(2.5.2)

$$\Delta V_{th}\left(Narrow\_width1\right) = \left(K3 + K3B \cdot V_{bs}\right)\frac{TOXE}{W_{eff}' + W0}\Phi_s$$

In addition, we must consider the narrow width effect for small channel lengths. To do this we introduce the following

(2.5.3)

$$\Delta V_{th}\left(Narrow\_width2\right) = -\frac{0.5 \cdot DVT0W}{\cosh\left(DVT1W \cdot \frac{L_{eff}W_{eff}'}{l_{tw}}\right) - 1} \cdot \left(V_{bi} - \Phi_s\right)$$

with l_{tw} given by

(2.5.4)

$$l_{tw} = \sqrt{\frac{e_{si} \cdot TOXE \cdot X_{dep}}{EPSROX}} \cdot \left(1 + DVT2W \cdot V_{bs}\right)$$

The complete V_{th} model implemented in SPICE is

(2.5.5)

$$
\begin{aligned}
V_{th} = {} & VTH0 + \left(K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K1\cdot\sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K_{2ox}V_{bseff} \\
& + K_{1ox}\left(\sqrt{1+\frac{LPE0}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + \left(K3 + K3B\cdot V_{bseff}\right)\frac{TOXE}{W_{eff}' + W0}\Phi_s \\
& - 0.5\cdot\left[\frac{DVT0W}{\cosh\left(DVT1W\frac{L_{eff}W_{eff}'}{l_{tw}}\right)-1} + \frac{DVT0}{\cosh\left(DVT1\frac{L_{eff}}{l_t}\right)-1}\right]\left(V_{bi} - \Phi_s\right) \\
& - \frac{0.5}{\cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right)-1}\left(ETA0 + ETAB\cdot V_{bseff}\right)\cdot V_{ds} - nv_t.ln\left(\frac{L_{eff}}{L_{eff} + DVTP0.\left(1+e^{-DVTP1\cdot V_{DS}}\right)}\right)
\end{aligned}
$$

where *TOXE* dependence is introduced in model parameters *K*1 and *K*2 to improve the scalibility of V_{th} model over *TOXE* as

(2.5.6)

$$K_{1ox} = K1\cdot\frac{TOXE}{TOXM}$$

and

(2.5.7)

$$K_{2ox} = K2\cdot\frac{TOXE}{TOXM}$$

Note that all V_{bs} terms are substituted with a V_{bseff} expression as shown in (2.5.8). This is needed in order to set a low bound for the body bias during simulations since unreasonable values can occur during SPICE iterations if this expression is not introduced.

(2.5.8)

$$V_{bseff} = V_{bc} + 0.5 \cdot \left[(V_{bs} - V_{bc} - d_1) + \sqrt{(V_{bs} - V_{bc} - d_1)^2 - 4d_1 \cdot V_{bc}} \right]$$

where δ_1 = 0.001V, and V_{bc} is the maximum allowable V_{bs} and found from dV_{th}/dV_{bs}= 0 to be

(2.5.9)

$$V_{bc} = 0.9\left(\Phi_s - \frac{K1^2}{4K2^2} \right)$$

For positive $V_{bs,}$ there is need to set an upper bound for the body bias as:

(2.5.10)

$$V_{bseff} = 0.95\Phi_s - 0.5\left(0.95\Phi_s - V'_{bseff} - d_1 + \sqrt{\left(0.95\Phi_s - V'_{bseff} - d_1\right)^2 + 4d_1 \cdot 0.95\Phi_s}\right)$$

Chapter 3: Channel Charge and Subthreshold Swing Models

3.1 Channel Charge Model

The channel charge density in subthreshold for zero V_{ds} is written as

(3.1.1)

$$Q_{chsubs0} = \sqrt{\frac{qNDEPe_{si}}{2\Phi_s}} v_t \cdot \exp\left(\frac{V_{gse} - V_{th} - Voff'}{nv_t}\right)$$

where

(3.1.1a)

$$Voff' = VOFF + \frac{VOFFL}{L_{eff}}$$

VOFFL is used to model the length dependence of *Voff*' on non-uniform channel doping profiles.

In strong inversion region, the density is expressed by

(3.1.2)

$$Q_{chs0} = C_{oxe} \cdot \left(V_{gse} - V_{th}\right)$$

A unified charge density model considering the charge layer thickness effect is derived for both subthreshold and inversion regions as

(3.1.3)

$$Q_{ch0} = C_{oxeff} \cdot V_{gsteff}$$

where C_{oxeff} is modeled by

(3.1.4)

$$C_{oxeff} = \frac{C_{oxe} \cdot C_{cen}}{C_{oxe} + C_{cen}} \quad with\, C_{cen} = \frac{e_{si}}{X_{DC}}$$

and X_{DC} is given as

(3.1.5)

$$X_{DC} = \frac{1.9 \times 10^{-9}\ \mathrm{m}}{1 + \left(\frac{V_{gsteff} + 4(VTH0 - VFB - \Phi_s)}{2TOXP} \right)^{0.7}}$$

In the above equations, V_{gsteff}, the effective (V_{gse}-V_{th}) used to describe the channel charge densities from subthreshold to strong inversion, is modeled by

(3.1.6a)

$$V_{gsteff} = \frac{nv_t \ln\left\{1 + \exp\left[\frac{m^*(V_{gse} - V_{th})}{nv_t}\right]\right\}}{m^* + nC_{oxe} \cdot \sqrt{\frac{2\Phi_s}{qNDEP\varepsilon_{si}}} \exp\left[-\frac{(1 - m^*)(V_{gse} - V_{th}) - Voff'}{nv_t}\right]}$$

where

(3.1.6b)

$$m* = 0.5 + \frac{\arctan(MINV)}{p}$$

MINV is introduced to improve the accuracy of G_m, G_m/I_d and G_m^2/I_d in the moderate inversion region.

To account for the drain bias effect, The y dependence has to be included in (3.1.3). Consider first the case of strong inversion

$$Q_{chs}(y) = C_{oxeff} \cdot (V_{gse} - V_{th} - A_{bulk} V_F(y)) \tag{3.1.7}$$

$V_F(y)$ stands for the quasi-Fermi potential at any given point y along the channel with respect to the source. (3.1.7) can also be written as

$$Q_{chs}(y) = Q_{chs0} + \Delta Q_{chs}(y) \tag{3.1.8}$$

The term $\Delta Q_{chs}(y) = -C_{oxeff} A_{bulk} V_F(y)$ is the incremental charge density introduced by the drain voltage at y.

In subthreshold region, the channel charge density along the channel from source to drain can be written as

$$Q_{chsubs}(y) = Q_{chsubs0} \cdot \exp\left(-\frac{A_{bulk} V_F(y)}{n v_t}\right) \tag{3.1.9}$$

Taylor expansion of (3.1.9) yields the following (keeping the first two terms)

(3.1.10)

$$Q_{chsubs}(y) = Q_{chsubs0}\left(1 - \frac{A_{bulk}V_F(y)}{nv_t}\right)$$

Similarly, (3.1.10) is transformed into

(3.1.11)

$$Q_{chsubs}(y) = Q_{chsubs0} + \Delta Q_{chsubs}(y)$$

where $\Delta Q_{chsubs}(y)$ is the incremental channel charge density induced by the drain voltage in the subthreshold region. It is written as

(3.1.12)

$$\Delta Q_{chsubs}(y) = -Q_{chsubs0} \cdot \frac{A_{bulk}V_F(y)}{nv_t}$$

To obtain a unified expression for the incremental channel charge density $\Delta Q_{ch}(y)$ induced by V_{ds}, we assume $\Delta Q_{ch}(y)$ to be

(3.1.13)

$$\Delta Q_{ch}(y) = \frac{\Delta Q_{chs}(y) \cdot \Delta Q_{chsubs}(y)}{\Delta Q_{chs}(y) + \Delta Q_{chsubs}(y)}$$

Substituting $\Delta Q_{ch}(y)$ of (3.1.8) and (3.1.12) into (3.1.13), we obtain

(3.1.14)

$$\Delta Q_{ch}(y) = -\frac{V_F(y)}{V_b} Q_{ch0}$$

where $V_b = (V_{gsteff} + nv_t) / A_{bulk}$. In the model implementation, n of V_b is replaced by a typical constant value of 2. The expression for V_b now becomes

(3.1.15)

$$V_b = \frac{V_{gsteff} + 2v_t}{A_{bulk}}$$

A unified expression for $Q_{ch}(y)$ from subthreshold to strong inversion regions is

(3.1.16)

$$Q_{ch}(y) = C_{oxeff} \cdot V_{gsteff} \cdot \left(1 - \frac{V_F(y)}{V_b}\right)$$

3.2 Subthreshold Swing *n*

The drain current equation in the subthreshold region can be expressed as

(3.2.1)

$$I_{ds} = I_0 \left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off}'}{nv_t}\right)$$

where

(3.2.2)

$$I_0 = m\frac{W}{L}\sqrt{\frac{qe_{si}NDEP}{2\Phi_s}}v_t^2$$

v_t is the thermal voltage and equal to k_BT/q. $V_{off}' = VOFF + VOFFL / L_{eff}$ is the offset voltage, which determines the channel current at $V_{gs} = 0$. In (3.2.1), n is the

subthreshold swing parameter. Experimental data shows that the subthreshold swing is a function of channel length and the interface state density. These two mechanisms are modeled by the following

$$n = 1 + NFACTOR \cdot \frac{C_{dep}}{C_{oxe}} + \frac{Cdsc\_Term + CIT}{C_{oxe}} \tag{3.2.3}$$

where *Cdsc-Term*, written as

$$Cdsc\_Term = \left(CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bseff}\right) \cdot \frac{0.5}{\cosh\left(DVT1\frac{L_{eff}}{l_t}\right) - 1}$$

represents the coupling capacitance between drain/source to channel. Parameters *CDSC*, *CDSCD* and *CDSCB* are extracted. Parameter *CIT* is the capacitance due to interface states. From (3.2.3), it can be seen that subthreshold swing shares the same exponential dependence on channel length as the *DIBL* effect. Parameter *NFACTOR* is close to 1 and introduced to compensate for errors in the depletion width capacitance calculation.

Chapter 4: Gate Direct Tunneling Current Model

As the gate oxide thickness is scaled down to 3nm and below, gate leakage current due to carrier direct tunneling becomes important. This tunneling happens between the gate and silicon beneath the gate oxide. To reduce the tunneling current, high-k dielectrics are being studied to replace gate oxide. In order to maintain a good interface with substrate, multi-layer dielectric stacks are being proposed. The BSIM4 gate tunneling model has been shown to work for multi-layer gate stacks as well. The tunneling carriers can be either electrons or holes, or both, either from the conduction band or valence band, depending on (the type of the gate and) the bias regime.

In BSIM4, the gate tunneling current components include the tunneling current between gate and substrate (*Igb*), and the current between gate and channel (*Igc*), which is partitioned between the source and drain terminals by *Igc = Igcs + Igcd*.

The third component happens between gate and source/drain diffusion regions (*Igs* and *Igd*). Figure 4-1 shows the schematic gate tunneling current flows.

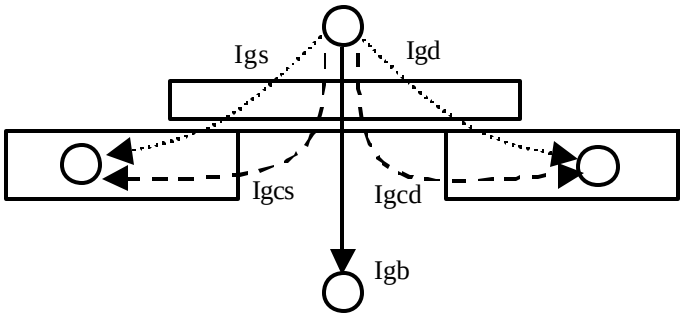


Figure 4-1. Shematic gate current components flowing between NMOST terminals in version.

4.1 Model selectors

Two global selectors are provided to turn on or off the tunneling components. ***igcMod*** = 1, 2 turns on *Igc*, *Igs*, and *Igd*; ***igbMod*** = 1 turns on *Igb*. When the selectors are set to zero, no gate tunneling currents are modeled. When tempMod = 2, following Vt (= kT/q) will be replaced by Vtnom(=kTnom/q)

4.2 Voltage Across Oxide V_{ox}

The oxide voltage V_{ox} is written as $V_{ox} = V_{oxacc} + V_{oxdepinv}$ with

(4.2.1a)

$$V_{oxacc} = V_{fbzb} - V_{FBeff}$$

(4.2.1b)

$$V_{oxdepinv} = K_{1ox}\sqrt{\Phi_s} + V_{gsteff}$$

(4.2.1) is valid and continuous from accumulation through depletion to inversion. V_{fbzb} is the flat-band voltage calculated from zero-bias V_{th} by

(4.2.2)

$$V_{fbzb} = V_{th}\Big|_{zero V_{bs} and V_{ds}} - \Phi_s - K1\sqrt{\Phi_s}$$

and

(4.2.3)

$$V_{FBeff} = V_{fbzb} - 0.5\left[\left(V_{fbzb} - V_{gb} - 0.02\right) + \sqrt{\left(V_{fbzb} - V_{gb} - 0.02\right)^2 + 0.08V_{fbzb}}\right]$$

4.3 Equations for Tunneling Currents

Note: when tempMod = 2, nominal temperature(TNOM) is used to replace the operating temperature in following gate tunneling current equations. When tempMod=0, or 1, operating temperature is still used.

4.3.1 Gate-to-Substrate Current (*Igb = Igbacc + Igbinv*)

Igbacc, determined by ECB (Electron tunneling from Conduction Band), is significant in accumulation and given by

(4.3.1)

$$Igbacc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE\left(AIGBACC - BIGBACC \cdot V_{oxacc}\right) \cdot \left(1 + CIGBACC \cdot V_{oxacc}\right)\right]$$

where the physical constants A = 4.97232e-7 A/V^2, B = 7.45669e11 (g/F-s^2)$^{0.5}$, and

$$T_{oxRatio} = \left(\frac{TOXREF}{TOXE}\right)^{NTOX} \cdot \frac{1}{TOXE^2}$$

$$V_{aux} = NIGBACC \cdot v_t \cdot \log\left(1 + \exp\left(-\frac{V_{gb} - V_{fbzb}}{NIGBACC \cdot v_t}\right)\right)$$

Igbinv, determined by EVB (Electron tunneling from Valence Band), is significant in inversion and given by

(4.3.2)

$$Igbinv = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE\left(AIGBINV - BIGBINV \cdot V_{oxdepinv}\right) \cdot \left(1 + CIGBINV \cdot V_{oxdepinv}\right)\right]$$

where A = 3.75956e-7 A/V^2, B = 9.82222e11 (g/F-s^2)$^{0.5}$, and

$$V_{aux} = NIGBINV \cdot v_t \cdot \log\left(1+\exp\left(\frac{V_{oxdepinv} - EIGBINV}{NIGBINV \cdot v_t}\right)\right)$$

4.3.2 Gate-to-Channel Current (*Igc0*) and Gate-to-S/D (*Igs* and *Igd*)

Igc0, determined by ECB for NMOS and HVB (Hole tunneling from Valence Band) for PMOS at Vds=0, is formulated as

(4.3.3)

$$\begin{aligned} Igc0 &= W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux} \\ &\cdot exp\left[-B \cdot TOXE\left(AIGC - BIGC \cdot V_{oxdepinv}\right) \cdot \left(1 + CIGC \cdot V_{oxdepinv}\right)\right] \end{aligned}$$

where A = 4.97232 A/V^2 for NMOS and 3.42537 A/V^2 for PMOS, B = 7.45669e11 (g/F-s^2)$^{0.5}$ for NMOS and 1.16645e12 (g/F-s^2)$^{0.5}$ for PMOS, and for igcMod = 1:

$$V_{aux} = NIGC \cdot v_t \cdot \log\left(1+\exp\left(\frac{V_{gse} - VTH0}{NIGC \cdot v_t}\right)\right)$$

for igcMod = 2:

$$V_{aux} = NIGC \cdot v_t \cdot \log\left(1+\exp\left(\frac{V_{gse} - VTH}{NIGC \cdot v_t}\right)\right)$$

Igs* and *Igd -- *Igs* represents the gate tunneling current between the gate and the source diffusion region, while *Igd* represents the gate tunneling current between the gate and the drain diffusion region. *Igs* and *Igd* are determined by ECB for NMOS and HVB for PMOS, respectively.

(4.3.4)

$$Igs = W_{eff}\,DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot \left(AIGSD - BIGSD \cdot V_{gs}'\right) \cdot \left(1 + CIGSD \cdot V_{gs}'\right)\right]$$

and

(4.3.5)

$$Igd = W_{eff}\,DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot \left(AIGSD - BIGSD \cdot V_{gd}'\right) \cdot \left(1 + CIGSD \cdot V_{gd}'\right)\right]$$

where A = 4.97232 A/V^2 for NMOS and 3.42537 A/V^2 for PMOS, B = 7.45669e11 (g/F-s^2)$^{0.5}$ for NMOS and 1.16645e12 (g/F-s^2)$^{0.5}$ for PMOS, and

$$T_{oxRatioEdge} = \left(\frac{TOXREF}{TOXE \cdot POXEDGE}\right)^{NTOX} \cdot \frac{1}{\left(TOXE \cdot POXEDGE\right)^2}$$

$$V_{gs}' = \sqrt{\left(V_{gs} - V_{fbsd}\right)^2 + 1.0e-4}$$

$$V_{gd}' = \sqrt{\left(V_{gd} - V_{fbsd}\right)^2 + 1.0e-4}$$

V_{fbsd} is the flat-band voltage between gate and S/D diffusions calculated as

If *NGATE* > 0.0

$$\boldsymbol{V_{fbsd} = \frac{k_B T}{q}\, log\left(\frac{NGATE}{NSD}\right) + VFBSDOFF}$$

Else V_{fbsd} = 0.0.

4.3.3 Partition of *Igc*

To consider the drain bias effect, *Igc* is split into two components, *Igcs* and *Igcd*, that is *Igc = Igcs + Igcd*, and

$$Igcs = Igc0 \cdot \frac{PIGCD \cdot V_{dseff} + \exp\left(-PIGCD \cdot V_{dseff}\right) - 1 + 1.0\text{e}-4}{PIGCD^2 \cdot V_{dseff}{}^2 + 2.0\text{e}-4} \tag{4.3.6}$$

and

$$Igcd = Igc0 \cdot \frac{1 - \left(PIGCD \cdot V_{dseff} + 1\right) \cdot \exp\left(-PIGCD \cdot V_{dseff}\right) + 1.0\text{e}-4}{PIGCD^2 \cdot V_{dseff}{}^2 + 2.0\text{e}-4} \tag{4.3.7}$$

Where Igc0 is Igc at V_{ds}=0.

If the model parameter *PIGCD* is not specified, it is given by

$$PIGCD = \frac{B \cdot TOXE}{V_{gsteff}{}^2}\left(1 - \frac{V_{dseff}}{2 \cdot V_{gsteff}}\right) \tag{4.3.8}$$

Chapter 5: Drain Current Model

5.1 Bulk Charge Effect

The depletion width will not be uniform along channel when a non-zero V_{ds} is applied. This will cause V_{th} to vary along the channel. This effect is called bulk charge effect.

BSIM4 uses A_{bulk} to model the bulk charge effect. Several model parameters are introduced to account for the channel length and width dependences and bias effects. A_{bulk} is formulated by

(5.1.1)

$$A_{bulk} = \left\{1 + F\_doping \cdot \left[\frac{A0 \cdot L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}} \cdot \left(1 - AGS \cdot V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}\right)^2\right) + \frac{B0}{W_{eff}' + B1}\right]\right\} \cdot \frac{1}{1 + KETA \cdot V_{bseff}}$$

where the second term on the RHS is used to model the effect of non-uniform doping profiles

(5.1.2)

$$F\_doping = \frac{\sqrt{1 + LPEB/L_{eff}}K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} + K_{2ox} - K3B\frac{TOXE}{W_{eff}' + W0}\Phi_s$$

Note that A_{bulk} is close to unity if the channel length is small and increases as the channel length increases.

5.2 Unified Mobility Model

A good mobility model is critical to the accuracy of a MOSFET model. The scattering mechanisms responsible for surface mobility basically include phonons, coulombic scattering, and surface roughness. For good quality interfaces, phonon scattering is generally the dominant scattering mechanism at room temperature. In general, mobility depends on many process parameters and bias conditions. For example, mobility depends on the gate oxide thickness, substrate doping concentration, threshold voltage, gate and substrate voltages, etc. [5] proposed an empirical unified formulation based on the concept of an effective field E_{eff} which lumps many process parameters and bias conditions together. E_{eff} is defined by

$$E_{eff} = \frac{Q_B + (Q_n/2)}{e_{si}} \tag{5.2.1}$$

The physical meaning of E_{eff} can be interpreted as the average electric field experienced by the carriers in the inversion layer. The unified formulation of mobility is then given by

$$m_{eff} = \frac{m_0}{1 + (E_{eff} \big/ E_0)^n} \tag{5.2.2}$$

For an NMOS transistor with n-type poly-silicon gate, (5.2.1) can be rewritten in a more useful form that explicitly relates E_{eff} to the device parameters

(5.2.3)

$$E_{eff} \approx \frac{V_{gs} + V_{th}}{6TOXE}$$

BSIM4 provides three different models of the effective mobility. The ***mobMod*** = 0 and 1 models are from BSIM3v3.2.2; the new ***mobMod*** = 2, a universal mobility model, is more accurate and suitable for predictive modeling.

- ***mobMod* = 0**

(5.2.4)

$$\mu_{eff} = \frac{\boldsymbol{U0} \cdot \boldsymbol{f(L_{eff})}}{1 + \left(\boldsymbol{UA} + \boldsymbol{UCV_{bseff}}\right)\left(\frac{\boldsymbol{V_{gsteff}} + 2\boldsymbol{V_{th}}}{\boldsymbol{TOXE}}\right) + \boldsymbol{UB}\left(\frac{\boldsymbol{V_{gsteff}} + 2\boldsymbol{V_{th}}}{\boldsymbol{TOXE}}\right)^2 + \boldsymbol{UD}\left(\frac{\boldsymbol{V_{th}} \cdot \boldsymbol{TOXE}}{\boldsymbol{V_{gsteff}} + 2\boldsymbol{V_{th}}}\right)^2}$$

- ***mobMod* = 1**

(5.2.5)

$$\mu_{eff} = \frac{\boldsymbol{U0} \cdot \boldsymbol{f(L_{eff})}}{1 + \left[\boldsymbol{UA}\left(\frac{\boldsymbol{V_{gsteff}} + 2\boldsymbol{V_{th}}}{\boldsymbol{TOXE}}\right) + \boldsymbol{UB}\left(\frac{\boldsymbol{V_{gsteff}} + 2\boldsymbol{V_{th}}}{\boldsymbol{TOXE}}\right)^2\right]\left(1 + \boldsymbol{UC} \cdot \boldsymbol{V_{bseff}}\right) + \boldsymbol{UD}\left(\frac{\boldsymbol{V_{th}} \cdot \boldsymbol{TOXE}}{\boldsymbol{V_{gsteff}} + 2\boldsymbol{V_{th}}}\right)^2}$$

- ***mobMod* = 2**

(5.2.6)

$$\mu_{eff} = \frac{U0}{1 + \left(UA + UC \cdot V_{bseff}\right)\left[\frac{V_{gsteff} + C_0 \cdot \left(VTHO - VFB - \Phi_s\right)}{TOXE}\right]^{EU}}$$

where the constant C_0 = 2 for NMOS and 2.5 for PMOS.

$$f(L_{eff}) = 1 - UP \cdot \exp\left(-\frac{L_{eff}}{LP}\right) \tag{5.2.7}$$

5.3 Asymmetric and Bias-Dependent Source/ Drain Resistance Model

BSIM4 models source/drain resistances in two components: bias-independent diffusion resistance (sheet resistance) and bias-dependent LDD resistance. Accurate modeling of the bias-dependent LDD resistances is important for deep-submicron CMOS technologies. In BSIM3 models, the LDD source/drain resistance $R_{ds}(V)$ is modeled internally through the I-V equation and symmetry is assumed for the source and drain sides. BSIM4 keeps this option for the sake of simulation efficiency. In addition, BSIM4 allows the source LDD resistance $R_s(V)$ and the drain LDD resistance $R_d(V)$ to be external and asymmetric (i.e. $R_s(V)$ and $R_d(V)$ can be connected between the external and internal source and drain nodes, respectively; furthermore, $R_s(V)$ does not have to be equal to $R_d(V)$). This feature makes accurate RF CMOS simulation possible. The internal $R_{ds}(V)$ option can be invoked by setting the model selector ***rdsMod*** = 0 (**interna**l) and the external one for $R_s(V)$ and $R_d(V)$ by setting ***rdsMod*** = 1 (**external**).

- ***rdsMod*** = 0 (Internal $R_{ds}(V)$)

$$R_{ds}(V) = \left\{ RDSWMIN + RDSW \cdot \left[PRWB \cdot \left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s} \right) + \frac{1}{1 + PRWG \cdot V_{gsteff}} \right] \right\} \Big/ \left(1e6 \cdot W_{effcj} \right)^{WR} \tag{5.3.1}$$

- ***rdsMod*** = 1 (External $R_d(V)$ and $R_s(V)$)

(5.3.2)

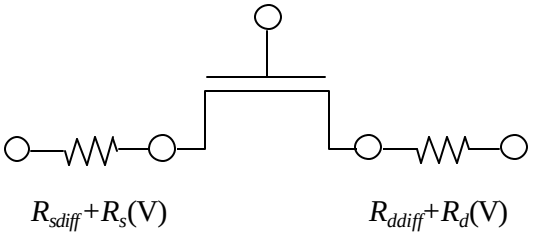
$$R_d(V) = \left\{ \begin{array}{l} RDWMIN + RDW \cdot \\ \left[-PRWB \cdot V_{bd} + \dfrac{1}{1 + PRWG \cdot (V_{gd} - V_{fbsd})} \right] \end{array} \right\} \Big/ \left[(1e6 \cdot W_{effcj})^{WR} \cdot NF \right]$$

(5.3.3)

$$R_s(V) = \left\{ \begin{array}{l} RSWMIN + RSW \cdot \\ \left[-PRWB \cdot V_{bs} + \dfrac{1}{1 + PRWG \cdot (V_{gs} - V_{fbsd})} \right] \end{array} \right\} \Big/ \left[(1e6 \cdot W_{effcj})^{WR} \cdot NF \right]$$

V_{fbsd} is the calculated flat-band voltage between gate and source/drain as given in Section 4.3.2.

The following figure shows the schematic of source/drain resistance connection for ***rdsMod*** = 1.



The diffusion source/drain resistance R_{sdiff} and R_{ddiff} models are given in the chapter of layout-dependence models.

5.4 Drain Current for Triode Region

5.4.1 R_{ds}(V)=0 or *rdsMod*=1 (" intrinsic case")

Both drift and diffusion currents can be modeled by

$$I_{ds}(y) = WQ_{ch}(y)\mu_{ne}(y)\frac{dV_F(y)}{dy} \tag{5.4.1}$$

where $u_{ne}(y)$ can be written as

$$\mu_{ne(y)} = \frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}} \tag{5.4.2}$$

Substituting (5.4.2) in (5.4.1), we get

$$I_{ds}(y) = WQ_{ch0}\left(1-\frac{V_F(y)}{V_b}\right)\frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}}\frac{dV_F(y)}{dy} \tag{5.4.3}$$

(5.4.3) is integrated from source to drain to get the expression for linear drain current. This expression is valid from the subthreshold regime to the strong inversion regime

(5.4.4)

$$I_{ds0} = \frac{Wm_{eff} Q_{ch0} V_{ds} \left(1 - \frac{V_{ds}}{2V_b}\right)}{L\left(1 + \frac{V_{ds}}{E_{sat} L}\right)}$$

5.4.2 R_{ds}(V) > 0 and *rdsMod*=0 ("Extrinsic case")

The drain current in this case is expressed by

(5.4.5)

$$I_{ds} = \frac{I_{dso}}{1 + \frac{R_{ds} I_{dso}}{V_{ds}}}$$

5.5 Velocity Saturation

Velocity saturation is modeled by [5]

(5.5.1)

$$\begin{aligned} v &= \frac{m_{eff} E}{1 + E/E_{sat}} && E < E_{sat} \\ &= VSAT && E \geq E_{sat} \end{aligned}$$

where E_{sat} corresponds to the critical electrical field at which the carrier velocity becomes saturated. In order to have a continuous velocity model at $E = E_{sat}$, E_{sat} must satisfy

(5.5.2)

$$E_{sat} = \frac{2VSAT}{m_{eff}}$$

5.6 Saturation Voltage V_{dsat}

5.6.1 Intrinsic case

In this case, the LDD source/drain resistances are either zero or non zero but not modeled inside the intrinsic channel region. It is easy to obtain V_{dsat} as [7]

(5.6.1)

$$V_{dsat} = \frac{E_{sat}L(V_{gsteff} + 2v_t)}{A_{bulk}E_{sat}L + V_{gsteff} + 2v_t}$$

5.6.2 Extrinsic Case

In this case, non-zero LDD source/drain resistance R_{ds}(V) is modeled internally through the I-V equation and symetry is assumed for the source and drain sides. V_{dsat} is obtained as [7]

(5.6.2a)

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

where

(5.6.2b)

$$a = A_{bulk}{}^{2} W_{eff} VSATC_{oxe} R_{ds} + A_{bulk}\left(\frac{1}{l} - 1\right)$$

(5.6.2c)

$$b = -\begin{bmatrix} \left(V_{gsteff} + 2v_t\right)\left(\frac{2}{l} - 1\right) + A_{bulk} E_{sat} L_{eff} \\ + 3A_{bulk}\left(V_{gsteff} + 2v_t\right) W_{eff} VSATC_{oxe} R_{ds} \end{bmatrix}$$

(5.6.2d)

$$c = \left(V_{gsteff} + 2v_t\right) E_{sat} L_{eff} + 2\left(V_{gsteff} + 2v_t\right)^2 W_{eff} VSATC_{oxe} R_{ds}$$

(5.6.2e)

$$l = A1 V_{gsteff} + A2$$

λ is introduced to model the non-saturation effects which are found for PMOSFETs.

5.6.3 V_{dseff} Formulation

An effective V_{ds}, V_{dseff}, is used to ensure a smooth transition near V_{dsat} from trode to saturation regions. V_{dseff} is formulated as

(5.6.3)

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left[\left(V_{dsat} - V_{ds} - d\right) + \sqrt{\left(V_{dsat} - V_{ds} - d\right)^2 + 4d \cdot V_{dsat}}\right]$$

where δ (*DELTA*) is a model parameter.

5.7 Saturation-Region Output Conductance Model

A typical I-V curve and its output resistance are shown in Figure 5-1. Considering only the channel current, the I-V curve can be divided into two parts: the linear region in which the current increases quickly with the drain voltage and the saturation region in which the drain current has a weaker dependence on the drain voltage. The first order derivative reveals more detailed information about the physical mechanisms which are involved in the device operation. The output resistance curve can be divided into four regions with distinct R_{out}~V_{ds} dependences.

The first region is the triode (or linear) region in which carrier velocity is not saturated. The output resistance is very small because the drain current has a strong dependence on the drain voltage. The other three regions belong to the saturation region. As will be discussed later, there are several physical mechanisms which affect the output resistance in the saturation region: channel length modulation (CLM), drain-induced barrier lowering (DIBL), and the substrate current induced body effect (SCBE). These mechanisms all affect the output resistance in the saturation range, but each of them dominates in a specific region. It will be shown

next that CLM dominates in the second region, DIBL in the third region, and SCBE in the fourth region.

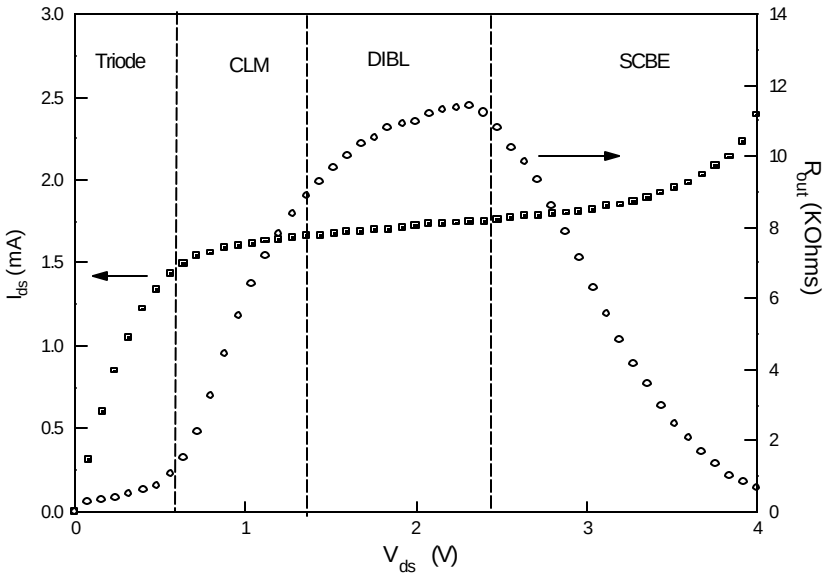


Figure 5-1. General behavior of MOSFET output resistance.

The channel current is a function of the gate and drain voltage. But the current depends on the drain voltage weakly in the saturation region. In the following, the Early voltage is introduced for the analysis of the output resistance in the saturation region:

(5.7.1)

$$I_{ds}(V_{gs},V_{ds}) = I_{dsat}(V_{gs},V_{dsat}) + \int_{V_{dsat}}^{V_{ds}} \frac{\partial I_{ds}(V_{gs},V_{ds})}{\partial V_d} \cdot dV_d$$

$$= I_{dsat}(V_{gs},V_{dsat}) \cdot \left[1 + \int_{V_{dsat}}^{V_{ds}} \frac{1}{V_A} \cdot dV_d \right]$$

where the Early voltage V_A is defined as

(5.7.2)

$$V_A = I_{dsat} \cdot \left[\frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_d} \right]^{-1}$$

We assume in the following analysis that the contributions to the Early voltage from all mechanisms are independent and can be calculated separately.

5.7.1 Channel Length Modulation (CLM)

If channel length modulation is the only physical mechanism to be taken into account, the Early voltage can be calculated by

(5.7.3)

$$V_{ACLM} = I_{dsat} \cdot \left[\frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial L} \cdot \frac{\partial L}{\partial V_d} \right]^{-1}$$

Based on quasi two-dimensional analysis and through integration, we propose V_{ACLM} to be

(5.7.4)

$$V_{ACLM} = C_{clm} \cdot (V_{ds} - V_{dsat})$$

where

(5.7.5)

$$C_{clm} = \frac{1}{PCLM} \cdot F \cdot \left(1 + PVAG \frac{V_{gsteff}}{E_{sat} L_{eff}} \right) \left(1 + \frac{R_{ds} \cdot I_{dso}}{V_{dseff}} \right) \left(L_{eff} + \frac{V_{dsat}}{E_{sat}} \right) \cdot \frac{1}{litl}$$

and the *F* factor to account for the impact of pocket implant technology is

(5.7.6)

$$F = \frac{1}{1 + FPROUT \cdot \frac{\sqrt{L_{eff}}}{V_{gsteff} + 2v_t}}$$

and *litl* in (5.7.5) is given by

(5.7.7)

$$litl = \sqrt{\frac{e_{si} TOXE \cdot XJ}{EPSROX}}$$

PCLM is introduced into V_{ACLM} to compensate for the error caused by *XJ* since the junction depth *XJ* can not be determined very accurately.

5.7.2 Drain-Induced Barrier Lowering (DIBL)

The Early voltage V_{ADIBLC} due to DIBL is defined as

(5.7.8)

$$V_{ADIBL} = I_{dsat} \cdot \left[\frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{th}} \cdot \frac{\partial V_{th}}{\partial V_d} \right]^{-1}$$

V_{th} has a linear dependence on V_{ds}. As channel length decreases, V_{ADIBLC} decreases very quickly

(5.7.9)

$$V_{ADIBL} = \frac{V_{gsteff} + 2v_t}{q_{rout}(1 + PDIBLCB \cdot V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t} \right) \cdot \left(1 + PVAG \frac{V_{gsteff}}{E_{sat} L_{eff}} \right)$$

where q_{rout} has a similar dependence on the channel length as the DIBL effect in V_{th}, but a separate set of parameters are used:

$$q_{rout} = \frac{PDIBLC1}{2\cosh\left(\frac{DROUT \cdot L_{eff}}{lt0}\right) - 2} + PDIBLC2 \tag{5.7.10}$$

Parameters *PDIBLC*1, *PDIBLC*2, *PDIBLCB* and *DROUT* are introduced to correct the DIBL effect in the strong inversion region. The reason why *DVT*0 is not equal to *PDIBLC*1 and *DVT*1 is not equal to *DROUT* is because the gate voltage modulates the DIBL effect. When the threshold voltage is determined, the gate voltage is equal to the threshold voltage. But in the saturation region where the output resistance is modeled, the gate voltage is much larger than the threshold voltage. Drain induced barrier lowering may not be the same at different gate bias. *PDIBLC*2 is usually very small. If *PDIBLC*2 is put into the threshold voltage model, it will not cause any significant change. However it is an important parameter in V_{ADIBLC} for long channel devices, because *PDIBLC*2 will be dominant if the channel is long.

5.7.3 Substrate Current Induced Body Effect (SCBE)

When the electrical field near the drain is very large (> 0.1MV/cm), some electrons coming from the source (in the case of NMOSFETs) will be energetic (hot) enough to cause impact ionization. This will generate electron-hole pairs when these energetic electrons collide with silicon atoms. The substrate current I_{sub} thus created during impact ionization will

increase exponentially with the drain voltage. A well known I_{sub} model [8] is

$$I_{sub} = \frac{A_i}{B_i} I_{ds}(V_{ds} - V_{dsat}) \exp\left(-\frac{B_i \cdot litl}{V_{ds} - V_{dsat}}\right) \tag{5.7.11}$$

Parameters A_i and B_i are determined from measurement. I_{sub} affects the drain current in two ways. The total drain current will change because it is the sum of the channel current as well as the substrate current. The total drain current can now be expressed as follows

$$I_{ds} = I_{ds-w/o-Isub} + I_{sub} = I_{ds-w/o-Isub} \cdot \left[1 + \frac{V_{ds} - V_{dsat}}{\frac{B_i}{A_i} \exp\left(\frac{B_i \cdot litl}{V_{ds} - V_{dsat}}\right)}\right] \tag{5.7.12}$$

The Early voltage due to the substrate current V_{ASCBE} can therefore be calculated by

$$V_{ASCBE} = \frac{B_i}{A_i} \exp\left(\frac{B_i \cdot litl}{V_{ds} - V_{dsat}}\right) \tag{5.7.13}$$

We can see that V_{ASCBE} is a strong function of V_{ds}. In addition, we also observe that V_{ASCBE} is small only when V_{ds} is large. This is why SCBE is important for devices with high drain voltage bias. The channel length and gate oxide dependence of V_{ASCBE} comes from V_{dsat} and *litl*. We replace B_i with *PSCBE*2 and A_i/B_i with $PSCBE1/L_{eff}$ to get the following expression for V_{ASCBE}

(5.7.14)

$$\frac{1}{V_{ASCBE}} = \frac{PSCBE2}{L_{eff}} \exp\left(-\frac{PSCBE1 \cdot litl}{V_{ds} - V_{dsat}} \right)$$

5.7.4 Drain-Induced Threshold Shift (DITS) by Pocket Implant

It has been shown that a long-channel device with pocket implant has a smaller R_{out} than that of uniformly-doped device [3]. The R_{out} degradation factor F is given in (5.7.6). In addition, the pocket implant introduces a potential barrier at the drain end of the channel. This barrier can be lowered by the drain bias even in long-channel devices. The Early voltage due to DITS is modeled by

(5.7.15)

$$V_{ADITS} = \frac{1}{PDITS} \cdot F \cdot \left[1 + \left(1 + PDITSL \cdot L_{eff} \right) \exp\left(PDITSD \cdot V_{ds} \right) \right]$$

5.8 Single-Equation Channel Current Model

The final channel current equation for both linear and saturation regions now becomes

(5.8.1)

$$I_{ds} = \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left[1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{Asat}} \right) \right] \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}} \right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}} \right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}} \right)$$

where NF is the number of device fingers, and

(5.8.2)

V_A is written as

(5.8.3)

$$V_A = V_{Asat} + V_{ACLM}$$

where V_{Asat} is

(5.8.4)

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{ds}vsatC_{oxe}W_{eff}V_{gsteff} \cdot \left[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2v_t)}\right]}{R_{ds}vsatC_{oxe}W_{eff}A_{bulk} - 1 + \frac{2}{l}}$$

V_{Asat} is the Early voltage at $V_{ds} = V_{dsat}$. V_{Asat} is needed to have continuous drain current and output resistance expressions at the transition point between linear and saturation regions.

5.9 New Current Saturation Mechanisms: Velocity Overshoot and Source End Velocity Limit Model

5.9.1 Velocity Overshoot

In the deep-submicron region, the velocity overshoot has been observed to be a significant effect even though the supply voltage is scaled down

according to the channel length. An approximate non-local velocity field expression has proven to provide a good description of this effect

(5.9.1)

$$v = v_d\left(1+\frac{l}{E}\frac{\partial E}{\partial x}\right) = \frac{\mu E}{1+E/E_c}\left(1+\frac{l}{E}\frac{\partial E}{\partial x}\right)$$

This relationship is then substituted into (5.8.1) and the new current expression including the velocity overshoot effect is obtained:

(5.9.2)

$$I_{DS,HD} = \frac{I_{DS}\cdot\left(1+\dfrac{V_{dseff}}{L_{eff}E_{sat}}\right)}{1+\dfrac{V_{dseff}}{L_{eff}E_{sat}^{OV}}}$$

where

(5.9.3)

$$E_{sat}^{OV} = E_{sat}\left[1+\frac{LAMBDA}{L_{eff}\cdot\mu_{eff}}\cdot\frac{\left(1+\dfrac{V_{ds}-V_{dseff}}{Esat\cdot litl}\right)^2-1}{\left(1+\dfrac{V_{ds}-V_{dseff}}{Esat\cdot litl}\right)^2+1}\right]$$

LAMBDA is the velocity overshoot coefficient.

5.9.2 Source End Velocity Limit Model

When MOSFETs come to nanoscale, because of the high electric field and strong velocity overshoot, carrier transport through the drain end of the channel is rapid. As a result, the dc current is controlled by how rapidly carriers are transported across a short low-field region near the beginning of the channel. This is known as injection velocity limits at the source end of the channel. A compact model is firstly developed to account for this current saturation mechanism .

Hydro-dynamic transportation gives the source end velocity as :

(5.9.4)

$$v_{sHD} = I_{DS,HD} \Big/ Wq_s$$

where qs is the source end inversion charge density. Source end velocity limit gives the highest possible velocity which can be given through ballistic transport as:

(5.9.5)

$$v_{sBT} = \frac{1-r}{1+r} VTL$$

where *VTL*: thermal velocity, r is the back scattering coefficient which is given:

(5.9.6)

$$r = \frac{L_{eff}}{XN \cdot L_{eff} + LC} \quad XN \geq 3.0$$

The real source end velocity should be the lower of the two, so a final Unified current expression with velocity saturation, velocity overshoot and source velocity limit can be expressed as :

(5.9.7)

$$I_{DS} = \frac{I_{DS,HD}}{\left[1+\left(v_{sHD} / v_{sBT}\right)^{2MM}\right]^{1/2MM}}$$

where MM=2.0.

Chapter 6: Body Current Models

In addition to the junction diode current and gate-to-body tunneling current, the substrate terminal current consists of the substrate current due to impact ionization (I_{ii}), and gate-induced drain leakage current (I_{GIDL}).

6.1 I_{ii} Model

The impact ionization current model in BSIM4 is the same as that in BSIM3v3.2, and is modeled by

(6.1.1)

$$I_{ii} = \frac{ALPHA0 + ALPHA1 \cdot L_{eff}}{L_{eff}} \left(V_{ds} - V_{dseff}\right) \exp\left(\frac{BETA0}{V_{ds} - V_{dseff}}\right) \cdot I_{dsNoSCBE}$$

where parameters *ALPHA*0 and *BETA*0 are impact ionization coefficients; parameter *ALPHA*1 is introduced to improves the I_{ii} scalability, and

(6.1.2)

$$I_{dsNoSCBE} = \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left[1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{Asat}}\right)\right] \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right)$$

6.2 I_{GIDL} and I_{GISL} Model

The GIDL/GISL current and its body bias effect are modeled by [9]-[10]

(6.2.1)

$$I_{GIDL} = AGIDL \cdot W_{effCJ} \cdot Nf \cdot \frac{V_{ds} - V_{gse} - EGIDL}{3 \cdot T_{oxe}} \cdot \exp\left(- \frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL} \right) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3}$$

(6.2.2)

$$I_{GISL} = AGIDL \cdot W_{effCJ} \cdot Nf \cdot \frac{-V_{ds} - V_{gde} - EGIDL}{3 \cdot T_{oxe}} \cdot \exp\left(- \frac{3 \cdot T_{oxe} \cdot BGIDL}{-V_{ds} - V_{gde} - EGIDL} \right) \cdot \frac{V_{sb}^3}{CGIDL + V_{sb}^3}$$

where *AGIDL*, *BGIDL*, *CGIDL*, and *EGIDL* are model parameters and explained in Appendix A. *CGIDL* accounts for the body-bias dependence of I_{GIDL} *and* I_{GISL}. W_{effCJ} and *Nf* are the effective width of the source/drain diffusions and the number of fingers. Further explanation of W_{effCJ} and *Nf* can be found in the chapter of the layout-dependence model.

Chapter 7: Capacitance Model

Accurate modeling of MOSFET capacitance plays equally important role as that of the DC model. This chapter describes the methodology and device physics considered in both intrinsic and extrinsic capacitance modeling in BSIM4.0.0. Complete model parameters can be found in Appendix A.

7.1 General Description

BSIM4.0.0 provides three options for selecting intrinsic and overlap/fringing capacitance models. These capacitance models come from BSIM3v3.2, and the BSIM3v3.2 capacitance model parameters are used without change in BSIM4. except that separate *CKAPPA* parameters are introduced for the source-side and drain-side overlap capacitances. The BSIM3v3.2 ***capMod*** = 1 is no longer supported in BSIM4. The following table maps the BSIM4 capacitance models to those of BSIM3v3.2.

BSIM4 capacitance models	Matched *capMod* in BSIM3v3.2.2
capMod = 0 (simple and piece-wise model)	Intrinsic ***capMod*** = 0 + overlap/fringing ***capMod*** = 0
capMod = 1 (single-equation model)	Intrinsic ***capMod*** = 2 + overlap/fringing ***capMod*** = 2
capMod = 2 (default model; singel-equation and charge-thickness model	Intrinsic ***capMod*** = 3 + overlap/fringing ***capMod*** = 2

Table 7-1. BSIM4 capacitance model options.

BSIM4 capacitance models have the following features:

- Separate effective channel length and width are used for capacitance models.
- ***capMod*** = 0 uses piece-wise equations. ***capMod*** = 1 and 2 are smooth and single equation models; therefore both charge and capacitance are continous and smooth over all regions.
- Threshold voltage is consistent with DC part except for ***capMod*** = 0, where a long-channel V_{th} is used. Therefore, those effects such as body bias, short/narrow channel and DIBL effects are explicitly considered in ***capMod*** = 1 and 2.
- Overlap capacitance comprises two parts: (1) a bias-independent component which models the effective overlap capacitance between the gate and the heavily doped source/drain; (2) a gate-bias dependent component between the gate and the lightly doped source/drain region.
- Bias-independent fringing capacitances are added between the gate and source as well as the gate and drain.

7.2 Methodology for Intrinsic Capacitance Modeling

7.2.1 Basic Formulation

To ensure charge conservation, terminal charges instead of terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain termianls, respectively. The gate charge is comprised of mirror charges from these components: the channel charge (Q_{inv}), accumulation charge (Q_{acc}) and substrate depletion charge (Q_{sub}).

The accumulation charge and the substrate charge are associated with the substrate while the channel charge comes from the source and drain terminals

$$\begin{cases} Q_g = -\left(Q_{sub} + Q_{inv} + Q_{acc}\right) \\ Q_b = Q_{acc} + Q_{sub} \\ Q_{inv} = Q_s + Q_d \end{cases} \tag{7.2.1}$$

The substrate charge can be divided into two components: the substrate charge at zero source-drain bias (Q_{sub0}), which is a function of gate to substrate bias, and the additional non-uniform substrate charge in the presence of a drain bias (dQ_{sub}). Q_g now becomes

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + dQ_{sub}\right) \tag{7.2.2}$$

The total charge is computed by integrating the charge along the channel. The threshold voltage along the channel is modified due to the non-uniform substrate charge by

(7.2.3)

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y$$

(7.2.4)

$$\begin{cases} Q_c = W_{active}\int_0^{L_{active}} q_c dy = -W_{active}C_{oxe}\int_0^{L_{active}}\left(V_{gt} - A_{bulk}V_y\right)dy \\ Q_g = W_{active}\int_0^{L_{active}} q_g dy = W_{active}C_{oxe}\int_0^{L_{active}}\left(V_{gt} + V_{th} - V_{FB} - \Phi_s - V_y\right)dy \\ Q_b = W_{active}\int_0^{L_{active}} q_b dy = -W_{active}C_{oxe}\int_0^{L_{active}}\left(V_{th} - V_{FB} - \Phi_s + \left(A_{bulk} - 1\right)V_y\right)dy \end{cases}$$

where $V_{gt} = V_{gse} - V_{th}$ and

$$dy = \frac{dV_y}{E_y}$$

where E_y is expressed in

(7.2.5)

$$I_{ds} = \frac{W_{active}m_{eff}C_{oxe}}{L_{active}}\left(V_{gt} - \frac{A_{bulk}}{2}V_{ds}\right)V_{ds} = W_{active}m_{eff}C_{oxe}\left(V_{gt} - A_{bulk}V_y\right)E_y$$

All capacitances are derived from the charges to ensure charge conservation. Since there are four terminals, there are altogether 16 components. For each component

(7.2.6)

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

where *i* and *j* denote the transistor terminals. C_{ij} satisfies

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

7.2.2 Short Channel Model

The long-channel charge model assume a constant mobility with no velocity saturation. Since no channel length modulation is considered, the channel charge remains constant in saturation region. Conventional long-channel charge models assume $V_{dsat,CV} = V_{gt} / A_{bulk}$ and therefore is independent of channel length. If we define a drain bias, $V_{dsat,CV}$, for capacitance modeling, at which the channel charge becomes constant, we will find that $V_{dsat,CV}$ in general is larger than V_{dsat} for I-V but smaller than the long-channel $V_{dsat} = V_{gt} / A_{bulk}$. In other words,

(7.2.7)

$$V_{dsat,IV} < V_{dsat,CV} < V_{dsat,IV}\Big|_{Lactive \to \infty} = \frac{V_{gsteff,CV}}{A_{bulk}}$$

and $V_{dsat,CV}$ is modeled by

(7.2.8)

$$V_{dsat,CV} = \frac{V_{gsteff,CV}}{A_{bulk} \cdot \left[1 + \left(\frac{CLC}{L_{active}}\right)^{CLE}\right]}$$

(7.2.9)

$$V_{gsteff,CV} = NOFF \cdot nv_t \cdot \ln\left[1+\exp\left(\frac{V_{gse}-V_{th}-VOFFCV}{NOFF \cdot nv_t}\right)\right]$$

Model parameters *CLC* and *CLE* are introduced to consider the effect of channel-length modulation. A_{bulk} for the capacitance model is modeled by

(7.2.10)

$$A_{bulk} = \left\{1+ F\_doping \cdot \left[\frac{A0 \cdot L_{eff}}{L_{eff}+2\sqrt{XJ \cdot X_{dep}}} \cdot + \frac{B0}{W_{eff}'+B1}\right] \cdot \right\} \frac{1}{1+ KETA \cdot V_{bseff}}$$

where

$$F\_doping = \frac{\sqrt{1+LPEB/L_{eff}}K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} + K_{2ox} - K3B\frac{TOXE}{W_{eff}'+W0}\Phi_s$$

7.2.3 Single Equation Formulation

Traditional MOSFET SPICE capacitance models use piece-wise equations. This can result in discontinuities and non-smoothness at transition regions. The following describes single-equation formulation for charge, capacitance and voltage modeling in ***capMod*** = 1 and 2.

(a) Transition from depletion to inversion region

The biggest discontinuity is at threshold voltage where the inversion capacitance changes abruptly from zero to C_{oxe}. Concurrently, since the substrate charge is a constant, the substrate capacitance drops abruptly to

zero at threshold voltage. The BSIM4 charge and capacitance models are formulated by substituting V_{gst} with $V_{gsteff,CV}$ as

$$Q(V_{gst}) = Q(V_{gsteff,CV}) \tag{7.2.11}$$

For capacitance modeling

$$C(V_{gst}) = C(V_{gsteff,CV})\frac{\partial V_{gsteff,CV}}{V_{g,d,s,b}} \tag{7.2.12}$$

(b) Transition from accumulation to depletion region

An effective smooth flatband voltage V_{FBeff} is used for the accumulation and depletion regions.

$$V_{FBeff} = V_{fbzb} - 0.5\left[(V_{fbzb} - V_{gb} - 0.02) + \sqrt{(V_{fbzb} - V_{gb} - 0.02)^2 + 0.08V_{fbzb}}\right] \tag{7.2.13}$$

where

$$V_{fbzb} = V_{th}\Big|_{zero V_{bs} and V_{ds}} - \Phi_s - K1\sqrt{\Phi_s} \tag{7.2.14}$$

A bias-independent V_{th} is used to calculate V_{fbzb} for ***capMod*** = 1 and 2. For ***capMod*** = 0, *VFBCV* is used instead (refer to Appendix A).

(c) Transition from linear to saturation region

An effective V_{ds}, V_{cveff}, is used to smooth out the transition between linear and saturation regions.

(7.2.15)

$$V_{cveff} = V_{dsat,CV} - 0.5\left\{V_4 + \sqrt{V_4^2 + 4d_4 V_{dsat,CV}}\right\} \quad where V_4 = V_{dsat,CV} - V_{ds} - d_4;\ d_4 = 0.02V$$

7.2.4 Charge partitioning

The inversion charges are partitioned into $Q_{inv} = Q_s + Q_d$. The ratio of Q_d to Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 (*XPART* = 1, 0.5 and 0).

50/50 charge partition

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain terminals.

40/60 charge partition

This is the most physical model of the three partitioning schemes in which the channel charges are allocated to the source and drain terminals by assuming a linear dependence on channel position *y*.

(7.2.16)

$$\begin{cases} Q_s = W_{active} \int_0^{L_{active}} q_c \left(1 - \frac{y}{L_{active}}\right) dy \\ Q_d = W_{active} \int_0^{L_{active}} q_c \frac{y}{L_{active}} dy \end{cases}$$

0/100 charge partition

In fast transient simulations, the use of a quasi-static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem.

7.3 Charge-Thickness Capacitance Model (CTM)

Current MOSFET models in SPICE generally overestimate the intrinsic capacitance and usually are not smooth at V_{fb} and V_{th}. The discrepancy is more pronounced in thinner T_{ox} devices due to the assumption of inversion and accumulation charge being located at the interface. Numerical quantum simulation results in Figure 7-1 indicate the significant charge thickness in all regions of operation.

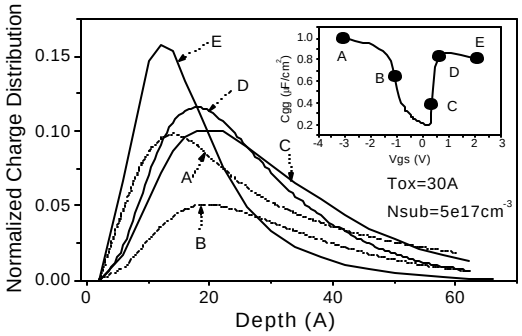


Figure 7-1. Charge distribution from numerical quantum simulations show significant charge thickness at various bias conditions shown in the inset.

CTM is a charge-based model and therefore starts with the DC charge thicknss, X_{DC}. The charge thicknss introduces a capacitance in series with C_{ox} as illustrated in Figure 7-2, resulting in an effective C_{oxeff}. Based on numerical self-consistent solution of Shrodinger, Poisson and Fermi-Dirac equations, universal and analytical X_{DC} models have been developed. C_{oxeff} can be expressed as

(7.3.1)

$$C_{oxeff} = \frac{C_{oxp} \times C_{cen}}{C_{oxp} + C_{cen}}$$

where

$$C_{cen} = \varepsilon_{si} / X_{DC}$$

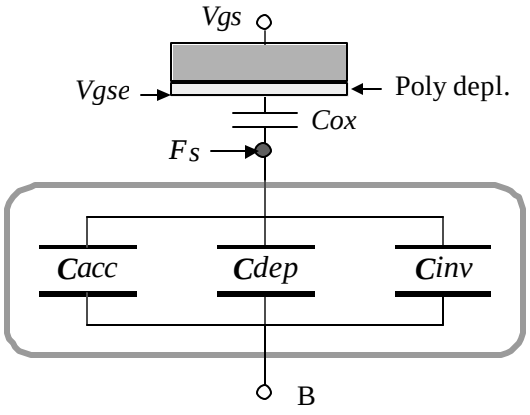


Figure 7-2. Charge-thickness capacitance concept in CTM. V_{gse} accounts for the poly depletion effect.

(i) X_{DC} for accumulation and depletion

The DC charge thickness in the accumulation and depletion regions can be expressed by

(7.3.2)

$$X_{DC} = \frac{1}{3} L_{debye} \exp\left[ACDE \cdot \left(\frac{NDEP}{2\times 10^{16}} \right)^{-0.25} \cdot \frac{V_{gse} - V_{bseff} - V_{FBeff}}{TOXP} \right]$$

where L_{debye} is Debye length, and X_{DC} is in the unit of cm and (V_{gse} - V_{bseff} - V_{FBeff}) / $TOXP$ is in units of MV/cm. For numerical statbility, (7.3.2) is replaced by (7.3.3)

(7.3.3)

$$X_{DC} = X_{\max} - \frac{1}{2}\left(X_0 + \sqrt{X_0^2 + 4 d_x X_{\max}} \right)$$

where

$$X_0 = X_{\max} - X_{DC} - d_x$$

and $X_{max} = L_{debye} / 3$; $\delta_x = 10^{-3} TOXE$.

(ii) X_{DC} of inversion charge

The inversion charge layer thichness can be formulated as

(7.3.4)

$$X_{DC} = \frac{1.9\times10^{-9}\ \text{m}}{1+\left(\frac{V_{gsteff}+4(VTH0-VFB-\Phi_s)}{2TOXP}\right)^{0.7}}$$

Through the *VFB* term, equation (7.3.4) is found to be applicable to N^+ or P^+ poly-Si gates and even other future gate materials.

(iii) Body charge thickness in inversion

In inversion region, the body charge thickness effect is modeled by including the deviation of the surface potential Φ_s (bias-dependence) from $2\Phi_B$ [2]

(7.3.5)

$$j_d = \Phi_s - 2\Phi_B = n_t \ln\left(1+\frac{V_{gsteffCV}\cdot(V_{gsteffCV}+2K_{1ox}\sqrt{2\Phi_B}}{MOIN\cdot K_{1ox}^2 n_t}\right)$$

The channel charge density is therefore derived as

(7.3.6)

$$q_{inv} = -C_{oxeff}\,\chi\left(V_{gsteff,CV} - j_d\right)_{eff}$$

where

(7.3.7)

$$\left(V_{gsteffCV} - j_d\right)_{eff} = 0.5 \cdot \left[\left(V_{gsteffCV} - j_d - 0.001\right) + \sqrt{\left(V_{gsteffCV} - j_d - 0.001\right)^2 + V_{gsteffCV} \cdot 0.004}\right]$$

7.4 Intrinsic Capacitance Model Equations

7.4.1 *capMod* = 0

Accumulation region

$$Q_g = W_{active} L_{active} C_{oxe} \left(V_{gs} - V_{bs} - VFBCV\right)$$

$$Q_{sub} = -Q_g$$

$$Q_{inv} = 0$$

Subthreshold region

$$Q_{sub0} = -W_{active} L_{active} C_{oxe} \cdot \frac{K_{1ox}{}^2}{2} \left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - VFBCV - V_{bs}\right)}{K_{1ox}{}^2}} \right)$$

$$Q_g = -Q_{sub0}$$

$$Q_{inv} = 0$$

Strong inversion region

$$V_{dsat,cv} = \frac{V_{gs} - V_{th}}{A_{bulk}'}$$

$$A_{bulk}' = A_{bulk}\left(1 + \left(\frac{CLC}{L_{eff}}\right)^{CLE}\right)$$

$$V_{th} = VFBCV + \Phi_s + K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

Linear region

$$Q_g = C_{oxe}W_{active}L_{active}\left(V_{gs} - VFBCV - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}'V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'V_{ds}}{2}\right)}\right)$$

$$Q_b = C_{oxe}W_{active}L_{active}\left(VFBCV - V_{th} - \Phi_s + \frac{(1 - A_{bulk}')V_{ds}}{2} - \frac{(1 - A_{bulk}')A_{bulk}'V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'V_{ds}}{2}\right)}\right)$$

50/50 partitioning:

$$Q_{inv} = -C_{oxe}W_{active}L_{active}\left(V_{gs} - V_{th} - \Phi_s - \frac{A_{bulk}'V_{ds}}{2} + \frac{A_{bulk}'^2V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}'V_{ds}}{2}\right)}\right)$$

$$Q_s = Q_d = 0.5Q_{inv}$$

40/60 partitioning:

$$Q_d = -C_{oxe} W_{active} L_{active} \left(\frac{V_{gs} - V_{th}}{2} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}' V_{ds} \left[\frac{(V_{gs} - V_{th})^2}{6} - \frac{A_{bulk}' V_{ds} (V_{gs} - V_{th})}{8} + \frac{(A_{bulk}' V_{ds})^2}{40} \right]}{12 \left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} \right)^2} \right)$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

0/100 partitioning:

$$Q_d = -C_{oxe} W_{active} L_{active} \left(\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk}' V_{ds}}{4} - \frac{(A_{bulk}' V_{ds})^2}{24} \right)$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

Saturation region

$$Q_g = C_{oxe} W_{active} L_{active} \left(V_{gs} - VFBCV - \Phi_s - \frac{V_{dsat}}{3} \right)$$

$$Q_b = -C_{oxe} W_{active} L_{active} \left(VFBCV + \Phi_s - V_{th} + \frac{(1 - A_{bulk}') V_{dsat}}{3} \right)$$

50/50 partitioning:

$$Q_s = Q_d = -\frac{1}{3} C_{oxe} W_{active} L_{active} (V_{gs} - V_{th})$$

40/60 partitioning:

$$Q_d = -\frac{4}{15} C_{oxe} W_{active} L_{active} (V_{gs} - V_{th})$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

0/100 partitioning:

$$Q_d = 0$$

$$Q_s = -\left(Q_g + Q_b\right)$$

7.4.2 *capMod* = 1

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + dQ_{sub}\right)$$

$$Q_b = -\left(Q_{acc} + Q_{sub0} + dQ_{sub}\right)$$

$$Q_{inv} = Q_s + Q_d$$

$$Q_{acc} = -W_{active} L_{active} C_{oxe} \cdot \left(V_{FBeff} - V_{fbzb}\right)$$

$$Q_{sub0} = -W_{active} L_{active} C_{oxe} \cdot \frac{{K_{1ox}}^2}{2} \cdot \left[-1 + \sqrt{1 + \frac{4\left(V_{gse} - V_{FBeff} - V_{gsteff} - V_{bseff}\right)}{{K_{1ox}}^2}} \right]$$

$$V_{dsat,cv} = \frac{V_{gsteffcv}}{A_{bulk}'}$$

$$Q_{inv} = -W_{active}L_{active}C_{oxe}\cdot\left[V_{gsteff,cv} - \frac{1}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)}\right]$$

$$dQ_{sub} = W_{active}L_{active}C_{oxe}\cdot\left[\frac{1-A_{bulk}'}{2}V_{cveff} - \frac{\left(1-A_{bulk}'\right)\cdot A_{bulk}'V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)}\right]$$

50/50 charge partitioning:

$$Q_S = Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2}\left[V_{gsteff,cv} - \frac{1}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)}\right]$$

40/60 charge partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxe}}{2\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l}V_{gsteff,cv}^{\ 3} - \frac{4}{3}V_{gsteff,cv}^{\ 2}A_{bulk}'V_{cveff}\\ + \frac{2}{3}V_{gsteff,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\end{array}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l}V_{gsteff,cv}^{\ 3} - \frac{5}{3}V_{gsteff,cv}^{\ 2}A_{bulk}'V_{cveff}\\ + V_{gsteff,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\end{array}\right]$$

0/100 charge partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxe}}{2}\cdot\left[V_{gsteff,cv}+\frac{1}{2}A_{bulk}'V_{cveff}-\frac{A_{bulk}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv}-A_{bulk}'V_{cveff}/2\right)}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2}\cdot\left[V_{gsteff,cv}-\frac{3}{2}A_{bulk}'V_{cveff}+\frac{A_{bulk}'^2V_{cveff}^2}{4\cdot\left(V_{gsteff,cv}-A_{bulk}'V_{dveff}/2\right)}\right]$$

7.4.3 *capMod* = 2

$$Q_{acc} = W_{active}L_{active}C_{oxeff}\cdot V_{gbacc}$$

$$V_{gbacc} = \frac{1}{2}\cdot\left[V_0+\sqrt{V_0^2+0.08V_{fbzb}}\right]$$

$$V_0 = V_{fbzb}+V_{bseff}-V_{gs}-0.02$$

$$V_{cveff} = V_{dsat}-\frac{1}{2}\cdot\left(V_1+\sqrt{V_1^2+0.08V_{dsat}}\right)$$

$$V_1 = V_{dsat}-V_{ds}-0.02$$

$$V_{dsat} = \frac{V_{gsteff,cv}-j_d}{A_{bulk}'}$$

$$j_d = \Phi_s-2\Phi_B = n_t\ln\left(1+\frac{V_{gsteffCV}\cdot(V_{gsteffCV}+2K_{1ox}\sqrt{2\Phi_B}}{MOIN\cdot K_{1ox}^2 n_t}\right)$$

$$\left(V_{gsteff,CV} - j_d\right)_{eff} = 0.5 \cdot \left[\left(V_{gsteff,CV} - j_d - 0.001\right) + \sqrt{\left(V_{gsteff,CV} - j_d - 0.001\right)^2 + V_{gsteff,CV} \cdot 0.004}\right]$$

$$Q_{sub0} = -W_{active} L_{active} C_{oxeff} \cdot \frac{K_{1ox}{}^2}{2} \cdot \left[-1 + \sqrt{1 + \frac{4\left(V_{gse} - V_{FBeff} - V_{bseffs} - V_{gsteff,cv}\right)}{K_{1ox}{}^2}}\right]$$

$$\boldsymbol{Q_{inv}} = -\boldsymbol{W_{active} L_{active} C_{oxeff}} \left[\left(\boldsymbol{V_{gsteff,cv}} - j_d\right)_{\boldsymbol{eff}} - \frac{1}{2}\boldsymbol{A_{bulk}'V_{cveff}} + \frac{\boldsymbol{A_{bulk}'^2 V_{cveff}^2}}{12\left[\left(\boldsymbol{V_{gsteff,cv}} - j_d\right)_{\boldsymbol{eff}} - \boldsymbol{A_{bulk}'V_{cveff}}/2\right]}\right]$$

$$dQ_{sub} = W_{active} L_{active} C_{oxeff} \cdot \left[\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{\left(1 - A_{bulk}'\right) \cdot A_{bulk}' V_{cveff}^2}{12 \cdot \left(V_{gsteff,cv} - j_d - A_{bulk}' V_{cveff}/2\right)}\right]$$

50/50 partitioning:

$$\boldsymbol{Q_S} = \boldsymbol{Q_D} = -\frac{\boldsymbol{W_{active} L_{active} C_{oxeff}}}{2}\left[\boldsymbol{V_{gsteff,cv}} - j_d - \frac{1}{2}\boldsymbol{A_{bulk}'V_{cveff}} + \frac{\boldsymbol{A_{bulk}'^2 V_{cveff}^2}}{12\left[\left(\boldsymbol{V_{gsteff,cv}} - j_d\right)_{\boldsymbol{eff}} - \boldsymbol{A_{bulk}'V_{cveff}}/2\right]}\right]$$

40/60 partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxeff}}{2\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l}\left(V_{gsteff,cv} - j_d\right)^3 - \frac{4}{3}\left(V_{gsteff,cv} - j_d\right)^2 A_{bulk}'V_{cveff} \\ + \frac{2}{3}\left(V_{gsteff,cv} - j_d\right)\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\end{array}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l}\left(V_{gsteff,cv} - j_d\right)^3 - \frac{5}{3}\left(V_{gsteff,cv} - j_d\right)^2 A_{bulk}'V_{cveff} \\ + \left(V_{gsteff,cv} - j_d\right)\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\end{array}\right]$$

0/100 partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxeff}}{2}\cdot\left[V_{gsteff,cv} - j_d + \frac{1}{2}A_{bulk}'V_{cveff} - \frac{A_{bulk}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)}\right]$$

$$\boldsymbol{Q_D} = -\frac{\boldsymbol{W_{active}L_{active}C_{oxeff}}}{2}\times\left[\left(\boldsymbol{V_{gsteff,cv}} - j_d\right)_{\boldsymbol{eff}} - \frac{3}{2}\boldsymbol{A_{bulk}'V_{cveff}} + \frac{\boldsymbol{A_{bulk}'^2V_{cveff}^2}}{4\times\left(\left(\boldsymbol{V_{gsteff,cv}} - j_d\right)_{\boldsymbol{eff}} - \boldsymbol{A_{bulk}'V_{dveff}}/2\right)}\right]$$

7.5 Fringing/Overlap Capacitance Models

7.5.1 Fringing capacitance model

The fringing capacitance consists of a bias-independent outer fringing capacitance and a bias-dependent inner fringing capacitance. Only the bias-independent outer fringing capacitance (*CF*) is modeled. If *CF* is not given, it is calculated by

(7.5.1)

$$CF = \frac{2 \cdot EPSROX \cdot \varepsilon_0}{\pi} \cdot \log\left(1 + \frac{4.0e-7}{TOXE}\right)$$

7.5.2 Overlap capacitance model

An accurate overlap capacitance model is essential. This is especially true for the drain side where the effect of the capacitance is amplified by the transistor gain. In old capacitance models this capacitance is assumed to be bias independent. However, experimental data show that the overlap capacitance changes with gate to source and gate to drain biases. In a single drain structure or the heavily doped S/D to gate overlap region in a LDD structure the bias dependence is the result of depleting the surface of the source and drain regions. Since the modulation is expected to be very small, we can model this region with a constant capacitance. However in LDD MOSFETs a substantial portion of the LDD region can be depleted, both in the vertical and lateral directions. This can lead to a large reduction of the overlap capacitance. This LDD region can be in accumulation or depletion. We use a single equation for both regions by using such smoothing parameters as $V_{gs,overlap}$ and $V_{gd,overlap}$ for the source and drain side, respectively. Unlike the case with the intrinsic capacitance, the overlap capacitances are reciprocal. In other words, $C_{gs,overlap} = C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$.

If capMod is non-zero, BSIM4 uses the bias-dependent overlap capacitance model; otherwise, a simple bias-independent model will be used.

Bias-dependent overlap capacitance model

(i) Source side

(7.5.2)

$$\frac{Q_{overlaps}}{W_{active}} = CGSO \cdot V_{gs} + CGSL\left(V_{gs} - V_{gs,overlap} - \frac{CKAPPAS}{2}\left(-1 + \sqrt{1 - \frac{4V_{gs,overlap}}{CKAPPAS}} \right) \right)$$

(7.5.3)

$$V_{gs,overlap} = \frac{1}{2}\left(V_{gs} + d_1 - \sqrt{\left(V_{gs} + d_1\right)^2 + 4d_1} \right), \quad d_1 = 0.02V$$

(ii) Drain side

(7.5.4)

$$\frac{Q_{overlapd}}{W_{active}} = CGDO \cdot V_{gd} + CGDL\left(V_{gd} - V_{gd,overlap} - \frac{CKAPPAD}{2}\left(-1 + \sqrt{1 - \frac{4V_{gd,overlap}}{CKAPPAD}} \right) \right)$$

(7.5.5)

$$V_{gd,overlap} = \frac{1}{2}\left(V_{gd} + d_1 - \sqrt{\left(V_{gd} + d_1\right)^2 + 4d_1} \right), \quad d_1 = 0.02V$$

(iii) Gate Overlap Charge

(7.5.6)

$$Q_{overlap,g} = -\left(Q_{overlap,d} + Q_{overlap,s} + \left(CGBO \cdot L_{active}\right) \cdot V_{gb}\right)$$

where *CGBO* is a model parameter, which represents the gate-to-body overlap capacitance per unit channel length.

Bias-independent overlap capacitance model

If ***capMod*** = 0, a bias-independent overlap capacitance model will be used. In this case, model parameters *CGSL*, *CGDL*, *CKAPPAS* and *CKAPPD* all have no effect.

The gate-to-source overlap charge is expressed by

$$Q_{overlap,s} = W_{active} \cdot CGSO \cdot V_{gs}$$

The gate-to-drain overlap charge is calculated by

$$Q_{overlap,d} = W_{active} \cdot CGDO \cdot V_{gd}$$

The gate-to-substrate overlap charge is computed by

$$Q_{overlap,b} = L_{active} \cdot CGBO \cdot V_{gb}$$

Default *CGSO* and *CGDO*

If *CGSO* and *CGDO* (the overlap capacitances between the gate and the heavily doped source/drain regions, respectively) are not given, they will be calculated. Appendix A gives the information on how *CGSO*, *CGDO* and *CGBO* are calculated.

Chapter 8: High-Speed/RF Models

As circuit speed and operating frequency rise, the need for accurate prediction of circuit performance near cut-off frequency or under very rapid transient operation becomes critical. BSIM4.0.0 provides a set of accurate and efficient high-speed/RF (radio frequency) models which consist of three modules: charge-deficit non-quasi-static (NQS) model, intrinsic-input resistance (IIR) model (bias-dependent gate resistance model), and substrate resistance network model. The charge-deficit NQS model comes from BSIM3v3.2 NQS model [11] but many improvements are added in BSIM4. The IIR model considers the effect of channel-reflected gate resistance and therefore accounts for the first-order NQS effect [12]. Thus, the charge-deficit NQS model and the IIR model should not be turned on simultaneously. These two models both work with multi-finger configuration. The substrate resistance model does not include any geometry dependence.

8.1 Charge-Deficit Non-Quasi-Static (NQS) Model

BSIM4 uses two separate model selectors to turn on or off the charge-deficit NQS model in transient simulation (using ***trnqsMod***) and AC simulation (using ***acnqsMod***). The AC NQS model does not require the internal NQS charge node that is needed for the transient NQS model. The transient and AC NQS models are developed from the same fundamental physics: the channel/gate charge response to the external signal are relaxation-time (t) dependent and the transcapacitances

and transconductances (such as G_m) for AC analysis can therefore be expressed as functions of jwt.

MOSFET channel region is analogous to a bias-dependent RC distributed transmission line (Figure 8-1a). In the Quasi-Static (QS) approach, the gate capacitor node is lumped with the external source and drain nodes (Figure 8-1b). This ignores the finite time for the channel charge to build-up. One way to capture the NQS effect is to represent the channel with *n* transistors in series (Figure 8-1c), but it comes at the expense of simulation time. The BSIM4 charge-deficit NQS model uses Elmore equivalent circuit to model channel charge build-up, as illustrated in Figure 8-1d..

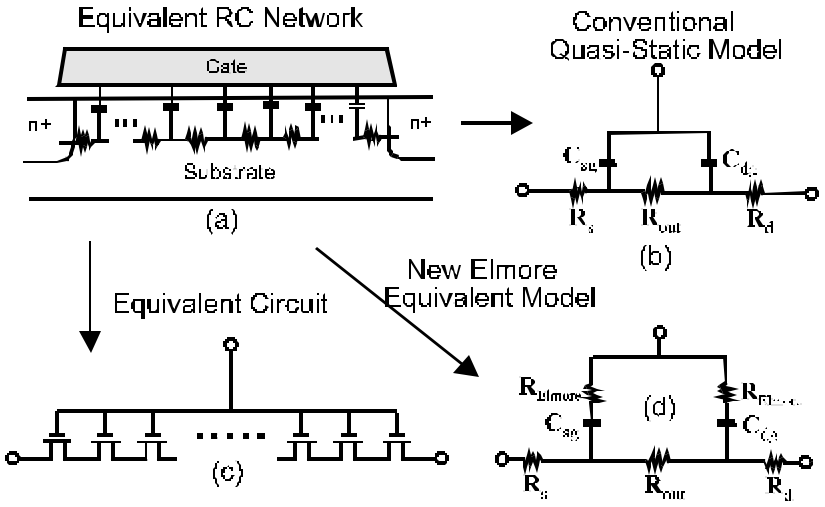


Figure 8-1. Quasi-Static and Non-Quasi-Static models for SPICE analysis.

8.1.1 The Transient Model

The transient charge-deficit NQS model can be turned on by setting ***trnqsMod*** = 1 and off by setting ***trnqsMod*** = 0.

Figure 8-2 shows the RC sub-circuit of charge deficit NQS model for transient simulation [13]. An internal node, $Q_{def}(t)$, is created to keep track of the amount of deficit/surplus channel charge necessary to reach equilibrium. The resistance ***R*** is determined from the RC time constant (t). The current source $i_{cheq}(t)$ represents the equilibrium channel charging effect. The capacitor ***C*** is to be the value of C_{fact} (with a typical value of 1×10^{-9} Farad [11]) to improve simulation accuracy. Q_{def} now becomes

$$Q_{def}(t) = V_{def} \times C_{fact} \tag{8.1.1}$$

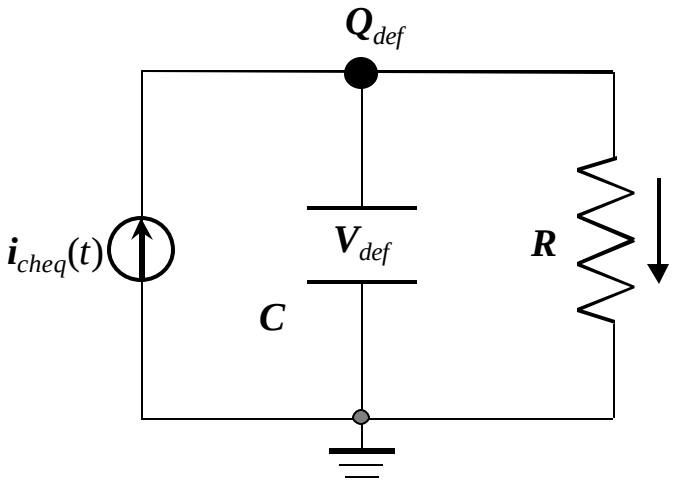


Figure 8-2. Charge deficit NQS sub-circuit for transient analysis.

Considering both the transport and charging component, the total current related to the terminals D, G and S can be written as

(8.1.2)

$$i_{D,G,S}(t) = I_{D,G,S}(\mathrm{DC}) + \frac{\partial Q_{d,g,s}(t)}{\partial t}$$

Based on the relaxation time approach, the terminal charge and corresponding charging current are modeled by

(8.1.3)

$$Q_{def}(t) = Q_{cheq}(t) - Q_{ch}(t)$$

and

(8.1.4a)

$$\frac{\partial Q_{def}(t)}{\partial t} = \frac{\partial Q_{cheq}(t)}{\partial t} - \frac{Q_{def}(t)}{t}$$

(8.1.4b)

$$\frac{\partial Q_{d,g,s}(t)}{\partial t} = D, G, S_{xpart} \frac{Q_{def}(t)}{t}$$

where D,G,S_{xpart} are charge deficit NQS channel charge partitioning number for terminals D, G and S, respectively; $D_{xpart} + S_{xpart} = 1$ and $G_{xpart} = -1$.

The transit time t is equal to the product of R_{ii} and $W_{eff}L_{eff}C_{oxe}$, where R_{ii} is the intrinsic-input resistance [12] given by

(8.1.5)

$$\frac{1}{R_{ii}} = XRCRG1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff} m_{eff} C_{oxeff} k_B T}{q L_{eff}} \right)$$

where C_{oxeff} is the effective gate dielectric capacitance calculated from the DC model. Note that R_{ii} in (8.1.5) considers both the drift and diffusion componets of the channel conduction, each of which dominates in inversion and subthreshold regions, respectively.

8.1.2 The AC Model

Similarly, the small-signal AC charge-deficit NQS model can be turned on by setting ***acnqsMod*** = 1 and off by setting ***acnqsMod*** = 0.

For small signals, by substituting (8.1.3) into (8.1.4b), it is easy to show that in the frequency domain, $Q_{ch}(t)$ can be transformed into

(8.1.6)

$$\Delta Q_{ch}(t) = \frac{\Delta Q_{cheq}(t)}{1 + jwt}$$

where w is the angular frequency. Based on (8.1.6), it can be shown that the transcapacitances C_{gi}, C_{si}, and C_{di} (i stands for any of the G, D, S and B terminals of the device) and the channel transconductances G_m, G_{ds}, and G_{mbs} all become complex quantities. For example, now G_m have the form of

(8.1.7)

$$G_m = \frac{G_{m0}}{1+w^2t^2} + j\left(-\frac{G_{m0}\cdot wt}{1+w^2t^2}\right)$$

and

(8.1.8)

$$C_{dg} = \frac{C_{dg0}}{1+w^2t^2} + j\left(-\frac{C_{dg0}\cdot wt}{1+w^2t^2}\right)$$

Those quantities with sub "0" in the above two equations are known from OP (operating point) analysis.

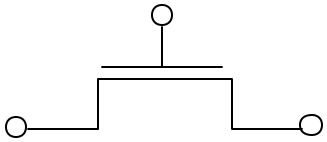
8.2 Gate Electrode Electrode and Intrinsic-Input Resistance (IIR) Model

8.2.1 General Description

BSIM4 provides four options for modeling gate electrode resistance (bias-independent) and intrinsic-input resistance (IIR, bias-dependent). The IIR model considers the relaxation-time effect due to the distributive RC nature of the channel region, and therefore describes the first-order non-quasi-static effect. Thus, the IIR model should not be used together with the charge-deficit NQS model at the same time. The model selector ***rgateMod*** is used to choose different options.

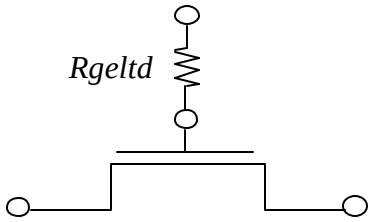
8.2.2 Model Option and Schematic

rgateMod = 0 (zero-resistance):



In this case, no gate resistance is generated.

rgateMod = 1 (constant-resistance):



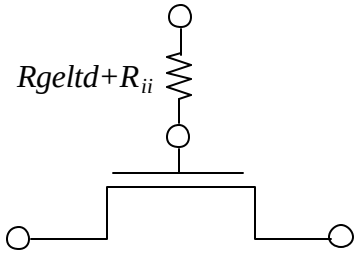
In this case, only the electode gate resistance (bias-independent) is generated by adding an internal gate node. Rgeltd is give by

(8.1.9)

$$Rgeltd = \frac{RSHG \cdot \left(XGW + \frac{W_{effcj}}{3 \cdot NGCON}\right)}{NGCON \cdot \left(L_{drawn} - XGL\right) \cdot NF}$$

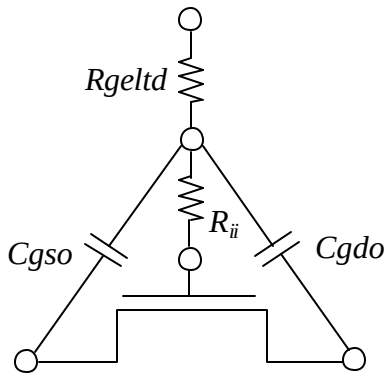
Refer to Chapter 7 for the layout parameters in the above equation.

rgateMod = 2 (IIR model with variable resistance):



In this case, the gate resistance is the sum of the electrode gate resistance (8.1.9) and the intrinsic-input resistance R_{ii} as given by (8.1.5). An internal gate node will be generated. ***trnqsMod*** = 0 (default) and ***acnqsMod*** = 0 (default) should be selected for this case.

rgateMod = 3 (IIR model with two nodes):



In this case, the gate electrode resistance given by (8.1.9) is in series with the intrinsic-input resistance R_{ii} as given by (8.1.5) through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance. ***trnqsMod*** = 0 (default) and ***acnqsMod*** = 0 (default) should be selected for this case.

8.3 Substrate Resistance Network

8.3.1 General Description

For CMOS RF circuit simulation, it is essential to consider the high frequency coupling through the substrate. BSIM4 offers a flexible built-in substrate resistance network. This network is constructed such that little simulation efficiency penalty will result. Note that the substrate resistance parameters as listed in Appendix A should be extracted for the total device, not on a per-finger basis.

8.3.2 Model Selector and Topology

The model selector ***rbodyMod*** can be used to turn on or turn off the resistance network.

rbodyMod = 0 (Off):

No substrate resistance network is generated at all.

rbodyMod = 1 (On):

All five resistances in the substrate network as shown schematically below are present simultaneously.

A minimum conductance, *GBMIN*, is introduced in parallel with each resistance and therefore to prevent infinite resistance values, which would otherwise cause poor convergence. In Figure 8-3, *GBMIN* is merged into each resistance to simplify the representation of the model topology. Note that the intrinsic model substrate reference point in this case is the internal body node **bNodePrime**, into which the impact ionization current I_{ii} and the GIDL current I_{GIDL} flow.

rbodyMod = 2 (On : Scalable Substrate Network):

The schematic is similar to ***rbodyMod*** = 1 but all the five resistors in the substrate network are now scalable with a possibility of chosing either five resistors, three resistors or one resistor as the substrate network.

The resistors of the substrate network are scalable with respect to channel length (*L*), channel width (*W*) and number of fingers (*NF*). The scalable model allows to account for both horizontal and vertical contacts.

The scalable resistors *RBPS* and *RBPD* are evaluated through

(8.1.10)

$$RBPS = RBPS\ 0 \bullet \left(\frac{L}{10^{-6}}\right)^{RBPSL} \bullet \left(\frac{W}{10^{-6}}\right)^{RBPSW} \bullet NF^{\ RBPSNF}$$

(8.1.11)

$$RBPD = RBPD\ 0 \bullet \left(\frac{L}{10^{-6}}\right)^{RBPDL} \bullet \left(\frac{W}{10^{-6}}\right)^{RBPDW} \bullet NF^{\ RBPDNF}$$

The resistor *RBPB* consists of two parallel resistor paths, one to the horizontal contacts and other to the vertical contacts. These two resistances are scalable and *RBPB* is given by a parallel combination of these two resistances.

(8.1.12)

$$RBPBX = RBPBX\ 0 \bullet \left(\frac{L}{10^{-6}}\right)^{RBPBXL} \bullet \left(\frac{W}{10^{-6}}\right)^{RBPBXW} \bullet NF^{\ RBPBNF}$$

$$RBPBY = RBPBY\ 0 \bullet \left(\frac{L}{10^{-6}}\right)^{RBPBYL} \bullet \left(\frac{W}{10^{-6}}\right)^{RBPBYW} \bullet NF^{\ RBPBYNF}$$

$$RBPB = \frac{RBPBX \bullet RBPBY}{RBPBX + RBPBY}$$

The resistors *RBSB* and *RBDB* share the same scaling parameters but have different scaling prefactors. These resistors are modeled in the same way as *RBPB*. The equations for *RBSB* are shown below. The calculation for *RBDB* follows *RBSB*.

(8.1.13)

$$RBSBX = RBSBX\ 0 \bullet \left(\frac{L}{10^{-6}}\right)^{RBSDBXL} \bullet \left(\frac{W}{10^{-6}}\right)^{RBSDBXW} \bullet NF^{RBSDBXNF}$$

$$RBSBX = RBSBX\ 0 \bullet \left(\frac{L}{10^{-6}}\right)^{RBSDBXL} \bullet \left(\frac{W}{10^{-6}}\right)^{RBSDBXW} \bullet NF^{RBSDBXNF}$$

$$RBSB = \frac{RBSBX \bullet RBSBY}{RBSBX + RBSBY}$$

The implementation of ***rbodyMod*** = 2 allows the user to chose between the 5-R network (with all five resistors), 3-R network (with *RBPS*, *RBPD* and *RBPB*) and 1-R network (with only *RBPB*).

If the user doesn't provide both the scaling parameters *RBSBX0* and *RBSBY0* for *RBSB* **OR** both the scaling parameters *RBDBX0* and *RBDBY0* for *RBDB*, then the conductances for both *RBSB* and *RBDB* are set to *GBMIN*. This converts the 5-R schematic to 3-R schematic where the substrate network consists of the resistors *RBPS*, *RBPD* and *RBPB*. *RBPS*, *RBPD* and *RBPB* are then calculated using (8.1.10), (8.1.11) and (8.1.12).

If the user chooses not to provide either of *RBPS0* or *RBPD0*, then the 5-R schematic is converted to 1-R network with only one resistor *RBPB*. The conductances for *RBSB* and *RBDB* are set to *GBMIN*. The resistances *RBPS* and *RBPD* are set to 1e-3 Ohm. The resistor *RBPB* is then calculated using (8.1.12).

In all other situations, 5-R network is used with the resistor values calculated from the equations aforementioned.

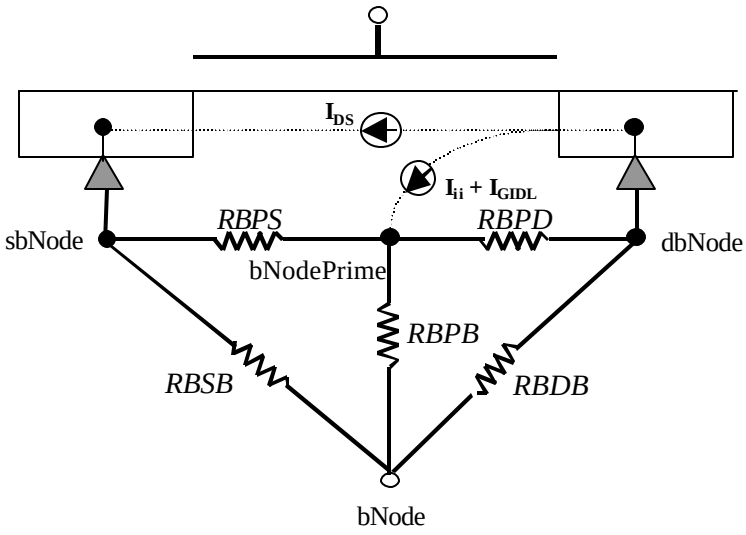


Figure 8-3. Topology with the substrate resistance network turned on.

Chapter 9: Noise Modeling

The following noise sources in MOSFETs are modeled in BSIM4 for SPICE noise ananlysis: flicker noise (also known as 1/f noise), channel thermal noise and induced gate noise and their correlation, thermal noise due to physical resistances such as the source/ drain, gate electrode, and substrate resistances, and shot noise due to the gate dielectric tunneling current. A complete list of the noise model parameters and explanations are given in Appendix A.

9.1 Flicker Noise Models

9.1.1 General Description

BSIM4 provides two flicker noise models. When the model selector ***fnoiMod*** is set to 0, a simple flicker noise model which is convenient for hand calculations is invoked. A unified physical flicker noise model, which is the default model, will be used if ***fnoiMod*** = 1. These two modes come from BSIM3v3, but the unified model has many improvements. For instance, it is now smooth over all bias regions and considers the bulk charge effect.

9.1.2 Equations

- ***fnoiMod* = 0 (simple model)**

The noise density is

(9.1.1)

$$S_{id}(f) = \frac{KF \cdot I_{ds}^{\ AF}}{C_{oxe} L_{eff}^{\ 2} f^{EF}}$$

where *f* is device operating frequency.

- ***fnoiMod* = 1 (unified model)**

The physical mechanism for the flicker noise is trapping/detrapping-related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobilities in the channel. The unified flicker noise model captures this physical process.

In the inversion region, the noise density is expressed as [14]

(9.1.2)

$$S_{id,inv}(f) = \frac{k_B T q^2 m_{eff} I_{ds}}{C_{oxe}(L_{eff} - 2 \cdot LINTNOI)^2 A_{bulk} f^{ef} \cdot 10^{10}} \left(NOIA \cdot \log\left(\frac{N_0 + N^*}{N_l + N^*}\right) + NOIB \cdot (N_0 - N_l) + \frac{NOIC}{2}(N_0^{\ 2} - N_l^{\ 2}) \right)$$
$$+ \frac{k_B T I_{ds}^{\ 2} \Delta L_{clm}}{W_{eff} \cdot (L_{eff} - 2 \cdot LINTNOI)^2 f^{ef} \cdot 10^{10}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^{\ 2}}{(N_l + N^*)^2}$$

where m_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source side given by

(9.1.3)

$$N_0 = C_{oxe} \cdot V_{gsteff} / q$$

The parameter N_l is the charge density at the drain end given by

(9.1.4)

$$N_l = C_{oxe} \cdot V_{gsteff} \cdot \left(1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2n_t} \right) \Big/ q$$

N^* is given by

(9.1.5)

$$N^* = k_B T \cdot \left(C_{oxe} + C_d + CIT \right) \Big/ q^2$$

where *CIT* is a model parameter from DC IV and C_d is the depletion capacitance.

DL_{clm} is the channel length reduction due to channel length modulation and given by

(9.1.6)

$$\Delta L_{\text{clm}} = Litl \cdot \log \left(\frac{\frac{V_{ds} - V_{dseff}}{Litl} + EM}{E_{sat}} \right)$$

$$E_{sat} = \frac{2VSAT}{m_{eff}}$$

In the subthreshold region, the noise density is written as

(9.1.7)

$$S_{id,subVt}(f) = \frac{NOIA \cdot k_B T \cdot {I_{ds}}^2}{W_{eff} L_{eff} f^{EF} N^{*2} \cdot 10^{10}}$$

The total flicker noise density is

(9.1.8)

$$S_{id}(f) = \frac{S_{id,inv}(f) \times S_{id,subvt}(f)}{S_{id,subvt}(f) + S_{id,inv}(f)}$$

9.2 Channel Thermal Noise

There are two channel thermal noise models in BSIM4. One is a charge-based model (default model) similar to that used in BSIM3v3.2. The other is the holistic model. These two models can be selected through the model selector ***tnoiMod***.

- ***tnoiMod* = 0 (charge based)**

The noise current is given by

(9.2.1)

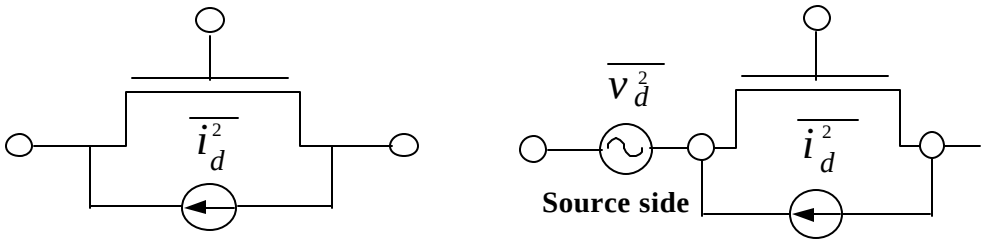
$$\overline{i_d^2} = \frac{4k_B T \Delta f}{R_{ds}(V) + \frac{{L_{eff}}^2}{m_{eff}|Q_{inv}|}} \cdot NTNOI$$

where $R_{ds}(V)$ is the bias-dependent LDD source/drain resistance, and the parameter *NTNOI* is introduced for more accurate fitting of short-channel devices. Q_{inv} is modeled by

(9.2.2)

$$Q_{inv} = W_{active} L_{active} C_{oxeff} \cdot NF \cdot \left[V_{gsteff} - \frac{A_{bulk} V_{dseff}}{2} + \frac{A_{bulk}^{\ 2} V_{dseff}^{\ 2}}{12 \cdot \left(V_{gsteff} - \frac{A_{bulk} V_{dseff}}{2} \right)} \right]$$

Figure 9-1a shows the noise source connection for ***tnoiMod*** = 0.



(a) ***tnoiMod*** = 0 (b) ***tnoiMod*** = 1

Figure 9-1. Schematic for BSIM4 channel thermal noise modeling.

- ***tnoiMod*** **= 1 (holistic)**

In this thermal noise model, all the short-channel effects and velocity saturation effect incorporated in the IV model are automatically included, hency the name “holistic thermal noise model”. In addition, the amplification of the channel thermal noise through G_m and G_{mbs} as well as the induced-gate noise with partial correlation to the channel thermal noise are all captured in the new “noise partition” model. Figure 9-1b shows schematically that part of the channel thermal noise source is partitioned to the source side.

The noise voltage source partitioned to the source side is given by

(9.2.3)

$$\overline{v_d^{\,2}} = 4k_B T \cdot q_{tnoi}^{\,2} \cdot \frac{V_{dseff}\Delta f}{I_{ds}}$$

and the noise current source put in the channel region with gate and body amplication is given by

(9.2.4)

$$\overline{i_d^{\,2}} = 4k_B T \frac{V_{dseff}\Delta f}{I_{ds}}\left[G_{ds} + b_{tnoi}\cdot\left(G_m + G_{mbs}\right)\right]^2 - \overline{v_d^{\,2}}\cdot\left(G_m + G_{ds} + G_{mbs}\right)^2$$

where

(9.2.5)

$$q_{tnoi} = RNOIB\cdot\left[1 + TNOIB\cdot L_{eff}\cdot\left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right]$$

and

(9.2.6)

$$b_{tnoi} = RNOIA\cdot\left[1 + TNOIA\cdot L_{eff}\cdot\left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right]$$

where *RNOIB* and *RNOIA* are model parameters with default values 0.37 and 0.577 respectively.

9.3 Other Noise Sources Modeled

BSIM4 also models the thermal noise due to the substrate, electrode gate, and source/drain resistances. Shot noise due to various gate tunneling components is modeled as well.

Chapter 10: Asymmetric MOS Junction Diode Models

10.1 Junction Diode IV Model

In BSIM4, there are three junction diode IV models. When the IV model selector ***dioMod*** is set to 0 ("resistance-free"), the diode IV is modeled as resistance-free with or without breakdown depending on the parameter values of *XJBVS* or *XJBVD*. When ***dioMod*** is set to 1 ("breakdown-free"), the diode is modeled exactly the same way as in BSIM3v3.2 with current-limiting feature in the forward-bias region through the limiting current parameters *IJTHSFWD* or *IJTHDFWD*; diode breakdown is not modeled for ***dioMod*** = 1 and *XJBVS*, *XJBVD*, *BVS*, and *BVD* parameters all have no effect. When ***dioMod*** is set to 2 ("resistance-and-breakdown"), BSIM4 models the diode breakdown with current limiting in both forward and reverse operations. In general, setting ***dioMod*** to 1 produces fast convergence.

10.1.1 Source/Body Junction Diode

In the following, the equations for the source-side diode are given. The model parameters are shown in Appendix A.

- ***dioMod* = 0 (resistance-free)**

(10.1.1)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{\min}$$

where I_{sbs} is the total saturation current consisting of the components through the gate-edge (J_{sswgs}) and isolation-edge sidewalls (J_{ssws}) and the bottom junction (J_{ss}),

(10.1.2)

$$I_{sbs} = A_{seff} J_{ss}(T) + P_{seff} J_{ssws}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T)$$

where the calculation of the junction area and perimeter is discussed in Chapter 11, and the temperature-dependent current density model is given in Chapter 12. In (10.1.1), $f_{breakdown}$ is given by

(10.1.3)

$$f_{breakdown} = 1 + XJBVS \cdot \exp\left(-\frac{q \cdot (BVS + V_{bs})}{NJS \cdot k_B TNOM}\right)$$

In the above equation, when *XJBVS* = 0, no breakdown will be modeled. If *XJBVS* < 0.0, it is reset to 1.0.

- ***dioMod* = 1 (breakdown-free)**

No breakdown is modeled. The exponential IV term in (10.1.4) is linearized at the limiting current *IJTHSFWD* in the forward-bias model only.

(10.1.4)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] + V_{bs} \cdot G_{\min}$$

- ***dioMod* = 2 (resistance-and-breakdown):**

Diode breakdown is always modeled. The exponential term (10.1.5) is linearized at both the limiting current *IJTHSFWD* in the forward-bias mode and the limiting current *IJTHSREV* in the reverse-bias mode.

(10.1.5)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{\min}$$

For ***dioMod*** = 2, if *XJBVS* <= 0.0, it is reset to 1.0.

10.1.2 Drain/Body Junction Diode

The drain-side diode has the same system of equations as those for the source-side diode, but with a separate set of model parameters as explained in detail in Appendix A.

- ***dioMod* = 0 (resistance-free)**

(10.1.6)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bd} \cdot G_{\min}$$

where I_{sbd} is the total saturation current consisting of the components through the gate-edge (J_{sswgd}) and isolation-edge sidewalls (J_{sswd}) and the bottom junction (J_{sd}),

(10.1.7)

$$I_{sbd} = A_{deff} J_{sd}(T) + P_{deff} J_{sswd}(T) + W_{effcj} \cdot NF \cdot J_{sswgd}(T)$$

where the calculation of the junction area and perimeter is discussed in Chapter 11, and the temperature-dependent current density model is given in Chapter 12. In (10.1.6), $f_{breakdown}$ is given by

(10.1.8)

$$f_{breakdown} = 1 + XJBVD \cdot \exp\left(- \frac{q \cdot (BVD + V_{bd})}{NJD \cdot k_B TNOM} \right)$$

In the above equation, when *XJBVD* = 0, no breakdown will be modeled. If *XJBVD* < 0.0, it is reset to 1.0.

- ***dioMod* = 1 (breakdown-free)**

No breakdown is modeled. The exponential IV term in (10.1.9) is linearized at the limiting current *IJTHSFWD* in the forward-bias model only.

(10.1.9)

$$I_{bd} = I_{sbd} \left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM} \right) - 1 \right] + V_{bd} \cdot G_{\min}$$

- ***dioMod* = 2 (resistance-and-breakdown):**

Diode breakdown is always modeled. The exponential term (10.1.10) is linearized at both the limiting current *IJTHSFWD* in the forward-bias mode and the limiting current *IJTHSREV* in the reverse-bias mode.

(10.1.10)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD\cdot k_B TNOM}\right)-1\right]\cdot f_{breakdown} + V_{bd}\cdot G_{\min}$$

For ***dioMod*** = 2, if *XJBVD* <= 0.0, it is reset to 1.0.

10.1.3 Total Junction Source/Drain Diode Including Tunneling

Total diode current including the carrier recombination and trap-assisted tunneling current in the space-charge region is modeled by:

(10.1.11)

$$\begin{aligned} I_{bs\_total} &= I_{bs} \\ &- W_{effcj}\cdot NF\cdot J_{tsswgs}(T)\cdot\left[exp\left(\frac{-V_{bs}}{NJTSSWG(T)\cdot Vtm0}\cdot\frac{VTSSWGS}{VTSSWGS-V_{bs}}\right)-1\right] \\ &- P_{s,deff} J_{tssws}(T)\left[exp\left(\frac{-V_{bs}}{NJTSSW(T)\cdot Vtm0}\cdot\frac{VTSSWS}{VTSSWS-V_{bs}}\right)-1\right] \\ &- A_{s,deff} J_{tss}(T)\left[exp\left(\frac{-V_{bs}}{NJTS(T)\cdot Vtm0}\cdot\frac{VTSS}{VTSS-V_{bs}}\right)-1\right] + g_{min}\cdot V_{bs} \end{aligned}$$

(10.1.12)

$$\begin{aligned} I_{bd\_total} &= I_{bd} \\ &- W_{effcj}\cdot NF\cdot J_{tsswgd}(T)\cdot\left[exp\left(\frac{-V_{bd}}{NJTSSWG(T)\cdot Vtm0}\cdot\frac{VTSSWGD}{VTSSWGD-V_{bd}}\right)-1\right] \\ &- P_{d,deff} J_{tsswd}(T)\left[exp\left(\frac{-V_{bd}}{NJTSSW(T)\cdot Vtm0}\cdot\frac{VTSSWD}{VTSSWD-V_{bd}}\right)-1\right] \\ &- A_{d,deff} J_{tsd}(T)\left[exp\left(\frac{-V_{bd}}{NJTS(T)\cdot Vtm0}\cdot\frac{VTSD}{VTSD-V_{bd}}\right)-1\right] + g_{min}\cdot V_{bd} \end{aligned}$$

10.2 Junction Diode CV Model

Source and drain junction capacitances consist of three components: the bottom junction capacitance, sidewall junction capacitance along the isolation edge, and sidewall junction capacitance along the gate edge. An analogous set of equations are used for both sides but each side has a separate set of model parameters.

10.2.1 Source/Body Junction Diode

The source-side junction capacitance can be calculated by

$$C_{bs} = A_{seff} C_{jbs} + P_{seff} C_{jbssw} + W_{effcj} \cdot NF \cdot C_{jbsswg} \tag{10.2.1}$$

where C_{jbs} is the unit-area bottom S/B junciton capacitance, C_{jbssw} is the unit-length S/B junction sidewall capacitance along the isolation edge, and C_{jbsswg} is the unit-length S/B junction sidewall capacitance along the gate edge. The effective area and perimeters in (10.2.1) are given in Chapter 11.

C_{jbs} is calculated by

if $V_{bs} < 0$

$$C_{jbs} = CJS(T) \cdot \left(1 - \frac{V_{bs}}{PBS(T)}\right)^{-MJS} \tag{10.2.2}$$

otherwise

(10.2.3)

$$C_{jbs} = CJS(T) \cdot \left(1 + MJS \cdot \frac{V_{bs}}{PBS(T)} \right)$$

C_{jbssw} is calculated by

if $V_{bs} < 0$

(10.2.4)

$$C_{jbssw} = CJSWS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWS(T)} \right)^{-MJSWS}$$

otherwise

(10.2.5)

$$C_{jbssw} = CJSWS(T) \cdot \left(1 + MJSWS \cdot \frac{V_{bs}}{PBSWS(T)} \right)$$

C_{jbsswg} is calculated by

if $V_{bs} < 0$

(10.2.6)

$$C_{jbsswg} = CJSWGS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWGS(T)} \right)^{-MJSWGS}$$

otherwise

(10.2.7)

$$C_{jbsswg} = CJSWGS(T)\cdot\left(1-\frac{V_{bs}}{PBSWGS(T)}\right)^{-MJSWGS}$$

10.2.2 Drain/Body Junction Diode

The drain-side junction capacitance can be calculated by

(10.2.8)

$$C_{bd} = A_{deff}C_{jbd} + P_{deff}C_{jbdsw} + W_{effcj}\cdot NF\cdot C_{jbdswg}$$

where C_{jbd} is the unit-area bottom D/B junciton capacitance, C_{jbdsw} is the unit-length D/B junction sidewall capacitance along the isolation edge, and C_{jbdswg} is the unit-length D/B junction sidewall capacitance along the gate edge. The effective area and perimeters in (10.2.8) are given in Chapter 11.

C_{jbd} is calculated by

if $V_{bd} < 0$

(10.2.9)

$$C_{jbd} = CJD(T)\cdot\left(1-\frac{V_{bd}}{PBD(T)}\right)^{-MJD}$$

otherwise

(10.2.10)

$$C_{jbd} = CJD(T)\cdot\left(1+MJD\cdot\frac{V_{bd}}{PBD(T)}\right)$$

C_{jbdsw} is calculated by

if $V_{bd} < 0$

(10.2.11)

$$C_{jbdsw} = CJSWD(T)\cdot\left(1-\frac{V_{bd}}{PBSWD(T)}\right)^{-MJSWD}$$

otherwise

(10.2.12)

$$C_{jbdsw} = CJSWD(T)\cdot\left(1+MJSWD\cdot\frac{V_{bd}}{PBSWD(T)}\right)$$

C_{jbdswg} is calculated by

if $V_{bd} < 0$

(10.2.13)

$$C_{jbdswg} = CJSWGD(T)\cdot\left(1-\frac{V_{bd}}{PBSWGD(T)}\right)^{-MJSWGD}$$

otherwise

(10.2.14)

$$C_{jbdswg} = CJSWGD(T)\cdot\left(1+MJSWGD\cdot\frac{V_{bd}}{PBSWGD(T)}\right)$$

Chapter 11: Layout-Dependent Parasitics Model

BSIM4 provides a comprehensive and versatile geometry/layout-dependent parasitcs model [15]. It supports modeling of series (such as isolated, shared, or merged source/ drain) and multi-finger device layout, or a combination of these two configurations. This model have impact on every BSIM4 sub-models except the substrate resistance network model. Note that the narrow-width effect in the per-finger device with multi-finger configuration is accounted for by this model. A complete list of model parameters and selectors can be found in Appendix A.

11.1 Geometry Definition

Figure 11-1 schematically shows the geometry definition for various source/drain connections and source/drain/gate contacts. The layout parameters shown in this figure will be used to calculate resistances and source/drain perimeters and areas.

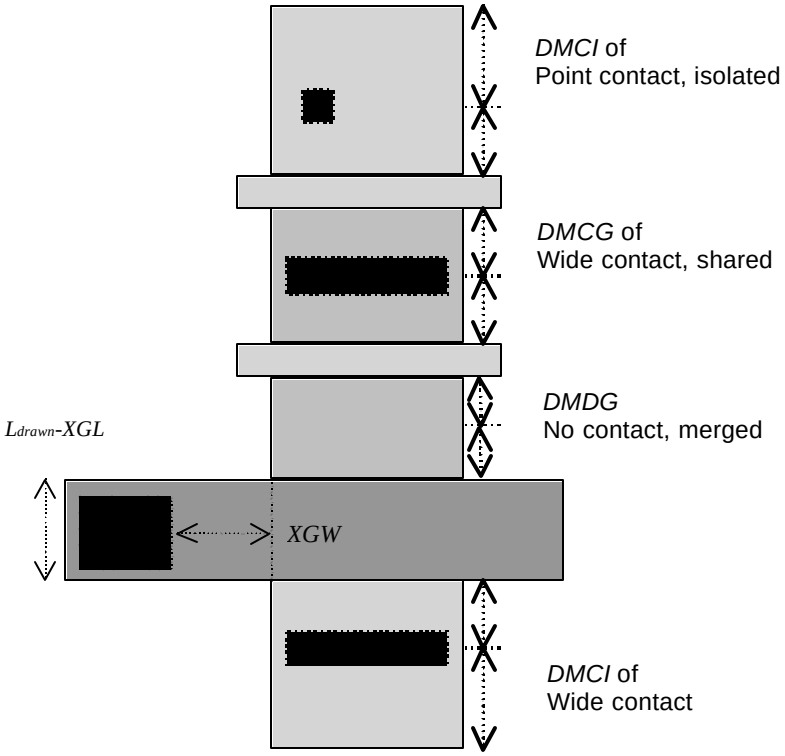


Figure 11-1. Definition for layout parameters.

11.2 Model Formulation and Options

11.2.1 Effective Junction Perimeter and Area

In the following, only the source-side case is illustrated. The same approach is used for the drain side. The effective junction perimeter on the source side is calculated by

If (*PS* is given)
  if (***perMod*** == 0)
    $P_{seff} = PS$
  else
    $P_{seff} = PS - W_{effcj} \cdot NF$
Else
  P_{seff} computed from *NF*, *DWJ*, ***geoMod***, *DMCG*, *DMCI*, *DMDG*, *DMCGT*, and *MIN*.

The effective junction area on the source side is calculated by

If (*AS* is given)
  $A_{seff} = AS$
Else
  A_{seff} computed from *NF*, *DWJ*, ***geoMod***, *DMCG*, *DMCI*, *DMDG*, *DMCGT*, and *MIN*.

In the above, P_{seff} and A_{seff} will be used to calculate junction diode IV and CV. P_{seff} does not include the gate-edge perimeter.

11.2.2 Source/Drain Diffusion Resistance

The source diffusion resistance is calculated by

If (number of source squares *NRS* is given)

$R_{sdiff} = NRS \cdot RSH$

Else if (***rgeoMod*** == 0)

Source diffusion resistance R_{sdiff} is not generated.

Else

R_{sdiff} computed from *NF*, *DWJ*, ***geoMod***, *DMCG*, *DMCI*, *DMDG*, *DMCGT*, *RSH*, and *MIN*.

where the number of source squares *NRS* is an instance parameter. Similarly, the drain diffusion resistance is calculated by

If (number of source squares *NRD* is given)

$R_{ddiff} = NRD \cdot RSH$

Else if (***rgeoMod*** == 0)

Drain diffusion resistance R_{ddiff} is not generated.

Else

R_{ddiff} computed from *NF*, *DWJ*, ***geoMod***, *DMCG*, *DMCI*, *DMDG*, *DMCGT*, *RSH*, and *MIN*.

11.2.3 Gate Electrode Resistance

The gate electrode resistance with multi-finger configuration is modeled by

(11.2.1)

$$Rgeltd = \frac{RSHG \cdot \left(XGW + \frac{W_{effcj}}{3 \cdot NGCON}\right)}{NGCON \cdot \left(L_{drawn} - XGL\right) \cdot NF}$$

11.2.4 Option for Source/Drain Connections

Table 11-1 lists the options for source/drain connections through the model selector ***geoMod***.

geoMod	**End source**	**End drain**	**Note**
0	isolated	isolated	*NF=Odd*
1	isolated	shared	*NF=Odd, Even*
2	shared	isolated	*NF=Odd, Even*
3	shared	shared	*NF=Odd, Even*
4	isolated	merged	*NF=Odd*
5	shared	merged	*NF=Odd, Even*
6	merged	isolated	*NF=Odd*
7	merged	shared	*NF=Odd, Even*
8	merged	merged	*NF=Odd*
9	sha/iso	shared	*NF=Even*
10	shared	sha/iso	*NF=Even*

Table 11-1. *geoMod* options.
For multi-finger devices, all inside S/D diffusions are assumed shared.

11.2.5 Option for Source/Drain Contacts

Talbe 11-2 lists the options for source/drain contacts through the model selector ***rgeoMod***.

rgeoMod	End-source contact	End-drain contact
0	No R_{sdiff}	No R_{ddiff}
1	wide	wide
2	wide	point
3	point	wide
4	point	point
5	wide	merged
6	point	merged
7	merged	wide
8	merged	point

Table 11-2. *rgeoMod* options.

Chapter 12: Temperature Dependence Model

Accurate modeling of the temperature effects on MOSFET characteristics is important to predict circuit behavior over a range of operating temperatures (*T*). The operating temperature might be different from the nominal temperature (*TNOM*) at which the BSIM4 model parameters are extracted. This chapter presents the BSIM4 temperature dependence models for threshold voltage, mobility, saturation velocity, source/drain resistance, and junction diode IV and CV.

12.1 Temperature Dependence of Threshold Voltage

The temperature dependence of V_{th} is modeled by

(12.1.1)

$$V_{th}(T) = V_{th}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \cdot \left(\frac{T}{TNOM} - 1 \right)$$

(12.1.2)

$$V_{fb}(T) = V_{fb}(TNOM) - KT1 \times \left(\frac{T}{TNOM} - 1 \right)$$

(12.1.3)

$$VOFF(T) = VOFF(TNOM) \times [1 + TVOFF \times (T - TNOM)]$$

(12.1.4)

$$VFBSDOFF(T) = VFBSDOFF(TNOM) \times [1 + TVFBSDOFF \times (T - TNOM)]$$

12.2 Temperature Dependence of Mobility

The BSIM4 mobility model parameters have the following temperature dependences depending on the model selected through **TEMPMOD.**

If **TEMPMOD** = 0,

(12.2.1)

$$U0(T) = U0(TNOM) \cdot (T/TNOM)^{UTE}$$

(12.2.2)

$$UA(T) = UA(TNOM) + UA1 \cdot (T/TNOM - 1)$$

(12.2.3)

$$UB(T) = UB(TNOM) + UB1 \cdot (T/TNOM - 1)$$

(12.2.4)

$$UC(T) = UC(TNOM) + UC1 \cdot (T/TNOM - 1)$$

and

(12.2.5)

$$UD(T) = UD(TNOM) + UD1 \times (T/TNOM - 1)$$

If **TEMPMOD** = 1,

$$U0(T) = U0(TNOM) \cdot (T/TNOM)^{UTE} \tag{12.2.6}$$

$$UA(T) = UA(TNOM)[1 + UA1 \cdot (T - TNOM)] \tag{12.2.7}$$

$$UB(T) = UB(TNOM)[1 + UB1 \cdot (T - TNOM)] \tag{12.2.8}$$

$$UC(T) = UC(TNOM)[1 + UC1 \cdot (T - TNOM)] \tag{12.2.9}$$

and

$$\boldsymbol{UD(T) = UD(TNOM)[1 + UD1 \times (T - TNOM)]} \tag{12.2.10}$$

12.3 Temperature Dependence of Saturation Velocity

If **TEMPMOD** = 0, the temperature dependence of *VSAT* is modeled by

(12.3.1)

$$VSAT(T) = VSAT(TNOM) - AT \cdot (T/TNOM - 1)$$

If **TEMPMOD** = 1, the temperature dependence of *VSAT* is modeled by

(12.3.2)

$$VSAT(T) = VSAT(TNOM)[1 - AT \cdot (T - TNOM)]$$

12.4 Temperature Dependence of LDD Resistance

If **TEMPMOD** = 0,

- ***rdsMod* = 0 (internal source/drain LDD resistance)**

(12.4.1)

$$RDSW(T) = RDSW(TNOM) + PRT \cdot (T/TNOM - 1)$$

(12.4.2)

$$RDSWMIN(T) = RDSWMIN(TNOM) + PRT \cdot (T/TNOM - 1)$$

- ***rdsMod* = 1 (external source/drain LDD resistance)**

(12.4.3)

$$RDW(T) = RDW(TNOM) + PRT \cdot (T/TNOM - 1)$$

(12.4.4)

$$RDWMIN(T) = RDWMIN(TNOM) + PRT \cdot (T/TNOM - 1)$$

(12.4.5)

$$RSW(T) = RSW(TNOM) + PRT \cdot (T/TNOM - 1)$$

and

(12.4.6)

$$RSWMIN(T) = RSWMIN(TNOM) + PRT \cdot (T/TNOM - 1)$$

If **TEMPMOD** = 1,

- ***rdsMod* = 0 (internal source/drain LDD resistance)**

(12.4.7)

$$RDSW(T) = RDSW(TNOM)[1 + PRT \cdot (T - TNOM)]$$

(12.4.8)

$$RDSWMIN(T) = RDSWMIN(TNOM)[1 + PRT \cdot (T - TNOM)]$$

- ***rdsMod* = 1 (external source/drain LDD resistance)**

(12.4.9)

$$RDW(T) = RDW(TNOM)[1 + PRT \cdot (T - TNOM)]$$

(12.4.10)

$$RDWMIN(T) = RDWMIN(TNOM)[1 + PRT \cdot (T - TNOM)]$$

(12.4.11)

$$RSW(T) = RSW(TNOM)[1 + PRT \cdot (T - TNOM)]$$

and

$$RSWMIN(T) = RSWMIN(TNOM)[1 + PRT \cdot (T - TNOM)] \tag{12.4.12}$$

12.5 Temperature Dependence of Junction Diode IV

- **Source-side diode**

The source-side saturation current is given by

$$I_{sbs} = A_{seff} J_{ss}(T) + P_{seff} J_{ssws}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T) \tag{12.5.1}$$

where

$$J_{ss}(T) = JSS(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTIS \cdot \ln\left(\frac{T}{TNOM}\right)}{NJS} \right) \tag{12.5.2}$$

$$J_{ssws}(T) = JSSWS(TNOM) \cdot \exp\left(\frac{\frac{E_g(TNOM)}{v_t(TNOM)} - \frac{E_g(T)}{v_t(T)} + XTIS \cdot \ln\left(\frac{T}{TNOM}\right)}{NJS} \right) \tag{12.5.3}$$

and

(12.5.4)

$$J_{sswgs}(T) = JSSWGS(TNOM)\cdot exp\left(\frac{\frac{E_g(TNOM)}{k_b\cdot TNOM} - \frac{E_g(T)}{k_b\cdot T} + XTIS\cdot ln\left(\frac{T}{TNOM}\right)}{NJS}\right)$$

where E_g is given in Section 12.7.

- **Drain-side diode**

The drain-side saturation current is given by

(12.5.5)

$$I_{sbd} = A_{deff}J_{sd}(T) + P_{deff}J_{sswd}(T) + W_{effcj}\cdot NF\cdot J_{sswgd}(T)$$

where

(12.5.6)

$$J_{sd}(T) = JSD(TNOM)\cdot exp\left(\frac{\frac{E_g(TNOM)}{k_b\cdot TNOM} - \frac{E_g(T)}{k_b\cdot T} + XTID\cdot ln\left(\frac{T}{TNOM}\right)}{NJD}\right)$$

(12.5.7)

$$J_{sswd}(T) = JSSWD(TNOM)\cdot exp\left(\frac{\frac{E_g(TNOM)}{k_b\cdot TNOM} - \frac{E_g(T)}{k_b\cdot T} + XTID\cdot ln\left(\frac{T}{TNOM}\right)}{NJD}\right)$$

and

(12.5.8)

$$J_{sswgd}(T) = JSSWGD(TNOM)\cdot exp\left(\frac{\frac{E_g(TNOM)}{k_b\cdot TNOM} - \frac{E_g(T)}{k_b\cdot T} + XTID\cdot ln\left(\frac{T}{TNOM}\right)}{NJD}\right)$$

- **trap-assisted tunneling and recombination current**

(12.5.9)

$$J_{tsswgs}(T) = J_{tsswgs}(TNOM)\cdot exp\left[\frac{-Eg(TNOM)}{k_B T}\cdot X_{tsswgs}\cdot\left(1-\frac{T}{TNOM}\right)\right]$$

(12.5.10)

$$J_{tssws}(T) = J_{tssws}(TNOM)\cdot exp\left[\frac{-Eg(TNOM)}{k_B T}\cdot X_{tssws}\cdot\left(1-\frac{T}{TNOM}\right)\right]$$

(12.5.11)

$$J_{tss}(T) = J_{tss}(TNOM)\cdot exp\left[\frac{-Eg(TNOM)}{k_B T}\cdot X_{tss}\cdot\left(1-\frac{T}{TNOM}\right)\right]$$

(12.5.12)

$$J_{tsswgd}(T) = J_{tsswgd}(TNOM)\cdot exp\left[\frac{-Eg(TNOM)}{k_B T}\cdot X_{tsswgd}\cdot\left(1-\frac{T}{TNOM}\right)\right]$$

(12.5.13)

$$J_{tsswd}(T) = J_{tsswd}(TNOM)\cdot exp\left[\frac{-Eg(TNOM)}{k_B T}\cdot X_{tsswd}\cdot\left(1-\frac{T}{TNOM}\right)\right]$$

(12.5.14)

$$J_{tsd}(T) = J_{tsd}(TNOM) \cdot exp\left[\frac{-Eg(TNOM)}{k_B T} \cdot X_{tsd} \cdot \left(1 - \frac{T}{TNOM}\right)\right]$$

(12.5.15)

$$NJTSSW(T) = NJTSSW(TNOM) \cdot \left[1 + TNJTSSW\left(\frac{T}{TNOM} - 1\right)\right]$$

(12.5.16)

$$NJTSSW(T) = NJTSSW(TNOM) \cdot \left[1 + TNJTSSW\left(\frac{T}{TNOM} - 1\right)\right]$$

(12.5.17)

$$NJTS(T) = NJTS(TNOM) \cdot \left[1 + TNTJS\left(\frac{T}{TNOM} - 1\right)\right]$$

12.6 Temperature Dependence of Junction Diode CV

- **Source-side diode**

The temperature dependences of zero-bias unit-length/area junction capacitances on the source side are modeled by

(12.6.1)

$$CJS(T) = CJS(TNOM) \cdot [1 + TCJ \cdot (T - TNOM)]$$

(12.6.2)

$$CJSWS(T) = CJSWS(TNOM) + TCJSW \cdot (T - TNOM)$$

and

$$CJSWGS(T) = CJSWGS(TNOM) \cdot [1 + TCJSWG \cdot (T - TNOM)] \tag{12.6.3}$$

The temperature dependences of the built-in potentials on the source side are modeled by

$$PBS(T) = PBS(TNOM) - TPB \cdot (T - TNOM) \tag{12.6.4}$$

$$PBSWS(T) = PBSWS(TNOM) - TPBSW \cdot (T - TNOM) \tag{12.6.5}$$

and

$$PBSWGS(T) = PBSWGS(TNOM) - TPBSWG \cdot (T - TNOM) \tag{12.6.6}$$

- **Drain-side diode**

The temperature dependences of zero-bias unit-length/area junction capacitances on the drain side are modeled by

$$CJD(T) = CJD(TNOM) \cdot [1 + TCJ \cdot (T - TNOM)] \tag{12.6.7}$$

$$CJSWD(T) = CJSWD(TNOM) + TCJSW \cdot (T - TNOM) \tag{12.6.8}$$

and

(12.6.9)

$$CJSWGD(T) = CJSWGD(TNOM)\cdot[1+TCJSWG\cdot(T-TNOM)]$$

The temperature dependences of the built-in potentials on the drain side are modeled by

(12.6.10)

$$PBD(T) = PBD(TNOM)-TPB\cdot(T-TNOM)$$

(12.6.11)

$$PBSWD(T) = PBSWD(TNOM)-TPBSW\cdot(T-TNOM)$$

and

(12.6.12)

$$PBSWGD(T) = PBSWGD(TNOM)-TPBSWG\cdot(T-TNOM)$$

12.7 Temperature Dependences of E_g and n_i

- **Energy-band gap of Si (E_g)**

The temperature dependence of E_g is modeled by

(12.7.1)

$$E_g(TNOM) = 1.16-\frac{7.02\times10^{-4}TNOM^2}{TNOM+1108}$$

and

(12.7.2)

$$E_g(T) = 1.16 - \frac{7.02\times10^{-4}T^2}{T+1108}$$

- **Intrinsic carrier concentration of Si (n_i)**

The temperature dependence of n_i is modeled by

(12.7.3)

$$n_i = 1.45e10 \cdot \frac{TNOM}{300.15} \cdot \sqrt{\frac{TNOM}{300.15}} \cdot \exp\left[21.5565981 - \frac{qE_g(TNOM)}{2\cdot k_B T}\right]$$

Chapter 13: Stress Effect Model

CMOS feature size aggressively scaling makes shallow trench isolation(STI) very popular active area isolatiohn process in advanced technologies. Recent years, strain channel materials have been employed to achieve high device performance. The mechanical stress effect induced by these process causes MOSFET performance function of the active area size(OD: oxide definition) and the location of the device in the active area. And the necessity of new models to describe the layout dependence of MOS parameters due to stress effect becomes very urgent in advance CMOS technologies.

Influence of stress on mobility has been well known since the 0.13um technology. The stress influence on saturation velocity is also experimentally demonstrated. Stress-induced enhancement or suppression of dopant diffusion during the processing is reported. Since the doping profile may be changed due to different STI sizes and stress, the threshold voltage shift and changes of other second-order effects, such as DIBL and body effect, were shown in process integration.

BSIM4 considers the influence of stress on mobility, velocity saturation, threshold voltage, body effect, and DIBL effect.

13.1Stress Effect Model Development

Experimental analysis show that there exist at least two different mechanisms within the influence of stress effect on device characteristics. The first one is mobility-related and is induced by the band structure modification. The second one is Vth-related as a result of doping profile variation. Both of them follow the same 1/LOD trend but reveal different L and W scaling. We have derived a phenomenological model based on these findings by modifying some parameters in the BSIM model. Note that the following equations have no impact on the iteration time because there are no voltage-controlled components in them.

13.1.1 Mobility-related Equations

This model introduces the first mechanism by adjusting the U0 and Vsat according to different W, L and OD shapes. Define mobility relative change due to stress effect as :

(13.1.1)

$$r_{m_{eff}} = \Delta m_{eff} / m_{effo} = (m_{eff} - m_{effo}) / m_{effo} = \frac{m_{eff}}{m_{effo}} - 1$$

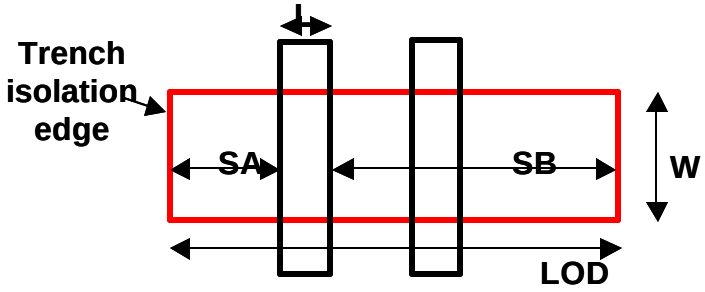
So,

(13.1.2)

$$\frac{m_{eff}}{m_{effo}} = 1 + r_{m_{eff}}$$

Figure(13.1) shows the typical layout of a MOSFET on active layout surrounded by STI isolation. SA, SB are the distances between isolation edge to Poly from one and

the other side, respectively. 2D simulation shows that stress distribution can be expressed by a simple function of SA and SB.



$$LOD = SA + SB + L$$ OD: gate Oxide Definition

Fig. (13.1) shows the typical layout of a MOSFET

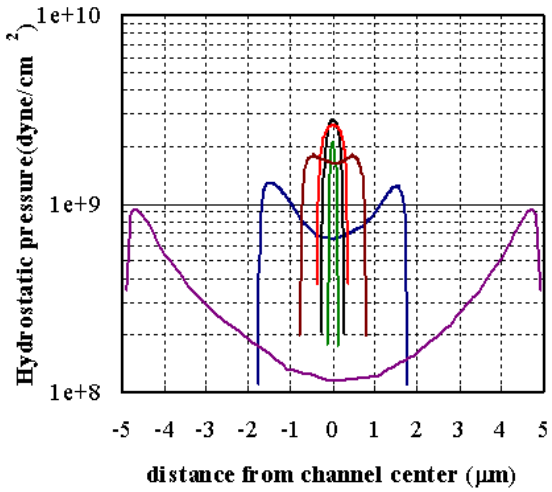


Fig. (13.2) Stress distribution within MOSFET channel using 2D simulation

Assuming that mobility relative change is propotional to stress distribution. It can be described as function of SA, SB(LOD effect), L, W, and T dependence:

(13.1.3)

$$r_{meff} = \frac{KU0}{Kstress\_u0} \cdot \left(Inv\_sa + Inv\_sb\right)$$

Where:

$$Inv\_sa = \frac{1}{SA + 0.5 \cdot L_{drawn}} \qquad Inv\_sb = \frac{1}{SB + 0.5 \cdot L_{drawn}}$$

$$Kstress\_u0 = \left(1 + \frac{LKU0}{(L_{drawn} + XL)^{LLODKU0}} + \frac{WKU0}{(W_{drawn} + XW + WLOD)^{WLODKU0}} + \frac{PKU0}{(L_{drawn} + XL)^{LLODKU0} \cdot (W_{drawn} + XW + WLOD)^{WLODKU0}}\right) \times \left(1 + TKU0 \cdot \left(\frac{Temperature}{TNOM} - 1\right)\right)$$

So that:

(13.1.4)

$$m_{eff} = \frac{1 + r_{meff}(SA, SB)}{1 + r_{meff}(SA_{ref}, SB_{ref})} m_{effo}$$

(13.1.5)

$$u_{sattemp} = \frac{1 + KVSAT \cdot r_{meff}(SA, SB)}{1 + KVSAT \cdot r_{meff}(SA_{ref}, SB_{ref})} u_{sattempo}$$

Where m_{effo} , u_{sato} are low field mobility, saturation velocity at SA_{ref}, SB_{ref}

and SAref , SBref are reference distances between OD edge to poly from one and the other side.

13.1.2 Vth-related Equations

Vth0, K2 and ETA0 are modified to cover the doping profile change in the devices with different LOD. They use the same 1/LOD formulas as shown in section(13.1.1), but different equations for W and L scaling:

$$VTH0 = VTH0_{original} + \frac{KVTH0}{Kstress\_vth0} \cdot \left(Inv\_sa + Inv\_sb - Inv\_sa_{ref} - Inv\_sb_{ref}\right) \qquad (13.1.6)$$

$$K2 = K2_{original} + \frac{STK2}{Kstress\_vth0^{LODK2}} \cdot \left(Inv\_sa + Inv\_sb - Inv\_sa_{ref} - Inv\_sb_{ref}\right) \qquad (13.1.7)$$

$$ETA0 = ETA0_{original} + \frac{STETA0}{Kstress\_vth0^{LODETA0}} \cdot \left(Inv\_sa + Inv\_sb - Inv\_sa_{ref} - Inv\_sb_{ref}\right) \qquad (13.1.8)$$

Where:

$$Inv\_sa_{ref} = \frac{1}{SA_{ref} + 0.5 \cdot L_{drawn}} \qquad Inv\_sb_{ref} = \frac{1}{SB_{ref} + 0.5 \cdot L_{drawn}}$$

$$Kstress\_vth0 = 1 + \frac{LKVTH0}{(L_{drawn} + XL)^{LLODKVTH}} + \frac{WKVTH0}{(W_{drawn} + XW + WLOD)^{WLODKVTH}} + \frac{PKVTH0}{(L_{drawn} + XL)^{LLODKVTH} \cdot (W_{drawn} + XW + WLOD)^{WLODKVTH}}$$

13.1.3 Multiple Finger Device

For multiple finger device, the total LOD effect is the average of LOD effect to every finger. That is(see Fig.(13.3) for the layout for multiple finger device):

$$Inv\_sa = \frac{1}{NF}\sum_{i=0}^{NF-1}\frac{1}{SA + 0.5\cdot L_{drawn} + i\cdot(SD + L_{drawn})}$$

$$Inv\_sb = \frac{1}{NF}\sum_{i=0}^{NF-1}\frac{1}{SB + 0.5\cdot L_{drawn} + i\cdot(SD + L_{drawn})}$$

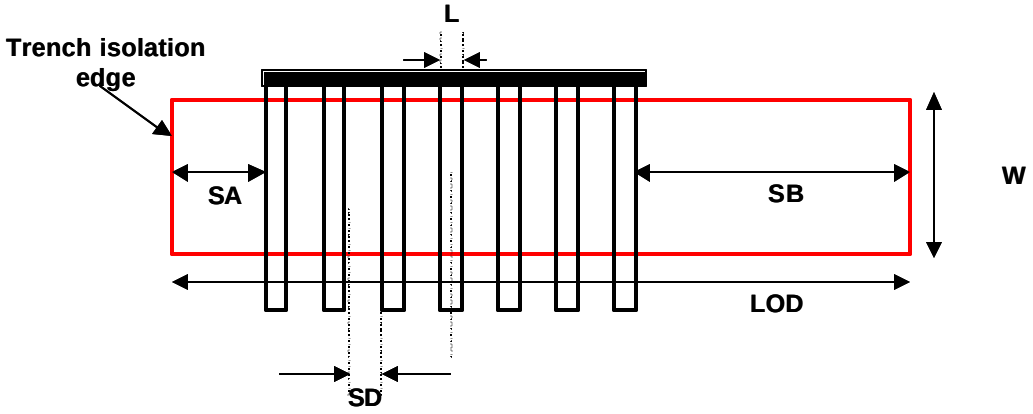


Fig. (13.3) Layout of multiple finger MOSFET

13.2 Effective SA and SB for Irregular LOD

General MOSFET has an irregular shape of active area shown in Fig.(13.4). To fully describe the shape of OD region will require additional instance parameters. However, this will result in too many parameters in the net lists and would massively increase the read-in time and degrade the readability of parameters. One way to overcome this difficulty is the concept of effective SA and SB similar to ref. [16].

Stress effect model described in Section(13.1) allows an accurate and efficient layout extraction of effective SA and SB while keeping fully compatibility of the LOD model. They are expressed as:

$$\frac{1}{SA_{eff} + 0.5 \cdot L_{drawn}} = \sum_{i=1}^{n} \frac{sw_i}{W_{drawn}} \cdot \frac{1}{sa_i + 0.5 \cdot L_{drawn}} \qquad (13.2.1)$$

$$\frac{1}{SB_{eff} + 0.5 \cdot L_{drawn}} = \sum_{i=1}^{n} \frac{sw_i}{W_{drawn}} \cdot \frac{1}{sb_i + 0.5 \cdot L_{drawn}} \qquad (13.2.2)$$

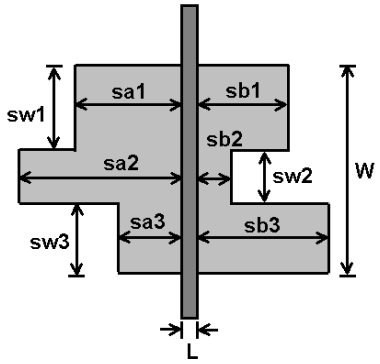


Fig.(13.4) A typical layout of MOS devices with more instance parameters (swi, sai and sbi) in addition to the traditional L and W

Chapter 14: Well Proximity Effect Model

Retrograde well profiles have several key advantages for highly scaled bulk complementary metal oxide semiconductor(CMOS) technology. With the advent of high-energy implanters and reduced thermal cycle processing, it has become possible to provide a relatively heavily doped deep nwell and pwell without affecting the critical device-related doping at the surface. The deep well implants provide a low resistance path and suppress parasitic bipolar gain for latchup protection, and can also improve soft error rate and noise isolation. A deep buried layer is also key to forming triple-well structures for isolated-well NMOSFETs. However, deep buried layers can affect devices located near the mask edge. Some of the ions scattered out of the edge of the photoresist are implanted in the silicon surface near the mask edge, altering the threshold voltage of those devices[17]. It is observed a threshold voltage shifts of up to 100 mV in a deep boron retrograde pwell, a deep phosphorus retrograde nwell, and also a triple-well implementation with a deep phosphorus isolation layer below the pwell over a lateral distance on the order of a micrometer[17]. This effect is called well proximity effect.

BSIM4 considers the influence of well proximity effect on threshold voltage, mobility, and body effect. This well proximity effect model is developed by Compact Model Council[18].

14.1 Well Proximity Effect Model

Experimental analysis[17] shows that well proximity effect is strong function of distance of FET from mask edge, and electrical quantities influenced by it follow the same geometrical trend. A phenomenological model based on these findings has been developed by modifying some parameters in the BSIM model. Note that the following equations have no impact on the iteration time because there are no voltage-controlled components in them.

14.1.1 Equations for Threshold Voltage, Body Effect, and Mobility

Due to the well proximity effect, their new equations can be described as:

(14.1.1)

$$Vth0 = Vth0_{org} + KVTH0WE \times (SCA + WEB \times SCB + WEC \times SCC)$$

$$K2 = K2_{org} + K2WE \times (SCA + WEB \times SCB + WEC \times SCC)$$

$$\mu_{eff} = \mu_{eff,org} \times (1 + KU0WE \times (SCA + WEB \times SCB + WEC \times SCC))$$

where SCA, SCB, SCC are instance parameters that represent the integral of the first/second/third distribution function for scattered well dopant.

14.2 Extraction of Instance Parameters (Preliminary for post-layout simulation)

14.2.1SCA, SCB, SCC calculation

Figure(14.1) shows the typical layout of a MOSFET with an irregular shape well surrounded by other retrograde implanted wells. The measurement for SCi and Wi and Li could be done by the projection of channel region (overlap of OD and PO).

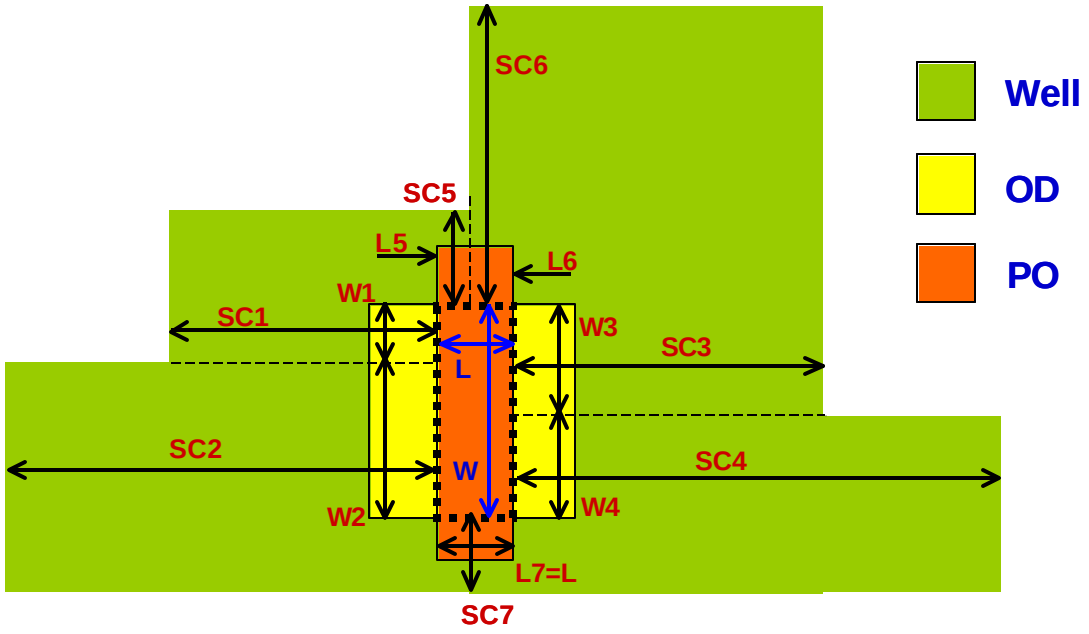


Fig. (14.1) the typical layout of a MOSFET

SCA, SCB, SCC can be calculated through:

(14.2.1)

$$SCA = \left\{ \frac{1}{W_{drawn} \times L_{drawn}} \left[\sum_{i=1}^{n} \left(W_i \times \int_{SC_i}^{SC_i + L_{drawn}} f_A(u)du \right) + \sum_{i=n+1}^{n+m} \left(L_i \times \int_{SC_i}^{SC_i + W_{drawn}} f_A(u)du \right) + corners\_A \right] \right\}$$

$$f_A(u) = \frac{SC_{ref}^{\ 2}}{u^2}$$

(14.2.2)

$$SCB = \left\{ \frac{1}{W_{drawn} \times L_{drawn}} \left[\sum_{i=1}^{n} \left(W_i \times \int_{SC_i}^{SC_i + L_{drawn}} f_B(u)du \right) + \sum_{i=n+1}^{n+m} \left(L_i \times \int_{SC_i}^{SC_i + W_{drawn}} f_B(u)du \right) + corners\_B \right] \right\}$$

$$f_B(u) = \frac{u}{SC_{ref}} \exp\left(-10 \times \frac{u}{SC_{ref}} \right)$$

(14.2.3)

$$SCC = \left\{ \frac{1}{W_{drawn} \times L_{drawn}} \left[\sum_{i=1}^{n} \left(W_i \times \int_{SC_i}^{SC_i + L_{drawn}} f_C(u)du \right) + \sum_{i=n+1}^{n+m} \left(L_i \times \int_{SC_i}^{SC_i + W_{drawn}} f_C(u)du \right) + corners\_C \right] \right\}$$

$$f_C(u) = \frac{u}{SC_{ref}} \exp\left(-20 \times \frac{u}{SC_{ref}} \right)$$

(n is the number of segments in the projection of L direction. And m is the number of segments in the project of W direction.)

The impact of scattered dopants from well corners outside the projection regions can be calculated (see Fig. 14.2) as:

(14.2.4)

$$corners\_A = \sum_{i=m+1}^{m+4} \left(\frac{L_{drawn}}{2} \times \int_{SCX_i+SCY_i}^{SCX_i+SCY_i+W_{drawn}} f_A(u)du \right) + \sum_{i=n+1}^{n+4} \left(\frac{W_{drawn}}{2} \times \int_{SCX_i+SCY_i}^{SCX_i+SCY_i+L_{drawn}} f_A(u)du \right)$$

$$corners\_B = \sum_{i=m+1}^{m+4} \left(\frac{L_{drawn}}{2} \times \int_{SCX_i+SCY_i}^{SCX_i+SCY_i+W_{drawn}} f_B(u)du \right) + \sum_{i=n+1}^{n+4} \left(\frac{W_{drawn}}{2} \times \int_{SCX_i+SCY_i}^{SCX_i+SCY_i+L_{drawn}} f_B(u)du \right)$$

$$corners\_C = \sum_{i=m+1}^{m+4} \left(\frac{L_{drawn}}{2} \times \int_{SCX_i+SCY_i}^{SCX_i+SCY_i+W_{drawn}} f_C(u)du \right) + \sum_{i=n+1}^{n+4} \left(\frac{W_{drawn}}{2} \times \int_{SCX_i+SCY_i}^{SCX_i+SCY_i+L_{drawn}} f_C(u)du \right)$$

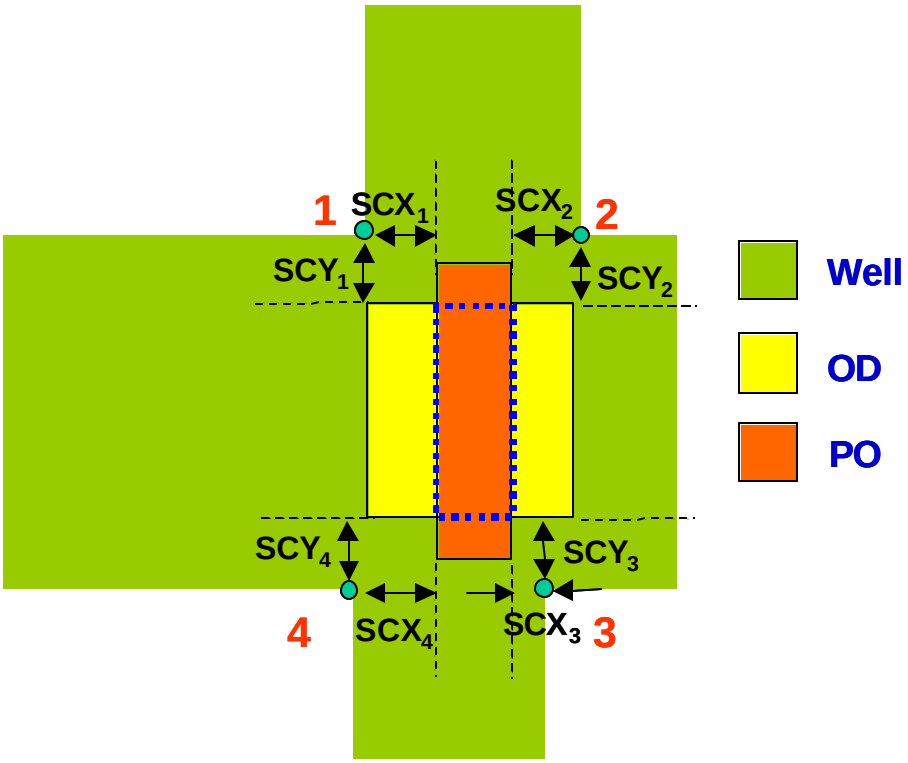


Fig. (14.2) layout for corner terms calculation

14.2.2 SC Definition (for Pre-layout Simulation)

SC is defined as “The distance to a single well edge used in calculations of SCA, SCB and SCC when layout information is not available”. If SCA, SCB and SCC are not given due to lack of detailed layout information, their estimation can be made by simulators based on the assumption that for most of layouts(Fig.14.3), the devices are close to only one well edge:

(14.2.5)

$$\mathrm{SCA} = \frac{SC_{ref}^{\,2}}{W_{drawn}} \times \left(\frac{1}{SC} - \frac{1}{SC + W_{drawn}} \right)$$

$$\mathrm{SCB} = \frac{1}{W_{drawn} \times SC_{ref}} \left(\frac{SC_{ref}}{10} \times SC \times \exp\left(-10 \times \frac{SC}{SC_{ref}} \right) + \frac{SC_{ref}^{\,2}}{100} \exp\left(-10 \times \frac{SC}{SC_{ref}} \right) - \frac{SC_{ref}}{10} \times \left(SC + W_{drawn} \right) \times \exp\left(-10 \times \frac{SC + W_{drawn}}{SC_{ref}} \right) - \frac{SC_{ref}^{\,2}}{100} \exp\left(-10 \times \frac{SC + W_{drawn}}{SC_{ref}} \right) \right)$$

$$\mathrm{SCC} = \frac{1}{W_{drawn} \times SC_{ref}} \left(\frac{SC_{ref}}{20} \times SC \times \exp\left(-20 \times \frac{SC}{SC_{ref}} \right) + \frac{SC_{ref}^{\,2}}{400} \exp\left(-20 \times \frac{SC}{SC_{ref}} \right) - \frac{SC_{ref}}{20} \times \left(SC + W_{drawn} \right) \times \exp\left(-20 \times \frac{SC + W_{drawn}}{SC_{ref}} \right) - \frac{SC_{ref}^{\,2}}{400} \exp\left(-20 \times \frac{SC + W_{drawn}}{SC_{ref}} \right) \right)$$

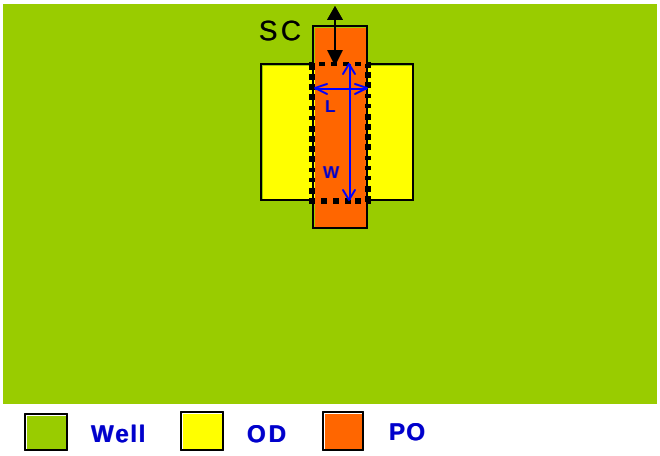


Fig. (14.3) layout for SCA, SCB, SCC estimation

For multi-finger case, still assuming there is only one well edge close to the multi-finger devices as shown in Fig. 14.4, the calculation of SCA, SCB and SCC can be (14.2.5).

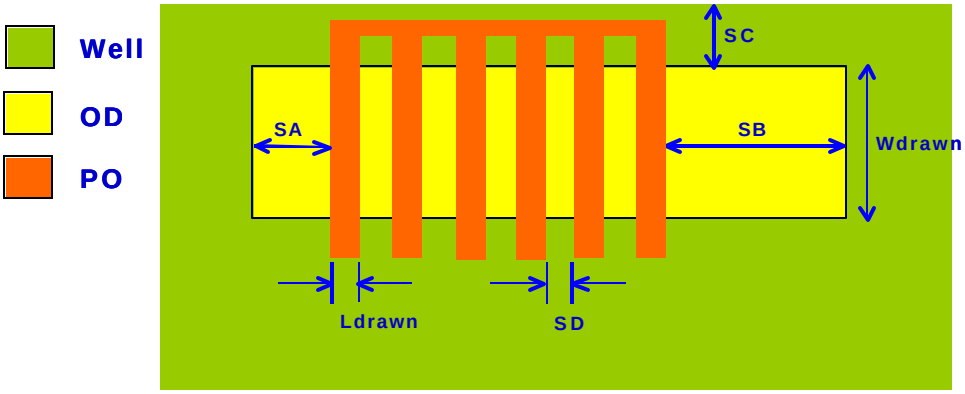


Fig. (14.4) layout for SCA, SCB, SCC estimation with multi-finger case

CHAPTER 15: Parameter Extraction Methodology

Parameter extraction is an important part of model development. The extraction methodology depends on the model and on the way the model is used. A combination of a local optimization and the group device extraction strategy is adopted for parameter extraction.

15.1 Optimization strategy

There are two main, different optimization strategies: global optimization and local optimization. Global optimization relies on the explicit use of a computer to find one set of model parameters which will best fit the available experimental (measured) data. This methodology may give the minimum average error between measured and simulated (calculated) data points, but it also treats each parameter as a "fitting" parameter. Physical parameters extracted in such a manner might yield values that are not consistent with their physical intent.

In local optimization, many parameters are extracted independently of one another. Parameters are extracted from device bias conditions which correspond to dominant physical mechanisms. Parameters which are extracted in this manner might not fit experimental data in all the bias conditions. Nonetheless, these extraction methodologies are developed specifically with respect to a given parameter’s physical meaning. If properly executed, it should, overall, predict

device performance quite well. Values extracted in this manner will now have some physical relevance.

15.2 Extraction Strategy

Two different strategies are available for extracting parameters: single device extraction strategy and group device extraction strategy. In single device extraction strategy, experimental data from a single device is used to extract a complete set of model parameters. This strategy will fit one device very well but will not fit other devices with different geometries. Furthermore, single device extraction strategy can not guarantee that the extracted parameters are physical. If only one set of channel length and width is used, parameters related to channel length and channel width dependencies can not be determined.

It is suggested that BSIM4 use group device extraction strategy. This requires measured data from devices with different geometries. All devices are measured under the same bias conditions. The resulting fit might not be absolutely perfect for any single device but will be better for the group of devices under consideration. In the following, a general extraction methodology is proposed for basic BSIM4 model parameters. Thus, it will not cover other model parameters, such as those of the gate tunneling current model and RF models, etc.

15.3 Extraction Procedure

15.3.1 Extraction Requirements

One large size device and two sets of smaller-sized devices are needed to extract parameters, as shown in Figure 13-1.

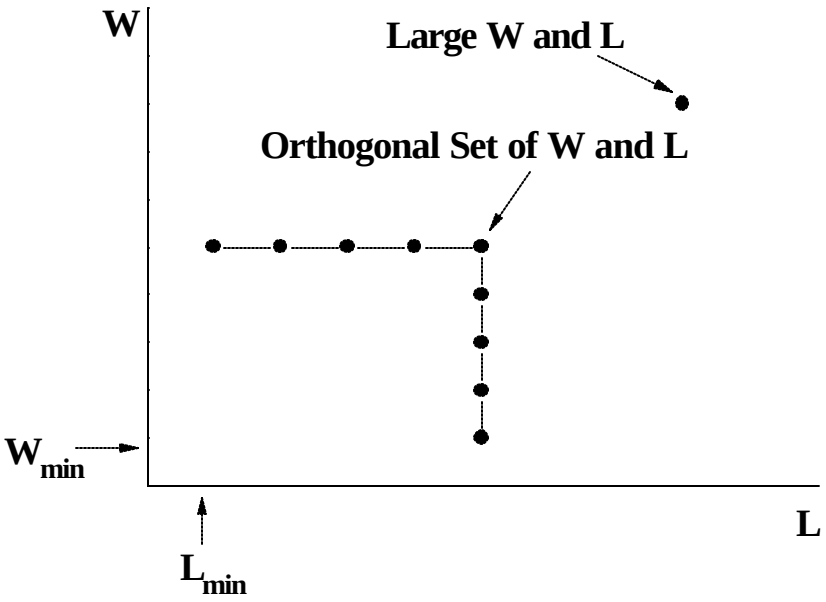


Figure 13-1. Device geometries used for parameter extraction

The large-sized device (W ≥ 10μm, L ≥ 10μm) is used to extract parameters which are independent of short/narrow channel effects and parasitic resistance. Specifically, these are: mobility, the large-sized device

threshold voltage *VTH*0, and the body effect coefficients *K*1 and *K*2 which depend on the vertical doping concentration distribution. The set of devices with a fixed large channel width but different channel lengths are used to extract parameters which are related to the short channel effects. Similarly, the set of devices with a fixed, long channel length but different channel widths are used to extract parameters which are related to narrow width effects. Regardless of device geometry, each device will have to be measured under four, distinct bias conditions.

(1) I_{ds} vs. V_{gs} @ V_{ds} = 0.05V with different V_{bs}.

(2) I_{ds} vs. V_{ds} @ V_{bs} = 0V with different V_{gs}.

(3) I_{ds} vs. V_{gs} @ V_{ds} = V_{dd} with different V_{bs}.

(4) I_{ds} vs. V_{ds} @ V_{bs} = V_{bb} with different V_{gs}. ($|V_{bb}|$ is the maximum body bias).

15.3.2 Optimization

The optimization process recommended is a combination of Newton-Raphson's iteration and linear-squares fit of either one, two, or three variables. A flow chart of this optimization process is shown in Figure 13-2. The model equation is first arranged in a form suitable for Newton-Raphson's iteration as shown in (14.3.1):

(14.3.1)

$$f_{\exp}(P_{10},P_{20},P_{30}) - f_{sim}(P_1^{(m)},P_2^{(m)},P_3^{(m)}) = \frac{\partial f_{sim}}{\partial P_1} DP_1^m + \frac{\partial f_{sim}}{\partial P_2} DP_2^m + \frac{\partial f_{sim}}{\partial P_3} DP_3^m$$

The variable $f_{sim}()$ is the objective function to be optimized. The variable $f_{exp}()$ stands for the experimental data. P_{10}, $P_{20,}$ and P_{30} represent the

desired extracted parameter values. $P_1^{(m)}$, $P_2^{(m)}$ and $P_3^{(m)}$ represent parameter values after the *m*th iteration.

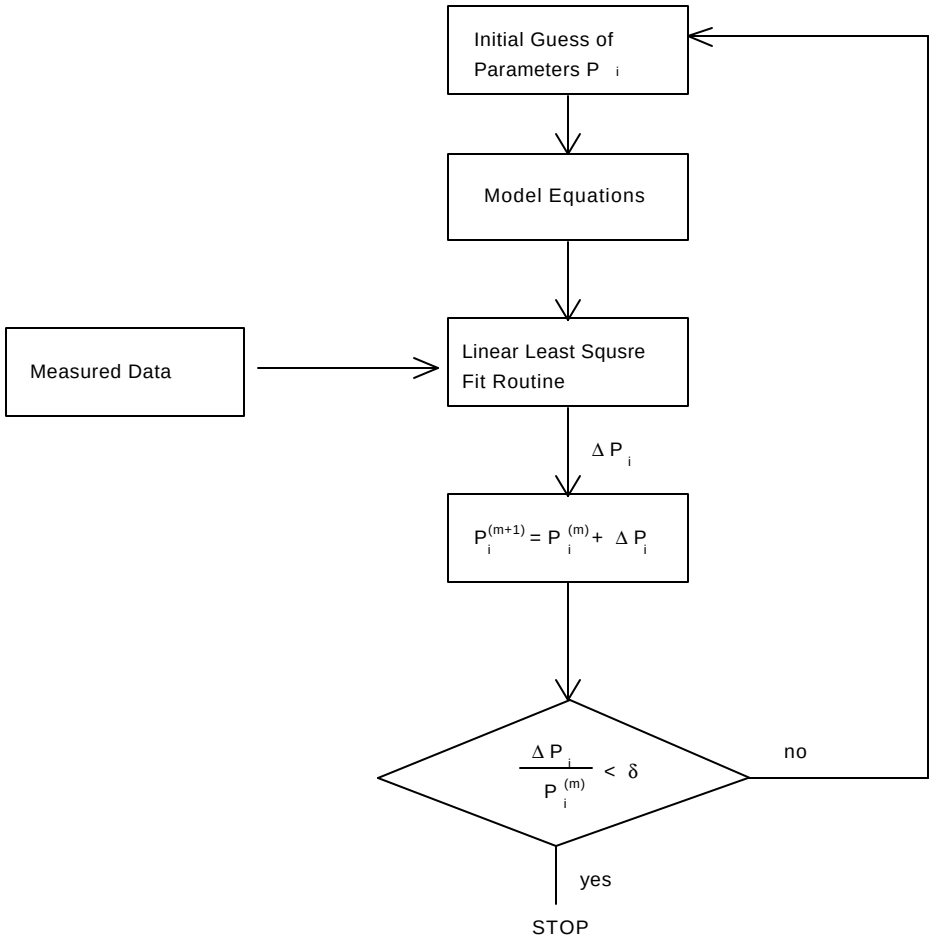


Figure 13-2. Optimization flow.

To change (14.3.1) into a form that a linear least-squares fit routine can be used (i.e. in a form of $y = a + bx_1 + cx_2$), both sides of (14.3.1) are divided

by $\partial f_{sim} / \partial P_1$. This gives the change in P_1, $\Delta P_1^{(m)}$, for the next iteration such that:

$$P_i^{(m+1)} = P_i^{(m)} + DP_i^{(m)} \tag{14.3.2}$$

where i=1, 2, 3 for this example. The (m+1) parameter values for P_2 and P_3 are obtained in an identical fashion. This process is repeated until the incremental parameter change in parameter values $\Delta P_i^{(m)}$ are smaller than a pre-determined value. At this point, the parameters P_1, P_2, and P_3 have been extracted.

15.3.3 Extraction Routine

Before any model parameters can be extracted, some process parameters have to be provided. They are listed below in Table 13-1:

Input Parameters Names	Physical Meaning
TOXE, TOXP, DTOX, or EPSROX	Gate oxide thickness and dielectric constant
NDEP	Doping concentration in the channel
TNOM	Temperature at which the data is taken
L_{drawn}	Mask level channel length
W_{drawn}	Mask level channel width
XJ	Junction depth

Table 13-1. Prerequisite input parameters prior to extraction process.

The parameters are extracted in the following procedure. These procedures are based on a physical understanding of the model and based on local optimization. (Note: *Fitting Target Data* refers to measurement data used for model extraction.)

Step 1

Extracted Parameters & Fitting Target Data	Device & Experimental Data
VTH0, K1, K2 Fitting Target Exp. Data: $V_{th}(V_{bs})$	Large Size Device (Large W & L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs} Extracted Experimental Data $V_{th}(V_{bs})$

Step 2

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
UA, UB, UC, EU Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	Large Size Device (Large W & L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 3

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

LINT, R_{ds}(RDSW, W, V_{bs}) Fitting Target Exp. Data: Strong Inversion region I_{ds}(V_{gs}, V_{bs})	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 4

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
WINT, R_{ds}(RDSW, W, V_{bs}) Fitting Target Exp. Data: Strong Inversion region I_{ds}(V_{gs}, V_{bs})	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 5

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
RDSW, PRWG, PRWB, WR Fitting Target Exp. Data: R_{ds}(RDSW, W, V_{gs}, V_{bs})	R_{ds}(RDSW, W, V_{gs}, V_{bs})

Step 6

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

DVT0, DVT1, DVT2, LPE0, LPEB Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed W & Different L). $V_{th}(V_{bs}, L, W)$

Step 7

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
DVT0W, DVT1W, DVT2W Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed L & Different W). $V_{th}(V_{bs}, L, W)$

Step 8

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
K3, K3B, W0 Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed L & Different W). $V_{th}(V_{bs}, L, W)$

Step 9

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
MINV, VOFF, VOFFL, NFACTOR, CDSC, CDSCB Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 10

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
CDSCD Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{bs} = V_{bb}$ at Different V_{ds}

Step 11

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
DWB Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 12

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
VSAT, A0, AGS, LAMBDA, XN, VTL, LC Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$ A1, A2 (PMOS Only) Fitting Target Exp. Data $V_{dsat}(V_{gs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 13

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
B0, B1 Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 14

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
DWG Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 15

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
PSCBE1, PSCBE2 Fitting Target Exp. Data: $R_{out}(V_{gs}, V_{ds})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 16

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

PCLM, θ(DROUT, PDIBLC1, PDIBLC2, *L*), PVAG, FPROUT, DITS, DITSL, DITSD Fitting Target Exp. Data: $R_{out}(V_{gs}, V_{ds})$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 17

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
DROUT, PDIBLC1, PDIBLC2 Fitting Target Exp. Data: θ(DROUT, PDIBLC1, PDIBLC2, *L*)	One Set of Devices (Large and Fixed *W* & Different *L*). θ(DROUT, PDIBLC1, PDIBLC2, *L*)

Step 18

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
PDIBLCB Fitting Target Exp. Data: θ(DROUT, PDIBLC1, PDIBLC2, *L*, V_{bs})	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{gs} @ fixed V_{gs} at Different V_{bs}

Step 19

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

θ_{DIBL}(ETA0, ETAB, DSUB, DVTP0, DVTP1, *L*) Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ at Different V_{bs}

Step 20

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
ETA0, ETAB, DSUB Fitting Target Exp. Data: θ_{DIBL}(ETA0, ETAB, *L*)	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ at Different V_{bs}

Step 21

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
KETA Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ at Different V_{gs}

Step 22

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

ALPHA0, ALPHA1, BETA0 Fitting Target Exp. Data: $I_{ii}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ at Different V_{ds}

Step 23

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
ku0, kvsat, tku0, lku0, wku0, pku0, llodku0, wlodku0 Fitting Target Exp. Data: *Mobility (SA, SB, L, W)*	Set of Devices (Different L, W, *SA*, *SB*). $I_{ds\text{-}linear}$ @ $V_{gs} = V_{dd,}$ $V_{ds} = 0.05$

Step 24

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
kvth0, lkvth0, wkvth0, pvth0, llodvth, wlodvth Fitting Target Exp. Data: V_{th}(*SA*, *SB*, *L*, *W*)	Set of Devices (Different L, W, *SA*, *SB*). V_{th}(*SA*, *SB*, *L*, *W*)

Step 24

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

stk2, lodk2, steta0, lodeta0 Fitting Target Exp. Data: *k2*(*SA, SB, L, W*), eta0(*SA, SB, L, W*)	Set of Devices (Different L, W, *SA, SB*). *k2*(*SA, SB, L, W*), eta0(*SA, SB, L, W*)

Appendix A: Complete Parameter List

A.1 BSIM4.5.0 Model Selectors/Controllers

Parameter name	Description	Default value	Binnable?	Note
LEVEL **(SPICE3 parameter)**	SPICE3 model selector	14	NA	BSIM4 also set as the default model in SPICE3
VERSION	Model version number	4.5.0	NA	Berkeley Latest official release
BINUNIT	Binning unit selector	1	NA	-
PARAMCHK	Switch for parameter value check	1	NA	Parameters checked
MOBMOD	Mobility model selector	0	NA	-
RDSMOD	Bias-dependent source/drain resistance model selector	0	NA	$R_{ds}(V)$ modeled internally through IV equation
IGCMOD	Gate-to-channel tunneling current model selector	0	NA	OFF
IGBMOD	Gate-to-substrate tunneling current model selector	0	NA	OFF
CAPMOD	Capacitance model selector	2	NA	-
RGATEMOD **(Also an instance parameter)**	Gate resistance model selector	0 (no gate resistance)		-

Parameter name	Description	Default value	Binnable?	Note
RBODYMOD **(Also an instance parameter)**	Substrate resistance network model selector	0 (network off)	NA	-
TRNQSMOD **(Also an instance parameter)**	Transient NQS model selector	0	NA	OFF
ACNQSMOD **(Also an instance parameter)**	AC small-signal NQS model selector	0	NA	OFF
FNOIMOD	Flicker noise model selector	1	NA	-
TNOIMOD	Thermal noise model selector	0	NA	-
DIOMOD	Source/drain junction diode IV model selector	1	NA	-
TEMPMOD	Temperature mode selector	0	No	If 0,original model is used If 1, new format used
PERMOD	Whether PS/PD (when given) includes the gate-edge perimeter	1 (including the gate-edge perimeter)	NA	-
GEOMOD **(Also an instance parameter)**	Geometry-dependent parasitics model selector - specifying how the end S/D diffusions are connected	0 (isolated)	NA	-
RGEOMOD **(Instance parameter only)**	Source/drain diffusion resistance and contact model selector - specifying the end S/D contact type: point, wide or merged, and how S/D parasitics resistance is computed	0 (no S/D diffusion resistance)	NA	-
WPEMOD	Flag for WPE model (WPEMOD=1 to activate this model	0	NA	-

A.2 Process Parameters

Parameter name	Description	Default value	Binnable?	Note
EPSROX	Gate dielectric constant relative to vacuum	3.9 (SiO_2)	No	Typically greater than or equal to 3.9
TOXE	Electrical gate equivalent oxide thickness	3.0e-9m	No	Fatal error if not positive
TOXP	Physical gate equivalent oxide thickness	TOXE	No	Fatal error if not positive
TOXM	Tox at which parameters are extracted	TOXE	No	Fatal error if not positive
DTOX	Defined as (TOXE-TOXP)	0.0m	No	-
XJ	S/D junction depth	1.5e-7m	Yes	-
GAMMA1 (γ1 in equation)	Body-effect coefficient near the surface	calculated	$V^{1/2}$	Note-1
GAMMA2 (γ2 in equation)	Body-effect coefficient in the bulk	calculated	$V^{1/2}$	Note-1
NDEP	Channel doping concentration at depletion edge for zero body bias	1.7e17cm^{-3}	Yes	Note-2
NSUB	Substrate doping concentration	6.0e16cm^{-3}	Yes	-
NGATE	Poly Si gate doping concentration	0.0cm^{-3}	Yes	-
NSD	Source/drain doping concentrationFatal error if not positive	1.0e20cm^{-3}	Yes	-
VBX	V_{bs} at which the depletion region width equalsXT	calculated (V)	No	Note-3
XT	Doping depth	1.55e-7m	Yes	-

Parameter name	Description	Default value	Binnable?	Note
RSH	Source/drain sheet resistance	0.0ohm/ square	No	Should not be negative
RSHG	Gate electrode sheet resistance	0.1ohm/ square	No	Shoule not be negative

A.3 Basic Model Parameters

Parameter name	Description	Default value	Binnable?	Note
VTH0 or VTHO	Long-channel threshold voltage at V_{bs}=0	0.7V (NMOS) -0.7V (PMOS)	Yes	Note-4
DELVTO (Instance parameter only)	Zero bias threshold voltage variation	0.0V	No	
VFB	Flat-band voltage	-1.0V	Yes	Note-4
PHIN	Non-uniform vertical doping effect on surface potential	0.0V	Yes	-
K1	First-order body bias coefficient	$0.5V^{1/2}$	Yes	Note-5
K2	Second-order body bias coefficient	0.0	Yes	Note-5
K3	Narrow width coefficient	80.0	Yes	-
K3B	Body effect coefficient of K3	$0.0\ V^{-1}$	Yes	-
W0	Narrow width parameter	2.5e-6m	Yes	-
LPE0	Lateral non-uniform doping parameter at V_{bs}=0	1.74e-7m	Yes	-
LPEB	Lateral non-uniform doping effect on K1	0.0m	Yes	-
VBM	Maximum applied body bias in VTH0 calculation	-3.0V	Yes	-
DVT0	First coefficient of short-channel effect on V_{th}	2.2	Yes	-
DVT1	Second coefficient of short-channel effect on V_{th}	0.53	Yes	-
DVT2	Body-bias coefficient of short-channel effect on Vth	$-0.032V^{-1}$	Yes	-
DVTP0	First coefficient of drain-induced V_{th} shift due to for long-channel pocket devices	0.0m	Yes	Not modeled if binned DVTP0 <=0.0

Parameter name	Description	Default value	Binnable?	Note
DVTP1	First coefficient of drain-induced V_{th} shift due to for long-channel pocket devices	$0.0V^{-1}$	Yes	-
DVT0W	First coefficient of narrow width effect on V_{th} for small channel length	0.0	Yes	-
DVT1W	Second coefficient of narrow width effect on V_{th} for small channel length	$5.3e6m^{-1}$	Yes	-
DVT2W	Body-bias coefficient of narrow width effect for small channel length	$-0.032V^{-1}$	Yes	-
U0	Low-field mobility	0.067 $m^2/(Vs)$ (NMOS); 0.025 $m^2/(Vs)$ PMOS	Yes	-
UA	Coefficient of first-order mobility degradation due to vertical field	1.0e-9m/V for MOBMOD =0 and 1; 1.0e-15m/V for MOBMOD =2	Yes	-
UB	Coefficient of secon-order mobility degradation due to vertical field	$1.0e\text{-}19m^2/V^2$	Yes	-
UC	Coefficient of mobility degradation due to body-bias effect	$-0.0465V^{-1}$ for MOB-MOD=1; $-0.0465e\text{-}9 m/V^2$ for MOBMOD =0 and 2	Yes	-
UD	Mobility Coulumb scattering coeffi-cient	$1E14(1/m^2)$	Yes	-

Parameter name	Description	Default value	Binnable?	Note
UP	Mobility channel length coefficient	0($1/m^2$)	Yes	-
LP	Mobility channel length exponential coefficient	1e-8(m)	Yes	-
EU	Exponent for mobility degradation of MOBMOD=2	1.67 (NMOS); 1.0 (PMOS)		-
VSAT	Saturation velocity	8.0e4m/s	Yes	-
A0	Coefficient of channel-length dependence of bulk charge effect	1.0	Yes	-
AGS	Coefficient of V_{gs} dependence of bulk charge effect	$0.0V^{-1}$	Yes	-
B0	Bulk charge effect coefficient for channel width	0.0m	Yes	-
B1	Bulk charge effect width offset	0.0m	Yes	-
KETA	Body-bias coefficient of bulk charge effect	$-0.047V^{-1}$	Yes	-
A1	First non-saturation effect parameter	$0.0V^{-1}$	Yes	-
A2	Second non-saturation factor	1.0	Yes	-
WINT	Channel-width offset parameter	0.0m	No	-
LINT	Channel-length offset parameter	0.0m	No	-
DWG	Coefficient of gate bias dependence of W_{eff}	0.0m/V	Yes	-
DWB	Coefficient of body bias dependence of W_{eff} bias dependence	$0.0m/V^{1/2}$	Yes	-
VOFF	Offset voltage in subthreshold region for large W and L	-0.08V	Yes	-
VOFFL	Channel-length dependence of VOFF	0.0mV	No	-
MINV	V_{gsteff} fitting parameter for moderate inversion condition	0.0	Yes	-
NFACTOR	Subthreshold swing factor	1.0	Yes	-

Parameter name	Description	Default value	Binnable?	Note
ETA0	DIBL coefficient in subthreshold region	0.08	Yes	-
ETAB	Body-bias coefficient for the sub-threshold DIBL effect	$-0.07V^{-1}$	Yes	-
DSUB	DIBL coefficient exponent in sub-threshold region	DROUT	Yes	-
CIT	Interface trap capacitance	$0.0F/m^2$	Yes	-
CDSC	coupling capacitance between source/ drain and channel	$2.4e-4F/m^2$	Yes	-
CDSCB	Body-bias sensitivity of Cdsc	$0.0F/(Vm^2)$	Yes	-
CDSCD	Drain-bias sensitivity of CDSC	$0.0(F/Vm^2)$	Yes	-
PCLM	Channel length modulation parameter	1.3	Yes	-
PDIBLC1	Parameter for DIBL effect on Rout	0.39	Yes	-
PDIBLC2	Parameter for DIBL effect on Rout	0.0086	Yes	-
PDIBLCB	Body bias coefficient of DIBL effect on Rout	$0.0V^{-1}$	Yes	-
DROUT	Channel-length dependence of DIBL effect on Rout	0.56	Yes	-
PSCBE1	First substrate current induced body-effect parameter	4.24e8V/m	Yes	-
PSCBE2	Second substrate current induced body-effect parameter	1.0e-5m/V	Yes	-
PVAG	Gate-bias dependence of Early voltage	0.0	Yes	-
DELTA (δ in equation)	Parameter for DC V_{dseff}	0.01V	Yes	-
FPROUT	Effect of pocket implant on Rout degradation	$0.0V/m^{0.5}$	Yes	Not modeled if binned FPROUT not positive

Parameter name	Description	Default value	Binnable?	Note
PDITS	Impact of drain-induced V_{th} shift on Rout	$0.0V^{-1}$	Yes	Not modeled if binned PDITS=0; Fatal error if binned PDITS negative
PDITSL	Channel-length dependence of drain-induced V_{th} shift for Rout	$0.0m^{-1}$	No	Fatal error if PDITSL negative
PDITSD	V_{ds} dependence of drain-induced V_{th} shift for Rout	$0.0V^{-1}$	Yes	-
LAMBDA	Velocity overshoot coefficient	0.0	Yes	If not given or (<=0.0), velocity overshoot will be turned off
VTL	Thermal velocity	2.05e5[m/s]	Yes	If not given or (<=0.0), source end thermal velocity will be turned off
LC	Velocity back scattering coefficient	0.0[m]	No	5e9[m] at room temperature
XN	Velocity back scattering coefficient	3.0	Yes	-

A.4 Parameters for Asymmetric and Bias-Dependent R_{ds} Model

Parameter name	Description	Default value	Binnable?	Note
RDSW	Zero bias LDD resistance per unit width for RDSMOD=0	200.0 ohm(μm)^{WR}	Yes	If negative, reset to 0.0
RDSWMIN	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0	0.0 ohm(μm)^{WR}	No	-
RDW	Zero bias lightly-doped drain resistance $R_d(V)$ per unit width for RDSMOD=1	100.0 ohm(μm)^{WR}	Yes	-
RDWMIN	Lightly-doped drain resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1	0.0 ohm(μm)^{WR}	No	-
RSW	Zero bias lightly-doped source resistance $R_s(V)$ per unit width for RDSMOD=1	100.0 ohm(μm)^{WR}	Yes	-
RSWMIN	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1	0.0 ohm(μm)^{WR}	No	-
PRWG	Gate-bias dependence of LDD resistance	1.0V^{-1}	Yes	-
PRWB	Body-bias dependence of LDD resistance	0.0V$^{-0.5}$	Yes	-
WR	Channel-width dependence parameter of LDD resistance	1.0	Yes	-
NRS **(instance parameter only)**	Number of source diffusion squares	1.0	No	-
NRD **(instance parameter only)**	Number of drain diffusion squares	1.0	No	-

A.5 Impact Ionization Current Model Parameters

Parameter name	Description	Default value	Binnable?	Note
ALPHA0	First parameter of impact ionization current	0.0m/V	Yes	-
BETA0	First Vds dependent parameter of impact ionization current	0.0/V	Yes	-
BETA1	Second Vds dependent parameter of impact ionization current	0.0	Yes	-
BETA2	Third Vds dependent parameter of impact ionization current	0.1V	Yes	-
VDSATII0	Nominal drain saturation voltage at threshold for impact ionization current	0.9V	Yes	-
TII	Temperature dependent parameter for impact ionization current	0.0	Yes	-
LII	Channel length dependent parameter at threshold for impact ionization current	0.0	Yes	-
ESATII	Saturation channel electric field for impact ionization current	1E7/m	Yes	-
SII0	First Vgs dependent parameter for impact ionization current	0.5/V	Yes	-
SII1	Second Vgs dependent parameter for impact ionization current	0.1/V	Yes	-
SII2	Third Vgs dependent parameter for impact ionization current	0.0	Yes	-
SIID	Vds dependent parameter of drain saturation voltage for impact ionization current	0.0/V	Yes	-

A.6 Gate-Induced Drain Leakage Model Parameters

Parameter name	Description	Default value	Binnable?	Note
AGIDL	Pre-exponential coefficient for GIDL	0.0mho	Yes	I_{gidl}=0.0 if binned AGIDL =0.0
BGIDL	Exponential coefficient for GIDL	2.3e9V/m	Yes	I_{gidl}=0.0 if binned BGIDL =0.0
CGIDL	Paramter for body-bias effect on GIDL	$0.5V^3$	Yes	-
EGIDL	Fitting parameter for band bending for GIDL	0.8V	Yes	-

A.7 Gate Dielectric Tunneling Current Model Parameters

Parameter name	Description	Default value	Binnable?	Note
AIGBACC	Parameter for I_{gb} in accumulation	9.49e-4 $(Fs^2/g)^{0.5}m^{-1}$	Yes	-
BIGBACC	Parameter for I_{gb} in accumulation	1.71e-3 $(Fs^2/g)^{0.5}$ $m^{-1}V^{-1}$	Yes	-
CIGBACC	Parameter for I_{gb} in accumulation	$0.075V^{-1}$	Yes	-
NIGBACC	Parameter for I_{gb} in accumulation	1.0	Yes	Fatal error if binned value not positive
AIGBINV	Parameter for I_{gb} in inversion	1.11e-2 $(Fs^2/g)^{0.5}m^{-1}$	Yes	-
BIGBINV	Parameter for I_{gb} in inversion	9.49e-4 $(Fs^2/g)^{0.5}$ $m^{-1}V^{-1}$	Yes	-
CIGBINV	Parameter for I_{gb} in inversion	$0.006V^{-1}$	Yes	-
EIGBINV	Parameter for I_{gb} in inversion	1.1V	Yes	-
NIGBINV	Parameter for I_{gb} in inversion	3.0	Yes	Fatal error if binned value not positive
AIGC	Parameter for I_{gcs} and I_{gcd}	1.36e-2 (NMOS) and 9.8e-3 (PMOS) $(Fs^2/g)^{0.5}m^{-1}$	Yes	-

Parameter name	Description	Default value	Binnable?	Note
BIGC	Parameter for I_{gcs} and I_{gcd}	1.71e-3 (NMOS) and 7.59e-4 (PMOS) $(Fs^2/g)^{0.5} m^{-1}V^{-1}$	Yes	-
CIGC	Parameter for I_{gcs} and I_{gcd}	0.075 (NMOS) and 0.03 (PMOS) V^{-1}	Yes	-
AIGSD	Parameter for I_{gs} and I_{gd}	1.36e-2 (NMOS) and 9.8e-3 (PMOS) $(Fs^2/g)^{0.5}m^{-1}$	Yes	-
BIGSD	Parameter for I_{gs} and I_{gd}	1.71e-3 (NMOS) and 7.59e-4 (PMOS) $(Fs^2/g)^{0.5} m^{-1}V^{-1}$	Yes	-
CIGSD	Parameter for I_{gs} and I_{gd}	0.075 (NMOS) and 0.03 (PMOS) V^{-1}	Yes	-
DLCIG	Source/drain overlap length for I_{gs} and I_{gd}	LINT	Yes	-
NIGC	Parameter for I_{gcs}, I_{gcd} ,I_{gs} and I_{gd}	1.0	Yes	Fatal error if binned value not positive
POXEDGE	Factor for the gate oxide thickness in source/drain overlap regions	1.0	Yes	Fatal error if binned value not positive

Parameter name	Description	Default value	Binnable?	Note
PIGCD	V_{ds} dependence of I_{gcs} and I_{gcd}	1.0	Yes	Fatal error if binned value not positive
NTOX	Exponent for the gate oxide ratio	1.0	Yes	-
TOXREF	Nominal gate oxide thickness for gate dielectric tunneling current model only	3.0e-9m	No	Fatal error if not positive
VFBSDOFF	Flatband Voltage Offset Parameter	0.0V	Yes	-

A.8 Charge and Capacitance Model Parameters

Parameter name	Description	Default value	Binnable?	Note
XPART	Charge partition parameter	0.0	No	-
CGSO	Non LDD region source-gate overlap capacitance per unit channel width	calculated (F/m)	No	Note-6
CGDO	Non LDD region drain-gate overlap capacitance per unit channel width	calculated (F/m)	No	Note-6
CGBO	Gate-bulk overlap capacitance per unit channel length	0.0	F/m	Note-6
CGSL	Overlap capacitance between gate and lightly-doped source region	0.0F/m	Yes	-
CGDL	Overlap capacitance between gate and lightly-doped source region	0.0F/m	Yes	-
CKAPPAS	Coefficient of bias-dependent overlap capacitance for the source side	0.6V	Yes	-
CKAPPAD	Coefficient of bias-dependent overlap capacitance for the drain side	CKAPPAS	Yes	-
CF	Fringing field capacitance	calculated (F/m)	Yes	Note-7
CLC	Constant term for the short channel model	1.0e-7m	Yes	-
CLE	Exponential term for the short channel model	0.6	Yes	-
DLC	Channel-length offset parameter for CV model	LINT (m)	No	-
DWC	Channel-width offset parameter for CV model	WINT (m)	No	-
VFBCV	Flat-band voltage parameter (for CAPMOD=0 only)	-1.0V	Yes	-
NOFF	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion	1.0	Yes	-
VOFFCV	CV parameter in $V_{gsteff,CV}$ for week to strong inversion	0.0V	Yes	-

Parameter name	Description	Default value	Binnable?	Note
ACDE	Exponential coefficient for charge thickness in CAPMOD=2 for accumulation and depletion regions	1.0m/V	Yes	-
MOIN	Coefficient for the gate-bias dependent surface potential	15.0	Yes	-

A.9 High-Speed/RF Model Parameters

Parameter name	Description	Default value	Binnable?	Note
XRCRG1	Parameter for distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models	12.0	Yes	Warning message issued if binned XRCRG1 <=0.0
XRCRG2	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models	1.0	Yes	-
RBPB **(Also an instance parameter)**	Resistance connected between bNodePrime and bNode	50.0ohm	No	If less than 1.0e-3ohm, reset to 1.0e-3ohm
RBPD **(Also an instance parameter)**	Resistance connected between bNodePrime and dbNode	50.0ohm	No	If less than 1.0e-3ohm, reset to 1.0e-3ohm
RBPS **(Also an instance parameter)**	Resistance connected between bNodePrime and sbNode	50.0ohm	No	If less than 1.0e-3ohm, reset to 1.0e-3ohm
RBDB **(Also an instance parameter)**	Resistance connected between dbNode and bNode	50.0ohm	No	If less than 1.0e-3ohm, reset to 1.0e-3ohm
RBSB **(Also an instance parameter)**	Resistance connected between sbNode and bNode	50.0ohm	No	If less than 1.0e-3ohm, reset to 1.0e-3ohm
GBMIN	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to unreasonably too large a substrate resistance	1.0e-12mho	No	Warning message issued if less than 1.0e-20 mho

Parameter name	Description	Default value	Binnable?	Note
RBPS0	Scaling prefactor for RBPS	50 Ohms	No	
RBPSL	Length Scaling parameter for RBPS	0.0	No	
RBPSW	Width Scaling parameter for RBPS	0.0	No	
RBPSNF	Number of fingers Scaling parameter for RBPS	0.0	No	
RBPD0	Scaling prefactor for RBPD	50 Ohms	No	
RBPDL	Length Scaling parameter for RBPD	0.0	No	
RBPDW	Width Scaling parameter for RBPD	0.0	No	
RBPDNF	Number of fingers Scaling parameter for RBPD	0.0	No	
RBPBX0	Scaling prefactor for RBPBX	100 Ohms	No	
RBPBXL	Length Scaling parameter forRBPBX	0.0	No	
RBPBXW	Width Scaling parameter for RBPBX	0.0	No	
RBPBXNF	Number of fingers Scaling parameter for RBPBX	0.0	No	
RBPBY0	Scaling prefactor for RBPBY	100 Ohms	No	
RBPBYL	Length Scaling parameter forRBPBY	0.0	No	
RBPBYW	Width Scaling parameter for RBPBY	0.0	No	
RBPBYNF	Number of fingers Scaling parameter for RBPBY	0.0	No	
RBSBX0	Scaling prefactor for RBSBX	100 Ohms	No	
RBSBY0	Scaling prefactor for RBSBY	100 Ohms	No	
RBDBX0	Scaling prefactor for RBDBX	100 Ohms	No	
RBDBY0	Scaling prefactor for RBDBY	100 Ohms	No	
RBSDBXL	Length Scaling parameter for RBSBX and RBDBX	0.0	No	
RBSDBXW	Width Scaling parameter for RBSBX and RBDBX	0.0	No	
RBSDBXNF	Number of fingers Scaling parameter for RBSBX and RBDBX	0.0	No	
RBSDBYL	Length Scaling parameter for RBSBY and RBDBY	0.0	No	
RBSDBYW	Width Scaling parameter for RBSBY and RBDBY	0.0	No	
RBSDBYNF	Number of fingers Scaling parameter for RBSBY and RBDBY	0.0	No	

A.10 Flicker and Thermal Noise Model Parameters

Parameter name	Description	Default value	Binnable?	Note
NOIA	Flicker noise parameter A	6.25e41 $(eV)^{-1}s^{1-EF}m^{-3}$ for NMOS; 6.188e40 $(eV)^{-1}s^{1-EF}m^{-3}$ for PMOS	No	-
NOIB	Flicker noise parameter B	3.125e26 $(eV)^{-1}s^{1-EF}m^{-1}$ for NMOS; 1.5e25 $(eV)^{-1}s^{1-EF}m^{-1}$ for PMOS	No	-
NOIC	Flicker noise parameter C	8.75 $(eV)^{-1}s^{1-EF}m$	No	-
EM	Saturation field	4.1e7V/m	No	-
AF	Flicker noise exponent	1.0	No	-
EF	Flicker noise frequency exponent	1.0	No	-
KF	Flicker noise coefficient	0.0 $A^{2-EF}s^{1-EF}F$	No	-
LINTNOI	Length Reduction Parameter Offset	0.0 m	No	-
NTNOI	Noise factor for short-channel devices for TNOIMOD=0 only	1.0	No	-
TNOIA	Coefficient of channel-length dependence of total channel thermal noise	1.5E6	No	-

Parameter name	Description	Default value	Binnable?	Note
TNOIB	Channel-length dependence parameter for channel thermal noise partitioning	3.5E6	No	-
RNOIA	Thermal Noise Coefficient	0.577	No	-
RNOIB	Thermal Noise Coefficient	0.37	No	-

A.11 Layout-Dependent Parasitics Model Parameters

Parameter name	Description	Default value	Binnable?	Note
DMCG	Distance from S/D contact center to the gate edge	0.0m	No	-
DMCI	Distance from S/D contact center to the isolation edge in the channel-length direction	DMCG	No	-
DMDG	Same as DMCG but for merged device only	0.0m	No	-
DMCGT	DMCG of test structures	0.0m	No	-
NF **(instance parameter only)**	Number of device fingers	1	No	Fatal error if less than one
DWJ	Offset of the S/D junction width	DWC (in CVmodel)	No	-
MIN **(instance parameter only)**	Whether to minimize the number of drain or source diffusions for even-number fingered device	0 (minimize the drain diffusion number)	No	-
XGW**(Also an instance parameter)**	Distance from the gate contact to the channel edge	0.0m	No	-
XGL	Offset of the gate length due to variations in patterning	0.0m	No	-
XL	Channel length offset due to mask/etch effect	0.0m	No	-

Parameter name	Description	Default value	Binnable?	Note
XW	Channel width offset due to mask/etch effect	0.0m	No	-
NGCON**(Also an instance parameter)**	Number of gate contacts	1	No	Fatal error if less than one; if not equal to 1 or 2, warning message issued and reset to 1

A.12 Asymmetric Source/Drain Junction Diode Model Parameters

Parameter name (separate for source and drain side as indicated in the names)	**Description**	**Default value**	**Binnable?**	**Note**
IJTHSREV IJTHDREV	Limiting current in reverse bias region	IJTHSREV =0.1A IJTHDREV =IJTHSREV	No	If not positive, reset to 0.1A
IJTHSFWD IJTHDFWD	Limiting current in forward bias region	IJTHSFWD =0.1A IJTHDFWD =IJTHS-FWD	No	If not positive, reset to 0.1A
XJBVS XJBVD	Fitting parameter for diode breakdown	XJBVS=1.0 XJBVD =XJBVS	No	Note-8
BVS BVD	Breakdown voltage	BVS=10.0V BVD=BVS	No	If not positive, reset to 10.0V
JSS JSD	Bottom junction reverse saturation current density	JSS= 1.0e-4A/m^2 JSD=JSS	No	-
JSWS JSWD	Isolation-edge sidewall reverse saturation current density	JSWS =0.0A/m JSWD =JSWS	No	-

Parameter name (separate for source and drain side as indicated in the names)	**Description**	**Default value**	**Binnable?**	**Note**
JSWGS JSWGD	Gate-edge sidewall reverse saturation current density	JSWGS =0.0A/m JSWGD =JSWGS	No	-
JTSS JTSD	Bottom trap-assisted saturation current density	JTSS =0.0A/m JTSD =JTSS	No	-
JTSSWS JTSSWD	STI sidewall trap-assisted saturation current density	JTSSWS =0.0A/m^2 JTSSWD =JTSSWS	No	-
JTSSWGS JTSSWGD	Gate-edge sidewall trap-assisted saturation current density	JTSSWGS =0.0A/m JTSSWGD =JTSSWGS	No	-
NJTS	Non-ideality factor for JTSS, JTSD	NJTS=20.0	No	-
NJTSSW	Non-ideality factor for JTSSWS, JTSSWD	NJTSSW=20.0	No	-
NJTSSWG	Non-ideality factor forJTSSWGS, JTSSWGD	NJTSSWG=20.0	No	-
XTSS, XTSD	Power dependence of JTSS, JTSD on temperature	XTSS=0.02 XTSD=0.02	No	-
XTSSWS, XTSSWD	Power dependence of JTSSWS, JTSSWD on temperature	XTSSWS=0.02 XTSSWD=0.02	No	-

Parameter name (separate for source and drain side as indicated in the names)	**Description**	**Default value**	**Binnable?**	**Note**
XTSSWGS, XTSSWGD	Power dependence of JTSSWGS, JTSSWGD on temperature	XTSSWGS=0.02 XTSSWGD=0.02	No	-
VTSS VTSD	Bottom trap-assisted voltage dependent parameter	VTSS =10V VTSD =VTSS	No	-
VTSSWS VTSSWD	STI sidewall trap-assisted voltage dependent parameter	VTSSWS =10V VTSSWD =VTSSWS	No	-
VTSSWGS VTSSWGD	Gate-edge sidewall trap-assisted voltage dependent parameter	VTSSWGS =10V VTSSWGD =VTSSWGS	No	-
TNJTS	Temperature coefficient for NJTS	TNJTS=0.0	No	-
TNJTSSW	Temperature coefficient for NJTSSW	TNJTSSW=0.0	No	-
TNJTSSWG	Temperature coefficient for NJTSSWG	TNJTSSWG=0.0	No	-
CJS CJD	Bottom junction capacitance per unit area at zero bias	CJS=5.0e-4 F/m^2 CJD=CJS	No	-
MJS MJD	Bottom junction capacitance grating coefficient	MJS=0.5 MJD=MJS	No	-

Parameter name (separate for source and drain side as indicated in the names)	**Description**	**Default value**	**Binnable?**	**Note**
MJSWS MJSWD	Isolation-edge sidewall junction capacitance grading coefficient	MJSWS =0.33 MJSWD =MJSWS	No	-
CJSWS CJSWD	Isolation-edge sidewall junction capacitance per unit area	CJSWS= 5.0e-10 F/m CJSWD =CJSWS	No	-
CJSWGS CJSWGD	Gate-edge sidewall junction capacitance per unit length	CJSWGS =CJSWS CJSWGD =CJSWS	No	-
MJSWGS MJSWGD	Gate-edge sidewall junction capacitance grading coefficient	MJSWGS =MJSWS MJSWGD =MJSWS	No	-
PB	Bottom junction built-in potential	PBS=1.0V PBD=PBS	No	-

Parameter name (separate for source and drain side as indicated in the names)	**Description**	**Default value**	**Binnable?**	**Note**
PBSWS PBSWD	Isolation-edge sidewall junction built-in potential	PBSWS =1.0V PBSWD =PBSWS	No	-
PBSWGS PBSWGD	Gate-edge sidewall junction built-in potential	PBSWGS =PBSWS PBSWGD =PBSWS	No	-

A.13 Temperature Dependence Parameters

Parameter name	Description	Default value	Binnable?	Note
TNOM	Temperature at which parameters are extracted	27°C	No	-
UTE	Mobility temperature exponent	-1.5	Yes	-
KT1	Temperature coefficient for threshold voltage	-0.11V	Yes	-
KT1L	Channel length dependence of the temperature coefficient for threshold voltage	0.0Vm	Yes	-
KT2	Body-bias coefficient of Vth temperature effect	0.022	Yes	-
UA1	Temperature coefficient for UA	1.0e-9m/V	Yes	-
UB1	Temperature coefficient for UB	-1.0e-18 $(m/V)^2$	Yes	-
UC1	Temperature coefficient for UC	0.056V^{-1} for MOBMOD=1; 0.056e-9m/V^2 for MOBMOD=0 and 2	Yes	-
UD1	Temperature coefficient for UD	0.0$(1/m)^2$	Yes	-
AT	Temperature coefficient for saturation velocity	3.3e4m/s	Yes	-
PRT	Temperature coefficient for Rdsw	0.0ohm-m	Yes	-
NJS, NJD	Emission coefficients of junction for source and drain junctions, respectively	NJS=1.0; NJD=NJS	No	-

Parameter name	Description	Default value	Binnable?	Note
XTIS, XTID	Junction current temperature exponents for source and drain junctions, respectively	XTIS=3.0; XTID=XTIS	No	-
TPB	Temperature coefficient of PB	0.0V/K	No	-
TPBSW	Temperature coefficient of PBSW	0.0V/K	No	-
TPBSWG	Temperature coefficient of PBSWG	0.0V/K	No	-
TCJ	Temperature coefficient of CJ	$0.0K^{-1}$	No	-
TCJSW	Temperature coefficient of CJSW	$0.0K^{-1}$	No	-
TCJSWG	Temperature coefficient of CJSWG	$0.0K^{-1}$	No	-
TVOFF	Temperature coefficient of VOFF	$0.0K^{-1}$	No	-
TVFBSDOFF	Temperature coefficient of VFBSDOFF	$0.0K^{-1}$	No	-

A.14 Stress Effect Model Parameters

Parameter name	Description	Default value	Binnable?	Note
SA (**Instance Parameter)**	Distance between OD edge to Poly from one side	0.0		If not given or(<=0), stress effect will be turned off
SB (**Instance Parameter)**	Distance between OD edge to Poly from other side	0.0		If not given or(<=0), stress effect will be turned off
SD (**Instance Parameter)**	Distance between neighbouring fingers	0.0		For NF>1 :If not given or(<=0), stress effect will be turned off
SAref	Reference distance between OD and edge to poly of one side	1E-06[m]	No	>0.0
SBref	Reference distance between OD and edge to poly of the other side	1E-06[m]	No	>0.0
WLOD	Width parameter for stress effect	0.0[m]	No	-
KU0	Mobility degradation/enhancement coefficient for stress effect	0.0[m]	No	-
KVSAT	Saturation velocity degradation/ enhancement parameter for stress effect	0.0[m]	No	-1<=kvsat <=1
TKU0	Temperature coefficient of KU0	0.0	No	-

Parameter name	Description	Default value	Binnable?	Note
LKU0	Length dependence of ku0	0.0	No	-
WKU0	Width dependence of ku0	0.0	No	-
LLODKU0	Length parameter for u0 stress effect	0.0	No	>0
WLODKU0	Width parameter for u0 stress effect	0.0	No	>0
KVTH0	Threshold shift parameter for stress effect	0.0[Vm]	No	-
LKVTH0	Length dependence of kvth0	0.0	No	-
WKVTH0	Width dependence of kvth0	0.0	No	-
PKVTH0	Cross-term dependence of kvth0	0.0	No	-
LLODVTH	Length parameter for Vth stress effect	0.0	No	>0
WLODVTH	Width parameter for Vth stress effect	0.0	No	>0
STK2	K2 shift factor related to Vth0 change	0.0[m]	No	
LODK2	K2 shift modification factor for stress effect	1.0	No	>0
STETA0	eta0 shift factor related to Vth0 change	0.0[m]	No	
LODETA0	eta0 shift modification factor for stress effect	1.0	No	>0

A.15 Well-Proximity Effect Model Parameters

Parameter name	Description	Default value	Binnable?	Note
SCA (**Instance Parameter)**	Integral of the first distribution function for scattered well dopant	0.0	no	If not given , calculated
SCB (**Instance Parameter)**	Integral of the second distribution function for scattered well dopant	0.0	no	If not given , calculated
SCC (**Instance Parameter)**	Integral of the third distribution function for scattered well dopant	0.0	no	If not given , calculated
SC (**Instance Parameter)**	Distance to a single well edge	0.0[m]	no	If not given or <=0.0, turn off WPE
WEB	Coefficient for SCB	0.0	No	>0.0
WEC	Coefficient for SCC	0.0	No	>0.0
KVTH0WE	Threshold shift factor for well proximity effect	0.0	Yes	-
K2WE	K2 shift factor for well proximity effect	0.0	Yes	-
KU0WE	Mobility degradation factor for well proximity effect	0.0	Yes	-
SCREF	Reference distance to calculate SCA, SCB and SCC	1e-6[m]	No	>0

A.16 *dW* and *dL* Parameters

Parameter name	Description	Default name	Binnable?	Note
WL	Coefficient of length dependence for width offset	$0.0m^{WLN}$	No	-
WLN	Power of length dependence of width offset	1.0	No	-
WW	Coefficient of width dependence for width offset	$0.0m^{WWN}$	No	-
WWN	Power of width dependence of width offset	1.0	No	-
WWL	Coefficient of length and width cross term dependence for width offset	$0.0\ m^{WWN+WLN}$	No	-
LL	Coefficient of length dependence for length offset	$0.0m^{LLN}$	No	-
LLN	Power of length dependence for length offset	1.0	No	-
LW	Coefficient of width dependence for length offset	$0.0m^{LWN}$	No	-
LWN	Power of width dependence for length offset	1.0	No	-
LWL	Coefficient of length and width cross term dependence for length offset	$0.0\ m^{LWN+LLN}$	No	-
LLC	Coefficient of length dependence for CV channel length offset	LL	No	-
LWC	Coefficient of width dependence for CV channel length offset	LW	No	-
LWLC	Coefficient of length and width cross-term dependence for CV channel length offset	LWL	No	-
WLC	Coefficient of length dependence for CV channel width offset	WL	No	-

Parameter name	Descrition	Default name	Binnable?	Note
WWC	Coefficient of width dependence for CV channel width offset	WW	No	-
WWLC	Coefficient of length and width cross-term dependence for CV channel width offset	WWL	No	-

A.17 Range Parameters for Model Application

Parameter name	Description	Default value	Binnable?	Note
LMIN	Minimum channel length	0.0m	No	-
LMAX	Maximum channel length	1.0m	No	-
WMIN	Minimum channel width	0.0m	No	-
WMAX	Maximum channel width	1.0m	No	-

A.18 Notes 1-8

Note-1: If γ_1 is not given, it is calculated by

$$g_1 = \frac{\sqrt{2qe_{si}NDEP}}{C_{oxe}}$$

If γ_2 is not given, it is calculated by

$$g_2 = \frac{\sqrt{2qe_{si}NSUB}}{C_{oxe}}$$

Note-2: If *NDEP* is not given and γ_1 is given, *NDEP* is calculated from

$$NDEP = \frac{g_1^2 C_{oxe}^2}{2qe_{si}}$$

If both γ_1 and *NDEP* are not given, *NDEP* defaults to 1.7e17cm^{-3} and γ_1 is calculated from *NDEP*.

Note-3: If *VBX* is not given, it is calculated by

$$\frac{qNDEP \cdot XT^2}{2e_{si}} = \Phi_s - VBX$$

Note-4: If *VTH*0 is not given, it is calculated by

$$VTH0 = VFB + \Phi_s + K1\sqrt{\Phi_s - V_{bs}}$$

where *VFB* = -1.0. If *VTH*0 is given, *VFB* defaults to

$$VFB = VTH0 - \Phi_s - K1\sqrt{\Phi_s - V_{bs}}$$

Note-5: If K_1 and K_2 are not given, they are calculated by

$$K1 = g_2 - 2K2\sqrt{\Phi_s - VBM}$$

$$K2 = \frac{(g_1 - g_2)\left(\sqrt{\Phi_s - VBX} - \sqrt{\Phi_s}\right)}{2\sqrt{\Phi_s}\left(\sqrt{\Phi_s - VBM} - \sqrt{\Phi_s}\right) + VBM}$$

Note-6: If *CGSO* is not given, it is calculated by

If (*DLC* is given and > 0.0)

$$CGSO = DLC \cdot C_{oxe} - CGSL$$

if (*CGSO* < 0.0), *CGSO* = 0.0

Else

$$CGSO = 0.6 \cdot XJ \cdot C_{oxe}$$

If *CGDO* is not given, it is calculated by

If (*DLC* is given and > 0.0)

$$CGDO = DLC \cdot C_{oxe} - CGDL$$

if (*CGDO* < 0.0), *CGDO* = 0.0

Else

$$CGDO = 0.6 \cdot XJ \cdot C_{oxe}$$

If *CGBO* is not given, it is calculated by

$$CGBO = 2 \cdot DWC \cdot C_{oxe}$$

Note-7: If *CF* is not given, it is calculated by

$$CF = \frac{2 \cdot EPSROX \cdot \varepsilon_0}{\pi} \cdot \log\left(1 + \frac{4.0e-7}{TOXE}\right)$$

Note-8:

For ***dioMod*** = 0, if *XJBVS* < 0.0, it is reset to 1.0.

For ***dioMod*** = 2, if *XJBVS* <=0.0, it is reset to 1.0.

For ***dioMod*** = 0, if *XJBVD* < 0.0, it is reset to 1.0.

For ***dioMod*** = 2, if *XJBVD* <=0.0, it is reset to 1.0.

Appendix B: CORE PARAMETERS

Parameter name	Description	Default value	Binnable?	Note
TOXE	Electrical gate equivalent oxide thickness	3.0e-9m	No	Fatal error if not positive
TOXP	Physical gate equivalent oxide thickness	TOXE	No	Fatal error if not positive
DTOX	Defined as (TOXE-TOXP)	0.0m	No	-
XJ	S/D junction depth	1.5e-7m	Yes	-
NDEP	Channel doping concentration at depletion edge for zero body bias	1.7e17cm^{-3}	Yes	Note-2
VTH0 or VTHO	Long-channel threshold voltage at V_{bs}=0	0.7V (NMOS) -0.7V (PMOS)	Yes	Note-4
K1	First-order body bias coefficient	0.5$V^{1/2}$	Yes	Note-5
K2	Second-order body bias coefficient	0.0	Yes	Note-5
LPE0	Lateral non-uniform doping parameter at V_{bs}=0	1.74e-7m	Yes	-
DVT0	First coefficient of short-channel effect on V_{th}	2.2	Yes	-
DVT1	Second coefficient of short-channel effect on V_{th}	0.53	Yes	-
U0	Low-field mobility	0.067 m^2/(Vs) (NMOS); 0.025 m^2/(Vs) PMOS	Yes	-
VSAT	Saturation velocity	8.0e4m/s	Yes	-

Parameter name	Description	Default value	Binnable?	Note
WINT	Channel-width offset parameter	0.0m	No	-
LINT	Channel-length offset parameter	0.0m	No	-
VOFF	Offset voltage in subthreshold region for large W and L	-0.08V	Yes	-
NFACTOR	Subthreshold swing factor	1.0	Yes	-
ETA0	DIBL coefficient in subthreshold region	0.08	Yes	-
PCLM	Channel length modulation parameter	1.3	Yes	-
RDSW	Zero bias LDD resistance per unit width for RDSMOD=0	200.0 ohm$(\mu m)^{WR}$	Yes	If negative, reset to 0.0
ALPHA0	First parameter of impact ionization current	0.0Am/V	Yes	-
BETA0	The second parameter of impact ionization current	30.0V	Yes	-
CGSO	Non LDD region source-gate overlap capacitance per unit channel width	calculated (F/m)	No	Note-6
CGDO	Non LDD region drain-gate overlap capacitance per unit channel width	calculated (F/m)	No	Note-6
CGBO	Gate-bulk overlap capacitance per unit channel length	0.0	F/m	Note-6
DLC	Channel-length offset parameter for CV model	LINT (m)	No	-
DWC	Channel-width offset parameter for CV model	WINT (m)	No	-
NOFF	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion	1.0	Yes	-
VOFFCV	CV parameter in $V_{gsteff,CV}$ for week to strong inversion	0.0V	Yes	-
NTNOI	Noise factor for short-channel devices for TNOIMOD=0 only	1.0	No	-
TNOIA	Coefficient of channel-length dependence of total channel thermal noise	1.5E6	No	-
TNOIB	Channel-length dependence parameter for channel thermal noise partitioning	3.5E6	No	-

Parameter name	Description	Default value	Binnable?	Note
JSS JSD	Bottom junction reverse saturation current density	JSS= 1.0e-4A/m^2 JSD=JSS	No	-
CJS CJD	Bottom junction capacitance per unit area at zero bias	CJS=5.0e-4 F/m^2 CJD=CJS	No	-
WW	Coefficient of width dependence for width offset	$0.0m^{WWN}$	No	-
WWN	Power of width dependence of width offset	1.0	No	-
LL	Coefficient of length dependence for length offset	$0.0m^{LLN}$	No	-
LLN	Power of length dependence for length offset	1.0	No	-

Appendix C: References

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