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博 士 論 文

高速低耗能逐漸趨近式類比至數位轉換器之設計

Design of High-Speed Energy-Efficient Successive-Approximation Analog-to-Digital Converters

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Design of High-Speed Energy-Efficient Successive-Approximation Analog-to-Digital Converters

by

Chun-Cheng Liu

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摘　要

本論文提出三個應用於逐漸趨近式類比至數位轉換器的電路設計技術，並且透過實際的晶片下線和量測驗證，證實所提出之電路設計技術可以有效提升電路的操作速度以及降低每次轉換所消耗的能量。所提出的電路設計技術以及晶片實作成果簡述如下：

第一個技術為單調式的電容切換機制，其比傳統架構的切換方式節省約 81.3%的切換能量以及 50%的取樣電容。在 0.13 微米互補式金氧半電晶體製程下，我們利用此技術來實現一個 10 位元，每秒 5 千萬次取樣的逐漸趨近式類比至數位轉換器。此類比至數位轉換器在 1.2 伏特的電壓下，其功率消耗為 0.92 毫瓦，有效位元為 8.48 bits，等效的 FOM 僅為 52 fJ/conversion-step。然而，單調式的電容切換機制會導致比較器輸入端訊號共模電壓的改變，使得比較器的動態偏移嚴重影響電路的效能。為了改善這個問題，我們提出一個改良版的比較器電路，可以有效控制比較器的動態偏移量。此外，在電路內部改採用非同步操作方式以避免使用數倍於取樣速度的高頻時脈訊號，降低系統整合的複雜度。同樣在 0.13 微米互補式金氧半電晶體製程下，我們實現另一個 10 位元，每秒 5 千萬次取樣的逐漸趨近式類比至數位轉換器。在 1.2 伏

特的電壓下，其功率消耗為 0.826 毫瓦，有效位元提升為 9.18 bits，等效的 FOM 僅為 29 fJ/conversion-step。

第二個技術為二進制的錯誤補償機制。高速操作的逐漸趨近式類比至數位轉換器，由於每個位元週期的時間非常短，常常在 DAC 電壓還沒穩定的時候就必須要做下一次的比較，DAC 電壓穩定的問題嚴重影響電路的效能，也限制了電路的操作速度。我們提出了一個二進制的錯誤補償機制，在電路中插入額外的補償位元來做錯誤校正，因此比較器可以在 DAC 還沒穩定的時候先做比較，以提升電路操作速度。在 65 奈米互補式金氧半電晶體製程下，我們利用此技術來實現一個 10 位元，取樣速度可以達到每秒 1 億次的逐漸趨近式類比至數位轉換器。在 1.2 伏特的電壓下，其功率消耗為 1.13 毫瓦，有效位元為 9.51 bits，等效的 FOM 僅為 15.5 fJ/conversion-step。

第三個技術則是利用一個輔助預測電路，來避免不必要的電容切換，此技術可以省下 40-45%的電容切換能量消耗。配合第一個技術，電容切換的能量消耗可以比傳統方法減少約 90%左右。除此之外，這個技術還能改善電路的靜態以及動態效能。在 0.18 微米互補式金氧半電晶體製程下，我們利用此技巧來實現一個 10 位元，每秒 1 千萬次取樣的逐漸趨近式類比至數位轉換器。在 1 伏特的電壓下，其功率消耗僅為 98 微瓦，有效位元為接近理想的 9.83 bits，等效的 FOM 僅為 11 fJ/conversion-step。

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Abstract

This dissertation proposes three circuit design techniques for successive-approximation register (SAR) analog-to-digital converters (ADCs). According to the measurement results of the proof-of-concept prototypes, the proposed techniques are able to improve the operating speed and achieve excellent energy efficiency. The proposed techniques and chip measurement results are sketched as follows:

The first technique is a monotonic capacitor switching procedure. Compared to converters that use the conventional procedure, the average switching energy and total sampling capacitance are reduced by about 81.3% and 50%, respectively. A 10-bit, 50-MS/s SAR ADC with the proposed monotonic capacitor switching procedure is implemented in a 0.13-μm 1P8M CMOS technology. The prototype ADC consumes 0.92 mW from a 1.2-V supply, and the effective number of bit (ENOB) is 8.48 bits. The resulting figure of merit (FOM) is 52 fJ/conversion-step. However, the signal-dependent offset caused by the variation of the input common-mode voltage degrades the linearity of ADC. We proposed an improved comparator design to avoid the linearity degradation. Besides, to avoid a clock signal with frequency higher than sampling rate, we used an

asynchronous control circuit to internally generate the necessary control signals. The revised prototype is also implemented in a 0.13-μm 1P8M CMOS technology. It consumes 0.826 mW from a 1.2-V supply and achieves an ENOB of 9.18 bits. The resultant FOM is 29 fJ/conversion-step.

The second technique is a binary-scaled error compensation method. In a medium-to-high resolution case, the DAC settling issue limits the operating speed of a SAR ADC, because it is not easy for the capacitive DAC to stabilize in a short time interval. We insert extra binary-scaled compensation bits to compensate for the DAC settling error. Accordingly, the comparator can perform comparison before the DAC is completely settled, resulting in improved operating speed. A 10-bit, 100-MS/s SAR ADC using the binary-scaled error compensation method is implemented in a 65-nm 1P6M CMOS technology. The prototype consumes 1.13 mW from a 1.2-V supply and achieves an ENOB of 9.51 bits. The resultant FOM is 15.5 fJ/conversion-step.

The third technique is a predictive capacitor switching method that uses a predictive circuit to avoid unnecessary switching in a DAC network. This method saves 40~45% switching energy. Combined with the first technique, the average switching energy is reduced by about 90% than the conventional one. In addition, this technique improves static and dynamic performance of a SAR ADC. A 10-bit, 10-MS/s SAR ADC using this method is implemented in a 0.18-μm 1P6M CMOS technology. The prototype consumes 98 μW from a 1-V supply and achieves an excellent ENOB of 9.83 bits. The resultant FOM is only 11 fJ/conversion-step.

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劉純成 謹誌於

國立成功大學電機系 SSCAS 實驗室

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Chapter 1
Introduction

1.1 Motivation

Conventionally, successive-approximation register (SAR) analog-to-digital converters (ADCs) are extensively used in low-power and low-speed (below several MS/s) applications. For medium- to high-speed applications, the flash ADC and pipelined ADC have been the popular architectures. In recent years, with the feature sizes of CMOS devices scaled down, the increasing speed of devices has enabled the SAR ADCs to achieve several tens of MS/s to low GS/s sampling rates with 5- to 12-bit resolutions [1-15]. Additionally, SAR ADCs have the features of low power and low cost that makes it more appealing than the other architectures for some portable systems or low-power-demand applications. Many recent researches have been involved in this ADC. The main techniques of SAR ADCs in recent published papers can be categorized as follows:

(1)Passive charge sharing SAR ADC

The passive charge sharing SAR ADC [1-2] works completely in charge domain instead of voltage domain. During the SAR algorithm, charge is added or subtracted to the sampling capacitor until the result converges to zero. The ADC uses tracking capacitors to pre-track the input signals in all clock period except the sampling phase. Therefore, it has a sufficient time interval to track the input and no settling problems occur.

(2) Non-binary SAR ADC

To reduce the power consumption, a SAR ADC usually uses a capacitive DAC to generate the reference voltage instead of a resistive DAC. However, the capacitive DAC has a longer settling time which is proportional to the resolution. Therefore, a capacitive-DAC-based SAR ADC has limited operation speed. The non-binary SAR ADC [3-5] uses a non-binary-scaled capacitor sizes (e.g., 1 1.85 1.85^2 1.85^3 1.85^4…). More decision levels are generated than the conventional design. There are several digital codes for every input voltage. Hence, a certain range of DAC settling error does not affect the conversion result. The conversion rate of the ADC was improved.

(3)Time-interleaving SAR ADC

The sampling rate of a single SAR ADC is not as fast as the flash ADC or pipelined ADC. The time-interleaving SAR ADC [5-12] was proposed to improve the sampling rate. However, the time-interleaving SAR ADC has a channel mismatch problem. For medium- to high-resolution applications, the interleaved ADC must use digital calibration or post processing [5] to overcome the channel mismatch and some non-ideal effects to achieve sufficient performance. The time-interleaving SAR ADC increases the sampling rate, but on-chip digital calibration circuit usually occupies large area and results in large power consumption. Therefore, developing a low-cost high-efficiency digital calibration

technique is one of the hottest topics of SAR ADCs.

(4) Asynchronous SAR ADC

Conventional SAR ADCs only convert one bit in each bit cycle. For an *N*-bit SAR ADC, it needs *N+1* clock cycles to complete one conversion (one clock cycle is used to sample the input signal). An extra PLL circuit is needed to provide the high frequency clock that increases the design and hardware overhead. The asynchronous SAR ADC [11] internally generates the necessary control signal. The sampling rate is equal to the clock rate. Therefore, an asynchronous SAR ADC does not need any extra PLL circuit.

(5)Reduce the switching energy in DAC network

In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator, and capacitive reference DAC network. Digital power consumption becomes lower with the advancement of technology. Technology scaling also improves the speed of digital circuits. On the other hand, the power consumption of the comparator and capacitor network is limited by mismatch and noise. Recently, several energy-efficient switching methods have been proposed to lower the switching energy of the capacitor network. The split capacitor method [12] reduces switching energy by 37%, and the energy-saving method [16] reduces energy consumption by 56%.

There are some other techniques, like multi-bit/step [8], pipelined-SAR [13], etc., are also presented to improve the sampling rate or reduce the power consumption of the SAR ADC. The SAR architecture become feasible alternatives to flash ADCs and pipelined ADCs in nanometer scaled CMOS processes.

Except the above techniques, we proposed and demonstrated several circuit techniques to improve the operating speed and achieve excellent energy efficiency. The proposed monotonic switching procedure leads to both lower switching energy and smaller total

capacitance. It also simplifies the digital logic control circuit that reduces the power consumption and improves the operating speed. The proposed method is suited for high-speed, low-power and low-cost design. However, the signal-dependent offset caused by the variation of the input common-mode voltage degrades the linearity of ADC. Therefore, we proposed a biased comparator to reduce the dynamic offset. The improved comparator design mitigates the linearity degradation. In addition, a splitting monotonic switching procedure is also proposed to avoid the input common-mode voltage variation. Hence, the signal-dependent offset has no influence on the ADC linearity.

A binary-scaled error compensation method is proposed to overcome the DAC settling issue in the high-speed SAR ADC. Similar to the non-binary search technique, the binary-scaled error compensation method is capable of enhancing the sampling rate, and results in fewer design and hardware overhead compared to the non-binary search technique.

We proposed an improved switching scheme which uses a predictive circuit to avoid unnecessary switching in DAC network. This method reduces the power consumption and improves linearity of ADC without degrading the operation speed.

1.2 Organization of the dissertation

This dissertation presents the design and implementation of several circuit design techniques for SAR ADCs. The remainder of the dissertation is organized as follows:

Chapter 2 discusses and analyzes the conventional switching procedure and the proposed monotonic capacitor switching procedure. Chapter 3 introduces the proposed binary-scaled error compensation method. In Chapter 4, we will introduce a splitting monotonic switching method and a predictive capacitor switching procedure which uses a predictive circuit to reduce unnecessary switching in DAC network. Finally, generalized conclusions are presented in Chapter 5, and future works of this research are summarized for further exploration.

Chapter 2
Monotonic Capacitor Switching Procedure for SAR ADC

Recently, several energy-efficient switching methods [12] [16] have been proposed to lower the switching energy of the capacitor network for the SAR ADC. Although these methods reduce the switching energy, they make the SAR control logic more complicated due to the increased number of capacitors and switches, yielding higher digital power consumption. In Section 2.1, we proposed a monotonic switching procedure that reduces power consumption by 81.3% in the DAC network without splitting or adding any capacitors and switches. The total capacitance in the DAC capacitor network is reduced by 50%. In Section 2.2, a SAR ADC with proposed monotonic switching procedure is introduced. The work demonstrates the effectiveness of the switching procedure. However, the signal-dependent offset caused by the variation of the input common-mode voltage degrades the ADC linearity. Section 2.3 presents an improved comparator design to avoid the linearity degradation, and the implementation of the revised prototype is also presented. Section 2.4 introduces the implementation of a 6-bit time-interleaving SAR ADC using the proposed switching scheme.

2.1 Proposed Monotonic Capacitor Switching Procedure

2.1.1 Conventional SAR ADC

To achieve medium-to-high resolutions, a fully differential architecture suppresses the substrate and supply noise and has good common-mode noise rejection. SAR ADCs usually use a binary-weighted capacitor array rather than a C-2C capacitor array for better linearity. Figure 2-1 shows a conventional 10-bit fully differential SAR ADC. The fundamental building blocks are the comparator, sample-and-hold (S/H) circuit, capacitor network, and successive approximation registers. In the charge-redistribution based architecture, the capacitor network serves both as a S/H circuit and a reference DAC capacitor array. Therefore, this architecture does not require a monolithic S/H circuit. The main function of the capacitor network is D/A conversion. The input voltage is subtracted from the output voltage of the D/A converter, which is realized by properly controlling the switches of the capacitor network. The comparator connects to the outputs of capacitor arrays. The result of the comparison will send to SAR control logic.

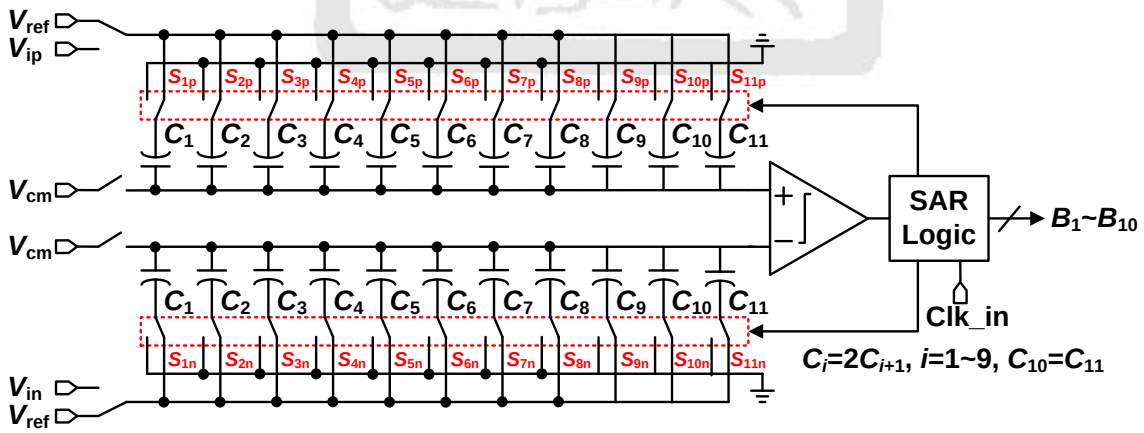


Figure 2-1 A conventional 10-bit SAR ADC.

Since this ADC is fully differential, the operation of the two sides is complementary. For simplicity, only the positive-side (upper-side) operation of the ADC is described below. At the sampling phase, the bottom plates of the capacitors are charged to V_{ip}, and the top plates are reset to the common-mode voltage V_{cm}. Next, the largest capacitor C_1 is switched to V_{ref} and the other capacitors are switched to ground. The comparator then performs the first comparison. If V_{ip} is higher than V_{in}, the most significant bit (MSB) B_1 is 1. Otherwise, B_1 is 0, and the largest capacitor is reconnected to ground. Then, the second largest capacitor C_2 is switched to V_{ref}. The comparator does the comparison again. The ADC repeats this procedure until the least significant bit (LSB) is decided. Although the trial-and-error search procedure is simple and intuitive, it is not an energy efficient switching scheme, especially when unsuccessful trials occur.

2.1.2 Proposed SAR ADC

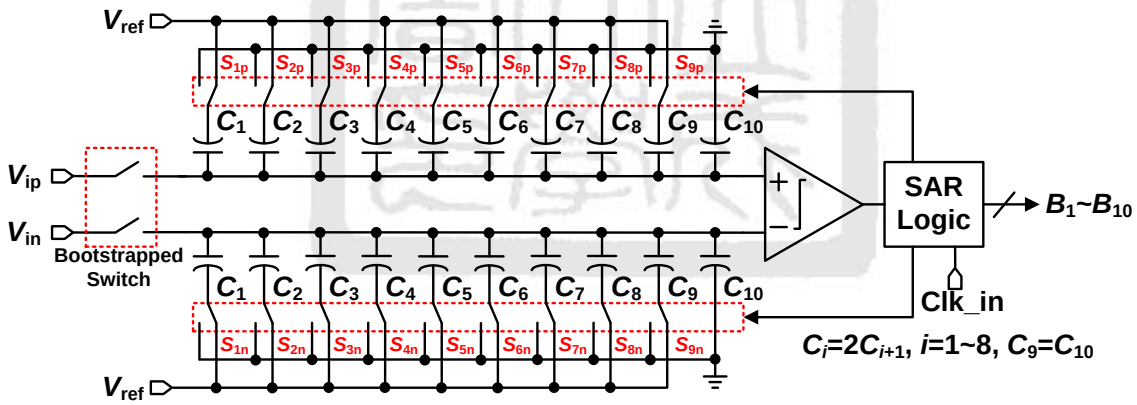


Figure 2-2 The proposed SAR ADC architecture.

Figure 2-2 shows the proposed SAR ADC. The proposed ADC samples the input signal on the top plates via bootstrapped switches, which increases the settling speed and input bandwidth. At the same time, the bottom plates of the capacitors are reset to V_{ref}. Next, after the ADC turns off the bootstrapped switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the

largest capacitor C_1 on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switched, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. The proposed switching procedure can be either upward or downward. For fast reference settling, i.e., discharging through n-type transistors, downward switching was selected in this ADC. The flow chart of the proposed successive-approximation procedure is shown in Figure 2-3.

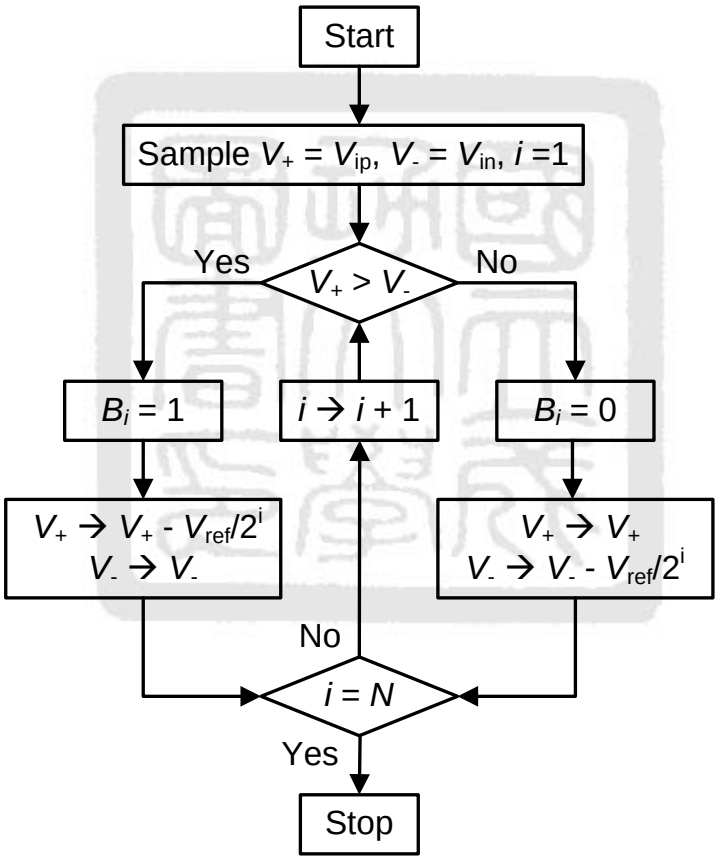


Figure 2-3 Flow chart of the proposed SAR ADC.

The proposed switching sequence does not require upward transition. At the same transistor size, the on-resistance of a NMOS switch is only about 1/3 that of a PMOS one. Having no upward transition speeds up the DAC settling. In addition, since sampling is

done on the top plate [17], the comparator can perform the first comparison without any capacitor switching, leading to a faster algorithm. For an *n*-bit ADC, the number of unit capacitors in a capacitor array is 2^{n-1}, only half that of the conventional one.

One of the major differences between the proposed method and the conventional one is that the common-mode voltage of the reference DAC gradually decreases from half V_{ref} to ground as shown in Figure 2-4.

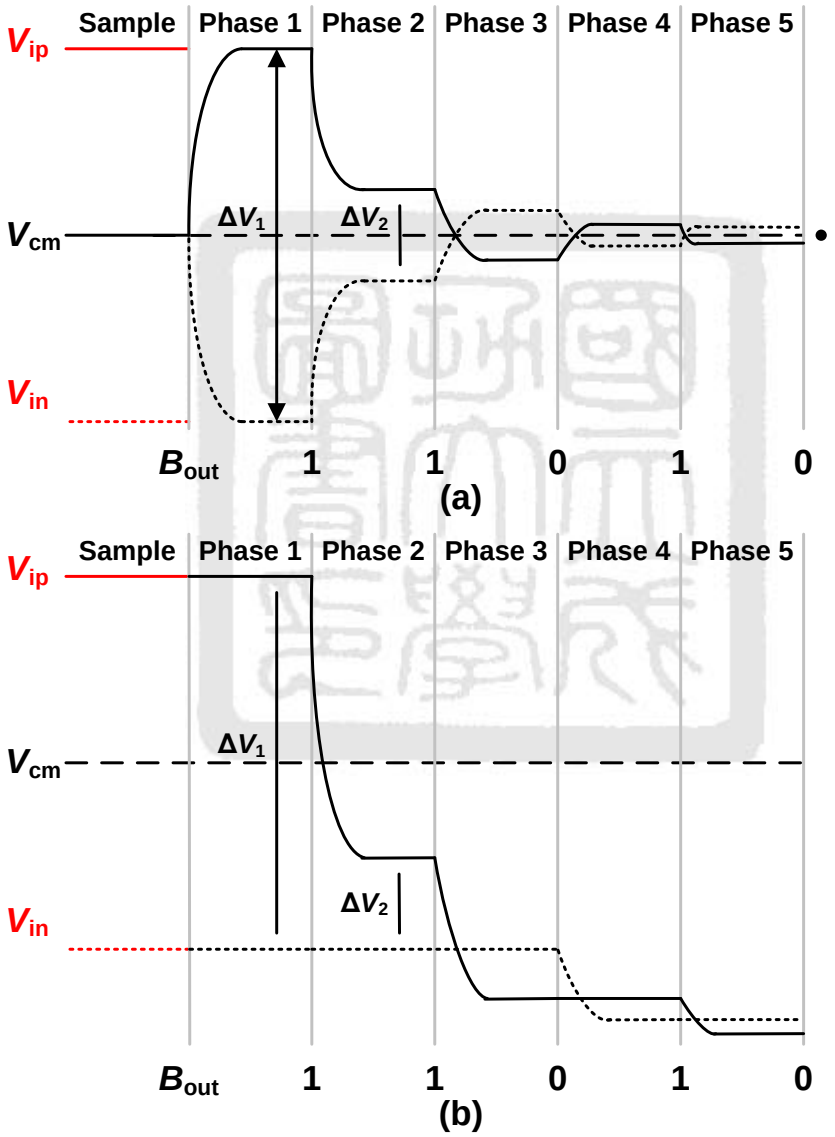


Figure 2-4 (a) Waveform of conventional switching procedure. (b) Waveform of proposed monotonic switching procedure.

2.1.3 Analysis of Switching Energy in DAC Network

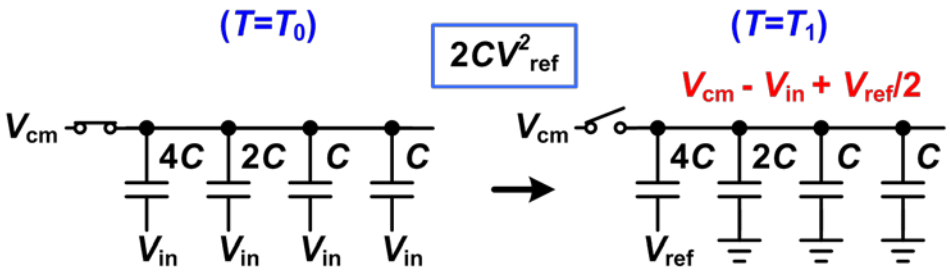


Figure 2-5 A 3-bit capacitor array with conventional switching method.

It is instructive to calculate the total energy drawn from V_{ref} when switching the capacitor array. For alleviating the computation, a 3-bit capacitor array is taken as an example (Figure 2-5). If the capacitor array settles in the time interval T_0~T_1, the total energy drawn from V_{ref} is:

$$E_{T_0 \to T_1} = \int_{T_0}^{T_1} I_{\text{ref}}(t) V_{\text{ref}} dt = V_{\text{ref}} \int_{T_0}^{T_1} I_{\text{ref}}(t) dt \tag{2-1}$$

Since $I_{\text{ref}}(t) = -dQ_{\text{C}} / dt$ and $Q_{\text{C}}(T) = 4CV_{\text{X}}[T]$, equation (2-1) simplifies to:

$$\begin{aligned} E_{T_0 \to T_1} &= -V_{\text{ref}} \int_{T_0}^{T_1} \frac{dQ_{\text{C}}}{dt} dt = -V_{\text{ref}} \int_{Q_{\text{C}}(T_0)}^{Q_{\text{C}}(T_1)} dQ_{\text{C}} = -V_{\text{ref}} (Q_{\text{C}}(T_1) - Q_{\text{C}}(T_0)) \\ &= -V_{\text{ref}} (4C)(V_{\text{X}}[T_1] - V_{\text{X}}[T_0]) \end{aligned} \tag{2-2}$$

Since $V_{\text{X}}[T_0] = \Delta V_{\text{C}}[T_0]$, $V_{\text{X}}[T_1] = \Delta V_{\text{C}}[T_1]$,

and $\Delta V_{\text{C}}[T_0] = V_{\text{cm}} - V_{\text{in}}$, $\Delta V_{\text{C}}[T_1] = (V_{\text{cm}} - V_{\text{in}} + \frac{1}{2} V_{\text{ref}}) - V_{\text{ref}}$.

Then, equation (2-2) is:

$$E_{T_0 \to T_1} = 2CV_{\text{ref}}^2 \tag{2-3}$$

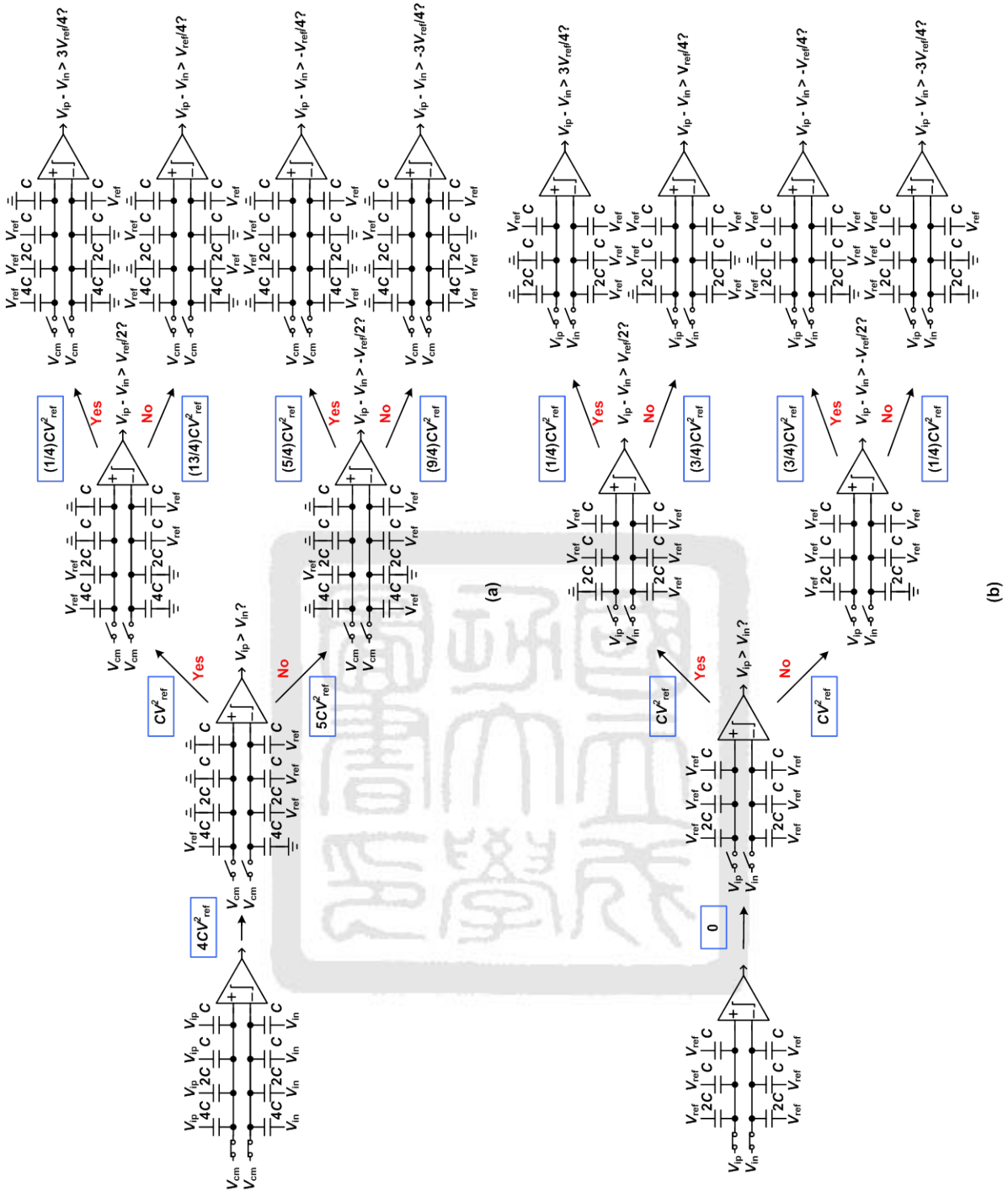


Figure 2-6 (a) Conventional switching procedure. (b) Proposed switching procedure.

Figure 2-6 shows 3-bit examples of the conventional and proposed switching methods. The conventional switching method is based on a trial-and-error search procedure. Figure 2-6(a) shows all possible conversions. The quantitative energy consumption of each switching phase is also shown in the figure. The conventional switching sequence is efficient when all the attempts are successful, as in the upper cases. However, the switching sequence consumes a lot of energy when attempts are unsuccessful, as in the lower cases. Figure 2-6(b) shows all possible switching cases of the proposed method. After the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. Therefore, the proposed switching sequence consumes no energy before the first comparison. In contrast, the conventional sequence consumes $4CV_{\text{ref}}^2$ before the first comparison. The subsequent switching sequence of the proposed method is also more efficient than that of the conventional one.

For an *n*-bit conventional SAR ADC, if each digital output code is equiprobable, the average switching energy can be derived as:

$$E_{\text{avg,conv}} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1)CV_{\text{ref}}^2 \tag{2-4}$$

The average switching energy for an *n*-bit SAR ADC using the proposed switching procedure can be derived as:

$$E_{\text{avg,mono}} = \sum_{i=1}^{n-1} (2^{n-2-i})CV_{\text{ref}}^2 \tag{2-5}$$

For a 10-bit case, the conventional switching procedure consumes $1365.3CV_{\text{ref}}^2$ while the proposed switching procedure consumes only $255.5CV_{\text{ref}}^2$. The proposed technique thus requires 81.3% less switching energy than that of the conventional one. Split capacitor [12] and energy-saving [16] switching methods provide only 37% and 56% reductions, respectively.

Figure 2-7 shows a comparison of switching energy for the four methods versus the digital output code in a 10-bit ADC. The proposed method has the best power efficiency.

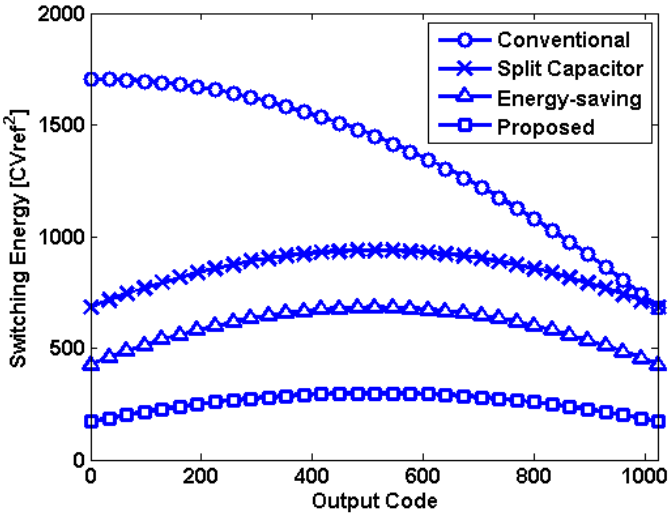


Figure 2-7 Switching energy versus output code in a 10-bit ADC.

Table 2-1 Comparison of Switching Procedures

Switching Procedure	Conventional	Split Capacitor	Energy-saving	Proposed
Normalized Switching Power	1	0.63	0.44	0.19
No. of Switches	$4N+10$	$8N+6$	$8N+2$	$4N$
No. of Capacitors	$2N+2$	$4N$	$4N-2$	$2N$
No. of Unit Capacitors in Capacitor Array	2^N	2^N	2^N	2^{N-1}

Table 2-1 summarizes the features of the four methods. The proposed architecture not only has the lowest switching power consumption but also the fewest switches and unit capacitors, which simplifies digital control logic. Therefore, the proposed ADC is very hardware efficient as well.

2.2 A 0.92mW 10-bit 50-MS/s SAR ADC

This section presents the design of a 10-bit 50-MS/s SAR ADC with the proposed monotonic switching procedure [18]. The schematic of the proposed SAR ADC is as shown in Fig 2-2. The fundamental building blocks of the proposed ADC are a S/H circuit, a dynamic comparator, SAR control logic, and a capacitor network. The design considerations of the building blocks are described in the following sub-sections.

2.2.1 Sample and Hold Circuit

The proposed SAR ADC samples the input signal via the bootstrapped switches at the top plates of capacitors. An NMOS transistor used as a switch has a non-zero on-resistance, which can roughly be approximated as [19]:

$$R_{ON} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_G - V_T - \frac{V_S + V_D}{2})}. \quad (2\text{-}6)$$

This means that the on-resistance is signal dependent. When applying such a switch in a switched capacitor network, this non-linearity will result in harmonic distortion. A known solution for this problem is bootstrapping, which increases the overdrive voltage without special processing steps or compromising on reliability. The bootstrapped switch [20] shown in Figure 2-8 performs the S/H function. With the bootstrapped switch, the gate-source voltage of the sampling transistor is fixed at the supply voltage (V_{DD}), which makes the on-resistance a small constant value and thus improves the switch linearity. Although the absolute voltage applied to the gate may exceed V_{DD} for a positive input signal, none of the terminal-to-terminal device voltages exceeds V_{DD}.

The bootstrapped circuit operates with a single phase clock (*Clks*) that turns the switch M_{10} on and off. During the off phase, *Clks* is low. Devices M_8 and M_9 discharge the gate of

M_{10} to ground. At the same time, V_{DD} is applied across capacitor C_S by M_2 and M_1. This capacitor will act as the battery across the gate and source during the on phase. M_5 and M_7 isolate the switch from C_S while it is charging. When *Clks* goes high, M_3 pulls down the gate of M_5, allowing charges from the capacitor C_S to flow onto the gate of M_7 and M_{10}. This turns on both M_7 and M_{10}. M_7 enables the gate of M_{10} to track the input voltage (*IN*) with a shift of V_{DD}, keeping the gate-source voltage constant regardless of the input signal.

In this design, the value of C_S is 400 fF, where the capacitor is a Metal-Insulator-Metal (MIM) capacitor. Because the switch (M_{10}), V_{GS} is independent of the signal. Rail-to-rail signals can be used. The switch linearity is also improved, and signal-dependent charge injection is reduced. The result obtains fast settling and large input bandwidth.

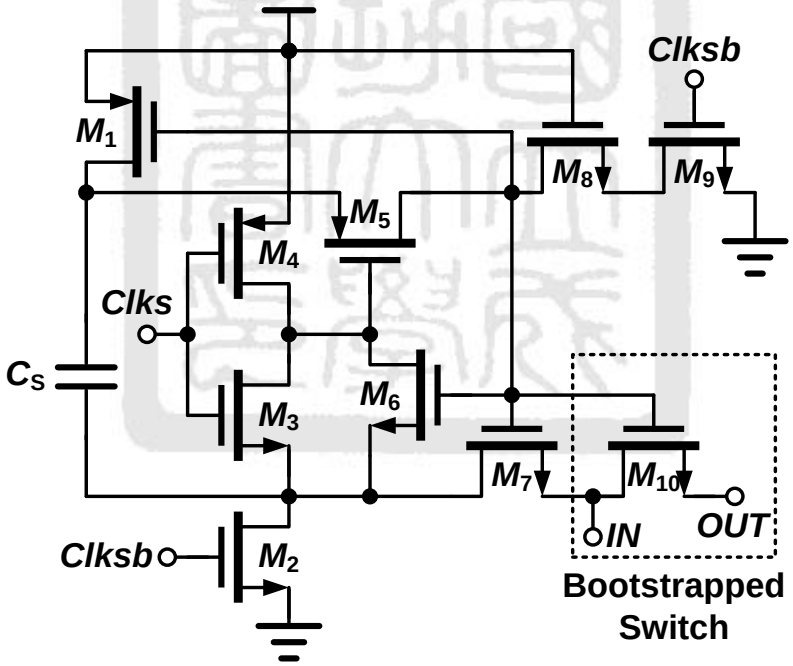


Figure 2-8 Bootstrapped switch.

2.2.2 Comparator Design

A high-speed, low-power and accurate CMOS comparator is crucial for the SAR ADC. To satisfy the above considerations, a latched differential input comparator [1] is chosen. Figure 2-9 shows the schematic of the comparator without static power consumption. In order to work properly in a common-voltage range from $V_{ref}/2$ to ground, the comparator utilizes a p-type input pair.

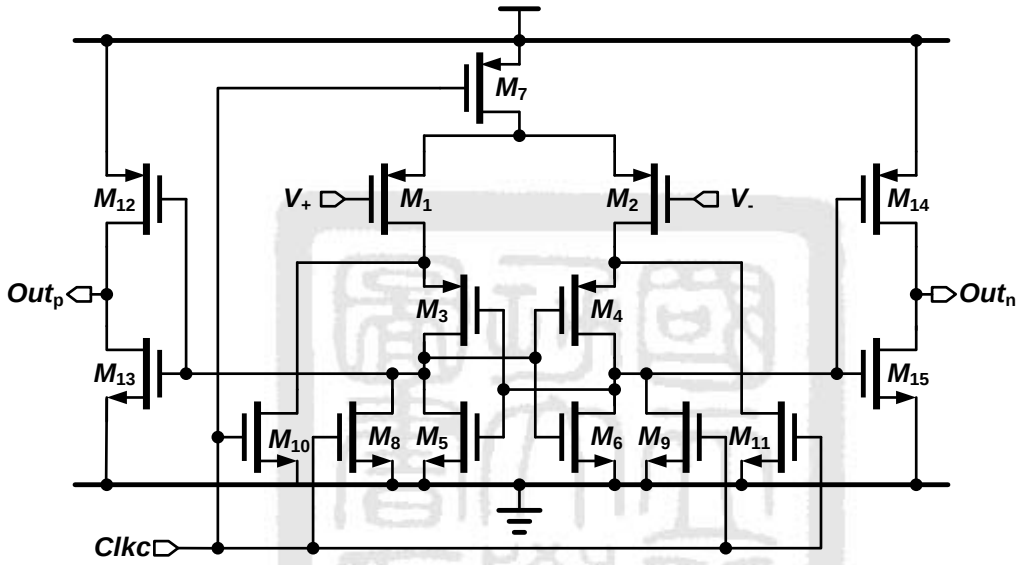


Figure 2-9 The schematic of a latch-based dynamic comparator.

The operation principle is described as follow: When *Clkc* is high, the comparator is in pre-charge phase. The comparator outputs Out_p and Out_n are reset to high. When *Clkc* goes to low, the comparator is in comparison phase. The differential pair, M_1 and M_2, compares the differential input voltages V_+ and V_-. Then, the latch regeneration forces one output to high and the other to low according the comparison result. When the comparator is in steady-state, there is no dc current flowing from V_{DD} to ground. Therefore, it is suitable for low power applications.

2.2.3 SAR Control Logic

Figure 2-10 shows the schematic of the internal clock generator and its timing diagram. *Clks* is used to sample the input signal. We use two clock cycles as the sampling phase to ensure the sampling bandwidth is larger than the Nyquist frequency. Therefore, the SAR ADC needs 12 clock cycles to complete one conversion. At 50 MS/s sampling rate, it needs a global 600-MHz clock. *Clkc* is the control signal of the comparator. Clk_1 to Clk_{10} sample the digital output codes of the comparator and serve as control signals for the capacitor arrays to perform the monotonic switching procedure.

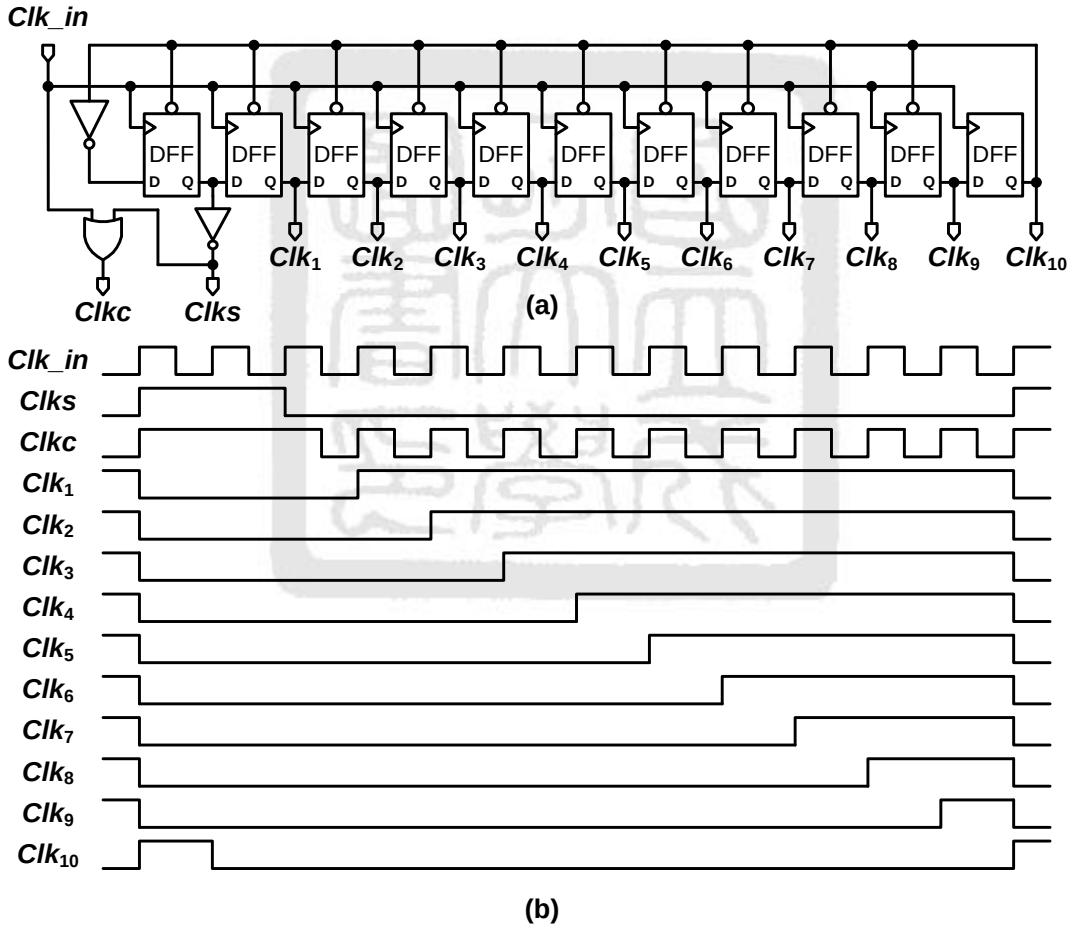


Figure 2-10 Internal clock generator: (a) Schematic. (b) Timing diagram.

Figure 2-11 shows the schematic and timing diagram of the DAC control logic. At the rising edge of Clk_i, a static flip-flop samples the comparator output. If the output is high,

the relevant capacitor is switched from V_{ref} to ground. If the output is low, the relevant capacitor is kept connected to V_{ref}. At the falling edge of Clk_i, all capacitors are reconnected to V_{ref}. The delay buffer guarantees that Clk_i triggers the AND gate after the output of the static flip-flop arrived. This timing arrangement avoids unnecessary transitions. This work uses an inverter as a switch buffer. The conventional architecture in Figure 2-1 samples both the input signal and reference voltages on the bottom plates. If the input swing is nearly rail-to-rail, transmission gates are needed to sample input signal. This work uses bootstrapped switches to sample input signal onto top plates of the capacitors and uses inverter buffers to switch between positive and negative voltages. Hence, compared to the conventional architecture, no transmission gates are used, which enables high-speed and low-power operation.

To prevent unnecessary energy consumption and to keep the RC value the same, the sizes of the first six switch buffers are scaled down according to the driven capacitances and the buffers of the last three capacitors are unit size ones.

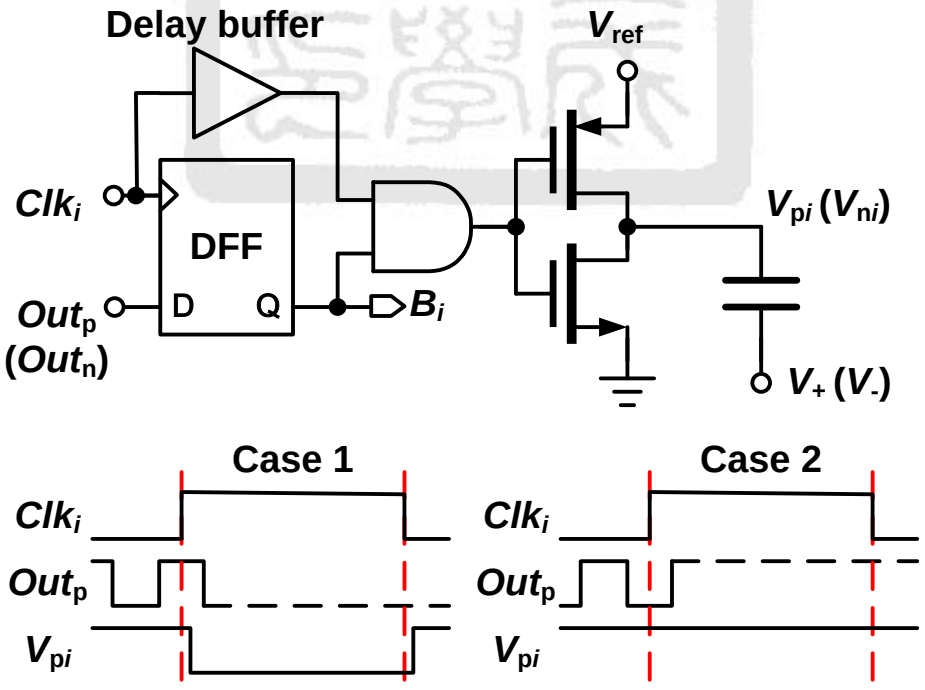


Figure 2-11 DAC control logic.

2.2.4 Capacitor Array

This prototype used MIM capacitors to construct the capacitor array. For device matching, a unit capacitor of 10 fF is used. The binary capacitor array of the 10-bit SAR ADC uses 2^9 unit capacitors. Therefore, the total sampling capacitance is 5.12 pF in each terminal.

Due to the small unit capacitance, the routing parasitic capacitance has a considerable influence on the matching of capacitances. The capacitors were placed in an intuitive way to simplify the layout routing. Figure 2-12 shows the layout floorplan of the capacitor array.

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	7	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	7	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	7	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	7	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	8	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	8	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	9	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	10	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Figure 2-12 The layout floorplan of the capacitor array.

2.2.5 Measurement Results

The prototype is fabricated in TSMC 0.13-μm 1P8M triple well CMOS technology. The micrograph is shown in Figure 2-13. The active core area is 0.075 mm^2 (250 μm × 300 μm).

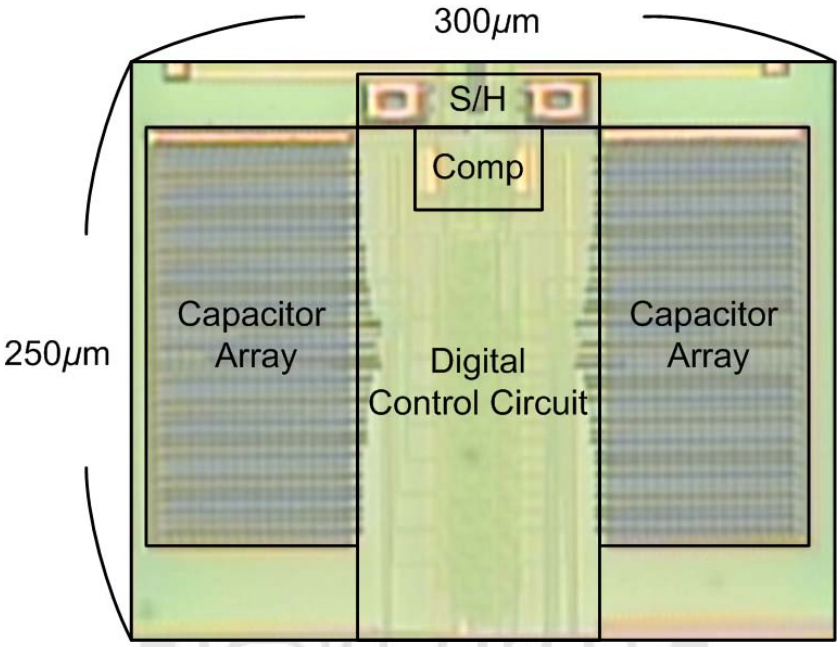


Figure 2-13 Micrograph of the prototype ADC.

The dynamic specifications, including SNDR and SFDR were analyzed by fast Fourier transform (FFT). The specifications of the static linearity, including integral nonlinearity (INL) and differential nonlinearity (DNL), were measured based on the code density testing method [21]. At 1.2-V supply and 50-MS/s sampling rate, the measured DNL and INL are shown in Figure 2-14. The measured peak DNL and INL are +0.88/-1.00 LSB and +2.20/-2.09 LSB, respectively. Large DNL peaks appear periodically every 32 digital codes, which possibly come from the underestimated comparator dynamic offset. The signal-dependent dynamic offset caused by the variation of the input common-mode voltage degraded ADC linearity.

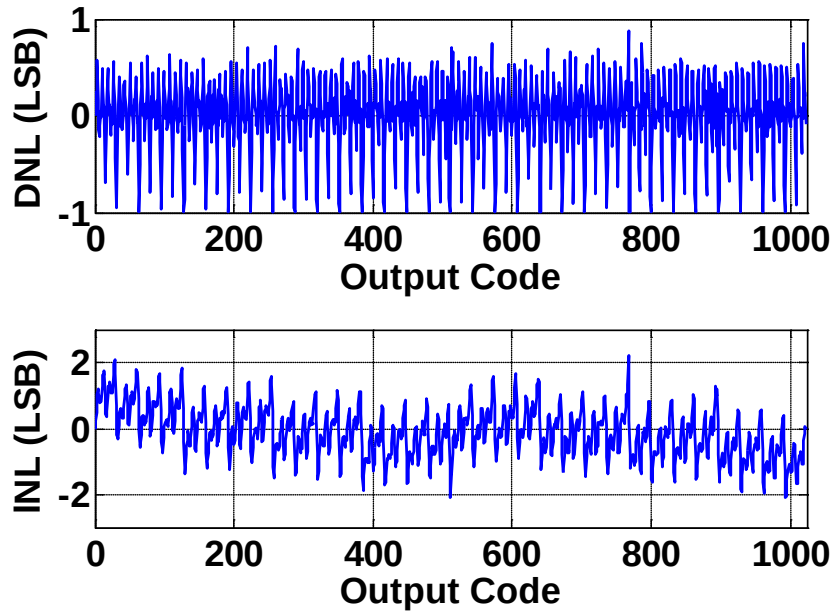


Figure 2-14 Measured DNL and INL.

Figure 2-15 shows the measured FFT spectrum with an input frequency close to 20 MHz at 1.2-V supply and 50-MS/s sampling rate. The measured SNDR and SFDR are 52.18 dB and 63.91 dB, respectively.

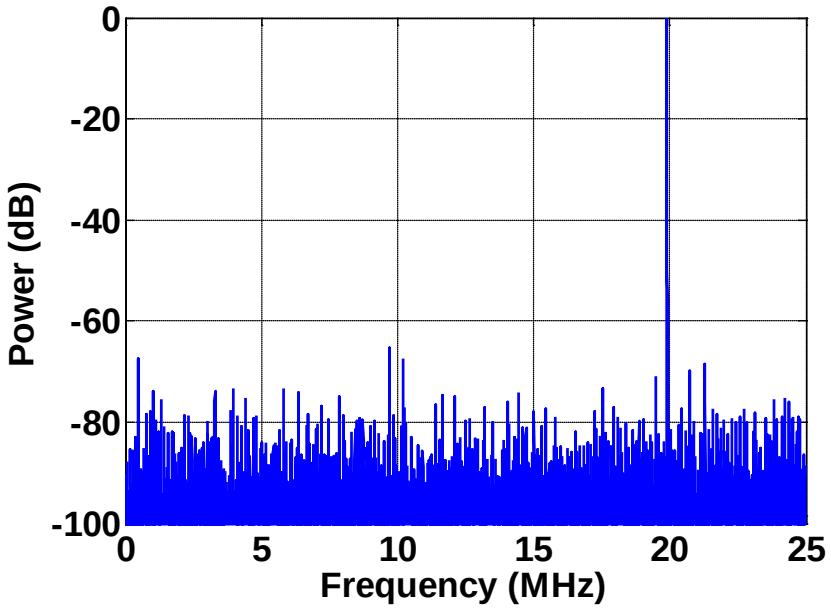


Figure 2-15 Measured FFT spectrum at 50 MS/s with a 20-MHz input frequency.

Figure 2-16 plots the measured SNDR, SFDR values versus the input frequency at 50 MS/s. At a 2-MHz input frequency, the measured SNDR and SFDR are 52.8 dB and 67.7 dB, respectively. The resultant ENOB is 8.48 bits. When the input frequency is up to 50 MHz, the measured SNDR and SFDR were 50.9 dB and 60.1 dB, respectively. The effective resolution bandwidth (ERBW) is higher than 100 MHz.

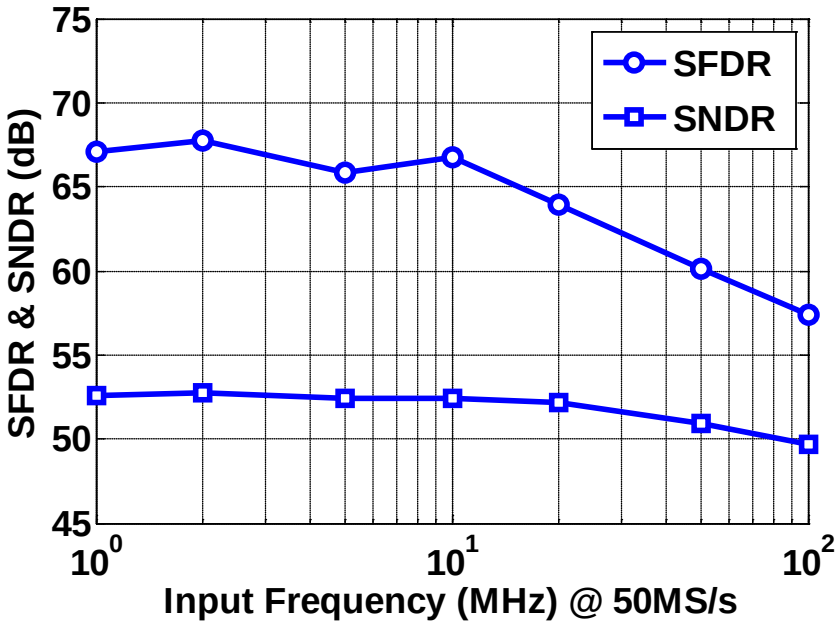


Figure 2-16 Measured SFDR and SNDR versus input frequency at 50 MS/s.

The power dissipation consumed by analog circuits including the comparator, T/H circuit and capacitor network is 0.39 mW. The digital power consumption is 0.53 mW. The total power consumption of the ADC is 0.92 mW. The measured results of the proposed ADC are summarized in Table 2-2. A comparison with state-of-the-art ADCs is listed in Table 2-3. To compare the proposed ADC to other works with different sampling rates and resolutions, the well-known figure-of-merit (FOM) equation [6] is used.

$$FOM = \frac{Power}{2^{ENOB} \times \min\{2 \times ERBW,\ f_s\}} \tag{2-7}$$

The resultant FOM of the prototype ADC is 52 fJ/conversion-step. The result shows our work is comparable to those excellent designs with similar speed and resolution.

Table 2-2 Summary of ADC Performance

Specification (Unit)	Experimental Result		
Supply Voltage (V)	1.2		
Input CM Voltage (V)	0.6		
Input Range (V_{p-p})	2		
Sampling Capacitance (pF)	5.12		
Sampling Rate (MS/s)	50		
Active Area (mm^2)	0.075		
DNL (LSB)	+0.88 / -1.00		
INL (LSB)	+2.20 / -2.09		
ENOB (bits)	8.48		
ERBW (MHz)	100		
Power (mW)	Analog	Digital	Total
	0.39	0.53	0.92
FOM (fJ/Conv.-step)	52		

Table 2-3 Comparison to State-of-the-Art Works

Specifications	*ISSCC*'07 [1]	*ISSCC*'08 [2]	*ISSCC*'10 [13]	*ISSCC*'10 [14]	*VLSI*'08 [22]	This Work
Architecture	SAR	SAR	SAR	SAR	Pipelined	SAR
Technology	90 nm	90 nm	65 nm	65 nm	90 nm	0.13 μm
Supply Voltage (V)	1	1	1.1	1.2	1.2	1.2
Sampling Rate (MS/s)	50	40	40	50	50	50
Resolution (bits)	9	9	10	10	9.4	10
ENOB (bits)	7.8	8.56	8.9	9.16	7.91	8.48
Power (mW)	0.7	0.82	1.21	0.82	1.44	0.92
FOM (fJ/Conv.-step)	65	54	65	30	119	52
Active Area (mm^2)	0.08	0.09	0.06	0.039	0.123	0.075

2.3 A 10-bit 50-MS/s SAR ADC with an Improved Comparator Design

The experimental results in Section 2.2 demonstrate the power and hardware efficiency and also the high-speed potential of the proposed SAR ADC. However, the signal-dependent offset caused by the variation of the input common-mode voltage degraded ADC linearity. The synchronous control logic needs a high-frequency global clock that results in extra design and hardware overhead. Based on the design in Section 2.2, an improved comparator was proposed to avoid the linearity degradation [23]. An asynchronous SAR control logic is proposed to avoid the requirement of a high frequency clock. Besides, the S/H circuit and capacitor network are redesigned to enhance the performance of the ADC. The design considerations of those building blocks are described in the following sub-sections.

2.3.1 S/H circuit

The bootstrapped switch shown in Figure 2-17(a) performs the S/H function. With the bootstrapped switch, the gate-source voltage of the sampling transistor is fixed at the supply voltage (V_{DD}), which makes the on-resistance a small constant value and thus improves the switch linearity. When the bootstrapped switch is off, the input signals couple to the sampling capacitors through the C_{ds} (around 5fF) which is composed of the drain-source capacitor of the sampling transistor and the routing parasitic capacitance. The coupling effect degrades the high frequency performance because C_{ds} induces unequal charges in the comparison cycles, which results in a dynamic offset. Therefore, two cross-coupled metal-oxide-metal (MOM) capacitors (around 5fF) are used to neutralize the effect (see Figure 2-17(b)). The two cross-coupled capacitors reduce the coupling effect to

less than 1/2 LSB (2.5fF) in the 10-bit case under processing variation. To achieve higher precision, dummy switches and dummy routing are alternative solutions to reduce the coupling effect.

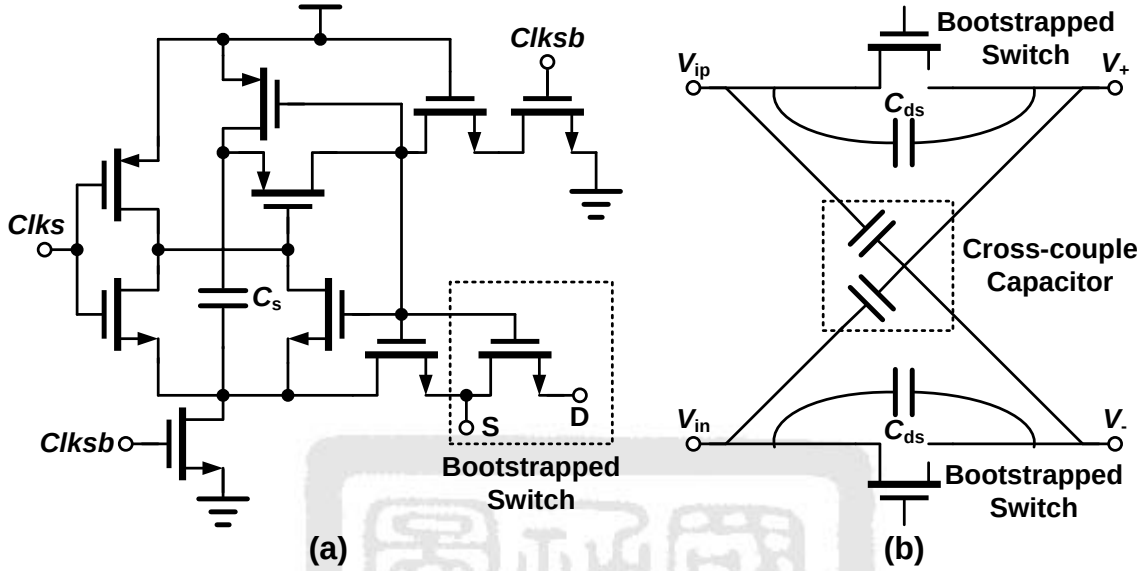


Figure 2-17 (a) Bootstrapped switch. (b) Cross-coupled capacitors.

2.3.2 Dynamic Comparator with a Current Source

Figure 2-18 shows a schematic of the comparator. During the conversion phase, the input voltages of the comparator approach ground. For the proper function within the input common-mode voltage range from half V_{ref} to ground, the comparator uses a p-type input pair. Because a dynamic comparator does not consume static current, it is suitable for energy efficient design.

When *Clkc* is high, the comparator outputs Out_p and Out_n are reset to high. When *Clkc* goes to low, the differential pair, M_1 and M_2, compares the two input voltages. Then, the latch regeneration forces one output to high and the other to low according the comparison result. Consequently, the *Valid* signal is pulled to high to enable the asynchronous control clock. The offset voltage of this comparator can be expressed as [24]:

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right) \tag{2-8}$$

where $\Delta V_{TH1,2}$ is the threshold voltage offset of the differential pair M_1 and M_2, $(V_{GS}-V_{TH})_{1,2}$ is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension mismatch between M_1 and M_2, and ΔR is the loading resistance mismatch induced by M_3-M_6. The first term is a static offset which does not affect the performance of a SAR ADC. However, the second term is a signal-dependent dynamic offset. The effective voltage of the input pair varies with the input common-mode voltage. The dynamic offset degraded the performance of the work in Section 2.2.

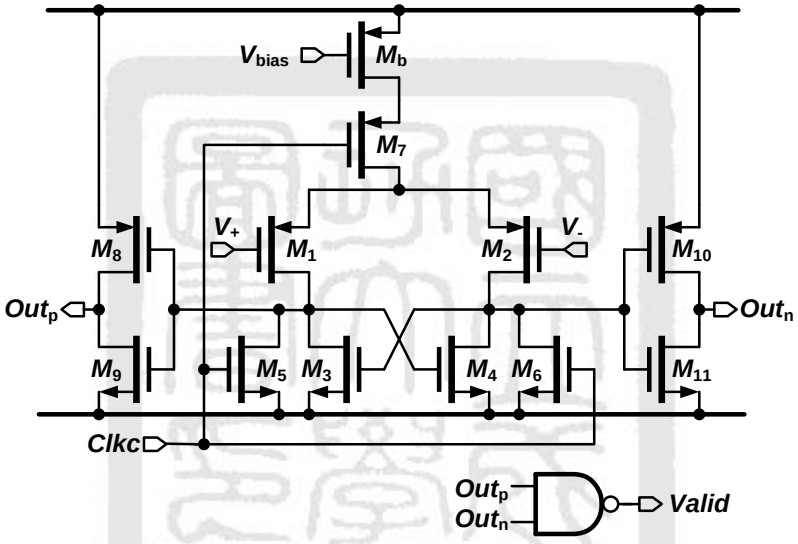


Figure 2-18 Dynamic comparator with a current source.

There are several possible approaches to improve the dynamic offset. The comparator size can be enlarged, which results in larger power consumption. The effective voltage of the input pair can be reduced, but this decreases the comparison speed. The error tolerant non-binary search algorithm [3] is also a feasible method. A simple and reliable way is to cascode a biased MOS (M_b) at the top of the switch MOS (M_7), as shown in Figure 2-18. Because M_b is in the saturation region, the change of its drain-source voltage has only a slight influence on the drain current. Hence, M_b keeps the effective voltage of the input

pair near a constant value when common-mode voltage changes. The dynamic offset thus has a minor influence on the conversion linearity.

2.3.3 SAR Control Logic

To avoid a high frequency clock generator, an asynchronous control circuit is used to internally generate the necessary clock signals. Figure 2-19 shows a schematic and a timing diagram of the asynchronous control logic. The dynamic comparator generates the *Valid* signal. *Clks* is the control signal of the sampling switches which turns on these switches at high potential and turns off the switches at low potential. The sampling phase is about 20% of the whole clock period. *Clkc* is the control signal of the dynamic comparator. Clk_1 to Clk_{10} sample the comparator output and trigger the control logic.

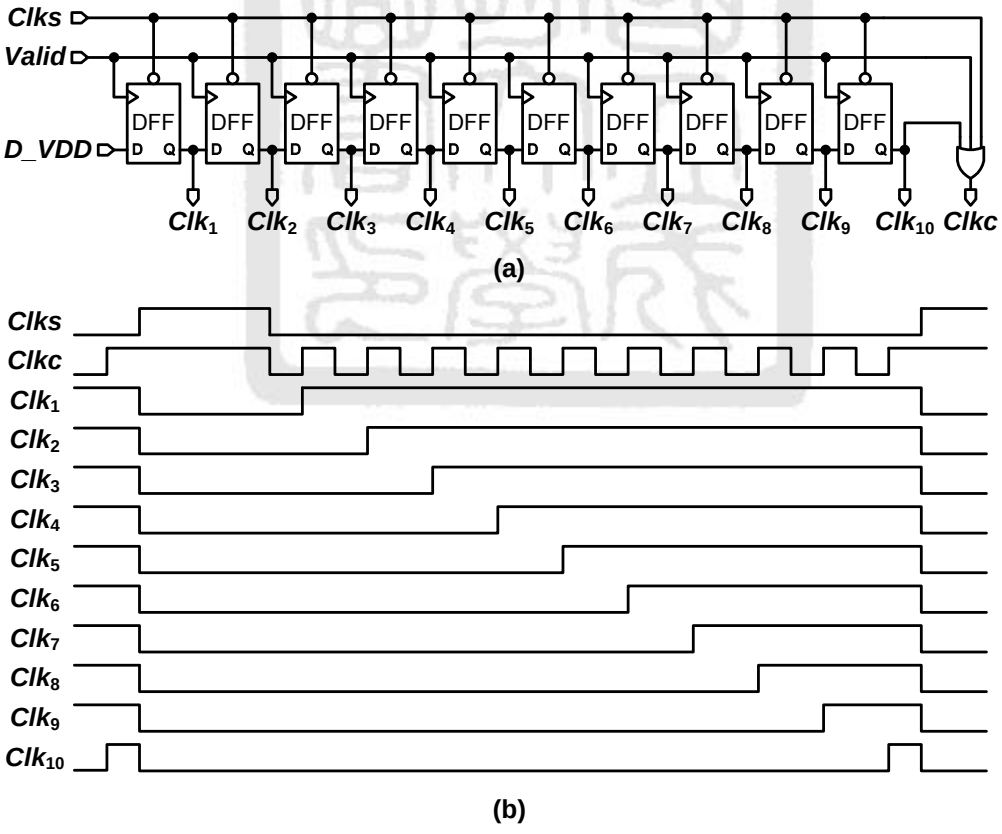


Figure 2-19 Asynchronous control logic: (a) Schematic. (b) Timing diagram.

2.3.4 Unit Capacitor

The first prototype used MIM capacitors while this revised work uses MOM capacitors to construct the capacitor array. Figure 2-20(a) shows a sandwich capacitor [8], where the gray part is the top plate. The bottom plate encloses the top plate to minimize the parasitic capacitance. The capacitor consists of only three metals, yielding a small capacitance per unit area. For a SAR ADC, capacitors occupy most of the area. Therefore, increasing the unit capacitance greatly improves the area efficiency.

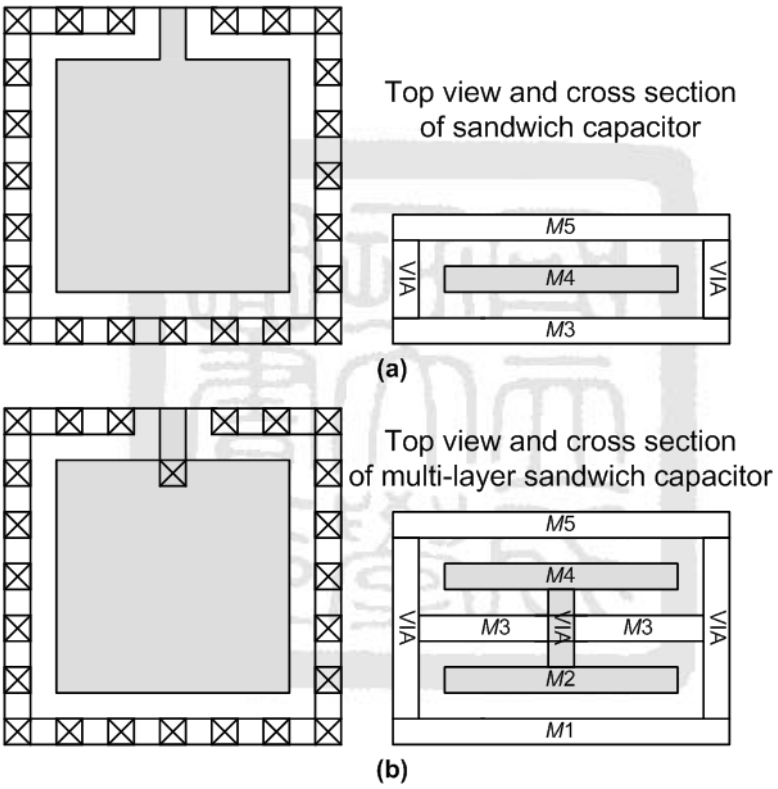


Figure 2-20 (a) Sandwich capacitor. (b) Multi-layer sandwich capacitor.

Figure 2-20(b) shows a multi-layer sandwich capacitor which doubles the effective capacitor area. The capacitance of a unit multi-layer sandwich capacitor (3.3 μm × 3.3 μm) is about 4.8 fF while that of a sandwich capacitor of the same size is only 2.4 fF. Therefore, the multi-layer sandwich capacitor is much more hardware efficient. The binary capacitor array of the proposed 10-bit SAR ADC uses 2^9 unit capacitors. Therefore, the total

sampling capacitance of one capacitor network is 2.5 pF. The two capacitor networks occupy a total active area of 195 μm × 195 μm, about 72% of the whole ADC.

2.3.5 Measurement Results

The prototype ADC was fabricated in TSMC 0.13-μm 1P8M triple well CMOS technology. The full micrograph and the zoomed-in view of the core are shown in Figure 2-21. The total area of the chip is 0.93 mm × 1.03 mm, with the ADC core taking up only 195 μm × 265 μm. The switches for capacitors are placed close to the capacitor arrays. In this improved work, the logic control circuit has been optimized for power consumption and area, and the layout of the digital logic circuit is more compact. Therefore, the core area is smaller than that of the first prototype. An on-chip 100-Ω resistor is placed between the differential input ports to match the 50-Ω resistance of the signal cable. The measurement results of the prototype are presented below.

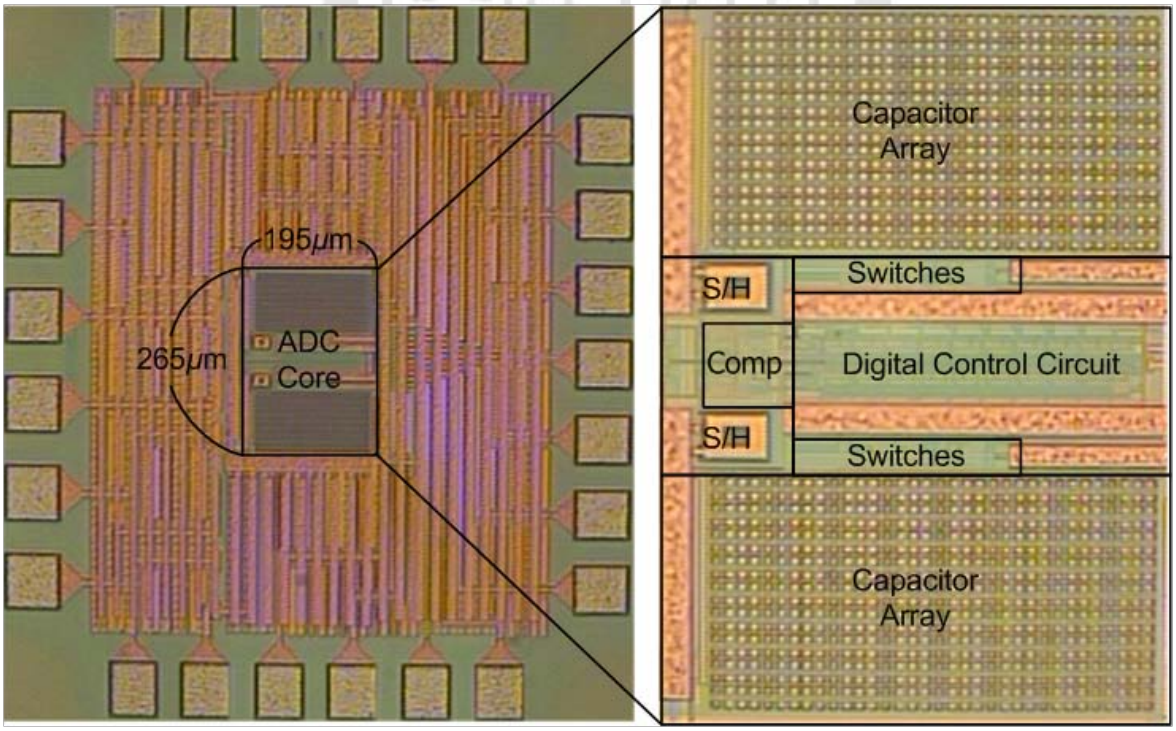


Figure 2.21 Die micrograph and the zoomed view.

At a 1.2-V supply and a 50-MS/s sampling rate, the measured DNL and INL are shown in Figure 2-22. The peak DNL and INL are +0.91/-0.63 LSB and +1.27/-1.36 LSB, respectively. The figure shows that the INL has a jump at the middle of output codes. Since each test chip has this characteristic, the parasitic capacitance induced by the layout routing might be responsible for this inference. The MSB capacitance is around one LSB larger than the expected value. The performance of the ADC is mainly limited by this deterministic capacitor mismatch.

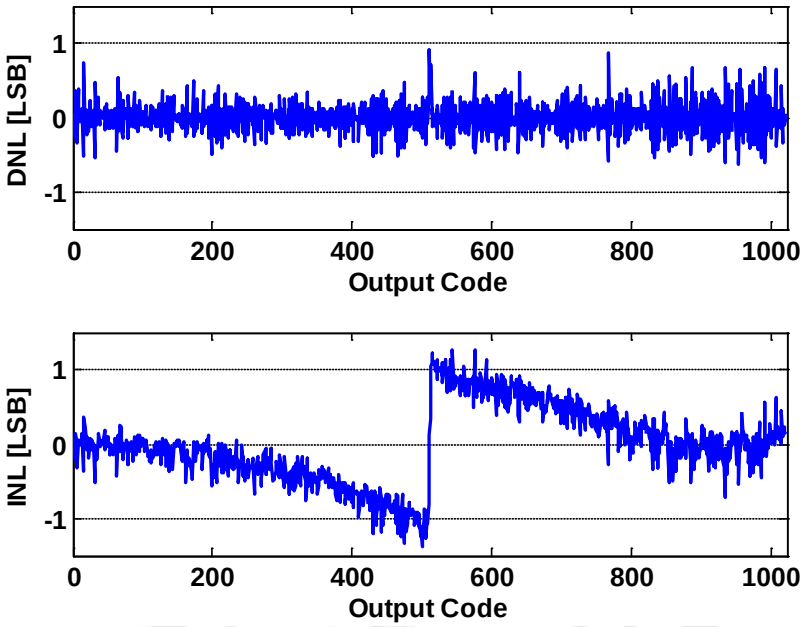


Figure 2-22 Measured DNL and INL.

Figure 2-23 shows the measured FFT spectrum with an input frequency of close to 10 MHz at a 1.2-V supply and a 50-MS/s sampling rate. The measured SNDR and SFDR are 56.5 dB and 64.6 dB, respectively. Figure 2-24 plots the measured SNDR, SNR, SFDR, THD, and ENOB values versus the input frequency at 50 MS/s. At low input frequency, the measured SNDR and SFDR are 57.0 dB and 65.9 dB, respectively. The resultant ENOB is 9.18 bits. When the input frequency was increased to 50 MHz, the measured SNDR and SFDR were 54.4 dB and 61.8 dB, respectively. The ERBW is higher than 50 MHz.

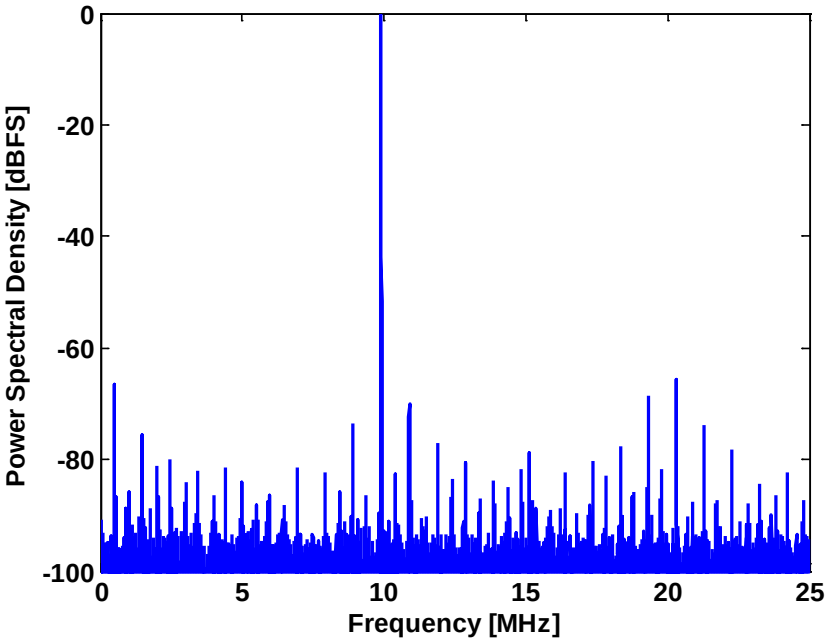


Figure 2-23 Measured FFT spectrum at 50 MS/s with a 10-MHz input frequency.

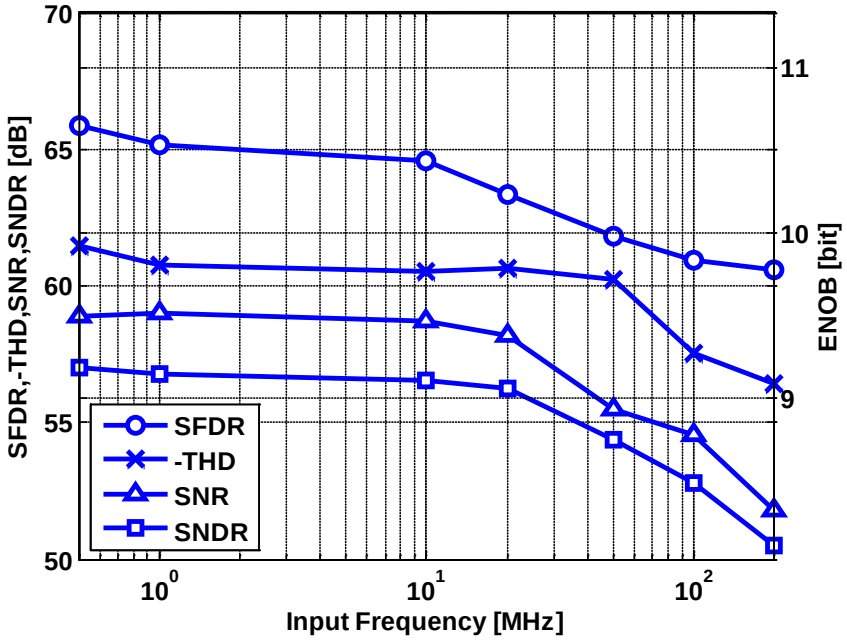


Figure 2-24 Measured performance versus input frequency at 1.2 V and 50 MS/s.

Figure 2-25 shows the measured performance versus the sampling frequency with a 0.5-MHz sinusoidal stimulus. When the sampling rate was 60 MS/s, the ENOB was still close to 9 bits. Further increasing the sampling rate rapidly degraded the performance because the conversion time was insufficient.

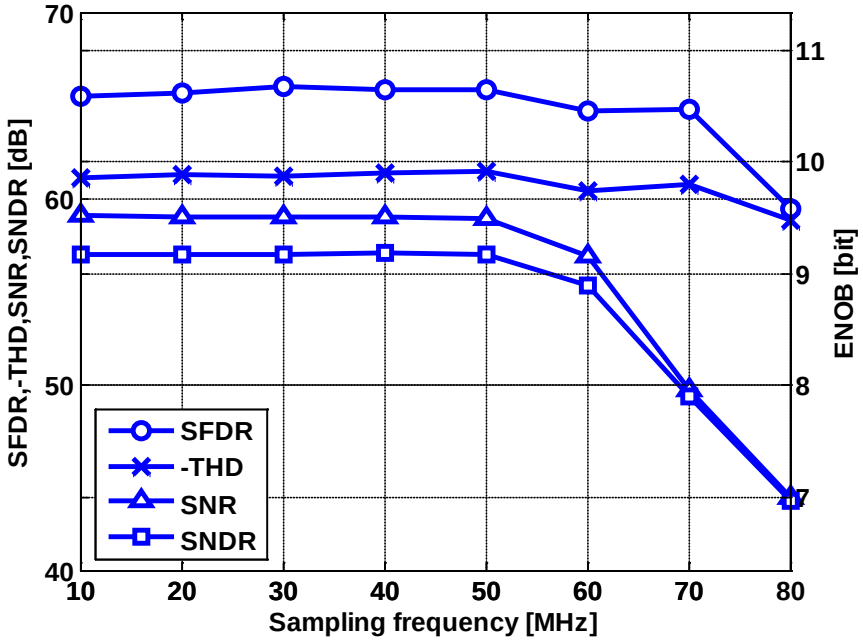


Figure 2-25 Measured dynamic performance versus sampling frequency.

At a 1.2-V supply, the analog part, including the S/H circuit and comparator, consumes 0.276 mW, and the digital control logic draws 0.42 mW. The ideal power consumption of the reference voltage V_{ref} is

$$P(V_{ref}) = \frac{E_{avg,n-bit}}{T} = f \bullet \sum_{i=1}^{n-1} (2^{n-2-i}) C V_{ref}^{\ 2} \qquad (2\text{-}9)$$

At a 1-V reference voltage, a 50-MS/s sampling rate, and a 4.8-fF unit capacitance, the expected power consumption is 0.062 mW. The measured value was 0.13 mW because the switch buffers consume dynamic current during transitions. The parasitic capacitors at the bottom plates and the drains of the switch MOS transistors also increase power consumption. Excluding the output buffers, the total power consumption of the active circuit is 0.826 mW. A summary of the ADC is listed in Table 2-4.

Table 2-4 Summary of ADC Performance

Specification (Unit)	Experimental Result
Supply Voltage (V)	1.2
Input CM Voltage (V)	0.6
Input Range (V_{p-p})	2
Sampling Capacitance (pF)	2.5
Sampling Rate (MS/s)	50
Active Area (mm^2)	0.052
DNL (LSB)	+0.91 / -0.63
INL (LSB)	+1.27 / -1.36
SNDR/SFDR (dB)	57.0 / 65.9 (0.5 MHz)
	56.5 / 64.6 (10 MHz)
	54.4 / 61.8 (50 MHz)
ENOB (bits)	9.18 (0.5MHz)
ERBW (MHz)	50
Power (mW)	0.826

Because the ADC has no transmission gates or preamplifiers, it can operate at low supply voltage conditions. At 40 MS/s and a 1-V supply, the low frequency ENOB is 9.15 bits and the ERBW is around 50 MHz. At 20 MS/s and a 0.8-V supply, the low frequency ENOB is 9.19 bits and the ERBW is around 20 MHz. When the sampling rate and supply voltage were decreased to 10 MS/s and 0.6 V, respectively, the low frequency ENOB and ERBW were 8.91 bits and 20 MHz. Figure 2-26 plots the performance versus input frequency at 0.6 V. Table 2-5 shows a performance summary for various supply voltages. The excellent low-voltage performance demonstrates that the proposed ADC is a feasible alternative to switched-operational-amplifier pipelined ADCs [25].

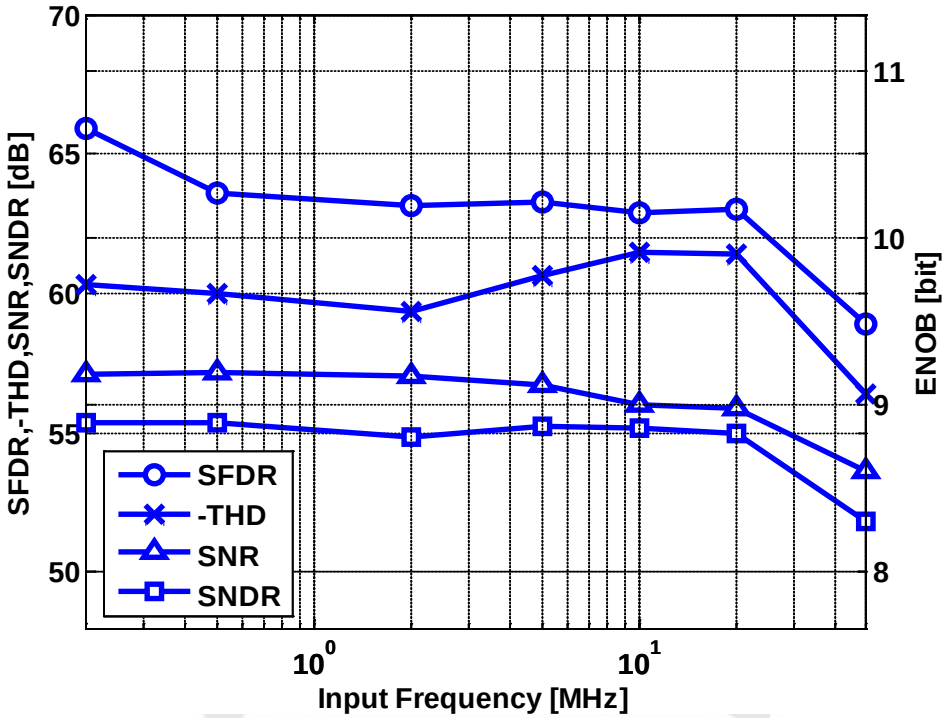


Figure 2-26 Measured performance versus input frequency at 0.6 V and 10 MS/s.

Table 2-5 Specification Summary at Different Supply Voltages

Specification (Unit)	Experimental Result			
Supply Voltage (V)	1.2	1.0	0.8	0.6
Input CM Voltage (V)	0.6	0.4	0.3	0.2
Input Range (V_{p-p})	2	1.6	1.2	0.8
Sampling Rate (MS/s)	50	40	20	10
ERBW (MHz)	50	50	20	20
ENOB (bits)	9.18	9.15	9.19	8.91
Power (mW)	0.826	0.496	0.154	0.046
FOM (fJ/Conv.-step)	29	22	13	9.6

The FOM of the proposed ADC is 29 fJ/conversion-step at 50 MS/s and a 1.2-V supply. The FOM is 9.6 fJ/conversion-step when the sampling rate and supply voltage are 10 MS/s and 0.6 V, respectively. Table 2-6 compares the proposed ADC with other state-of-the-art ADCs. Although the proposed ADC was fabricated in older technology, it still has the lowest FOM and smallest active area compared to those ADCs with similar sampling rates and resolutions.

Table 2-6 Comparison to State-of-the-Art Works

Specifications	*ISSCC*'07 [1]	*ISSCC*'08 [2]	*ISSCC* '10 [13]	First Prototype	This Work
Architecture	SAR	SAR	SAR	SAR	SAR
Technology	90 nm	90 nm	65 nm	0.13 μm	0.13 μm
Supply Voltage (V)	1	1	1.1	1.2	1.2
Sampling Rate (MS/s)	50	40	40	50	50
Resolution (bits)	9	9	10	10	10
ENOB (bits)	7.8	8.56	8.9	8.48	9.18
Power (mW)	0.7	0.82	1.21	0.92	0.826
FOM (fJ/Conv.-step)	65	54	65	52	29
Active Area (mm^2)	0.08	0.09	0.06	0.075	0.052

2.4 A 6-bit 220-MS/s Time-Interleaving SAR ADC

In digital data processing fields like hard disk drives and some local-area networks, a high sampling speed ADC is required in these applications where a 6-bit resolution is sufficient. This section shows a 6-bit asynchronous time-interleaved SAR ADC [26]. The sampling rate was enhanced by time-interleaving two slices. We use the time-interleaved architecture to avoid high frequency clock which will double the sampling rate. There are power and area overheads as the number of parallel converters increases. Therefore, a single ADC should be optimized for high speed, low power and small silicon area. This work was fabricated in a 0.18-μm 1P5M digital CMOS process. The ADC achieves a peak SNDR of 32.62 dB, while only occupies an active area of 240 μm × 130 μm and power consumption of 6.8 mW.

2.4.1 Architecture

Figure 2-27 shows a time-interleaving SAR ADC architecture composed of two sub-ADCs with the proposed monotonic switching procedure. Each sub-ADC needs two clock cycles to convert analog signal into digital signal. It takes half a clock cycle to sample and the remaining time is for successive approaching. The SAR logic block provides all the control signals which ensure the switches and the comparator working correctly, and provides control signals for the D/A converter capacitor network to implement the proposed switching sequence. It also generates the digital output code. The multiplexer is adopted to synchronize clock and two sub-ADCs' output data.

Figure 2-28 shows the schematic of the proposed SAR ADC. The fundamental building blocks of the SAR ADC are the comparator, S/H circuit, capacitor network, and successive approximation registers.

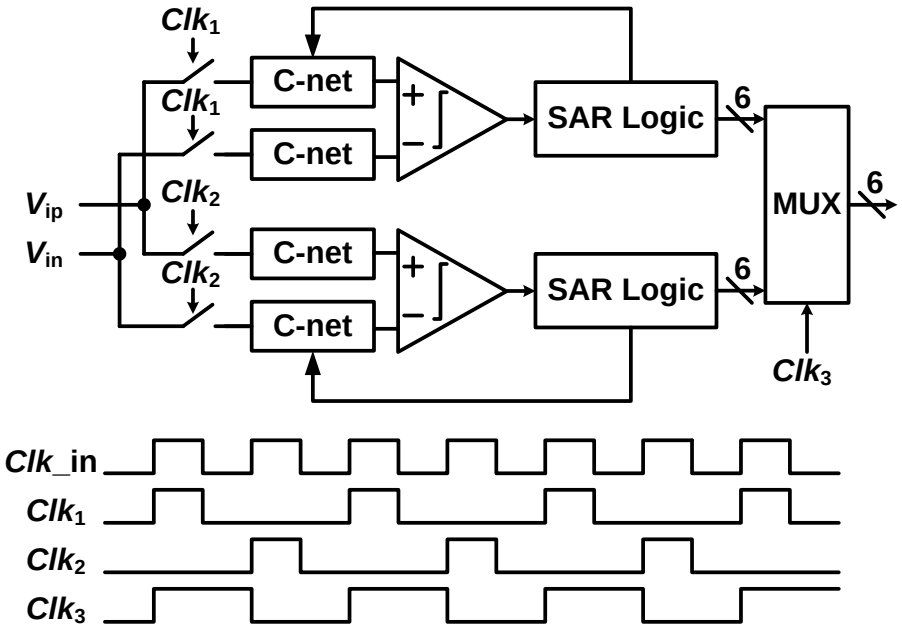


Figure 2-27 Timing diagram of the time-interleaving SAR ADC.

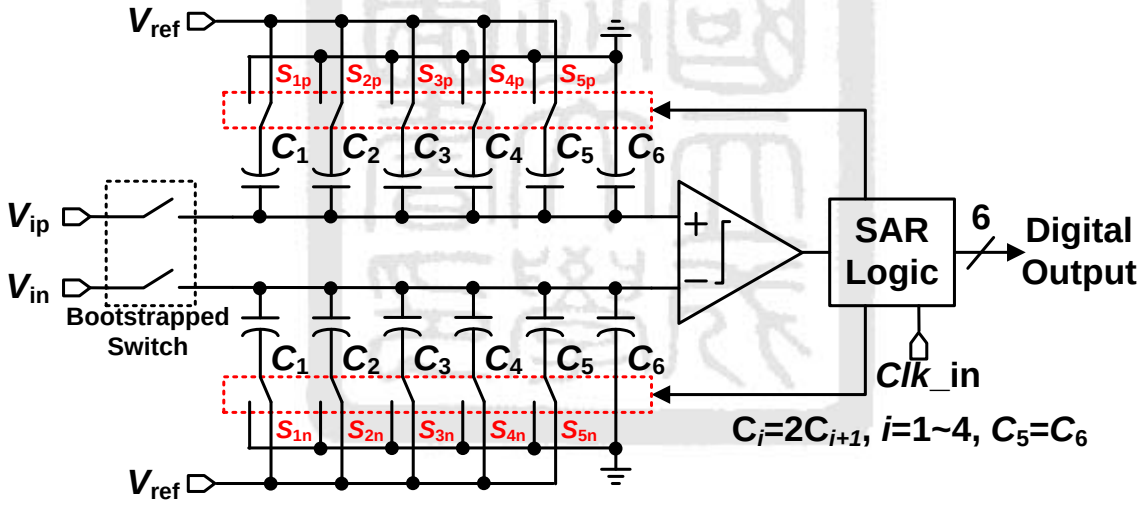


Figure 2-28 Architecture of a 6-bit single channel SAR ADC.

2.4.2 Comparator Design

Figure 2-29 shows the schematic of the comparator. When *Clkc* is high, the comparator outputs Out_p and Out_n are reset to high. When *Clkc* goes low, the differential pair M_1 and M_2 compares the voltage difference of V_+ and V_-. Because of latch regeneration, Out_p and Out_n go to high or low according by the input voltage. Then the *Valid* signal is pulled to high to enable the asynchronous clock. In order to reduce the channel mismatch of two sub-ADCs, the offset voltages of each comparator are designed to be less than 1/6 LSB. The layout is carefully done by using the common-centroid technique. In addition, when the comparator is in steady-state, there is no dc current flowing from V_{DD} to ground. Therefore, it is suitable for low power application.

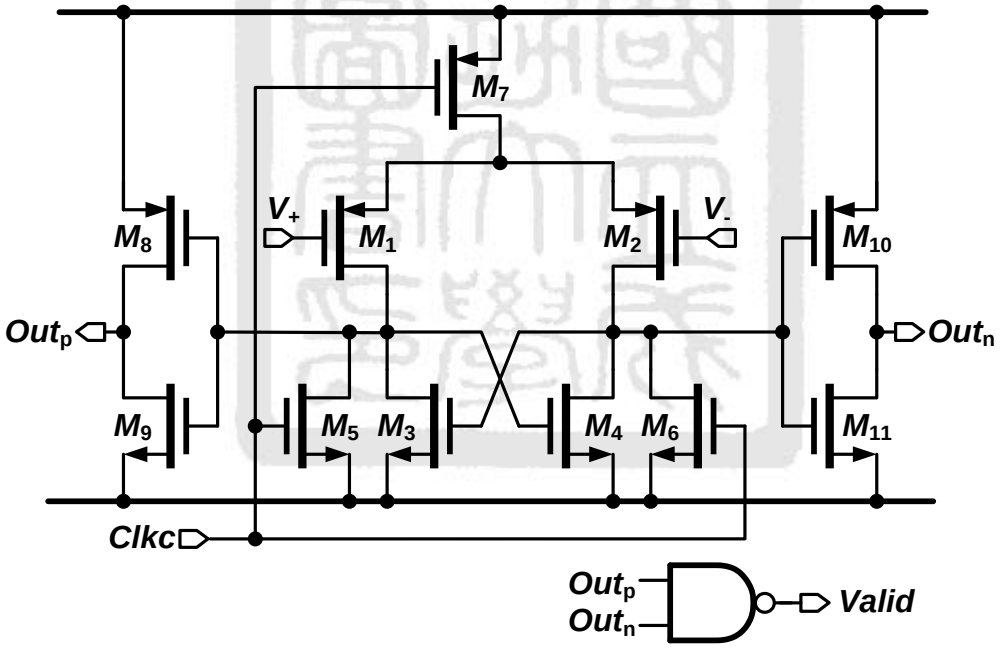


Figure 2-29 Schematic of the comparator.

2.4.3 SAR Control Logic

Figure 2-30 shows the SAR controller which samples the digital output codes from the comparator and provides control signals for the DAC capacitor network to implement the

monotonic switching sequence.

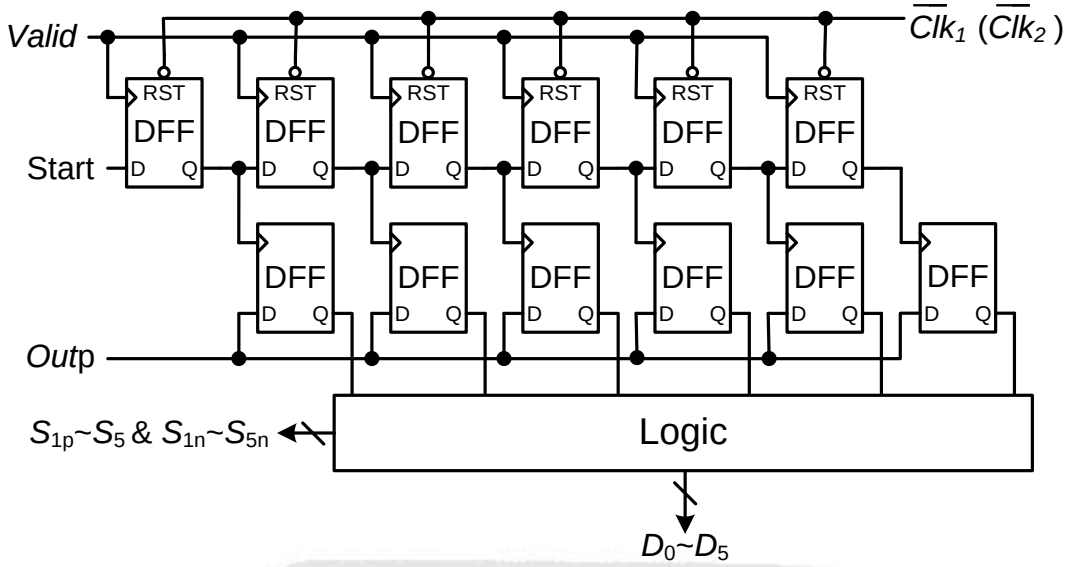


Figure 2-30 The SAR logic implementation.

2.4.4 Unit Capacitor

As process scales, the accuracy of interconnect metal patterns improve, making it possible to realize highly matched, very small value capacitors using interconnect metals. In this ADC, the capacitor is a low-cost MOM finger sandwich capacitor available in any standard digital CMOS process instead of a higher quality MIM capacitor.

Figure 2-31(b) shows the structure of the proposed finger-sandwich capacitor, which combines finger capacitor and sandwich capacitor [8]. The unit capacitor is composed of metal 1 to metal 5. The gray part is the top plate, which is almost encaged by the bottom plate that minimizes the parasitic capacitor.

The capacitance of a unit finger-sandwich capacitor (5μm × 5μm) is 10 fF while that of a sandwich capacitor as shown in Figure 2-31(a) with the same size is only 2.8 fF. Therefore, the proposed finger sandwich capacitor is very hardware efficient. The binary

capacitor array of the proposed 6-bit ADC needs 32 unit capacitors, and the total input capacitance of the capacitor network is 320 fF. A single capacitor array occupies only 100 μm × 50 μm which is about 16.7% of the layout core area.

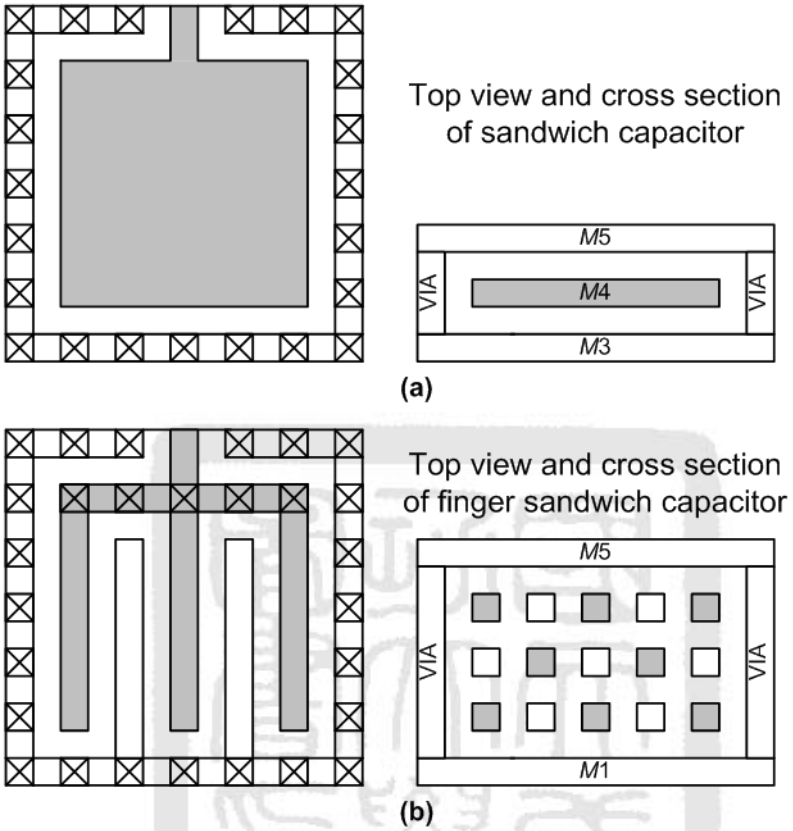


Figure 2-31. Unit capacitor structure: (a) sandwich capacitor (b) finger sandwich capacitor.

2.4.5 Layout and Floorplan

The layout of the SAR ADC and the floorplan of ADC core are shown in Figure 2-32 and Figure 2-33, respectively. To achieve high-speed operation and reduce power consumption, it is crucial to minimize layout parasitic, which requires the layout to be as compact as possible. The chip occupies 0.57 mm × 0.41 mm and the ADC core (the major circuit without pad and output buffer) only occupies an active area of 240 μm × 130 μm.

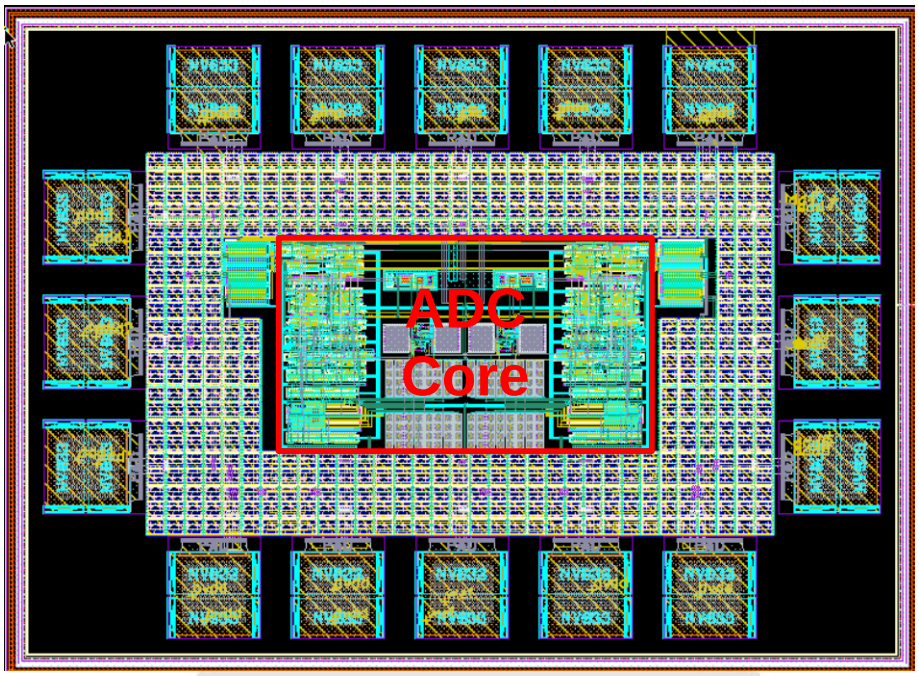


Figure 2-32 Layout of the implemented SAR ADC.

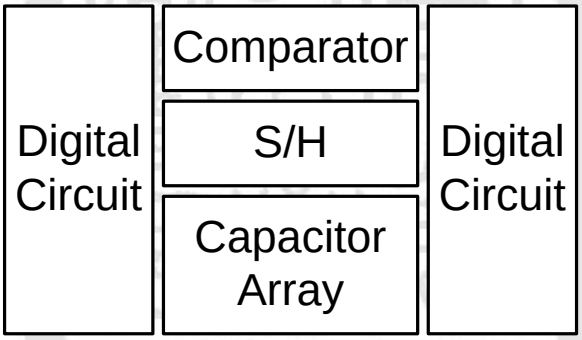


Figure 2-33 Floor plan of ADC core.

2.4.6 Measurement Results

The proposed ADC is fabricated in TSMC 0.18-μm 1P5M digital CMOS technology with MOM capacitors. At 1.8-V supply and 220-MS/s sampling rate, the measured DNL and INL are shown in Figure 2-34. The measured peak DNL and INL are +1.15/-0.88 LSB and +0.75/-1.05 LSB, respectively.

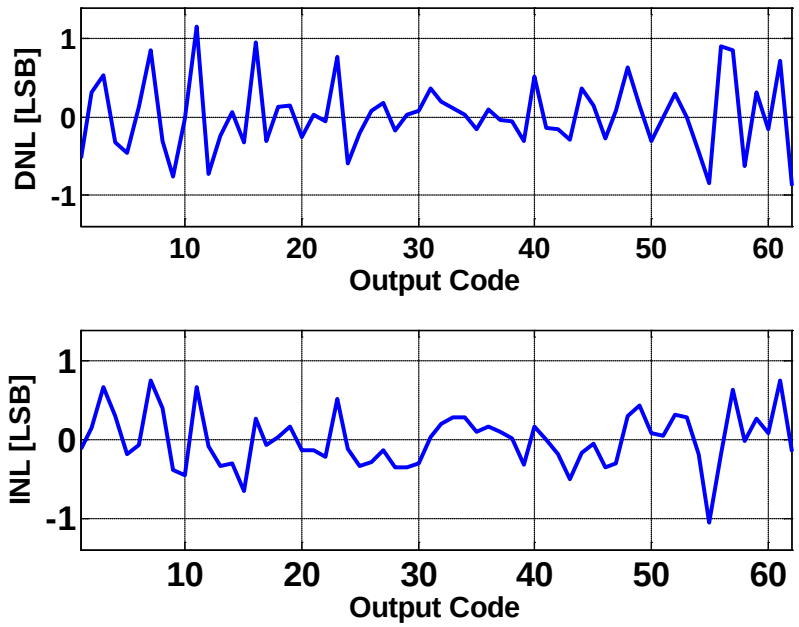


Figure 2-34 Measured INL and DNL.

Figure 2-35 shows the measured FFT spectrum with an input frequency of 2 MHz at a 1.8-V supply and a 220-MS/s sampling rate. The measured SNDR and SFDR are 32.62 dB and 48.96 dB, respectively. The ENOB is 5.13 bits.

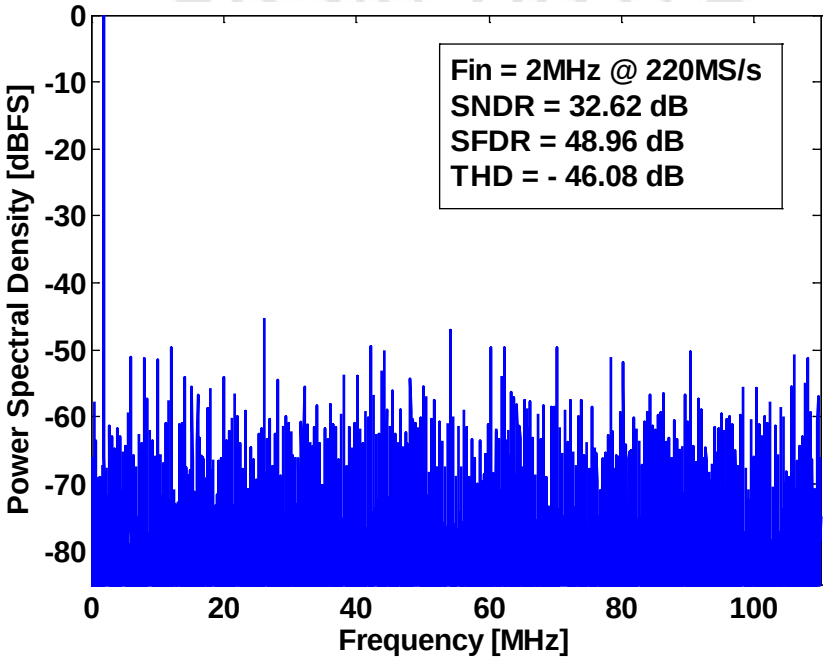


Figure 2-35 Measured FFT spectrum at 220 MS/s with a 2-MHz input frequency.

Figure 2-36 plots the measured SNDR, SFDR values versus the input frequency at 220 MS/s. At 200-MHz input signal frequency, the peak SNDR and peak SFDR are 30.25 dB and 42.56 dB, respectively. The resultant ENOB is 4.73 bits. The ERBW is higher than 200MHz.

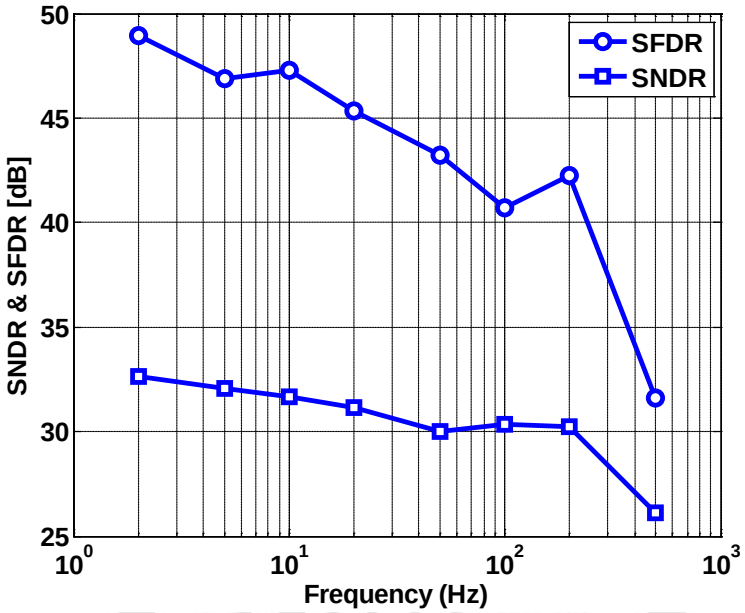


Figure 2-36 Measured performance versus input frequency at 1.8 V and 220 MS/s.

The power dissipation consumed by analog circuits including the comparator, T/H circuit and capacitor network is 0.84 mW. The digital power consumption (clock generator and successive approximation register logic) is 5.96 mW. The total power dissipation of this ADC is 6.8 mW. The performance of this ADC is summarized in Table 2-7.

Table 2-8 summarizes the comparison with the other ADCs with sampling rates in excess of 100 MS/s and resolutions of 8-bit or less. The result shows that our work is more power efficient than the previous publications. This ADC is fabricated in a digital process without MIM capacitor, and the core area of the ADC is pretty small. The fabrication cost is reduced obviously. In addition, this work requires no digital post-processing or post-calibration between two sub-ADC channels.

Table 2-7 Summary of ADC Performance

Specification (Unit)	Experimental Result	
Resolution (bit)	6	
Supply Voltage (V)	1.8	
Conversion Rate (MS/s)	220	
Input Range (V_{p-p})	2	
SNDR/SFDR (dB)	32.62 / 48.96 (2 MHz)	
	31.17 / 45.34 (20 MHz)	
	30.25 / 42.56 (200 MHz)	
DNL (LSB)	+1.15 / -0.88	
INL (LSB)	+0.75 / -1.05	
FOM (pJ/Conversion-step)	0.88	
ERBW (MHz)	200	
Power (mW)	Analog	0.84
	Digital	5.96
	Total	6.8
Active area (μm^2)	240 × 130	
Chip area (μm^2)	570 × 410	

Table 2-8 Comparison to the Other Works

Specifications	*JSCC*'07 [7]	*JSCC*'07 [12]	*ISSCC* '04 [27]	This Work
Technology	0.18 μm	65 nm	0.18 μm	0.18 μm
Supply Voltage (V)	1.8	1.2	1.8	1.8
Resolution (bits)	5	5	8	6
Convertion Rate (MS/s)	500	500	150	220
Input Range (V_{p-p})	0.8	0.8	1.6	2
Power (mW)	7.47	5.93	71	6.8
SNDR (dB)	20.2	27.8	45.4	32.62
SFDR (dB)	24	36	52.5	48.96
ENOB (bits)	3.06	4.04	7.25	5.13
FOM (pJ/Conv.-step)	1.8	0.75	2.5	0.88
Core Area (mm^2)	0.5	0.91	1.8	0.031

2.5 Summary

In this chapter, an efficient capacitor switching procedure for SAR ADCs was presented. The proposed switching procedure leads to both lower switching energy and smaller total capacitance. It also simplifies the digital logic control circuit. The switching method also improves the settling speed of the DAC capacitor network. Three works are designed to demonstrate power and hardware efficiency of the proposed method.

In work I, the prototype ADC demonstrated the effectiveness of the monotonic switching scheme. However, the signal-dependent offset caused by the variation of the input common-mode voltage degraded ADC linearity. In work II, the revised prototype of work I, a biased comparator was proposed to reduce the dynamic offset induced by input common-mode voltage variation. The improved comparator design avoids the linearity degradation. In addition, an asynchronous control circuit is used to internally generate the necessary clock signals to avoid a high frequency clock generator. Moreover, a hardware-efficient multi-layer sandwich capacitor implemented with normal metal layers was proposed to reduce the area of the capacitor network. In work III, the prototype using asynchronous processing and time interleaved technique achieves excellent power efficiency. In addition, a hardware-efficient finger sandwich capacitor was proposed to construct the capacitor network.

The experiment results of the three works demonstrate the power and hardware efficiency and also the high-speed potential of the proposed SAR ADC.

Chapter 3
Binary-Scaled Error Compensation Method for High-Speed SAR ADC

3.1 Introduction

In recent years, due to the improvements in CMOS technologies, medium resolution (8- to 10-bit) SAR ADCs have been able to achieve sampling rates of several tens of MS/s with excellent power efficiency and small area. When the sampling rate increases, the SAR ADCs suffer from settling issues. Take a 10-bit 100-MS/s SAR ADC as the example. When the sampling settling time, comparator active time and SAR logic delay are subtracted from each period, the DAC settling time has to be less than 0.4 ns in each bit cycle. Such a short time interval is not sufficient for the capacitive DAC to stabilize because the increasing interconnect line impedance in advanced processes slows down the charge transfer, especially in the longest routing path of the DAC capacitor network. Furthermore, the reference voltage sinks noise and line coupling also affects the settling. A non-binary SAR can tolerate DAC settling error at the cost of increased design complexity and hardware overhead [3]. We proposed a binary-scaled error compensation technique to overcome the settling issue in high-speed SAR ADC [28].

3.2 The proposed Binary-Scaled Error Compensation Method

3.2.1 Conventional Binary Search

Analog-to-digital conversion is to find a correct digital representation for an analog signal. An analog signal always locates between two digital codes. For a correct conversion, the difference between the analog signal and digital representation should be less than 1 LSB. If the difference is larger than 1 LSB, there are some errors happened during the conversion. Figure 3-1(a) shows an example of a binary search SAR ADC. This is a 4-bit case. Hence, it has sixteen quantization levels. V_i is the input signal and the bold line is the threshold. The comparator distinguishes the input signal is higher or lower than the threshold and generates one bit digital code. In the first bit cycle, the input signal is lower the threshold. Therefore, the MSB (B_1) is equal to 0. After the MSB is decided, the number of possible quantization levels is reduced from 16 to 8. The effective input range is reduced by a factor of 2. The ADC will repeat this procedure until the final bit is obtained. If the remaining bit cycling operations are all correct, we can get a correct digital output code. In this case, the digital output code is equal to 4.

If a wrong decision is made before the last cycle as shown in Figure 3-1(b), even the remaining decisions and their corresponding DAC switching are all correct, the difference between the input and reference in the last cycle is still larger than one LSB, resulting in the ADC performance degradation. There are many possible sources lead to the wrong decision. Small voltage difference may result in a wrong decision due to the comparator metastability issue. The thermal noise and supply noise may have influence on the comparison result. In SAR ADC, the capacitive DAC needs sufficient time to stabilize to convert a correct digital output code, as shown in Figure 3-2(a). When we increase the

sampling rate, the bit cycle time is decreased. The shorter time interval is not sufficient for a capacitive DAC to stabilize, and the incompletely settled DAC lead to a wrong decision. The DAC settling issue limits the operation speed of the SAR ADC especially in high resolution cases.

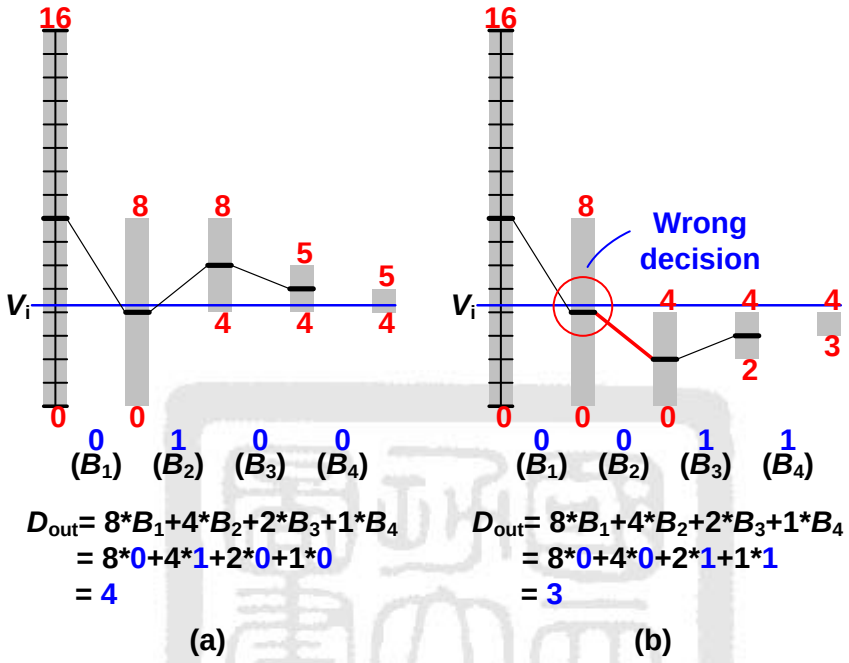


Figure 3-1 Conventional binary search: (a) Correct conversion. (b) Wrong conversion.

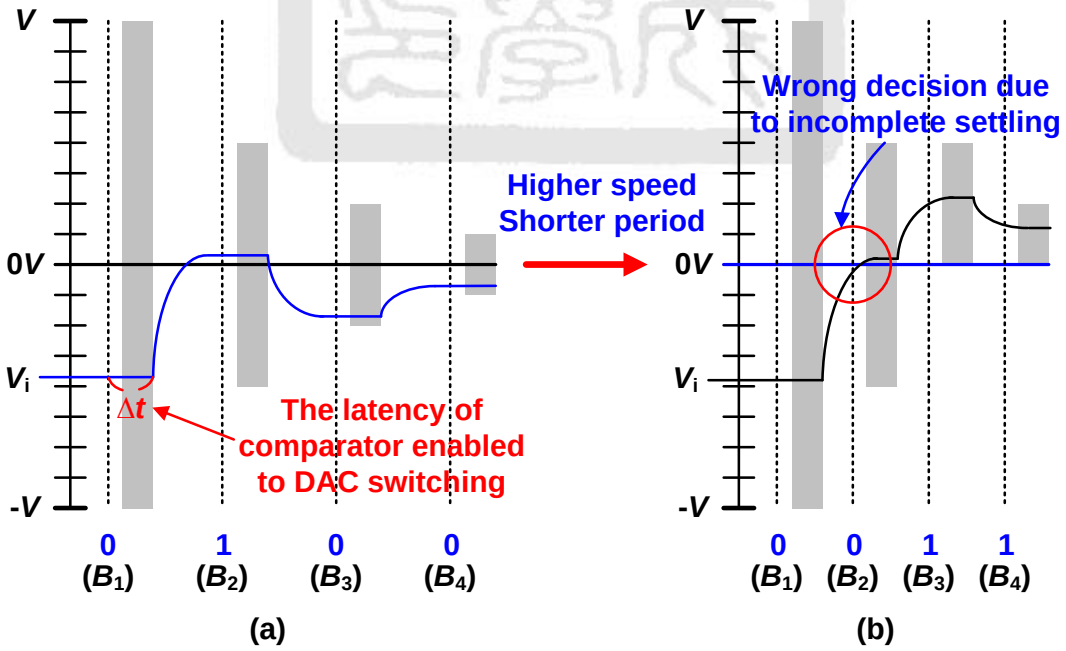


Figure 3-2 DAC settling: (a) Longer period. (b) Shorter period.

3.2.2 Non-binary Search

Figure 3-3 shows the concept of the non-binary search algorithm [3]. This is also a 4-bit case. The effective input range is reduced by a factor smaller than 2 after each bit cycling operation. For example, after the first bit cycling operation, the number of possible quantization levels is reduced from 16 to 9. Therefore, even a wrong decision happened during the conversion, if the remaining bit cycling operations are all correct, it is possible to get a correct digital output code at the cost of extra bit cycles. In this 4-bit example, it needs 5 bit cycles to complete the conversion.

The non-binary SAR ADC generates more decision levels. There are several digital codes for each input voltage. Hence, a certain range of error does not have influence on the conversion result. Therefore, the comparator can do comparison before the DAC is well settled. Though the non-binary SAR ADC needs extra bit cycles, the total conversion time still can be improved.

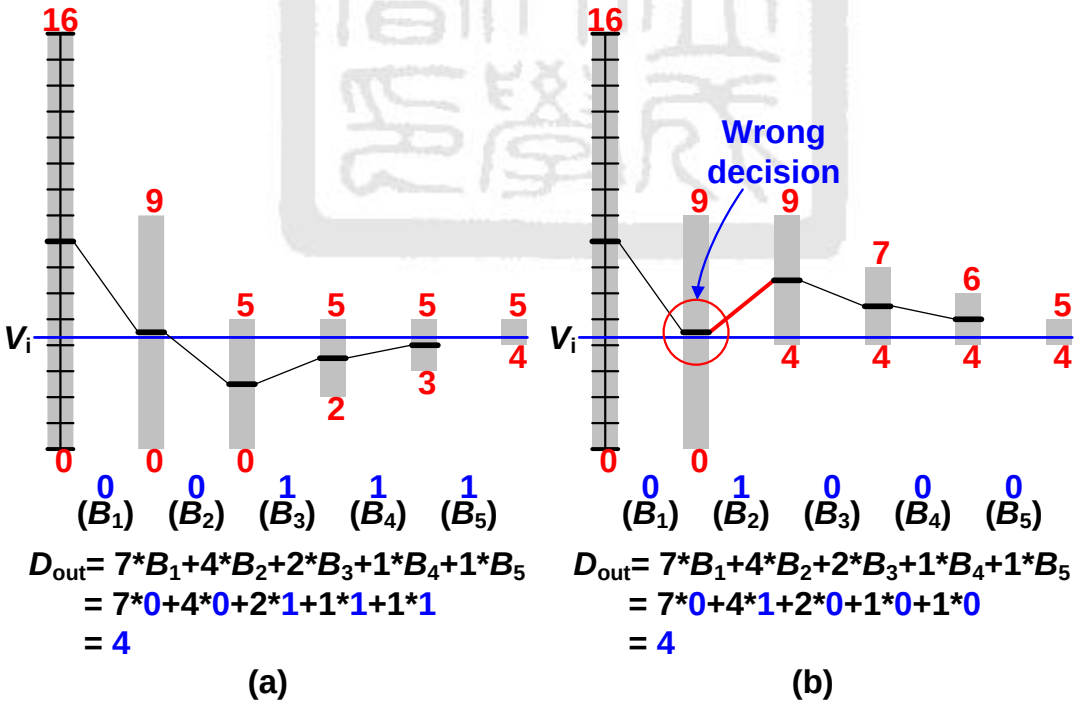


Figure 3-3 Non-binary search: (a) Correct conversion. (b) Conversion with wrong decision.

However, the non-binary search SAR ADC increases the design complexity and hardware overhead. It needs extra circuits – like ROM and arithmetical unit to correct the digital output code. Most important of all, the non-binary scaled is not favored in device matching for layout. It needs larger cell size to diminish the mismatch, and it may need calibration in high-resolution cases.

3.2.3 Proposed Binary Search with Error Compensation

Figure 3-4 shows the concept of proposed binary search with error compensation method. Like the binary search method, the effective input range is reduced by a factor of 2. But in some bit cycles, the input range does not reduce but shift to compensate for some DAC errors. Therefore, even a wrong decision happened during the conversion, it is still possible to get a correct digital output code. In this case, we added a compensative bit cycle to correct the wrong decision. The compensative level shift is equal to one LSB. If the compensative bit B_{3C} is equal to 1, the digital output adds 1. On the contrary, if the compensative bit is equal to 0, the digital output subtracts 1. Therefore, the output can be express as $D_{out}=8\times B_1+4\times B_2+2\times B_3+2\times(B_{3C}-0.5)+1\times B_4$. The wrong decision can be corrected by B_{3C}.

If there is no wrong decision happened during the conversion (Fig 3-4(a)), the digital output code is still the same as the case with wrong decision (Fig 3-4(b)). With the extra compensative bit cycles, there are multiple digital presentations for the same input voltage. Different output codes can lead to the same result. Therefore, the proposed ADC can tolerate a certain range of error. Fig 3-5 shows a DAC settling example of conventional and proposed methods. In a conventional SAR ADC, the comparator must do comparison after the DAC is well settled. Otherwise, it may lead to a wrong conversion result. In the proposed ADC, a certain range of error does not have influence on the conversion result. Hence, the comparator can do comparison before the DAC is well settled. Each bit cycle

time can be reduced. Although extra bit cycles are necessary, the total conversion time is still improved.

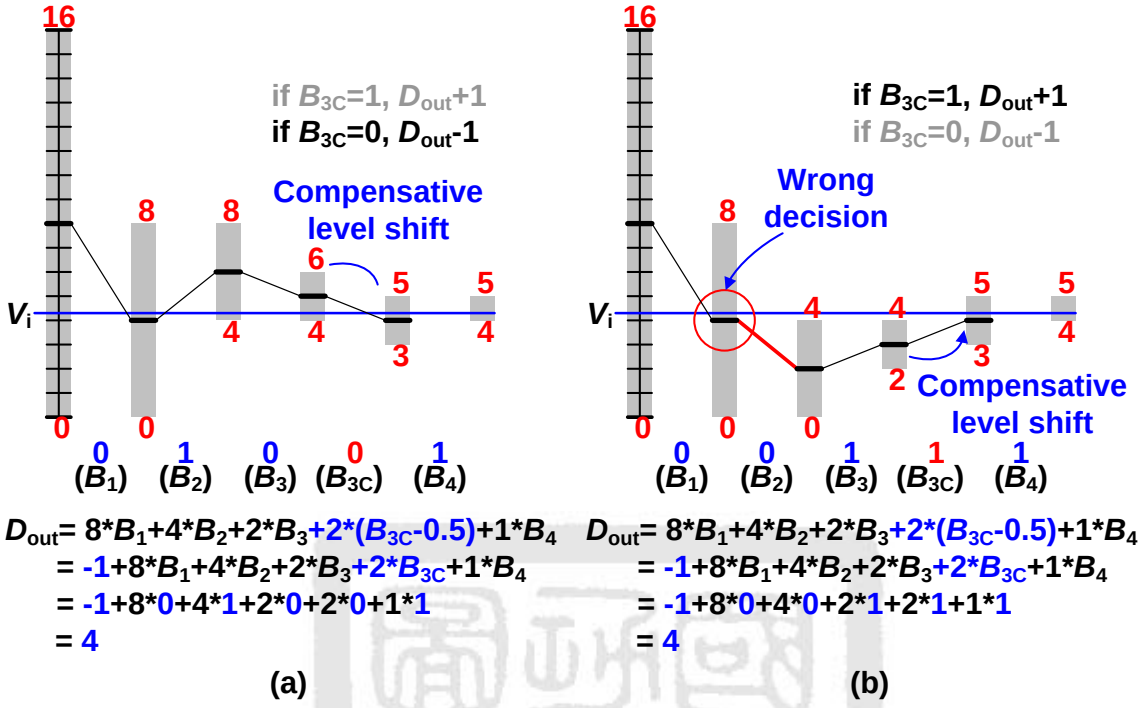


Figure 3-4 Binary search with error compensation: (a) Correct conversion (b) Conversion with wrong decision.

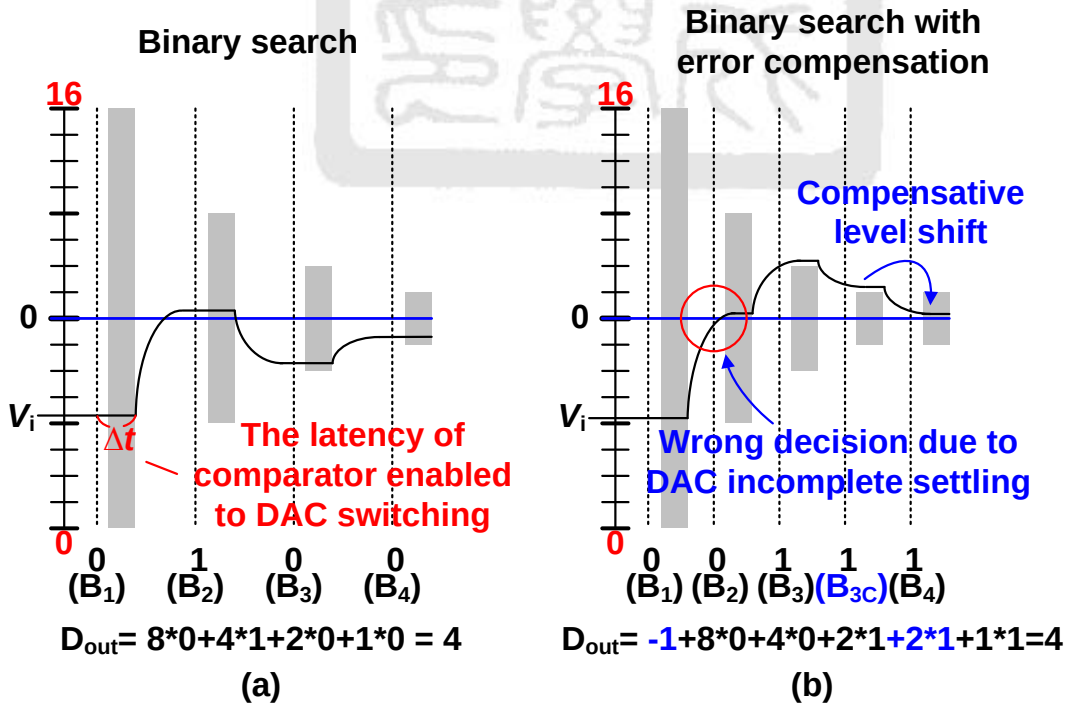


Figure 3-5 DAC settling: (a) Binary search. (b) Binary search with error compensation.

3.3 A 10-bit 100-MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation

3.3.1 Architecture

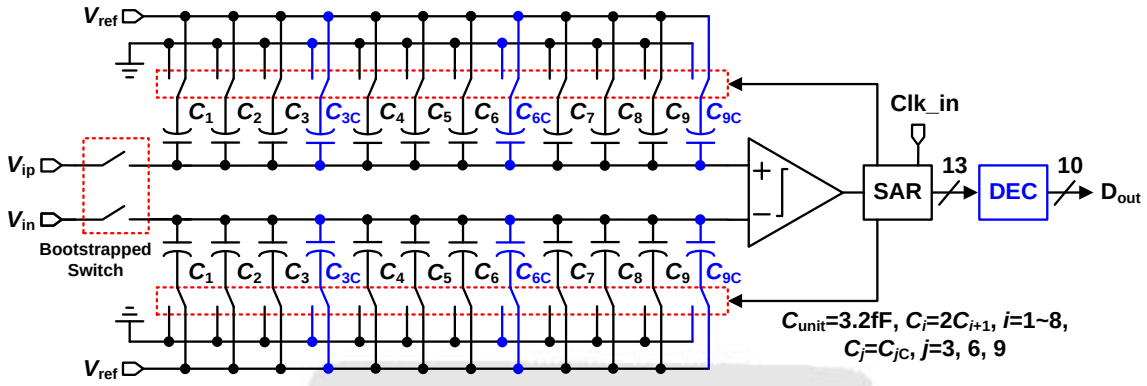


Figure 3-6 Block diagram of a 10-bit SAR ADC with binary-scaled error compensation.

For a conventional binary SAR ADC, if a termination capacitor with the same value as the LSB capacitor is added, the capacitance of the MSB capacitor would be equal to the sum of all LSB capacitors. Likewise, the capacitor MSB-1 is equal to the sum of all the remaining LSB capacitors. Based on the architecture (Figure 2-2) proposed in Chapter 2, we add three compensative capacitors (C_{3C}, C_{6C}, C_{9C}) and digital error correction circuit (DEC) to the ADC to perform the error compensation function.

When conversion starts, the input signals are sampled onto the top plates of the two capacitor arrays. Then, the comparator performs the first comparison. Without the three compensative capacitors, the voltage difference of the two DACs will add or subtract $V/2$, depending on the first comparison, where V is the maximum input amplitude. If the comparator makes the second decision at the moment the first DAC switching settles to 50% of its target value ($V/2\times1/2^1$), the maximum error is $V/2$ ($V/2\times1/2^1+V/4$), i.e., the incomplete settling value of the first DAC switching plus the second DAC switching. Because the maximum sum of the remaining voltage values is $V/4$ ($V/8+V/16+\ldots$), a

voltage of $V/4$ must be added to compensate for the error. If the comparator makes the second decision after the DAC settles to 75% of its target value, the maximum error is $3V/8$ ($V/2\times1/2^2+V/4$). A voltage of $V/8$ is required to compensate for the error. Binary-scaled capacitors are inserted in the original DAC network to provide compensative voltage values. In the proposed case, the SAR ADC with three compensative capacitors can tolerate settling error of at least 12.5% in each bit cycle. Note the precise error tolerance range depends on where the wrong decision occurs. The amplitude of the input signal swing is $V_{ref}\times(C_{1to9}/C_{total})$ where V_{ref} is the reference voltage range, C_{1to9} is the total capacitance of C_1 to C_9, C_{total} is the total capacitance including C_{1to9}, the three compensative capacitors and the parasitic capacitance at the comparator input terminal.

With the three compensative capacitors and digital error correction circuit, this ADC can tolerate at least 12.5% error in each bit cycle. With more compensative capacitors, the error tolerance ratio can be larger, the bit cycle time can be reduced, but it needs extra bit cycles. There is a tradeoff in adding how many compensative capacitors. According to simulation result, add three compensative cycles achieves the shortest conversion time. Therefore, we added three compensative capacitors in this ADC.

The binary search with error compensation SAR ADC has the same advantage as the non-binary architecture. It can tolerate a certain range of error during the conversion. The total conversion time can be improved even extra bit cycles added. The proposed binary search with error compensation method results in less design and hardware overhead. Most important of all, it is binary-scaled, which is favored in device matching for layout. Each bit weight only takes 1 bit digital code. Therefore, the digital correction circuit is simpler.

3.3.2 Digital Error Correction Logic

Figure 3-7 illustrates the digital error correction logic, which converts the 13-bit redundant codes to 10-bit binary codes. The bit weights of the 13-bit redundant codes are

512, 256, 128, 128, 64, 32, 16, 16, 8, 4, 2, 2, 1. The digital output can be expressed as $-(64+8+1)+(512\times B_1+256\times B_2+128\times B_3+128\times B_{3C}+\ldots)$. As shown in Figure 3-7, the digital output has an offset of 73, and the offset is removed by logic operation. Figure 3-8 shows the logic implementation of digital correction circuit, which consists of 5 inverters, 9 full adders, 1 half adder and 10 multiplexers. The half-adder is used to detect overflow. If the signal swing is over range, overflow occurs and the digital output will be set to either 0 or 1023 to keep the function normal.

The design of the other block circuits in the ADC is the same as that in Section 2.3. Therefore, we do not recapitulate the design of those block circuits here.

$$D_{out}= 512*B_1+256*B_2+128*B_3+128*(B_{3C}-0.5)+64*B_4+32*B_5+16*B_6 +16*(B_{6C}-0.5)+8*B_7+4*B_8+2*B_9+2*(B_{9C}-0.5)+1*B_{10}$$

$$= -73+512*B_1+256*B_2+128*B_3+128*B_{3C}+64*B_4+32*B_5+16*B_6 +16*B_{6C}+8*B_7+4*B_8+2*B_9+2*B_{9C}+1*B_{10}$$

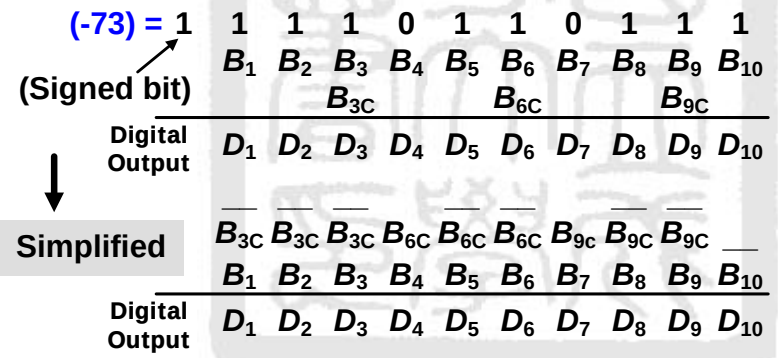


Figure 3-7 Digital error correction logic.

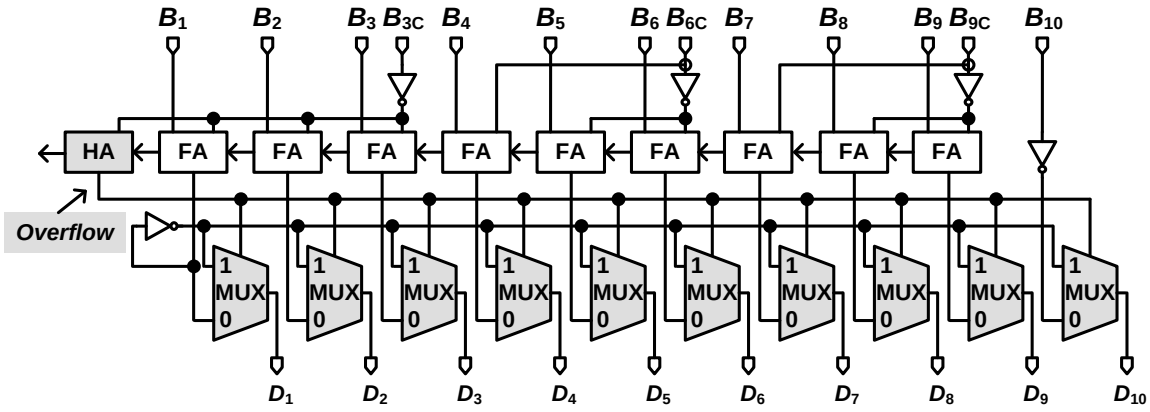


Figure 3-8 Implementation of digital error correction logic.

3.3.3 Measurement Results

The prototype is fabricated in a 1P6M 65nm low-leakage low-power CMOS technology with MOM capacitors. Figure 3-9 shows the chip micrograph and zoomed in view of the ADC core which occupies 155 μm × 165 μm. The digital error correction circuit only occupies 18 μm × 27 μm. We used multi-layer sandwich capacitor to construct the capacitor network. The unit capacitance is around 3.2 fF, and the total sampling capacitance of a single capacitor array is 1.86 pF.

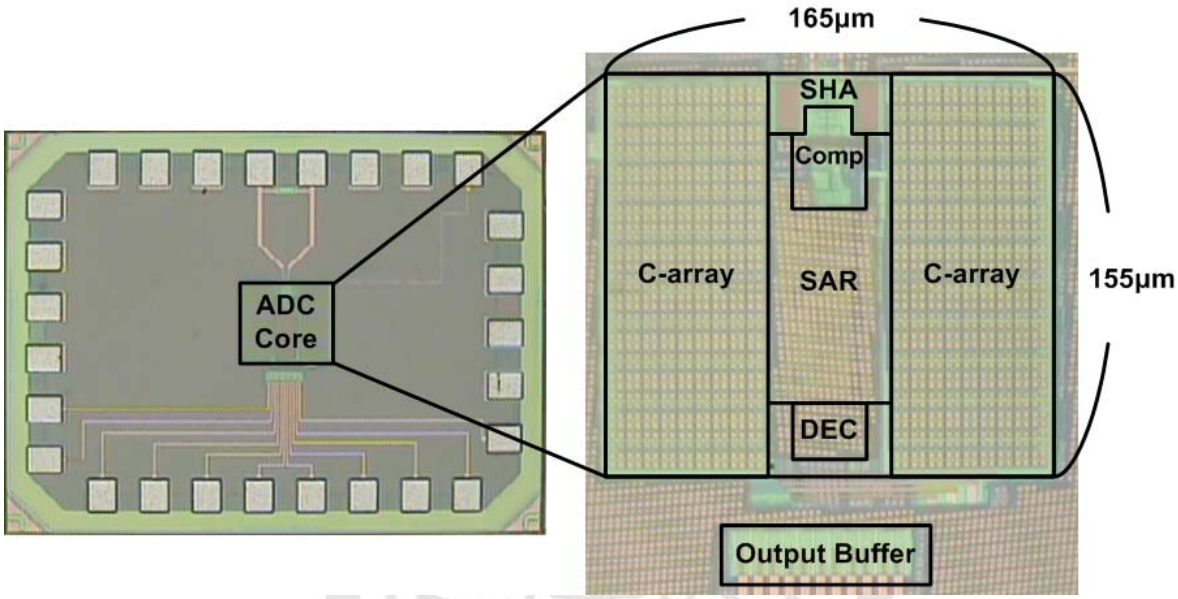


Figure 3-9 Chip micrograph and zoomed view.

Figure 3-10 illustrates the measured static performance (at 100-MS/s sampling rate and 1.2-V supply). The peak DNL and INL are +0.58/-0.53 LSB and +0.69/-0.61 LSB, respectively.

Figure 3-11 provides the measured FFT spectrum with an input frequency close to 10 MHz at a 1.2-V supply and a 100-MS/s sampling rate. The measured SNDR and SFDR are 58.4 dB and 70.4 dB, respectively.

Figure 3-12 plots the measured SFDR and SNDR versus the input frequency. At 1-MHz input frequency, the measured SNDR and SFDR are 59.0 dB and 75.6 dB, respectively.

The resultant ENOB is 9.51 bits. When the input frequency is up to 50 MHz (Nyquist frequency), the measured SNDR and SFDR are 56.0 dB and 66.9 dB, respectively.

Figure 3-13 shows the measured performance versus the sampling frequency with a 1-MHz sinusoidal stimulus. The measured SNDR is higher than 59 dB when sampling frequency less than 100 MS/s. When the sampling rate is up to 120 MS/s, the SNDR is still higher than 55 dB. Further increases the sampling rate, the performance degrades rapidly because the conversion time is insufficient.

The analog circuits (the S/H circuit and comparator) consume 0.37 mW. The SAR control logic and digital error correction circuits draw 0.46 mW. The power consumption of the DAC reference voltage is 0.30 mW. Excluding the output buffers, the total power consumption of the active circuits is 1.13 mW. A summary of the ADC is listed in Table 3-1. Table 3-2 compares the proposed ADC with other state-of-the-art ADCs. The proposed one has the lowest FOM and best ENOB compared to those of ADCs with similar sampling rates and resolutions.

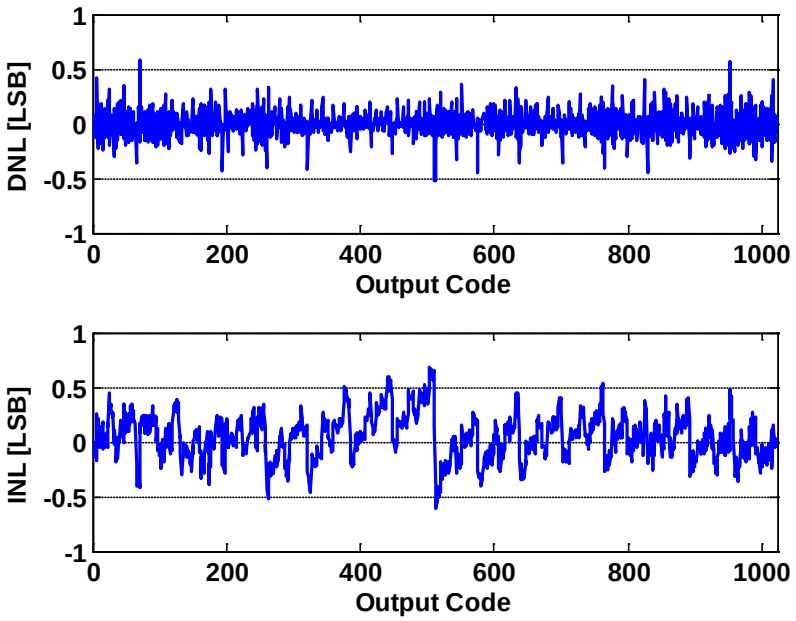


Figure 3-10 Measured INL and DNL performance.

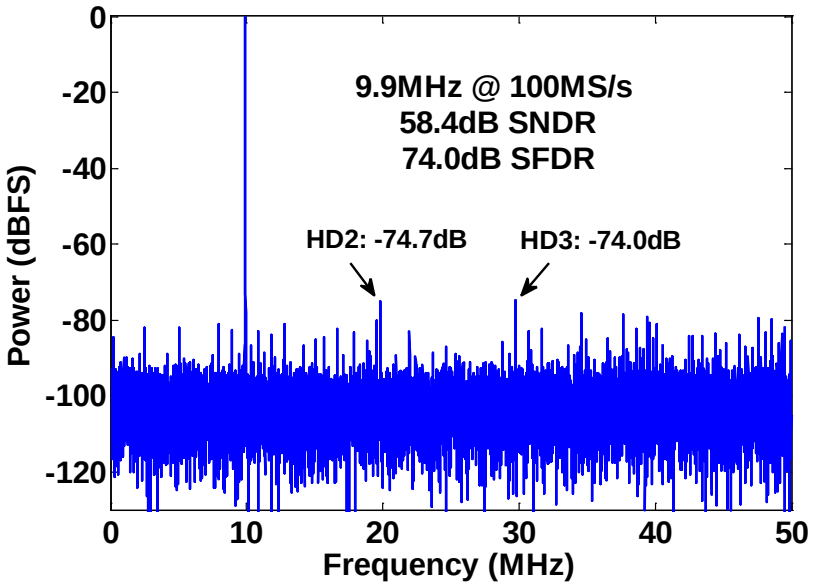


Figure 3-11 Measured FFT spectrum at 100 MS/s with a 9.9-MHz input frequency.

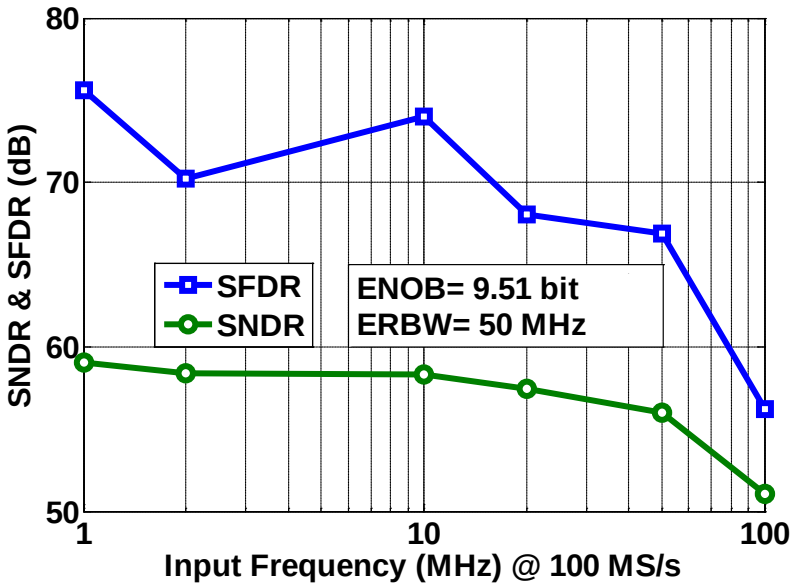


Figure 3-12 Measured dynamic performance versus input frequency at 100 MS/s.

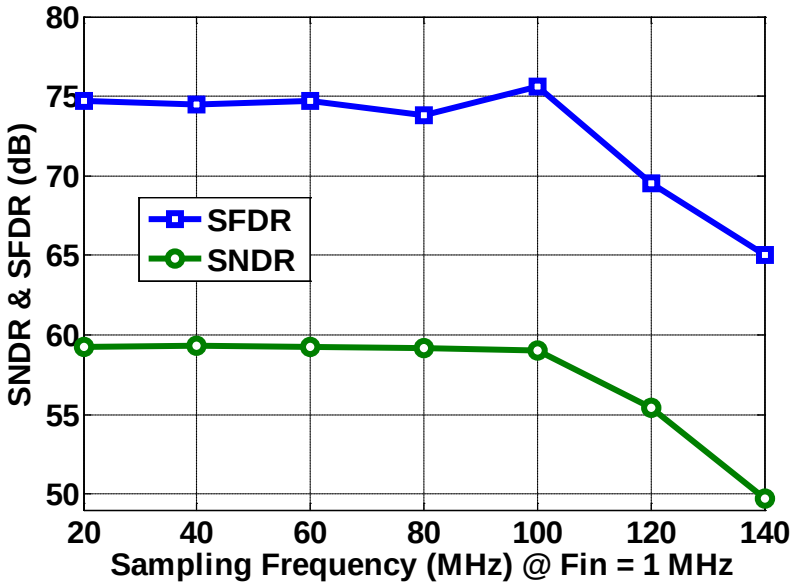


Figure 3-13 Measured dynamic performance versus sampling frequency.

Table 3-1 Summary of ADC Performance

Specification (Unit)	Experimental Result
Supply Voltage (V)	1.2
Input CM Voltage (V)	0.6
Input Range (V_{p-p})	2
Sampling Capacitance (pF)	1.86
Sampling Rate (MS/s)	100
Active Area (mm^2)	0.026
DNL (LSB)	+0.58 / -0.53
INL (LSB)	+0.69 / -0.61
SNDR/SFDR (dB)	59.0 / 75.6 (1 MHz)
	58.4 / 74.0 (10 MHz)
	56.0 / 66.9 (50 MHz)
ENOB (bits)	9.51
ERBW (MHz)	50
Power (mW)	1.13

Table 3-2 Comparison to State-of-the-Art Works

Specifications	*ISSCC* '10 [13]	*ISSCC*'10 [14]	*ASSCC*'09 [29]	*ISSCC*'07 [30]	*ISSCC*'08 [31]	This Work
Architecture	SAR	SAR	SAR	pipelined	pipelined	SAR
Technology	65 nm	65 nm	65 nm	90 nm	65 nm	65 nm
Supply Voltage (V)	1.1	1.2	1.2	0.8	1.2	1.2
Sampling Rate (MS/s)	40	50	100	80	100	100
Resolution (bits)	10	10	9	10	10	10
ENOB (bits)	8.9	9.16	8.53	8.84	9.5	9.51
Power (mW)	1.21	0.82	1.46	6.5	4.5	1.13
FOM (fJ/Conv.-step)	65	30	39	178	62	15.5
Active Area (mm^2)	0.06	0.039	* 0.012	0.64	0.07	0.026

*** off-chip calibration**

3.4 Summary

In this chapter, we proposed a binary-scaled error compensation method to overcome the DAC settling issue in high-speed SAR ADC. The proposed method has the same advantage as the no-binary search method. It can tolerate a certain range of error during the conversion. The total conversion time can be improved even added extra bit cycles. The proposed binary-scaled error compensation method results in less design and hardware overhead compared to the non-binary method. Most important of all, it is in binary-scaled, which is favored in device matching for layout.

The 10-bit prototype SAR ADC achieves 100 MS/s sampling rate with an outstanding FOM of 15.5 fJ/conversion-step which steps well into the domain that was previously dominated by pipelined ADCs.

Chapter 4
Predictive Capacitor Switching Procedure for SAR ADC

4.1 Introduction

The monotonic capacitor switching procedure proposed in Chapter 2 saves 81.3% switching energy and 50% total capacitance as compared to the conventional switching procedure. However, the signal-dependent comparator offset caused by the input common-mode voltage variation degrades the ADC performance. Hence, this chapter presents a splitting monotonic switching procedure to maintain the common-mode voltage during bit cycling.

Besides, we reduce the unnecessary switching in the DAC network by using a predictive circuit, which consists of two coarse comparators and a sub-DAC. The method saves the power consumption in comparators, capacitor networks and switch buffers at the expense of little hardware overhead. It also improves the operating speed and enhances the linearity of a SAR ADC.

4.2 Splitting Monotonic Capacitor Switching Procedure

To avoid the signal-dependent comparator offset degrades the ADC linearity. The splitting monotonic capacitor switching procedure is proposed to maintain the common-mode voltage during bit cycling. Figure 4-1 (b) shows a switching example of splitting capacitor monotonic switching procedure. Similar to the split capacitor array method [12], the capacitors in the capacitor array are split into two equal sub-capacitors to perform the splitting monotonic switching method. Note the final two unit capacitors (LSB capacitor and dummy capacitor) are not split. At the sampling phase, the top plates of all capacitors capture the input signal via the bootstrapped switches. At the same time, the bottom plates of capacitors are reset to ground or V_{ref}, respectively. Next, the comparator performs the first comparison. The capacitor $2C$ connected to V_{ref} on the higher voltage potential side is pulled down to ground. On the lower voltage potential side, the capacitor $2C$ connected to ground is pulled up to V_{ref}. Therefore, the common-mode voltage does not change. The ADC will repeat this procedure until the final bit is obtained.

Figure 4-2 shows the DAC waveform of the two methods. Using the monotonic switching method, the common-mode voltage of the reference DAC gradually decreases from half V_{ref} to ground as shown in Figure 4-2(a). Using the splitting monotonic switching method, the common-mode voltage of the reference DAC is kept at V_{cm} as shown in Figure 4-2(b). Compare to the monotonic switching procedure, the splitting monotonic switching procedure only needs adding two extra inverters to the control logic in each bit cycling. Hence, the method only results in very little hardware overhead.

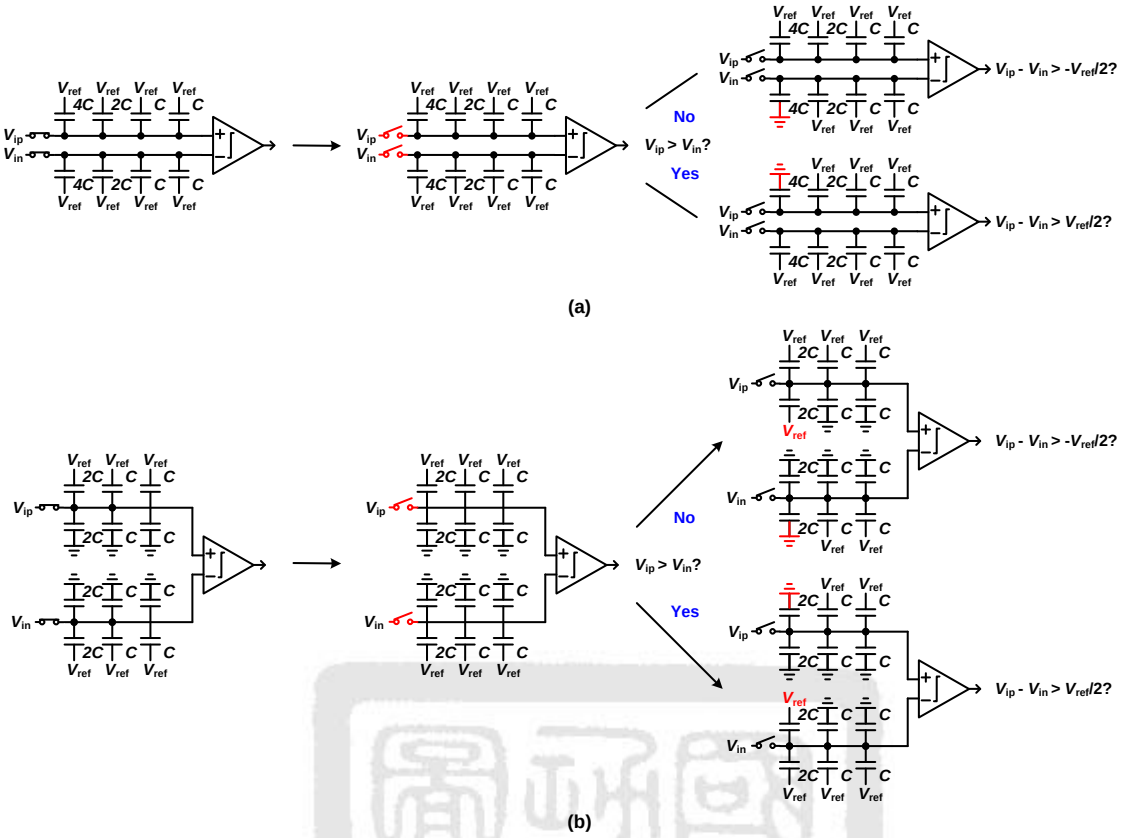


Figure 4-1 Switching examples: (a) Monotonic switching method. (b) Splitting monotonic switching method.

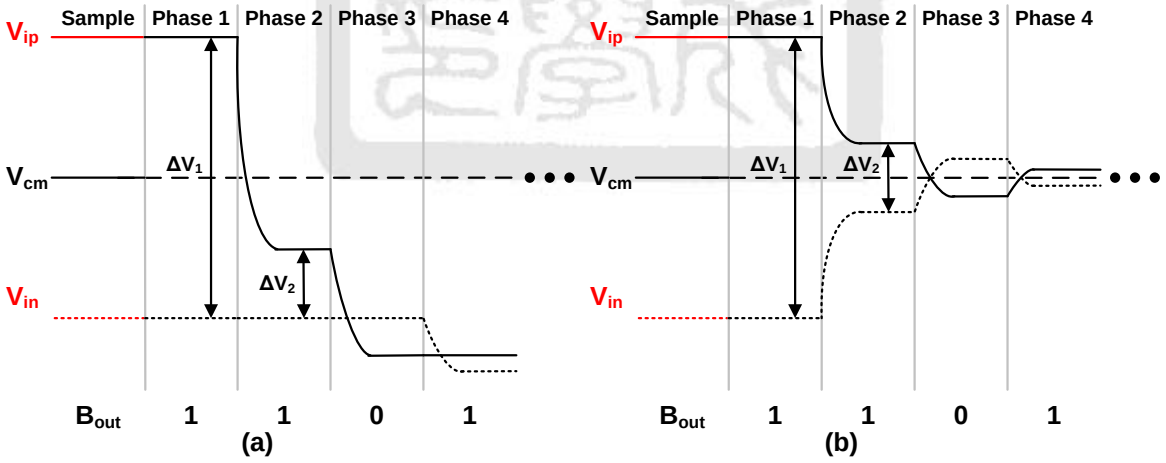


Figure 4-2 (a) Waveform of monotonic switching procedure. (b) Waveform of splitting monotonic switching procedure.

4.3 Predictive Capacitor Switching Procedure

The conventional SAR ADCs apply a binary-search algorithm to approach the closest digital code to match the input signal. In a typical conversion, the reference DAC is added or subtracted a binary-weighted voltage according to the comparator output in each bit cycles. The effective signal range is reduced by a factor of 2 after each bit cycling operation. In the last cycle, the difference between input signal and reference is less than one LSB. However, during the conversion, the difference increases when adds a large voltage to a small difference, which results in unnecessary energy wasted. Reduce some unnecessary switching activities in a DAC network can avoid some switching energy wasted. Figure 4-3 shows the concept of our idea. When the difference is small, this ADC does not add or subtract any voltages until the remaining bit cycling operations could not reduce the difference to less than one LSB.

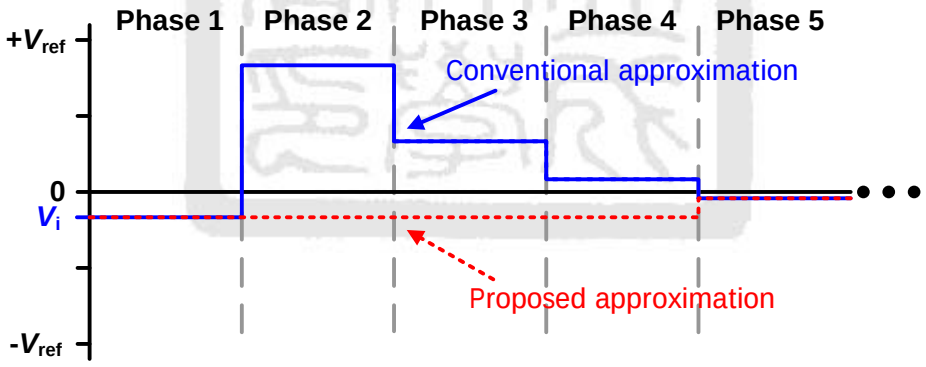


Figure 4-3 The approximations of conventional and proposed methods.

Figure 4-4 shows how to reduce the unnecessary switching in DAC network. Take the Phase 1 as an example. When the voltage difference of input signal and reference is located in the “No Switching” region which is in the operating range of next bit cycle, even no capacitors switched in this bit cycle, the remaining bit cycling operations could reduce the

difference to less than one LSB. Hence, the ADC does not switch any capacitors in this bit cycle. On the contrary, when the voltage difference is located in the “Switching” region which is out of the operating range of next bit cycle, the ADC switches the relative capacitors according to the comparison. Otherwise the remaining bit cycling operations could not reduce the difference to less than one LSB.

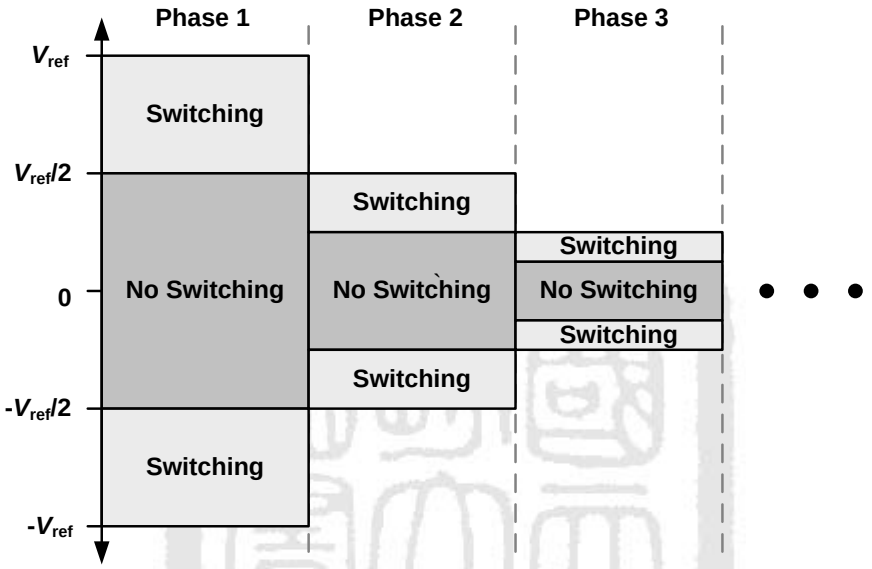


Figure 4-4 The graph of proposed switching procedure.

Figure 4-5(a) shows the transfer curves of the first bit cycling operation using the conventional switching method. The input signal range is from $-V_{ref}$ to V_{ref}. When the signal is positive, the signal is pulled down by $V_{ref}/2$. On the contrary, when the signal is negative, the signal is pulled up by $V_{ref}/2$. After this bit cycle, the effective signal range becomes $-V_{ref}/2$ to $V_{ref}/2$.

Figure 4-5(b) shows the transfer curves of the first bit cycling operation using the predictive switching method. When the signal is higher than $V_{ref}/2$, the signal is pulled down by $V_{ref}/2$. On the contrary, when the signal is lower than $-V_{ref}/2$, the signal is pulled up by $V_{ref}/2$. When the signal is located in $-V_{ref}/2$ to $V_{ref}/2$, the signal is kept at the same voltage potential. To perform such a function, the ADC needs to do two comparisons in

each bit cycle. Therefore, two coarse comparators and a sub-DAC are added to the ADC. The ADC using the proposed switching method can be viewed as a 1.5-bit/cycle SAR ADC.

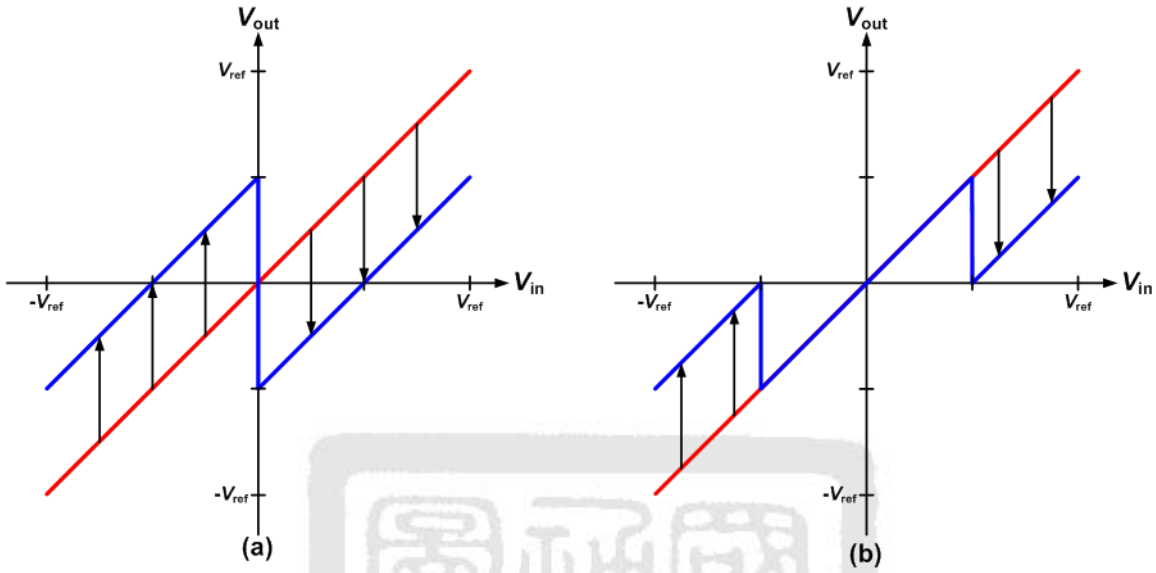


Figure 4-5 Transfer curves in the first bit cycle: (a) Conventional 1-bit/cycle SAR ADC. (b)Proposed 1.5-bit/cycle SAR ADC.

4.4 A 1-V 11 fJ/Conversion-Step 10-bit 10-MS/s Asynchronous SAR ADC

4.4.1 Architecture

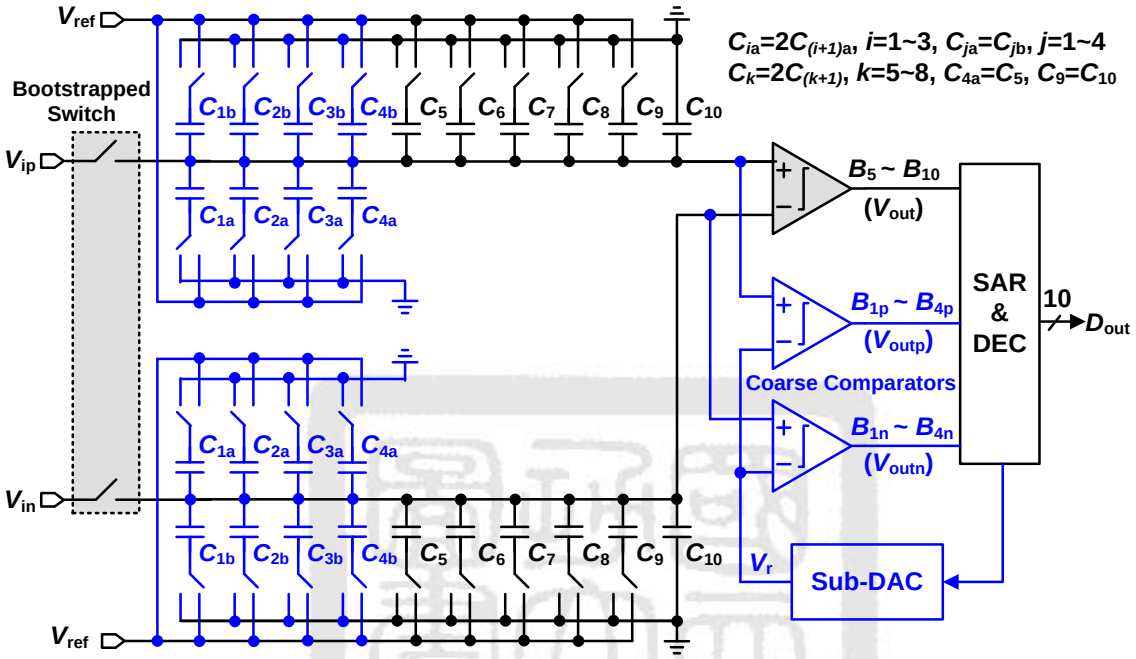


Figure 4-6 The architecture proposed SAR ADC.

Based on the architecture (Figure 2-2) proposed in Chapter 2, Figure 4-6 shows the schematic of the proposed SAR ADC. The first 4 MSB capacitors in the capacitor array are all split into two equal sub-capacitors to perform the splitting monotonic switching method. At the sampling phase, the top plates of all capacitors capture the input signal via the bootstrapped switches. At the same time, the bottom plates of capacitors C_{1a}~C_{4a} are reset to ground, and the others (C_{1b}~C_{4b} and C_5~C_9) are reset to V_{ref}. Next, the comparators do the first comparison. The capacitor C_{1b} on the higher voltage potential side is pulled down to ground. On the lower voltage potential side, the capacitor C_{1a} is pulled up to V_{ref}. Therefore, the common-mode voltage does not change. To avoid complicated control logic and layout routing, the splitting monotonic switching method is only applied to the first 4

MSB capacitors. The remaining operations still use the monotonic switching method. The common-mode voltage variation is diminished to only 1/16 of that using monotonic switching method in all bit cycles. The comparator dynamic offset problem becomes negligible in this 10-bit case.

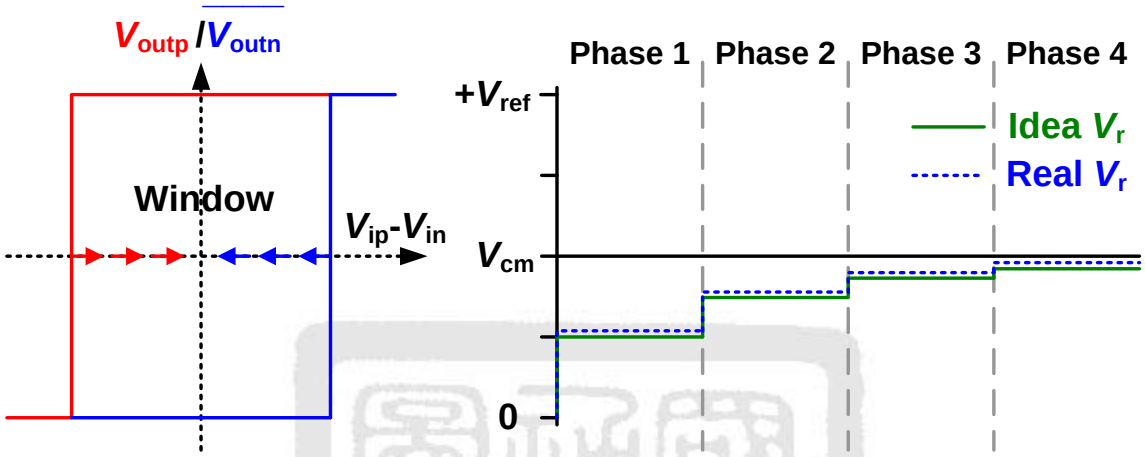
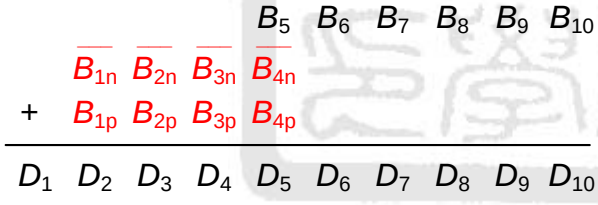


Figure 4-7 Variable window function.

The two coarse comparators and a sub-DAC are added to perform the function as shown in Figure 4-4. In order to achieve a variable window function in different bit cycles, the reference voltage V_r must be variable. Figure 4-7 shows the variable window function and V_r. A 6-bit sub-DAC generates the variable V_r. The real V_r in this ADC is higher than the ideal value about 8 LSBs, the real window size is a little smaller than the ideal one. Therefore, this ADC has about 8-LSB margin to tolerate the sub-DAC and coarse comparator offset errors. For best efficiency, the mechanism is only used in the first 4 MSB capacitors. Even including the overhead of the 6-bit sub-DAC, this method saves 40~45% power dissipation in the capacitor network and switch buffers compared to the monotonic switching method. Figure 4-8 shows the digital error correction logic, which consists of only 4 full-adders.

This ADC uses a dynamic comparator with a p-type input pair as shown in Figure 2-18.

The dynamic comparator does not consume static current and hence is suitable for an energy efficient design. Internal control logic triggered by the global clock and comparator output asynchronously generates internal control clocks, which avoids a high frequency clock generator and makes the sampling rate equal to the clock rate. This ADC uses multi-sandwich capacitors to construct the capacitor array. The unit capacitor is about 5 fF, composed of 5 metal layers in a 4 × 4.8 μm^2 area. The total input capacitance is 2.5 pF each terminal. Table 4-1 lists the pre-layout simulation results of the ADCs with or without using the predictive switching method. According to simulation result, the ADC using the predictive switching method saves about 17.6 % total power consumption. The main power reduction is from the two coarse comparators, the capacitor networks and the switch buffers. In this case, the two coarse comparators are designed conservatively, the physical size is about half of the fine comparator. If the coarse comparators are designed smaller, they will result in more power reduction.



	B_{xp}	$\overline{B_{xn}}$	State
$V_{ip} > V_r$ $V_{in} < V_r$	1	1	Switching
$V_{ip} > V_r$ $V_{in} > V_r$	1	0	No Switching
$V_{ip} < V_r$ $V_{in} > V_r$	0	0	Switching

Figure 4-8 Digital error correction logic.

Table 4-1 Power Consumption of Each Parts

Power	Without Predictive Switching Method	With Predictive Switching Method
Analog	26.6	25.2
Digital	46.1	39.2
DAC	19.5	11.6 (10.1+1.5)
Total	92.2 (μW)	76.0 (μW)

4.4.2 Discussion on DAC Settling

Figure 4-9 is an example of the DAC waveform with the predictive capacitor switching procedure. After the input signal sampled, the two coarse comparators do the first comparisons. After some logic delay, the DAC switches the relative capacitors according to the comparison results. After the DAC is well-settled, the coarse comparators make the second decisions. Because the signals are in the no switching region, therefore, the DAC does not switching any capacitor in this bit cycle. After the remaining bit cycling and logic operations, The ADC generates correct digital output codes. The first 5 MSBs are 11011.

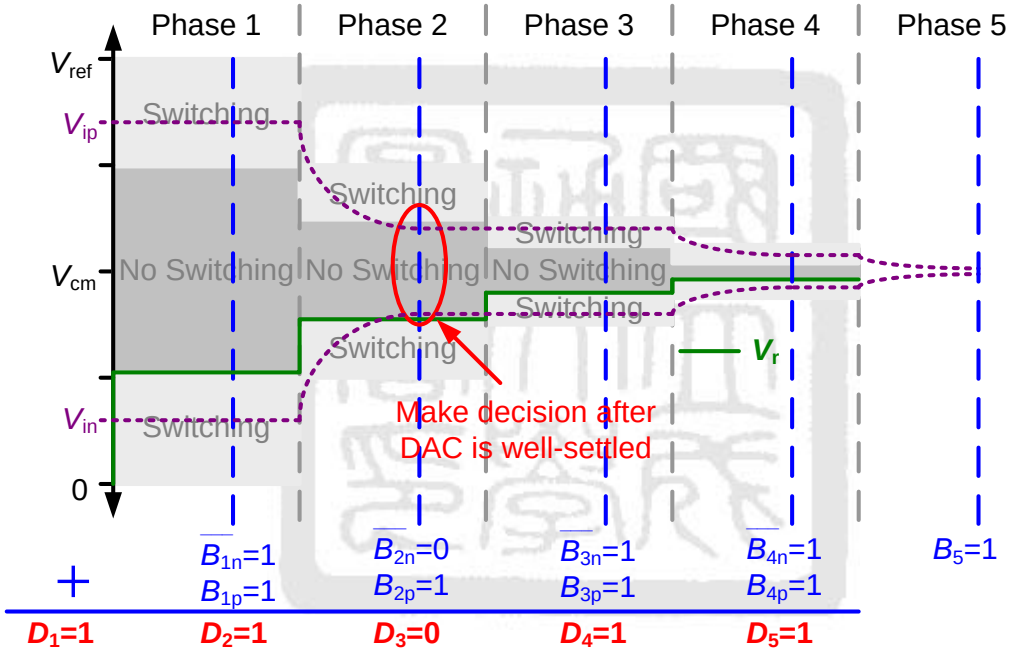


Figure 4-9 The waveform of the DAC network with sufficient settling time.

If the bit cycling time is reduced as shown in Figure 4-10, the comparators make decisions before the DAC is well-settled. In Phase 2, the comparison results are different from the previous case. After the remaining bit cycling and logic operations, the first 5 MSBs are 11011 which is still the same as the previous case. That means the proposed ADC can tolerate a certain range of settling error. Figure 4-11 shows a critical case, the signal always located in the “switching” region regardless of the DAC is well-settled or not,

the DAC needs to switch in each bit cycling. Although the DAC does not save any switching energy in this case, but the operating speed of the ADC is still improved.

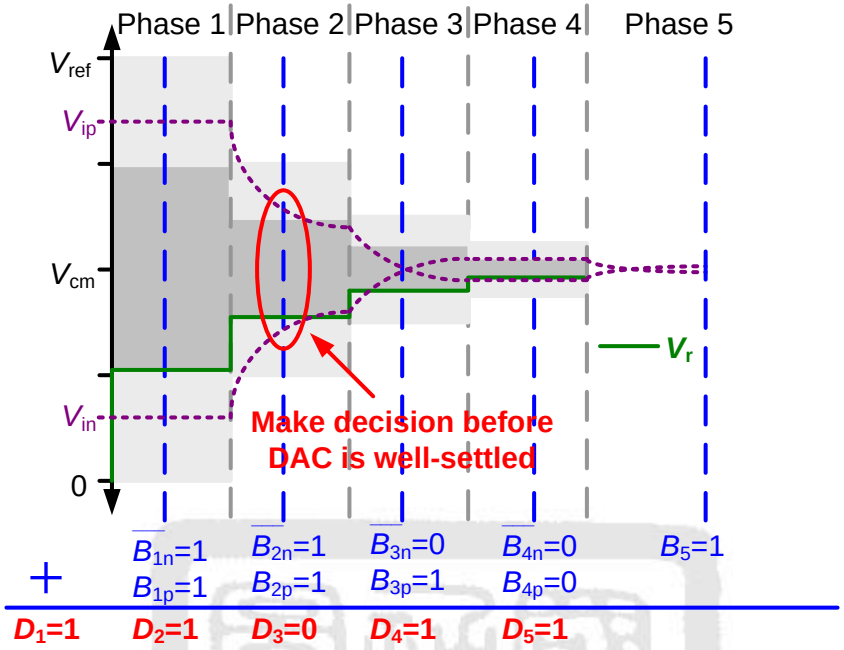


Figure 4-10 The waveform of DAC network without sufficient settling time.

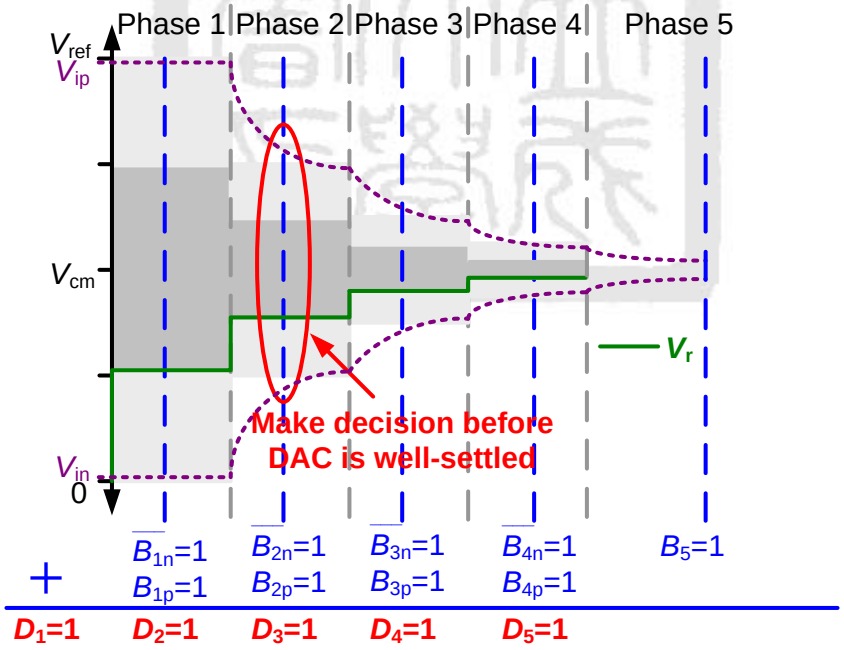


Figure 4-11 The waveform of DAC network in a critical case.

In the first bit cycle of a conventional SAR ADC, according to the first comparison result, the DAC must settle to 9-bit precision. Then the comparator can make the second decision. Table 4-2 lists the demand of settling times for different bit cycles and different methods. The unit “RC × ln2” is the settling time for DAC settles to 1-bit precision. In the proposed ADC, the first 3 bit cycling operations are insensitive to the DAC settling error, Ideally, the DAC settled to 1-bit precision is sufficient to perform a correct conversion. But in real case, in order to tolerate the offset of coarse comparators and sub-DAC, the window size is a little smaller than the ideal one. It takes a little longer settling time, but less than 2RC × ln2. With the proposed method, the operating speed of ADC is improved.

Table 4-2 Settling Times with Different Methods

Bit cycle	1	2	3	4	5	6	7	8	9	10
The Settling Time of Conventional SAR ADC (Unit: RC × ln2)	9	8	7	6	5	4	3	2	1	0
The Settling Time of Proposed SAR ADC (Unit : RC × ln2)	<2	<2	<2	6	5	4	3	2	1	0

4.4.3 Matlab Simulation Result

The SAR ADC which uses binary-scaled capacitor arrays to perform the DAC network usually has good linearity. However, the two digital codes 10000… and 01111… have the most different switching sequences. When the process variation leads to some mismatches between each capacitor cells, the MSB capacitor is not equal to the sum of the other capacitors. Therefore, the static performance DNL and INL usually have large spur and jump at the middle of the output codes, respectively. But in the proposed SAR ADC which have a 4-bit predictive circuit, the switching sequences of the two digital codes 10000…

and 01111… are the same in the first four bit cycles. No capacitor was switching in the first four bit cycles. With less capacitors switched, the DNL and INL performance was improved especially around the middle of output codes. Hence, the linearity of ADC is enhanced. A behavioral simulation of the SAR ADC was performed. The values of the unit capacitor are taken to be the Gaussian random variable with standard deviation of 3%, and the other parts of the ADC are ideal. Figure 4-12 shows the results of 10000 runs, where the standard deviation of the INL and DNL are plotted versus digital output codes. As expected, the spur at the middle of the output codes in DNL was suppressed in the proposed SAR ADC, and the proposed SAR ADC has $\sqrt{2}$ times better INL performance.

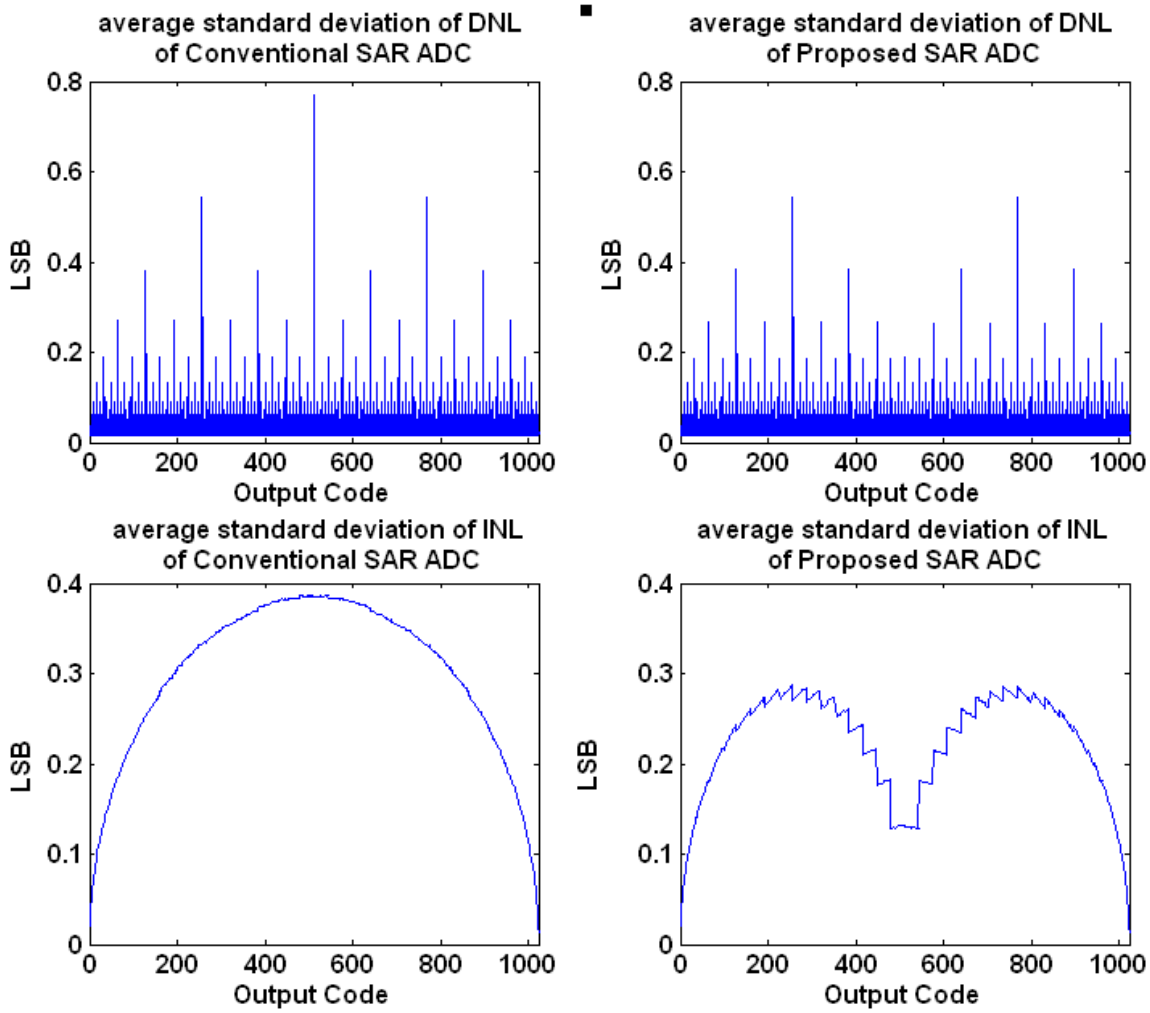


Figure 4-12 The standard deviation of INL and DNL.

4.4.4 Measurement Results

The prototype was fabricated in a 0.18-μm 1P6M CMOS technology. The full micrograph and the zoomed-in view of the core are shown in Figure 4-13. The total area of the chip is 0.98 mm × 0.78 mm, with the ADC core taking up only 330 μm × 260 μm. The measurement results of the prototype are presented below.

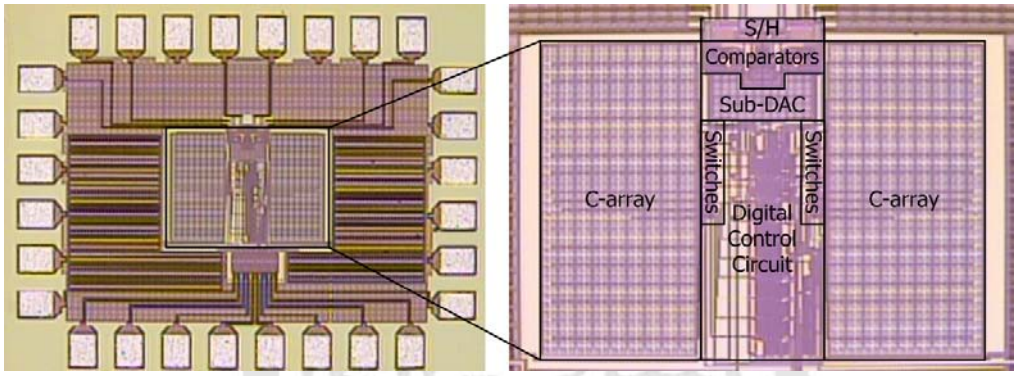


Figure 4-13 Die micrograph and the zoomed view.

At a 1-V supply and a 10-MS/s sampling rate, the measured DNL and INL are shown in Figure 4-14. The peak DNL and INL are +0.28/-0.34 LSB and +0.23/-0.38 LSB, respectively. The figure shows that the DNL and INL have no spur at the middle of output codes which agrees with the simulation result.

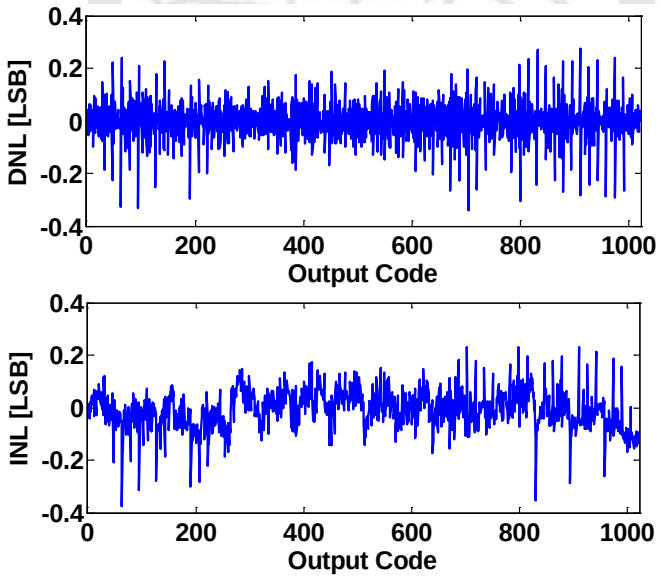


Figure 4-14 Measured DNL and INL.

Figure 4-15 shows the measured FFT spectrum with an input frequency close to 5 MHz at a 1-V supply and a 10-MS/s sampling rate. The measured SNDR and SFDR are 60.29 dB and 68.92 dB, respectively.

Figure 4-16 plots the measured SNDR, SFDR values versus the input frequency at 10 MS/s. At 1-MHz input frequency, the measured SNDR and SFDR are 60.97 dB and 79.4 dB, respectively. The resultant ENOB is 9.83 bits. When the input frequency was increased to 10 MHz, the measured SNDR and SFDR are 59.12 dB and 69.84 dB, respectively. The ERBW is higher than 10 MHz.

Figure 4-17 shows the measured performance versus the sampling frequency with a 1-MHz sinusoidal stimulus.

The analog circuit, including the S/H circuit and comparators, consumes 32 μW, and the digital control circuit draws 50 μW. The capacitor networks and Sub-DAC consume 16 μW. The total power consumption of the ADC is 98 μW. The prototype achieves an FOM of only 11 fJ/conversion-step. A summary of the ADC is listed in Table 4-3.

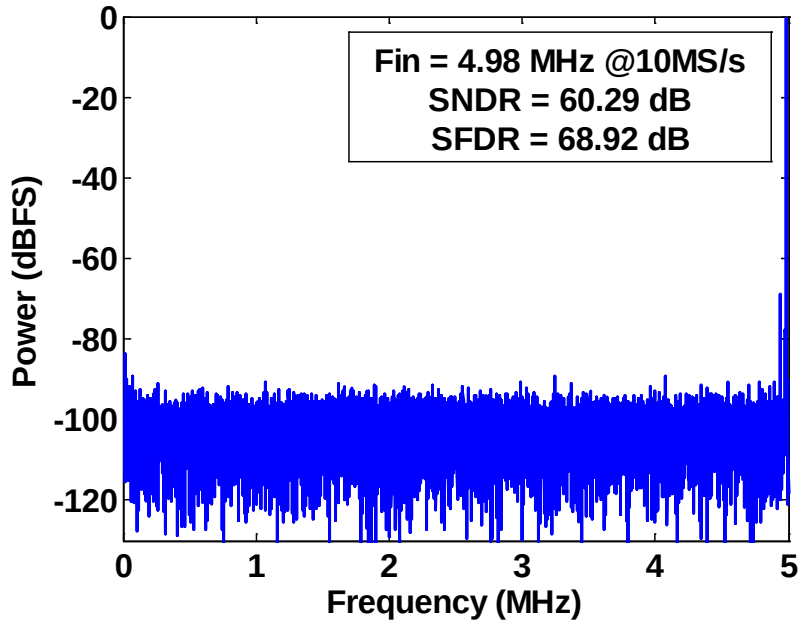


Figure 4-15 Measured FFT spectrum at 10 MS/s with a 4.98-MHz input frequency.

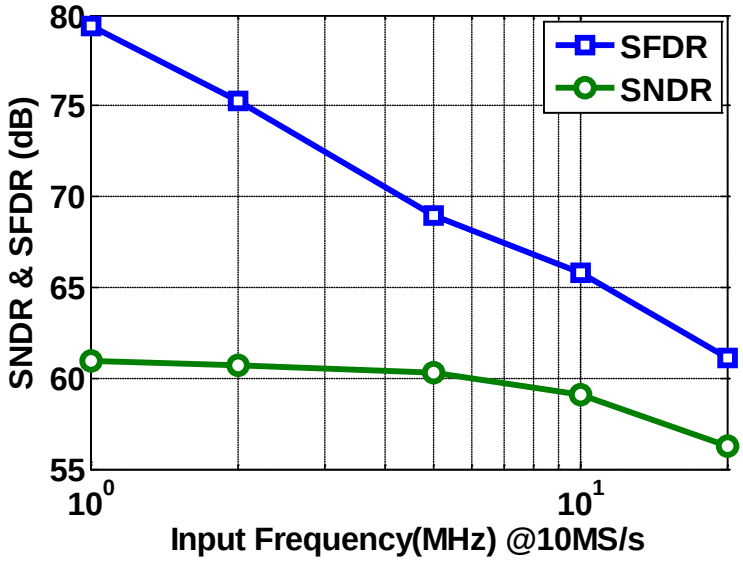


Figure 4-16 Measured dynamic performance versus input frequency at 1 V and 10 MS/s.

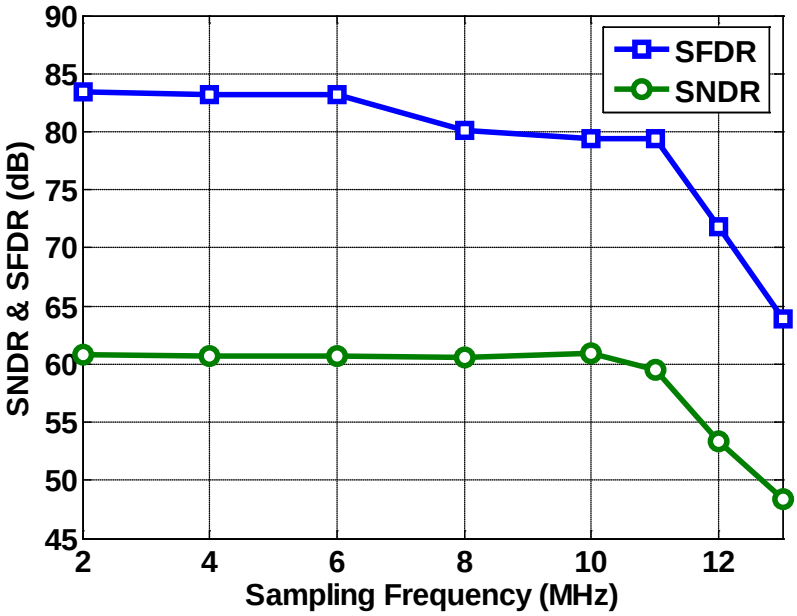


Figure 4-17 Measured dynamic performance versus sampling frequency.

Table 4-3 Summary of ADC Performance

Specification (Unit)	Experimental Result
Technology	0.18μm CMOS
Resolution (bit)	10
Sampling Rate (MS/s)	10
Input Range (V_{p-p})	2
Supply Voltage (V)	1
Sampling Capacitance (pF)	2.5
Active Area (mm^2)	0.086
DNL (LSB)	+0.34/-0.28
INL (LSB)	+0.38/-0.23
SNDR/SFDR (dB)	60.97 / 79.4 (1 MHz)
	59.12 / 65.84 (10 MHz)
ENOB (bits)	9.83
Power (μW)	98
FOM (fJ/Conv.-step)	11

At a regular 1.8-V supply, the prototype ADC achieves 40 MS/s. Figure 4-18 shows the measured FFT spectrum with an input frequency of close to 5 MHz. The measured SNDR and SFDR are 59.99 dB and 76.27 dB, respectively.

Figure 4-19 plots the performance versus input frequency. At 1-MHz input frequency, the measured SNDR and SFDR are 60.43 dB and 80.55 dB, respectively. The resultant ENOB is 9.75 bits. When the input frequency was increased to 35 MHz, the measured SNDR and SFDR are 57.31 dB and 66.34 dB, respectively. The ERBW is closed to 35 MHz.

Table 4-4 compares the proposed ADC with other state-of-the-art ADCs. Although the proposed ADC was fabricated using an older technology, it still achieves similar FOM, sampling rates and area with those excellent works.

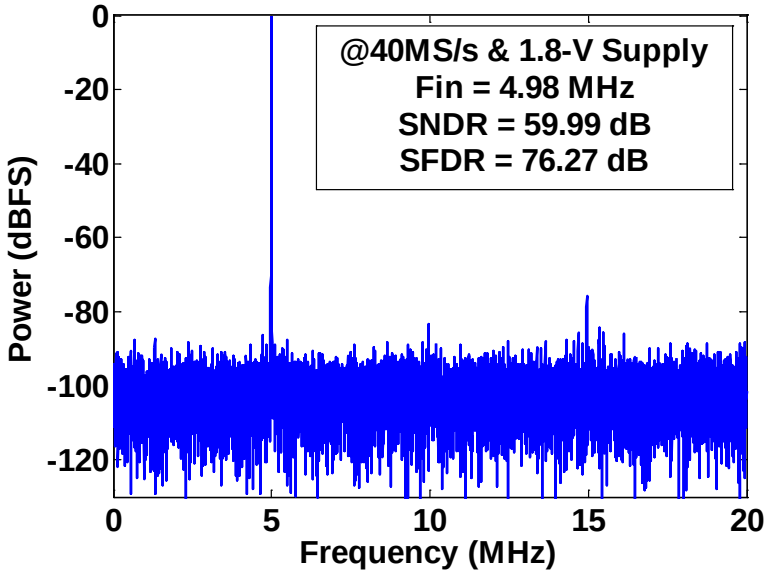


Figure 4-18 Measured FFT spectrum at 40 MS/s with a 4.98-MHz input frequency.

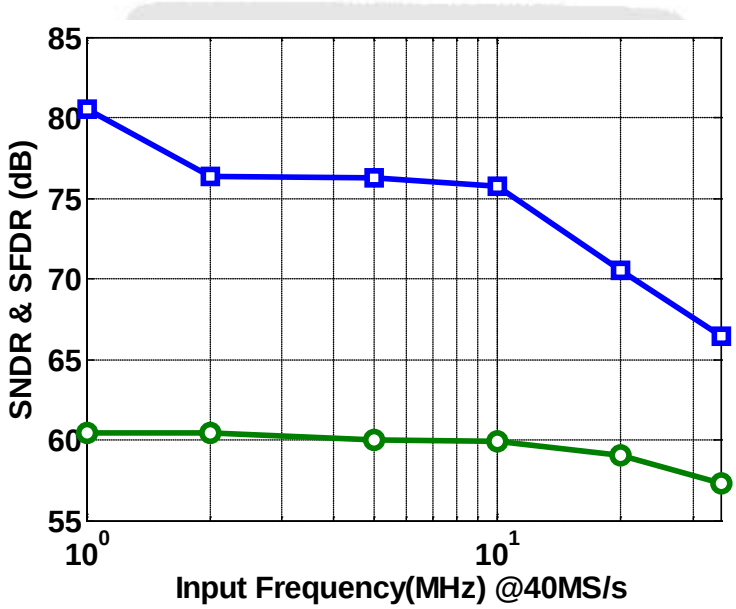


Figure 4-19 Measured performance versus input frequency at 1.8 V and 40 MS/s.

Table 4-4 Comparison to State-of-the-Art Works

Specifications	*ISSCC*'10 [13]	*ISSCC*'10 [14]	*ISSCC*'10 [15]	This Work	
Architecture	SAR	SAR	SAR	SAR	
Technology	65 nm	65 nm	90 nm	180 nm	
Resolution (bit)	10	10	8	10	
Supply Voltage (V)	1.1	1.2	1	1	1.8
Sampling Rate (MS/s)	40	50	10.24	10	40
ENOB (bits)	8.9	9.16	7.8	9.83	9.75
Power (mW)	1.21	0.82	0.069	0.098	1.33
FOM (fJ/Conv.-step)	65	30	30	11	39
Active Area (mm^2)	0.06	0.039	0.54	0.86	

4.5 Summary

In this chapter, we proposed a splitting monotonic switching procedure to suppress the ADC performance degradation caused by the variation of the input common-mode voltage. Besides, we proposed a predictive circuit to avoid unnecessary switching in the DAC network. With less capacitors switched, the proposed method not only reduces the power consumption but also improves the static and dynamic performance. Compared to the conventional method, the proposed method can use a smaller size unit capacitor to achieve the same accuracy.

The experiment results demonstrate the effectiveness of the proposed techniques. The proposed two methods enhance the ADC linearity without degrading the operation speed of the SAR ADC, and maintain the low-power and low-cost feature of the SAR architecture with monotonic switching procedure.

Chapter 5
Conclusions and Future Work

5.1 Conclusions

This dissertation proposes several circuit design techniques to reduce the power consumption and enhance the operating speed of SAR ADCs. To demonstrate the effectiveness of the proposed techniques, the details of analyses and implementations are also presented. The main contributions of this dissertation are summarized as follows:

For SAR ADC architecture, the proposed monotonic switching procedure offers lower switching energy, provides higher settling speed, and uses smaller capacitor network compared to the conventional one. By using the simple asynchronous control logic, the SAR ADC does not need an extra high frequency clock. The experiment results demonstrate the power and hardware efficiency and also the high-speed potential of the proposed architecture.

The proposed binary-scaled error compensation method overcomes the DAC settling issue in the high-speed SAR ADC. Similar to the non-binary search technique, the proposed method is capable of enhancing the sampling rate of the SAR ADC, and results in fewer design and hardware overhead than the non-binary search technique. Besides, with binary-weighted capacitor array, the SAR ADC can achieve higher linearity with proper layout matching.

The proposed splitting monotonic switching procedure improves the shortcoming of the monotonic switching procedure. It splits the capacitors and modifies the switching scheme to maintain the common-mode voltage during bit cycling. This method suppresses the ADC performance degradation caused by the input common-mode voltage variation which results in signal-dependent offset when the comparator makes decision. In addition, we proposed a predictive circuit to avoid unnecessary switching in a DAC network. This method reduces the power consumption and improves the linearity of an ADC without degrading the operating speed. The simulation and experiment results demonstrate the effectiveness of the technique.

In this dissertation, we also proposed two low-cost MOM capacitor structures: multi-layer sandwich capacitor and finger-sandwich capacitor. Both of the two capacitor structures have larger capacitance in unit area than the sandwich capacitor. Therefore, the proposed structures are very hardware efficient. Besides, for the same capacitance, the proposed capacitor structures have better matching than the MIM capacitor structure. That means the SAR ADC can use a smaller unit capacitance cell to achieve the same linearity. Therefore, the total sampling capacitance can be reduced, that decreases the power consumption and design effort of the front-end circuit.

5.2 Future Work

Several circuit techniques for the SAR ADC have been proposed in this dissertation. There are some research topics, extended from the proposed techniques, can be further investigated in the future. The related topics are listed as follows:

1. The single channel SAR ADC has limited operating speed. The time-interleaving architecture is a feasible way to increase the sampling rate. The channel mismatches is adequate for low-to-medium resolutions. In case of high-resolution data conversion, however, spectral purity is easily compromised by even slight channel mismatches because of the low quantization noise floor. Therefore, one of the challenges for the design of medium-to-high resolutions and very high-speed time-interleaved SAR ADCs is the channel mismatch problem. To diminish the gain error and offset between ADC channels, developing a simple but effective digital correction algorithm is necessary.
2. The 10-bit prototype ADC with splitting monotonic switching procedure and predictive switching procedure achieves excellent performance (ENOB is 9.83 bits). The conversion is almost ideal. Therefore, the architecture is suitable for higher resolution (12- to 14-bit) applications. In the high resolution case, the sampling capacitance increases exponentially if using binary weighted capacitor array to perform the DAC network. The split capacitor DAC mismatch calibration method [35] provides a solution to reduce the sampling capacitance. Hence, designing a low-capacitance but high linearity capacitor array is worthwhile.

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Publication List

A. Transaction / Journal Papers:

[1] **C.-C. Liu**, S.-J. Chang, G.-Y. Huang and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure," *IEEE J. Solid-State Circuits*, vol 45, no. 4, pp. 731-740, Apr. 2010.

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B. Conference Papers:

[1] **C.-C. Liu**, Y.-T. Huang, G.-Y. Huang, S.-J. Chang, C.-M. Huang and C.-H. Huang, "A 6-bit 220-MS/s Time-Interleaving SAR ADC in 0.18-μm Digital CMOS Process," *IEEE International Symp. on VLSI Design, Automation & Test*, Apr. 2009, pp. 215-218.

[2] **C. C. Liu**, S. J. Chang, G. Y. Huang and Y. Z. Lin, "A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13μm CMOS process," *IEEE Symp. on VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 236-237.

[3] **C.-C. Liu**, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang and C.-H. Huang, "A 10b 100MS/s 1.13mW SAR ADC with Binary Scaled Error Compensation," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 386-387.

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11fJ/Conversion-Step 10bit 10MS/s Asynchronous SAR ADC in 0.18μm CMOS," *IEEE Symp. on VLSI Circuits Dig. Tech. Papers*, Jun. 2010. pp. 241-242

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C. Awards:

[1] 2007 全國大專院校 IC 設計競賽 類比組 佳作

Third Prize, Analog Circuits Deign, University/College IC Contest 2007, Ministry of Education, Taiwan

[2] 2008 全國大專院校 IC 設計競賽 類比組 特優

First Prize, Analog Circuits Deign, University/College IC Contest 2008, Ministry of Education, Taiwan

[3] 2010 國家晶片系統設計中心 優良設計獎

The Best Design Award for Outstanding Chip, National Chip Implementation Center, 2010, Taiwan

[4] 2010 第 10 屆旺宏金矽獎

Macronix Golden Silicon Award, 2010, Macronix Foundation, Taiwan

Biography

Chun-Cheng Liu was born in Changhua, Taiwan, in 1983. He received the B.S. and Ph.D. degree in electrical engineering from the National Cheng Kung University, Tainan, Taiwan in 2005 and 2010, respectively. His research interests are in analog and mixed-signal circuits, especially on analog-to-digital converters.