Analog Front-End Design for Gb/s Wireline Receivers

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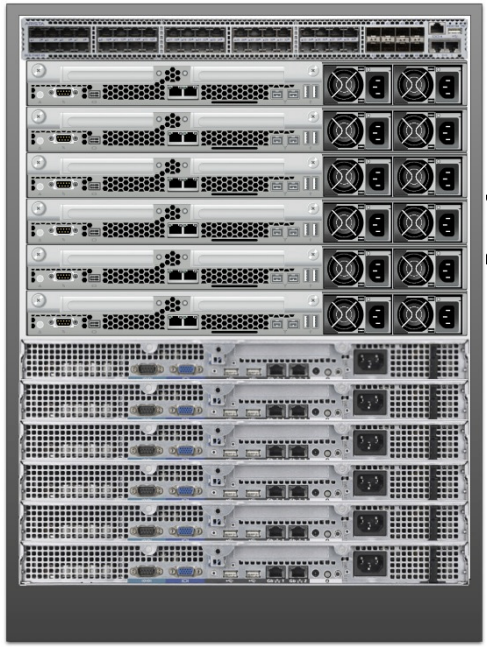
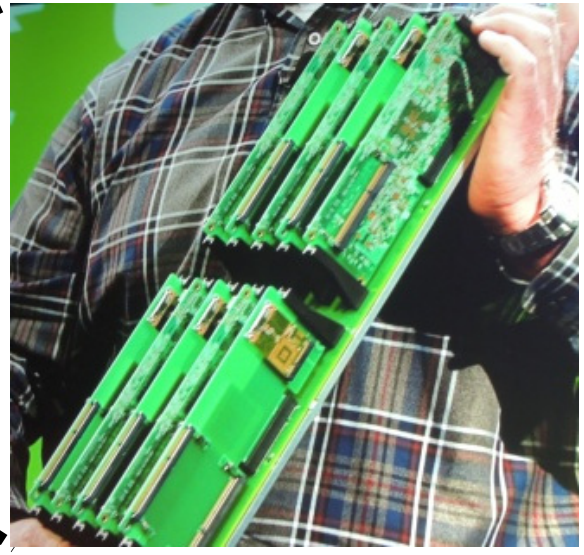
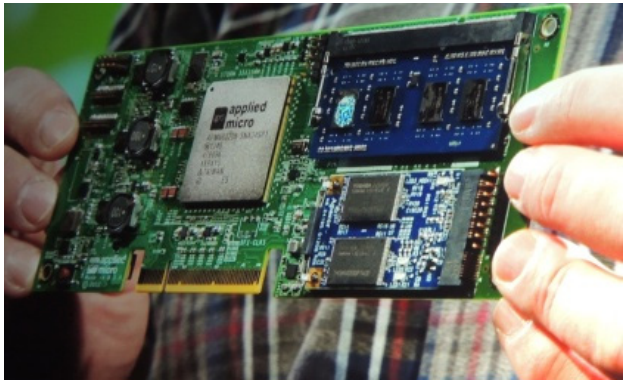
Importance of Wireline Links





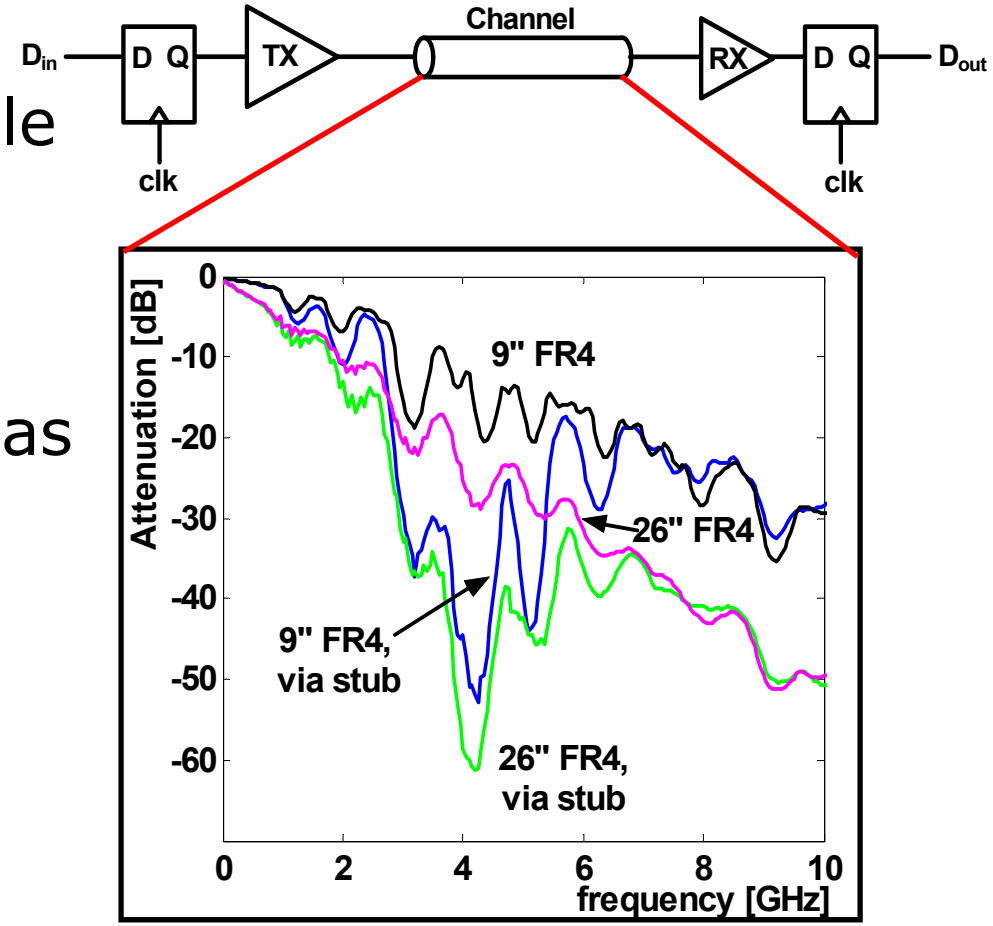


- Wireline I/O performance and power increasingly critical differentiators
  - Chassis can contain tens of 1000's of these links

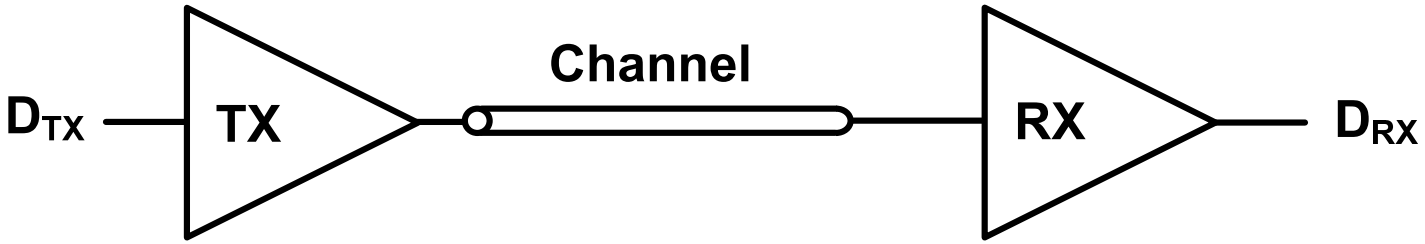
Images from eetimes.com

The High-Speed Wireline Challenge

- Deliver as much throughput as possible
  - Multiple Tb/s for the whole chip
- Using as little power as possible
  - ~1pJ/bit or less
- While dealing with "badness" of the channels



Focus of this Tutorial: RX



- By definition, TX knows the data, RX doesn't
  - Tends to place more stringent constraints on RX circuit design
- RX impedance levels tend to be higher – more efficient to implement signal processing there
- Knowledge of RX design techniques maps directly to TX design too

Tutorial Outline

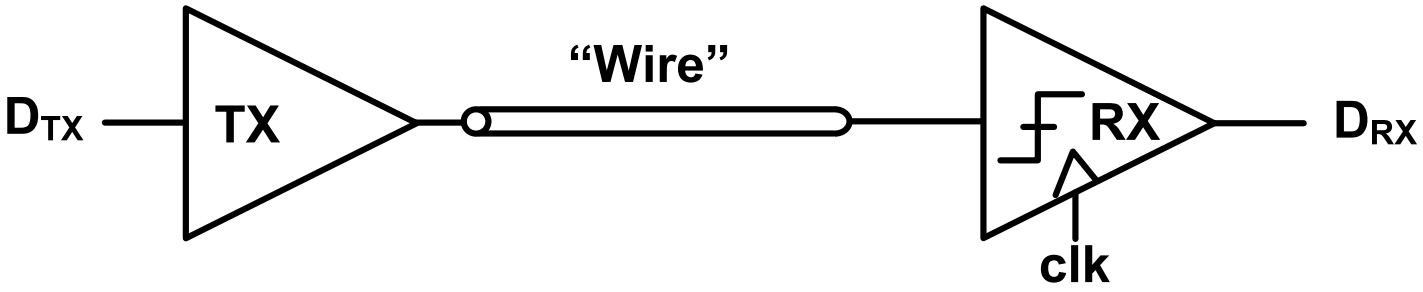
- RX AFE Basics
- RX AFE Circuits & Power Analysis
- Practical Issues and Common Gotchas
- Key Lessons

Tutorial Outline

- RX AFE Basics
  - Basic AFE requirements
  - RX Equalizers

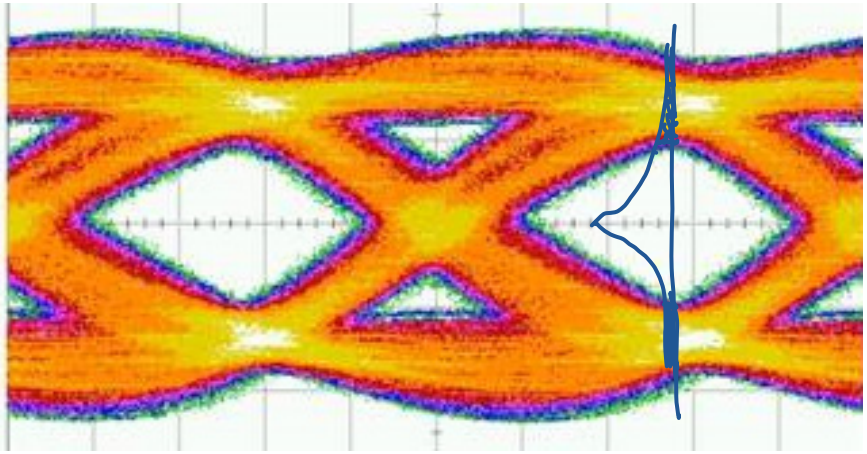
- RX AFE Circuits & Power Analysis
- Practical Issues and Common Gotchas
- Key Lessons

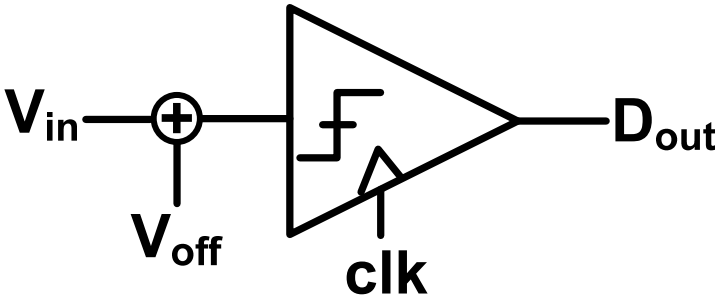
Most Basic RX



- Most basic RX really is "just" a comparator
  - Converts potentially small, analog voltages on the "wire" into digital levels
- What can go wrong?

Key Constraint: Bit Error Rate





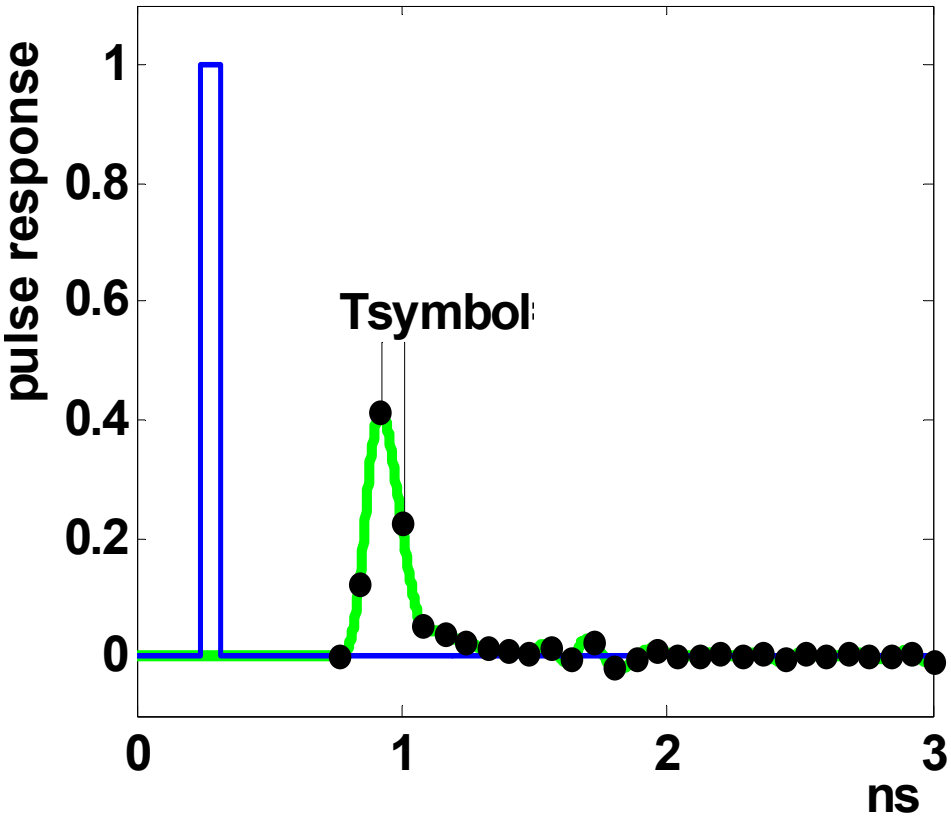
- BER = Bit Error Rate
  - Average # of wrong received bits / total transmitted bits
- Simplified example: (voltage only)

$$BER = \frac{1}{2} erfc\left(\frac{V_{in,ampl} - V_{off}}{\sqrt{2}\sigma_{noise}}\right)$$

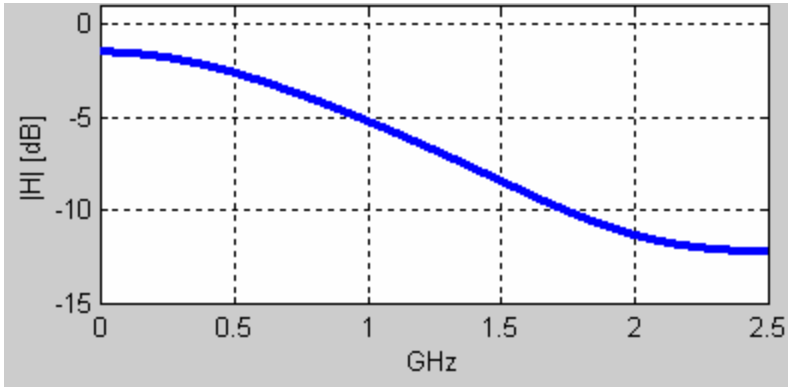
- BER = 10^{-12}: $(V_{in,ampl} - V_{off}) = 7\sigma_n$
- BER = 10^{-20}: $(V_{in,ampl} - V_{off}) = 9.25\sigma_n$

Noise Not the Only Source of Errors: ISI

- ISI: Inter-Symbol Interference
- Channel is band-limited
  - I.e., dispersive (low pass)
  - Short TX pulses get spread out
  - Low latency
- Also get reflections
  - Z mismatches, connectors, etc.
  - Longer latency



Equalization



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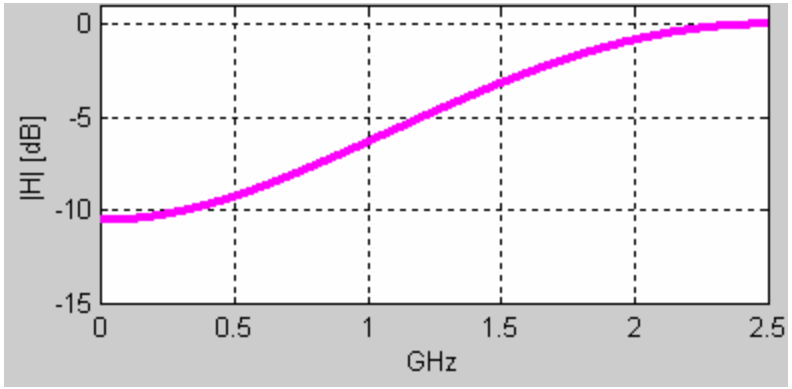

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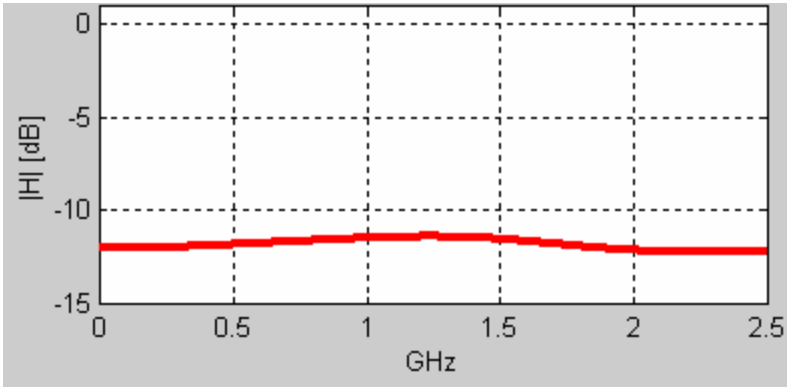
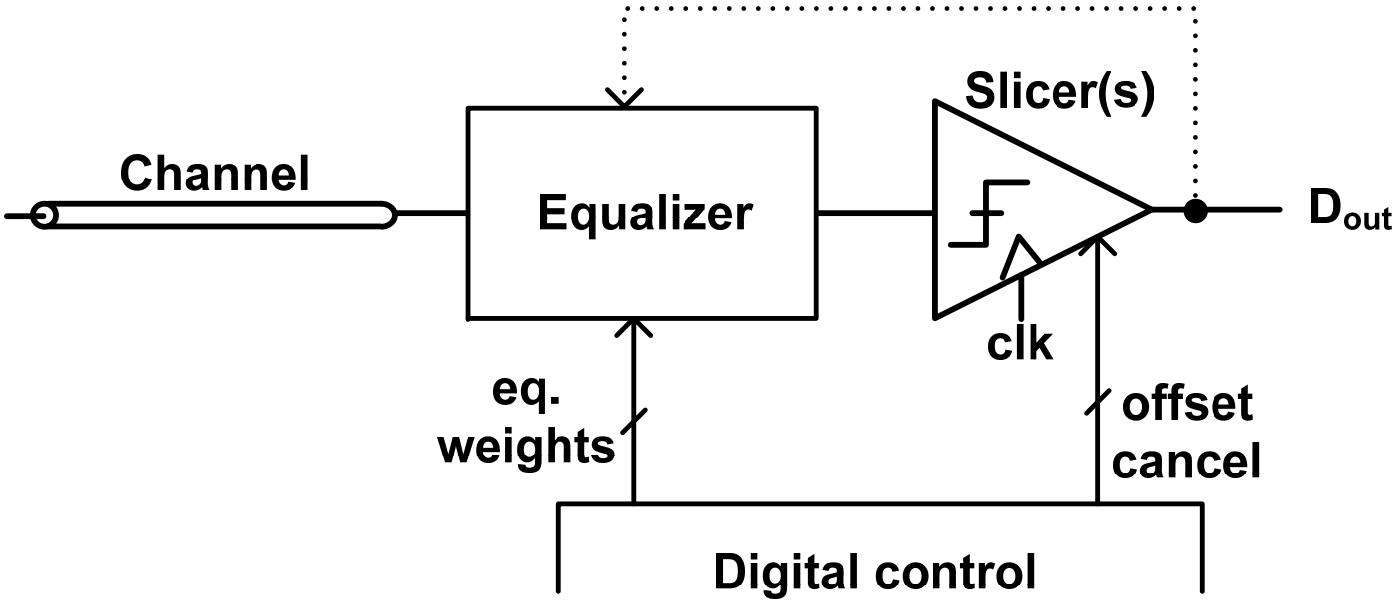


- Basic goal is to "flatten" channel response
  - I.e., in time domain, get back our nice clean pulse

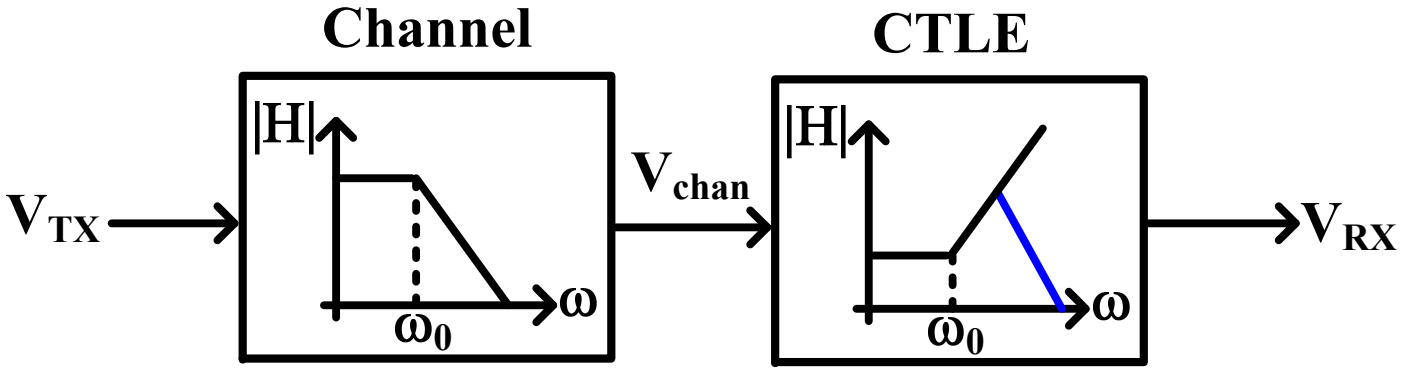
More Complete RX AFE



- Let's look at the types of equalizers we will need
  - Note that equalization is also often done on TX
  - But equalization burden is increasingly moving to RX

Continuous Time Linear Equalizer (CTLE)

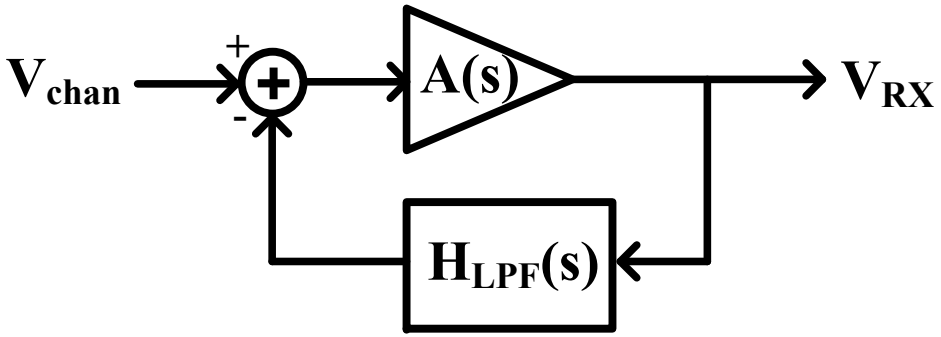
- Basic idea: build an analog circuit that approximates the inverse of the channel



- Can't (and don't need to) exactly invert – finite gain @ high f
  - CTLE bandwidth set by data-rate: typically ~2/3*(1/T_{bit})

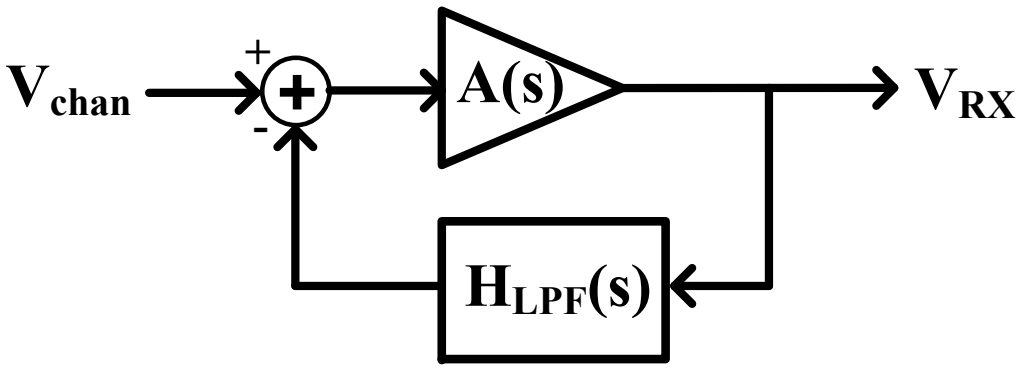
CTLE Implementation, Limitations (1)

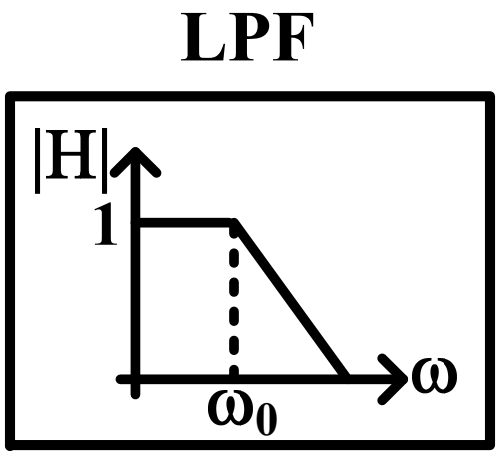
- Often implemented using implicit or explicit negative feedback:

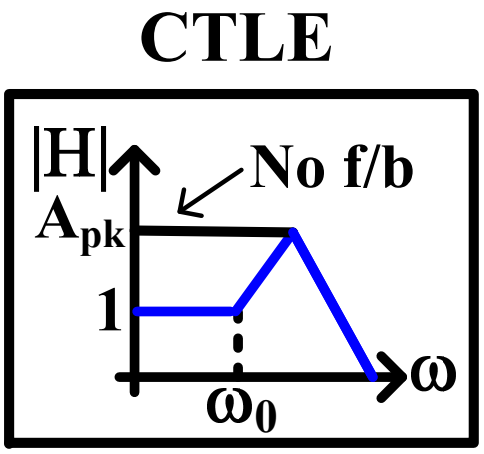


- Low-pass filter usually built out of R's and C's
  - Easy & efficient way to implement large time constants
  - Most effective with small # of poles & zeros
- May be hard to match complicated channels
  - Usually combined with a discrete-time equalizer

CTLE Implementation, Limitations (2)

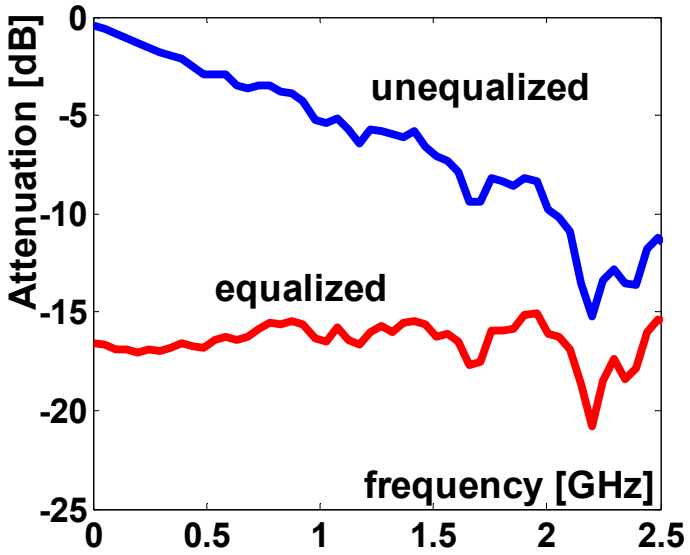




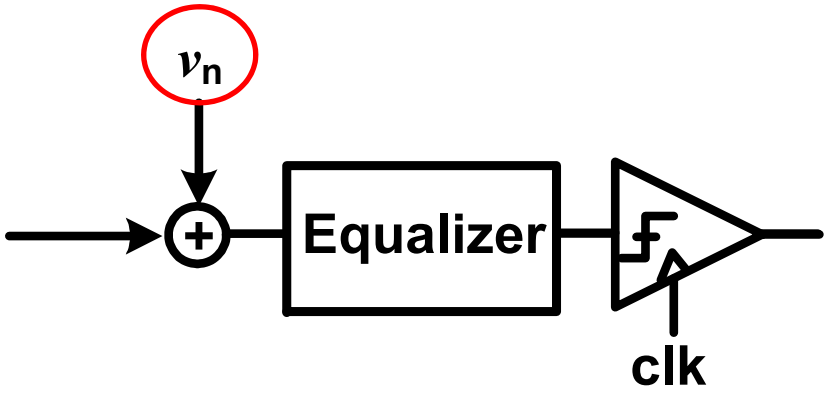


- Implication of feedback:
  - Equalization is actually achieved by throwing away gain at DC…

The Fundamental Issue: Noise



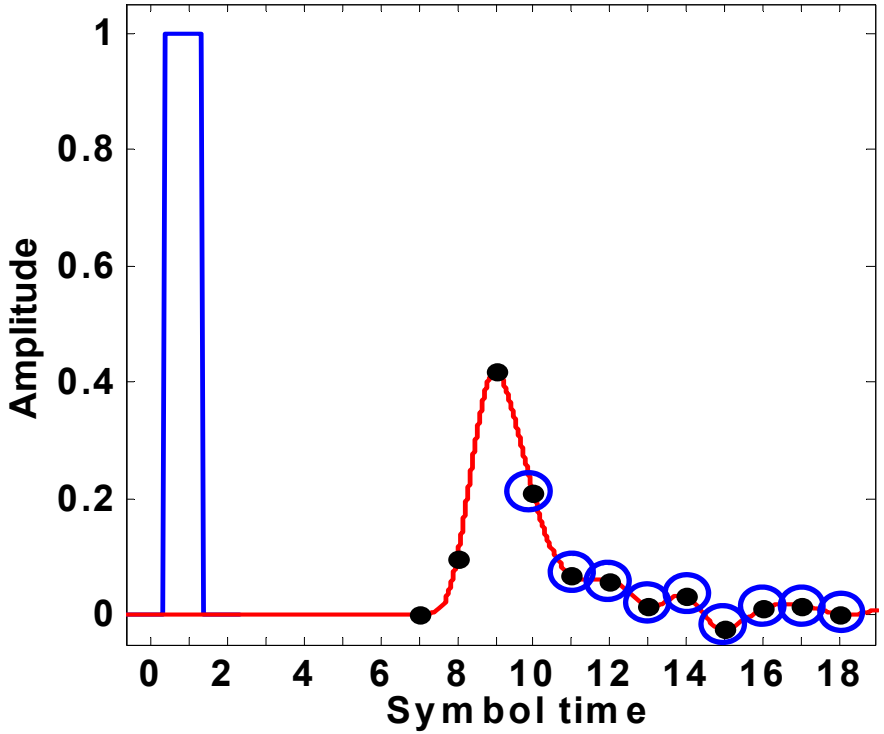
(figure from [2])



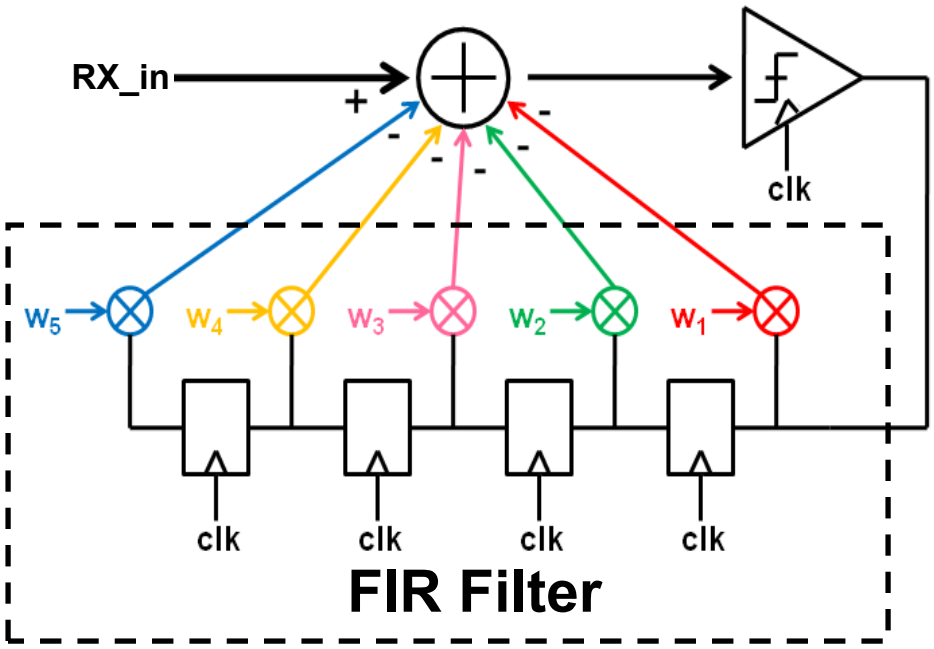
- Linear equalizers can eliminate ISI
  - But increase magnitude of noise (and high-f crosstalk) relative to signal
- Particularly bad on channels with notches
  - Equalizer needs large atten./gain

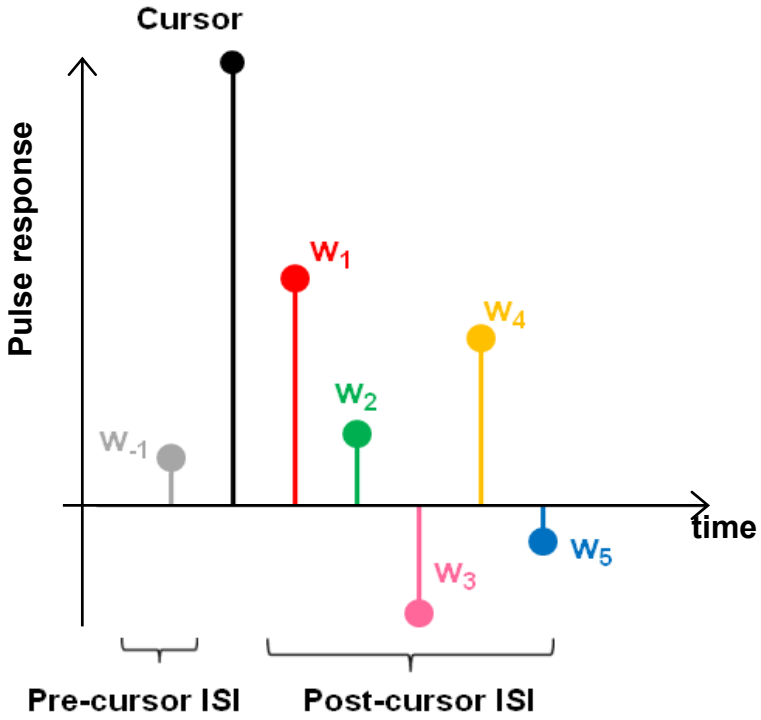
Good News: There is Another Way

- Once you know which bit was transmitted
  - You also know exactly what ISI that bit will cause
- Why not directly cancel the ISI you know is coming?



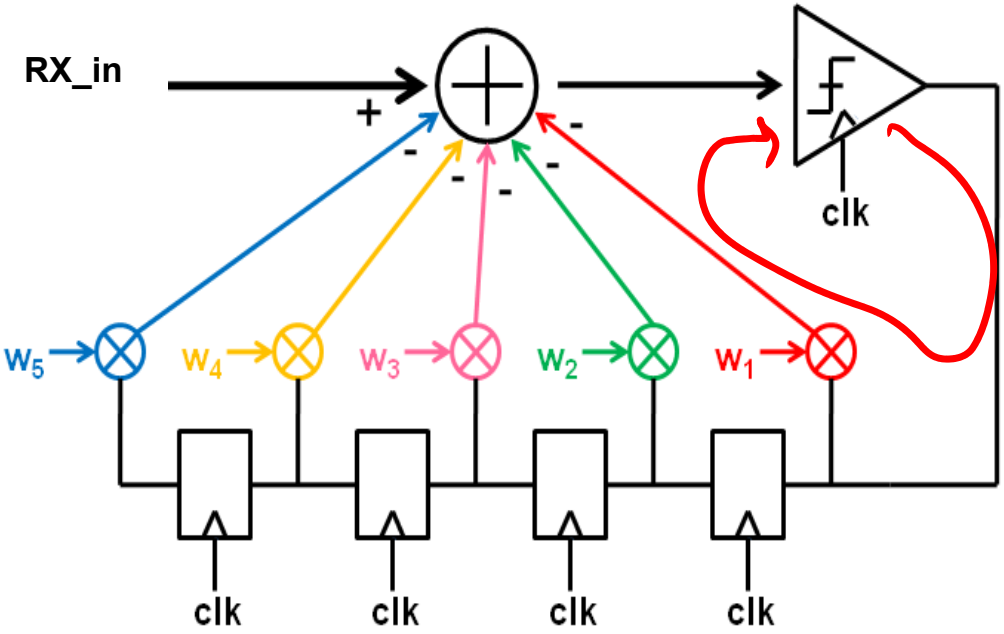
Decision Feedback Equalization





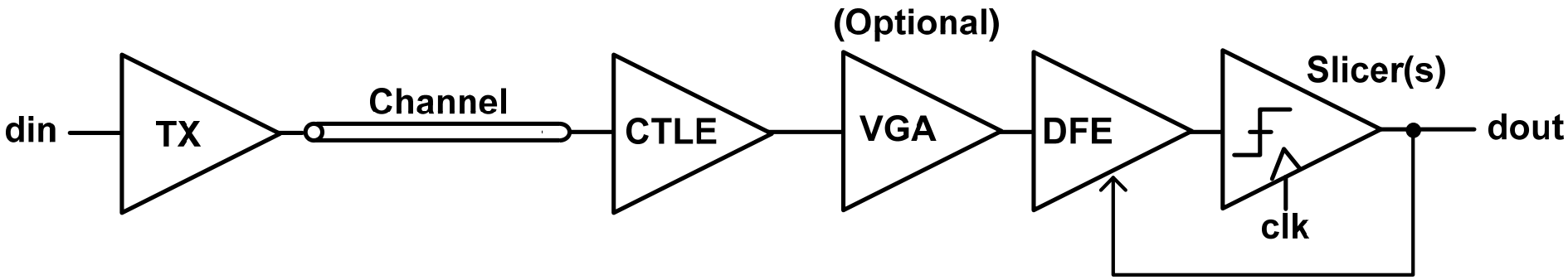
- Key advantage: no noise penalty
  - Feedback is based on "perfect" digital bits
  - ISI subtracted based on those bits

Key Constraint: Timing



- Need to do all of the following in at most 1 T_{bit}:
  - Resolve the (small) input voltage
  - Scale the bit by the coefficient
  - Sum the new analog value

Complete Signal Chain

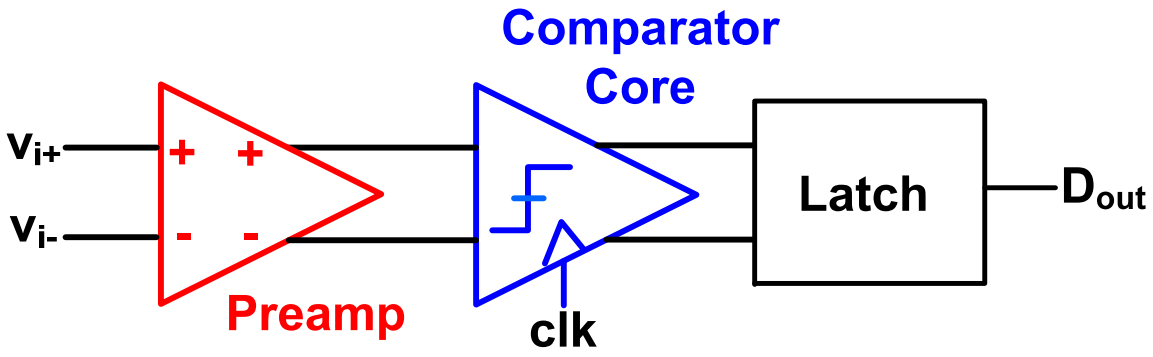


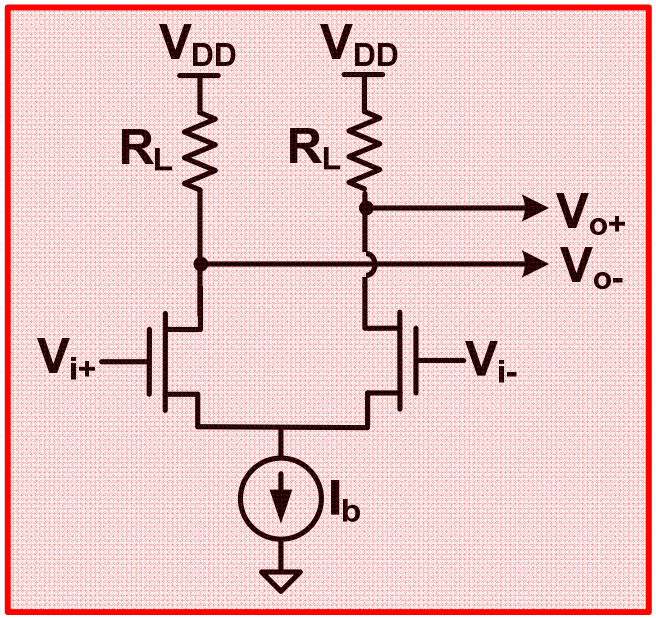
- VGA sometimes included to ensure DFE processes its input linearly
  - So that a linear FIR filter can be used to cancel the ISI
  - More later

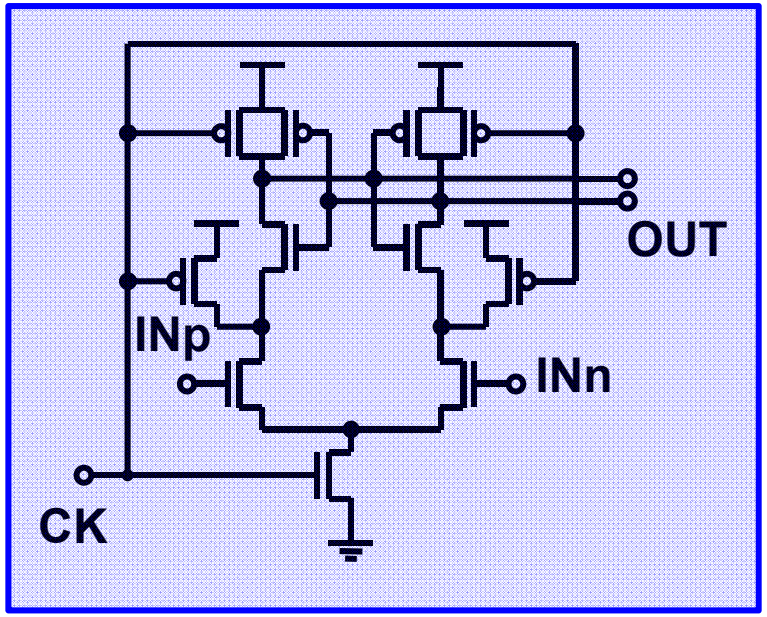
Tutorial Outline

- RX AFE Basics
- **RX AFE Circuits & Power Analysis**
  - Comparator
  - CTLE
  - VGA
  - DFE
- Practical Issues and Common Gotchas
- Key Lessons

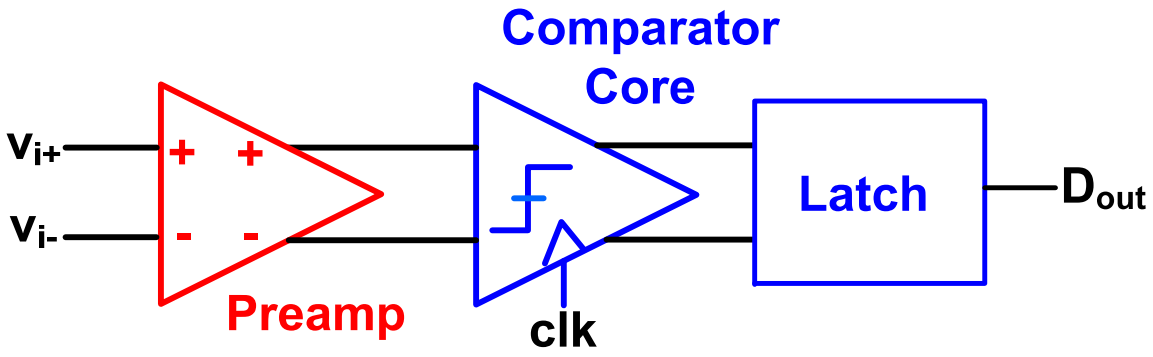
Comparator Circuit Design







Comparator Power Consumption



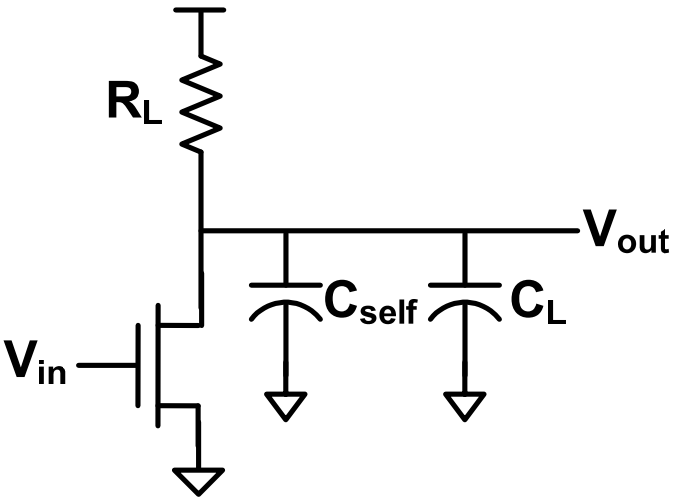
- Comparator core and latch typically just like digital gates:

$$P_{core,latch} = C_{sw,tot} V_{DD}^{\ 2} f_{clk}$$

- Let's look more carefully at preamp power

Preamp Power Consumption (1)

- Single-ended equiv. circuit:



- Reminder and definition:

$$\frac{g_m}{C_{self}+C_L} = A_V \omega_{bw}$$

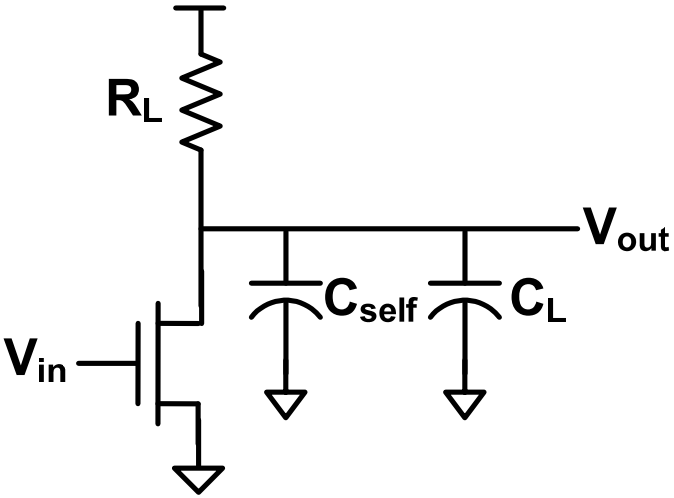
$$C_{self} = \gamma \frac{g_m}{\omega_T}$$

- So:

$$g_m = \frac{A_V \omega_{bw} C_L}{1 - A_V \omega_{bw} / (\omega_T / \gamma)}$$

Preamp Power Consumption (2)

- Single-ended equiv. circuit:



$$g_m = \frac{A_V \omega_{bw} C_L}{1 - A_V \omega_{bw} / (\omega_T / \gamma)}$$

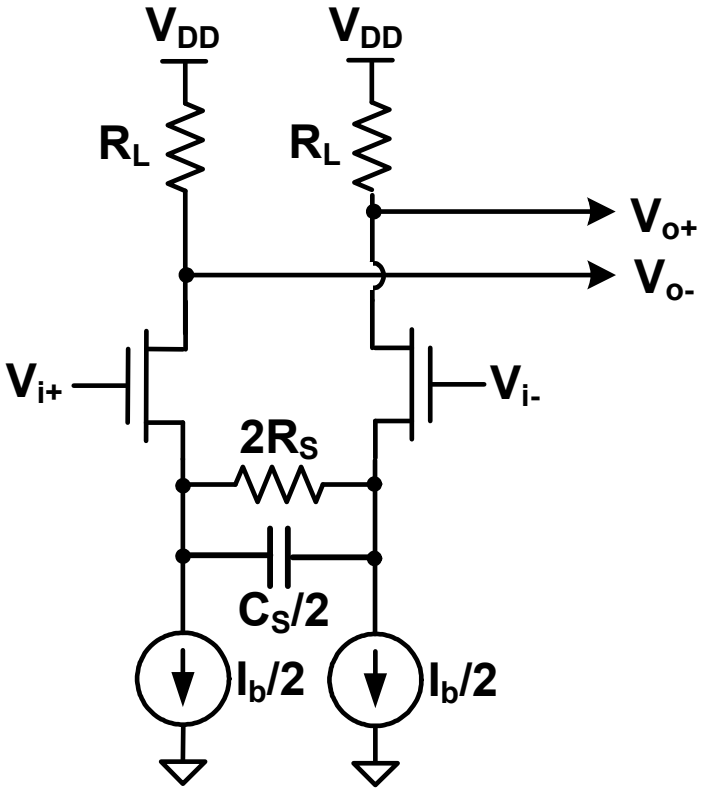
$$V^* \equiv \frac{I_D}{g_m} \text{ (diff. pair)}$$

$$I_{bias} = \frac{A_V \omega_{bw} V^* C_L}{1 - A_V \omega_{bw} / (\omega_T / \gamma)}$$

- Typical 20Gb/s numbers in 65nm:
  - A_v = 2, ω_{bw} = 80Grps, V* = 200mV, C_L = 10fF, ω_T = 400Grps
  - **I_{bias} = 533μA**

CTLE Circuit Design

- Most common design: source-degenerated
  - Excellent linearity – more later



- At system level, really only care about:
  - ω_{zero} ← set by channel pole(s)
  - ω_{bw} ← CTLE BW (data-rate)
  - A_{pk} ← peak gain
  - A_{DC} ← DC gain

CTLE Design Equations (Simplified)

System	Circuit
$A_{pk} = g_m R_L$	$g_m = A_{pk}\omega_{bw} C_L$
$\omega_{bw} = \frac{1}{R_L C_L}$	$R_L = \frac{1}{\omega_{bw} C_L}$
$\frac{A_{pk}}{A_{DC}} = \left(1 + g_m R_s\right)$	$R_s = \left(\frac{A_{pk}}{A_{DC}} - 1\right)\frac{1}{g_m}$
$\omega_{zero} = \frac{1}{R_s C_s}$	$C_s = \frac{g_m}{\omega_{zero}} \frac{A_{DC}}{\left(A_{pk} - A_{DC}\right)}$

CTLE Power Consumption

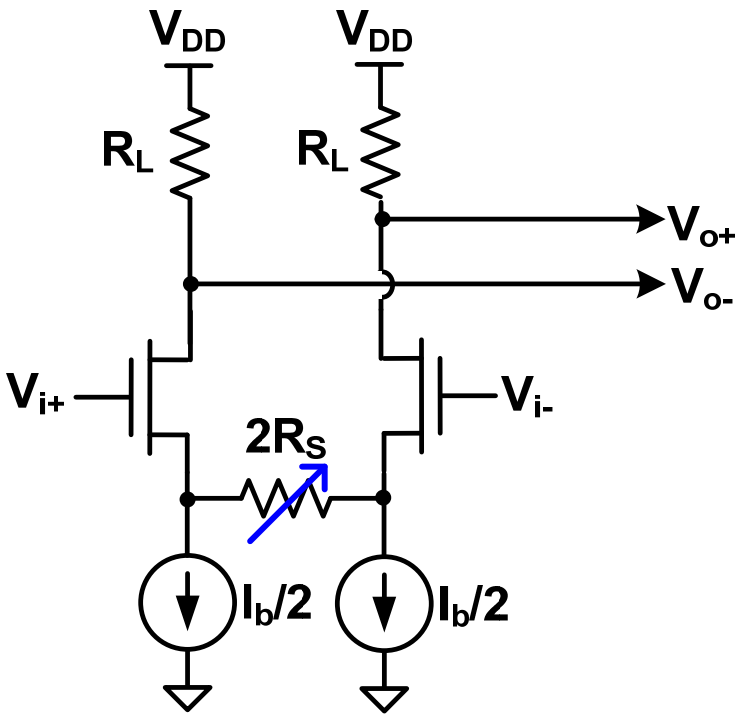
- Identical equation as preamp:

$$I_{bias} = \frac{A_{pk}\omega_{bw}V^{*}C_{L}}{1 - A_{pk}\omega_{bw}/(\omega_{T}/\gamma)}$$

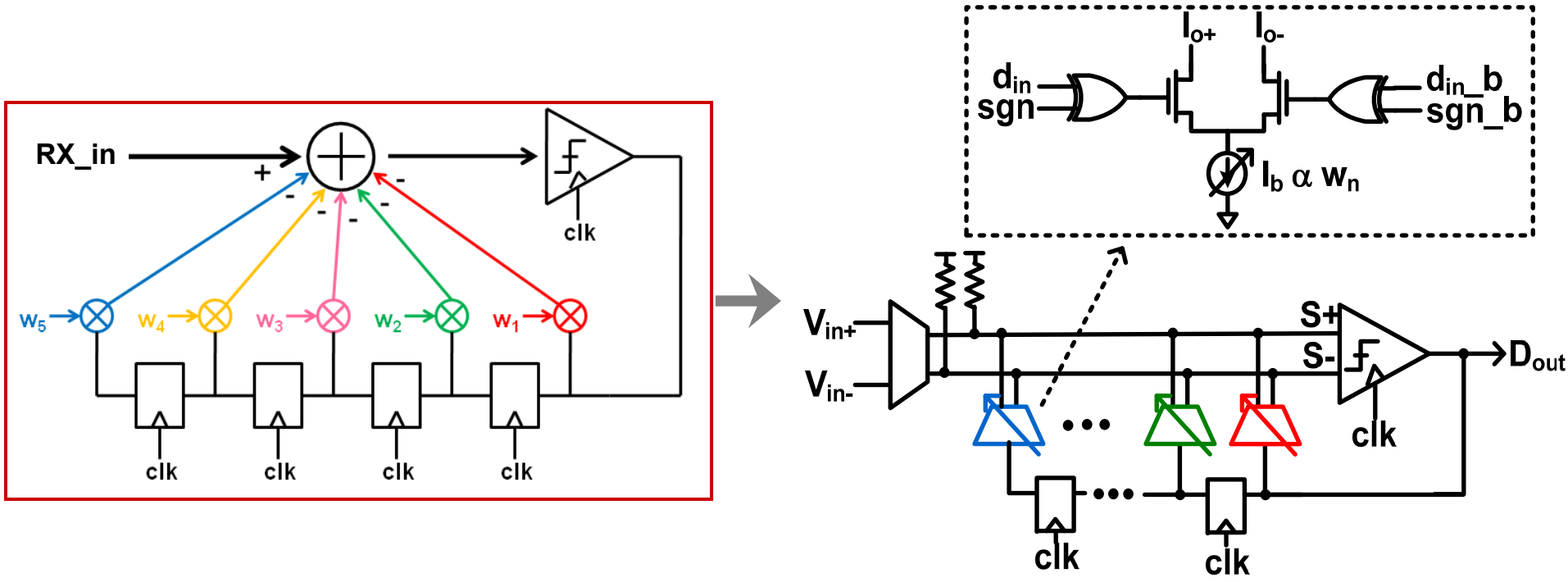
- (Remember, CTLE is just an amplifier with gain reduced at low frequencies)

VGA Implementation and Power

- Many possible implementations
- Source degeneration again attractive:
  - Better linearity when gain is low
  - (Ideally) no extra loading on signal path
- Equation for power once again identical to preamp
  - Set by max. achievable gain

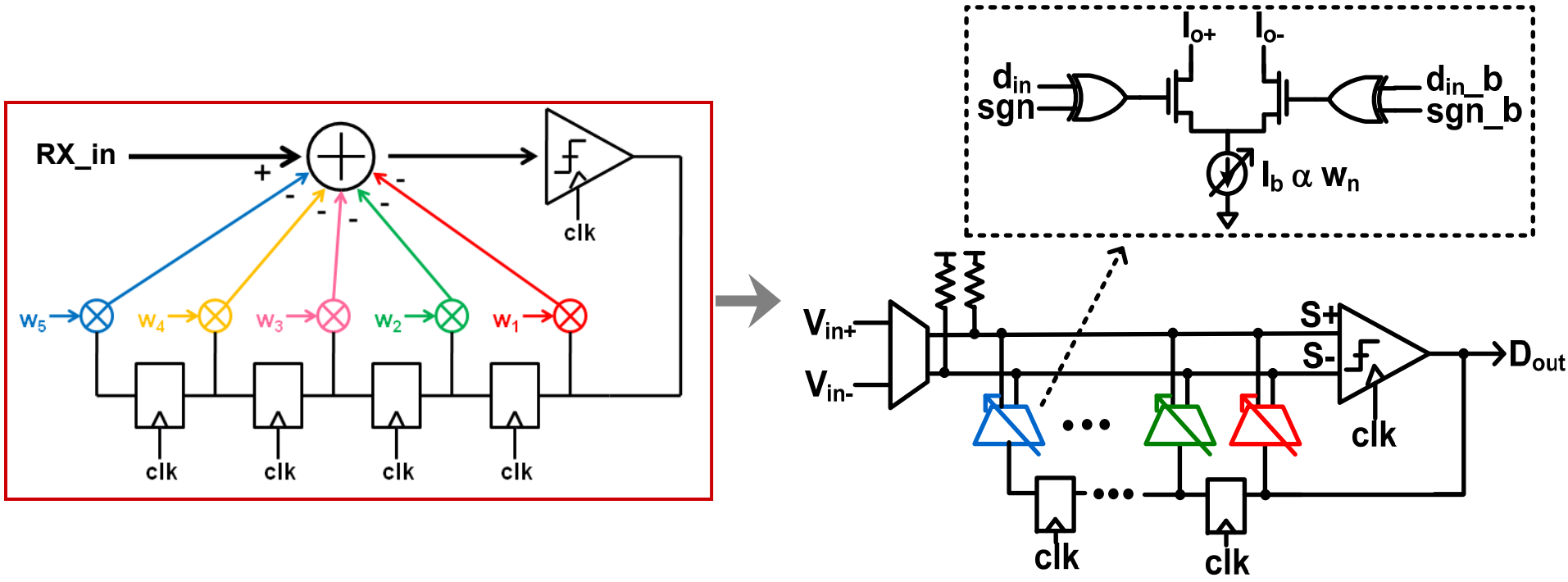


DFE Implementation (1)



- Mixed-signal FIR filter:
  - Digital delay
  - Analog scaling/summation

DFE Implementation (2)

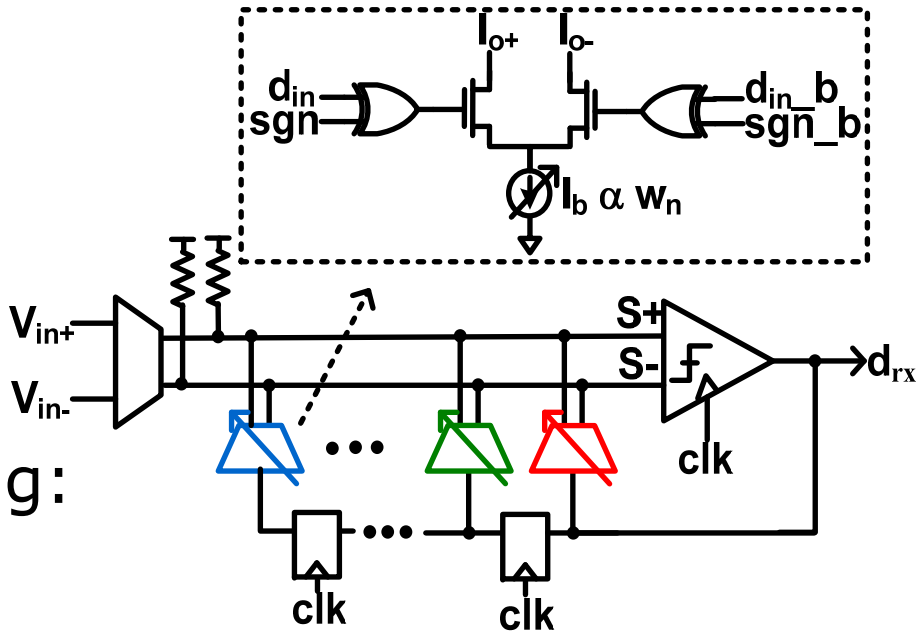


- Design driven by feedback latency constraint
  - Summer output must settle within one bit time

DFE Summer Design

- Key constraint:

$$t_{dig\_fb} + t_{ana\_settle} = T_{bit}$$



- Need some N_τ of settling:

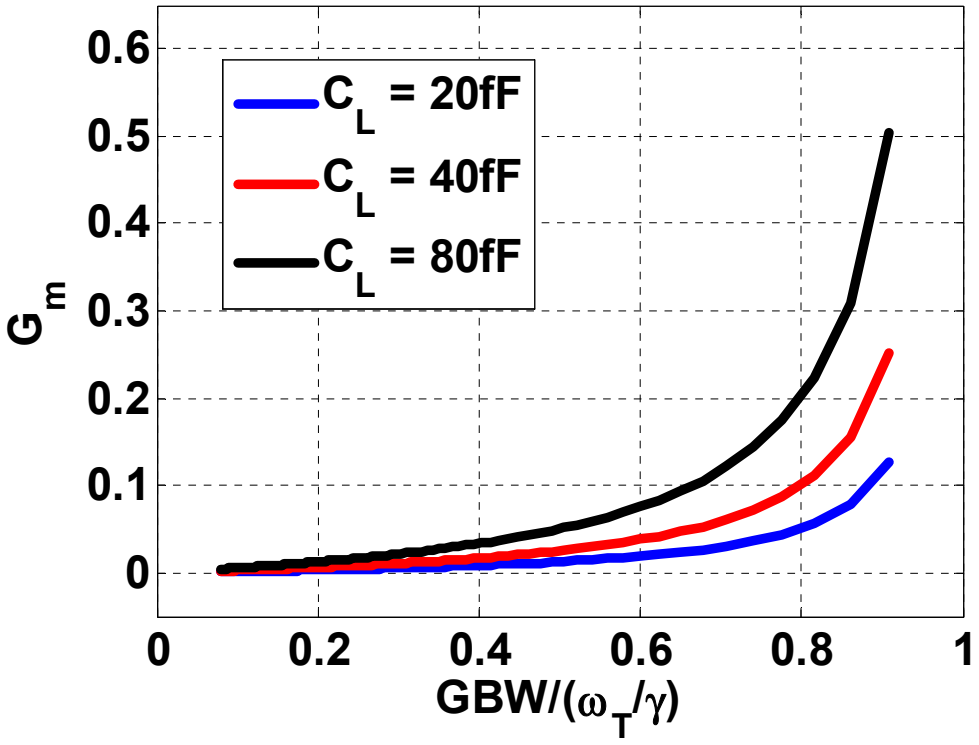
$$\tau_{sum} = (T_{bit} - t_{dig\_fb})/N_\tau$$

  - Typically want ~4τ for ~98% settling

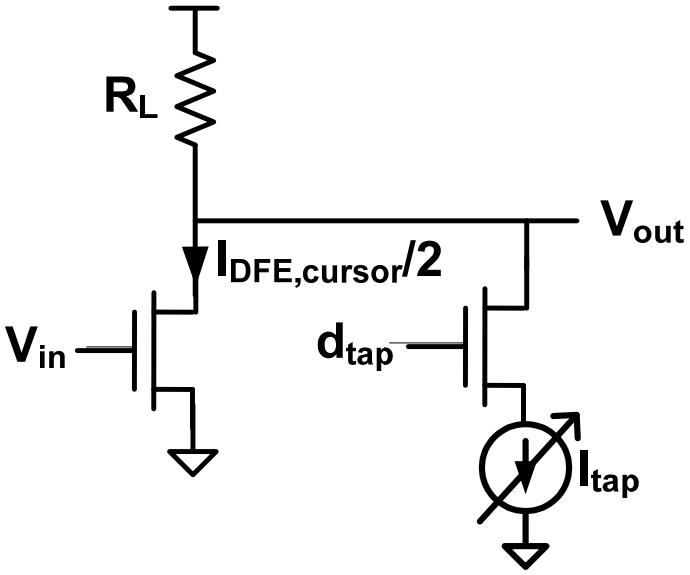
A Reminder: Self-Loading

$$I_{bias} = \frac{A_V \omega_{bw} V^* C_L}{1 - A_V \omega_{bw} / (\omega_T / \gamma)}$$

- Creates bandwidth limit
  - No matter how much power you spend
- DFE has increased "self-loading" due to taps…



DFE Summer Power Consumption



- Definition:

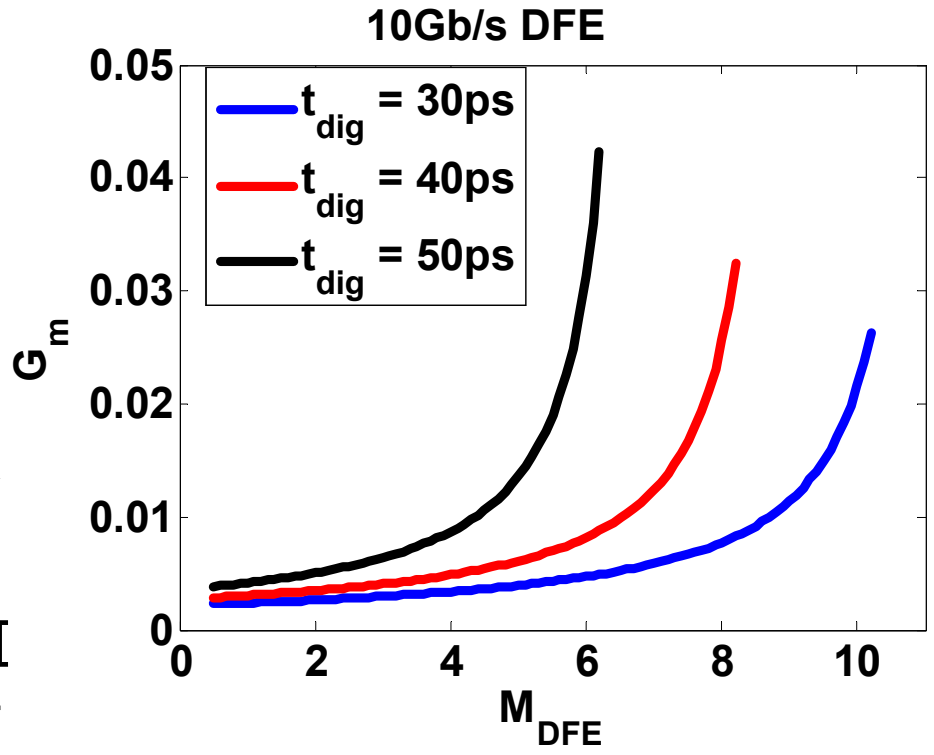
$$M_{DFE} = \frac{V_{out,tap}}{V_{out,cursor}} = \frac{I_{tap}}{g_m V_{cursor}}$$

- Assuming same biasing for tap & cursor devices (see [4]):

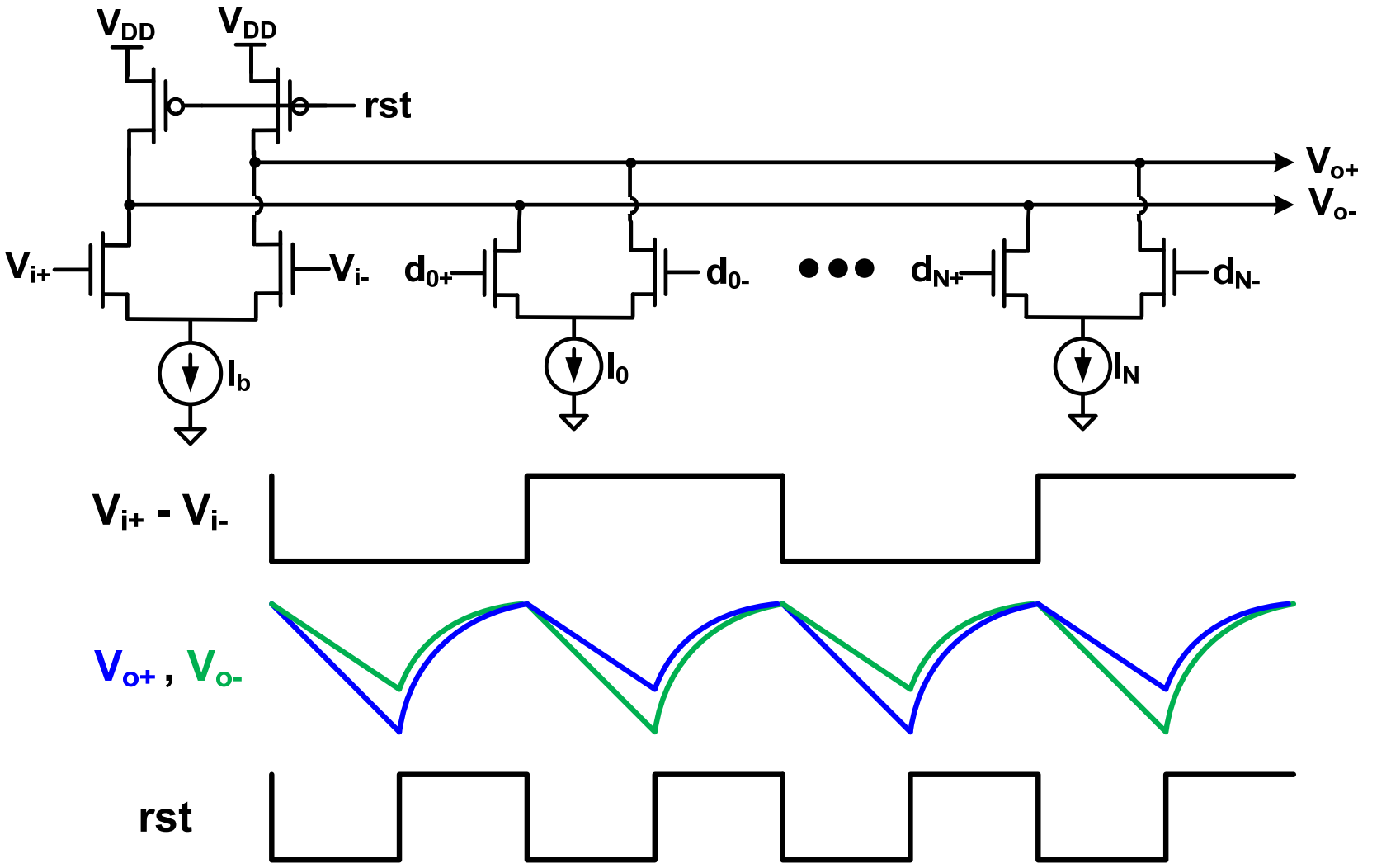
$$I_{DFE,curosr} = \frac{A_v V^* C_L N_\tau \Big/ \left(T_{bit} - t_{dig}\right)}{1 - \left(1 + \frac{2M_{DFE} V_{cursor}}{V^*}\right) \frac{A_v N_\tau \Big/ \left(T_{bit} - t_{dig}\right)}{\left(\omega_T / \gamma\right)}}$$

Implication

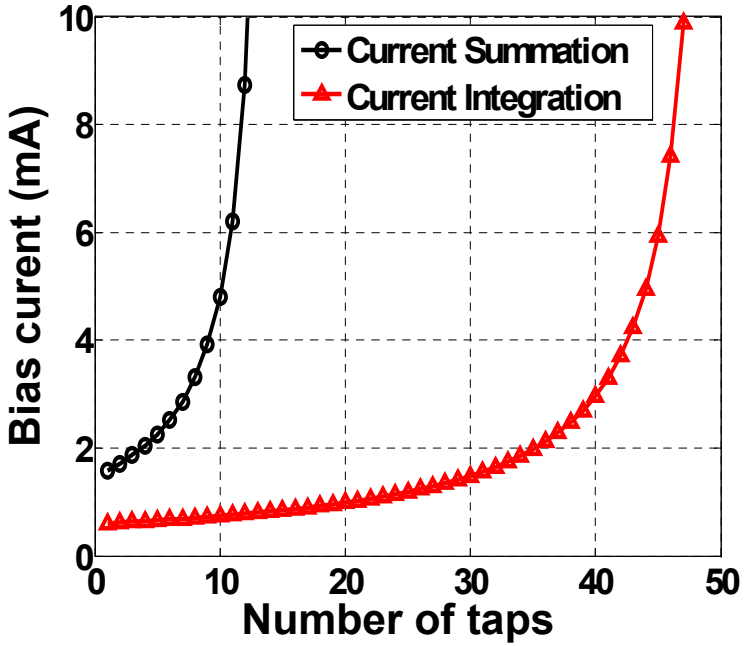
- There is a maximum M_{DFE} you can achieve
- Don't forget that every tap has to handle worst-case possible ISI
  - Implies max. number of taps (in given tech.)
- What if you need more taps/larger M_{DFE}?



Current Integrating Summer[5]



Why Current Integration Helps



- Maximizes load impedance
  - ISI eliminated by resetting
- Power/number of taps improved by N_τ:

$$I_{DFE,curosr} = \frac{A_v V^* C_L \Big/ \left(T_{bit} - t_{dig}\right)}{1 - \left(1 + \frac{2M_{DFE} V_{cursor}}{V^*}\right) \frac{A_v \Big/ \left(T_{bit} - t_{dig}\right)}{\left(\omega_T / \gamma\right)}}$$

Example DFE Power Numbers

- 20Gb/s 10-tap DFE in 65nm (same process/bias as preamp example)
  - M_{DFE} = 2.5, V_{cursor} = 75mV, t_{dig} = 25ps, A_v = 1, C_L = 30fF
- Current integration summer power: ~337μA
- Digital power (flip-flops, XORs, etc.): ~2mA w/1V V_{DD}
  - Typically ~10fF switching cap/tap

Tutorial Outline

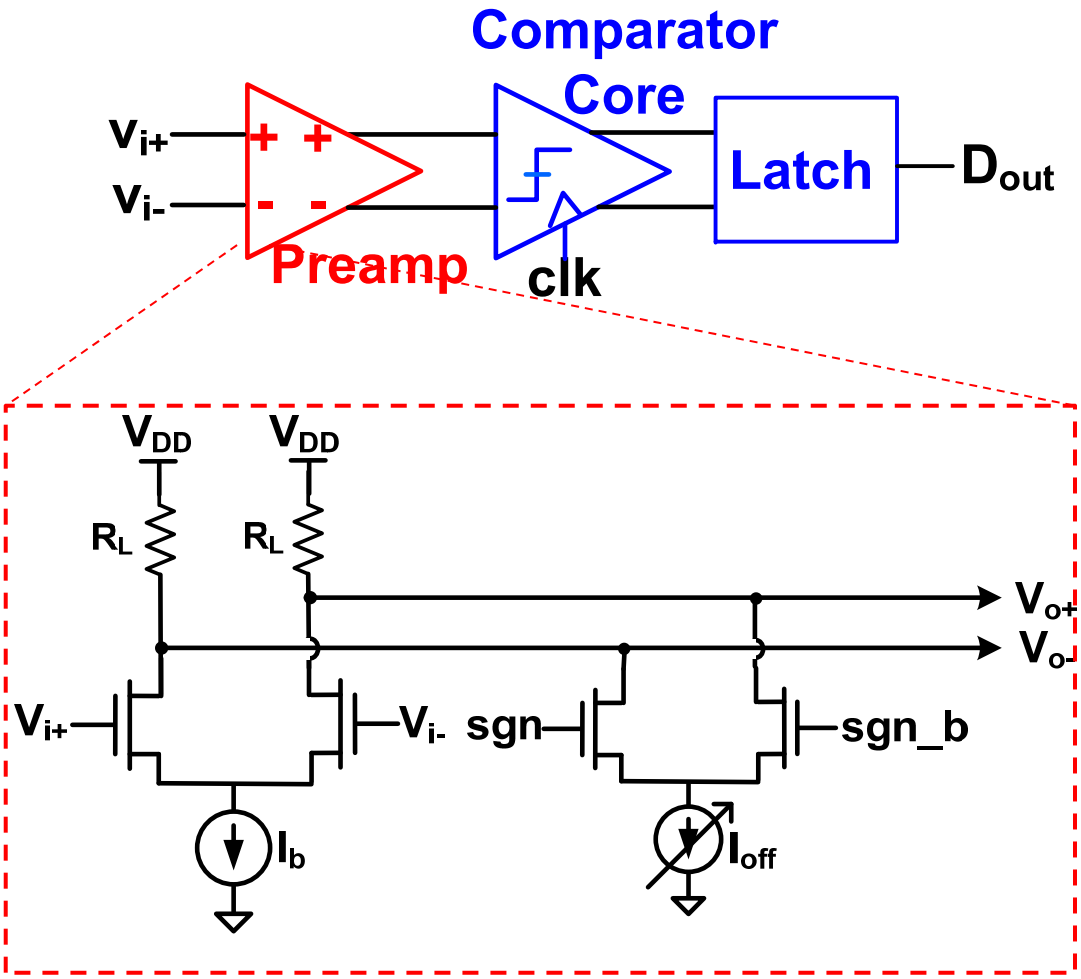
- RX AFE Basics
- RX AFE Circuits & Power Analysis

- **Practical Issues and Common Gotchas**

- Key Lessons

Comparator Offset Cancellation

- Never fight offset with sizing
  - 4X penalty in capacitance and hence power for 2X reduction in offset
- Preamp is a convenient point to cancel offset
  - Keeps cancellation DAC parasitics off of the signal path



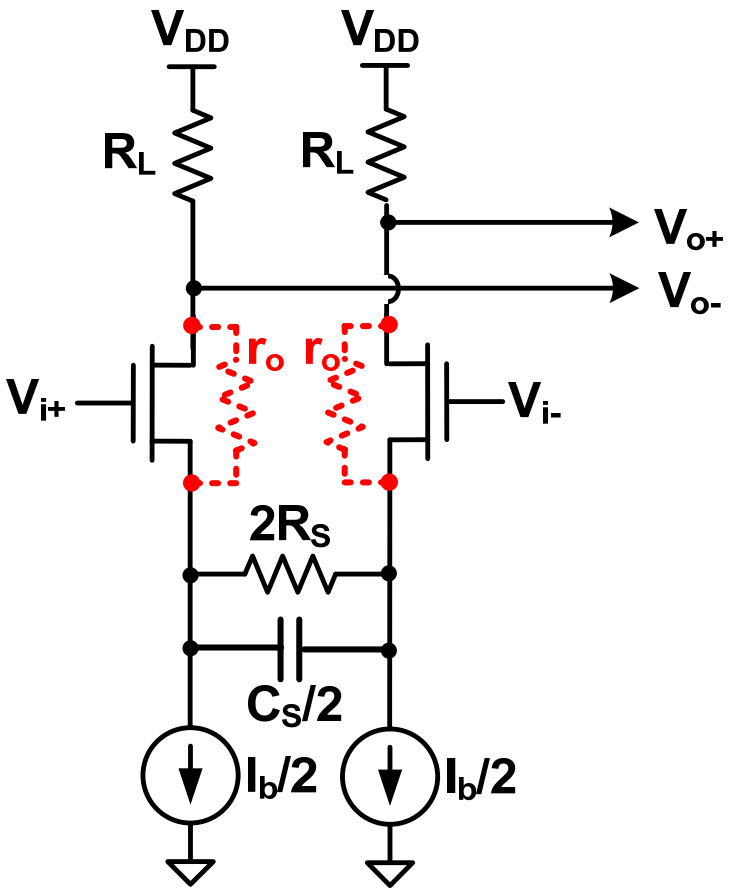
CTLE Design Issues (1)

Cause:

- Finite input device r_o

Effects:

- Couples source and drain dynamics
- Makes precise setting of poles/zeros more difficult



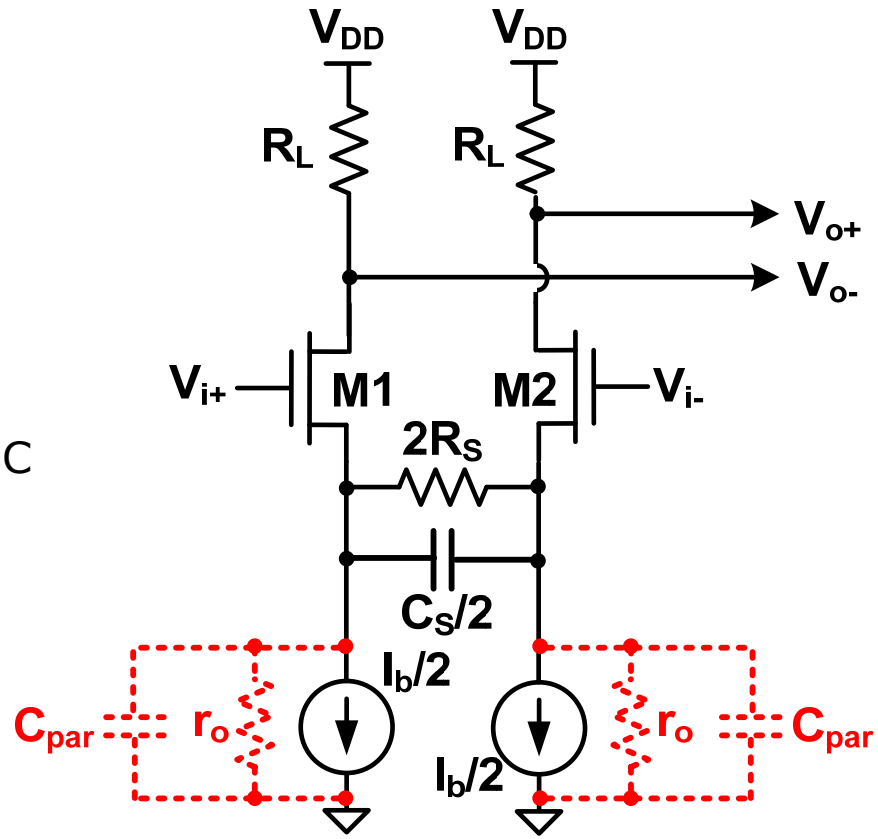
CTLE Design Issues (2)

Cause:

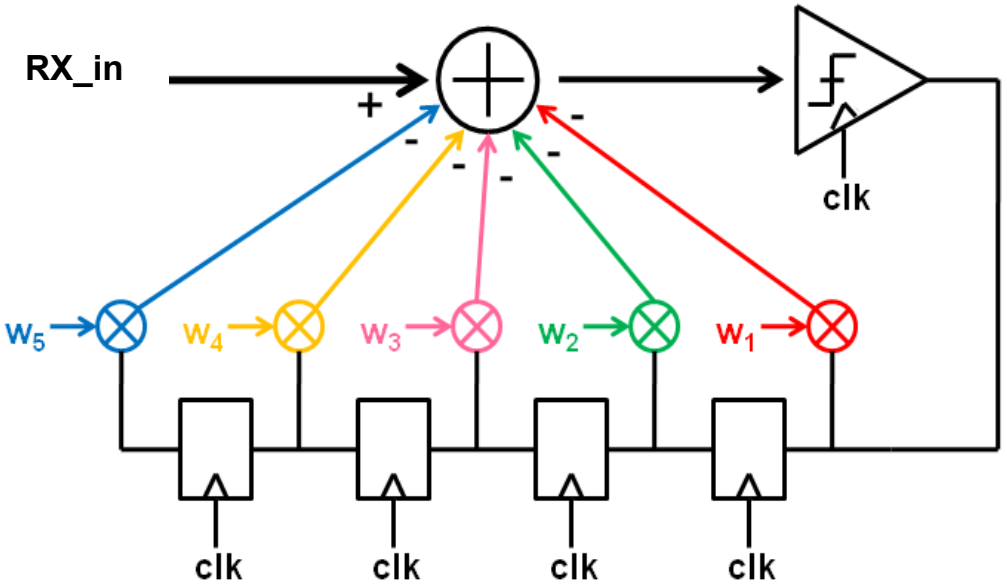
- Tail device r_o, C_{par}

Effects:

- r_o limits maximum A_{pk}/A_{DC}
- C_{par} limits maximum ω_p
  - I.e., pole @ source associated with ω_{zero}



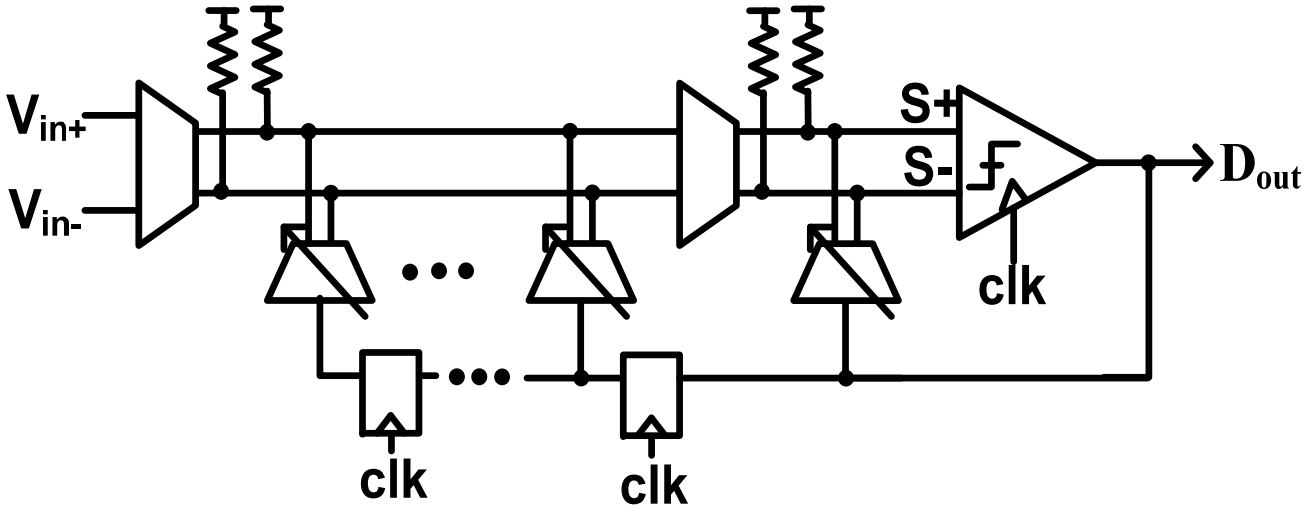
DFE Design: Closing the First Tap



- First tap timing often the most challenging
  - Other taps already have digital inputs
  - First tap must resolve/amplify small analog input signal

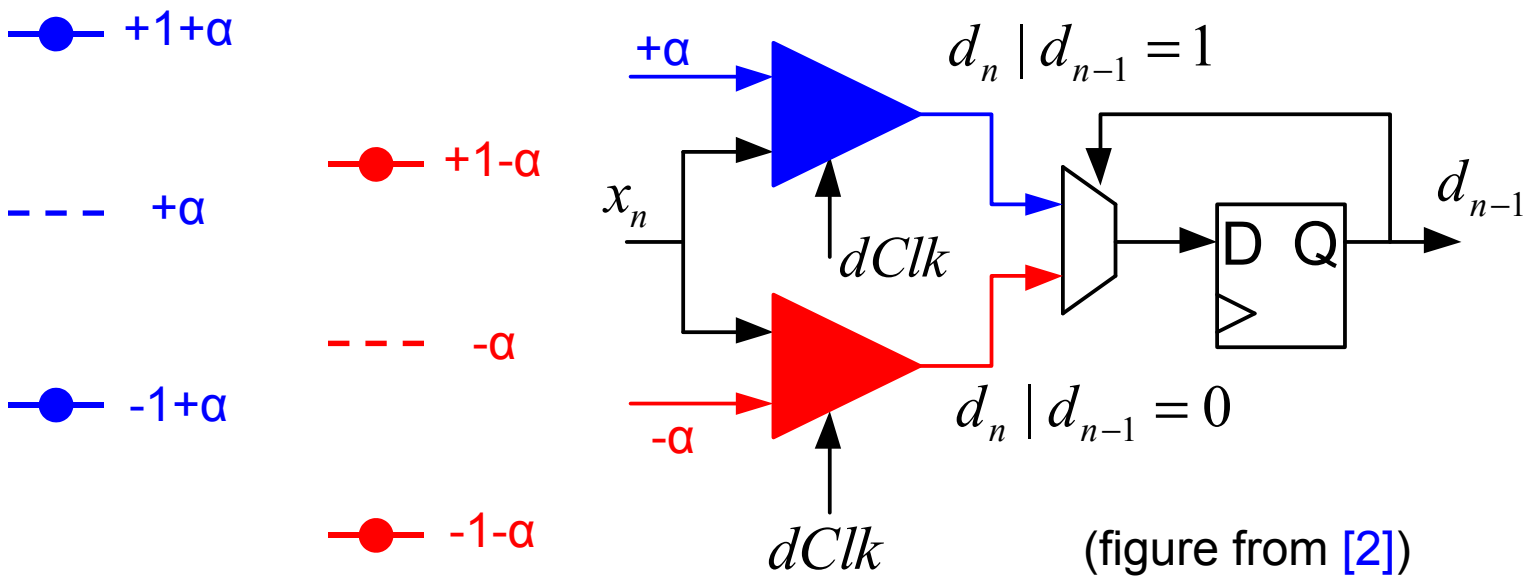
    → Larger "t_{dig}"

Option 1: Split Summation[6]



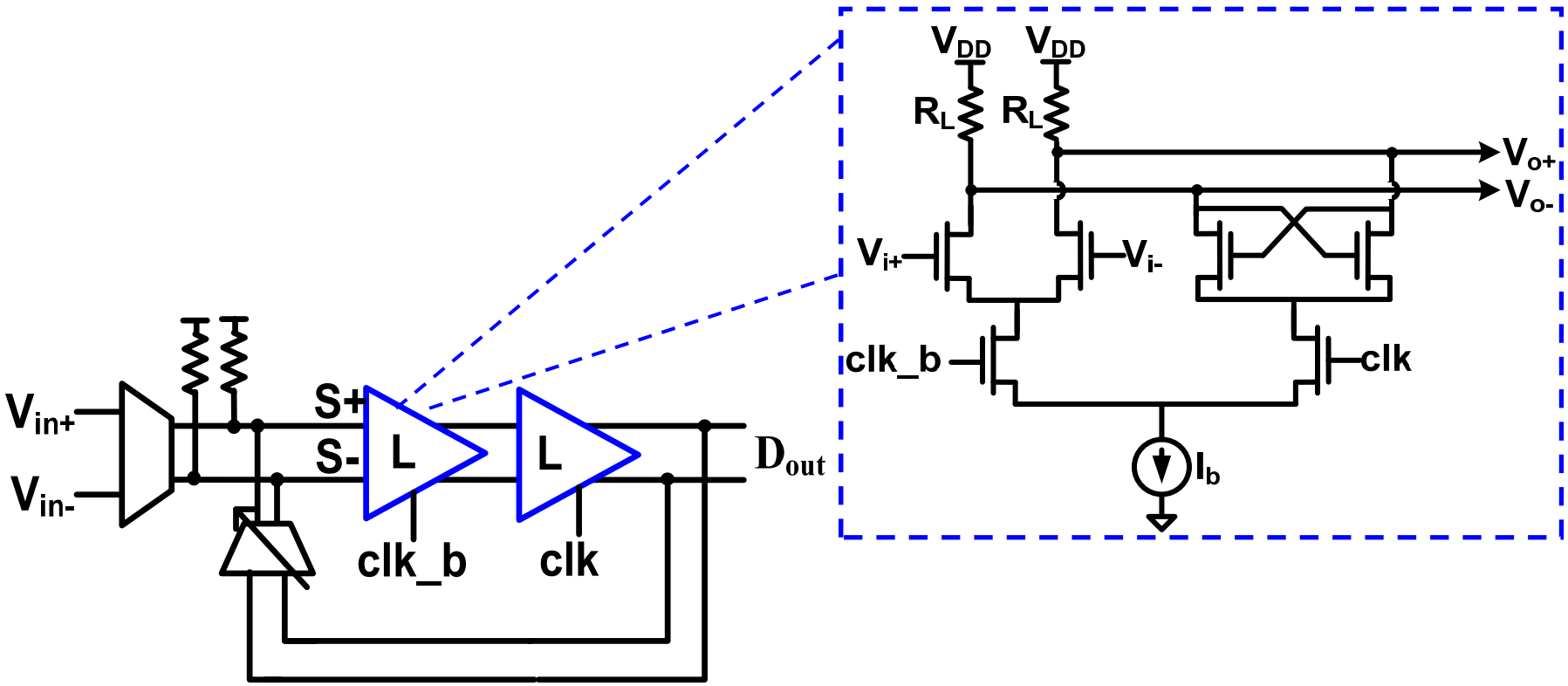
- Faster summer (less self-loading) for 1st tap
- Watch out for non-linearity
  - First summer (later taps) may distort the signal

Option 2: Loop Unrolling[7]



- Pushes feedback loop into digital domain
- Watch out for later taps (if there are any) though
  - MUX adds extra latency

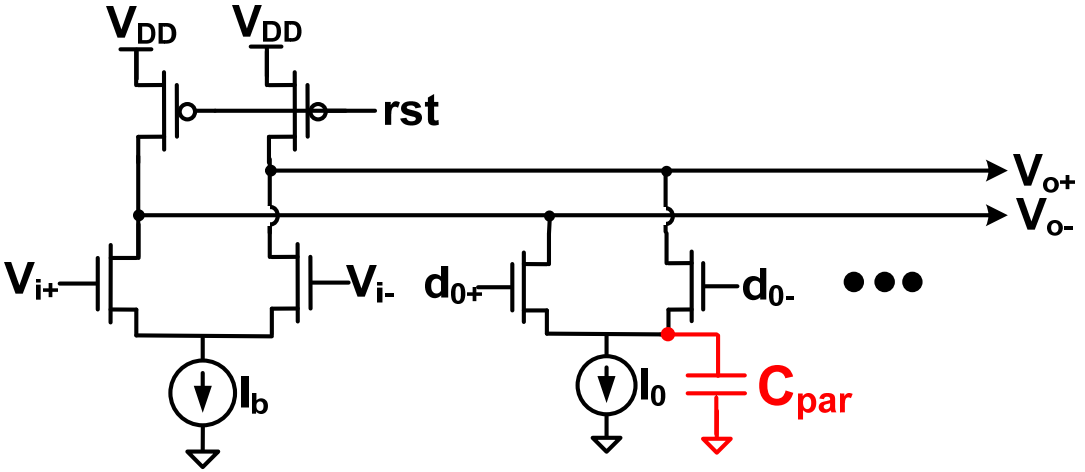
Option 3: All CML Design[8]

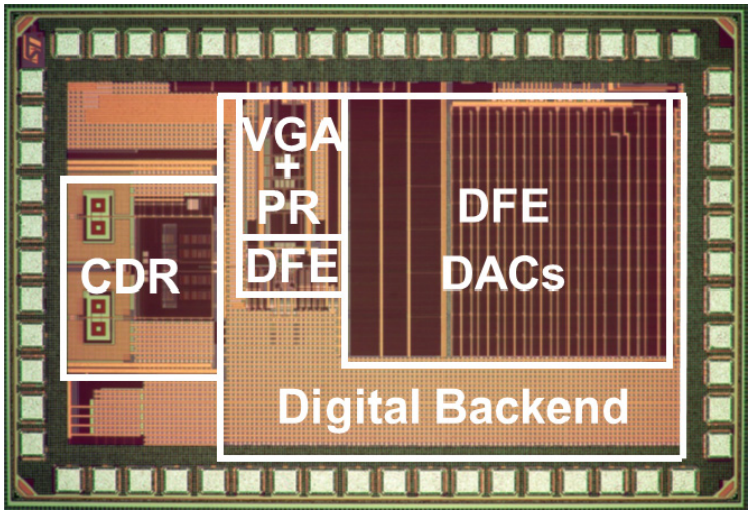


- Reduces required comparator gain
- [9] demonstrated over 20Gb/s in 65nm CMOS

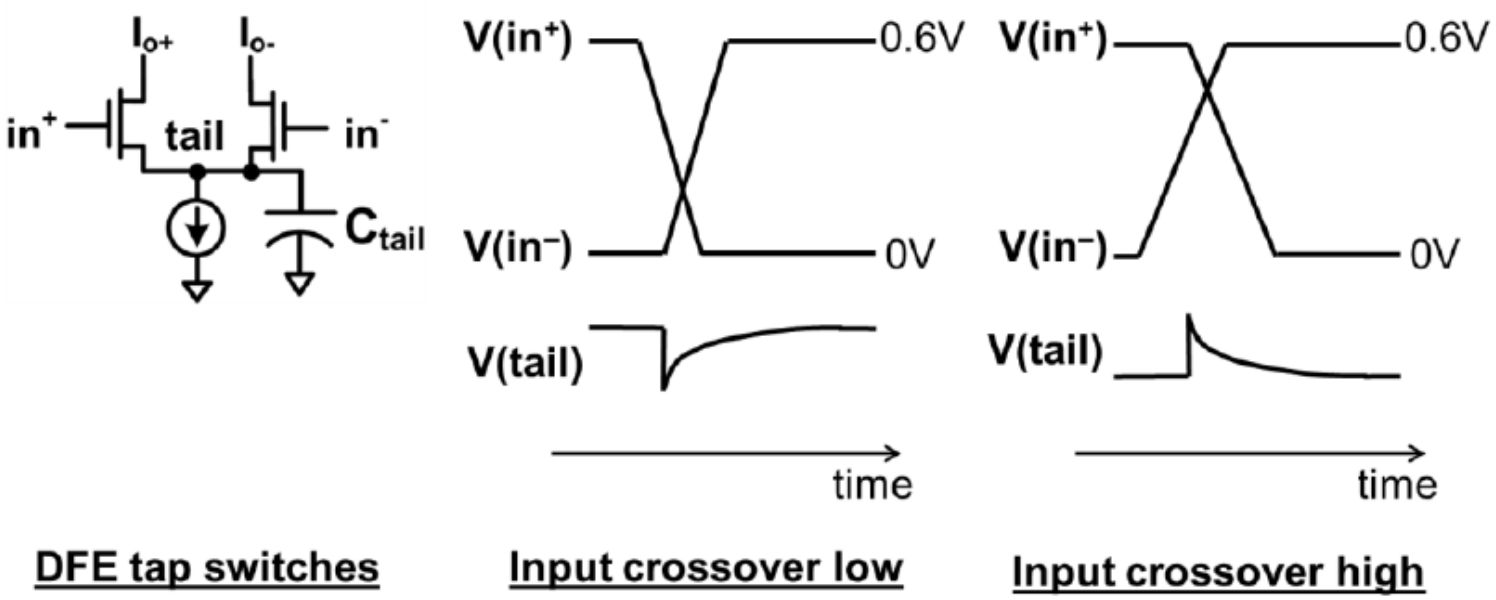
DFE Physical Design

- Tap DACs must be high resolution, hence large
- Don't want DACs to increase size (cap) of signal path
  - DACs placed far away
- Result: large C_{par}…



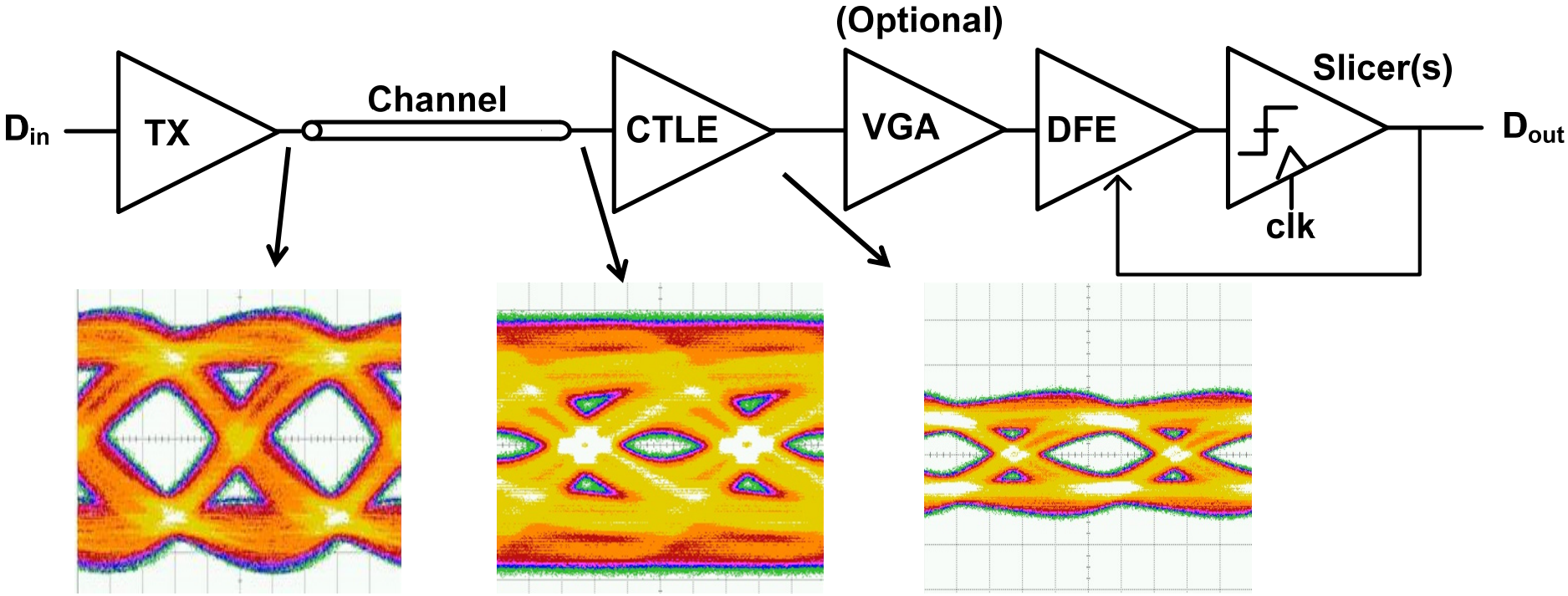


Impact of Tap Tail Capacitance



- Leads to signal-dependent glitches in DFE response
- Good news: adaptation can & will correct these errors[4]

Complete Signal Path: Linearity



- Ordering of components on RX matters
  - Especially in systems with large TX swing
- CTLE should always be first
  - Reduces dynamic range caused by ISI

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Key Take-Home Lessons (1)

- Receiver AFE circuit power easy to predict
  - Calculate power early and often – feed back to system design
- Analog circuits themselves can be very low power
  - Even for many taps (DFE)
  - Power often dominated by large number of high-speed digital structures (flops)

Key Take-Home Lessons (2)

- Minimize dynamic range on the high-speed signal path
  - Watch out for block ordering
  - Keep DACs for e.g. offset cancellation, channel adaptation off the signal path
- Think about the whole system!
  - Often opportunities to save power by moving functionality/problems from one place to another

ISSCC 2014 Papers to Check Out

- Papers 2.1, 26.1: Front-end design issues within state-of-the-art 20 - 28Gb/s transceivers
- Papers 2.4, 2.5: Extremely energy-efficient 16-25Gb/s front-ends based on current-integration and charge domain techniques

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Selected References

[1] J. Zerbe et al., "Equalization and Clock Recovery for a 2.5 – 10Gb/s 2-PAM/4-PAM Backplane Transceiver Cell," *IEEE JSSC*, Dec. 2003

[2] V. Stojanovic et al., "Modeling, Analysis, and Design of High-Speed Links," Ph.D. thesis, Stanford University, Dec. 2004.

[3] S. Shekhar et al., "Design Considerations for Low-Power Receiver Front-End in High-Speed Data Links," *IEEE CICC*, Sept. 2013

[4] C. Thakkar et. Al, "A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS," *IEEE JSSC*, Apr. 2012

[5] M. Park et. al., "A 7Gb/s 9.3mW 2-Tap Current-Integrating DFE Receiver," *IEEE ISSCC*, Feb. 2007

[6] B. Leibowitz, et al., "A 7.5Gb/s 10-Tap DFE Receiver with First Tap Partial Response, Spectrally Gated Adaptation, and 2nd-Order Data-Filtered CDR," *IEEE ISSCC*, Feb. 2007

[7] K. K. Parhi, "High-speed architectures for algorithms with quantizer loops," *IEEE ISCAS*, May 1990

[8] H. Wang et al., "A 21-Gb/s 87-mW transceiver with FFE/DFE/linear equalizer in 65-nm CMOS technology ," *IEEE JSSC*, Apr. 2010