Quadrature Bandpass Delta-Sigma Modulation for Digital Radio

by

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A thesis submitted in conformity with the requirements for the degree of
Doctor of Philosophy
Graduate Department of Electrical and Computer Engineering
University of Toronto

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Department of Electrical and Computer Engineering
University of Toronto
Degree of Doctor of Philosophy
1997

Abstract

Considerable research effort in the field of microelectronics pushes towards the realization of fully monolithic, chiefly digital, RF transceivers — with the ultimate objective being the implementation of small, inexpensive, low-power communication devices that are robust, testable, and capable of handling multiple communications standards. Two-path zero-IF architectures and single-path bandpass-ΔΣ-based architectures strive to attain these dual goals, but neither effectively achieves both.

This thesis proposes a low-IF receiver architecture, which, with modern quadrature image-reject mixers and strategic IF placement, offers a viable solution for realizing digital, monolithic receivers. A critical, and heretofore non-existing, component of such a system — and indeed of any receiver that uses image-reject mixing to alleviate off-chip filtering requirements — is one that efficiently performs bandpass A/D conversion on quadrature signals.

A quadrature variant of a bandpass delta-sigma (ΔΣ) modulator is thus proposed, which offers significant theoretical and practical performance advantages over the alternative of a pair of traditional bandpass ΔΣ modulators. The design of the transfer functions, systems and circuits needed to realize quadrature ΔΣ modulators are explored. Non-ideal effects are examined, interpreted, and combatted.

Unique code-driven layout techniques facilitate the implementation of a fourth-order prototype quadrature bandpass ΔΣ modulator in a 0.8-μm CMOS process. Clocked at 10 MHz, the IC converts narrow-band 3.75 MHz *I* and *Q* inputs, attaining 62-dB maximum SNDR and 67-dB dynamic range — true 10-bit accuracy — in 200-kHz (GSM) bandwidth. Moreover, the IC clearly demonstrates many of the theoretical predictions. Power consumption is 130 mW at 5 V. Die size is 2.4 x 1.8 mm^2.

Acknowledgments

To my thesis supervisors, Ken Martin and Adel Sedra, thank-you for your guidance and input. Ken, thank-you for keeping me on my toes, and for pushing me towards a complete thesis. Adel, thank-you for your clear insight into all things, and for your constant support and encouragement — you have a great deal of my respect; I hope I've managed a bit of the reverse.

To the members of my thesis committee, Professors Beno Benhabib, Glenn Gulak, David Johns, Frank Kschischang and Wai Tung Ng: thank-you for your input and comments. Many thanks to Professor Ian Galton for making the trek from San Diego.

To Richard Schreier and Martin Snelgrove, thank-you for introducing me to the intriguing world of bandpass delta-sigma modulation, years ago. To you, and to David Johns and John Long, thank-you for your continued interest in my thesis work, and my life. John, special thanks for the interesting chats and for your input and good sense.

Many thanks to my friends at Analog Devices — you know who you are. Special thanks to Paul Ferguson and Doug Grant for your constant support and friendship — even after "the decision." Paul, your input into the circuit and system design was invaluable. Doug, thanks for your help in obtaining the signal-generation boards.

To all my friends in the lab and at the University of Toronto in general: a huge thank-you! Chris, Karen and Ralph — our gang has dispersed in space, but not in spirit. To you, and to Angela, Bob, Brian, Bryn, Duncan, Frank, Hossein, Kapil, Khoman, and other past and present EA104 lab-mates: you were a large part of the reason I endured the long hours and hard work.

Thanks to Bryn Owen for copious help with BALLISTIC and the IC layout; to CMC & Nortel, and to ADI, for IC fabrication; and to Bob Richens for IC testing.

Thanks to NSERC, to U of T, and to the Walter Sumner Foundation for funding.

Thanks to the gangs at John's Italian Caffe and Juice For Life — two fabulous places for an "office" away from the office!

To Cindy & Scott, Mike & Amy and Marv: thanks for the soup (for the stomach and the soul)! Bob, Bryn and Steve: thanks for the adventure. Isis: you kept me smiling!

Finally, to Mom, Dad, Mike and Amy: I understand how lucky I am to have family like you. You are a constant, calm, and reassuring presence, no matter what life brings. I thank you, and hope that life will continue to smile upon you.

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CHAPTER

1 Introduction and Thesis Outline

Considerable research effort in the field of microelectronics pushes towards the realization of fully monolithic, chiefly digital, RF transceivers — with the ultimate objective being the implementation of small, inexpensive, low power communication devices that are robust, testable, and capable of handling multiple communications standards.

The goal of monolithic implementation has led to zero-IF architectures, which utilize quadrature mixing in the transceiver front end to reduce the passive RF image-reject filter requirements. Many problems limit their usefulness, however, resulting in other architectures that concentrate more on the goal of digital realization — tending towards the use of bandpass analog-to-digital conversion as soon after the antenna as possible, typically at an IF stage.

This thesis proposes a low-IF receiver architecture, which, with modern quadrature image-reject mixers and strategic IF placement, offers a viable solution for realizing digital, monolithic receivers. A critical, and heretofore non-existing, component of such a system — and indeed of any receiver that uses image-reject mixing to alleviate off-chip filtering requirements — is one that efficiently performs bandpass A/D conversion on quadrature signals. A quadrature variant of a bandpass delta-sigma ($\Delta\Sigma$) modulator is thus proposed, which offers significant theoretical and practical performance advantages over the alternative of a pair of traditional bandpass $\Delta\Sigma$ modulators.

The design of the transfer functions, systems and circuits needed to realize quadrature ΔΣ modulators are explored. Care is taken in the development of a robust prototype IC. Pertinent issues range from the study of non-ideal effects, and techniques with which to combat them, to sound IC circuit design, layout, and testing techniques.

1.1 Thesis Outline

Chapter 2 provides background information on bandpass delta-sigma modulation, complex signals and complex filters, and radio receiver spectra and architectures; all three topics are relied upon in later sections of the thesis.

Chapter 3 presents a low-IF receiver architecture that provides a viable solution for realizing single-chip radio receivers. A new quadrature bandpass ΔΣ modulator is proposed which is a tailor-made fit for the low-IF receiver — indeed, for any system that requires A/D modulation of narrow-band quadrature signals. A general quadrature ΔΣ modulator structure is shown, and a general design methodology discussed. Examples and theory are presented that contrast real and quadrature modulator performance, both for converting complex and real inputs. Under ideal conditions, the quadrature variants are shown to have significant performance advantages. Decimation and anti-aliasing techniques are discussed.

Chapter 4 examines the effects of mismatch upon quadrature ΔΣ modulator performance. A simple complex bandpass filter is first subjected to mismatch and examined in detail. These results are then applied to the more intricate case of a non-ideal fourth-order quadrature feedback system. The quadrature-modulator versus real-modulator performance comparison is again made, but this time with the influence of coefficient and amplifier non-idealities. It is seen that the quadrature modulator loses much of its performance advantage due to the severe effects of mismatch.

Chapter 5 describes an improved modulator that uses techniques revealed by the studies of Chapter 4 to dramatically minimize the effects of non-idealities. The design procedure for such a modulator is given, and the various allowable trade-offs discussed. The improved modulator is compared for SNR performance against a pair of real bandpass modulators, this time easily maintaining its distinct advantages in the face of mismatch.

Chapter 6 describes the steps undertaken to realize a silicon implementation of the improved quadrature bandpass ΔΣ modulator. First, the overall switched-capacitor architecture is presented and its operation explained. Then, constituent circuitry is discussed and simulation results are shown. Finally, a code-driven layout methodology is introduced, layout blocks are shown, and the advantages and disadvantages of the automated layout technique are outlined.

Chapter 7 describes the experimental testing of the integrated circuit. The pin connections of the IC are outlined, a circuit board is shown that houses the IC, and the test set-up is introduced and described. Experimental data is collected, analyzed, and discussed, showing the IC to be a true 10-bit analog-to-digital converter suitable for operating on complex input signals. Improvements are suggested for a next-generation version of the IC.

Chapter 8 concludes the thesis and makes suggestions for further research.

CHAPTER 2

Background Theory and State-of-the-Art

This chapter provides background information on bandpass delta-sigma modulation, complex signals and complex filters, and radio receiver spectra and architectures; all three topics are relied upon in later sections of the thesis.

Noise-shaping, or delta-sigma, modulators are well known for their ability to provide robust analog implementations of analog-to-digital converters for narrow-band input signals. Historically, the technique has been widely used for low-frequency input signals in high-fidelity audio circuitry and high-precision instrumentation devices. Within the last five years, bandpass variants have become popular for performing A/D conversion on narrow-band signals in radio receivers. Bandpass delta-sigma modulators will be discussed, and their benefits outlined.

In communication systems, it is often beneficial to think in terms of complex signals and complex systems. Complex signals are represented by pairs of real signals, and can be filtered and manipulated as are real signals. Complex filters are physically realizable using standard, real, filter sections. This section will attempt to take some of the mystery out of the world of complex signals and filters, and will introduce necessary terminology.

Lastly, architectures that are often considered for digital and monolithic radio-receiver implementations will be described, and contrasted against the traditional analog superhet receiver. The spectra that occur in the mixing processes in such receivers, and the implications of those spectra, will be discussed.

2.1 Bandpass Delta-Sigma Modulation

In a bandpass delta-sigma (ΔΣ) modulator [1]-[21], bandpass filtering and feedback around a low-resolution quantizer shape the noise spectrum, which, along with oversampling, facilitates accurate A/D conversion on narrow-band input signals. Bandpass ΔΣ modulators operate in much the same manner as lowpass ΔΣ modulators and retain many of their advantages over conventional Nyquist-rate converters. These advantages include inherent linearity, reduced anti-alias filter complexity and robust analog implementation [20].

2.1.1 Bandpass Modulator Design

A bandpass ΔΣ modulator can be constructed by connecting a filter and quantizer in a loop as shown in Fig. 2.1. The resonator may be implemented as a discrete-time filter using, for example, switched-capacitor (SC) or switched-current (SI) technology, or it may be implemented as a continuous-time filter using, for example, LC or G_mC filters. The quantizer may be single-bit or multi-bit and the loop may use multiple quantizers [20], though realizations to date are typically single-bit, single-quantizer ones.

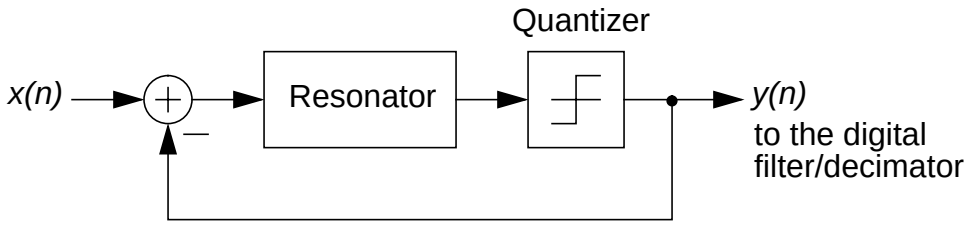

Fig. 2.1 A bandpass noise-shaping feedback loop.

Fig. 2.2 shows the simulated output spectrum of the one-bit output stream, $y(n)$, of a fourth-order bandpass ΔΣ modulator with a half-scale sinusoidal input. As this figure shows, the in-band sine-wave input is faithfully reproduced, yielding a spectral line inside a noise valley, but outside this valley large amounts of quantization noise (which have been "pushed" to out-of-band frequencies by the filtering action of the loop) would dominate any out-of-band signal components.

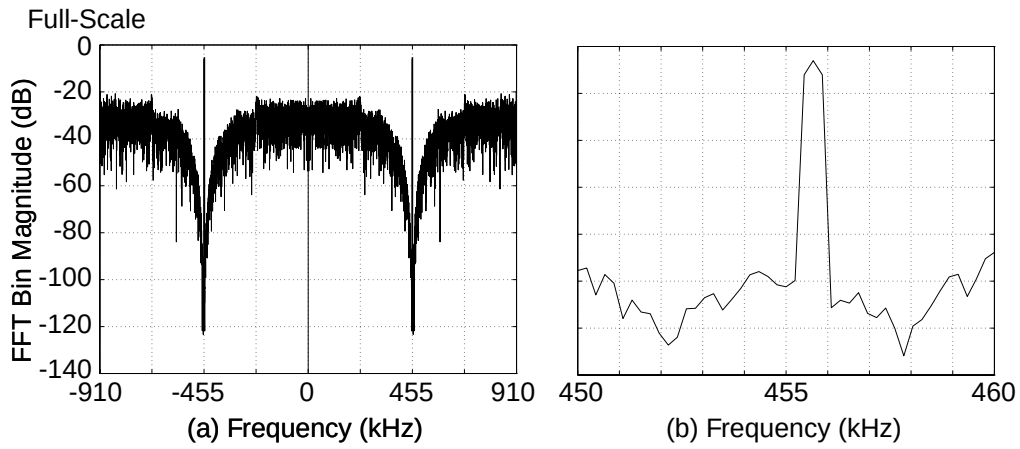

Fig. 2.2 (a) The 8k-bin output spectrum of a fourth-order modulator with a -6-dB peak input (relative to the DAC feedback levels). (b) The in-band region of the spectrum (the oversampling ratio is 91).

This particular modulator spectrum is that of the pioneer monolithic implementation of a bandpass ΔΣ modulator [4,5,6 Jantzi][1] which accounts for the relatively relaxed frequency specifications (sampling rate f_s = 1.82 MHz, center frequency f_0 = 455 kHz, and bandwidth f_b = 10 kHz). The modulator is fourth order, giving the output spectrum two in-band noise-shaping notches that are visible at approximately 452 kHz and 458 kHz in the spectrum in Fig. 2.2(b).

To make a complete bandpass ADC system, a post-filter and decimator are needed. These digital blocks remove the out-of-band quantization noise, lower the data rate and translate the signal to baseband. Thus, the structure and operation of bandpass converters are in many ways analogous to those of lowpass converters.

One major difference (and an obvious one for those familiar with filter design) is that, whereas an *N*th-order lowpass modulator achieves *N*th-degree in-band noise shaping, an *N*th-order bandpass modulator achieves only degree-$N/2$ in-band noise shaping (since its collection of noise-shaping zeros is divided between the positive and negative frequency bands). Thus, the signal-to-noise ratio (SNR) of bandpass modulators — as predicted using the linear model, which

1. In order to highlight the author's work within this research area, papers by the author are noted in the referring text as [1 Jantzi], for example.

is described below — increases at $3N$+3 dB for each octave increase in oversampling ratio,[1] half of the $6N$+3 dB/octave increase seen for lowpass modulators.

2.1.2 The Linear Model

Modeling the quantizer in Fig. 2.1 as an additive noise source, and generalizing to allow the input and feedback to use different feed-ins to the filter, yields the "linear model" shown in Fig. 2.3. The resultant system can be described by

$$Y(z) = G(z)X(z) + H(z)N(z). \tag{2.1}$$

The linear-model view of a modulator allows one to move the design of a ΔΣ noise-shaping loop into the realm of linear-filter design, which simplifies the design procedure while maintaining a reasonable prediction for the shape of the actual modulator output spectrum.

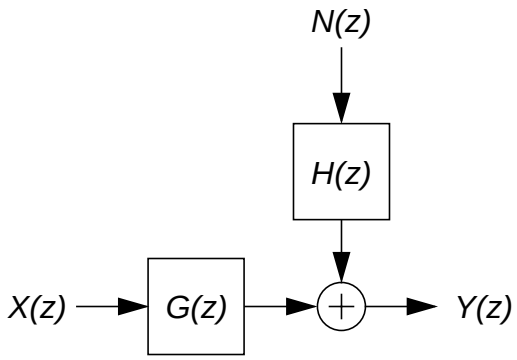

Fig. 2.3 The linear model of a delta-sigma modulator.

I. The Noise Transfer Function

The key design issue is to choose a noise transfer function (NTF), $H(z)$, that minimizes the in-band noise under two constraints: one for causality and one for stability.

The loop around the quantizer cannot be delay-free, so $H - 1$ must be strictly causal (first impulse-response coefficient zero) [20]. This constraint forces

$$\lim_{z \to \infty} H(z) = 1 \tag{2.2}$$

1. The oversampling ratio, R, is defined (as it is for lowpass converters) as one-half of the sampling rate divided by the width of the band of interest, or $R = f_s / 2f_b$. An oversampling ratio of unity signifies sampling at the Nyquist rate, $f_s = 2f_b$.

which indicates that one cannot just force H to zero everywhere. Making $|H|$ small in-band forces it above unity out-of-band.

Stability is a more difficult problem. Making the linear model stable does not guarantee that the real nonlinear system (which is difficult to analyze because of the hard nonlinearity of the quantizer) is stable. A complete theory of stability adequate for design is lacking, but in general terms, if the out-of-band noise gain gets too high overall, then the internal filter states will become very large. This leads to Lee's rule-of-thumb for one-bit quantizers [22] which claims that constraining the peak gain according to

$$|H(e^{j\omega T})| < 1.6 \tag{2.3}$$

will result in a stable modulator. The above form includes some safety margin to allow for component variation and for the approximate nature of the criterion.

The NTF magnitude response of the fourth-order modulator from Refs. [4,5,6 Jantzi] is shown in Fig. 2.4(a), and its pole-zero constellation in Fig. 2.4(b). The NTF response is a reasonable prediction of the actual spectral noise-shaping seen in Fig. 2.2.

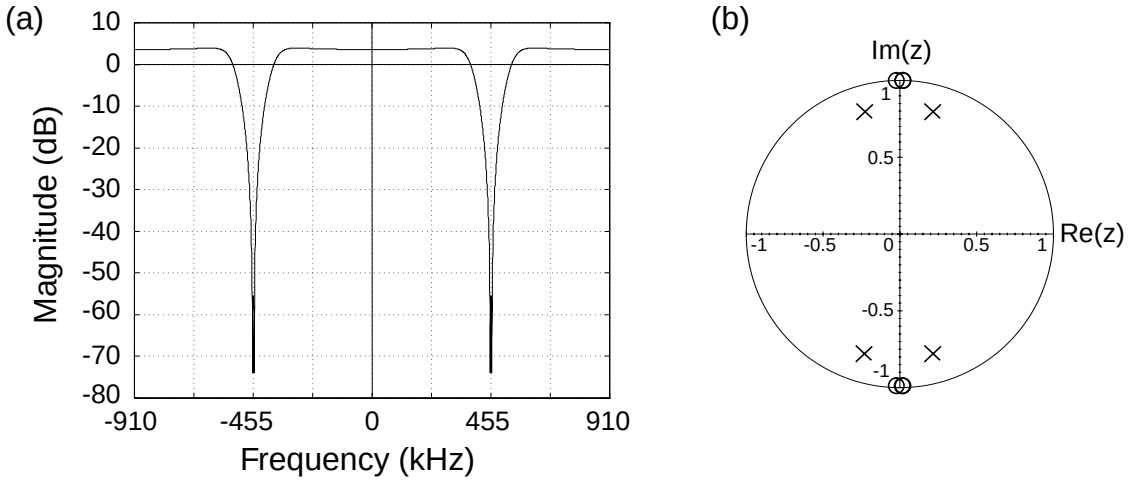

Fig. 2.4 (a) Magnitude response and (b) pole-zero constellation for the noise transfer function of the fourth-order modulator from Refs. [4,5,6 Jantzi].

II. The Signal Transfer Function

The modulator's input-output signal transfer function (STF), $G(z)$, is less critical. It is typically designed for unity gain and linear phase in-band, with little out-of-band gain peaking. More exotic functions may be designed, which, for example, reject adjacent radio channels before conversion.

The STF magnitude response of the fourth-order modulator from Refs. [4,5,6 Jantzi] is shown in Fig. 2.5(a), and its pole-zero constellation in Fig. 2.5(b). The in-band STF is flat to 0.006 dB and has phase linear to better than $0.01°$.

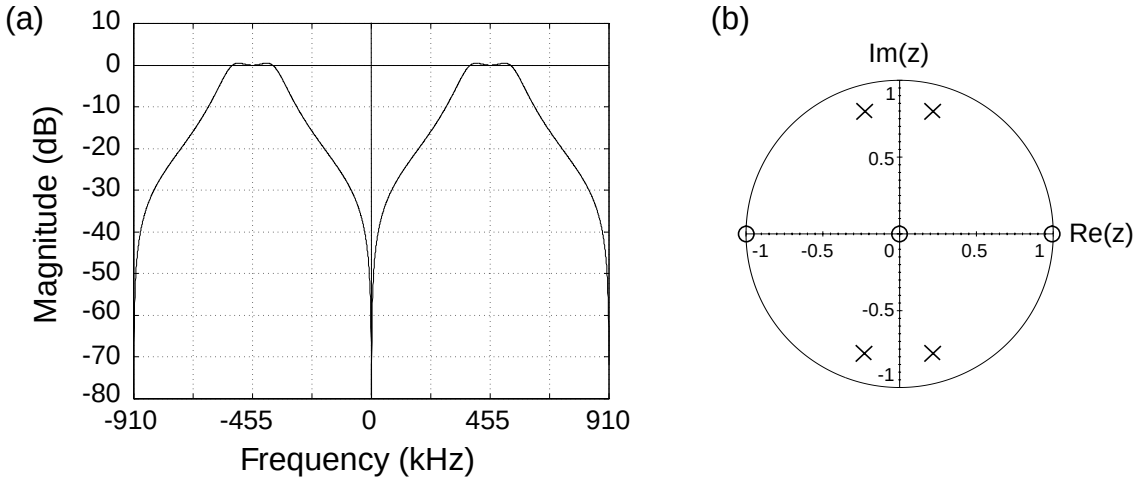

Fig. 2.5 (a) Magnitude response and (b) pole-zero constellation for the signal transfer function of the fourth-order modulator from Refs. [4,5,6 Jantzi].

2.1.3 Bandpass ΔΣ Modulator Performance

Many bandpass ΔΣ integrated circuits are published in the literature. They range from discrete-time switched-capacitor implementations, to continuous-time LC and G_mC implementations.[1] Performance specifications — such as sampling rate (f_s), input-signal center frequency (f_0) and bandwidth (f_b), signal-to-noise-plus-distortion ratio (SNDR), and dynamic range — vary as well, with overall performance generally increasing for more recent implementations. Table 2.1 summarizes the performance of the bandpass ΔΣ modulators

1. The LC versions are not monolithic, using off-chip LC-tanks as resonators.

published to date. Modulators are listed in chronological order based on the date of their initial publication.

Table 2.1: Performance Summary of Bandpass ΔΣ Modulator ICs

Type[a]	Lead Author	Year[b]	f_s [c]	f_0 [c]	f_b [c]	SNR/ SNDR	Ref.
SC	Jantzi	1992	1.82 MHz	455kHz	10 kHz	63 dB	[4][5][6]
LC	Tröster	1992	26 MHz	6.5MHz	200 kHz	55 dB	[7][8]
SC	Longo	1993	7.2 MHz	1.8MHz	30 kHz	75 dB	[9]
SC	Singor	1994	42.8 MHz	10.7MHz	200 kHz	55 dB	[10][11]
SC	Song	1995	8 MHz	2MHz	30 kHz	56 dB	[12][13]
SC	Hairapetian	1996	13 MHz	3.25MHz	200 kHz	63 dB	[14][15]
SC	Norman	1996	160 MHz	5MHz	2.5 MHz	84 dB[d]	[16][17]
SC	Ong	1997	40 MHz	20MHz	200 kHz	75 dB	[18]
G_mC	Raghavan	1997	4 GHz	0-70MHz	62.6 MHz	44 dB[e]	[19]

a. SC=switched-capacitor, LC=off-chip LC-tank resonators, G_mC=transconductance-C.

b. Year in which the IC was first published in a refereed conference or journal.

c. f_s =sampling rate, f_0 =center frequency, f_b =bandwidth.

d. The modulator achieves 65-dB sliding SNR and uses 20 dB of gain control (internal to the modulator) to give 84-dB *input* dynamic range.

e. The IC reportedly achieves 92-dB SNR in a 366-kHz bandwidth. At that bandwidth, the 4-GHz sampling rate signifies oversampling at 5465 times, an impractical level at which to obtain reasonable results. For practical bandwidths, it is likely that the modulator achieves SNR greater than the listed 44 dB.

2.2 Complex Signals and Complex Filters

Complex-valued signals are not particularly mysterious; rather, they are simply a convenient representation of a pair of real signals. Nor are complex *filters* mysterious; they do in fact have exact physical realizations and can be designed by straightforward techniques without resorting to Hilbert-transform methods and other ninety-degree phase-shift networks.

2.2.1 Complex Signals

One typically thinks of analog signals as being real, since they are represented by the voltages on, or currents through, single wires. If, however, one considers a pair of wires with different (in

this case discrete-time) signals, $f_1(n)$ and $f_2(n)$, one can think of the wire pair as carrying the complex signal, $f(n) = f_1(n) + j f_2(n)$. A more descriptive form is $f(n) = f_R(n) + j f_I(n)$, where the *R* and *I* subscripts denote the real part and the imaginary part of the fictitious complex signal.

The discrete-time Fourier transform of $f(n)$ is

$$F(e^{j\omega}) = F_R(e^{j\omega}) + jF_I(e^{j\omega}). \tag{2.4}$$

$F_R(e^{j\omega})$ is the transform of the real part of $f(n)$ and is itself a real function, i.e.

$$\left|F_R(e^{-j\omega})\right| = \left|F_R(e^{j\omega})\right| \text{ and} \tag{2.5}$$

$$\angle(F_R(e^{-j\omega})) = -\angle(F_R(e^{j\omega})). \tag{2.6}$$

$F_I(e^{j\omega})$ is the transform of the imaginary part of $f(n)$ and is again a real function, i.e.

$$\left|F_I(e^{-j\omega})\right| = \left|F_I(e^{j\omega})\right| \text{ and} \tag{2.7}$$

$$\angle(F_I(e^{-j\omega})) = -\angle(F_I(e^{j\omega})). \tag{2.8}$$

No such symmetries exist for the transform $F(e^{j\omega})$, however, and thus complex signals are not restricted, as are real signals,[1] to having magnitude spectra that are symmetric about dc.

2.2.2 The Complex Exponential

A commonly-encountered complex signal is the complex exponential, given here in its continuous-time version

$$f(t) = e^{-j\omega_c t} = \cos(\omega_c t) - j\sin(\omega_c t). \tag{2.9}$$

This signal has power only at the negative frequency $-\omega_c$, whereas each of its components has power at both $+\omega_c$ and $-\omega_c$, as mentioned above. Fig. 2.6 shows this in pictorial form.

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1. For example, the real signal $y(n)$, from Fig. 2.1, has a magnitude spectrum, shown in Fig. 2.2(a), that is symmetric about dc.

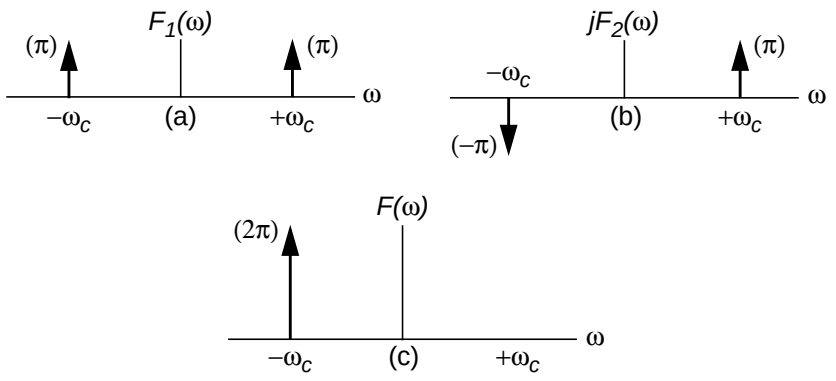

Fig. 2.6 The formation of a complex exponential. Subtracting spectrum (b) from (a) gives (c).
(a) $f_1(t) = \cos\omega_c t \leftrightarrow F_1(\omega) = \pi[\delta(\omega - \omega_c) + \delta(\omega + \omega_c)]$,
(b) $jf_2(t) = j\sin\omega_c t \leftrightarrow jF_2(\omega) = \pi[\delta(\omega - \omega_c) - \delta(\omega + \omega_c)]$, and
(c) $f(t) = e^{-j\omega_c t} = \cos\omega_c t - j\sin\omega_c t \leftrightarrow F(\omega) = 2\pi\delta(\omega + \omega_c)$.

The complex exponential signal is a useful one to examine in some detail, since it is ideally composed of two signals that have a very specific relationship — equal amplitude and 90° phase difference — and with circuit mismatch, this relationship can break down. These complex exponentials describe the quadrature local-oscillator signals used in some receiver architectures (see Section 2.3.3), and indeed are the types of signals used as inputs for the integrated circuit that is ultimately described in this thesis.

If either the equal-amplitude or 90° -phase relationship breaks down, the complex exponential signal no longer exists entirely at one negative (or one positive) frequency, though it will still be complex. In fact, with mismatch, the signal “leaks” into the conjugate frequency band, creating an “image” exponential.

The intuition behind this phenomenon is that the non-ideal exponential signal, comprising a mismatched sine and cosine signal, can actually be constructed from two complex exponentials. Take, for example, the cosine signal $f_1(t) = \cos(\omega_c t)$ and the lower-amplitude sine signal $f_2(t) = 0.8\sin(\omega_c t)$. The combined signal

$$f(t) = f_1(t) - j f_2(t) = \cos(\omega_c t) - 0.8 j \sin(\omega_c t) \qquad (2.10)$$

is clearly not a perfect single-frequency exponential at $-\omega_c$. It can, however, be written as

$$f(t) = 0.9[\cos(\omega_c t) - j\sin(\omega_c t)] + 0.1[\cos(\omega_c t) + j\sin(\omega_c t)] \tag{2.11}$$

or

$$f(t) = 0.9e^{-j\omega_c t} + 0.1e^{j\omega_c t} \tag{2.12}$$

which indeed describes a desired complex exponential at $-\omega_c$, and a smaller "leaked," or "image," exponential at $+\omega_c$. This case is shown pictorially in Fig. 2.7. The ratio between the strengths of the desired and image signals (19 dB in this example) is an important parameter in complex systems.

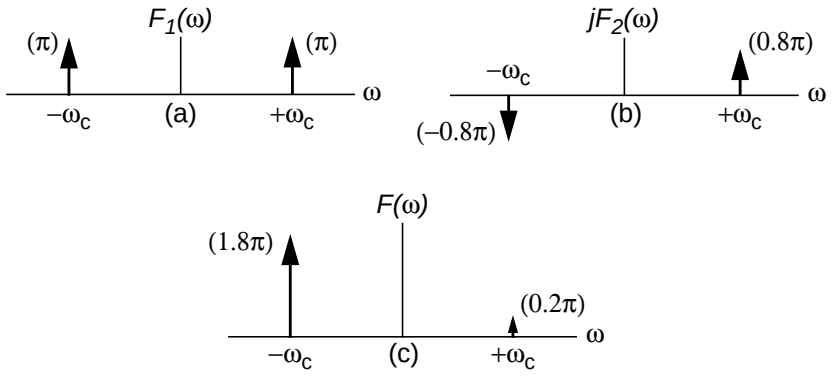

Fig. 2.7 A non-ideal complex exponential. Subtracting spectrum (b) from (a) gives (c).
(a) $f_1(t) = \cos\omega_c t \leftrightarrow F_1(\omega) = \pi[\delta(\omega - \omega_c) + \delta(\omega + \omega_c)]$,
(b) $jf_2(t) = 0.8j\sin\omega_c t \leftrightarrow jF_2(\omega) = 0.8\pi[\delta(\omega - \omega_c) - \delta(\omega + \omega_c)]$, and
(c) $f(t) = 0.9e^{-j\omega_c t} + 0.1e^{j\omega_c t} \leftrightarrow F(\omega) = 1.8\pi\delta(\omega + \omega_c) + 0.2\pi\delta(\omega - \omega_c)$.

2.2.3 Complex Filters

A filter whose transfer function has complex-valued coefficients is known as a complex filter [23][24][25]. Such a filter is thus neither limited to having complex-conjugate pairs of poles or zeros nor limited to having a symmetrical magnitude response around dc.

A discrete-time complex transfer function, $A(z)$, can always be written uniquely as

$$A(z) = A_R(z) + jA_I(z), \tag{2.13}$$

where $A_R(z)$ and $A_I(z)$ are functions with real-valued coefficients. If a discrete-time complex signal, $x(n)$, represented in the z-plane as

$$X(z) = X_R(z) + jX_I(z), \tag{2.14}$$

is applied as an input to the filter, $A(z)$, the output will be of the form

$$Y(z) = Y_R(z) + jY_I(z). \tag{2.15}$$

The usual input-output transfer-function relationship applies, so that

$$Y(z) = A(z)X(z) = [A_R(z) + jA_I(z)][X_R(z) + jX_I(z)]. \tag{2.16}$$

Clearly then,

$$Y_R(z) = A_R(z)X_R(z) - X_I(z)A_I(z) \tag{2.17}$$

and

$$Y_I(z) = A_R(z)X_I(z) + X_R(z)A_I(z), \tag{2.18}$$

as is familiar from the multiplication of two complex numbers.

These equations provide a physical description of the signal flow for a complex filter, as is pictured in Fig. 2.8. It is evident that, although a complex filter has a complex input signal and produces a complex output signal, the actual filter can be constructed from several cross-coupled real filters.

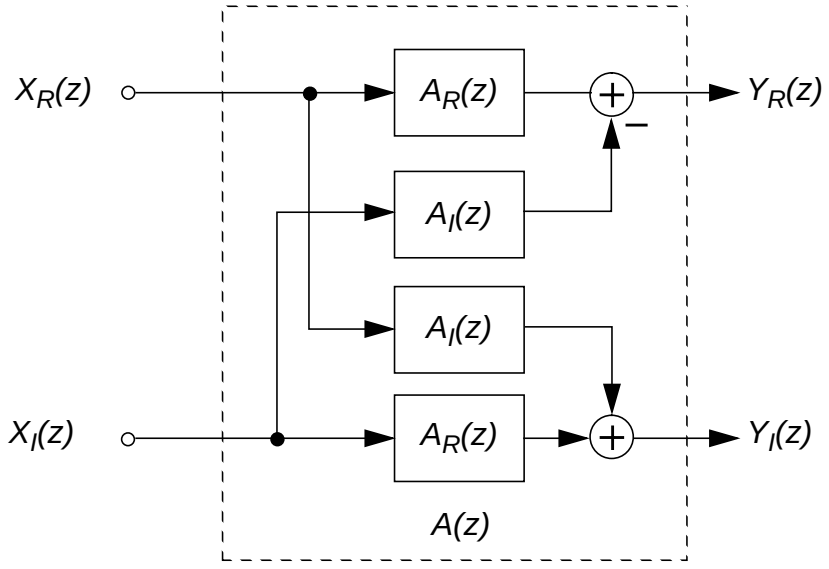

Fig. 2.8 Complex filter signal flow diagram.

2.2.4 Mismatch in Complex Filters

In Fig. 2.8, each of the blocks $A_R(z)$ and $A_I(z)$ appears twice in the complex filter structure — once to realize the real portion (the top two blocks) and once to realize the imaginary portion (the bottom two) of the output. In a circuit implementation, the two instances of $A_R(z)$ may not be identical, and the same is true for the two instances of $A_I(z)$. Fig. 2.9 shows the complex filter constructed with the non-identical filter pairs $A_{R1}(z) \neq A_{R2}(z)$ and $A_{I1}(z) \neq A_{I2}(z)$.

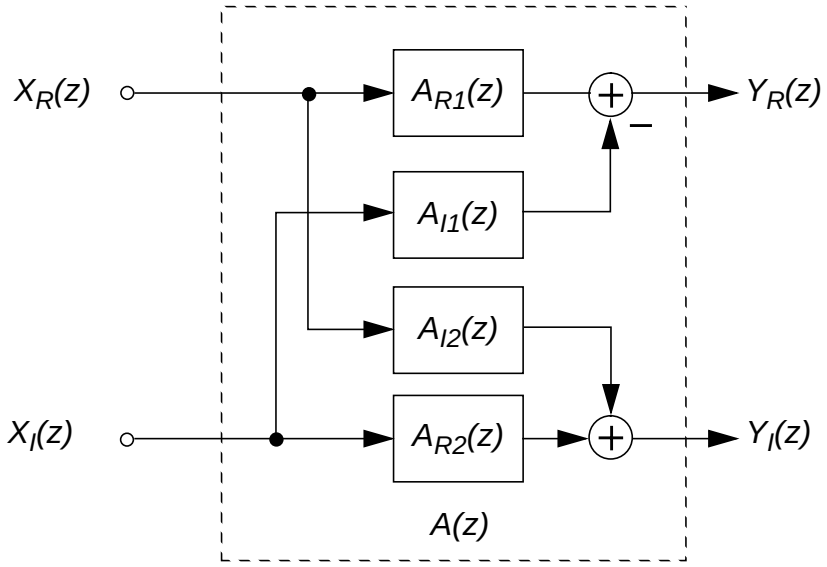

Fig. 2.9 Complex filter constructed from non-identical filter pairs $A_{R1}(z) \neq A_{R2}(z)$ and $A_{I1}(z) \neq A_{I2}(z)$.

It has been shown that the output of a mismatched complex filter can be written as the sum of a nominal term, a common-mode error term, and a differential-error term, as shown in Fig. 2.10 (in which double lines represent complex signal paths) [24].

The output of the filter, then, is written as

$$Y(z) = A_{nom}(z)X(z) + \Delta A_{cm}X(z) + \Delta A_{diff}X^*(z), \tag{2.19}$$

where the asterisk indicates the complex conjugate of a function, and the error transfer functions are defined as

$$\Delta A_{cm}(z) = \left\{\frac{A_{R1}(z) + A_{R2}(z)}{2} - A_{Rnom}(z)\right\} + j\left\{\frac{A_{I1}(z) + A_{I2}(z)}{2} - A_{Inom}(z)\right\} \quad (2.20)$$

and

$$\Delta A_{diff}(z) = \left\{\frac{A_{R1}(z) - A_{R2}(z)}{2}\right\} + j\left\{\frac{A_{I1}(z) - A_{I2}(z)}{2}\right\}. \quad (2.21)$$

From Eq. (2.19) and Fig. 2.10, it is clear that common-mode error simply perturbs the response of the filter from its ideal response, as is the case in a real filter. Differential error, on the other hand, adds an error term that is proportional to the conjugate of the input function.[1]

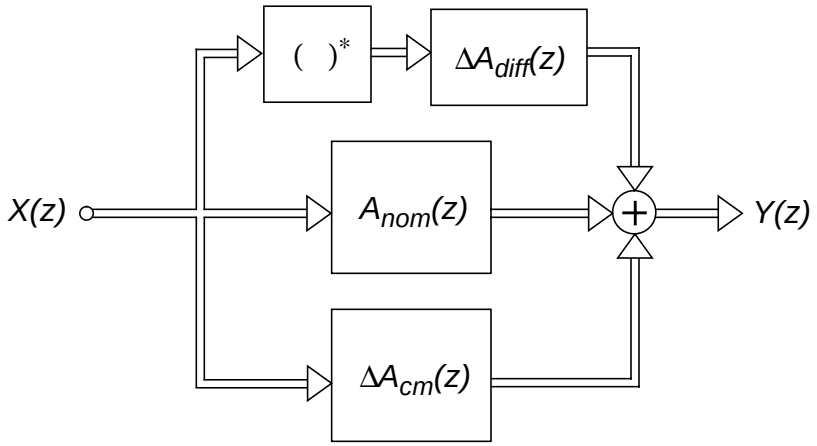

Fig. 2.10 Signal flow diagram of a complex filter, $A(z)$, showing common-mode and differential error components.

2.2.5 Image Rejection

The effects of differential error, as described by Eqs. (2.19) and (2.21), give rise to the concept of *image rejection* in complex systems. Consider two inputs into a complex bandpass filter that has a passband centered at $+\omega_x$ — a desired input at around $+\omega_x$ in the passband and another

1. This differential-error term makes the mismatched complex filter non-linear, since an input at a single frequency produces an output at two frequencies.

non-desired input (perhaps from an adjacent radio channel in a communication system) around $-\omega_x$ in the conjugate band (which is in the stopband of the complex bandpass filter).

The differential error creates a transfer function that causes some of the conjugate-band, or image-band, input to leak into the passband at the output. This interferes with the desired signal at the output. The extent to which the filter passes the desired signal relative to the image signal is called image rejection. So, if passband signals transfer to the output with 0-dB gain, and image signals do so with -60-dB gain, the filter has 60 dB of image rejection.

The opposite effect is also true, so some of the in-band signal will leak into the stopband at the output. This is usually less of an issue, but it does lessen the stopband-attenuation specification of the complex filter.

2.3 Digital and Monolithic Receiver Architectures

In order to reduce the size, power consumption and cost of hand-held radio devices, RF transceiver design continues to push towards increased levels of integration. Moving the analog-digital interface closer to the antenna is also desirable. Early conversion to digital at either the IF or RF stage results in a more robust system with improved IF-strip testability and provides opportunities for dealing with the multitude of standards present in commercial broadcasting and telecommunications.

2.3.1 Bandpass ΔΣ Modulation for IF Digitization

Architectures similar to that shown in Fig. 2.11 have recently become popular, using bandpass ΔΣ modulation to perform accurate, narrow-band, A/D conversion at the IF [15][26]. Compared with a pure analog receiver implementation, the signal processing and narrowband channel-selectivity filtering are moved into the digital domain where testing is systematic and changing filter coefficients is easy. Elimination of analog IF filters is also a key advantage when dealing with digital modulation schemes like those emerging for cellular telephones, because analog IF filters generally have poor (and poorly controlled) phase performance and hence induce intersymbol interference, whereas digital filters can have exactly linear, and well controlled, phase.

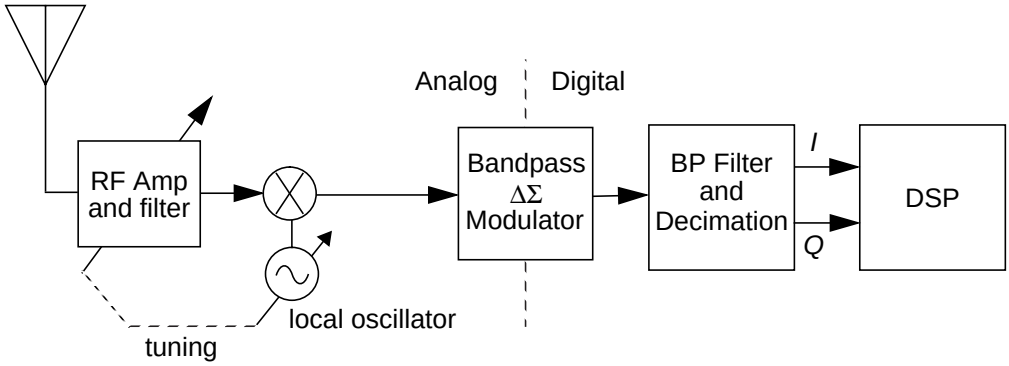

Fig. 2.11 IF digitization using a bandpass ΔΣ ADC.

A further advantage of using a ΔΣ converter, as opposed to a flash converter for example, is that the converter behaves much more like an analog circuit, having intermodulation-product levels that fall for reduced input levels[1] (for example, the 3rd-order IM products fall at a 3-dB-per-1-dB rate) [5 Jantzi][21]. Their behaviour in radio systems is therefore relatively easy to predict, while video converters can produce undesirable spurious effects.

Finally, in this architecture the in-phase/quadrature (*I/Q*) decomposition is performed in the digital world with arbitrary precision and perfect *I/Q*-channel matching [27].

2.3.2 Single-Path Mixing

This single-path architecture is not amenable to monolithic (single-chip) implementation, however, since it requires a high-*Q* front-end image-reject filter,[2] which is not easily integrated [15][28][29]. Fig. 2.12(a) shows the frequency spectra at the mixer inputs, where the shaded triangular and rectangular shapes represent the desired and image spectra, respectively, at the antenna, and the two impulse functions represent the local oscillator (LO) spectrum, which is that of a cosine.

Whereas trigonometric operations describe the mixing operation in the time domain, frequency-shifting operations do so in the frequency domain. The multiplication-in-time between

1. In typical Nyquist-rate converters, distortion products tend to remain at a fixed level regardless of signal strength.
2. In this context, *Q* refers to filter quality factor; in the majority of the thesis it signifies "quadrature."

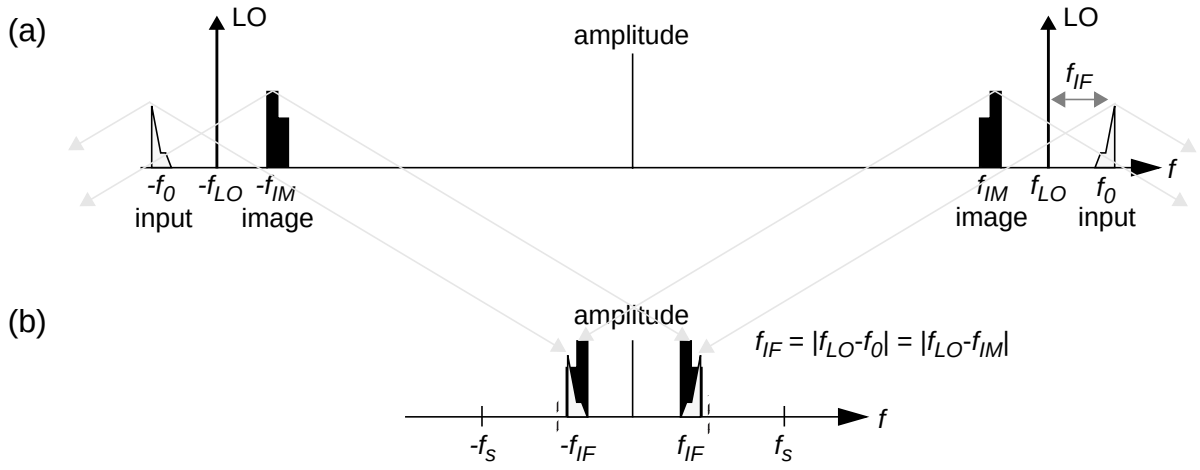

Fig. 2.12 Downconversion in a single-path IF receiver. (a) Mixer input spectra. (b) Mixer output spectrum.

the LO and antenna signals is equivalent to a convolution-in-frequency of their spectra. Thus, the impulse function at $-f_{LO}$ shifts the antenna spectrum left by f_{LO}; that at $+f_{LO}$ shifts the antenna spectrum right by f_{LO} (note the grey arrows). Fig. 2.12(b) shows the resulting mixing products at low frequencies.[1] The frequency labelled f_s signifies a possible sampling rate for A/D conversion of the mixer outputs.

Clearly there is a range of image frequencies which mix down into the same IF band as do the desired signals, thereby corrupting wanted information. The need for the high-*Q* front-end bandpass filter is obvious, since these image frequencies must be eliminated prior to the mixing operation and since the desired band and image band are separated by only twice the IF frequency. To meet the requirements, external high-*Q* passive filters are typically required, consuming power for the purpose of taking signals on and off the chip.

2.3.3 Image-Reject Mixing

An LO which has a pair of phase-quadrature outputs will mix with an RF input — in what is known as a quadrature-IF mixer [30] — such that the RF spectrum is shifted in only one direction. Image frequencies, then, will not (in the ideal case) fall into the same IF band as the desired signal, which alleviates the requirements on the front-end filter.

1. The high-frequency components are removed by a post-filter, and thus are not shown.

2.3.4 Monolithic Receivers Utilizing Direct-Conversion

Fig. 2.13 shows this *complex-exponential* mixing, where the single impulse function frequency-shifts the antenna spectrum to the left by f_{LO}. In the case shown, the chosen LO frequency is equal to the RF, so that the signal band is mixed directly to baseband. The quadrature-mixer output is now, obviously, a complex signal.

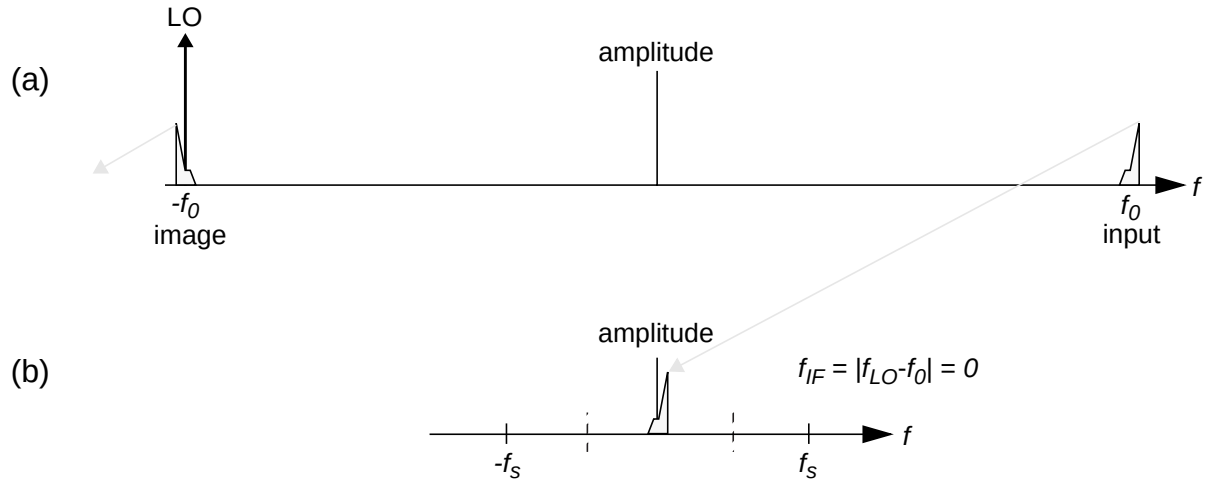

Fig. 2.13 Downconversion in a direct-conversion receiver. (a) Mixer input spectra. (b) Mixer output spectrum.

The direct-conversion architecture (Fig. 2.14) uses this combination of image-reject mixing and a zero IF. The receiver ideally has no image response, and thus the narrowband, off-chip, image-rejection filter in the RF stage can be replaced with a broadband integrated filter. This facilitates single-chip implementations of digital radio receivers [28][29][31].

Mixing the desired input spectrum directly to dc simplifies the signal processing, but poses considerable problems [28]-[35]. DC offsets at the outputs of the two mixers can be much greater in magnitude than the desired baseband signal. AC coupling can be used, but this places a notch in the effective receiver passband which can adversely affect some modulation schemes. The zero-IF approach means that $1/f$ noise is a serious concern in the back-end blocks; that the local oscillator radiates energy at the carrier frequency, which causes interference; and that even-order distortion is a concern. These problems have limited this architecture to use within a restricted set of applications [28][29][31].

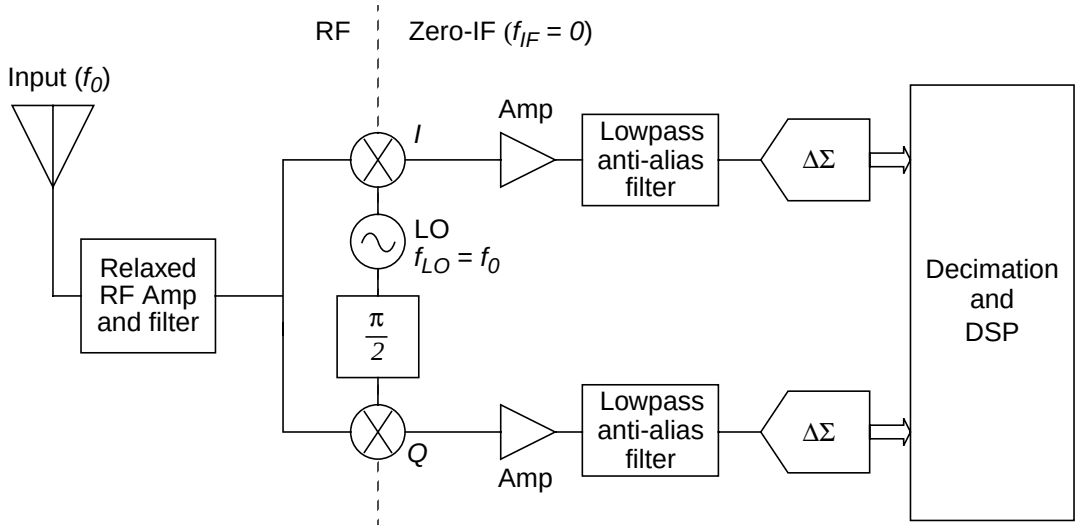

Fig. 2.14 Direct-conversion architecture.

2.3.5 Errors in Image-Rejection Mixers

Under ideal conditions (matched lines, identical mixers, etc.) the quadrature-IF mixer of Section 2.3.3 converts incoming RF signals into two IF outputs that are equal in amplitude but separated in phase by 90^o (i.e. *I* and *Q* signals). Given the discussions on mismatch in Sections 2.2.2 and 2.2.4, it is not surprising that errors in the quadrature mixer will create image problems. As a result, some unwanted signals will mix down to fall upon desired signals.

A closed-form expression describes the image rejection, IMR, that can be expected with various degrees of amplitude and phase imbalance between the two paths of a quadrature system [30].

$$IMR = 10\log 10\left[\frac{1+\frac{2k}{1+k^2}\cos\phi}{1-\frac{2k}{1+k^2}\cos\phi}\right] \tag{2.22}$$

where $k = \left|\frac{f_1}{f_2}\right|$ is the amplitude difference, and ϕ is the phase error from $90°$.

Fig. 2.15 presents this graphically, and is a useful reference when dealing with physically-implemented complex systems. The point marked as X in the figure is the case of the non-ideal complex exponential from Section 2.2.2, which had approximately 1.9 dB amplitude mismatch ($20\log 10|1/0.8|$) and $0°$ deviation from phase quadrature. The plotted value of 19 dB, calculated from Eq. (2.22), matches the "IMR" of 19 dB calculated in Section 2.2.2.

Quadrature oscillators from the literature use varied techniques to ensure close amplitude and phase matching between their *I* and *Q* outputs. One design uses a double-biquad loop and achieves phase accuracy better than $2.4°$ [36]. Other types of designs use a local oscillator and passive phase-shifters to realize quadrature outputs. One achieves better than $1.1°$ phase accuracy, and more than 40-dB IMR at 1.9 GHz [37]. Advances on the second method tune the phase-shift networks to improve performance [38][39], in one case achieving 60-dB IMR [40].

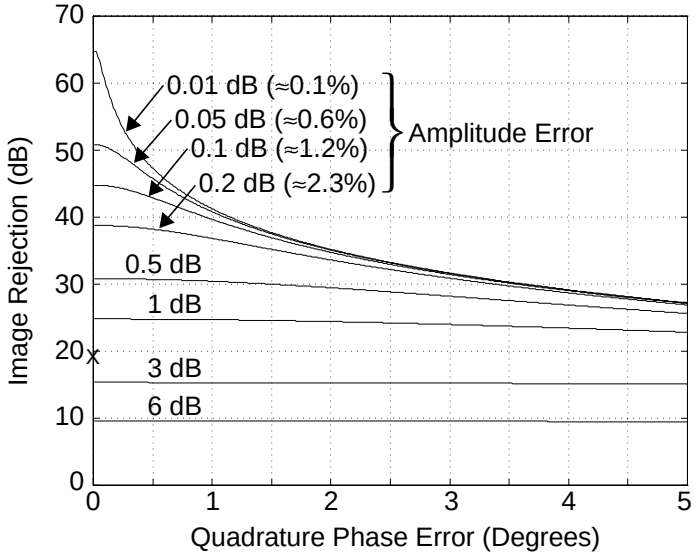

Fig. 2.15 Effects of phase and amplitude errors upon image rejection.

2.4 Summary

Bandpass ΔΣ modulation was discussed, and was shown to perform accurate A/D conversion on narrow-band input signals. Some design criteria for, and performance advantages of, bandpass modulators were highlighted.

Complex signals were introduced, and described as signals that are used to represent certain pairs of real signals. Complex filters were also described, and shown to have straightforward physical implementations.

Radio receivers that use bandpass ΔΣ modulation to convert to digital at an IF stage were shown to have many advantages over traditional analog superhet receivers. Since these receivers do not meet the necessary criteria for monolithic digital receivers, two-path direct-conversion systems were introduced. Although their use of image-reject mixers helps in achieving single-chip designs, direct-conversion receivers were shown to have many performance-inhibiting (and thus usefulness-limiting) problems.

Throughout the chapter, mismatch in complex signals and systems was shown to give rise to image signals, and thus make image rejection an important specification. Mismatch between any of the real and imaginary portions of a complex signal, the various sections of a complex filter, or the *I* and *Q* paths of a two-path receiver — each a type of real-versus-imaginary path mismatch — creates images. A relationship between path mismatch and image rejection was given. Some quadrature oscillators from the literature were discussed, one achieving nearly 60-dB image rejection.

CHAPTER 3

A Quadrature Bandpass ΔΣ Modulator

This chapter presents a low-IF receiver architecture which alleviates the problems with the direct-conversion architecture that was discussed in Chapter 2. With modern quadrature mixers, and strategic image placement, the low-IF architecture provides a viable solution for realizing single-chip radio receivers. The receiver seemingly requires a total ΔΣ modulator order twice that needed in the zero-IF version, which is wasteful from an IC area and power-consumption point of view, and also proves to be wasteful from a noise-shaping point of view.

A new quadrature bandpass ΔΣ modulator is proposed that is tailor-made for the low-IF receiver since it eliminates the aforementioned waste. It is a structure formed when the concepts of delta-sigma modulation and complex filtering are wed. A general quadrature ΔΣ modulator structure is shown and a general design methodology discussed; both are used to design a sample modulator for the GSM 200-kHz bandwidth specification. Performance aspects of the modulator are presented.

Examples and theory are presented that contrast real and quadrature modulators for converting complex and real inputs alike. The quadrature variants are seen to have significant performance advantages, in terms of total order (and thus area and power), SNR, or bandwidth — or some combination of the three.

Decimation and anti-aliasing techniques for quadrature ΔΣ modulators are discussed. Complex anti-aliasing filters are shown to be the preferred choice over a pair of real filters.

3.1 A Low-IF Receiver Architecture

The (zero-IF) direct-conversion receiver, described in Section 2.3.4 and shown in Fig. 2.14, was said to be problem plagued. If its LO is offset from the carrier frequency by a small amount, however, many problems of the architecture are alleviated [41 Jantzi][42]. The new "low-IF" architecture,[1] shown in Fig. 3.1, has spectra like those pictured in Fig. 3.2.

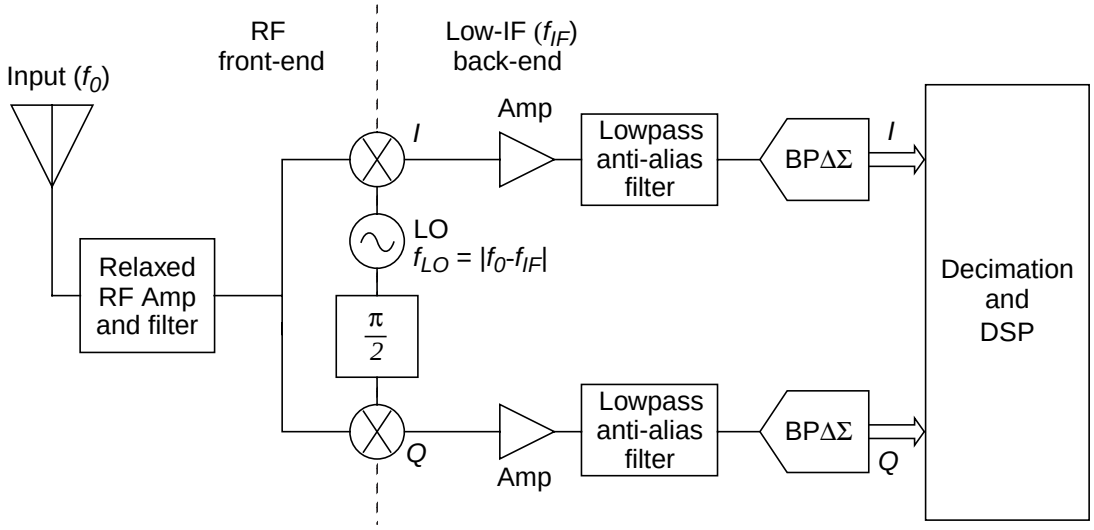

Fig. 3.1 Low-IF receiver architecture.

The architecture retains its image-rejection properties, and the fact that the desired input is mixed to a non-zero IF means that $1/f$ noise and dc offsets cause no problem, self-interference is not an issue (because the oscillator frequency is offset from the carrier frequency), and even-order distortion has less effect.

---

1. In this structure, the final mix to baseband is performed in the digital world. This is in contrast to the wide-band IF double-conversion technique [43][44] — which is also proposed as an alternative to direct conversion — in which the final conversion to baseband is performed in the analog domain by a four-multiplier/two-adder complex mixer. The wide-band IF double-conversion technique alleviates some of the problems of the direct-conversion architecture, since no oscillator operates at the RF input frequency, and it furthermore greatly alleviates the synthesizer problem, since the first LO is fixed. It, however, increases the third-order intermodulation distortion and consumes extra power due to its extra mixers, and retains many of the dc offset and drift problems of direct-conversion receivers.

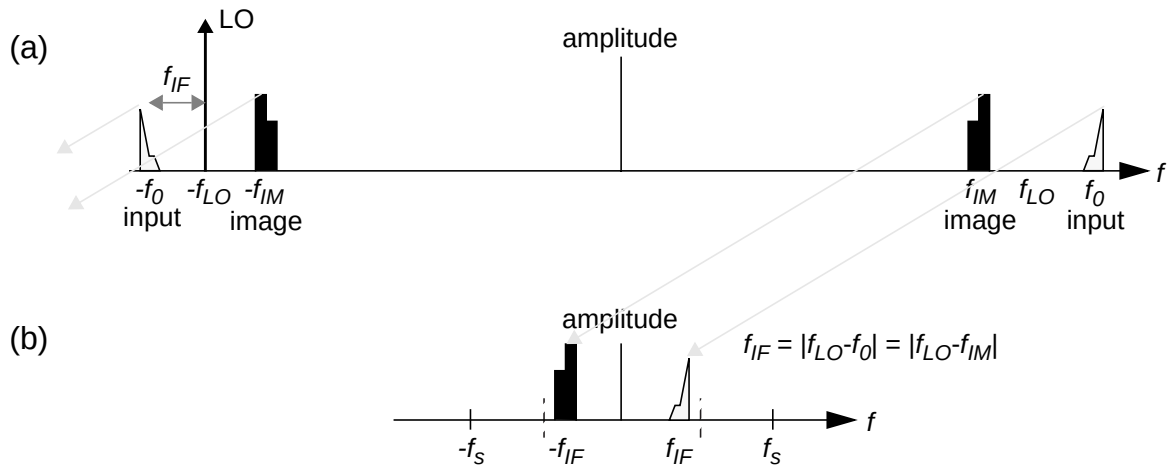

Fig. 3.2 Downconversion in the low-IF receiver. (a) Mixer input spectra. (b) Mixer output spectrum.

The downside is that the *I* and *Q* mixer outputs are narrow-band signals at the low IF, instead of near dc, so a pair of bandpass ΔΣ modulators must replace the lowpass converters in the zero-IF receiver. Thus, the total modulator order doubles,[1] since two lowpass modulators become two bandpass modulators, and double order means double area, power, etc.

3.1.1 The Low-IF Receiver with Imperfect *I/Q* Orthogonality

In the zero-IF topology, the image signal is equal to the desired signal (see Fig. 2.13), meaning that a relatively small image rejection (≈25 dB) will suffice for many applications [42]. This level of performance is easily achievable using standard quadrature mixers.

In the low-IF topology, in contrast, the image signal is not related to the desired signal (note the dissimilar rectangular and triangular spectra above), and can in fact be 20 dB, or more, larger [42][44]. In a non-ideal front-end, the quadrature oscillator signal leaks to positive frequencies (as demonstrated in Fig. 2.7), and mixes some of the image input (the rectangular spectrum) into the signal band. This produces the receiver spectra shown in Fig. 3.3. In order to minimize this image interference, the front-end image-rejection requirements for low-IF receivers are typically in the

1. Remember, to achieve the same degree of in-band noise shaping, a bandpass modulator requires twice the order of a lowpass modulator. A fourth-order bandpass modulator, for example, has basically the same second-order in-band noise shaping as a second-order lowpass modulator.

60 to 80-dB range [44], slightly higher than achievable with image-reject mixing alone (as was discussed in Section 2.3.5).[1]

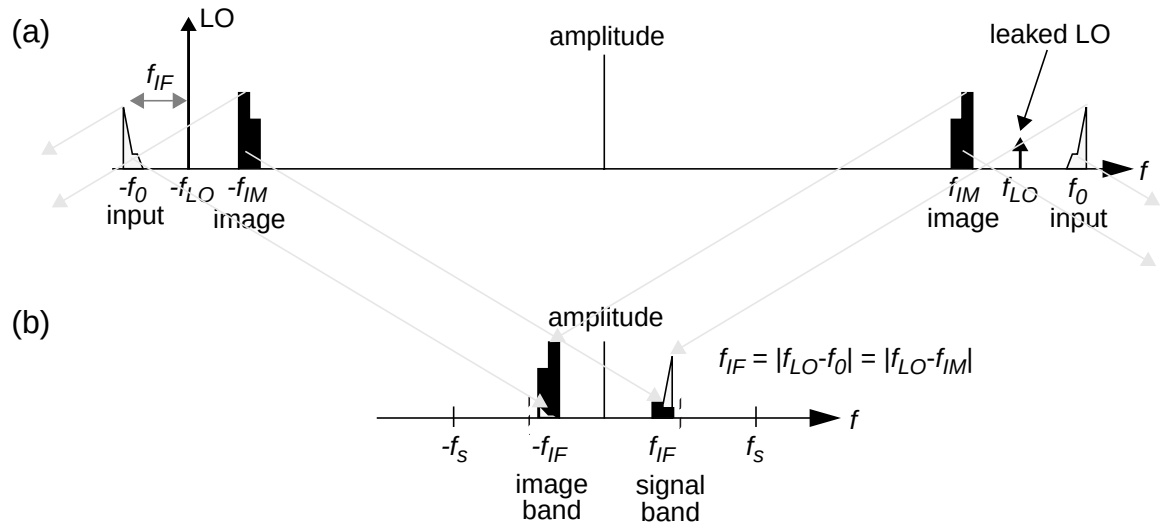

Fig. 3.3 Downconversion in the low-IF receiver with a non-ideal oscillator. (a) Mixer input spectra. (b) Mixer output spectrum.

One way to alleviate concerns over image interference, is to strategically locate the receiver's images. In GSM specifications, for example, there are guaranteed "holes" in the receive spectrum for two 200-kHz adjacent channels [44][45]. Choosing an IF such that images lie in this hole greatly reduces image concerns [44], and means that image-reject mixing alone may meet specifications.

If necessary, the IF can be chosen high enough that a relaxed (and thus integratable) front-end filter [46] may provide a modicum of image rejection, taking a share of the system's image-rejection specification by helping to reduce the amplitude of the image spectrum before it mixes down.[2]

---

1. Note, too, that the large image signal is mixed down to where it appears as an image input for the back-end blocks. Thus, the back end must also maintain high image-rejection performance.
2. If extreme system specifications call for traditional high-IF, or multiple-IF, techniques — thus precluding fully-monolithic implementation — image-reject mixing remains highly beneficial, which maintains the need for a two-path back end.

3.1.2 Receiver Operation Using Twin Bandpass ΔΣ Modulators

To observe the ideal receiver operation for a simple case, imagine an input to the antenna which is a single sinusoid of frequency $f_0 + \Delta f$ (as opposed to an input with actual bandwidth, as represented by the triangle in Fig. 3.2). The LO mixes the sinusoid down[1] to a cosine at $f_{IF} + \Delta f$ in the *I* channel, and a sine at $f_{IF} + \Delta f$ in the *Q* channel. These signals are converted to digital by a pair of bandpass ΔΣ modulators, each of which produces a bit-stream output that accurately represents its input tone within a narrow band.

The bandpass ΔΣ modulator output spectra for this case are shown in Fig. 3.4(a), where the modulators are the fourth-order ones from Chapter 2, for familiarity. Input sinusoids with peak amplitude of one-half the modulator peak feedback level are used (i.e. half-scale, or -6-dB, inputs). The *I*-channel and *Q*-channel modulator spectra are almost identical to one another,[2] except for some minor differences in the noise spectra which are revealed by using a different shade for each channel in the plot overlay. Fig. 3.4(b) shows a zoom into the spectrum in the negative-frequency (conjugate) band, and Fig. 3.4(c) shows the in-band zoom. There is nothing surprising about these spectra: each is the output of a real bandpass ΔΣ modulator that has a sinusoidal input at just above band center.

The more interesting spectrum occurs when we combine the two digital bit-stream outputs as *I*+j*Q*. This produces the complex spectrum shown in Fig. 3.5(a). Clearly, this spectrum represents a complex tone accurately in the region around +455 kHz. The zoom into the negative frequency band (Fig. 3.5(b)) shows no signal content, whereas the signal-band zoom (Fig. 3.5(c)) shows the expected tone (which is 6-dB stronger than was either constituent tone).

So, this arrangement does perform an A/D modulation on the complex IF input, and it does so with all the advantages of using bandpass ΔΣ technology. What is apparent though, is that there is noise-shaping that pushes noise away from the negative frequency bands, when we have no signals present therein.[3] Intuitively this seems wasteful.

---

1. The high-frequency components are removed by the anti-alias filters, and will be ignored.
2. Their phases differ, of course, since one spectrum represents a cosine in-band while the other represents a sine.
3. The noise-shaped band at negative frequencies could, of course, be utilized in some systems.

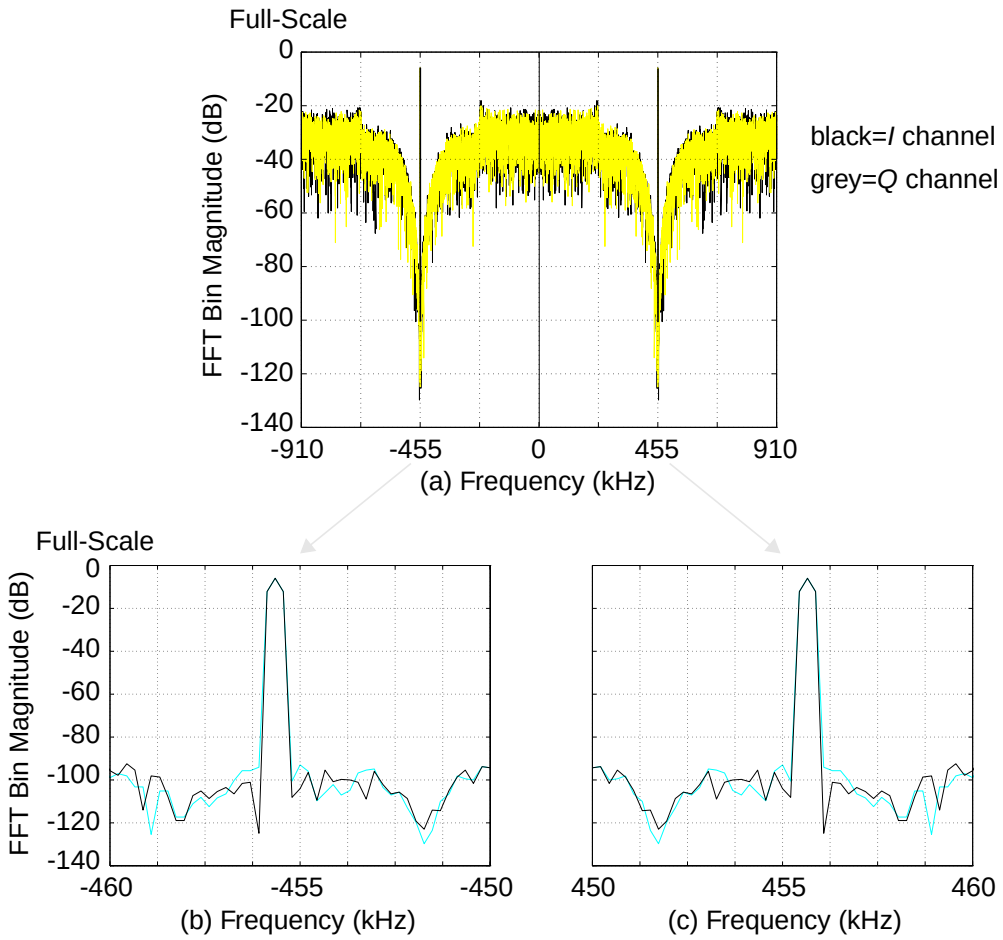

Fig. 3.4 Superimposition of the output spectra of the two bandpass ΔΣ modulators from Fig. 3.1. (a) Full magnitude spectra showing that each modulator output is real, and represents a tone accurately within a narrow band. (b) Zoom into the image-band (conjugate-band) region. (c) Zoom into the in-band region.

In fact, it is wasteful from a noise-shaping standpoint. It can be shown that the average logarithm of the NTF magnitude characteristic must be zero or positive [47], or that

$$\int_0^1 \log\left|H(e^{j\pi f})\right| df \geq 0\,. \tag{3.23}$$

The consequence of this is that pushing noise away from one band increases it in other bands, which impinges upon the stability of the modulator, or means that wasteful noise-shaping comes at the expense of desired noise shaping.

Based on our knowledge of complex filtering functions, one is led to wonder if the noise shaping itself could be complex. In the example above, the two noise-shaping zeros in the

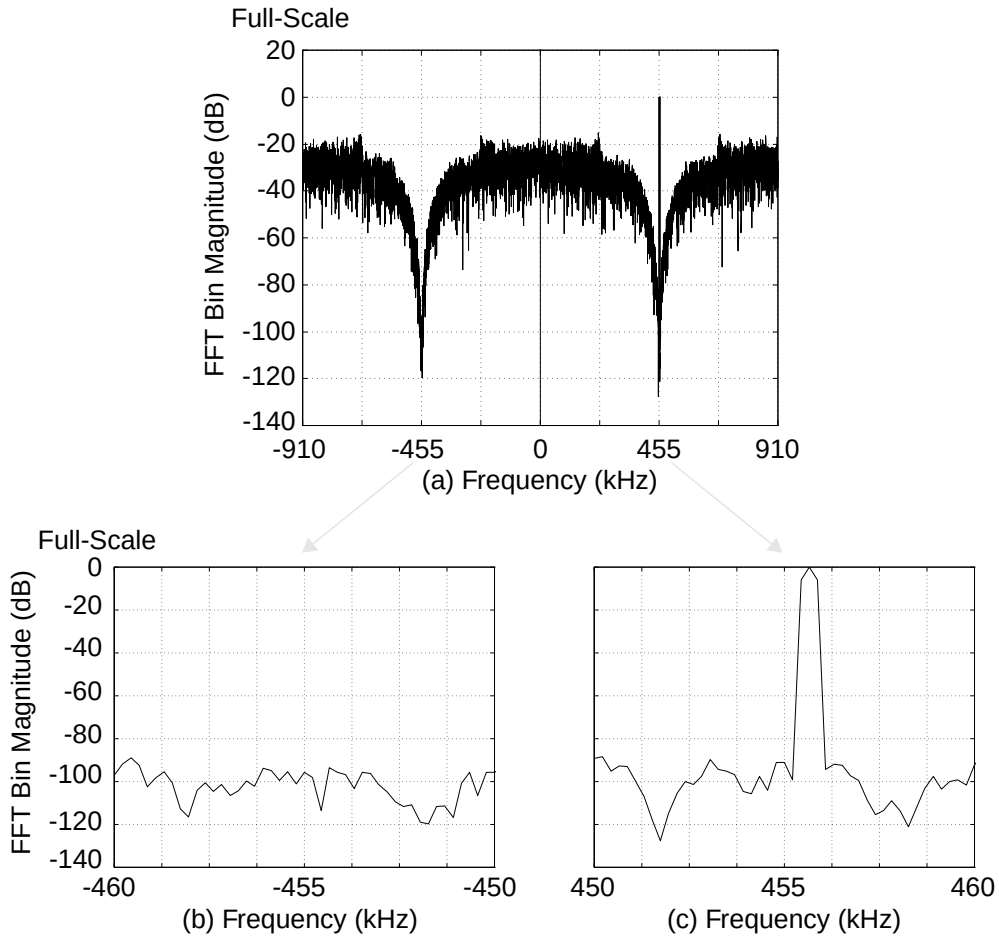

Fig. 3.5 The output spectrum of the two bandpass ΔΣ modulators from Fig. 3.1 combined as I+jQ. (a) Asymmetric magnitude spectra showing that the combined output is complex and represents a complex tone accurately within a narrow band around +455 kHz. (b) Zoom into the image-band (conjugate-band) region. (c) Zoom into the in-band region.

negative frequencies could be removed all together, which could potentially halve the total modulator order while at the same time helping the NTF according to Eq. (3.23), or they could be moved up to positive frequencies to give higher SNR performance and/or bandwidth.

3.2 Quadrature Bandpass ΔΣ Modulation

In Ref. [41 Jantzi], the structure of Fig. 3.6 was proposed, where a single quadrature bandpass ΔΣ modulator performs A/D conversion on the I and Q mixer outputs in concert, truly treating them as the complex analog signal, I+jQ. The structure is identical to that in Fig. 3.1, but the two real bandpass ΔΣ modulators have been replaced with a single, quadrature, one. The separate anti-alias filters have also been replaced by one complex anti-aliasing filter.

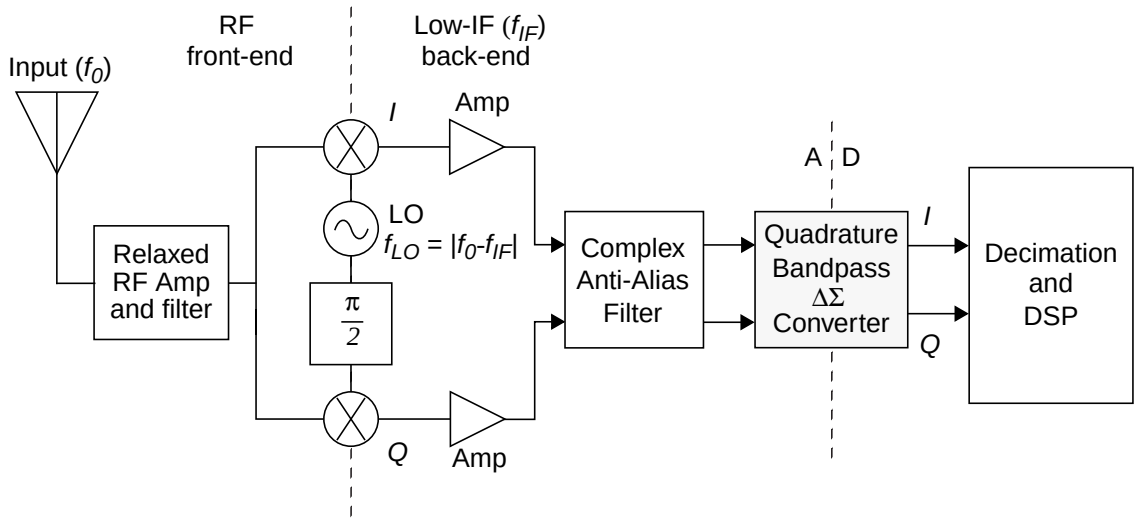

Fig. 3.6 A low-IF system utilizing a quadrature bandpass ΔΣ modulator.

3.2.1 A Complex Noise-Shaping Loop

The traditional bandpass ΔΣ modulator of Fig. 2.1 is extended to the quadrature, or complex, case if a complex filter is placed in the ΔΣ loop, as in Fig. 3.7 [41 Jantzi][48][49][50]. The structure shown is symbolic, in the sense that an actual modulator would likely feed both the input and output signals to various points within the loop filter.

A quadrature ΔΣ modulator can be thought of as performing a complex A/D conversion on its complex analog input $x(n) = x_R(n) + jx_I(n)$. The modulator generates two high-speed bit-streams that represent the I and Q channels. When combined as $I+jQ$ in the digital domain, these

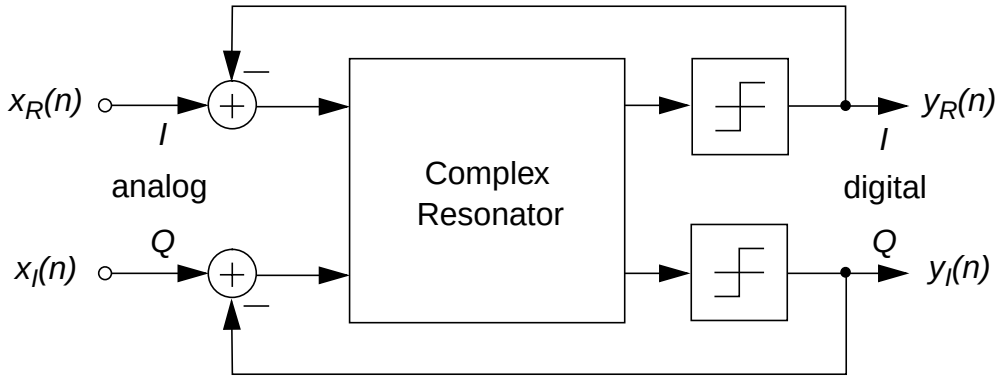

Fig. 3.7 A quadrature ΔΣ modulator structure.

bit-streams form a complex digital signal that accurately represents the complex input within a narrow frequency band. The spectrum of the output, being complex, may be asymmetric about dc.

3.2.2 Realizing Complex Poles

The loop filter in Fig. 3.7 is a complex SC filter, although it could be replaced with an appropriate complex continuous-time filter. The composition of this filter can be deduced from loop filters in traditional ΔΣ modulators: in a real lowpass ΔΣ modulator, the loop filter comprises integrators in order to shape noise away from dc; in a real bandpass ΔΣ modulator, the integrators are replaced by resonators in order to shape noise away from a band of positive and negative frequencies. It is understandable, then, that a quadrature ΔΣ modulator will have a loop filter comprising complex integrators, in order to shape noise away from complex frequency bands.

The requisite complex integrators are simple complex filters that each form a complex pole on the unit circle. With feedback applied around the quantizer, these poles form the noise-shaping zeros responsible for nulling in-band quantization noise.

I. A Brute-Force Complex-Pole Realization

A complex filter with a single pole at real-axis coordinate $(1+d)$ and imaginary-axis coordinate c has the transfer function

$$\frac{Y(z)}{X(z)} = \frac{1}{z-1-d-jc}, \tag{3.24}$$

or, when placed in rectangular form,

$$\frac{Y(z)}{X(z)} = \frac{z-1-d+jc}{(z-1-d)^2+c^2}. \tag{3.25}$$

We know from Chapter 2 that this can be constructed as shown in Fig. 3.8. This rectangular-form realization is not very efficient, however, using (at best) two second-order sections to create the single complex pole. This would then require, for example, sixteen orders worth of filtering to create four complex poles for the loop filter of a modulator with four in-band noise-shaping zeros.

II. An Elegant Complex-Pole Realization

It was realized in Ref. [51] that a far more efficient realization is possible since Eq. (3.24) describes the simple feedback network of Fig. 3.9(a), in which double lines represent complex

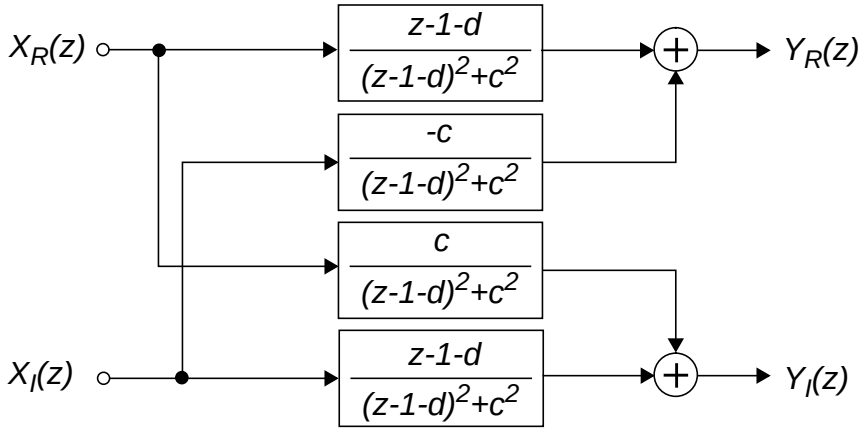

Fig. 3.8 Realizing a single complex pole by using a "rectangular form" representation.

signals. This network can be constructed using real blocks in the two-channel system shown in Fig. 3.9(b). One of the cross-coupling coefficients, c, is negative since the imaginary term of the coefficient is being multiplied by the imaginary-channel output — and $j \times j$ is equal to -1.

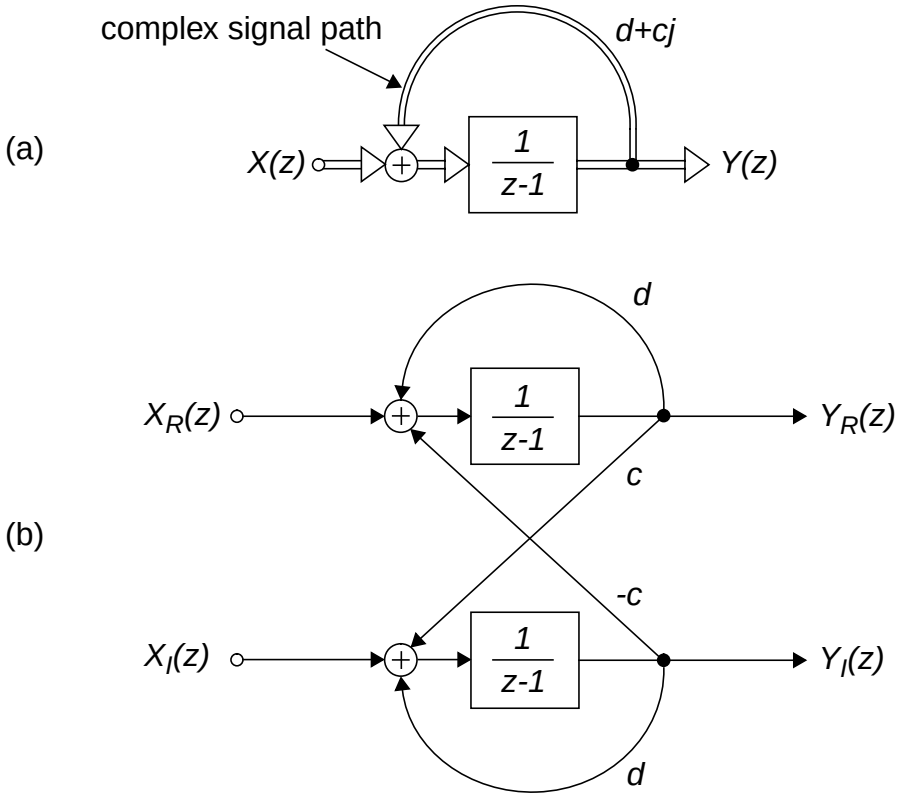

Fig. 3.9 Creating a pole at $z = 1 + d + jc$ using (a) a complex signal flow graph and (b) a two-path signal flow graph.

Constructing complex integrators in this pole-sharing fashion means that one complex pole is created with a second-order filtering section; so, a complex modulator with fourth-order in-band noise shaping requires only eight orders of filtering. That is, with *N*th-order filtering in the complex ΔΣ loop, one can realize *N*/2 zeros at a band of frequencies anywhere, positive or negative. An *N*th-order real bandpass modulator similarly realizes *N*/2 zeros in-band, though that band is restricted to occur at both positive and negative frequencies (which we surmised earlier might be wasteful, and which is shown to be so in Section 3.3).[1]

3.2.3 A General Quadrature ΔΣ Architecture

A structure that realizes a fourth-order quadrature ΔΣ modulator is shown in Fig. 3.10. Each of the four complex integrators embedded in the feedback loop is constructed as shown in Fig. 3.9(b). The structure is actually the extension, to complex form, of a similar structure used in higher-order real ΔΣ modulators [5 Jantzi][20][52]. It can be described as a chain of complex integrators with distributed feedback and a distributed feed-forward input.

In a sense, such a two-path architecture bears a resemblance to time-interleaved and parallel ΔΣ modulator structures [53][54]. Those techniques use multiple interconnected modulators to realize high noise-shaping performance on real inputs at reasonable sampling rates. Quadrature ΔΣ modulators, however, use two modulator channels that are specifically coupled so that they treat a pair of input signals as a single complex one.

I. Benefits of a General Structure

The general structure shown facilitates the independent positioning of all transfer-function poles and zeros, which is advantageous since noise-shaping can then be performed at an arbitrary fraction of the sampling frequency and since noise-shaping zeros can be spread optimally across the band of interest. Many bandpass ΔΣ structures do not have this design freedom, being constrained to having coincident noise-shaping zeros that are fixed at $f_s/4$ [26][15]. One penalty paid for the generality is an increase in the number of coefficients (capacitors) needed in the implementation.

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1. Remember too, the receiver of Fig. 3.1 requires *two* real bandpass ΔΣ modulators, which then requires twice the total order compared with the one quadrature modulator used in Fig. 3.6.

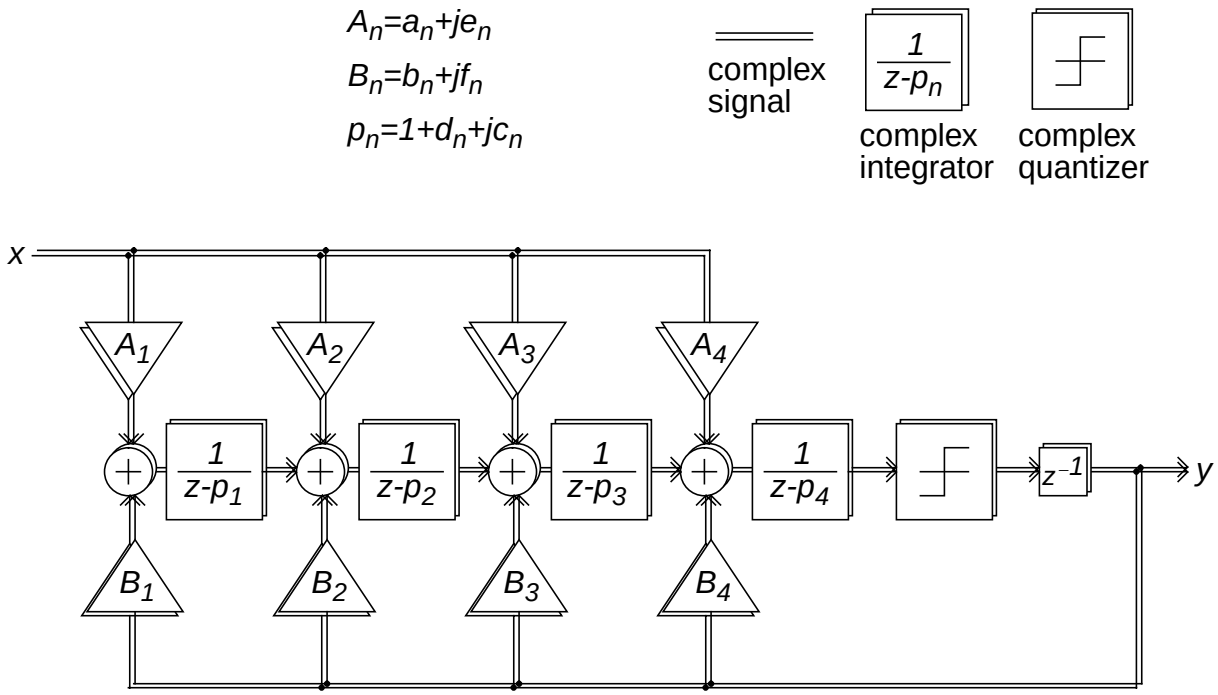


Fig. 3.10 General structure for a fourth-order quadrature ΔΣ modulator.

Arbitrary band placement means that a sampling rate can be chosen in order to achieve desired SNR performance over a specified bandwidth, without regard to center frequency. The latter can then be chosen as is optimal for the application at hand, if a specific IF is particularly desirable, for example.[1] Optimal positioning of zeros within the band of interest significantly increases the SNR obtainable by a given modulator order [20][55 Jantzi][56].

II. The Structure's Transfer Functions

The modulator input feeds in to each stage through the complex *A* coefficients, which set three zeros of the complex STF. The zeros of the complex NTF are set by the complex pole (integrator) positions, and thus by the *p* coefficients. Complex quantization is performed at the output, giving a one-bit output for each channel. The single-bit outputs feed back into the modulator stages through the *B* coefficients, which set the positions of the NTF and STF poles.

1. As mentioned in Section 3.1.1, strategic choice of IF can greatly alleviate receiver image-rejection concerns [44].

The structure can be linearized and its input-output relationships solved. This produces a set of *z*-plane equations, in polynomial form, that can be used to choose circuit coefficients once the desired NTF and STF pole-zero placement has been determined. These equations are included in Appendix A.

3.2.4 Noise-Transfer-Function Design

I. Design Specifications

The four in-band zeros realized by the structure of Fig. 3.10 should allow considerable SNR to be achieved over considerable bandwidths. The 200-kHz bandwidth specification for the GSM standard [45] is chosen as the design objective, so that narrower-bandwidth specifications[1] can be handled as well. The modulator can then be operated at a lower sampling rate to achieve similar performance in the smaller bandwidths, or run at the same sampling rate to achieve higher performance therein.

Choosing an angular center frequency of $3\pi/4$ in the *z*-plane gets us away from the sometimes troublesome band around $\pi/2$,[2] and provides the opportunity to prove the generality of the proposed structure. To provide a reasonably wide bandwidth with an acceptable sampling rate, an angular bandwidth of $\pi/32$ is selected.

At a sampling rate of f_s = 13 MHz, these *z*-plane specifications correspond to a center-frequency of f_c = 4.875 MHz, and a bandwidth of just slightly over f_b = 200 kHz — which in a real system would result in an oversampling ratio of $R = f_s/2f_b \approx 32$. In the complex system too, the oversampling ratio is approximately 32. It remains unchanged because, although the Nyquist frequency is twice as large — inputs with bandwidths all the way up to f_s can be uniquely distinguished when using complex sampling — the effective sampling rate also doubles, since there are now two bit-streams running at rate f_s.

---

1. CT2+ uses 100-kHz bandwidth; AMPS and IS-136 use 30-kHz bandwidth.
2. Clock signals, or their various mixing products, are more likely to leak in-band for modulators centered at $\pi/2$. Furthermore, quadrature $\Delta\Sigma$ modulators centered at $\pi/2$ often appear unstable, or to settle into limit cycles, for small input signals.

II. Lowpass-Prototype Methodology

A pole-zero optimizer (such as filtorX [55]) can be used to design the complex transfer function directly for the desired specifications, but tools that can handle complex transfer functions are not generally available, and such optimization can be burdensome.

Instead, we note that a complex frequency response is simply a frequency-shifted version of a real response — which in the *z*-plane is accomplished by the rotation of a lowpass pole-zero constellation. This means that all the techniques for designing lowpass modulators, including closed-form expressions for the optimal placement of noise-shaping zeros [56], can be borrowed for complex design.

A real, fourth-order, lowpass prototype was designed — using filtorX [55 Jantzi], closed-form expressions [56], a ΔΣ design toolbox [57], and Matlab [58] — to meet the bandwidth specifications. The prototype NTF was designed under the standard constraints of ΔΣ modulator design as outlined in Section 2.1.2: maximum in-band attenuation for quantization-noise suppression; small out-of-band gain (less than 4 dB) to help modulator stability; and a first NTF impulse-response coefficient of unity to avoid any delay-free loops containing the quantizer.

The resulting pole-zero plot is shown in Fig. 3.11(a) and the associated full-band magnitude response (i.e. from $-f_s/2$ to $f_s/2$) is shown in Fig. 3.11(b). Four zeros of the NTF are placed in the in-band region, to suppress quantization noise, while the four poles are clustered in a butterworth configuration around the in-band region to minimize the out-of-band NTF gain.

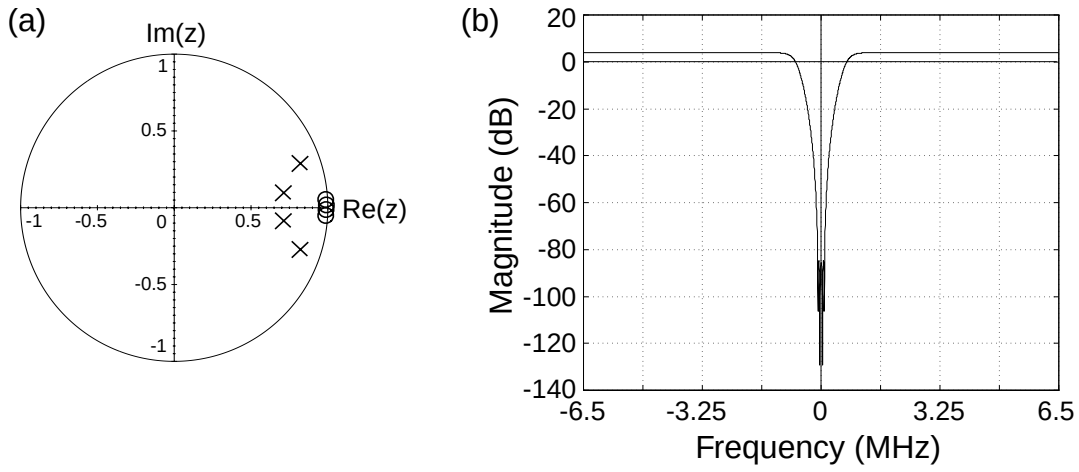


Fig. 3.11 Fourth-order lowpass prototype noise transfer function.
(a) Pole-zero constellation. (b) Magnitude response.

III. Shifting to Complex Frequencies

This lowpass-prototype function was frequency shifted to an angular center frequency of $\theta = 3\pi/4$ — by multiplying all pole and zero locations by $e^{j3\pi/4}$ — resulting in the pole-zero plot of Fig. 3.12(a) and the magnitude response of Fig. 3.12(b), which includes an expanded view of the in-band region. Note that the poles and zeros have no complex-conjugates and that the magnitude response is not symmetric about dc (i.e. the function is complex). The pole-zero locations are summarized in Table 3.1.

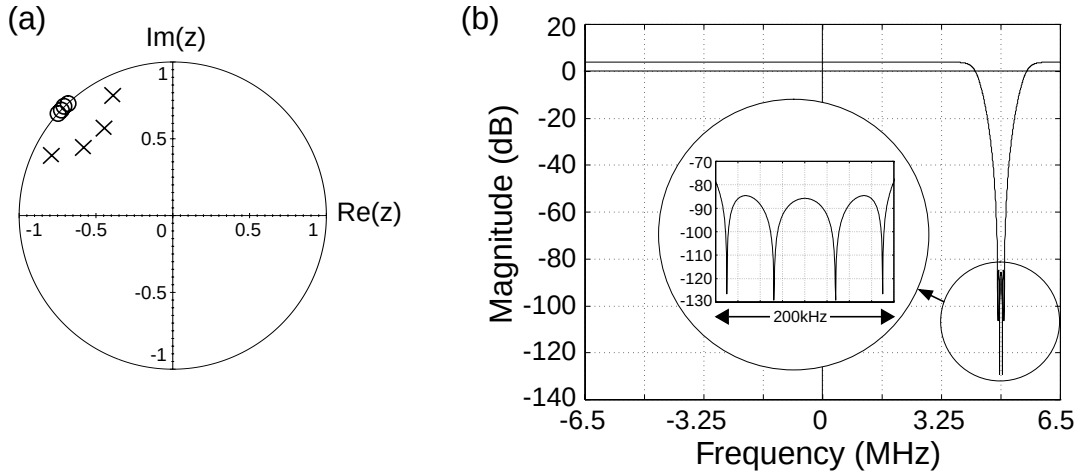


Fig. 3.12 Fourth-order complex noise transfer function. (a) Pole-zero constellation. (b) Magnitude response, with an inset showing a 200-kHz wide in-band region.

Table 3.1: Modulator Pole-Zero Locations

Singularity	Zero	Pole
1	-0.71881 + 0.69521j	-0.78199 + 0.38687j
2	-0.69521 + 0.71881j	-0.38687 + 0.78199j
3	-0.73636 + 0.67659j	-0.57442 + 0.43877j
4	-0.67659 + 0.73636j	-0.43877 + 0.57442j

3.2.5 The Signal Transfer Function

The STF has only feed-forward inputs into the main structure shown in Fig. 3.10, so it shares poles with the NTF; this saves on hardware and presents no significant limitations. Four complex inputs to the structure allow three STF zeros to be positioned.

A possible STF pole-zero plot is shown in Fig. 3.13(a), and its magnitude response in Fig. 3.13(b). This STF has an in-band gain of 0 dB and out-of-band rejection of more than 40 dB. A complex bandpass filtering function is achieved by placing zeros at $z = j$ (3.25 MHz), $z = -1$ (±6.5 MHz), and $z = 1/\sqrt{2} - j/\sqrt{2}$ (-1.625 MHz). The in-band STF has magnitude flat to within 0.04 dB and phase linear to within $\pm 0.02°$.

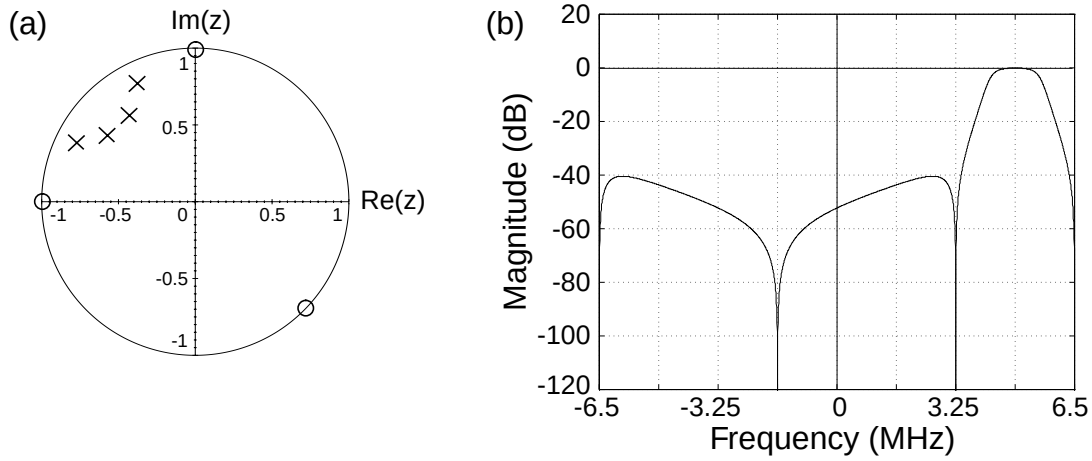


Fig. 3.13 The signal transfer function (STF). (a) Pole-zero constellation. (b) Magnitude response.

Even with no finite zeros, the STF would have been flat in-band given the butterworth positioning of the poles. The addition of the three zeros does little to change the in-band characteristics, but does allow the nulling of certain portions of the input spectrum, perhaps to help minimize specific interferers prior to conversion.

More design details are given for this modulator in Appendix B.

3.2.6 Ideal Simulated Performance

I. Output Spectra

Full system-level simulations were performed on the fourth-order modulator just described. Simulink [59], an extension to Matlab [58], was used to describe a system configuration like that in Fig. 3.10. The complex input tone was composed of a cosine and sine signal, each of peak amplitude half the size of the peak feed-back levels of the modulator, and each of frequency just slightly above band center.

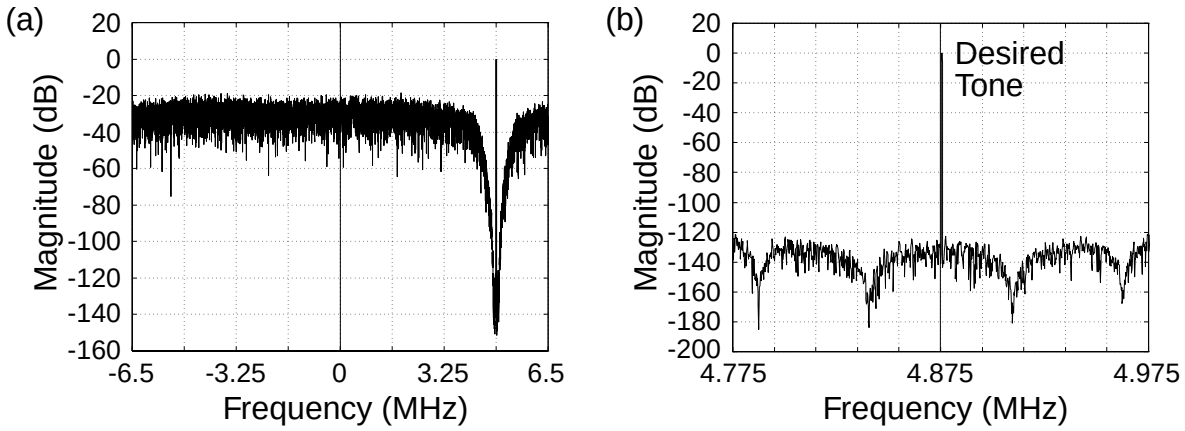


Fig. 3.14 (a) 8k-bin output spectrum of a simulated fourth-order quadrature modulator. (b) In-band portion of a 64k-bin spectrum. The portion shown contains 1009 bins.

Fig. 3.14 shows the complex output spectrum of the modulator simulated under those conditions. The spectrum confirms our supposition: appropriate placement of noise-shaping zeros using a complex loop filter can effect asymmetric noise shaping. The output spectrum shows a complex tone in a noise valley centered at 4.875 MHz, as designed. Fig. 3.14(b) shows a zoom of the in-band region. The four notches are visible across the band, appearing as they did in the inset of Fig. 3.12(b) (which showed the linear-model NTF).

Note that if the output *I* and *Q* connections are reversed, the noise-shaped band will effectively occur in the mirror-image band (i.e. at -4.875 MHz in the case above). This, along with the ability to swap the *I* and *Q* input connections or to use any of the signal-band's aliases (in an undersampling approach), gives additional freedom in the choice of modulator input frequency. As always, undersampling approaches require much more stringent anti-alias filtering.

II. Full-Scale Signal Amplitude

In a real modulator, input-signal amplitude is typically defined as an input sinusoid's peak amplitude relative to the modulator's peak feedback levels. For example, if the modulator feedback levels are ± 1 , a sinusoid with a peak level of 1 is considered to be a full-scale input (i.e. a 0-dB input, relative to the feedback levels). A half-scale input would be denoted a -6-dB input, and would appear as such in an output spectrum (which was the case, for example, in Fig. 3.4).

A similar definition of full scale is used in a quadrature modulator, where a 0-dB complex input signal is defined as being composed of cosine and sine inputs that *each* have peak

amplitudes equal to the peak feedback level. This definition produces a side effect: when the *I* and *Q* signals are combined in a quadrature modulator, the signal bin in the output spectrum grows by 6 dB (as was the case with Fig. 3.5 compared to Fig. 3.4).

Thus, for two half-scale inputs, the complex output signal bin will be at 0 dB (as in Figs. 3.5 and 3.14), and for two full-scale inputs the output signal bin will reach +6 dB. To avoid this somewhat unsettling visual result, the entire complex output spectrum, noise and signal, will be normalized — i.e. shifted down by 6 dB — in future plots herein. Thus, the 0-dB level in the output spectrum of a complex modulator will equate to the case of two 0-dB (full-scale, real) input signals. The normalization is done for purely aesthetic reasons, and does nothing to alter SNR calculations, for instance.

III. Modulator Signal-to-Noise Ratio

The modulator's signal-to-noise ratio (SNR) can be determined by calculating the ratio of signal power to integrated in-band noise power in its output spectrum. Plotting SNR values for varying input amplitudes reveals two important metrics of modulator performance: peak SNR is the maximum SNR attained over all input levels, while dynamic range is the range of input amplitudes over which the modulator is useful.[1]

Fig. 3.15 shows a plot of SNR versus input amplitude for the above modulator. The modulator achieves approximately 103-dB peak SNR (the highest SNR on the graph) and nearly 105-dB dynamic range. Bear in mind, however, that these results are for system-level simulations that do not take into account any non-ideal or circuit-implementation effects.

A point of interest on the plot is the input amplitude at which the SNR levels off and then drops. This is a metric of modulator stability, and occurs at approximately -5 dB for the above modulator. The maximum input value is related to the maximum out-of-band NTF gain chosen in the modulator design: larger out-of-band gain — which results in deeper in-band noise shaping — will cause a smaller maximum tolerable input; smaller out-of-band NTF gain — which indicates a more conservative design that has poorer in-band noise shaping — will tend to

1. Dynamic range is defined by a difference in input amplitudes: at the low end, the input amplitude which results in 0-dB SNR; at the high end, the largest input amplitude allowable before the modulator becomes unstable (which causes a drastic reduction in SNR).

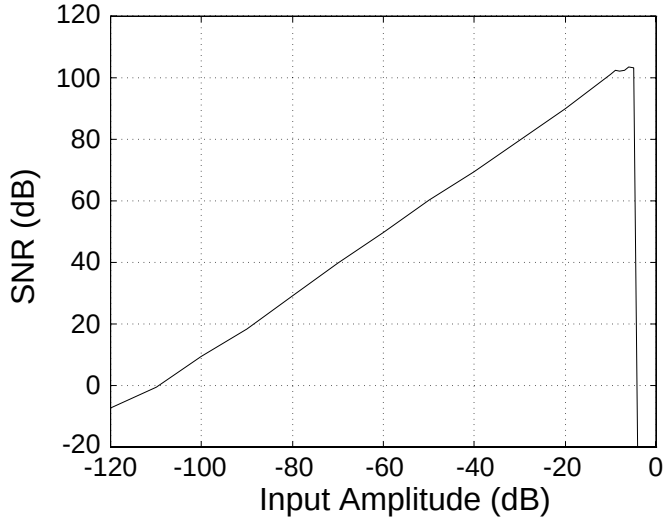


Fig. 3.15 Simulated SNR versus input amplitude. 0 dB indicates full-scale input sinusoids (i.e. cosine and sine signals with peak amplitudes equal to the peak feedback level).

increase the range of input amplitudes over which the modulator remains stable. From an SNR standpoint, there is an optimum trade-off between peak out-of-band NTF gain and maximum allowable input strength [60].

3.3 The Real-Versus-Quadrature ΔΣ Comparison

The in-band noise shaping of the quadrature modulator in Fig. 3.14 appears to be deeper than that achieved by the pair of real modulators in Fig. 3.5, even though the quadrature modulator has a lower oversampling ratio (32, rather than 91). Thus, moving the two zeros from the image band to the in-band region has seemingly bought us higher performance, at no cost in order.[1]

3.3.1 Quadrature-Modulator Advantages for Complex Input Signals

To quantify the advantages of quadrature modulators over real modulators, a comparison is made using a set of baseline design specifications (in order to keep the modulators on even ground): a sampling rate of f_s = 13 MHz, a center frequency of f_c = 4.875 MHz, and a bandwidth of just slightly over f_b = 200 kHz (for an oversampling ratio of exactly 32). All modulators have poles placed in a butterworth arrangement, zeros optimally spread across the band of interest, and peak out-of-band NTF gain of 4 dB.

1. The first simulation used two real fourth-order bandpass modulators, which require a total of eight filter orders; the second uses one complex modulator with four in-band zeros, which also requires eight filter orders.

I. Twin Fourth-Order Real Modulators (Total Order = 8)

To convert complex inputs, as in the receiver of Fig. 3.1, two real bandpass ΔΣ modulators are needed. For the specifications listed above, two fourth-order modulators with pole-zero plots like that in Fig. 3.16(a) could be used, requiring a total filter-order of eight. For complex tone inputs, the pair achieves a peak SNR of approximately 58 dB in the 200-kHz bandwidth, as seen in the lower plot in Fig. 3.16(a).

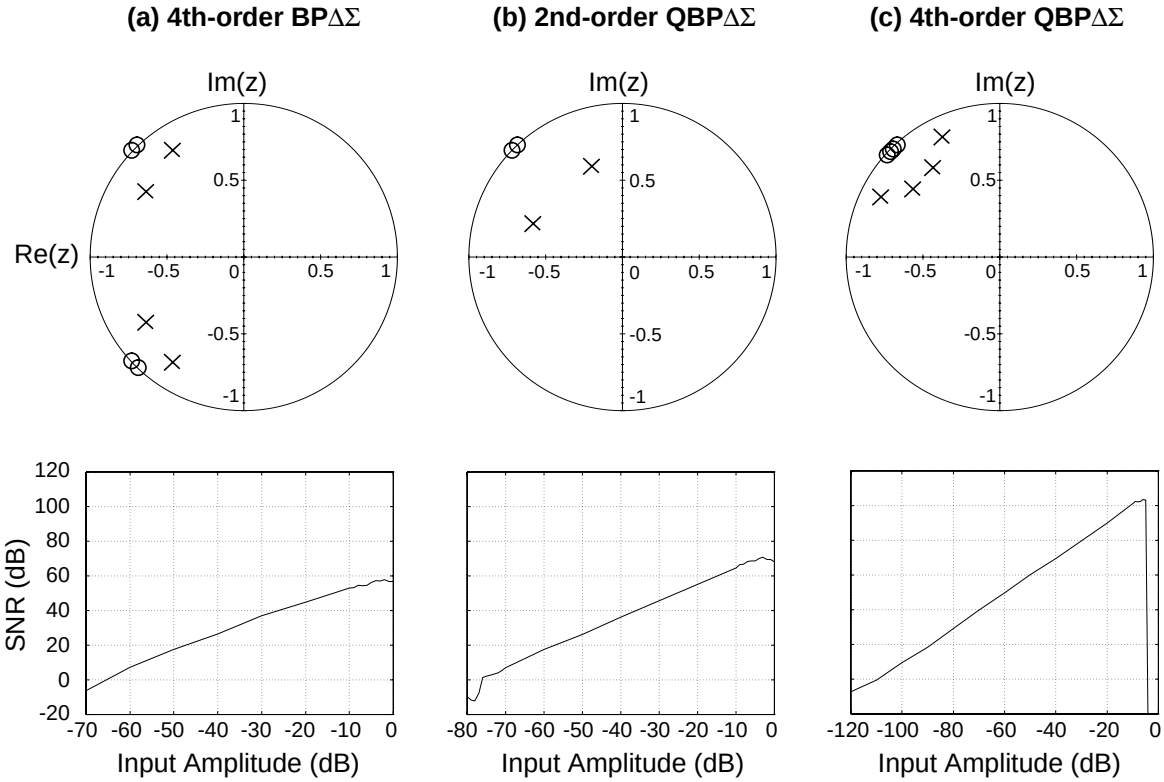


Fig. 3.16 Comparison of real and quadrature bandpass ΔΣ modulators. (a) Pole-zero plot for a real fourth-order modulator, and SNR performance for a pair of such modulators operating on a complex input. (b) A second-order complex modulator and its SNR performance. (c) A 4th-order complex modulator and its SNR performance.

II. One Second-Order Quadrature Modulator (Total Order = 4)

Surmising that the noise shaping in negative frequencies is wasteful, a second-order quadrature modulator (i.e. with second-order in-band noise shaping) is designed which eliminates the negative-frequency notches. The quadrature modulator requires a total filter-order of only four, and has a pole-zero plot shown in Fig. 3.16(b). This modulator achieves approximately 71-

dB peak SNR in the same 200-kHz bandwidth — giving a 13-dB (2-bit) performance increase with half the total order.

III. One Fourth-Order Quadrature Modulator (Total Order = 8)

Instead, the total filtering order can be held at eight, and the two negative-frequency zeros moved to positive frequencies (as in Fig. 3.16(c)). The peak SNR achievable for this fourth-order quadrature modulator is 103 dB in the 200-kHz bandwidth — or a 45-dB (>7-bit) improvement in peak SNR, for *equal* total order.

If such drastic SNR improvement is not needed, the quadrature modulator can instead operate on wider bandwidths than the pair of real modulators. A single quadrature modulator with four in-band notches — similar to that shown in Fig. 3.16(c) but with zeros spread across a wider band — achieves the original 58-dB SNR across a bandwidth of more than 650 kHz (more than three times the original bandwidth).

Thus, a quadrature modulator can achieve lower total order, higher SNR, or higher bandwidth, or some combination of the three, when compared with a pair of real bandpass modulators. Clearly, in the ideal case, a quadrature $\Delta\Sigma$ modulator should always replace a pair of real ones when A/D modulation of complex signals is needed.

3.3.2 Noise-Shaping Degradation due to Conjugate-Band Zeros

To understand the basis for the advantage, consider a transfer function whose pole-zero constellation has neither poles nor zeros. The gain at the point $z = 1$ is unity. If a zero is now added in the left-half of the unit circle, at $z = -1$, the gain seen for points on the right half of the unit circle goes up. At $z = 1$, the gain is two. That is, forcing attenuation on one half of the unit circle hurts attenuation on the other half [48].

For a quantitative comparison, a figure-of-merit is calculated for NTF appraisal, which is the in-band integral of the NTF-magnitude squared, or

$$F = \frac{1}{2\pi}\int_{\omega_1}^{\omega_2} |H(\omega)|^2 d\omega . \qquad (3.26)$$

If the linear model of the modulator is used, and a fixed quantizer step size assumed, the noise spectral density is white and well-defined. Thus, the figure-of-merit is really a measure of in-band noise power, and, of course, lower is better.

Changing variables, and noting that $de^{j\omega} = je^{j\omega}d\omega$, gives

$$F = \frac{1}{2\pi}\int_{e^{j\omega_1}}^{e^{j\omega_2}} |H(e^{j\omega})|^2 \left\{\frac{de^{j\omega}}{je^{j\omega}}\right\}. \tag{3.27}$$

Finally, a one-sided integral, usable since the function is a symmetric one,[1] simplifies the calculations; substituting $z = e^{j\omega}$ gives:

$$F = \frac{1}{\pi}\int_{1}^{z_2} |H(z)|^2 \left\{\frac{dz}{jz}\right\} = \frac{1}{\pi j}\int_{1}^{z_2} H(z)H(z^{-1})\frac{1}{z}dz\,. \tag{3.28}$$

I. Comparing Two Modulators

A first-order lowpass modulator with a pole at the origin and a notch at $z = 1$, as shown in Fig. 3.17(a), will be examined for lucidity; its NTF is $H(z) = (1 - z^{-1})$. Assuming an

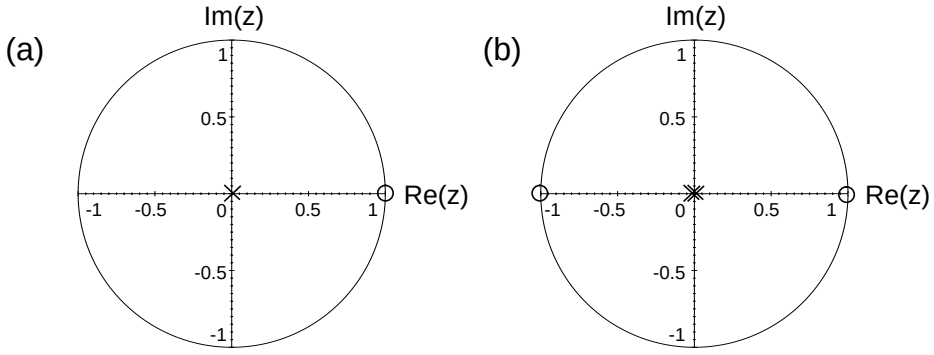


Fig. 3.17 (a) First-order lowpass modulator with $H(z) = (1 - z^{-1})$. (b) The same modulator with an additional zero at $z = -1$ and an additional pole at the origin.

1. The results are identical for complex pole-zero constellations as well, if they are symmetric about some bisecting line of the unit-circle.

oversampling ratio of 64 — which represents bandwidth equivalent to that of the quadrature modulators discussed up until now, which had oversampling ratios of 32 — the figure of merit is:

$$F_1 = \frac{1}{\pi j}\int_1^{e^{j\pi/64}} (1-z^{-1})(1-z)\frac{1}{z}dz = \frac{1}{\pi j}\int_1^{e^{j\pi/64}} (2z^{-1}-1-z^{-2})dz, \tag{3.29}$$

which solves to

$$F_1 = \frac{1}{\pi j}(2\ln z - z + z^{-1})\Big|_1^{e^{j\pi/64}} = \frac{1}{32} - \frac{2}{\pi}\sin\frac{\pi}{64}. \tag{3.30}$$

Modifying the noise transfer function to have an additional zero at $z = -1$ — and adding an additional pole at $z = 0$ to keep the orders of the numerator and denominator equal — results in $H(z) = (1-z^{-1})(1+z^{-1})$, which is shown in Fig. 3.17(b). This is essentially a lowpass-highpass modulator hybrid. The new figure-of-merit, across the same bandwidth, is

$$F_2 = \frac{1}{\pi j}\int_1^{e^{j\pi/64}} (1-z^{-2})(1-z^{2})\frac{1}{z}dz = \frac{1}{\pi j}\int_1^{e^{j\pi/64}} (2z^{-1}-z-z^{-3})dz, \tag{3.31}$$

which solves to

$$F_2 = \frac{1}{\pi j}\left(2\ln z - \frac{z^2}{2} + \frac{z^{-2}}{2}\right)\Bigg|_1^{e^{j\pi/64}} = \frac{1}{32} - \frac{1}{\pi}\sin\frac{\pi}{32}. \tag{3.32}$$

The ratio of the two figures is

$$\frac{F_2}{F_1} = 3.999. \tag{3.33}$$

That the figure is four times higher (worse) for the second transfer function is expected. The extra zero at $z = -1$ causes a two-times increase in the NTF gain near dc, which is the in-band region. Since noise power is related to the magnitude-squared of the in-band NTF gain, the integrated noise power actually goes up by four times. This represents a 6-dB (1-bit) SNR degradation for the modulator that has a second zero across the unit circle from the in-band one.

Clearly, this example parallels the case of a quadrature modulator versus a real one: rotate each set of zeros in Fig. 3.17 by $\pi/2$ to see that the first is a quadrature NTF with a single notch at $\pi/2$, while the second is a second-order real bandpass NTF with notches at $\pm\pi/2$. The difference in achievable SNR is most pronounced for cases such as this, where the conjugate zero is the full unit-distance across the unit circle — and thus causes the largest increase in in-band NTF gain — but it is substantial for other NTFs as well. Note that the effect is even larger when clusters of zeros are involved (i.e. for higher-order NTFs).

This is the essential reason for the superior in-band noise shaping of a quadrature modulator. The fact that removing the image-band zeros gives an SNR advantage *along* with a reduction in total modulator order (i.e. the case of Fig. 3.16(a) versus Fig. 3.16(b)) makes quadrature $\Delta\Sigma$ modulators that much more attractive for the A/D modulation of complex inputs.

3.3.3 Modulation of Real Inputs

The first comparison (*I* versus *II*) in Section 3.3.1 showed that a single quadrature modulator out-performed two real modulators in converting a complex input signal, with the former requiring only half the total order of the latter. It seems plausible, therefore, that quadrature modulators may prove superior for the conversion of real inputs as well [48].

The single fourth-order real modulator in Fig. 3.16(a) achieves more than 55-dB peak SNR for a real, tone, input. The second-order quadrature modulator in Fig. 3.16(b) achieves more than 66-dB peak SNR for the same real input.[1] Thus, for equal filter order, the quadrature modulator manages to out-perform its real counterpart by 11 dB. The modulators' SNR curves are shown in Fig. 3.18, for inputs 10-dB below full-scale and above.

These simulations raise another point: whereas the real modulator reaches peak SNR for inputs about 2-dB below full scale, the quadrature modulator does so for a full-scale real input. This suggests that the quadrature modulator might be somehow "more stable" than the real one. Alternately, the quadrature modulator may be able to represent larger real signals because it does so using twice the number of output quantizers.

1. The *Q* input is grounded, and the *I* input used as the lone modulator input (or vice versa).

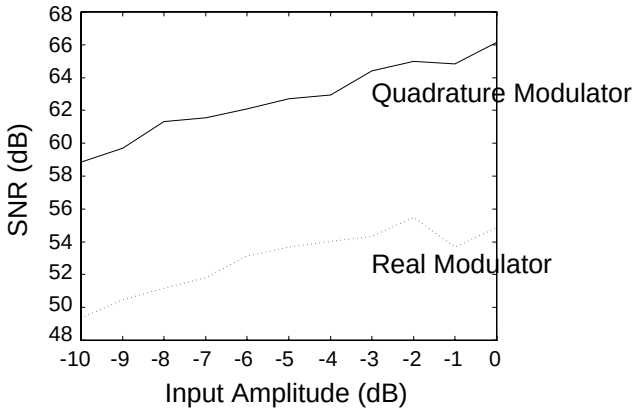


Fig. 3.18 Performance comparison for a quadrature modulator and a real modulator converting real input signals.

3.3.4 Stability Comparison

To investigate the phenomenon further, a new set of modulators is used. These modulators have peak NTF gain of 12 dB,[1] rather than the more conservative 4 dB of the previous set.

The new quadrature modulator remains well-behaved, even for real inputs up to full-scale, reaching a peak SNR of nearly 70 dB. The real modulator, on the other hand, is unstable, even for zero input. The fact that the real modulator is unstable for zero input — as opposed to simply reaching SNR degradation for smaller inputs than does the quadrature modulator — points to the difference being due to the internal workings of the quadrature modulator, and not simply to its possessing double output quantizers.

Indeed, a quadrature modulator gains a stability advantage over a traditional bandpass modulator because its poles and zeros are those of a rotated lowpass modulator, as we saw in Section 3.2.4. Real bandpass modulators — especially those near dc or $f_s/2$ — are more akin to lowpass modulators that have been doubled in order, and are hence less stable.

1. 12-dB peak NTF gain is that seen by a second-order lowpass modulator with $H(z) = (1 - z^{-1})^2$.

3.4 Anti-Alias Filtering

I. Real Versus Complex Filtering

Consider a band centered at an angular frequency of θ_0 in the z plane, with a bandwidth of θ_b. In a sampled-data real system, the first frequencies that alias into the signal band occur at an angular frequency of $2\pi - (\theta_0 + \theta_b/2)$. The anti-alias filter's transition band then, between the upper edge of the signal band and the lower edge of the first alias band, is from $\theta_0 + \theta_b/2$ to $2\pi - (\theta_0 + \theta_b/2)$. For our typical modulators centered at $\theta_0 = 3\pi/4$, and assuming narrow bandwidth relative to the center frequency, the transition band extends only from $\theta = 3\pi/4$ to $5\pi/4$. This represents a transition-band width of only $\pi/2$, one-quarter of the sampling rate.

In a sampled-data complex system, signals on the upper and lower halves of the unit circle are distinguishable, so the first alias bands do not occur until a full angle of 2π has been traversed. This equates to a transition-band width equal to the sampling rate. So, again for our typical modulators, a band centered at $\theta_0 = 3\pi/4$ does not encounter its first alias band until $\theta = 11\pi/4$ on one side, or $\theta = -5\pi/4$ on the other. Thus, if a complex bandpass anti-alias filter is used, centered at the band of interest, there is the predicted transition band of width 2π above and below. Complex continuous-time filters exist in the literature, and are reasonably straightforward to implement using standard components [24].

If real anti-alias filters are used in each channel of the complex system, however, the filters, which are forced to have symmetric magnitude responses, must remove signals at $\theta = -5\pi/4$ while passing those at $\theta = \pm 3\pi/4$. This necessitates the original, tighter, transition band of only one-quarter the sampling rate. The results are contrasted pictorially in Fig. 3.19.

II. IMR Effects of Complex Anti-Alias Filtering

The figure brings out a further advantage of complex anti-alias filtering: it helps to reduce the size of image inputs prior to their reaching the $\Delta\Sigma$ modulator, and thus improves the overall image-rejection performance of the back-end (i.e. the anti-alias-filter/$\Delta\Sigma$-modulator combination). As discussed in Section 3.1.1, the image-band input to the back-end can potentially be larger than the desired signal, making back-end image rejection very important. Strategic image placement, combined with complex anti-alias filtering, can greatly reduce the image-rejection requirements of the $\Delta\Sigma$ modulator itself.

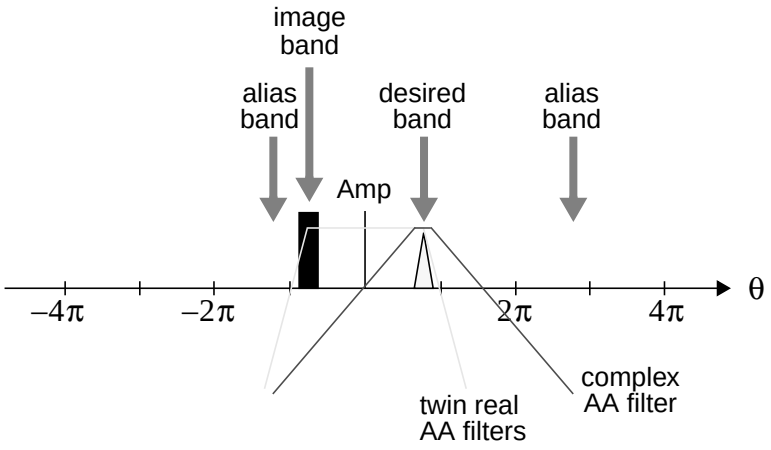


Fig. 3.19 Comparison between complex and real anti-alias filters in a complex-sampling system. A complex anti-alias filter has more relaxed transition-band requirements.

3.5 Decimation for Quadrature ΔΣ Modulators

A complex demodulator and (multiplexed) complex lowpass filter are often used to reduce the bit rate of a real bandpass modulator to a manageable level, as illustrated in Fig. 3.20. In this scheme, the bit-stream is modulated down to baseband by multiplication by $e^{-j\theta_0 n}$ and then filtered by a complex lowpass filter. Choosing θ_0 equal to a simple fraction of π allows both the complex modulator and the complex filter to be implemented with relatively simple hardware [15][20][27].

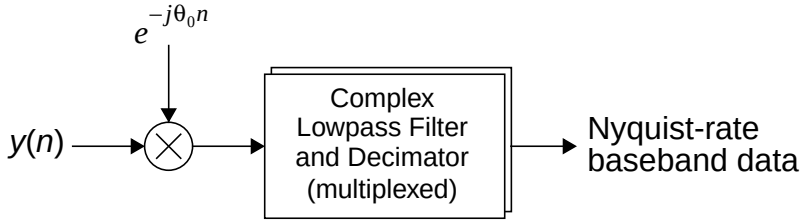


Fig. 3.20 A bandpass decimator employing complex modulation.

As an example, a decimator for the case $\theta_0 = 3\pi/4$ uses a multiplying signal which is a sum of two period-8 signals containing only zeros, plus or minus ones, and scaled plus or minus ones:

$$e^{-j\theta_0 n} = \cos\theta_0 n - j\sin\theta_0 n \text{ , where } n = 0, 1, 2, \ldots$$

$$= \left(1, \frac{1}{\sqrt{2}}, 0, -\frac{1}{\sqrt{2}}, -1, -\frac{1}{\sqrt{2}}, 0, \frac{1}{\sqrt{2}}, \ldots\right) + j\left(0, -\frac{1}{\sqrt{2}}, -1, -\frac{1}{\sqrt{2}}, 0, \frac{1}{\sqrt{2}}, 1, \frac{1}{\sqrt{2}}, \ldots\right).$$

Similarly, other choices of θ_0 which are rational fractions of π ($\theta_0 = \pi/2$ being the most common choice [15]) yield periodic modulation signals which can be decomposed into the sum of several 0, ± 1 streams multiplied by constants [27]. The decomposition can generally be arranged to provide non-overlapping multiplying streams, which allows a single multiplexed lowpass filter to perform the filtering. After the output of this filter is down-sampled, the streams are recombined with a few additions and multiplications to yield the decimated, bandpass-filtered complex data.

In the case of a quadrature $\Delta\Sigma$ modulator, the output stream itself is complex, so demodulation entails multiplying two complex sequences:

$$[I(n) + jQ(n)]e^{-j\theta_0 n} = [I(n) + jQ(n)](\cos\theta_0 n - j\sin\theta_0 n), \tag{3.34}$$

where $n = 0, 1, 2, \ldots$

Thus, the baseband I and Q sequences, $I_0(n)$ and $Q_0(n)$, are

$$I_0(n) = I(n)\cos\theta_0 n + Q(n)\sin\theta_0 n \tag{3.35}$$

and

$$Q_0(n) = Q(n)\cos\theta_0 n - I(n)\sin\theta_0 n. \tag{3.36}$$

The demodulation scheme is pictured in Fig. 3.21.

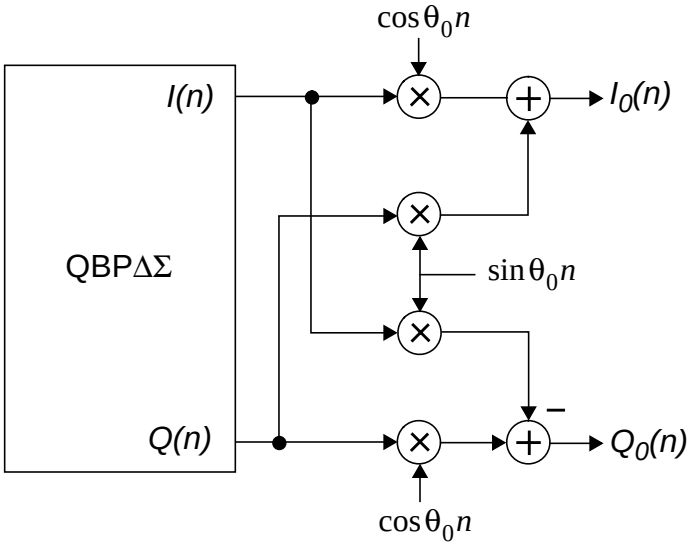


Fig. 3.21 Complex demodulation of the quadrature modulator's output streams.

The multi-level baseband streams are then passed to standard digital decimation filters, which reduce the bit-rate to the Nyquist rate and remove out-of-band quantization noise [20]. Thus, it is apparent that the problem of decimation for quadrature bandpass ΔΣ modulation is only marginally more involved than for traditional bandpass modulation.

3.6 Summary

A new low-IF receiver architecture has been proposed to alleviate many problems of the direct-conversion receiver. The architecture retains its image-rejection properties, but the non-zero IF means that $1/f$ noise and dc offsets cause no problem, self-interference is not an issue (because the oscillator frequency is offset from the carrier frequency), and even-order distortion has less effect. With modern quadrature mixers, and strategic image placement, the low-IF architecture provides a viable solution for realizing single-chip radio receivers.

The low-IF architecture requires two real bandpass ΔΣ converters — thus doubling the order (and area and power) required to perform A/D modulation on the complex analog signals — so a quadrature variant of a ΔΣ modulator was proposed. This architecture avoids the double-order penalty by sharing poles in its complex structure, and proves invaluable for performing A/D modulation on quadrature signals in any system.

Quadrature modulator structures and transfer functions were discussed, and a design methodology given. Simulated performance was presented and explained, demonstrating the concept of asymmetric noise shaping. This noise shaping was shown to give quadrature modulators significant advantages over pairs of real modulators for the conversion of complex inputs, allowing lower total order, higher SNR, higher bandwidth, or a combination thereof.

Quadrature modulators were shown to have performance advantages for the conversion of real inputs as well, since they do not suffer in-band noise-shaping degradation due to conjugate-band zeros. They were furthermore seen to gain a stability advantage over traditional bandpass modulators, since their poles and zeros are simply those of rotated lowpass modulators.

Finally, it was shown to be advantageous to use complex anti-alias filtering when performing complex-signalled sampling, since it improves both the alias rejection and the image rejection of the back-end portion of the low-IF receiver. Decimation was discussed, and seen to be only marginally more intricate than what is required for real modulators.

CHAPTER 4

Non-Ideal Effects

This Chapter examines the effects of mismatch upon the performance of the fourth-order quadrature ΔΣ modulator designed in Chapter 3. In order to understand the implications of mismatch, a simple complex bandpass filter is first subjected to differential coefficient perturbation, and examined in detail. These results are then applied to the more intricate case of a non-ideal fourth-order quadrature feedback system [61 Jantzi].

The quadrature-modulator versus bandpass-modulator-pair performance comparison is made, as it was in Chapter 3, but this time with the influence of coefficient and amplifier non-idealities. It is seen that the quadrature modulator loses its huge performance advantage due to the severe effects of mismatch.

The understanding garnered in this Chapter proves invaluable when dealing with complex systems, ultimately providing the knowledge necessary to combat the deleterious effects of mismatch.

4.1 Modulator Performance with Non-Idealities

In a circuit implementation, the coefficients of the system (Fig. 3.10) are realized by capacitor ratios, making them dependent upon the accuracy with which a feed-in capacitor can match an integrating capacitor. Furthermore, amplifiers implemented with physical circuits do not have infinite dc gain, and are not exact replicas from stage to stage, or from channel to channel.

The modulator from the previous chapter can be re-simulated to discern the effects of mismatch on modulator performance. Capacitor ratios with uniformly-distributed random errors, with 0.5% peak error, and amplifiers with random dc gain between 50 and 60 dB — but which are matched to within 2 dB (i.e. about 25% linear gain) between the real and imaginary channels within a stage — are used in these simulations.

Fig. 4.1(a) shows the 8k-bin output spectrum of the fourth-order quadrature modulator under these non-ideal conditions. The in-band noise floor is higher than in the ideal case (Fig. 3.14), as is clearly shown in Fig. 4.1(b), which presents an overlay of the ideal and non-ideal in-band spectra. The non-idealities have caused a large increase in the amount of in-band quantization noise, in this case reducing SNR from 103 dB in the ideal case to only 60 dB in the non-ideal case, for a half-scale tone input.

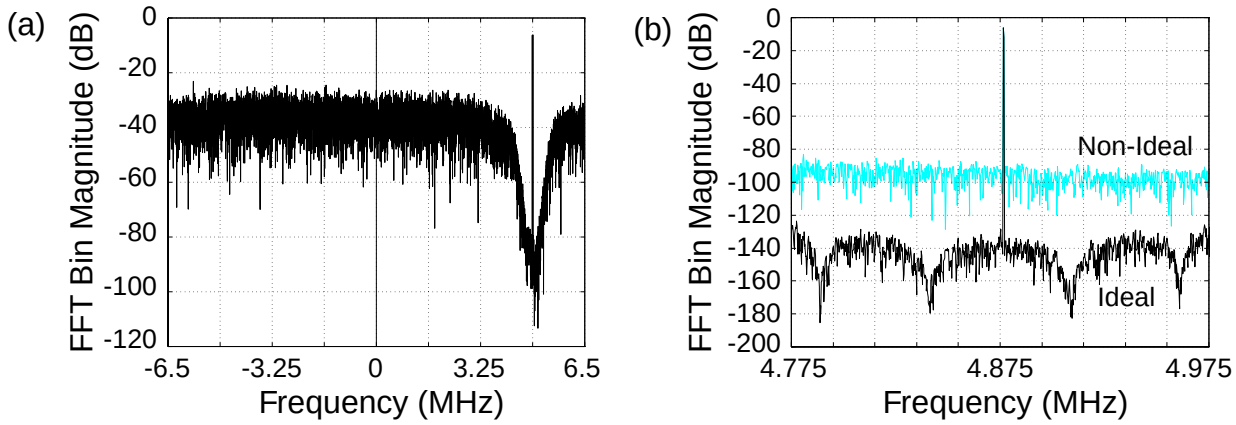


Fig. 4.1 (a) 8k-bin output spectrum of a simulated fourth-order quadrature modulator subjected to random 0.5%-peak coefficient mismatch. The input is a -6-dB complex tone. (b) In-band portion of a similar 64k-bin spectrum for a perturbed and ideal modulator. The portion shown contains 1009 bins.

A second simulation determines image-rejection performance, using in-band and image-band input tones 20-dB below full-scale. The in-band tone's frequency is just above band-center ($f = f_0 + \Delta f_1$), while the other's is slightly below the center of the image band (i.e. $f = -(f_0 - \Delta f_2)$). Fig. 4.2 shows an in-band zoom of the output spectrum for this case. As expected, the in-band tone has passed through to the modulator output, with unity gain, and appears at -20 dB in the spectrum. The image-band tone, however, also appears in the in-band portion of the output, 50-dB down from the desired tone.

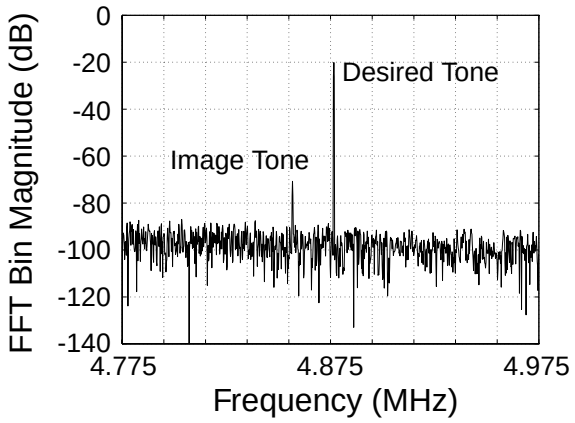


Fig. 4.2 In-band portion of a 64k-bin output spectrum for a perturbed modulator with -20-dB in-band and image inputs.

Based on the discussion in Chapter 2, it is apparent that differential mismatch is the likely culprit for the image-band tone leakage, and may also be responsible for the additional in-band noise. Simulations quickly show that pure common-mode errors do not have the drastic effects seen in these plots. Clearly, differential coefficient mismatch (and similar effects from mismatched amplifiers) creates several deleterious effects that merit further investigation.

4.2 A First-Order Complex Bandpass Filter

Rather than examining these effects by immediately delving into the modulator system (a high-order feedback structure), a simpler system is first examined in the quest for insight. This system is a one-pole complex bandpass filter, whose performance is scrutinized in the presence of differential coefficient mismatch.

As a convenient reminder of the effects of mismatch, Fig. 2.10 is re-drawn here, in a slightly new form, in Fig. 4.3. Any non-ideal complex filter can be separated into a filter seen by the input and another seen by the conjugate of the input [23]. In more intuitive terms, an output at frequency ω_x is effectively formed from two inputs: one at ω_x and another at $-\omega_x$.

4.2.1 The Ideal Single-Pole Structure

In Chapter 3, a structure like that in Fig. 4.4 was used to realize a single complex pole in the z-plane. The reason the filter acts as a complex one can be seen by analyzing the system as a two-input, two-output, linear system, and then interpreting the input and output as being complex. For the ideal case, $d_1 = d_2 = d$ and $c_1 = c_2 = c$.

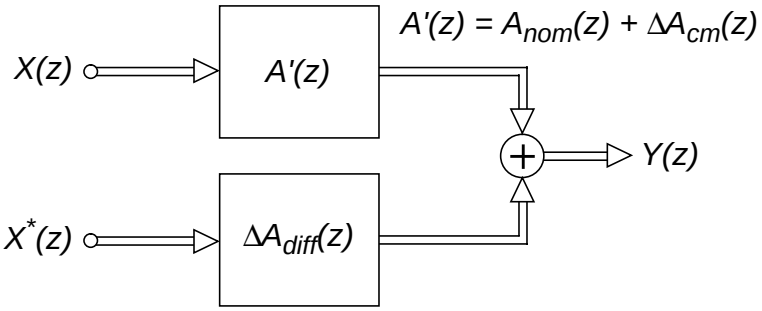


Fig. 4.3 Signal flow diagram of a complex filter, $A(z)$, showing common-mode and differential error components.

The dependence of the two outputs on each of the two inputs is (dropping the dependence of Y and X on z, for clarity):

$$Y_R = \frac{X_R(z-1-d) - cX_I}{(z-1-d)^2 + c^2} \tag{4.37}$$

and

$$Y_I = \frac{X_I(z-1-d) + cX_R}{(z-1-d)^2 + c^2}. \tag{4.38}$$

Forming the complex output as $Y = Y_R + jY_I$ gives

$$Y = Y_R + jY_I = \frac{[X_R(z-1-d) - cX_I] + j[X_I(z-1-d) + cX_R]}{(z-1-d)^2 + c^2}. \tag{4.39}$$

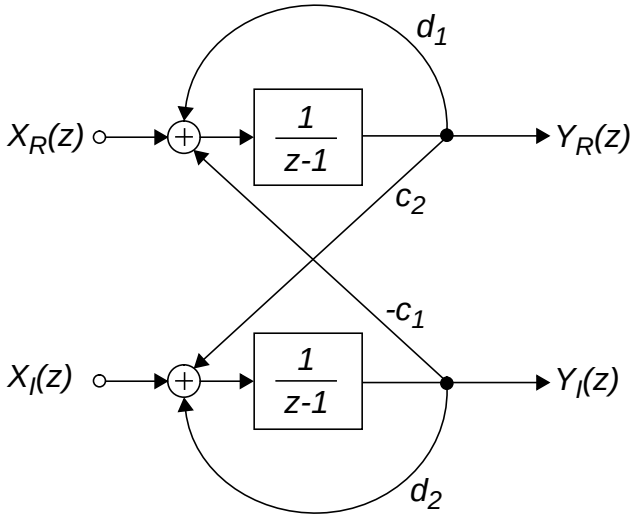


Fig. 4.4 Single-pole complex-filter realization.

To find the transfer function to the output from the complex input, $X = X_R + jX_I$, that term is factored out on the right-hand side, giving

$$Y_R + jY_I = (X_R + jX_I)\left\{\frac{z - 1 - d + jc}{(z - 1 - d)^2 + c^2}\right\}. \tag{4.40}$$

The denominator is the difference of squares,

$$(z - 1 - d)^2 + c^2 = (z - 1 - d)^2 - (jc)^2 = (z - 1 - d - jc)(z - 1 - d + jc), \tag{4.41}$$

so the singularity in the numerator cancels with one in the denominator. The equation thus simplifies to the desired result — a single complex pole:

$$\frac{Y}{X} = \frac{Y_R + jY_I}{X_R + jX_I} = \frac{1}{z - 1 - d - jc}. \tag{4.42}$$

This exercise gives an important insight into physically realized complex filters: the cross-coupled system realizes a complex-conjugate pair of poles, but the effect of one of them is nulled by a single zero. In the presence of mismatch, the nulling is not perfect, and the effects described in Chapter 2 arise.

4.2.2 An Ideal Complex Bandpass Filter

A simple context under which to investigate the mismatch phenomenon, is a complex bandpass filter that has a single pole of magnitude 0.9 at an angular frequency of 3π/4. This is essentially a complex integrator whose pole has been pulled off of the unit circle, for clarity of illustration. The filter is realized with the structure of Fig. 4.4, using nominal coefficient values of $d = -1 - 0.9/\sqrt{2}$ and $c = 0.9/\sqrt{2}$, which gives it the transfer function

$$A(z) = \frac{1}{z - 1 - d - jc} = \frac{1}{z + \frac{0.9}{\sqrt{2}} - \frac{0.9j}{\sqrt{2}}}. \tag{4.43}$$

It has the pole-zero constellation shown in Fig. 4.5(a) and the magnitude response shown in Fig. 4.5(b). Note that the signal response is asymmetric about dc (i.e. it is complex). The pole and zero that perfectly cancel one another are shown in grey in the pole-zero plot.

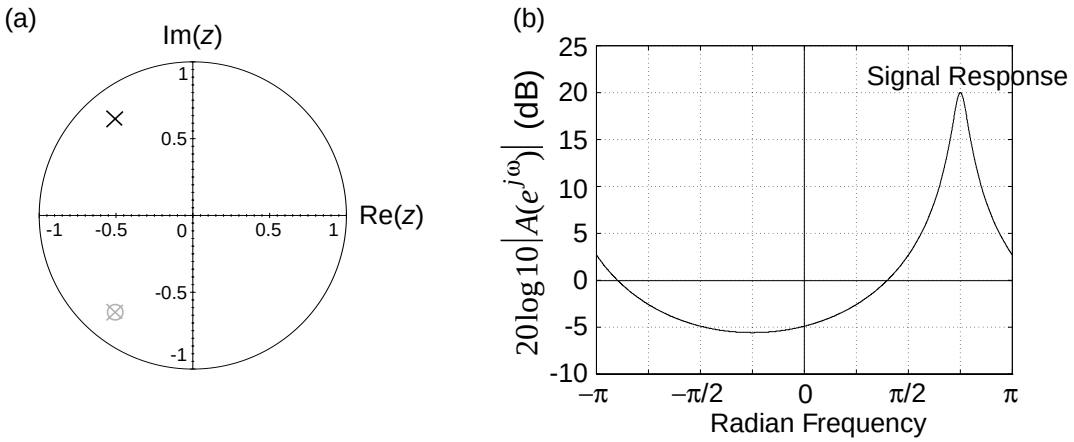


Fig. 4.5 Single-pole complex bandpass filter. (a) Pole-zero plot. (b) Magnitude response.

4.2.3 The Mismatched Bandpass Filter

I. The Image Transfer Function

The minor effects of common-mode errors are similar to the effects of coefficient mismatch in real filters, and are ignored in this example. Differential error is more interesting, since the transfer function $\Delta A_{diff}(z)$ defines a response from the conjugate, or image, input to the output. The image transfer function defines how much energy will appear in the output at a frequency ω_x, when the input is actually in the image band at frequency -ω_x, or

$$\Delta A_{diff}(e^{j\omega}) = \frac{Y(e^{j\omega})}{X(e^{-j\omega})}. \tag{4.44}$$

Perturbing the ideal coefficients in a symmetric fashion about their nominal values (i.e. differentially), gives the non-ideal coefficients the values $d_1 = d(1 + \Delta e_d)$, $d_2 = d(1 - \Delta e_d)$, $c_1 = c(1 + \Delta e_c)$ and $c_2 = c(1 - \Delta e_c)$. The terms Δe_d and Δe_c define the percentage error.

From Eq. (2.21), the differential-error transfer function is calculated:

$$\Delta A_{diff}(z) = \frac{d\Delta e_d + jc\Delta e_c}{(z - 1 - d - jc)(z - 1 - d + jc) - d^2\Delta e_d^2 - c^2\Delta e_c^2}. \tag{4.45}$$

The Δe_d^2 and Δe_c^2 terms are extremely small for even relatively large error percentages, and can be ignored. Thus, $\Delta A_{diff}(z)$ has the same pole as the complex filter, at $z = 1 + d - jc$, but also

has the conjugate pole at $z = 1 + d + jc$. Note that the gain of the function (i.e. the numerator) is directly related to the error terms.

For example, with $\Delta e_d = \Delta e_c = 0.1\,\%$ — i.e. the real-channel coefficients are 0.1% above nominal and the imaginary-channel ones are 0.1% below nominal — the transfer function becomes

$$\Delta A_{diff}(z) = \frac{-0.001(1.636 - 0.6364\,j)}{\left(z + \frac{0.9}{\sqrt{2}} - \frac{0.9\,j}{\sqrt{2}}\right)\left(z + \frac{0.9}{\sqrt{2}} + \frac{0.9\,j}{\sqrt{2}}\right) - 3.1 \cdot 10^{-6}}, \tag{4.46}$$

which has the pole-zero plot shown in Fig. 4.6(a).

The ideal signal response and the image response are shown in Fig. 4.6(b), as produced from full Simulink simulations. The image-response plot matches closely with Eq. (4.46), confirming the latter's validity; it has a gain of -37.7 dB at band-center (an angular frequency of $3\pi/4$).

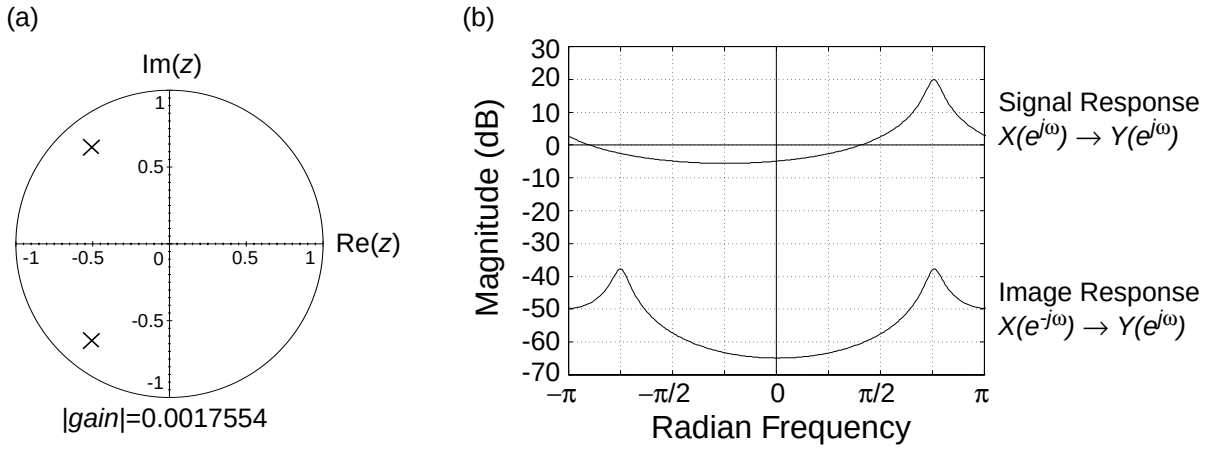


Fig. 4.6 Magnitude of the signal response and the image response for a non-ideal single-pole complex filter.

II. Image Rejection

The *image rejection* defines how effectively this complex filter passes in-band inputs while rejecting image-band inputs. At a frequency, ω, it is the ratio of the gain seen by an in-band signal to that seen by an image-band signal, or

$$IMR = 20\log 10\left\{\frac{\left|A(e^{j\omega})\right|}{\left|\Delta A_{diff}(e^{j\omega})\right|}\right\}. \tag{4.47}$$

For the example, using Eqs. (4.43) and (4.45), the image rejection at the center frequency, $\omega = 3\pi/4$, is

$$IMR \approx 20\log 10\left\{\frac{\left|e^{j\omega_0} - 1 - d + jc\right|}{\left|d\Delta e_d + jc\Delta e_c\right|}\right\} = 20\log 10\left\{\frac{\frac{1}{\sqrt{2}}\left|-1 + j + 0.9 + 0.9j\right|}{\left|-0.001(1.636 - 0.6364j)\right|}\right\} \tag{4.48}$$

$$= 57.7 \text{ dB},$$

which is apparent from Fig. 4.6(b). Of this value, 55.1 dB is due to the component mismatch vector in the denominator, while the remaining 2.6 dB is due to the numerator singularity that lies across the real axis from the in-band region. The example reaffirms image rejection's dependence on component matching, with 0.1% matching giving on the order of 60-dB image rejection.

Although the calculation of $\Delta A_{diff}(z)$ was fairly straightforward for the first-order complex filter, this is not generally true. Thus, simulated image-response curves, like those in Fig. 4.6(b), will be relied upon for more involved systems.

4.3 Mismatch in a Quadrature ΔΣ Modulator

The previous example substantiated the fact that coefficient errors create image transfer functions, and at the same time it introduced signal- and image-response plots. Now, the fourth-order quadrature ΔΣ modulator (actually, its linear model) can be competently investigated.

Section 2.1.2 showed a ΔΣ modulator modeled as a two-input, single-output, linear system. Modifying Fig. 2.3 to account for complex signal paths, and adding the extra image paths created by mismatch, results in the system of Fig. 4.7.

4.3.1 The Four Modulator Transfer Functions

The new modulator model has four complex input-output transfer functions, rather than the ideal two. The STF determines the gain from the signal input to the modulator output. With mismatch, it is slightly perturbed from its ideal value, and so is labelled as $G'(z)$ rather than $G(z)$:

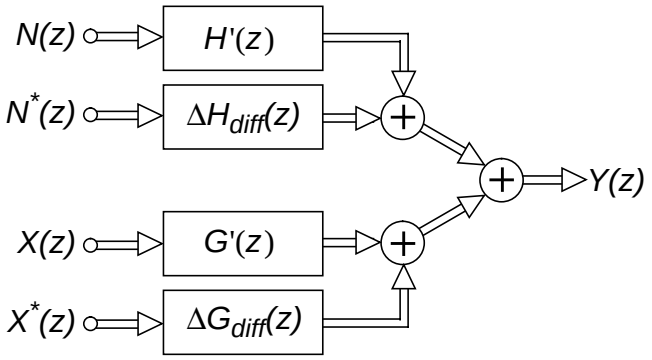


Fig. 4.7 The linear model of a quadrature ΔΣ modulator showing the four transfer functions that exist in the presence of mismatch.

$$G'(e^{j\omega}) = \frac{Y(e^{j\omega})}{X(e^{j\omega})}. \tag{4.49}$$

Similarly, the NTF determines the gain from the quantization-noise "input" to the modulator output:

$$H'(e^{j\omega}) = \frac{Y(e^{j\omega})}{N(e^{j\omega})}. \tag{4.50}$$

The first of the two transfer functions caused by differential mismatch is the *image* signal transfer function, or ISTF, which determines the gain from the image-signal input to the output:

$$G_{diff}(e^{j\omega}) = \frac{Y(e^{j\omega})}{X(e^{-j\omega})}. \tag{4.51}$$

The last is the *image* noise transfer function, or INTF, which determines the gain from the image quantization-noise "input" to the modulator output:

$$H_{diff}(e^{j\omega}) = \frac{Y(e^{j\omega})}{N(e^{-j\omega})}. \tag{4.52}$$

4.3.2 The Noise Responses

Fig. 4.8 shows a white input-noise spectrum along with the modulator's NTF, INTF, and output spectrum, with perturbed coefficients identical to those used in Section 4.1. These plots reveal the mechanism responsible for creating the in-band noise portions of the output spectrum. Fig. 4.8(a) shows the input, Fig. 4.8(b) shows the transfer functions, and Fig. 4.8(d) shows the resulting output.

The in-band noise in (a) is shaped by the deep in-band notches of the NTF in (b), which are clearly seen in the in-band zoom in (c); this operation ideally results in the deep in-band shaped noise shown (in black) in (e). Unfortunately, image-band noise from (a) is shaped by the INTF in (b), which lies about 40-dB above the ideal NTF. That means that large amounts of out-of-band quantization noise in the $\Delta\Sigma$ modulator flood into the in-band region. The resulting noise-floor is seen in (d), with the in-band zoom in (e).

Clearly, the INTF, created by differential mismatch, plays a critical role in the SNR performance of the non-ideal modulator.[1]

4.3.3 The Signal Responses

Fig. 4.9 shows the modulator's signal input spectrum, STF, ISTF, and output spectrum (using the same coefficient mismatch as above). These plots reveal the mechanism responsible for creating the signal portions of the output spectrum.

The -20-dB in-band signal in (a) is shaped by the STF in (b), which has unity in-band gain. This combination results in the -20-dB signal seen in (c). The -20-dB image-band tone in (a) is shaped by the in-band ISTF in (b), which lies approximately 50-dB below the ideal STF. Thus, the image tone appears at about -70 dB in the in-band output spectrum of (c) and (d), or about 50-dB below the desired signal. The image rejection is thus 50 dB, in-band.

Clearly, the ISTF, created by differential mismatch, plays a critical role in the image-rejection performance of the non-ideal modulator.

---

1. The effects of mismatch on the NTF are also shown in (c). The perturbed NTF, labelled as NTF', is not too different from the ideal in-band NTF; the effects of both are swamped out by those of the INTF, regardless.

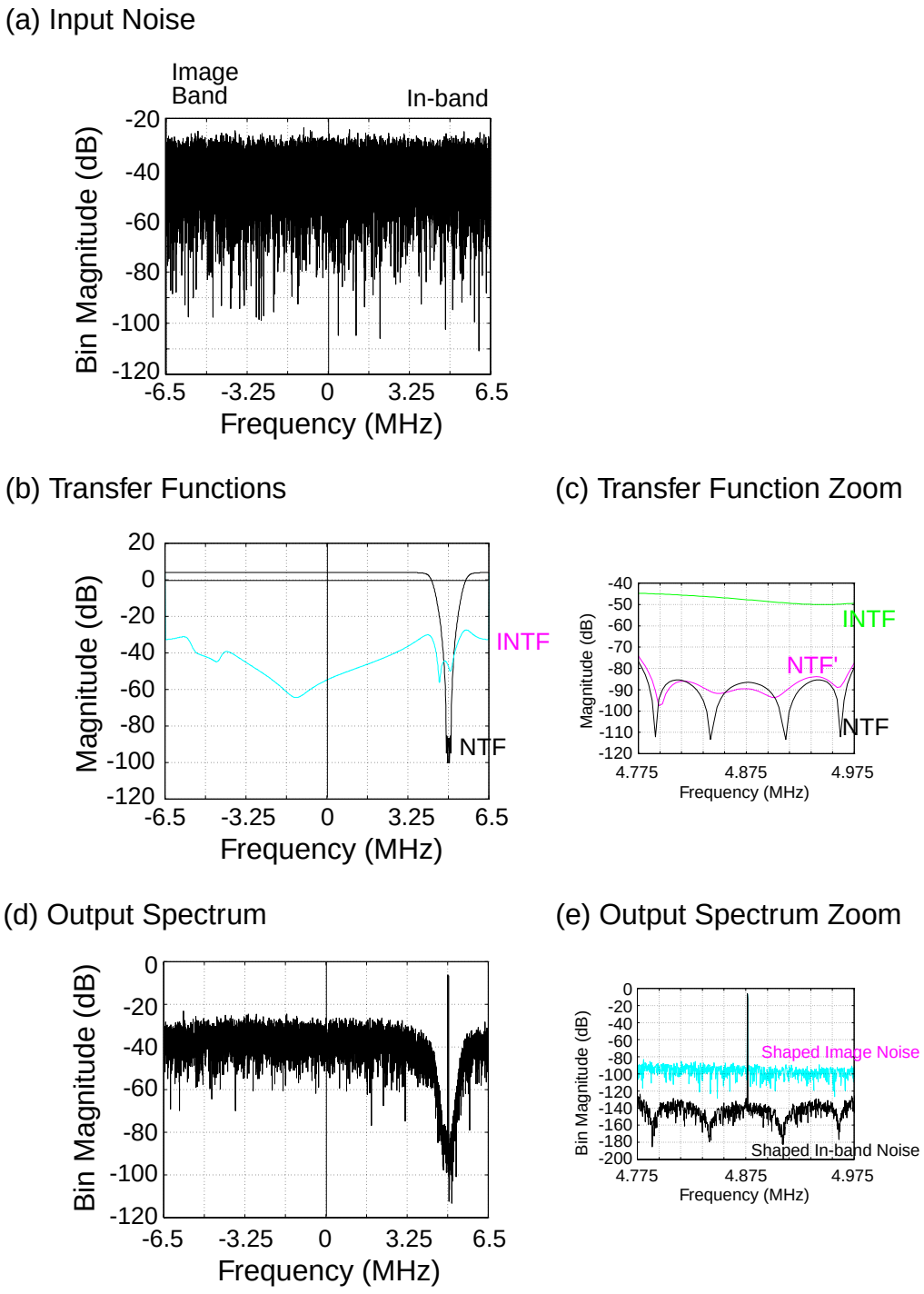
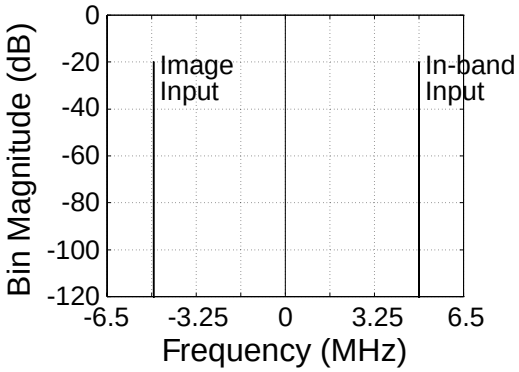
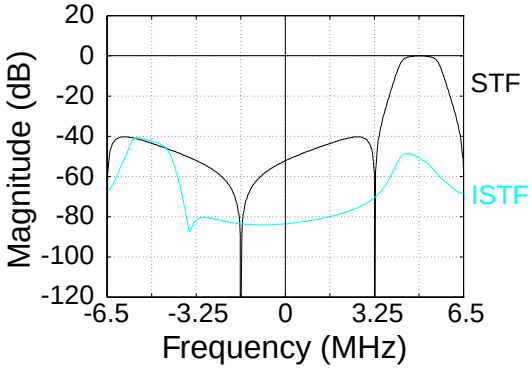


Fig. 4.8 The function of the NTF and the INTF in forming the noise spectrum.

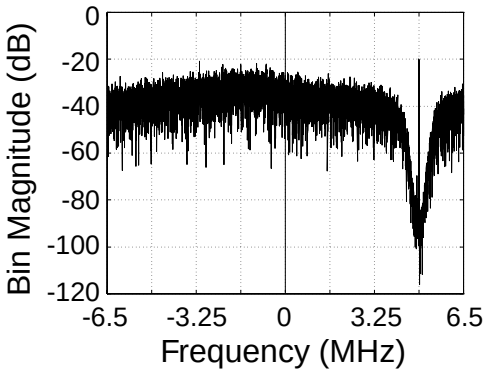
(a) Input Signals



(b) Transfer Functions



(c) Output Spectrum



(d) Output Spectrum Zoom

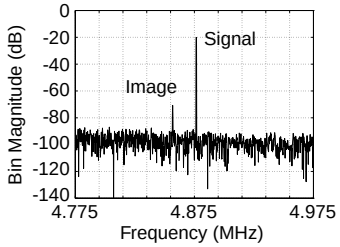


Fig. 4.9 The function of the STF and the ISTF in passing an in-band tone and an image-band tone to the in-band portion of the output spectrum.

4.3.4 Clusters of Random Transfer Functions

I. Random NTFs and INTFs

The previous NTF and INTF plots showed only a sample case of coefficient mismatch. Observing a large group of perturbed modulators, instead, gives a sense of the "average" modulator. In-band transfer functions for 100 modulators, with random 0.5%-peak coefficient mismatch, are shown in Fig. 4.10. The INTF curves lie substantially above the NTF curves, and thus are the dominant path through which noise enters the in-band region.

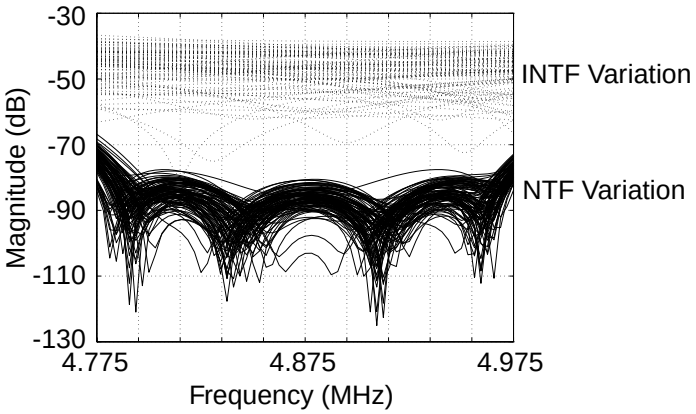


Fig. 4.10 NTF and INTF variations for 100 modulators with random 0.5%-peak coefficient mismatch.

To distill a single number from each individual curve in the figure, each curve's rms gain is calculated. This gain is the equivalent level of a flat line which could replace the associated curve in the figure. By comparing that value to the rms gain of the ideal NTF, the SNR degradation for that sample modulator is known. Fig. 4.11(a) shows this measure of degradation as caused by variation in the NTFs, while Fig. 4.11(b) shows the degradation as caused by variation in the INTFs. An X marks the 95th-percentile in each plot.

95% of the modulators encounter less than 5-dB SNR reduction due to variations in the in-band NTF, acting alone. The same proportion of modulators encounter less than 46-dB SNR reduction from the INTFs. A 46-dB SNR reduction due to aliased image-band noise is a huge amount, that swamps any reduction due to perturbation of the NTFs.[1]

1. The single modulator sample discussed in Section 4.1 had a SNR reduction of 43 dB, which falls within the expected range.

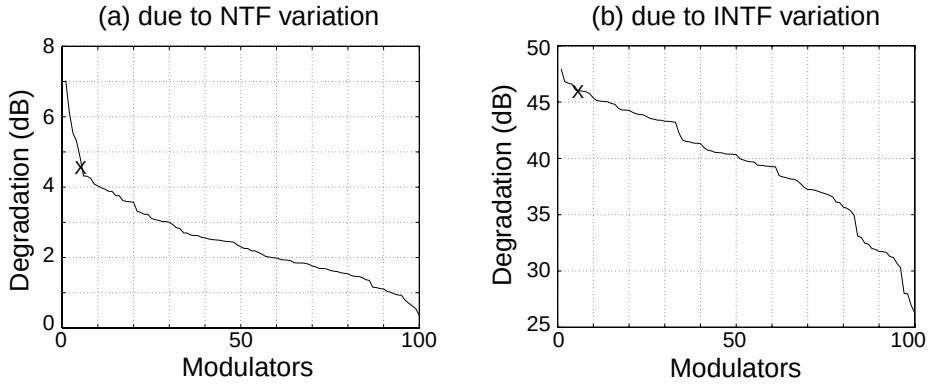


Fig. 4.11 Reduction of in-band rms noise attenuation due to coefficient variation in 100 modulators. (a) Degradation caused by non-optimal NTFs allowing excess in-band noise. (b) Degradation caused by non-ideal INTFs.

II. Random STFs and ISTFs

Similar STF and ISTF curves for 100 non-ideal modulators are presented in Fig. 4.12. Comparing the rms gain of the perturbed STFs against the ideal STF provides a measure of STF degradation. Fig. 4.13(a) shows that the in-band variation of the STF is limited to within about ± 0.5 dB, and that 95% of modulators lie within 0.36 dB.

Comparing the ISTFs to the ideal STF provides a measure of image rejection. As seen in Fig. 4.13(b), 95% of the modulators attain greater than 44.3-dB IMR. The simulated case in Section 4.1 showed 50-dB IMR, which falls within the expected range for 0.5% mismatch.

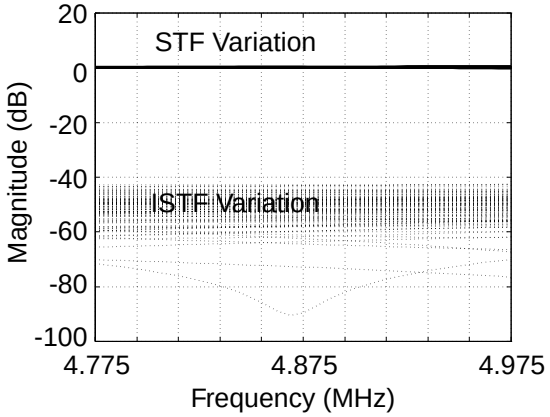


Fig. 4.12 STF and ISTF variations for 100 modulators with random 0.5%-peak coefficient mismatch.

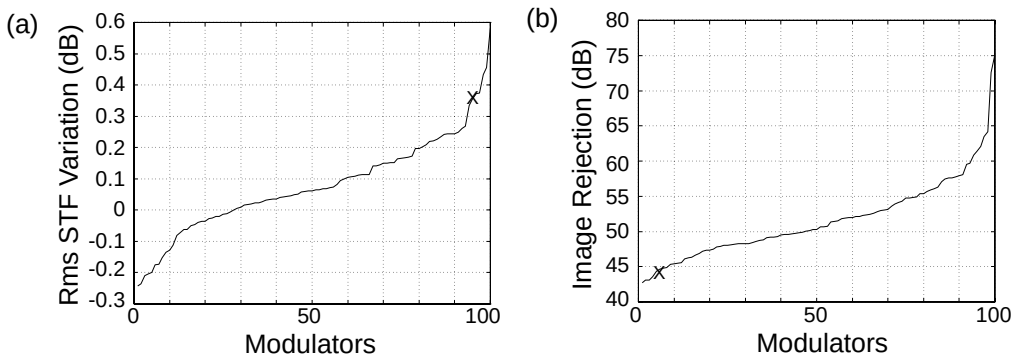


Fig. 4.13 Variation of (a) in-band rms STF gain and (b) image rejection, due to coefficient variation in 100 modulators.

4.3.5 SNR and IMR Histograms

The above curves are useful for determining the effects of mismatch, and ultimately prove useful in combatting those effects, but are based upon the linear model of the modulator. Full simulations of 1000 perturbed modulators, with random 0.5%-peak coefficient mismatch and half-scale tone inputs, result in the SNR histogram of Fig. 4.14(a). 95% of the perturbed modulators achieve SNR greater than 53 dB, which represents a degradation of 50 dB from the ideal — matching well with the linear model results from Section 4.3.4.

The IMR histogram is shown in Fig. 4.14(b). The in-band and image-band inputs both lie 20-dB below full-scale. 95% of the perturbed modulators achieve greater than 44-dB IMR — which, again, matches well with the results from the linear model.

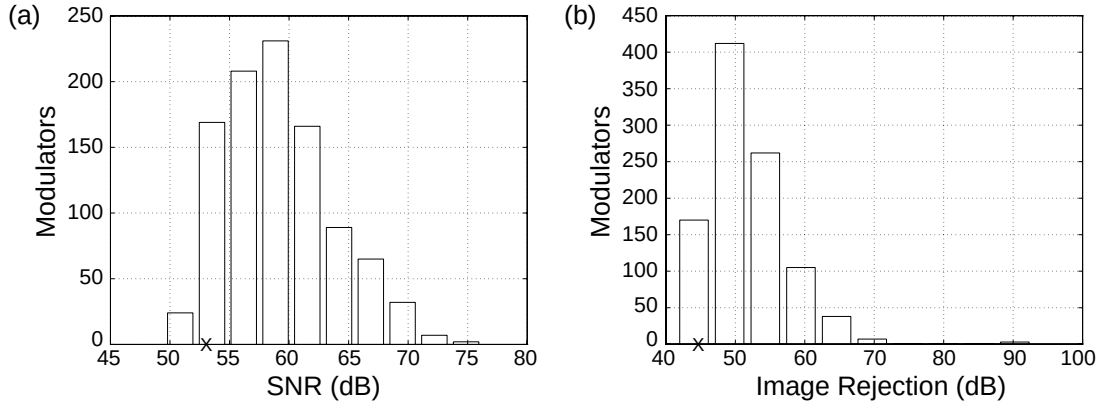


Fig. 4.14 Histograms for (a) SNR and (b) IMR for the modulator with random 0.5%-peak coefficient mismatch (1000 modulators).

4.4 The Real-Versus-Quadrature ΔΣ Comparison Revisited

The quadrature modulator appears to be quite sensitive to coefficient and amplifier mismatch: SNR drops from the ideal 103 dB to a 53-dB 95th-percentile, while IMR drops from the infinite ideal to a 44-dB 95th-percentile (both for 1000 samples with 0.5% mismatch). The many advantages of quadrature modulators trumpeted in Chapter 3 seem in jeopardy.

To make a fair comparison, similar techniques are used to evaluate the pair of bandpass ΔΣ modulators acting upon complex inputs in the presence of mismatch. Histograms, presented in Fig. 4.15, show a 95th-percentile for SNR at 51.2 dB, and a 95th-percentile for IMR at 27.4 dB.

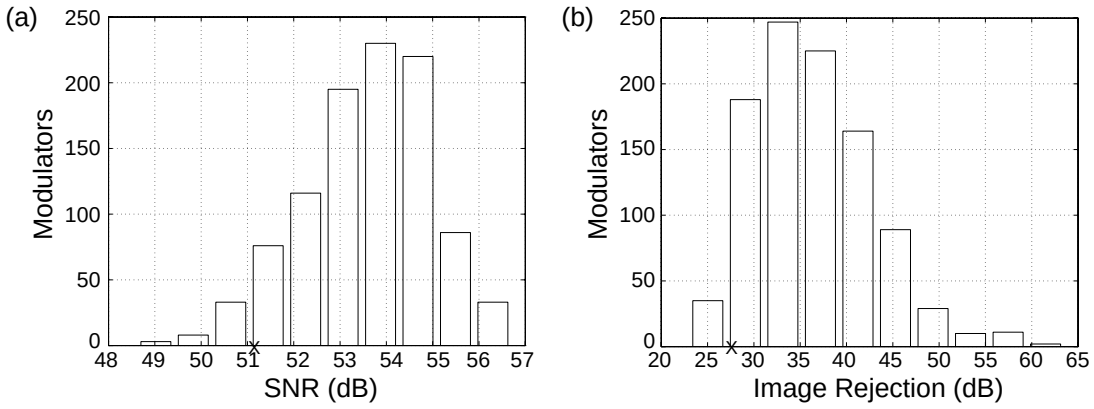


Fig. 4.15 Histograms for (a) SNR and (b) IMR for a pair of real bandpass ΔΣ modulators with random 0.5%-peak coefficient mismatch (1000 modulators).

The quadrature modulator still provides superior SNR performance compared to the pair of real modulators — a 95th-percentile of 53 dB compared to 51 dB — although it has far less of an advantage than it had in the ideal case.[1] Its IMR performance is superior, too, with a 95th-percentile of 44 dB compared to 27 dB. The strong cross-coupling within the single complex modulator proves helpful for IMR performance, maintaining more symmetry within transfer functions than is possible in a system of uncoupled real modulators.

The performance differential becomes more substantial as an ideal realization is approached. Table 4.1 compares quadrature-modulator performance with that of a real-modulator pair, for three levels of coefficient accuracy. Amplifier performance remains at 50 to 60 dB, with 2-dB matching between a stage's two amplifiers.

1. The advantage is reduced to the point where it may no longer be beneficial to use quadrature modulators to convert real input signals, as was proposed in Section 3.3.3.

With more accurate coefficient matching — or higher-gain (or more-closely matched) amplifiers — the quadrature modulator sees less performance degradation due to aliased in-band noise, and thus more nearly reaches its deep (four-zero) in-band NTF. On the other hand, the pair of real modulators is ultimately limited to the lesser in-band noise shaping of its two-zero NTF. At the 0.1%-matching level, the quadrature modulator is superior by about 13-dB (2-bits) SNR and 16-dB IMR.

Table 4.1: Performance Comparison for Three Degrees of Mismatch[a]

Matching Accuracy	Real-Modulator Pair		Quadrature Modulator	
	SNR	IMR	SNR	IMR
0.5%	51 dB	27 dB	53 dB	44 dB
0.3%	53 dB	32 dB	57 dB	49 dB
0.1%	54 dB	42 dB	67 dB	58 dB

a. Numbers listed are 95th-percentiles (1000 samples).

4.5 Summary

The effects of mismatch in quadrature systems were uncovered with the investigation of a simple complex bandpass filter. These results were applied to the quadrature modulator's linear model, and explained the drastic performance drop seen when modulator simulations included non-ideal effects such as coefficient mismatch and amplifier mismatch and finite dc gain.

The fourth-order quadrature modulator was shown to be quite sensitive to these non-ideal effects. Modulators facing random 0.5%-peak mismatch and amplifier dc gain between 50 and 60 dB, tended to lose more than 50-dB SNR compared to their ideal SNR, and dropped to approximately 45-dB IMR. The large SNR reduction was shown to be caused by image noise aliasing into the in-band region by way of the INTF, with the large amounts of out-of-band noise in a $\Delta\Sigma$ modulator making this aliasing phenomenon a problem.

The quadrature modulator still out-performs a pair of real modulators also subjected to mismatch, though the performance advantage is substantially lower than in the ideal case. The performance gap widens as matching accuracy improves.

CHAPTER 5

An Improved Quadrature Modulator

This chapter describes an improved modulator that possesses a notch in the image band of its NTF, which dramatically reduces the deleterious effects of non-idealities [61 Jantzi]. The design procedure for such a modulator is described, and the various allowable trade-offs discussed. The improved modulator is again compared for SNR performance against the pair of standard bandpass modulators, this time easily maintaining its distinct advantages in the face of mismatch.

5.1 Designing the Improved Modulator

5.1.1 An Image-Band Notch

Chapter 4 described the mechanism whereby large amounts of image-band noise alias into the in-band region of a modulator and, thus, degrade SNR performance. If a single notch is placed in the center of the NTF image band, a first-order zero reduces the image-band noise power before it aliases to the in-band region. If implemented correctly, this technique actually positions a notch in the center of the in-band region of the *INTF,* such that it aliases the out-of-band noise with a much smaller gain than that seen in Chapter 4.

There is some freedom in the design of the improved modulator. Three zeros are placed optimally in-band, and one zero is positioned in the center of the image band. The three in-band NTF poles are placed in a butterworth configuration, and are combined with a single image-band pole in order to maintain 4-dB peak out-of-band NTF gain. Fig. 5.1 shows the pole-zero configuration for such a modulator.

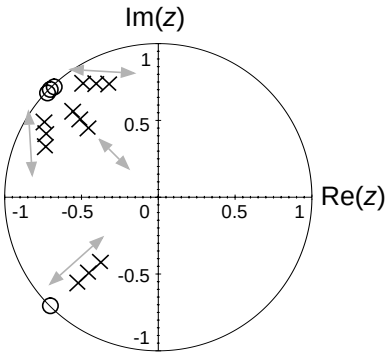


Fig. 5.1 Pole-zero constellation variations for modulators with one image-band zero.

There is a design trade-off between the depth of the in-band regions of the NTF and INTF: as the in-band poles move away from the in-band zeros, the in-band region deepens, but at the expense of the image-band depth (since the image-band pole must move closer to the image-band zero to maintain the 4-dB constraint); as the in-band poles move closer to the in-band zeros, worsening the in-band region, the image pole can move away from its zero, thus deepening the image-band region.

5.1.2 Image-Band Pole Placement and its Effects

The simplest parameter with which to describe a design of this type, is the magnitude of the image-band pole. Three designs are shown below in Fig. 5.2. The first has an image-band pole at a radius of 0.77. The second has an image-band pole at a radius of 0.6, which means that — in order to maintain the 4-dB peak out-of-band gain constraint — the in-band pole trio must move closer to the in-band zeros. The third has an image-band pole at a radius of 0.92 (closer to the unit circle), which forces the in-band poles to move away from the in-band zeros.

The position of the image-band pole controls the relative amounts of noise caused by the non-ideal NTFs and INTFs. Simulations of 100 perturbed modulators for the three designs are shown in Fig. 5.3. Below each NTF/INTF overlay, lies a graph of the rms attenuation degradation caused by each transfer function.

In the first design, the NTF and INTF curves lie nearly on top of each other. The NTF values have a 95th-percentile of 2.3 dB, whereas the INTF values have a 95th-percentile of 2.6 dB (though typical INTF curves fall well below the ideal NTF, some having rms values nearly 15-dB

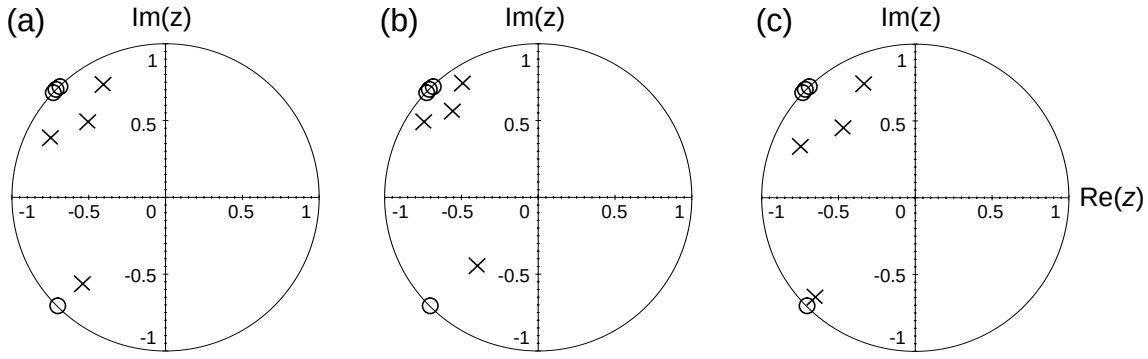


Fig. 5.2 Pole-zero constellations for modulators with one image-band zero. (a) Image-band pole radius of 0.77. (b) Image-band pole radius of 0.60. (c) Image-band pole radius of 0.92.

better). The 95th-percentile of the SNR histogram — shown at the bottom of Fig. 5.3, column (a) — is 74.1 dB.

In design (b), the INTF curves fall generally below the NTF curves. The 95th-percentile for rms degradation due to the NTFs is 2.8 dB, whereas for the INTFs it is -11.1 dB. Thus, the NTF perturbation is the main cause of in-band noise, which accounts for the tight range (about 5 dB) of SNR deviation seen in this design's histogram. The 95th-percentile of the SNR histogram is 67.3 dB, which is 7-dB worse than design (a). Thus, it is wasteful to make the image-band notch too deep (which is equivalent to making the in-band INTF too deep) since that comes at the cost of a worse in-band NTF.

In design (c), the INTF curves fall generally above the NTF curves. The 95th-percentile for rms degradation due to the NTFs is 6.4 dB, whereas for the INTFs it is 18.9 dB. Thus, the INTF perturbation is the main cause of in-band noise, accounting for the wide spread (about 21 dB) of SNR values seen in the design's histogram. The 95th-percentile for SNR is 65.8 dB, which is 8-dB worse than design (a). Thus, it is wasteful to make the in-band region too deep, since that comes at the cost of a worse in-band INTF, and aliased image-band noise will swamp out in-band noise.

Table 5.1 summarizes the results. It is clear that the first design is the best one: it has random INTFs that just begin to interfere with the random NTFs — giving the optimal trade-off between in-band NTF and INTF depth — which results in the best SNR statistics of the three designs.

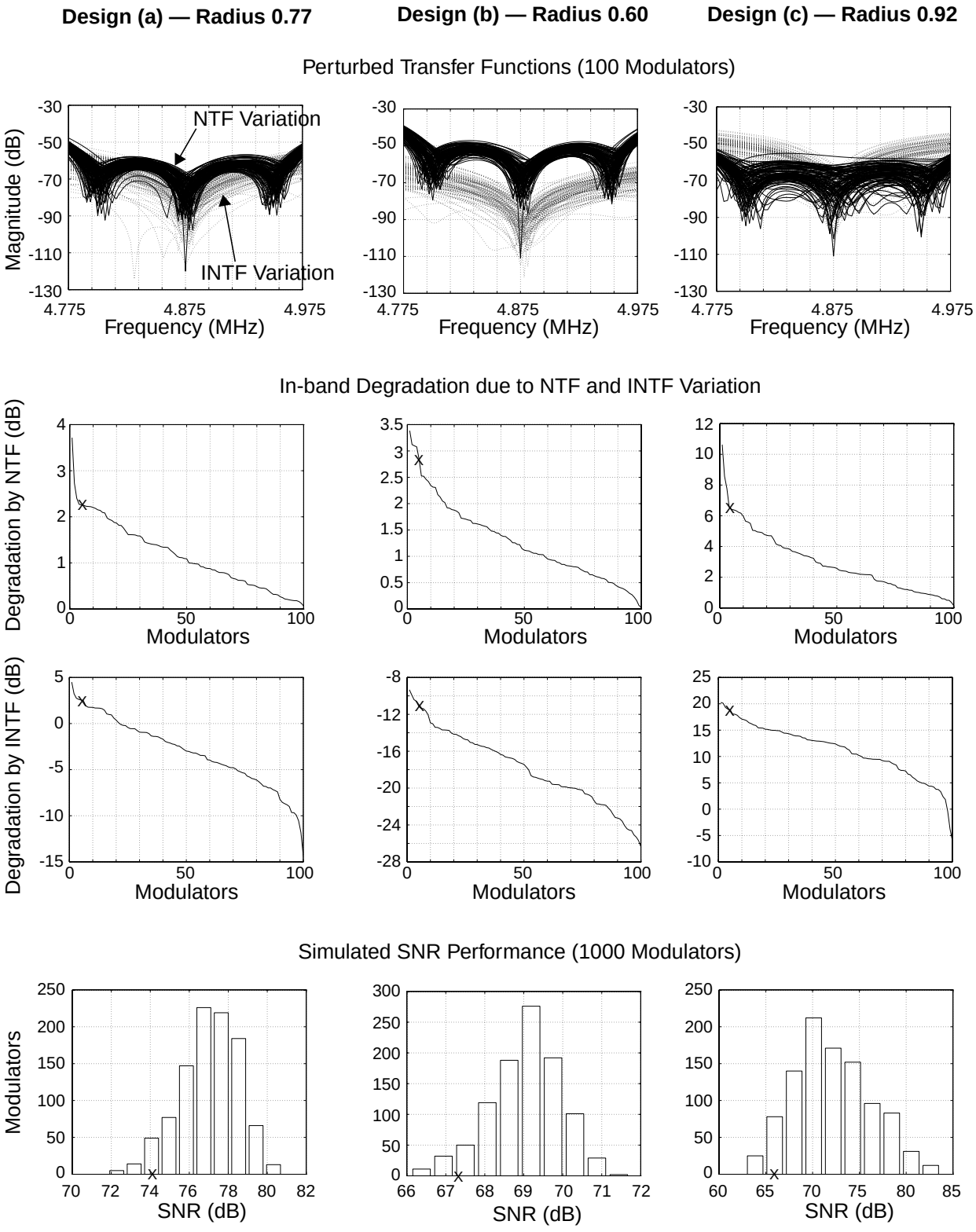


Fig. 5.3 Performance of improved designs with various image-band pole radii. (a) Radius 0.77. (b) Radius 0.60. (c) Radius 0.92.

Table 5.1: Effects of Image-Band Pole Placement

Specification	Design 1	Design 2	Design 3
image-band pole radius	0.77	0.60	0.92
NTF 95th[a]	2.3 dB	2.8 dB	6.4 dB
INTF 95th[b]	2.6 dB	-11.1 dB	18.9 dB
SNR 95th[c]	74.2 dB	67.3 dB	65.8 dB
SNR spread[d]	9 dB	5.5 dB	21 dB

a. The 95th-percentile of rms attenuation degradation due to NTF curves (100 sample modulators).

b. The 95th-percentile of rms attenuation degradation due to INTF curves (100 sample modulators).

c. The 95th-percentile of simulated SNR, for 1000 modulators.

d. The spread between lowest and highest SNR for 1000 modulators.

5.1.3 Stage Ordering

Once the transfer function is chosen, the four zeros can be realized in any of 24 different ways in the structure. The ordering of the stages is crucial to the effectiveness of the mismatch-combatting technique. If the three in-band zeros are labelled as `l`, `m`, and `u` — for the lower-, middle-, and upper-frequency zeros — and the image-band zero is labelled as `o` (for opposite), the 24 combinations are as listed Table 5.2.

The order in which the `l`, `m`, `o` and `u` labels appear, signifies in which stages the zeros are realized. For example, `lomu`, is the configuration where the low frequency in-band zero is realized in the first stage, the image-band zero in the second stage, and the middle- and upper-frequency in-band zeros in the third and fourth stages, respectively. The stage-orderings are listed by image-band zero groupings; the first six are for designs in which the first stage realizes the image-band zero, and so on.

The results show that the image-band zero should be realized in the third or fourth stage. If the image-band notch is realized in the first stage, the technique actually worsens performance compared to the original design (dropping the SNR 95th-percentile from 53 dB to 18 dB), while if the image-band notch is realized in the second stage, performance is marginally worse than in the original design. The third and fourth groupings both offer significant improvement over the original modulator. Note that there is little variation based on the order in which the in-band zeros

Table 5.2: Stage Ordering and SNR

Stage[a]	Ordering	SNR 95th (dB)	SNR Spread (dB)
1st	olmu	18.1	40.9
	olum	18.4	42.1
	omlu	17.8	38.2
	omul	18.1	42.2
	oulm	18.0	32.6
	ouml	18.1	36.9
2nd	lomu	48.0	31.2
	loum	48.1	33.8
	molu	52.7	31.8
	moul	52.1	28.6
	uolm	48.3	30.9
	uoml	47.9	32.6
3rd	ulom	74.5	9.0
	luom	74.1	8.8
	umol	73.6	10.2
	muol	73.9	9.5
	lmou	73.7	9.8
	mlou	74.0	9.5
4th	lmuo	74.0	8.8
	lumo	74.5	8.4
	mluo	74.5	9.7
	mulo	74.5	9.0
	ulmo	74.4	8.7
	umlo	74.4	9.0

a. Stage in which the image-band notch is realized.

are realized (the exception being within the grouping in which the image-band notch is realized in the second stage).

Random linear-model NTF and INTF overlays are shown in Fig. 5.4: the plots (a) through (d) correspond to the image-band notch being realized in stages one through four. Clearly, it is only

when the image-band notch is realized in the third or the fourth stage that there is a proper trade-off between the contribution to in-band noise by the NTFs and INTFs.

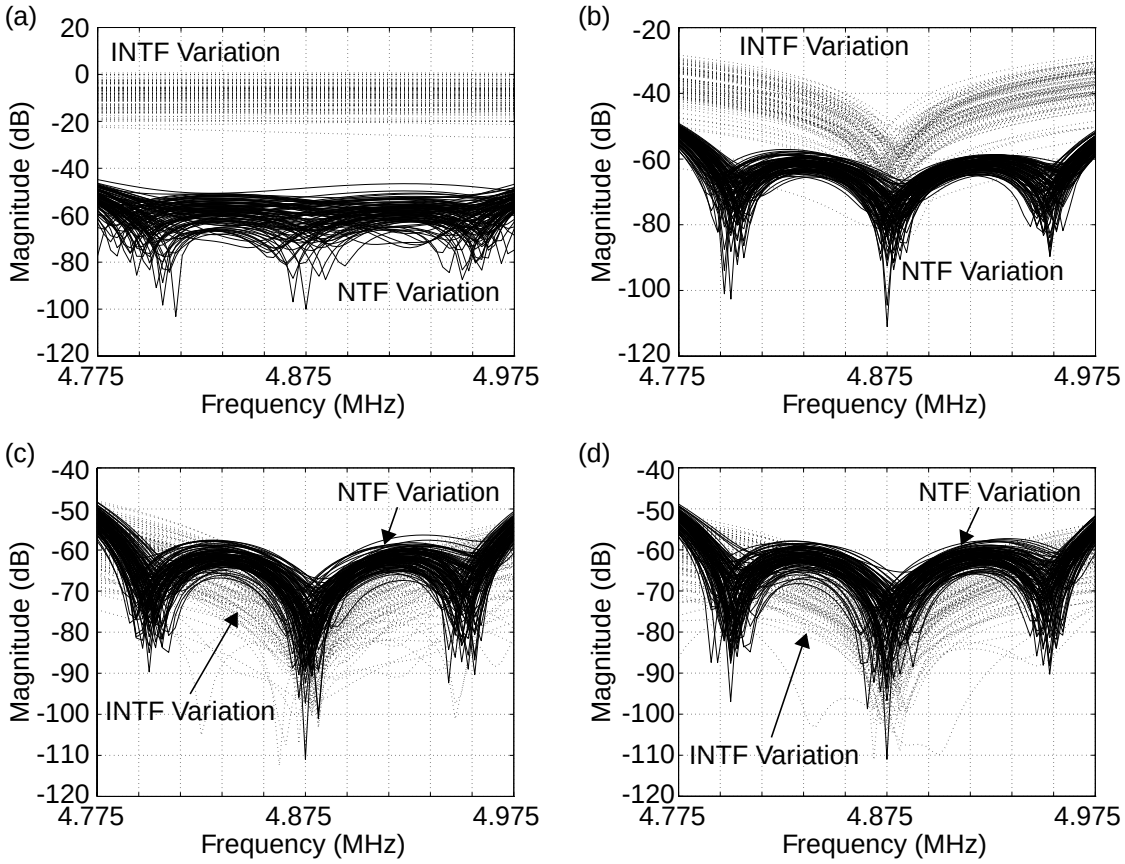


Fig. 5.4 NTF and INTF overlays for an image-band notch realized in the (a) first, (b) second, (c) third, and (d) fourth stage.

5.2 The Improved Modulator

5.2.1 The New NTF

The best of the three designs has an NTF whose pole-zero plot is shown in Fig. 5.5(a) and whose magnitude response is shown in Fig. 5.5(b), which includes an expanded view of the in-band region. The image-band pole magnitude is 0.77, shown in Section 5.1.2 to be a good choice. The image-band notch is realized in the fourth stage, with an overall ordering of `umlo` — the last entry in Table 5.2. This design will be referred to, hereafter, as the "*3/1*" modulator, due to its three in-band zeros and single image-band zero. The original design from Chapter 3 is thus named the "*4/0*" modulator. More design details are given in Appendix B.

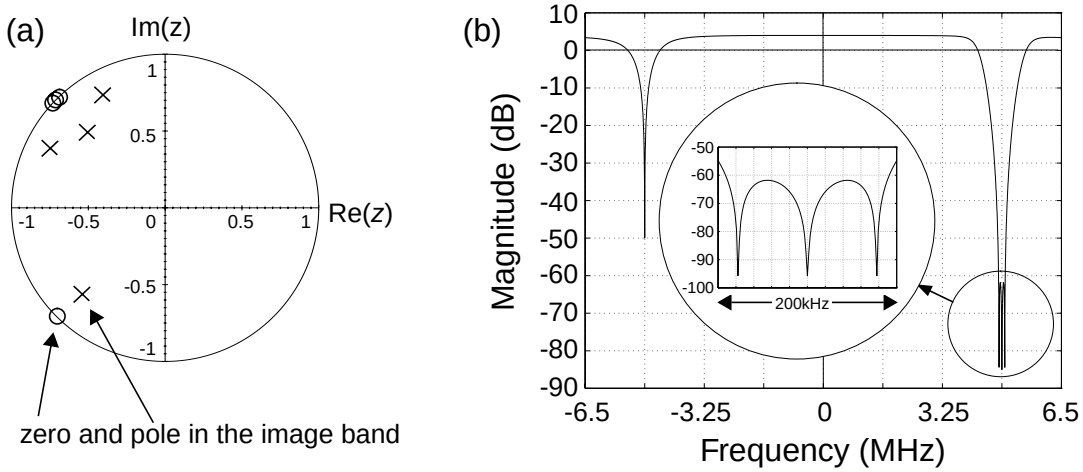


Fig. 5.5 The improved NTF. (a) Pole-zero constellation. (b) Magnitude response.

5.2.2 The New STF

The STF designed for the updated pole configuration is shown in Fig. 5.6. As seen in the pole-zero plot of Fig. 5.6(a), one STF zero is placed over the image-band pole to null its response, leaving two zeros available to effect shaping of the input spectrum. In this case, a complex bandpass filtering function is achieved by placing a zero at $z = j$ (3.25 MHz) and another at $z = -1$ (6.5 MHz).

The STF magnitude response is shown in Fig. 5.6(b). It has unity in-band gain and 30-dB out-of-band rejection. The in-band STF has magnitude flat to within 0.03 dB and phase linear to within $\pm 0.02°$.

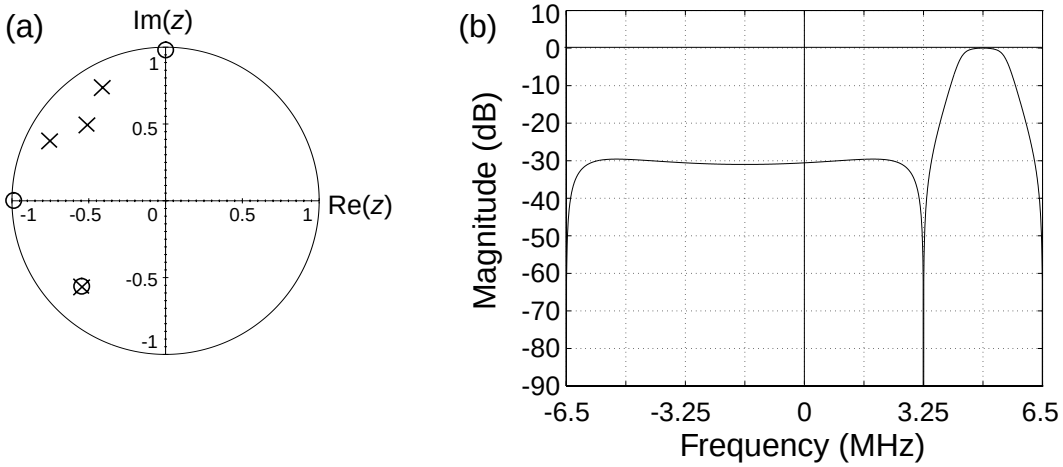


Fig. 5.6 The new STF. (a) Pole-zero constellation. (b) Magnitude response.

5.2.3 Improved-Modulator Spectra

Fig. 5.7(a) shows the 8k-bin spectrum of the fourth-order *3/1* quadrature modulator with random 0.5%-peak coefficient mismatch and moderate amplifier non-ideality. Note the deep noise shaping in-band, and the single noise-shaping notch in the image band. Note, too, that some of the in-band tone has leaked into the image band at the output. This leaked tone is removed along with the quantization noise, and thus is not important.

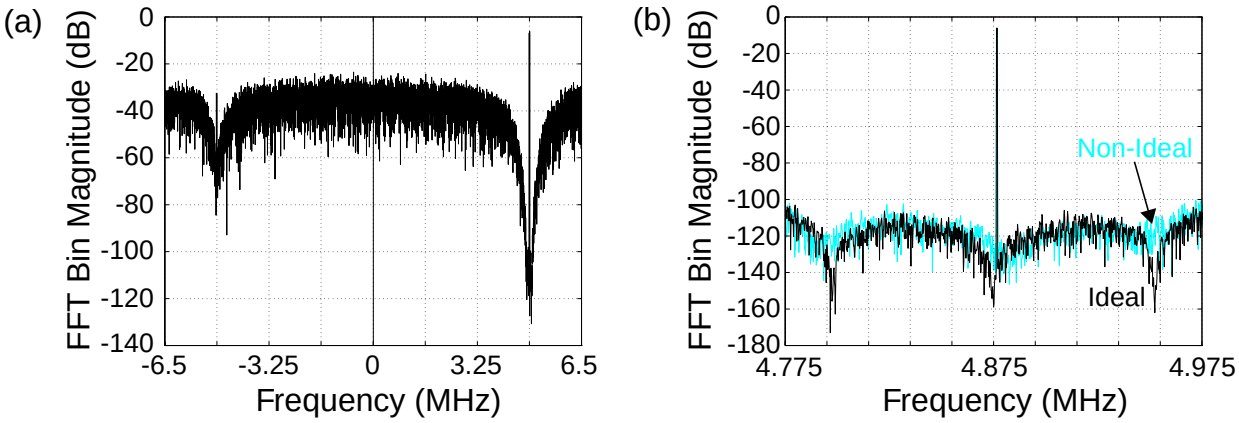


Fig. 5.7 (a) 8k-bin output spectrum of the improved fourth-order quadrature modulator subjected to random 0.5%-peak coefficient mismatch. The input is a -6-dB complex tone. (b) The in-band portion of a similar 64k-bin spectrum for a perturbed and ideal modulator. The portion shown contains 1009 bins.

The simulation shows that for a half-scale tone input, SNR decreases from nearly 81 dB in the ideal case to 79 dB in the non-ideal case — less than 2-dB degradation in SNR. The minimal perturbation of the in-band noise is clear in Fig. 5.7(b). This result is a dramatic improvement over the original *4/0* modulator, which in Chapter 4 saw a 43-dB degradation (for identical percentage perturbation of each coefficient).

Fig. 5.8 shows the in-band zoom of the output spectrum for a second simulation, run with -20-dB in-band and image-band input tones. As expected, the in-band tone has passed through to the modulator output, with unity gain, and appears at -20 dB in the spectrum. The image-band tone also appears in the in-band portion of the output, about 58-dB down from the desired tone. This 58-dB IMR represents a modest improvement over the 50 dB seen for the original *4/0* modulator.

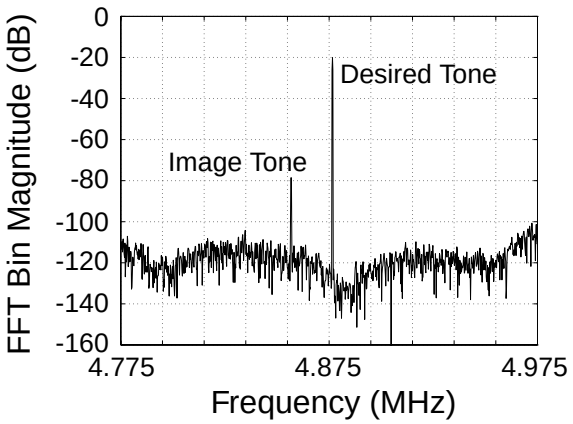


Fig. 5.8 The in-band portion of a 64k-bin output spectrum for a perturbed modulator with -20-dB in-band and image inputs.

5.2.4 Clusters of Random Transfer Functions

I. Random NTFs and INTFs

The *3/1* modulator's random NTFs and INTFs were plotted in Fig. 5.3, design (a), and are repeated below for comparison to those for the original modulator from Fig. 4.10. Fig. 5.9 shows the dramatic contrast between the two figures: whereas the INTF curves swamp out any NTF variations in the original *4/0* modulator (Fig. 5.9(a)), in the improved *3/1* modulator (Fig. 5.9(b)) the variations are of a similar order.

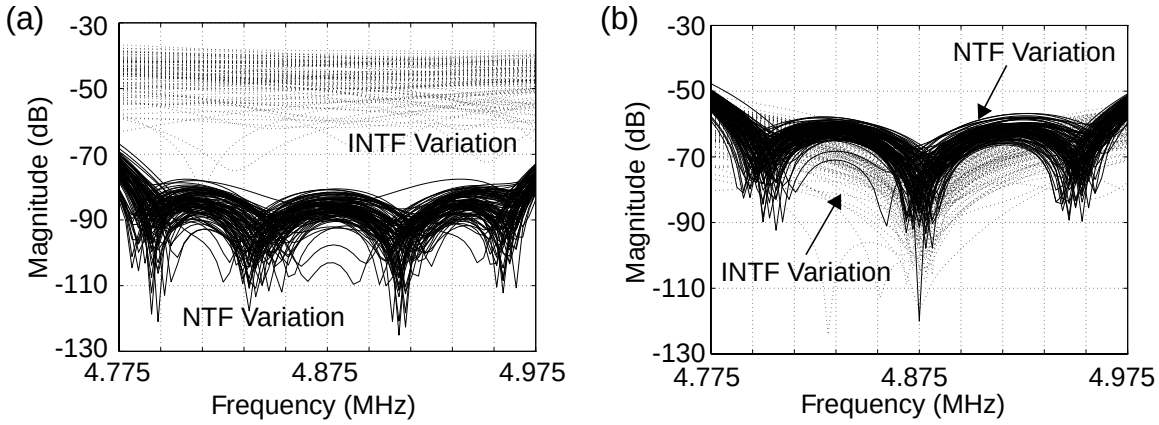


Fig. 5.9 NTF and INTF variations for 100 modulators with random 0.5%-peak coefficient mismatch. (a) Original *4/0* modulator. (b) Improved *3/1* modulator.

II. Random STFs and ISTFs

Random STFs and ISTFs for 100 perturbed *3/1* modulators are presented in Fig. 5.10. In Fig. 5.11(a), we see that the in-band variation of the STF is limited to within about ±0.4 dB, and that 95% of modulators lie within 0.28 dB. Fig. 5.11(b) shows that more than 95% of the modulators attain greater than 44.6-dB IMR. These results are very close to those for the original *4/0* modulator, presented in Fig. 4.12.

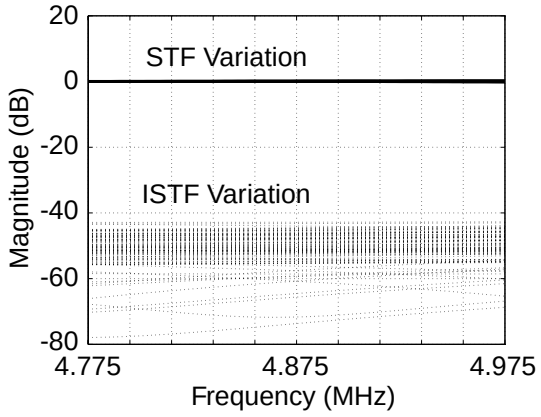


Fig. 5.10 STF and ISTF variations for 100 modulators with random 0.5%-peak coefficient mismatch.

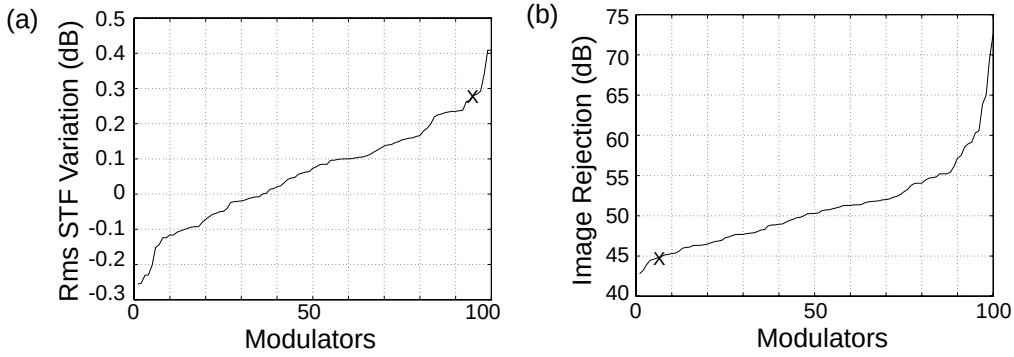


Fig. 5.11 Variation of (a) in-band rms STF gain and (b) image rejection, due to coefficient variation in 100 modulators.

5.2.5 SNR and IMR Histograms

Simulations of 1000 perturbed modified modulators, with random 0.5%-peak coefficient mismatch, moderate amplifier non-ideality, and half-scale tone inputs, result in the SNR histogram of Fig. 5.12(a). 95% of the perturbed modulators achieve greater than 74.2-dB SNR — which represents a degradation of less than 7 dB from the ideal.

The IMR histogram is shown in Fig. 5.12(b). 95% of the perturbed modulators achieve greater than 45.1-dB IMR — which matches closely with the results from the linear model.

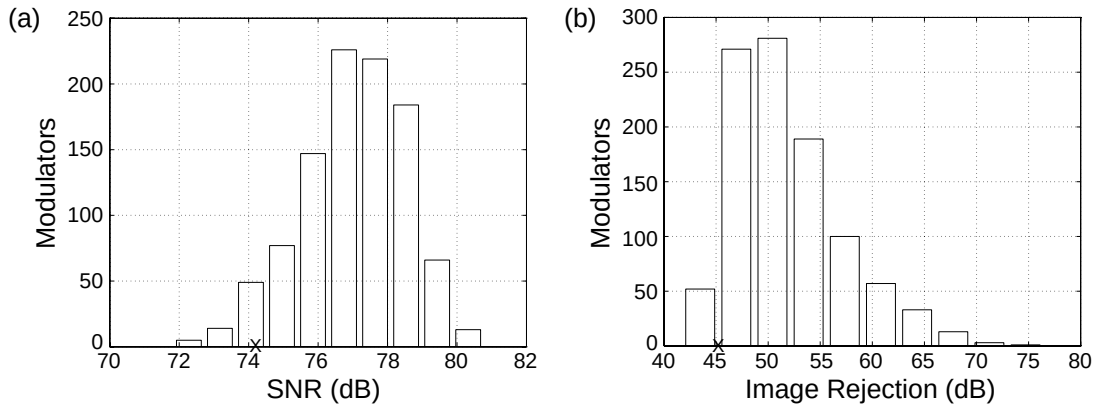


Fig. 5.12 Histograms for (a) SNR and (b) IMR for the modified modulator with random 0.5%-peak coefficient mismatch (1000 modulators).

5.3 SNR Comparison: the *3/1* Modulator Versus the *4/0* Modulator

Although in the ideal case the original *4/0* modulator had superior noise-shaping performance due to its four in-band zeros, the *3/1* modulator maintains its performance better in the face of coefficient mismatch, and proves superior. When properly implemented, the image-band-notch technique actually buys about 21-dB SNR for the examples chosen, or more than 3 bits.

Image rejection remains relatively unaffected by the technique, which is not surprising since we have not really changed the ISTF curves (as witnessed by comparing Fig. 5.10 with the earlier Fig. 4.12).

The statistical comparison is shown pictorially in Fig. 5.13, and summarized in Table 5.3.

Table 5.3: Simulated Modulator Performance with Mismatch

Specification	Initial Modulator (*4/0*)	Modified Modulator (*3/1*)
Ideal SNR	103 dB	81 dB
SNR (95th-percentile)	53 dB	74 dB
IMR (95th-percentile)	44 dB	45 dB

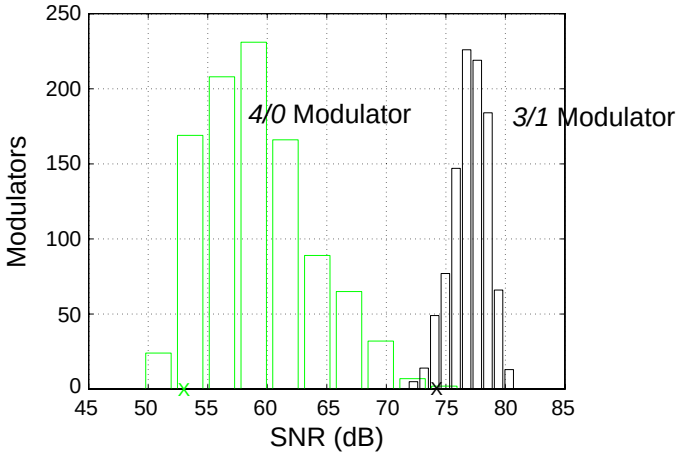


Fig. 5.13 SNR histogram comparison for modulators *3/1* (black) and *4/0* (grey).

5.4 The Real-Versus-Quadrature ΔΣ Comparison with the *3/1* Modulator

The *3/1* quadrature modulator appears quite robust in the face of coefficient and amplifier mismatch: SNR drops from an ideal 81 dB to a 74-dB 95th-percentile, while IMR drops from the infinite ideal to a 45-dB 95th-percentile (both for 1000 samples with 0.5% mismatch). To compare this modulator with the pair of bandpass ΔΣ modulators (in the presence of component mismatch), the simulations for the bandpass modulator pair are taken from the end of Chapter 4 and plotted together, in Fig. 5.14, with the simulations for the 3/1 modulator.

The improved *3/1* quadrature modulator provides superior SNR performance compared to the pair of real modulators: a 95th-percentile of 74 dB compared to 51 dB, or a 23-dB performance

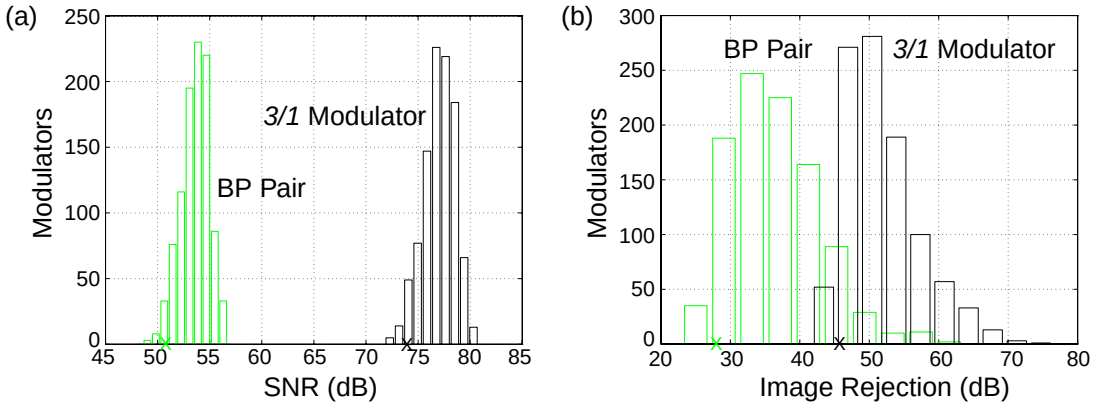


Fig. 5.14 (a) SNR and (b) IMR histogram comparison for modulator *3/1* (black) versus a pair of real bandpass modulators (grey).

advantage.[1] Its IMR performance is superior, too, with a 95th-percentile of 45 dB compared to 27 dB. The strong cross-coupling within the single complex modulator again proves helpful for IMR performance, maintaining more symmetry within transfer functions than is possible in a system of uncoupled real modulators.

The performance differential increases slightly as an ideal realization is approached. Table 5.4 compares performance between the *3/1* quadrature modulator and a real-modulator pair, for three levels of coefficient accuracy. Amplifier performance remains at 50 to 60 dB, with 2-dB matching between a stage's two amplifiers.

With more accurate coefficient matching — or higher-gain (or more-closely matched) amplifiers — the *3/1* modulator sees less performance degradation due to aliased in-band noise, and thus more closely reaches its deep (three-zero) in-band NTF. The pair of real modulators is ultimately limited to the lesser in-band noise shaping of its two-zero NTF. At the 0.1%-matching level, the quadrature modulator is superior by about 25-dB (4-bits) SNR and 17-dB IMR.

Table 5.4: Performance Comparison for Three Degrees of Mismatch[a]

Matching Accuracy	The *3/1* Modulator		Real-Modulator Pair	
	SNR	IMR	SNR	IMR
0.5%	74 dB	45 dB	51 dB	27 dB
0.3%	77 dB	49 dB	53 dB	32 dB
0.1%	79 dB	59 dB	54 dB	42 dB

a. 95th-percentiles for 1000 perturbed modulator samples.

1. Remember that this 23-dB performance advantage comes for equal total order. Although less than the 45-dB performance advantage that appeared to exist for the *4/0* modulator in Section 3.3 (i.e. prior to concerns over mismatch), 23 dB is a significant gain: almost 4 bits. As shown in Chapter 3, the increase in SNR performance can be traded off against bandwidth.

5.5 Summary

An improved fourth-order quadrature modulator was designed with a single notch in its image band. Proper implementation of the technique positioned a notch in the center of the INTF. Design trade-offs were investigated, and the design was optimized from the standpoint of its ability to combat the deleterious effects of mismatch.

The chosen design was shown to perform well in the presence of non-ideal effects. Modulators facing random 0.5%-peak coefficient mismatch and 50 to 60-dB amplifier dc gain, lost less than 7-dB SNR compared to their ideal SNR, and dropped to approximately 45-dB IMR.

The modulator was shown to significantly out-perform a pair of real modulators. Nearly 4-bit improvement in SNR performance was found, along with nearly 20-dB improvement in IMR performance, for the same total modulator order operating on complex inputs. The performance gap was seen to widen slightly with improved matching accuracy.

CHAPTER 6

Integrated Circuit Implementation

This chapter describes the steps undertaken to realize a 0.8-μm CMOS implementation of the *3/1* quadrature bandpass ΔΣ modulator [62 Jantzi]. First, the overall switched-capacitor architecture is presented and its operation explained. Then, constituent circuitry is discussed and simulation results are shown. Finally, the code-driven layout methodology is introduced, layout blocks are shown, and the advantages and disadvantages of the automated layout technique are outlined.

6.1 The Switched-Capacitor Architecture

6.1.1 From Signal Flow Graph to Switched-Capacitor Circuit

In Fig. 3.10, a general structure was shown for a fourth-order quadrature ΔΣ modulator. The architecture is amenable to switched-capacitor (SC) implementation, albeit a more involved one than used for traditional SC ΔΣ modulators.

The architecture consists of several blocks: the complex integrators are realized using amplifiers, switches and capacitors connected as SC integrators; the various feed-in and feed-back coefficients are realized using capacitors whose values have specific ratios to corresponding integrating capacitors; the quantization functions, which are single-bit sampled ones, are realized using latched comparators; and the two-level signals that drive the feedback capacitors are realized using a pair of one-bit DACs.

6.1.2 Complex Integrators

As discussed in Section 3.2.2, a complex integrator is created by the cross-coupled connection of two real integrators, as shown in Fig. 6.1(a). The $1/(z-1)$ blocks are simply $z^{-1}/(1-z^{-1})$ delaying-type SC integrators, so a single-ended version of a complex integrator is constructed as shown in Fig. 6.1(b).

The negative value for one of the capacitors, C_c, is easily realizable in a fully-differential implementation by reversing the connections to differential amplifier outputs. The ratio of the feed-back capacitor, C_d, to the integration capacitor, C_i, sets the *d* coefficient, while the ratio of C_c to C_i sets the *c* coefficient.

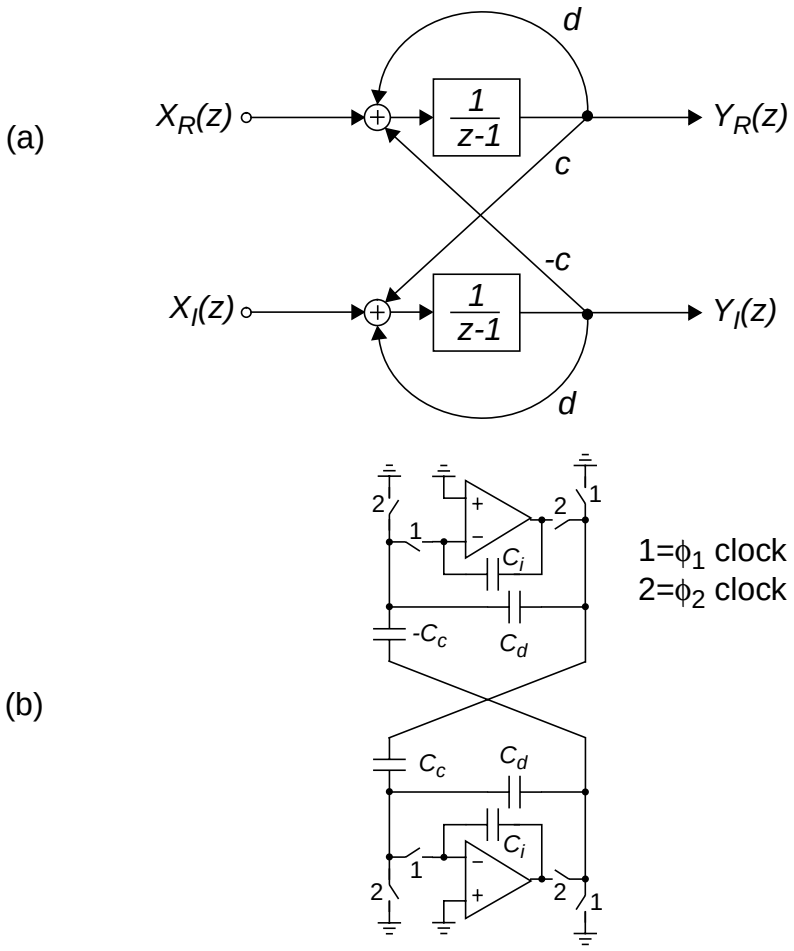


Fig. 6.1 (a) Complex-integrator system. (b) Single-ended circuit realization of a *z*-plane complex pole.

6.1.3 The Complete Fourth-Order SC Modulator

A fourth-order complex modulator, which contains four complex integrators inside a global feed-back loop, is constructed as shown in Fig. 6.2. For clarity, the structure is shown in its single-ended, rather than the actual, fully-differential, form.

The SC structure does bear a strong resemblance to the system-level diagram of Fig. 3.10. The modulator input has complex feed-ins to each stage through the C_a and C_e capacitors. Each channel has a latched comparator that produces a one-bit output and drives a one-bit feedback DAC, which, in turn, feeds its output back into the modulator stages through the C_b and C_f capacitors. Within each complex integrator, the C_c and C_d capacitors position the noise-shaping zeros.

6.1.4 The Switching Configuration

Fig. 6.3(a) shows the fully-differential interconnection of the real channel's fourth-stage amplifier, switched capacitors, and latched comparator. A non-overlapping clock generator provides the six necessary clock phases. Two versions of phase 1 (ϕ_1 and $\bar{\phi}_1$), and four of phase 2 (ϕ_2, $\bar{\phi}_2$ and their delayed counterparts, ϕ_{2d} and $\bar{\phi}_{2d}$) provide "early" and "late" clocking to minimize charge-injection. Transmission gates switch nodes with highly-varying voltages.

Integrators receive their input charge on the rising edge of ϕ_1 (note the clocking scheme in Fig. 6.3(b)), and have the entirety of that phase for settling. ϕ_2's rising edge then enables the comparator, whose output is latched into the RS flip-flop near the end of ϕ_2 (on the rising edge of the "latch" signal). This sets up the modulator feedback polarities for the following ϕ_1.

6.2 Circuit Blocks

The circuit is implemented in the CMOS-only portion of a 0.8-μm BiCMOS process [63]. All circuit simulations were performed with HSpice [64], using models supplied by Nortel. It is critical to properly design and verify each functional block of the SC modulator. These blocks include the amplifiers, the comparators, the clock generator, the input switching structure, and the one-bit DACs. The capacitor sizes must be determined first, so that the capacitive load on other circuitry is known.

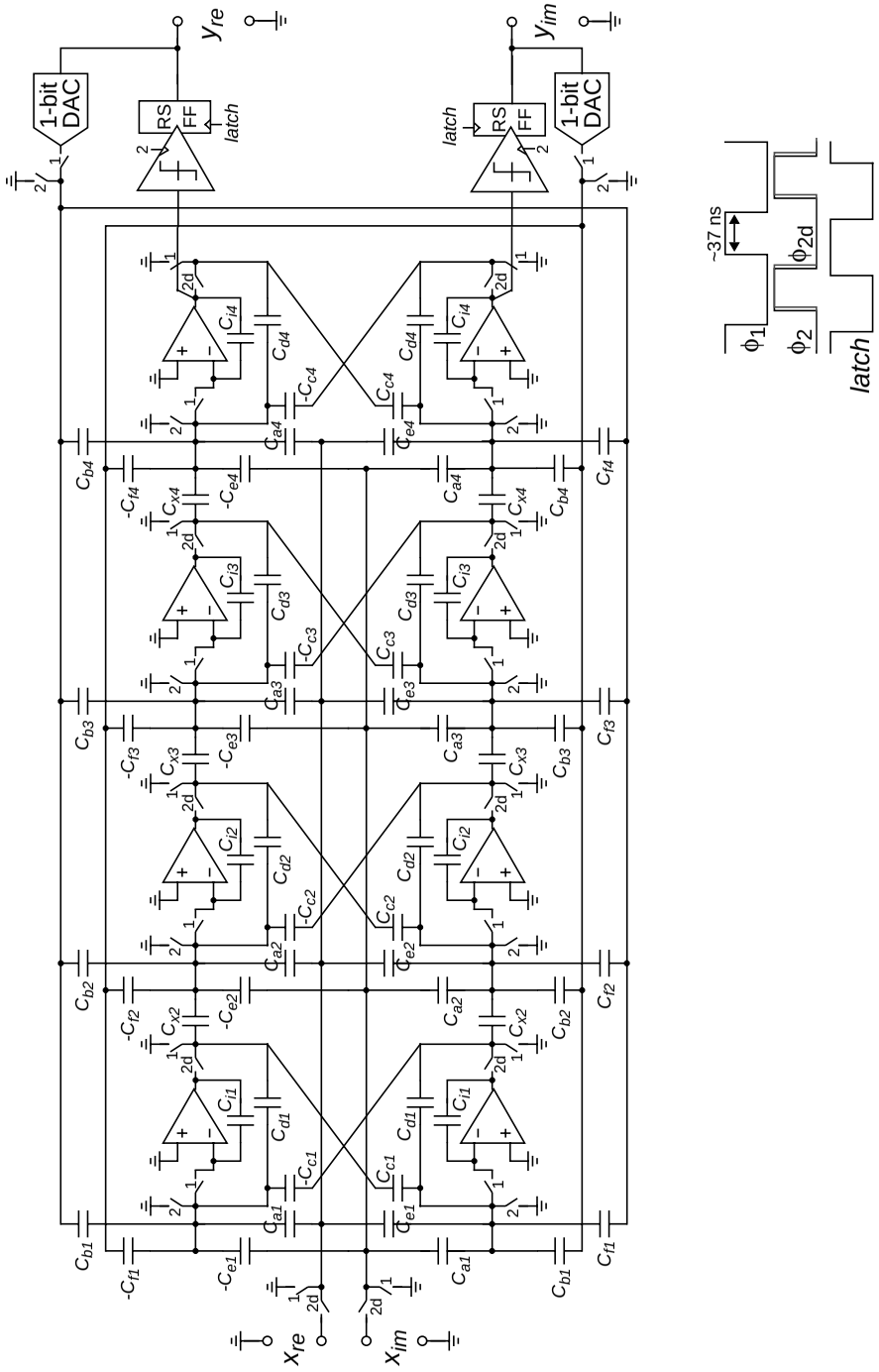


Fig. 6.2 Single-ended representation of the quadrature bandpass ΔΣ modulator circuit.

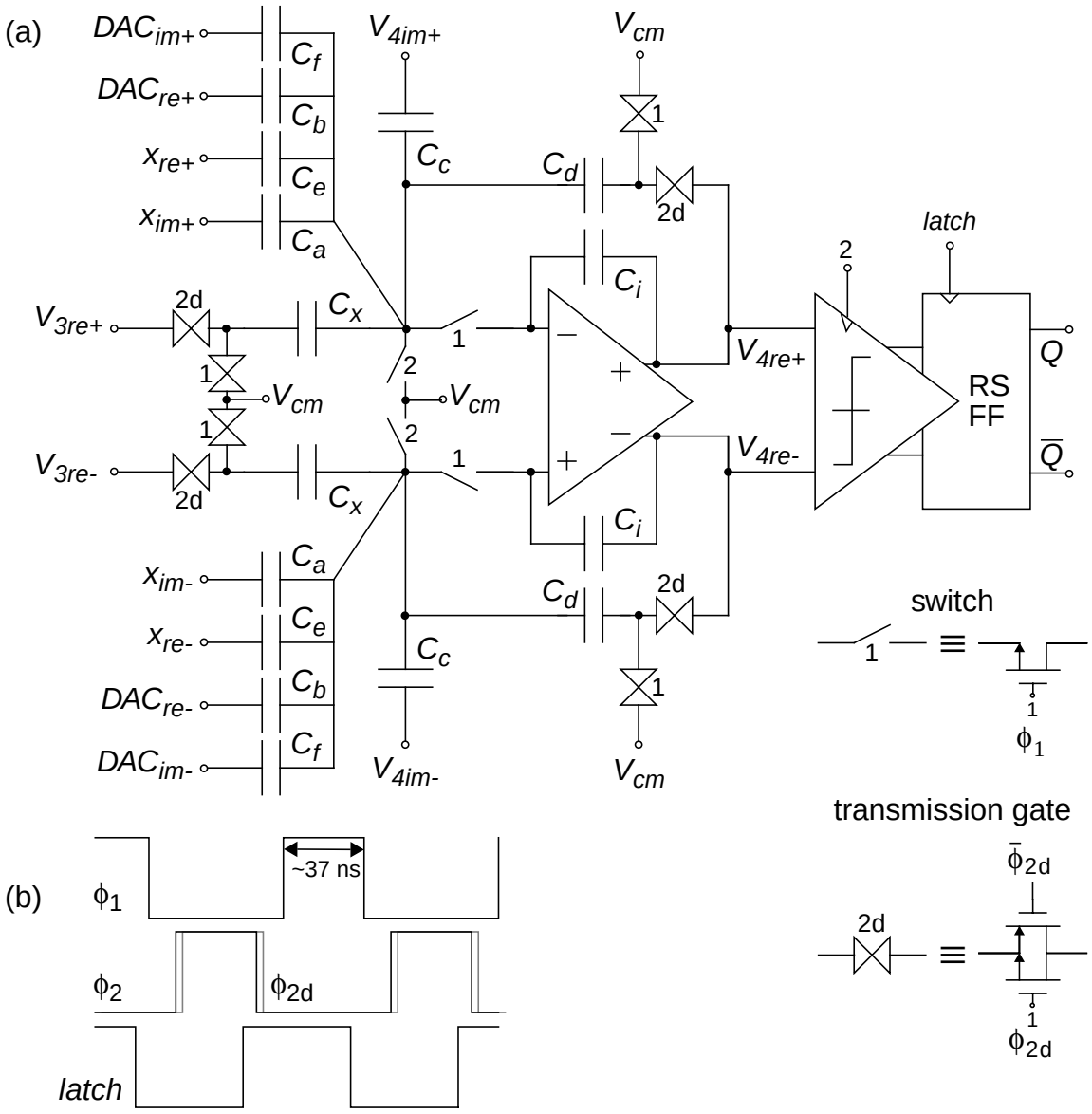


Fig. 6.3 (a) Real-channel fourth stage and comparator; other stages are similar.
(b) Clocking scheme.

6.2.1 Capacitor Sizing

I. Dynamic-Range Scaling

System-level modulator simulations were run in Simulink [59] for 2^{20} time steps, using the optimized coefficients designed for the NTF and STF in Chapter 5 and Appendix B. In an l_∞-scaling procedure, the peak values obtained for each state, multiplied by 1.1 for a 10% safety margin, were used to scale down the input coefficients of the appropriate state (and scale up its output coefficients) so that each amplifier output will never exceed the reference levels.

The reference voltages (the levels fed back from the one-bit DACs in Fig. 6.2) are set at 1 V and 4 V, centered around a common-mode (CM) level of 2.5 V (with 5-V supplies). Thus, each amplifier output is limited to 6-$V_{p\text{-}p}$ differential swing — i.e. ±1.5 V around the 2.5-V CM level, for each of the positive and negative amplifier outputs — and with the safety margin and coefficient scaling, should swing within about 90% of that range.

II. kT/C Noise

Once the scaling is complete, the desired capacitor *ratios* are known. The absolute capacitor sizes, though, define the total *kT/C* noise. A Lagrange-multiplier minimization approach [6 Jantzi] was used to set *kT/C* levels so that in-band noise requirements are met while capacitor area is minimized.

The *kT/C* noise is white, and thus the total in-band noise power is reduced by oversampling — falling by 3 dB for each doubling of the oversampling ratio. Furthermore, each capacitor's *kT/C* noise sees a certain transfer function (some of which have relatively small in-band power gains) to the modulator output — so some capacitors are more critical than others insofar as their contribution to total noise.

The end result is that, for this design, the largest capacitors required in all stages are those responsible for setting the noise-shaping zero locations (the capacitors labelled as C_c, C_d and C_i in Fig. 6.2) — which helps in positioning the notches accurately.

III. Sizes

The initial sizes so determined for the C_a and the C_e capacitors were quite small, resulting in unreasonably large capacitor spreads for some stages.[1] To reduce the spread, all *a* and *e* coefficients were increased tenfold. This coefficient increase manifests itself as a gain scaling of the STF, giving the STF an in-band gain of +20 dB, rather than 0 dB (which obviously reduces the maximum allowable input-signal size). Thus, the STF from Fig. 5.6(b) is shifted up by 20 dB, to appear as shown in Fig. 6.4. This scaling shows how gain can be incorporated into a modulator

1. Too large a capacitor spread — the ratio between the largest and smallest capacitor values in a stage — poses an implementation problem. There is a limit to the smallest capacitor that can be implemented in a given process (and the smaller the capacitor, the worse its accuracy), and once that is set, a large spread may mean the largest capacitor occupies an unreasonable area or creates too great a load on circuitry.

STF.[1] The final capacitor sizes used to realize the *3/1* modulator from Chapter 5, which has three in-band and notches and one image-band notch, are listed in Table 6.1. Note that the smallest (and thus least-accurately implemented) capacitors in each stage realize a portion of either an *A* or *B* coefficient, which is fortunate, since those coefficients are much less critical than the others.

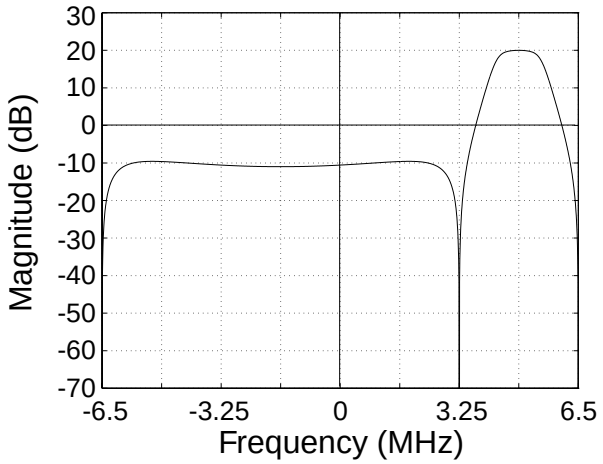


Fig. 6.4 The magnitude of the STF after 10x *A*-coefficient scaling.

Table 6.1: Stage Capacitor Sizes and Spreads

Parameter	Capacitor	Stage 1	Stage 2	Stage 3	Stage 4
feed-in coefficients $A = a + je$	C_a	1.719 pF	123 fF	60.8 fF	91.4 fF
	C_e	341 fF	379 fF	171 fF	—
feed-back coefficients $B = b + jf$	C_b	165 fF	176 fF	110 fF	124 fF
	C_f	60.8 fF	60.8 fF	190 fF	62.5 fF
zero-forming coefficients $p = d + jc$	C_d	2.73 pF	2.567 pF	2.742 pF	1.728 pF
	C_c	1.071 pF	1.063 pF	1.196 pF	716 fF
inter-stage capacitors	C_x	—	207 fF	488 fF	1.458 pF
integration capacitors	C_i	1.576 pF	1.503 pF	1.632 pF	1.013 pF
capacitor spreads	C_{max}/C_{min}	46	43	46	28

1. If multiple capacitors were implemented for each feed-in coefficient, a modulator STF could incorporate programmable gain amplification (PGA). In this structure, however, each complex feed-in coefficient requires eight capacitors, making multiple gain settings somewhat real-estate intensive.

6.2.2 Operational-Transconductance-Amplifier (OTA) Circuitry

I. Main Stage

The amplifiers are current-gain operational transconductance amplifiers [65] designed to drive the worst-stage capacitive load to 13-bit settling in under 35 nsec. In the main stage, shown in Fig. 6.5, the PMOS differential-pair (M_1-M_2) converts the differential input voltage to a differential current, which is mirrored to the output, with a gain of two, by wide-swing cascode current mirrors (M_3-M_6 and M_7-M_{10}) [66]. M_{15}-M_{16} set the tail current for the input diff-pair, while devices M_{11}-M_{12} and M_{13}-M_{14} are cascoded active loads that increase the amplifier gain.

Voltages V_{n2}, V_{p1}, and V_{p2} are set by a separate bias stage, while V_{ctl} is controlled by the common-mode feedback stage.

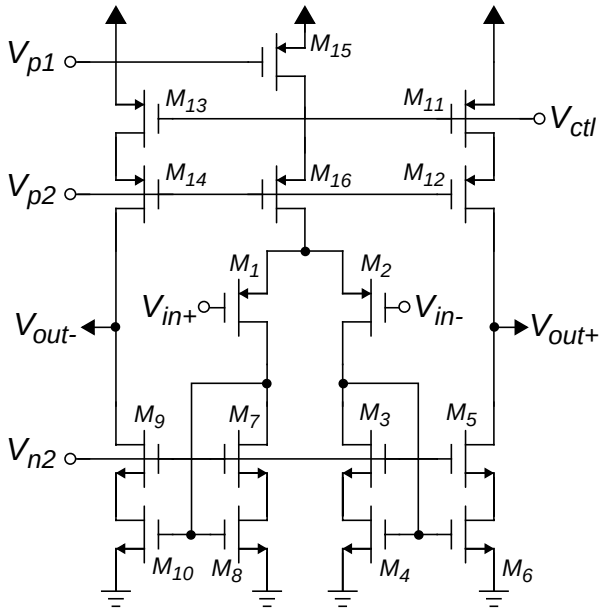


Fig. 6.5 Operational-transconductance-amplifier (OTA) main stage.

II. Bias Stage

A constant-g_m bias stage (Fig. 6.6) [67] provides bias levels for the main stage. The circuit is essentially a collection of high-swing cascode current mirrors connected in several feedback loops. The current in resistor R_b is set by the gate-source voltage differential between M_1 and M_2, which is defined by their aspect-ratio differential. This current flows in each of the transistor

quads M_1-M_4 and M_5-M_8, which set the voltages V_{p1} and V_{n1} for the single-stacked devices in the main stage and CMFB bias stage.

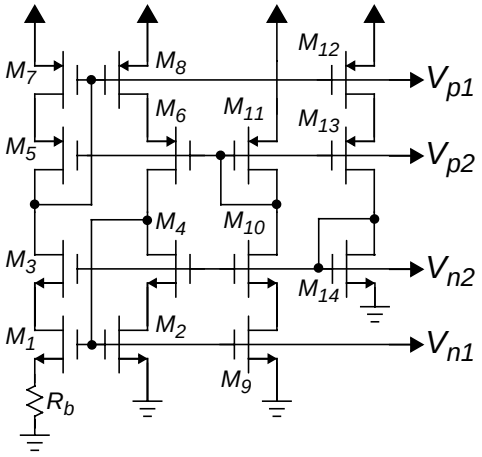


Fig. 6.6 OTA bias stage.

The same current is also mirrored to M_9-M_{10} and M_{12}-M_{13}, which set the current in devices M_{11} and M_{14}, respectively. The gate voltages of the latter devices, which are sized at one-quarter the width of the mirror devices driving them, define the bias levels V_{p2} and V_{n2} for the various "wide-swing" cascoded devices. It is wise to include start-up circuitry to ensure that the bias circuit does not begin in a stable zero-current state upon power up [67].

Thus, one high-resistance poly resistor sets the operating point for the amplifier. Furthermore, all device transconductances track, to a first degree, over power-supply, process and temperature variations.

III. Common-Mode Feedback Stage

Switched-capacitor common-mode feedback (CMFB) [68], shown in Fig. 6.7(a), maintains the average amplifier output level at 2.5 V. The amplifier outputs are ac averaged through the non-switched capacitors, C_c, whereas the (smaller) switched capacitors, C_s, maintain the necessary dc levels. In brief, feedback forces V_{ctl} to equal $V_{p1'}$, at which point the average of V_{out+} and V_{out-} is forced to equal the desired CM level of V_{cm} = 2.5 V. Lead compensation is provided for the amplifier by the resistors, R_z, in series with the ac-averaging capacitors in the CMFB block [69].

The CMFB has its own bias circuitry, shown in Fig. 6.7(b), which supplies $V_{p1'}$, a replica of the V_{p1} voltage that is generated in the main bias circuit. The separation keeps CMFB switching noise out of the main bias stage.

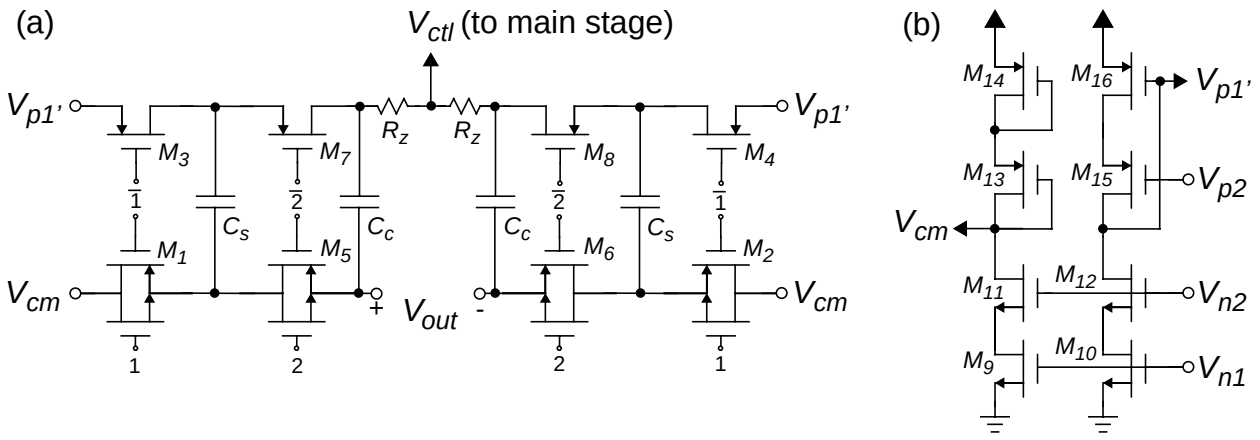


Fig. 6.7 (a) CMFB stage. (b) CMFB bias stage.

IV. Device Sizes

First-cut sizes for all devices in the amplifier were found using an amplifier design program known as PowerDesign [69]. This technique provides the designer with a tool that gives immediate estimates of amplifier performance from equation-based models of the amplifier. Modifications to the resulting sizes then optimize amplifier performance as needed. The sizes of all MOS devices, resistors, and capacitors, are summarized in Table 6.2.

Table 6.2: Amplifier Device Sizes

Main Stage		Bias Stage		CMFB Stage	
Component	Size[a]	Component	Size[a]	Component	Size[a]
M_1, M_2	400/0.8	M_1	40/1.2	M_1-M_8	5/0.8
M_3, M_7	40/1.6	M_2, M_9	10/1.2	M_9, M_{10}	10/1.2
M_4, M_8	40/1.2	M_3, M_4, M_{10}	10/1.6	M_{11}, M_{12}	10/1.6
M_5, M_9	80/1.6	M_5, M_6, M_{13}	25/1.6	M_{13}, M_{14}	45/1.2
M_6, M_{10}	80/1.2	M_7, M_8, M_{12}	25/1.2	M_{15}	25/1.6
M_{11}, M_{13}, M_{15}	200/1.2	M_{11}	6/1.6	M_{16}	25/1.2
M_{12}, M_{14}, M_{16}	200/1.6	M_{14}	2.4/1.6	C_c	1 pF
		R_b	2713 Ω	C_s	0.1 pF
				R_z	508 Ω

a. Sizes are given in μm, as width (W) divided by length (L), unless otherwise labelled.

V. Performance

Frequency-response simulations of the overall amplifier are shown in Fig. 6.8. The amplifier achieves nearly 60-dB dc gain, and when loaded with approximately 10-pF capacitance, achieves a unity-gain frequency of nearly 90 MHz and a phase margin greater than 70^{o}. It consumes 10.2 mW from 5-V supplies.

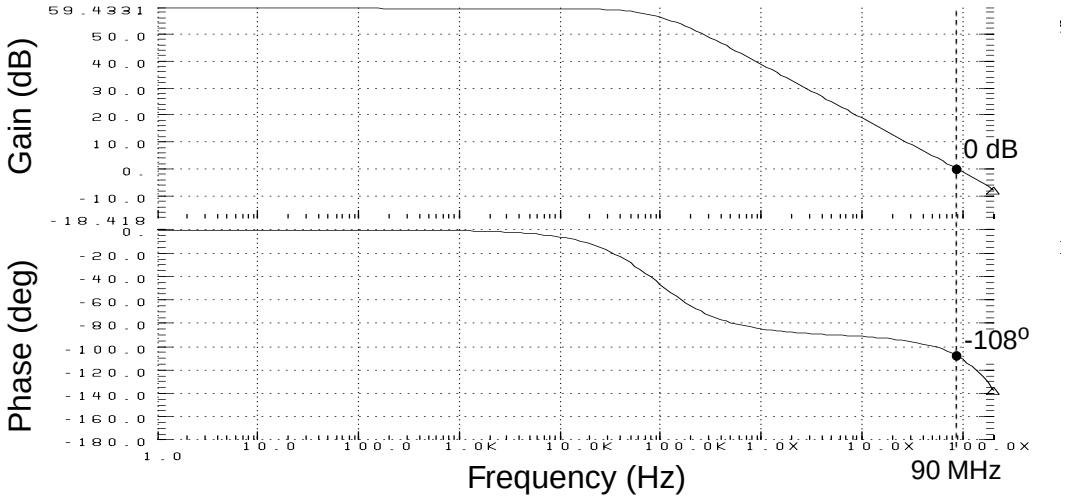


Fig. 6.8 OTA open-loop magnitude and phase response.

Transient-response simulations of the amplifier are shown in Fig. 6.9. For a 1-V input step, with 2-pF input and integrating capacitors and 4-pF load capacitance (including the CMFB capacitor, C_c), the amplifier settles to better than 13-bit accuracy within 23 ns — exhibiting a slew rate of nearly 200 V/μs (the input differential-pair tail current is nearly 600 μA). Note that the generous phase margin provides a smooth settling characteristic.

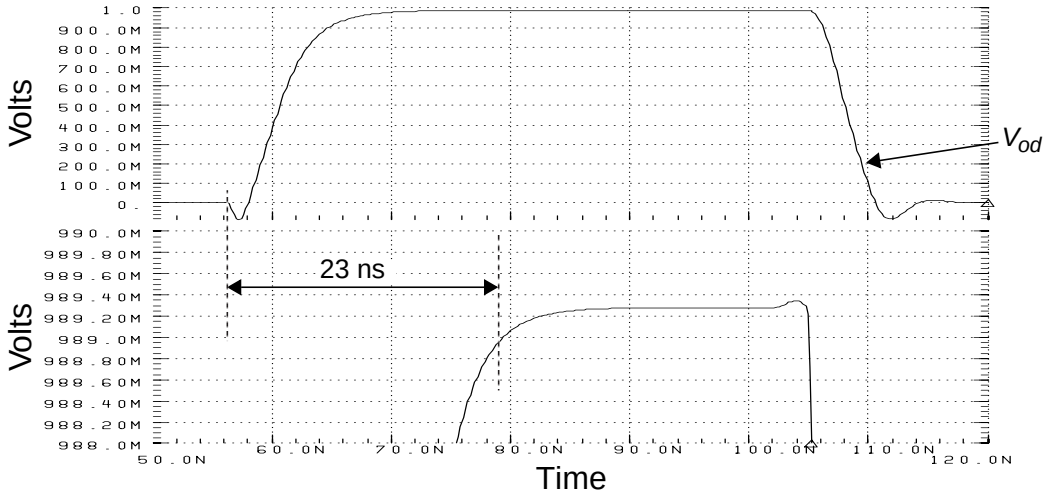


Fig. 6.9 OTA transient response.

6.2.3 Comparator Circuitry

I. The Comparator Core

Fig. 6.10 shows the straightforward comparator [70][71]; offset and hysteresis effects are not crucial since they are either reduced by the noise shaping or cause artefacts at out-of-band frequencies.

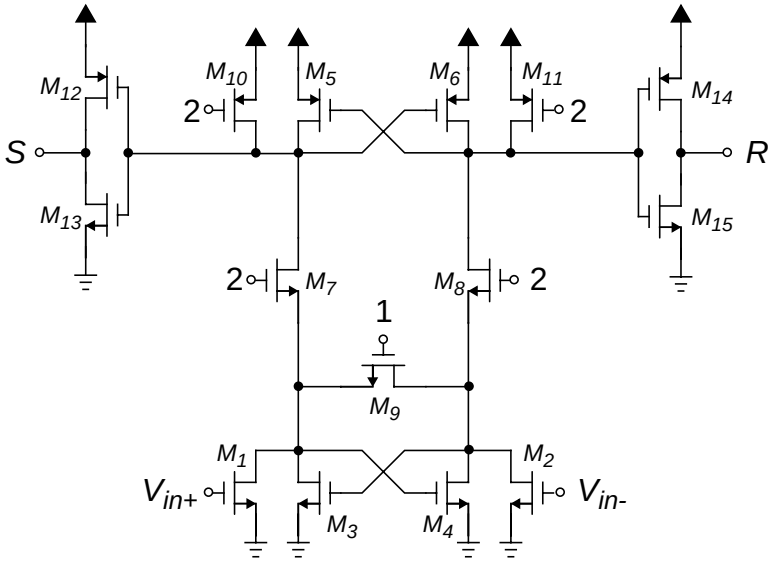


Fig. 6.10 CMOS comparator.

When ϕ_1 is high, and hence ϕ_2 is low (see the clocks in Fig. 6.3(b)), the comparator is reset since the NMOS latch (M_3-M_4) drains are tied together by M_9 and the PMOS latch (M_5-M_6) drains are pulled to the positive rail through M_{10} and M_{11}. When the comparator is enabled on the rising edge of ϕ_2, these drains are released and the NMOS and PMOS latches latch preferentially to a polarity determined by the pull-down currents in the input NMOS devices (M_1-M_2). Output inverters (M_{12}-M_{13} and M_{14}-M_{15}) drive the S and R (set and reset) output logic levels. Device sizes for the comparator are given in Table 6.3.

II. The Latched Comparator

The latched, or sampled-data, comparator required for the ΔΣ modulator is constructed by following the comparator with a clocked RS latch, which is shown in Fig. 6.11(a). When the "latch" signal is low, the X and Y levels are held high, which keeps the cross-coupled NAND latch in its current state. When the latch signal goes high, X and Y become $\bar{S}$ and $\bar{R}$, respectively. These signals set or reset the NAND latch, defining the Q and $\overline{Q}$ levels; naturally, S

Table 6.3: Comparator Device Sizes

Component	Size[a]
M_1, M_2	10/4
M_3, M_4, M_9	10/0.8
M_5, M_6	25/0.8
M_7, M_8	10/1.6
M_{10}, M_{11}	6/1.6
M_{12}-M_{15}	10/1.6

a. W/L (μm/μm).

being high forces *Q* high, and *R* being high forces *Q* low. Q and $\overline{Q}$ then set the appropriate levels for the reference signals fed back to the loop-filter capacitors. The symbol for the overall latched comparator is shown in Fig. 6.11(b).

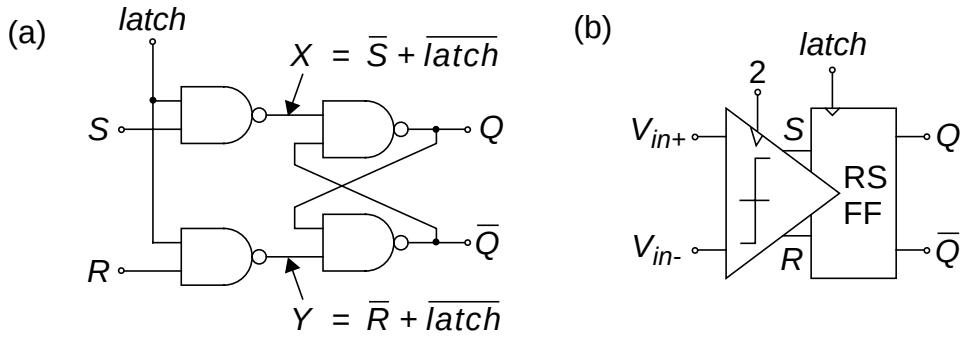


Fig. 6.11 (a) Clocked latch. (b) Latched comparator.

III. Performance

Fig. 6.12 shows the transient response of the comparator for a +10-mV differential input signal. 3.5 ns from the rising edge of ϕ_2, node *S* rises to 2.5 V (half-way between the supplies). The response is faster for larger differential inputs (i.e. 1 ns for a 3-V differential input), and is suitably fast for smaller inputs as well.

To determine the comparator's functionality for a formidable input sequence, the input's polarity and strength were varied throughout subsequent clock cycles — to either positive or negative, 10-mV or 3-V differential, levels. Examining the comparator operation under such

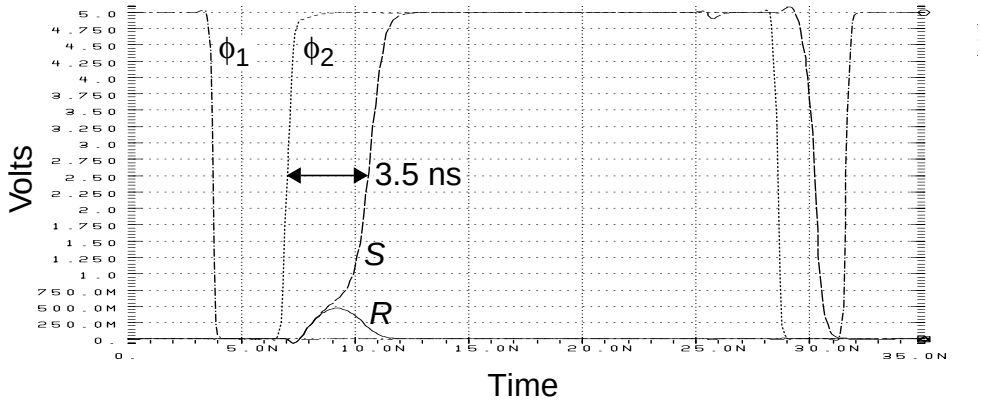


Fig. 6.12 Comparator transient response.

conditions highlights the worst-case events — i.e. when the comparator must recover to detect a small signal of one polarity immediately after comparing a large one of the opposite polarity.

The comparator operation for such a sequence is shown in Fig. 6.13, over ten comparison cycles. The size and polarity of its input (which is the signal V_{4re}), are represented by the + and - signs on the figure. For the first comparison, the input is small and positive, and thus causes *Q* to go high (and $\overline{Q}$ to go low). This is followed by a small negative and then a small positive input, which cause *Q* to go low then high, as desired. The fourth comparison is for a large negative input, and is followed by one for a small positive input (which is the tough transition, mentioned above). These comparisons also result in the correct *Q* settings — a low followed by a high. The sequence continues for five additional cycles, all resulting in correct decisions.

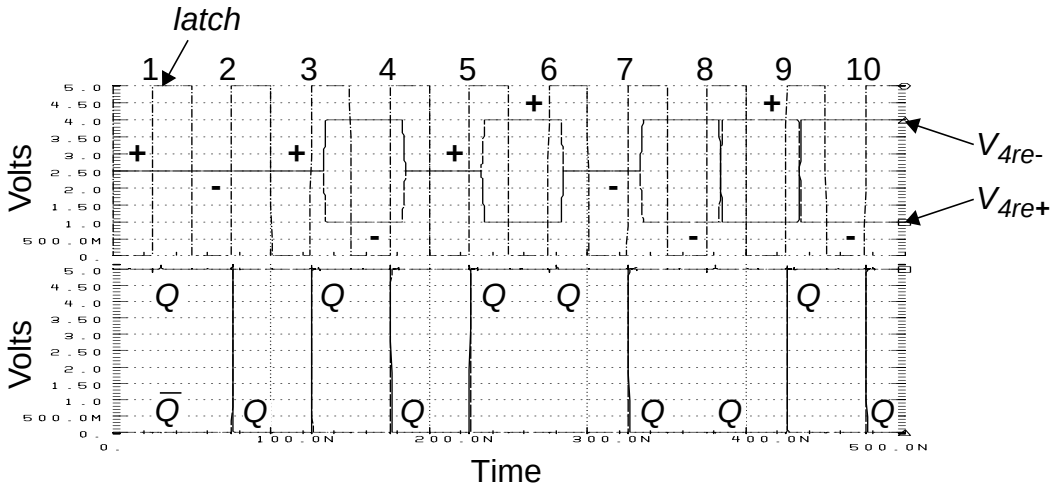


Fig. 6.13 Comparison sequence for ten clock cycles.

6.2.4 Clock Generator

A standard non-overlapping clock generator develops the six required clock phases. It consists of two cross-coupled NOR gates, as shown in Fig. 6.14. Extra delays in the loop extend the period of time after ϕ_1 goes low until ϕ_2 goes high, and vice-versa. The non-overlapping signals thus generated are buffered by large inverters to drive the on-chip clock buses. Device sizes for each gate are given in Table 6.4.

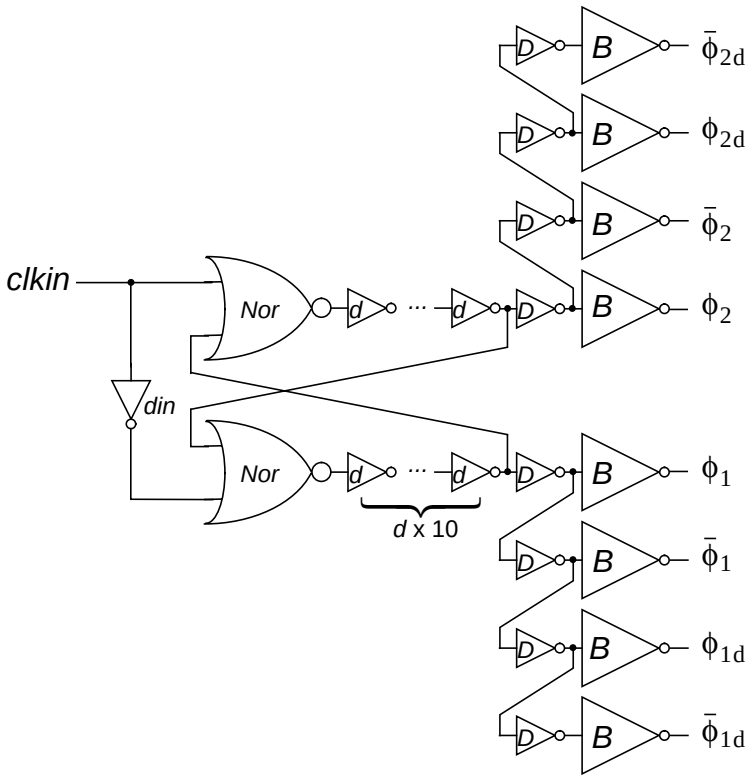


Fig. 6.14 Non-overlapping clock generator.

Table 6.4: Logic-Gate Device Sizes[a]

Gate	PMOS	NMOS
din	20/0.8	10/0.8
Nor	20/0.8	10/0.8
d	12/1.2	6/1.2
D	40/0.8	20/0.8
B	200/0.8	100/0.8

a. W/L (μm/μm).

Simulations of the clocks, with a 5-pF load on each clock output, are shown in Fig. 6.15. There is approximately 1-ns delay between the clocks and their delayed versions, and about 1-ns non-overlapping period.

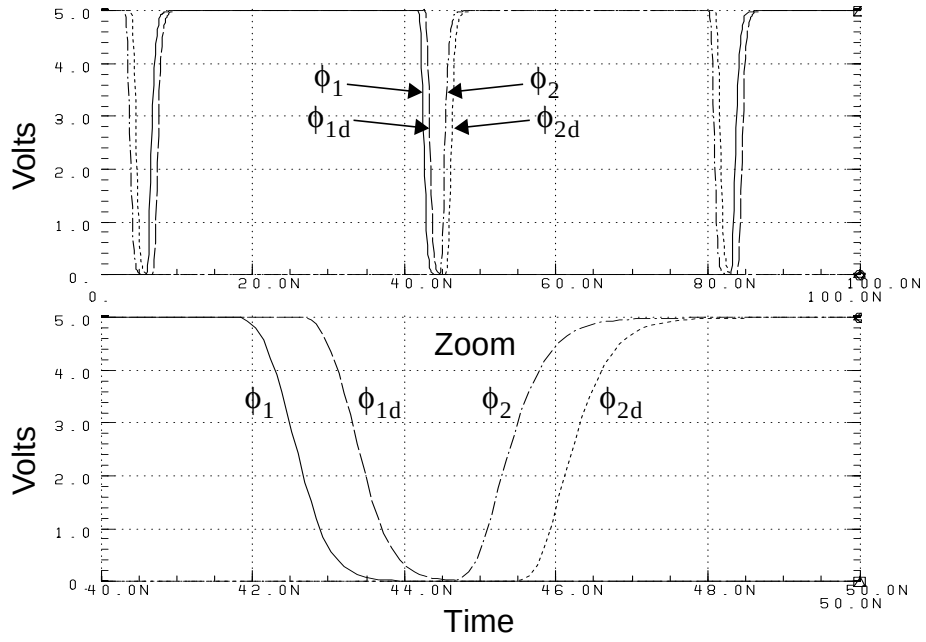


Fig. 6.15 Clock signals for phases one and two, and their delayed versions. The inverted clocks are not shown.

6.2.5 Input-Switch Structure

As was seen in Fig. 6.2, one set of input switches can drive all of one input's C_a and C_e capacitors. It is prudent to ensure that the associated waveforms are correct. From Fig. 6.16, which shows the real channel, it is apparent that the sampled voltage, $\hat{x}_{re}$, should follow the input signal, x_{re}, throughout ϕ_{2d}, while sitting at V_{cm} during ϕ_1.

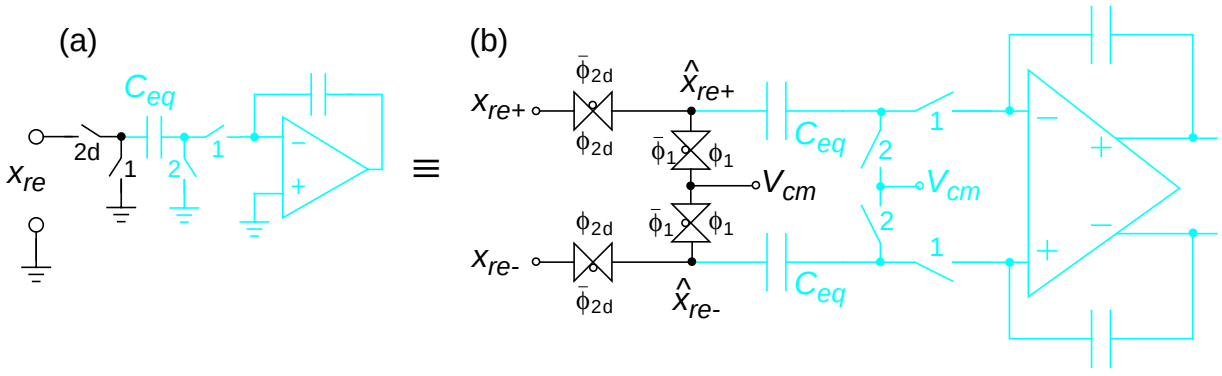


Fig. 6.16 Sampling the real input onto the total feed-in capacitance. (a) The simplified single-ended representation. (b) The differential configuration, which explicitly shows where transmission (tx) gates are used.

Simulations, shown in Fig. 6.17, demonstrate the correct input-sampling operation for both the real and the imaginary channels.

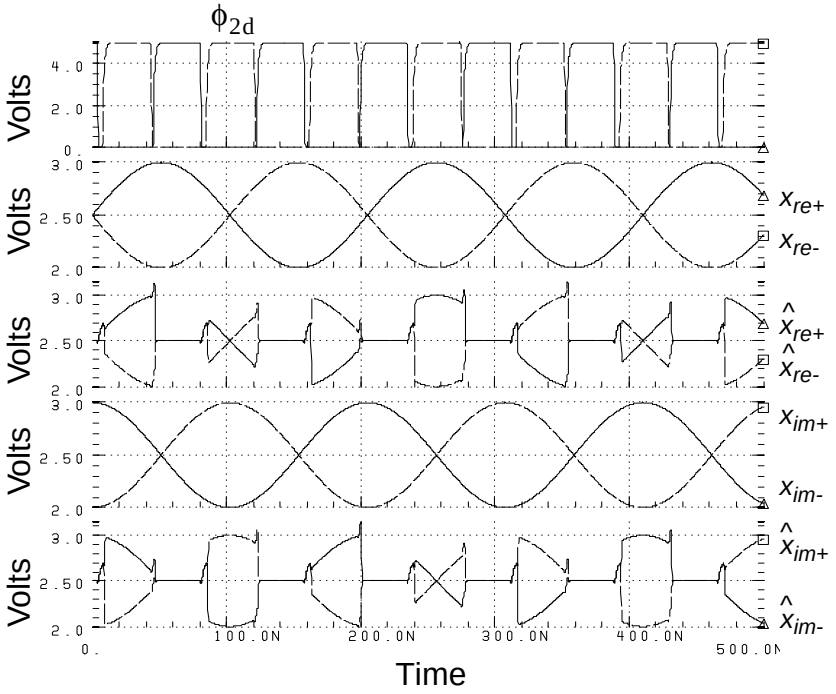


Fig. 6.17 Sampling of the real and imaginary input signals (sine waves) on ϕ_{2d}.

6.2.6 One-bit DAC

As seen in Fig. 6.2, the channel outputs, y_{re} and y_{im} (i.e. comparator outputs Q_{re} and Q_{im}), each drive a one-bit DAC that feeds either a "positive full scale" or "negative full scale" value back to the modulator on ϕ_1. Each one-bit DAC is constructed from a set of switches and two reference voltages, as shown in Fig. 6.18 for the real channel. The two feedback levels are the reference voltages V_{ref-} and V_{ref+} — 1 V and 4 V, respectively — which have opposite polarities with respect to the common-mode voltage of 2.5 V. The reference connection is controlled by a logical operator that depends on the state of Q_{re}.

Fig. 6.19 shows the levels fed back to each channel for some typical Q_{re} and Q_{im} outputs. When Q is high, the 4-V reference signal is fed to the capacitors during ϕ_1 — when Q is low, the 1-V signal is fed back.

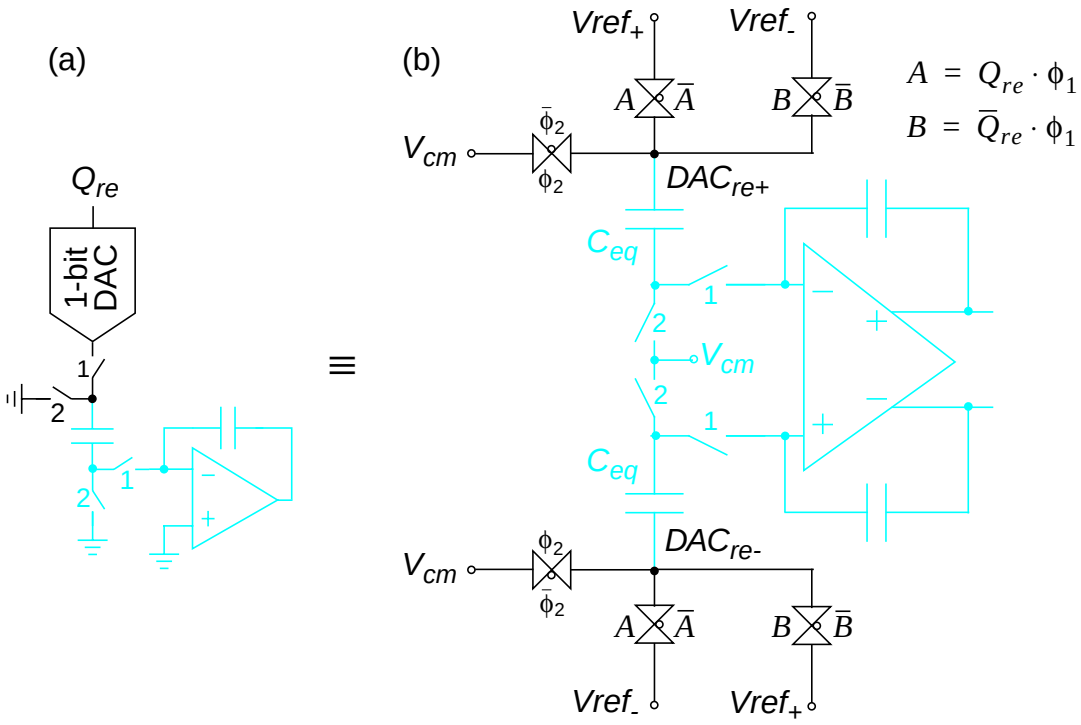


Fig. 6.18 One-bit DACs connect the appropriate reference voltages to the feedback capacitors. (a) The simplified single-ended representation. (b) The differential configuration.

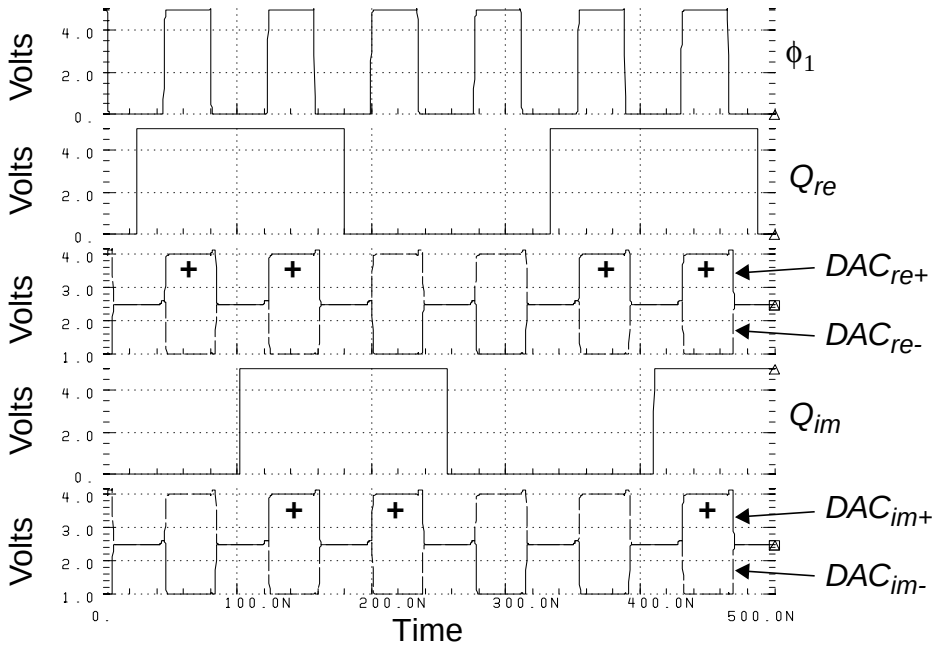


Fig. 6.19 The real and imaginary DAC feedback signals. These have 1-V and 4-V levels, and are sampled on ϕ_1.

6.3 Layout Techniques

Fully-custom layout was generated with BALLISTIC [72], an analog-layout language that runs with Mentor Graphics' GDT. ASCII files containing code and parameters define device geometries and positions, spacing between objects, and so on. A layout is constructed using both the user's code and process-technology information as inputs, so that very little user effort (the proverbial "push of a button") is required to generate new layouts. This is very useful for fast redesign in a new technology, modification of modulator specifications (order, sampling rate, bandwidth, etc.), modification of modulator flavor (real versus complex, lowpass versus bandpass), or for improved design of constituent circuitry (amplifiers, comparators, etc.).

The first IC implementation used the CMOS-only portion of a 0.8μm BiCMOS process [63].

6.3.1 Capacitors

Care was taken to obtain good accuracy in capacitor ratioing: unit-sized capacitors and extra capacitors, all rimmed with dummy rings, set the necessary ratios. A BALLISTIC routine calculates the exact width and length needed for each non-unit capacitor to maintain the proper perimeter-to-area ratio. The layout grid snap precludes use of these exact widths, so the routine then cycles through several nearby width and length combinations and selects those dimensions which minimize the capacitor-ratio error. The ability to include such routines in the midst of layout code is a powerful advantage of the automated-layout technique.

Fig. 6.20 shows the capacitor arrays for the third stage of the real modulator channel. The nodes AMP_{in} and AMP_{out} are the non-switched amplifier inputs and outputs; sum_{in} is the switched summing node, which is the junction of the input switches close to the amplifier (hence this node is common to all capacitors except the integrating capacitor); and the *in* and *ref* nodes are fed by the sampled modulator input and reference signals, respectively. Capacitor C_x is fed from the second stage, while C_d and C_c are fed by the real and imaginary outputs, respectively, of the third stage.

Note that all inputs feed into capacitor bottom plates, so that bottom-plate parasitic capacitances affect the capacitive loading only, and don't cause a charge division. The capacitor dummy rings are interconnected and tied to the common-mode level.

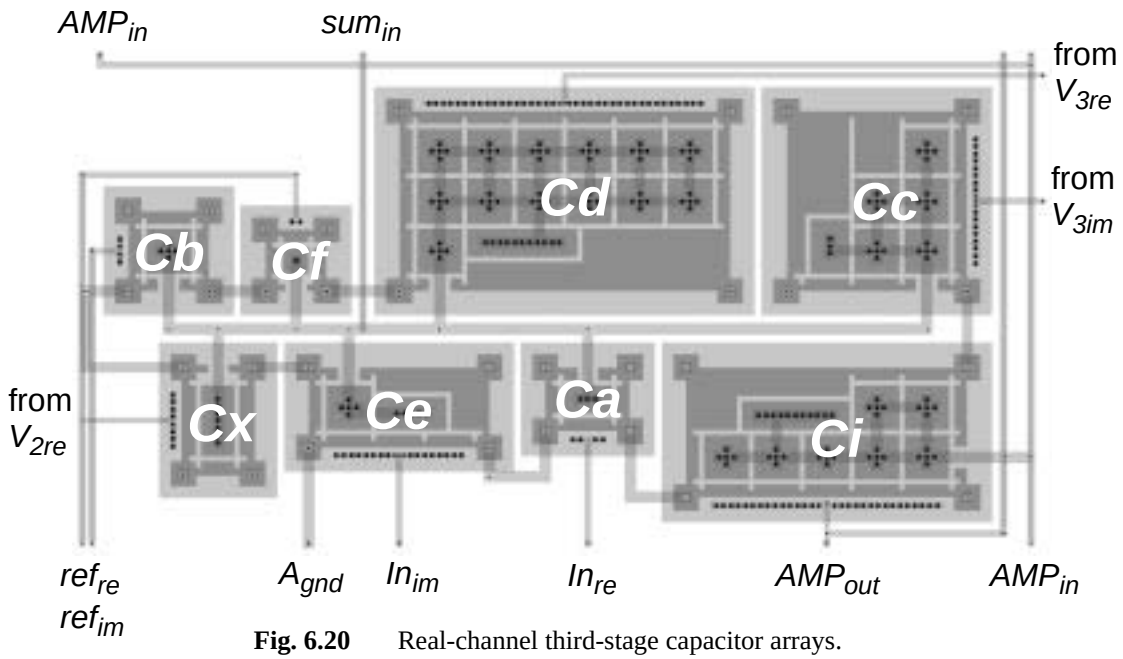


Fig. 6.20 Real-channel third-stage capacitor arrays.

All interconnect wiring and capacitors are generated in such a way that a completely new set of capacitor arrays can be laid out error free. In essence, all blocks grow away from a point in the center of the layout, and wires navigate around the capacitors so as not to violate design rules. This allows the same basic layout code to be used from one stage to the next, and furthermore, allows efficient modification of modulator coefficients from one design to the next — facilitating alteration of modulator noise-shaping specifications.

6.3.2 Switches

Fig. 6.21(a) shows the layout for the input-switch cluster that was discussed in Section 6.2.5. From Fig. 6.16(b), we see that each channel requires four transmission gates, resulting in the eight seen for both channels in this layout. The real and imaginary inputs feed into the top and bottom of the cluster, respectively, with the clock signals feeding in from the right, and the sampled outputs leaving at the left.

The layout for the DAC-switch cluster that was discussed in Section 6.2.6 is shown in Fig. 6.21(b). The reference voltages feed into the top of the cluster, with the clock signals feeding in from the left, and the sampled outputs leaving at the right.

All switch sizes are fully parameterized; capacitor charging-time is dependent on switch on-resistance, so the ability to re-size switches can be crucial if capacitor arrays are modified.

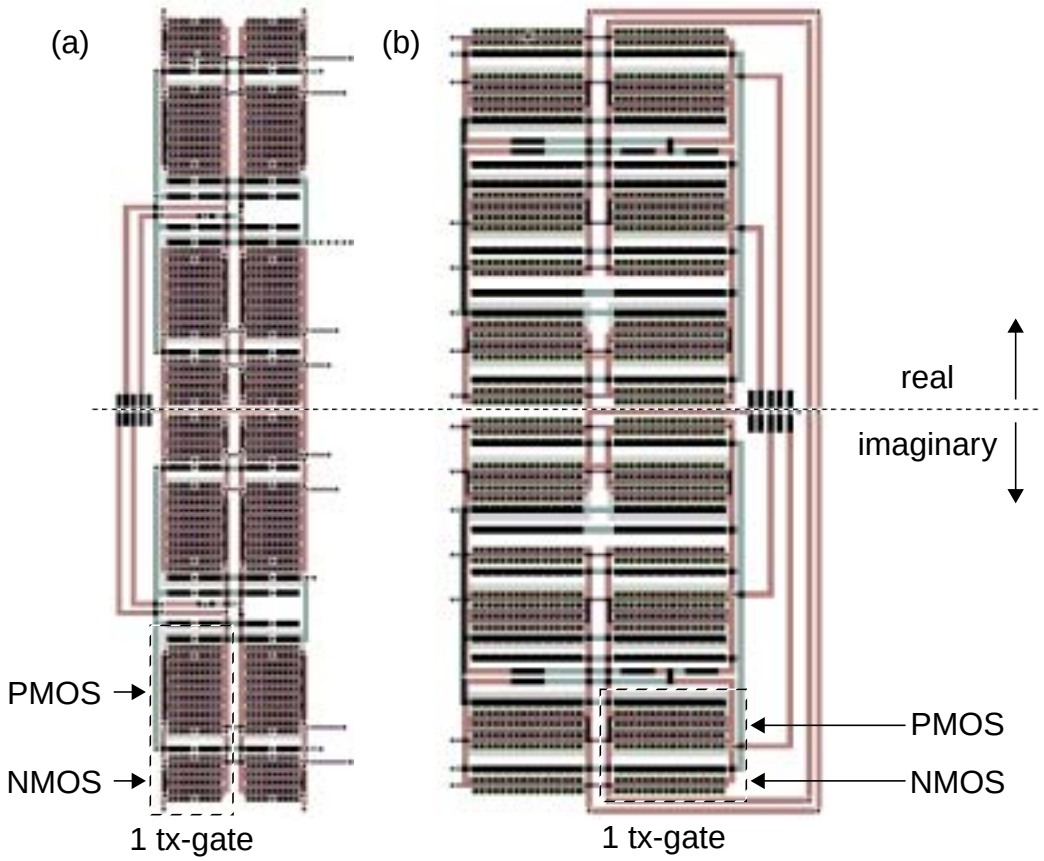


Fig. 6.21 (a) Input-switch cluster, comprising eight transmission gates (four for each channel). (b) DAC-switch cluster, comprising twelve transmission gates (six for each channel).

6.3.3 Comparator

The latched-comparator layout is shown in Fig. 6.22. Note the mirror-image symmetry between the upper and lower halves of the layout. The inner separation between the power buses (which run along the top and bottom of the layout) is matched to the same parameter in the main modulator channels. Once again, all sizes are parameterized and all layout locations are relative, allowing error-free automated layout.

6.3.4 Amplifiers

The OTA layout is shown in Fig. 6.23. The bias circuitry is the left portion of the layout, with the main stage in the center and the SC CMFB at right. The bus separation is 160 μm. Note the pairs of capacitors (the black rectangles) in the CMFB stage. Also note the rows of substrate connections separating the various amplifier subsections.

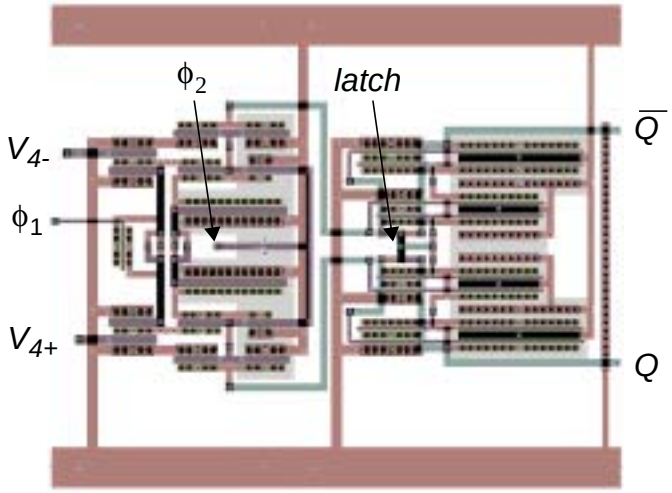


Fig. 6.22 Latched-comparator layout.

Parameterized layout proves especially useful in the case of amplifier design, where performance is so heavily based on the sizes, and relative sizes, of constituent devices.

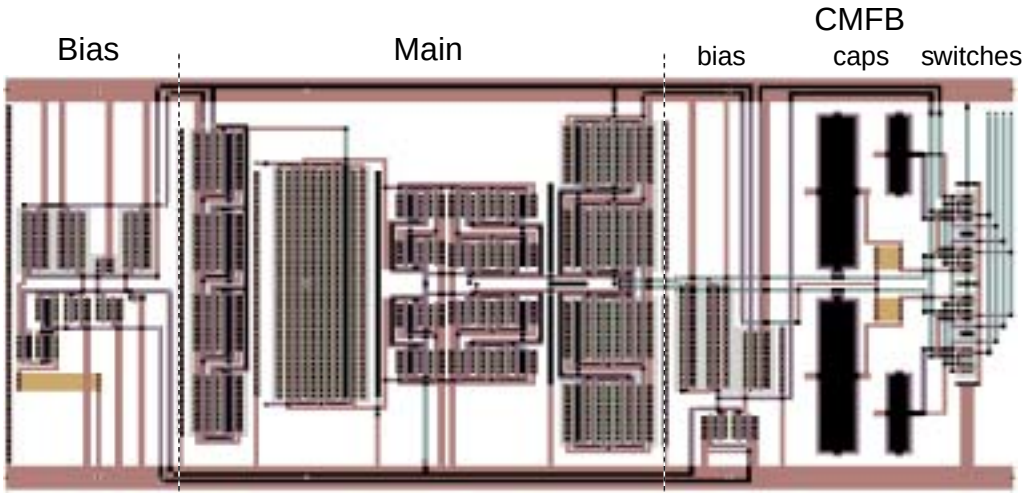


Fig. 6.23 Amplifier layout.

6.3.5 The 0.8-μm CMOS Modulator Layout

Fig. 6.24 outlines the floorplan, while Fig. 6.25 shows the complete layout, for a 0.8-μm CMOS version of the modulator. The modulator occupies a total area of 2.4 mm by 1.8 mm. The real and imaginary channels are apparent, being nearly mirror images above and below the horizontal center-line. The vertical symmetry within each channel is due to the differential nature of the design.

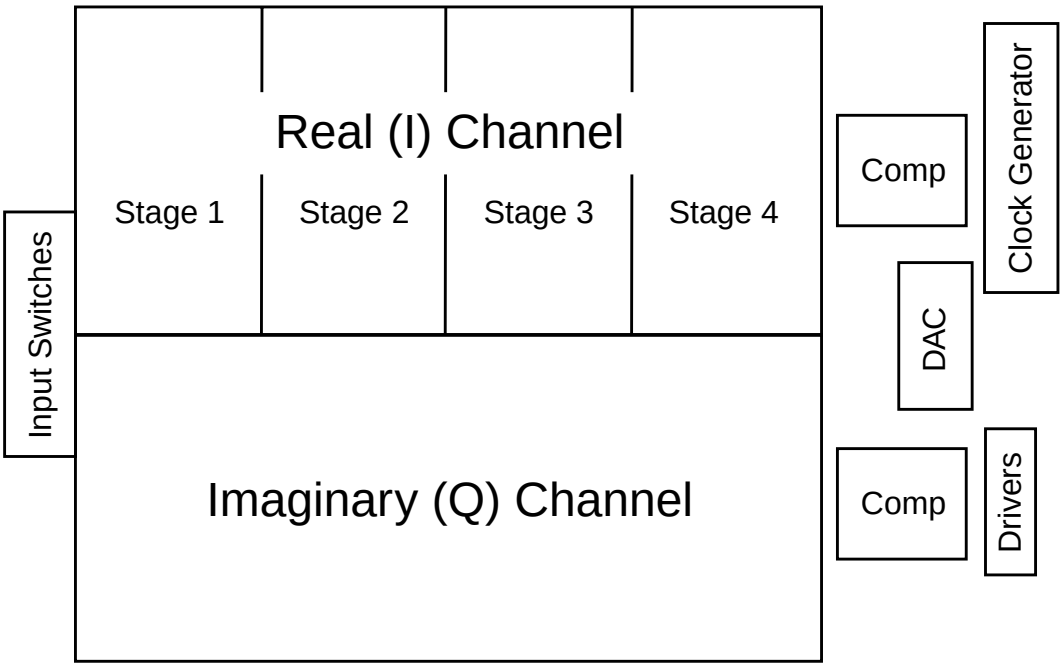


Fig. 6.24 Modulator floor-plan.

At the far left of the layout is the input-switch cluster, followed by stages one through four for each channel. The comparators attach to the right of the associated fourth stage, with the DAC and switches lying between them. The clock generator lies in the top right, with the pad-driver circuitry at bottom right. White space in the modulator can be reduced by decreasing several separation parameters specified in ASCII files.

Horizontal clock buses run across the center, and along the top and bottom, of the layout. The other four buses that run horizontally (above and below the amplifiers in each stage) carry differential signals and power. The vertical buses to the right of each stage supply clocks to the SC CMFB circuitry, and connect signals between the real and imaginary channels (for the cross-coupling capacitors, C_c).

At this level of the hierarchy, the coded-layout approach gives the designer great freedom to modify a layout without starting from scratch. If, for example, a faster amplifier was the only improvement required for the design, the entire layout could be regenerated very quickly with only minimal code changes — either a pointer to the new amplifier layout, or a small set of new code that would actually generate the improved amplifier layout.

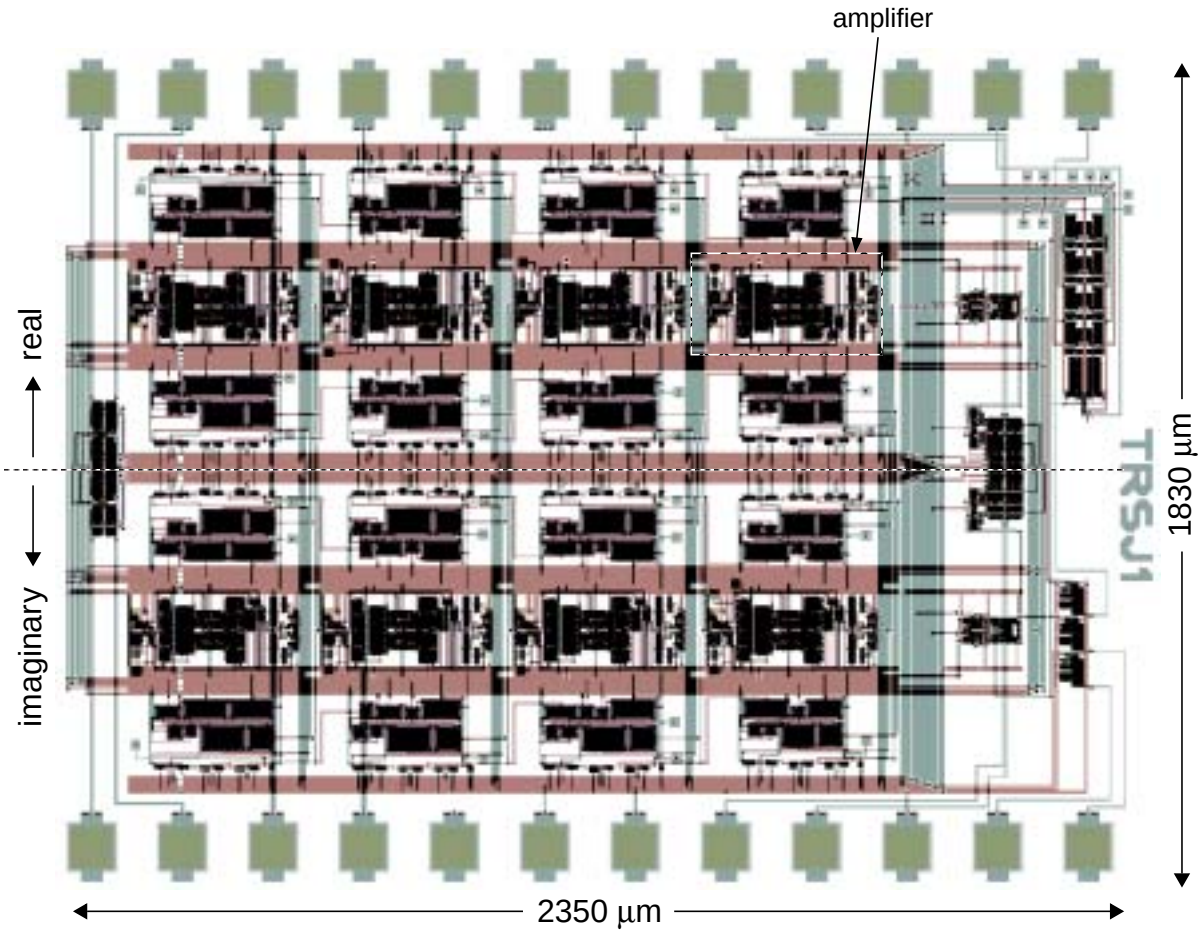


Fig. 6.25 The 0.8-µm CMOS modulator layout.

This example brings to light the fact that layout code can be combined with hand optimization. In one approach, hand-optimized layout blocks can be read as cells into a larger layout. In a second approach, a generated layout can be used as a quickly-reached starting point, providing only a first-cut layout and floorplan (or perhaps only providing unconnected blocks) which can then be optimized by hand. In the latter approach, one obviously loses the ability to regenerate the entire layout quickly in a new technology.

6.3.6 A 0.5-µm CMOS Modulator Layout

A second layout was generated for a 0.5-µm CMOS process in only two weeks time. The fast turn-around time was possible with the coded-layout methodology, even though the second process had different design rules and layers than the first. For example, while the first process had three levels of metal, high-resistance polysilicon, linear (poly-poly) capacitors, etc., the second process had only two levels of metal, and few of the other propitious features.

The second layout is shown in Fig. 6.26. The floor-plan is identical to the previous modulator, which is expected, since they were generated from nearly identical layout code. Note that the second layout is larger than the first — approximately 30% wider and 20% taller — which seems unusual, since the second uses a finer-line process (0.5 μm compared to 0.8 μm).

The increase in size is due to the lack of poly-poly capacitors in the second process. The replacement metal-poly-metal capacitors have much smaller capacitance-per-unit-area, resulting in much larger capacitor area.[1] For a visual comparison, notice that the SC CMFB capacitors in the first layout represent only a small fraction of each amplifier's area, while in the second layout the same capacitors occupy nearly half of an amplifier's total area.

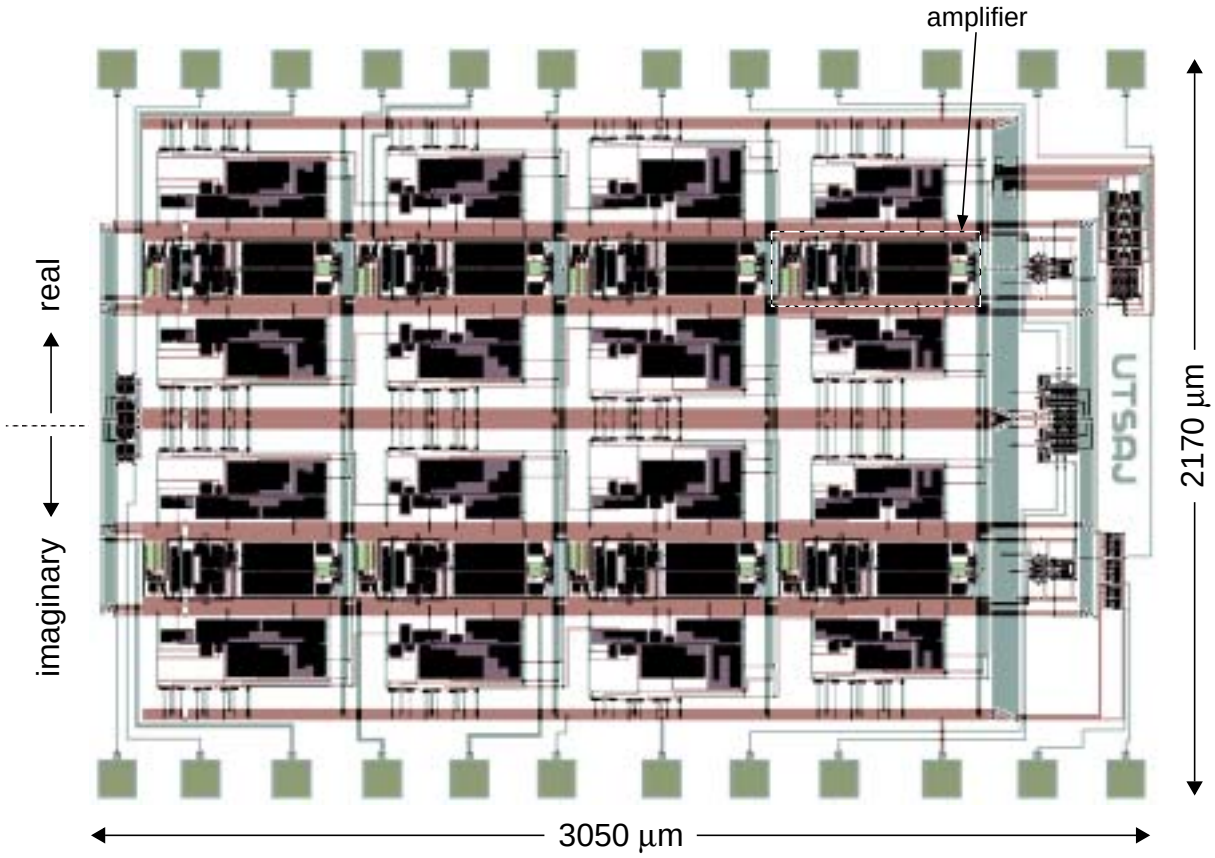


Fig. 6.26 The 0.5-μm CMOS modulator layout.

1. In fact, all switched- and integrating-capacitor values were scaled to 40% of their original values for this 0.5-μm version of the modulator. The overall layout-area increase is as stated, even with the reduced capacitor values. The amplifier CMFB capacitor sizes are equal to those in the first layout.

6.4 Summary

This chapter described all aspects of the silicon IC realization process. The switched-capacitor architecture was shown and the switch timing was described. All critical constituent circuits were examined, with simulations presented and discussed.

The layout of some important modulator blocks was shown, and two versions of the modulator layout were described. The coded-layout methodology was seen to afford great opportunities in the re-design of modified modulators; the technique allows fast regeneration of a modulator layout for a new technology (as was proven herein), or it greatly facilitates the regeneration of a layout for a modulator that has new specifications or improved constituent circuitry. The coded-layout technique also allowed automated routines to generate important layout blocks; a routine to optimally size the non-unit capacitor in a capacitor array was described. On the down side, unless considerable effort is invested into the layout code, generated layouts seem to be less compact than hand-optimized ones.

CHAPTER 7

Integrated Circuit Testing and Experimental Results

This chapter describes the experimental testing of the quadrature bandpass ΔΣ modulator integrated circuit [62 Jantzi]. First, the pin connections of the IC are described, a circuit board is shown that houses the IC, and the test set-up is introduced, and explained. Then, experimental data, collected using the same setup, is presented, analyzed, and discussed. Finally, by interpreting the test results in the context of Chapters 4 and 5 (which explored non-ideal effects, and methods with which to combat them), and by using hindsight, improvements are suggested for a next-generation version of the IC.

7.1 The Silicon Integrated Circuit

7.1.1 Die Photos

The die microphotograph of the 0.8-µm CMOS quadrature bandpass ΔΣ IC is shown in Fig. 7.1. This IC was fabricated at Nortel via CMC.[1] The only difference between the photo and the layout plot of Fig. 6.25, are the bond wires connecting to the pads. An overlay highlights the major blocks that were discussed in Chapter 6.

The 0.5-µm CMOS modulator die photo is shown in Fig. 7.2. This IC was fabricated by Analog Devices, Inc., Wilmington, MA.

1. The Canadian Microelectronics Corporation (CMC) provides Canadian universities with access to IC fabrication within the Canadian microelectronics industry.

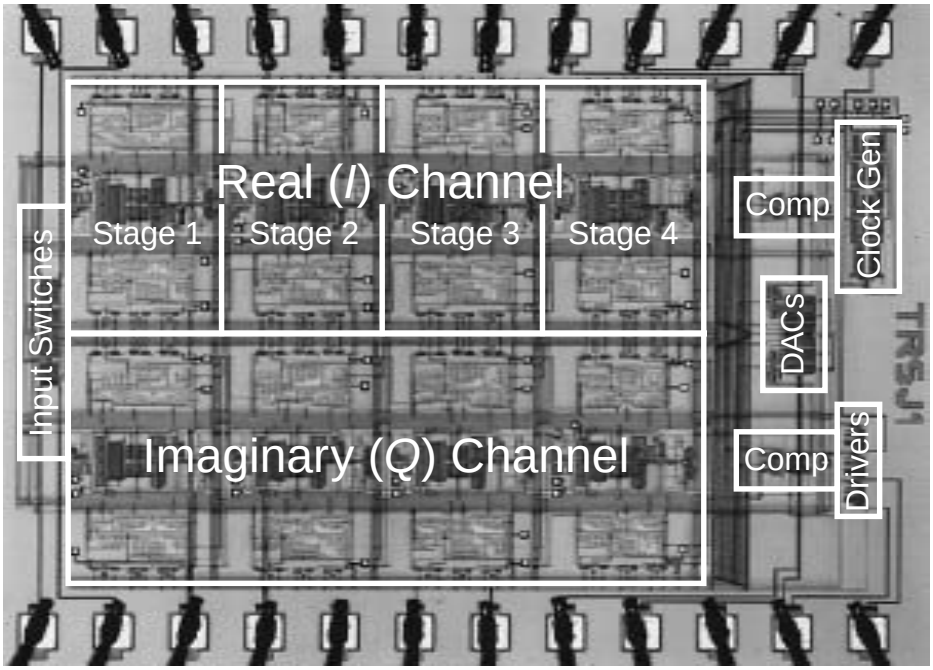


Fig. 7.1 Microphotograph of the 0.8-µm CMOS quadrature bandpass ΔΣ IC.

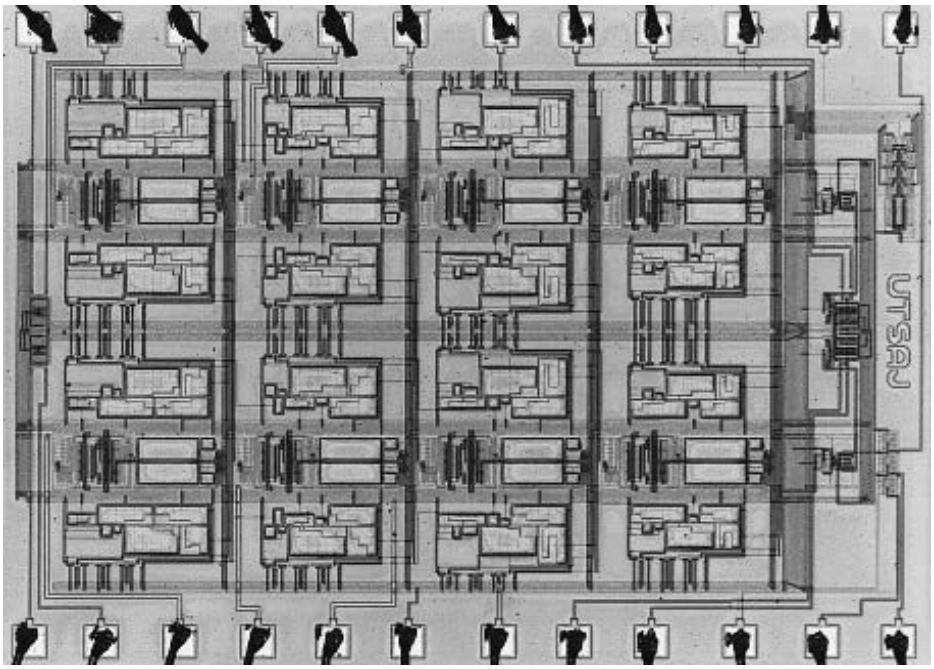


Fig. 7.2 Microphotograph of the 0.5-µm CMOS quadrature bandpass ΔΣ IC.

7.1.2 Pin Connections

Fig. 7.3 shows the modulator pin connections, with arrows indicating whether a pad is an input or an output. The pads are numbered according to their connections in a 68-pin grid array package.

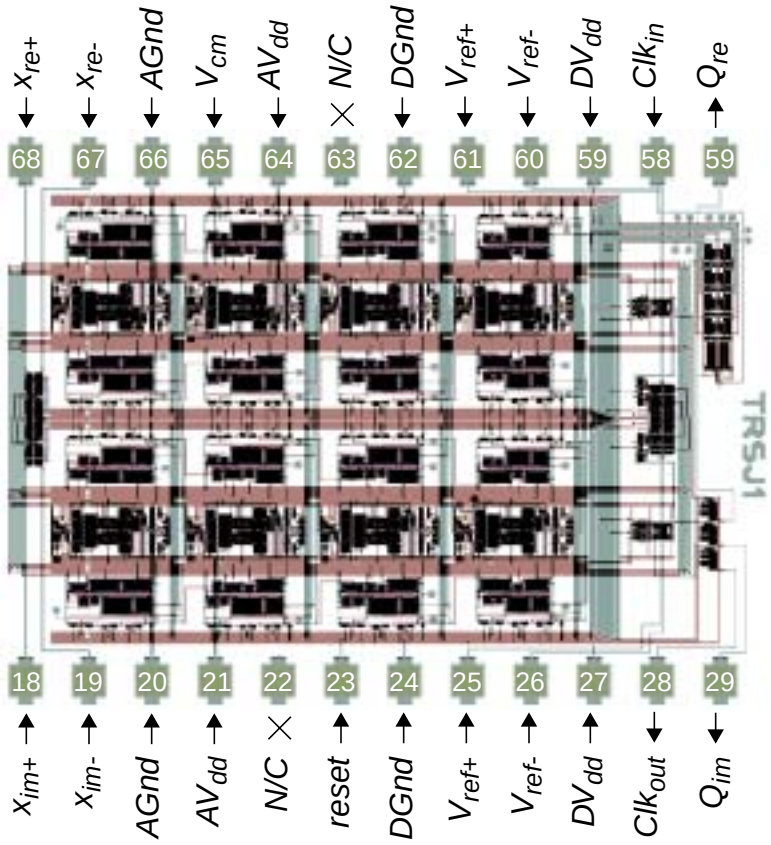


Fig. 7.3 Pin assignments for the 0.8-µm CMOS IC. The pads are numbered according to their connection in a 68-pin grid array package.

At the far left of the IC, the real and imaginary differential inputs enter from pads. At the far right, the modulator one-bit outputs and the clock input and output connect to pads. In the middle, lie connections for two versions of power and ground: *analog* power (including the analog common-mode voltage) and ground supply all non-switched circuitry, such as the amplifiers; *digital* power and ground supply the switched and digital circuitry, such as switches and comparators, the clock generator, and pad drivers.

The last connection of note is the reset pin (numbered 23), which is a logic input. When this input is tied high, all modulator integrating capacitors are discharged, allowing the user to either force the modulator to a known state upon start-up or to reset the modulator in case of instability.

7.2 The Test Configuration

7.2.1 The Printed-Circuit Board

A two-sided PCB, shown from its component side in Fig. 7.4, houses the quadrature bandpass ΔΣ modulator IC and support circuitry. Standard shielding and ground-plane techniques isolate the digital and analog portions of the IC [73].

An RF Mini-Circuits 0/90^o phase-splitter converts the incoming sinusoidal input into *I* and *Q* components, and 0/180^o phase-splitters convert each of these signals to fully-differential form. A 5-V voltage regulator supplies power to the analog portions of the IC, and, along with two resistor chains, sets the required bias voltages — 1-V and 4-V references, and a 2.5-V common-mode level.

A 10-MHz oscillator[1] (or a clock generator) drives the IC clock input, and a 74125 line-driver IC buffers the clock and bit-stream outputs.

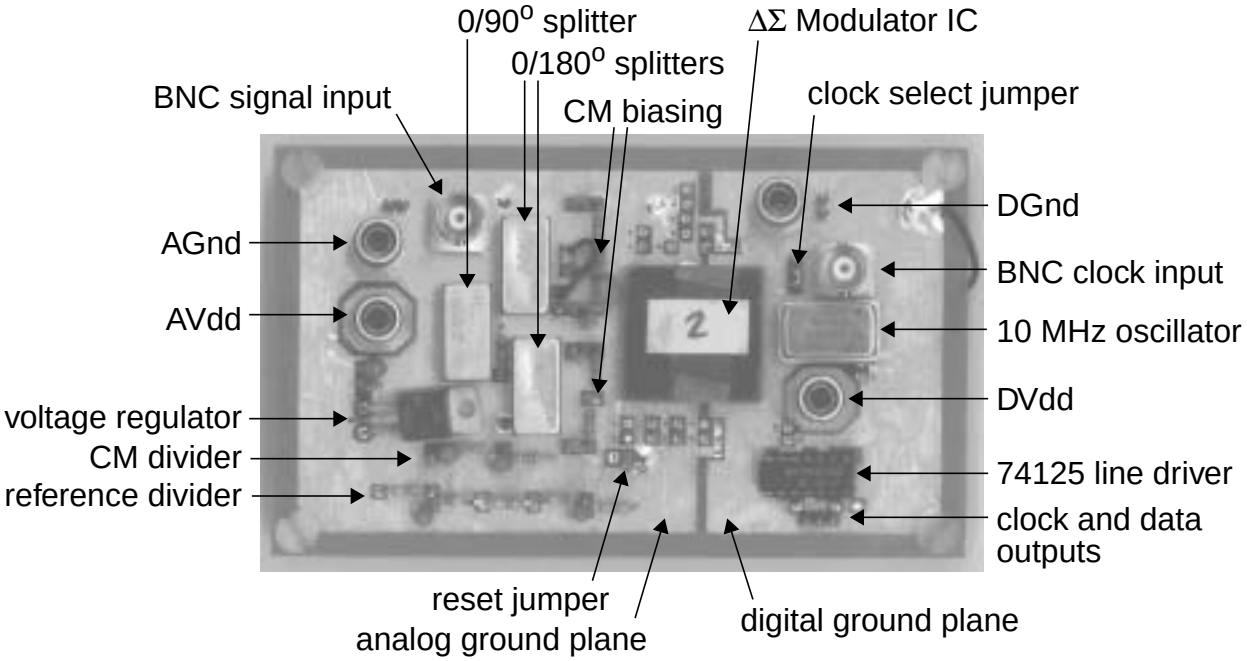


Fig. 7.4 Two-sided printed-circuit board housing the quadrature bandpass ΔΣ IC and support circuitry.

1. The 10-MHz sampling rate was chosen due to a limitation of the IC that precludes sampling at more than 11.5 MHz.

7.2.2 Data Collection and Analysis

Fig. 7.5 is a pictorial representation of the system in which the PCB is connected. A Rohde&Schwarz SMT03 signal generator provides the pure, in-band, sine-wave. To avoid spectral leakage in the data analysis, the input frequency is carefully selected to correspond to a minimal number of fft bins.

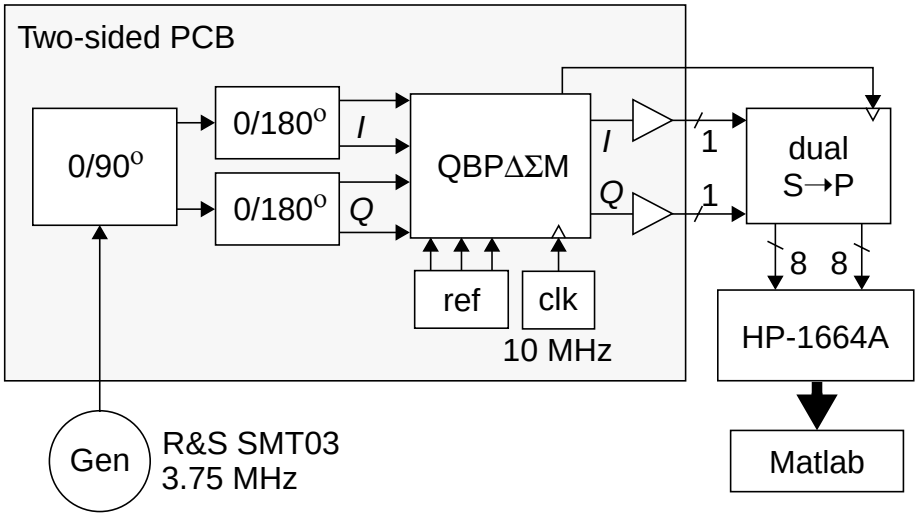


Fig. 7.5 Test configuration for characterization of the quadrature bandpass ΔΣ modulator (QBPΔΣM) IC.

A second circuit board contains two serial-to-parallel conversion blocks that buffer the single-bit *I* and *Q* streams from the modulator into 8-bit wide words for collection by an HP-1664A logic analyzer. Data is loaded into a Sun workstation for analysis using Matlab.

Once in Matlab, the digital *I* and *Q* bit-stream data is combined as *I*+j*Q*. This data is Hann windowed and fft'ed for analysis. Signal-to-noise-plus-distortion (SNDR) measurements are performed by comparing total in-band signal power to the in-band power of all noise and spurs. The bit-parallelization performed by the second circuit board facilitates collection of 64k data-bits per channel. A 64k-bin fft contains a sufficient number of in-band bins for accurate SNDR calculations.[1]

1. At a 10-MHz sampling rate and 200-kHz bandwidth, a 64k-bin fft contains over 1000 in-band bins. Without serial-to-parallel conversion, the 8k-bit data streams would produce only 126 in-band fft bins, for which signal-bin smearing makes it difficult to obtain accurate SNDR measurements.

7.3 Experimental Measurements

There are three levels of test for determining the operation of a ΔΣ modulator. The first is a simple examination of the time-domain bit-streams that emanate from the modulator. The second is an examination of the spectral content of the two-level modulator output stream on an analog spectrum analyzer. The last is a digital examination, using ffts, of the output bit-stream's spectral content. From first to last, the methods have increasing levels of usefulness at the expense of increased test complexity.

7.3.1 Bit-Stream Inspection

The first indication of a potentially operable ΔΣ modulator is that its two-level output stream — or in the case of the complex modulator, its two output streams — appears to randomly move between the high and low levels. If the outputs stay at one level only, the modulator channels are latched into one state, and the internal feedback is not operating properly. Fig. 7.6 shows simulated bit-streams for the quadrature modulator with a half-scale in-band tone input.

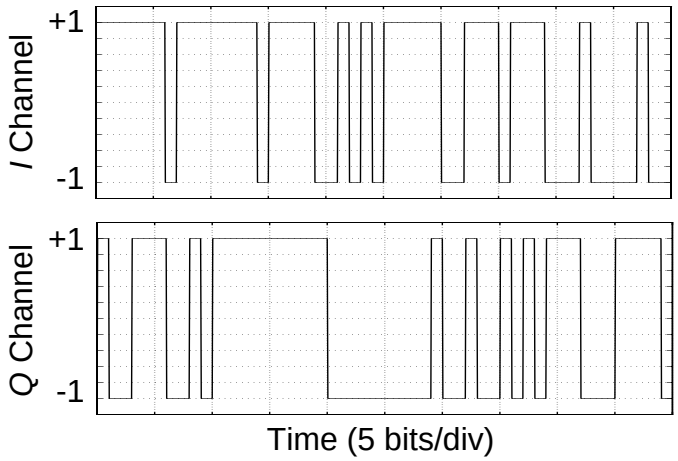


Fig. 7.6 Simulated bit-stream outputs from the ΔΣ modulator.

On an HP54510A oscilloscope, a single sweep captures similar looking streams for the IC, under similar test conditions. A plot of the real-channel output stream is shown in Fig. 7.7, along with a plot of the sample clock. The results provide confidence that the modulator, and its internal feedback, is operational, and also show that the data bits change value on the rising edge of the sample clock (thus, the data must be sampled on the clock's falling edge).

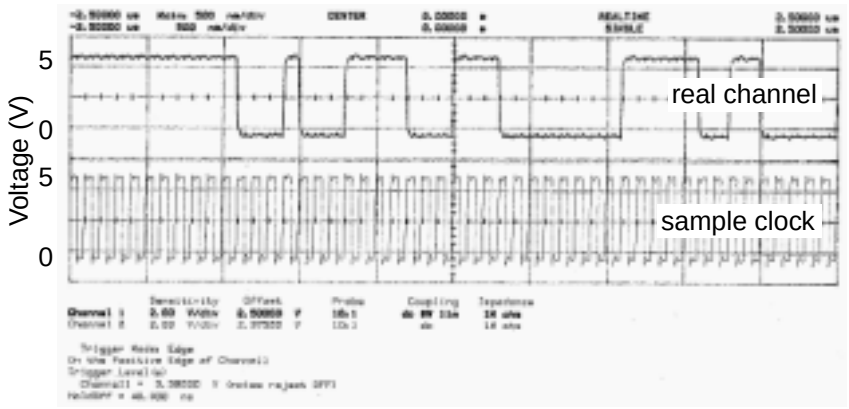


Fig. 7.7 IC real-channel bit-stream and clock signal (5 bits/division).

The IC's maximum clock rate can be determined from this test as well. The clock frequency is increased until the pattern of the output bit stream breaks down.[1] For this IC, both output bit streams latch into a random state once the clock frequency exceeds approximately 11.5 MHz.[2] For this reason, all subsequent tests are performed while driving the IC with a 10-MHz oscillator, which places the in-band region at 3.75 MHz.[3]

7.3.2 Analog Spectrum-Analyzer Plots

In the case of a real ΔΣ modulator, connecting the single output to an analog spectrum analyzer provides an estimate of the noise-shaping performance of a modulator. The spectrum analyzer, of course, does not treat the output stream as digital data, but rather as a two-level analog waveform. This limits the accuracy of the test, since the waveform has non-ideal rise and fall times, noise, etc. Integration of the in-band noise, by visual inspection, is also difficult to perform accurately. Nevertheless, the test provides a simple means for showing successful noise shaping.

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1. This is a "maximum output data rate" figure, that gives no regard to modulator noise-shaping performance.
2. It is conjectured that the maximum clock frequency is limited by the large parasitic clock-bus capacitances, which limit the integrity of clock signals that must traverse the IC.
3. Tests continue to measure performance across the full 200-kHz bandwidth. The lower clock rate thus reduces the expected performance of the IC, since the oversampling ratio is lower and the NTF is no longer optimal (because it was optimized for the higher oversampling ratio). Testing at the maximum 11.5-MHz rate would give slightly higher performance in the 200-kHz bandwidth, but proves less convenient.

In the case of a complex modulator, connecting one of the real- or imaginary-channel outputs, alone, to a spectrum analyzer, may not show a noise-shaped spectrum, since it is the combined complex output, I+jQ, which is noise shaped. In the case of the *3/1* modulator from Chapter 5, however, which had three in-band notches and one image-band notch, there exists a single notch at 3.75 MHz ($3f_s/8$) in the output spectrum of each channel. This single notch is created by the combination of the in-band *and* image-band notches.[1]

Fig. 7.8(a) shows the real-channel spectrum from a simulation (the imaginary spectrum looks similar). Fig. 7.8(b) shows the IC's real-channel spectrum, as observed on a spectrum analyzer. It, too, has a single notch at 3.75 MHz. Furthermore, the ratio between the top of the noise to the bottom of the notch is approximately 45 dB in each plot. Thus, this simple test provides a fast means for determining that the modulator does perform some noise shaping, and that it does so at the correct frequency.

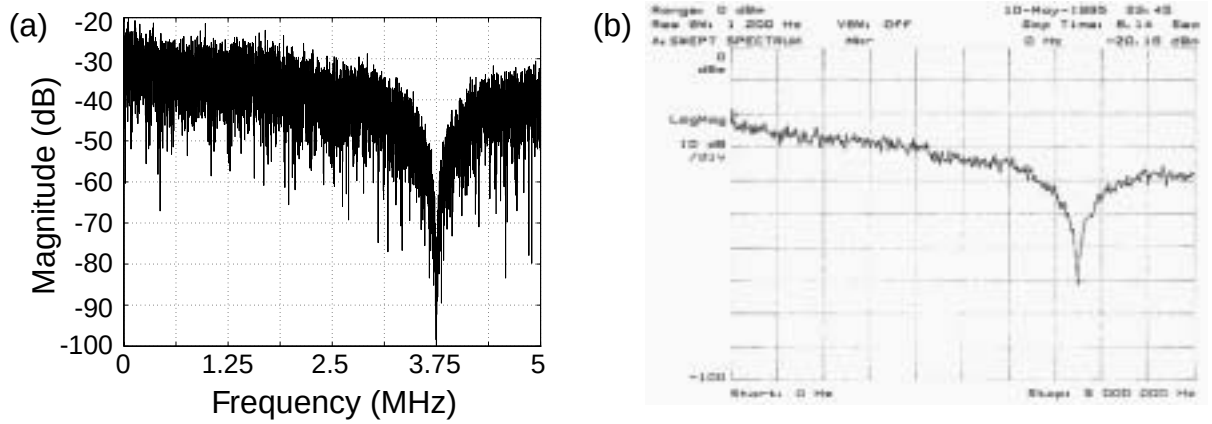


Fig. 7.8 (a) Simulated real-channel output spectrum. (b) The IC's real-channel output spectrum as observed on a spectrum analyzer.

7.3.3 Digital Bit-Stream Analysis

Ultimately, the bit-stream data is collected as *digital* information by a decimator. To determine the accuracy of the digital data, then, in representing the analog input within a narrow bandwidth, spectral analysis must be performed on the bit-stream outputs.

---

1. The *4/0* modulator from Section 3.2.4, which had four in-band and zero image-band notches, shows no such noise shaping in either of its channels' output spectra alone.

I. Spectra

An output spectrum, for zero input to the IC, is shown in Fig. 7.9(a). Note the wide-band noise-shaped region centered at 3.75 MHz — which is the in-band region — and the narrow notch at -3.75 MHz — which is the image-band region. Compare the noise-shaped output spectra with the NTF response shown in Fig. 5.5(b). Clearly the IC performs the desired *complex* noise shaping.

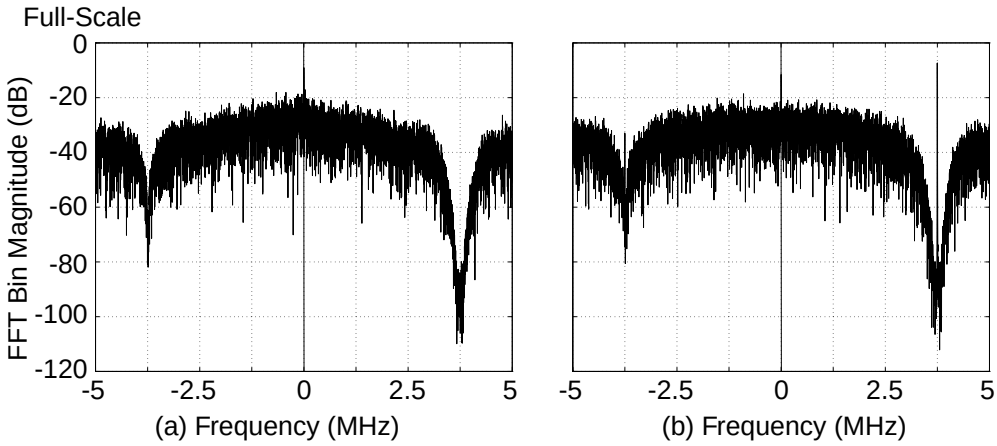


Fig. 7.9 Experimental 8k-bin output spectra. (a) Zero input. (b) -8-dBFS input.

A similar plot for an input 8-dB below modulator full-scale (-8 dBFS) is shown in Fig. 7.9(b). The noise-shaping is again evident, and in fact, functionality of the STF can also be determined. The input signal, a complex sinusoid positioned slightly above 3.75 MHz, has passed through to appear in the modulator output spectrum (Fig. 7.9(b)) with 20-dB gain (compared to the size of the input, which is not shown). This 20-dB in-band gain is expected from the STF response shown in Fig. 6.4 (i.e. after the 10x *A*-coefficient scaling).

II. SNDR

A plot of measured SNDR versus input amplitude is shown in Fig. 7.10. The modulator attains a dynamic range of 67 dB (11 bits) in 200-kHz bandwidth, increasing to 71 dB and 77 dB in the 100-kHz and 30-kHz bandwidths, respectively. Maximum SNDR is 62 dB (10 bits) in 200 kHz, 65 dB in 100 kHz, and 69 dB in 30 kHz.

The increase in SNDR with oversampling ratio is less than is expected for ideal third-order noise-shaping. This is the result of excess in-band noise which is shaped to less than third degree,

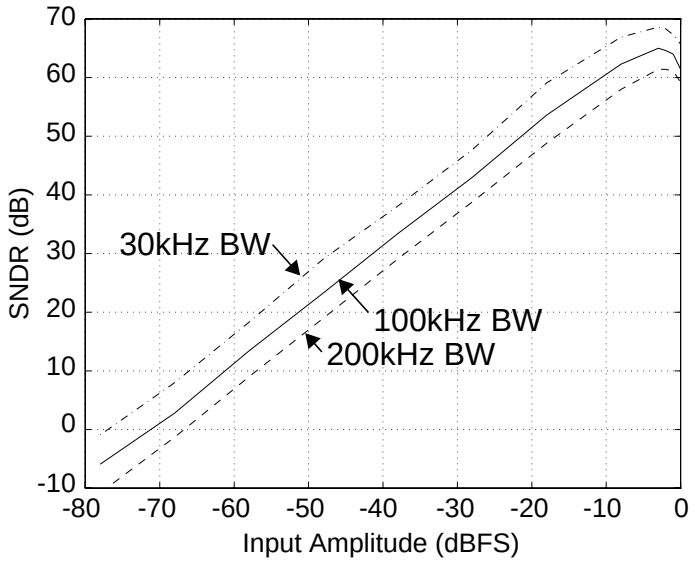


Fig. 7.10 Measured SNDR versus input amplitude.

and which is, in fact, nearly white (note the approximately 3-dB/octave increase in SNDR and dynamic range with oversampling ratio). This noise obscures the three distinct in-band notches expected from the ideal NTF of Fig. 5.5(b). Some of the excess in-band noise is due to circuit noise, and some is due to aliased noise caused by mismatch, which is discussed below.

7.3.4 Mismatch Effects

As described in detail in Chapters 4 and 5, mismatch, and particularly differential mismatch, causes two troublesome effects. First, image-band quantization noise, which tends to be large since it is in the out-of-band region of a $\Delta\Sigma$ modulator, aliases into the in-band region, reducing SNR. Second, any modulator input signals present in the image band alias to appear in the in-band region at the output, interfering with desired tones and causing an image-rejection problem.

I. Mismatch-Induced SNR Degradation

A portion of the excess in-band noise in Fig. 7.9 is caused by out-of-band quantization noise around –3.75 MHz aliasing into the desired frequency band around 3.75 MHz, by way of the mismatch-created INTF.

The magnitude of this effect can be inferred from Fig. 7.11, which is similar to Fig. 5.9(b), but re-simulated for a 10-MHz clock rate. The plot — which displays in-band NTFs and INTFs for 100 simulations of modulators subjected to random 0.5%-peak coefficient mismatch and

moderate amplifier non-ideality — shows that aliased quantization noise will, in a typical simulation, tend to fill in the outer two notches of the NTF, giving a slight SNR degradation and obscuring the outer two notches.

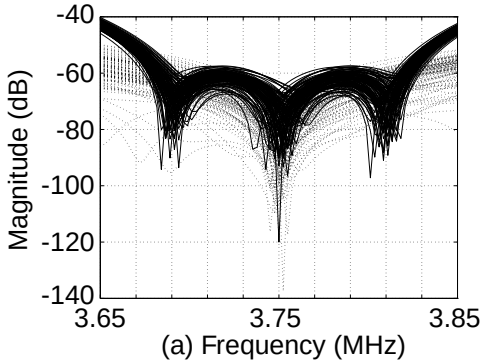


Fig. 7.11 NTFs and INTFs with random 0.5%-peak capacitor-ratio mismatch.

A histogram is shown in Fig. 7.12 for the *3/1* modulator. This is similar to Fig. 5.12(a), but is re-simulated for 100 non-ideal modulators sampled at 10 MHz. The 95th-percentile is 66.9 dB, which falls marginally above the measured 62-dB peak SNDR. Some of the difference can be attributed to in-band distortion products not seen in simulations, but most is likely attributable to circuit noise, coupling, etc. Regardless, the results are quite close to those expected.

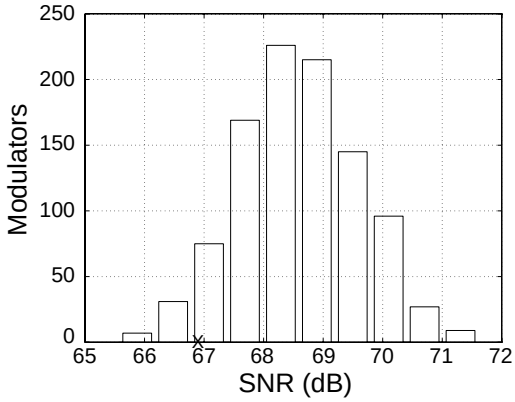


Fig. 7.12 Simulated modulator SNR, with mismatch, across a 200-kHz bandwidth at a 10-MHz sampling rate.

II. Mismatch-Induced IMR Degradation

The image-rejection effects of the ISTF are predicted, by simulation, in Fig. 7.13. The ideal STF has 20-dB in-band gain, whereas 100 non-ideal ISTFs have between -25-dB and -40-dB in-band gain. So, equal-sized complex-tone inputs injected at 3.75 MHz and at -3.75 MHz will both appear in-band at the output, with the latter being 45-dB to 60-dB smaller than the former. This gives a range of expected *image-rejection*.

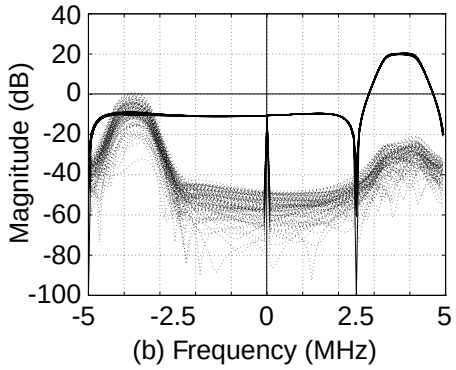


Fig. 7.13 Scatter plot of fifty STFs and ISTFs, with random 0.5%-peak coefficient mismatch.

In experimental tests, the major IMR limitation is not caused by the IC itself, but rather by the phase and amplitude imbalance of the phase-splitters used to drive the IC inputs. Specifications on these components list maximum amplitude/phase imbalances of 1.5-dB/3^{o} and 0.1-dB/2^{o} for the 90^{o} and 180^{o} splitters, respectively. Imbalances of even fractions of these values reduce image rejection to the neighborhood of 30 dB,[1] and cloud the performance of the IC. This matches measured values of just over 30 dB, and leaves the simulated range of 45 to 60 dB as a best estimate for the IMR of the IC itself.

III. Aliasing In-band Signals to the Image Band

Differential error also causes energy from the modulator input signal to appear in the image band at the output. As a result — although the input was a pure complex-exponential tone — there is not only the desired tone near 3.75 MHz in the output spectrum of Fig. 7.9(b), but also a smaller tone in the image band near -3.75 MHz. Fig. 7.13 shows that the random ISTFs have

1. For example, from Fig. 2.15 we see that 0.5 dB and 0.5^{o} of *I*/*Q*-input imbalance reduces image rejection to a mere 30.7 dB. The imbalance could be tuned out of the front-end circuitry used in the testing, but this was not attempted due to time considerations.

image-band gains between 0 and -20 dB — 20 to 40-dB less than the 20-dB in-band STF gain. Indeed, the image-band tone in Fig. 7.9(b) is about 25-dB smaller than the in-band tone. The image-band tone is insignificant regardless, since it is removed when the decimation filter eliminates all out-of-band frequency components.

7.3.5 Performance Summary

Power consumption for the 0.8-µm CMOS IC is 130 mW from 5-V supplies. Its performance is summarized in Table 7.1.[1] The 0.5-µm CMOS IC has not been characterized due to time constraints.

Table 7.1: IC Performance

Function	ADC for *I*/*Q* Inputs		
Sampling Rate	10 MHz		
Signal Frequency	3.75 MHz		
Signal Bandwidth	200 kHz (GSM)	100 kHz (CT2+)	30 kHz (IS-136, AMPS)
SNDR	62 dB	65 dB	69 dB
Dynamic Range	67 dB	71 dB	77 dB
Technology	0.8 µm CMOS		
Expected IMR[a]	45 - 60 dB		
Die Size	2.4 x 1.8 mm^2		
Power Dissipation	130 mW at 5 V		

a. IMR expected from modulator simulations with 0.5%-peak capacitor mismatch and moderate amplifier non-ideality.

1. These quadrature bandpass-ΔΣ-modulator IC performance results were the first presented to a world-wide audience [62 Jantzi]. An independent quadrature ΔΣ IC was fabricated during the same time-frame, and presented at an earlier workshop [49]; this IC achieved 48-dB SNR across a 10-kHz bandwidth, while sampling at 4 MHz.

7.4 Next Generation Possibilities

While the existing IC was carefully designed and laid out, and provides good performance — clearly demonstrating the theoretical concepts of the thesis — extensive IC testing, investigation, and analysis, invariably bring to mind thoughts of second-generation design. Modulator performance is affected by a wide assortment of factors, and each of them, in turn, can be dealt with in many ways and with varying levels of severity.

7.4.1 Floor-Plan Improvement

A relatively large proportion of the IC layout, shown in Fig. 7.1, is occupied by seven horizontal and six vertical buses; these are for analog signals, analog and digital power lines, and clock signals. The total bus area could be reduced if the differential-circuit symmetry were changed from the existing case — channels that are each internally symmetric about a horizontal line — to the case where each stage is symmetric about a vertical line.

The modified floor-plan would appear something like that shown in Fig. 7.14. It is clear that, for example, the digital bus real-estate is drastically reduced, since a single bus is shared between both channels. The one disadvantage of such a plan is that the cross-coupling between channels (necessary in a quadrature $\Delta\Sigma$ modulator) means that analog signals must pass over digital lines; shielding could help minimize this worry.

7.4.2 A Single-Feed-In STF

The fourth-order structure shown in Fig. 3.10 realizes a third-order STF numerator. This gives the freedom of positioning three independent STF zeros, which was ultimately done for the STF of the IC (shown in Fig. 6.4). The disadvantage is the considerable capacitance required, since each complex feed-in coefficient in the structure actually represents eight capacitors: one complex coefficient feeds into both stages, has a real and an imaginary portion, and is ultimately realized with differential circuitry.

By eliminating complex feed-in coefficients A_2 to A_4, twenty-four capacitors can be eliminated from the circuit. The remaining, single-feed-in, STF, has no finite zeros, and thus has a shape determined exclusively by its poles (which are also the NTF poles). In Section 5.1.1, the NTF poles were positioned in a butterworth arrangement around the in-band region. Thus, a

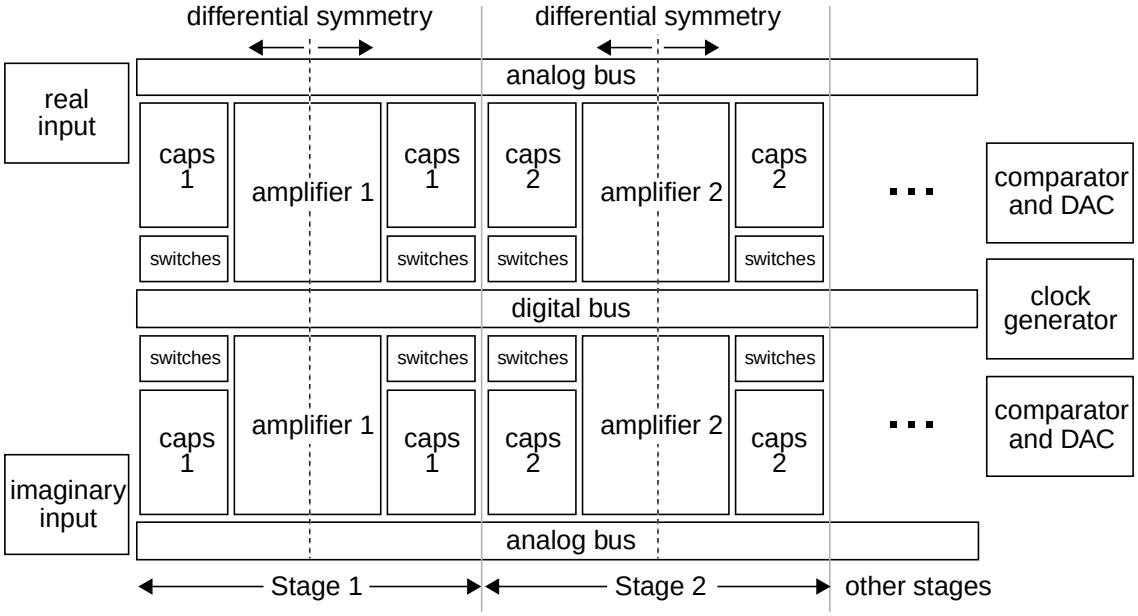


Fig. 7.14 Modified floor plan with reduced bus area.

single feed-in would be sufficient to achieve a butterworth STF response, if it were not for the single pole in the image band.

The in-band response caused by the image-band pole is nearly linear, and can easily be compensated for in the digital filter. If that is not a desirable option, two feed-in coefficients can be used (which still lowers the original capacitor count by sixteen) in order to realize one finite zero that can null the image-band pole. In either case, the total capacitor area is reduced, as is the capacitive load seen by some amplifiers.

The two suggested versions of the modified STF are shown in Fig. 7.15 below. Both are shown with 0-dB in-band gain.

With fewer feed-in capacitors, extra care could be taken to ensure their close matching — important since the feed-in capacitors (along with their integrating capacitors) are largely responsible for modulator IMR. Improved matching of the *A* coefficients could potentially increase modulator IMR to above the 60-dB level.

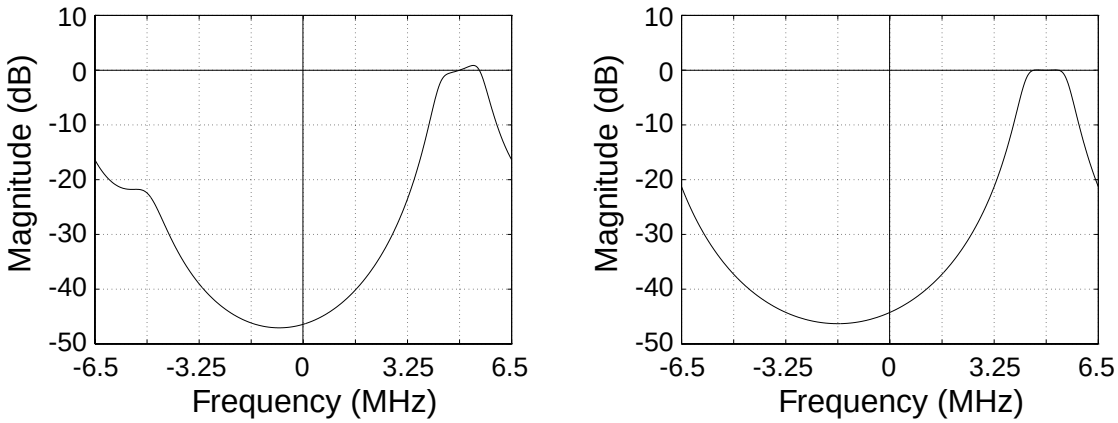


Fig. 7.15 (a) The single feed-in STF (no zeros). (b) The double feed-in STF, with one zero that nulls the image-band pole.

7.4.3 Miscellaneous Modifications

Other modifications, and general suggestions, for improved modulator performance are:

1. Faster amplifiers, such as class-AB amplifiers with exceptional slew-rate performance, combined with lower load capacitance, would allow an increase in the modulator sampling rate.
2. Off-chip control over the non-overlapping period of the two-phase clock would be a useful feature. Ensuring that there is sufficient non-overlap time across the entire IC is critical, and not guaranteed (because of clock skew along long buses).
3. Pad/pin-assignment should more fully isolate reference signals from noise sources, since noise on the references is not shaped by modulator feedback.
4. An extra version of analog power should be used for the switches connected to analog circuitry. This would give three versions of power: one for continuous-time analog circuitry (amplifiers), one for switched analog circuitry (switches and comparators), and one for digital support circuitry (clock generator and pad drivers).
5. Shielded (NWell) tubs should house the capacitor arrays, in order to prevent noise from coupling into sensitive analog nodes.
6. Analog buses could be shielded above and below by other grounded layers.

7.5 Summary

This chapter described all aspects of the IC characterization. Die microphotographs were shown and the pad assignment described. A circuit board was designed which is suitable for testing of a quadrature $\Delta\Sigma$ modulator.

Various levels of test were conducted which showed that the IC performs the desired complex noise shaping. Clocked at 10 MHz, the IC converts narrow-band 3.75-MHz *I* and *Q* inputs, attaining 62-dB maximum SNDR and 67-dB dynamic range in 200-kHz (GSM) bandwidth. Thus, the IC is a true 10-bit A/D converter suitable for converting complex input signals. Its power consumption is 130 mW at 5 V; its die size is 2.4 x 1.8 mm^2.

Improvements were suggested for a next-generation IC implementation.

CHAPTER 8

Closing Remarks

This Chapter summarizes the thesis, highlights its contributions, and offers suggestions for future research.

The first significant contribution of the thesis was the proposal of a low-IF receiver architecture, which, with the use of modern quadrature image-reject mixers and strategic IF placement, offers a viable solution for digital and monolithic receiver implementation. A quadrature variant of a bandpass delta-sigma ($\Delta\Sigma$) modulator was proposed, to provide a means for performing high-resolution analog-to-digital modulation on narrow-band complex inputs — such as those present in the back-end of the low-IF receiver. All aspects of the quadrature $\Delta\Sigma$ modulator were investigated — transfer functions; structures; mismatch effects, and methods to limit their severity; a switched-capacitor architecture; circuits; IC layout and testing — ultimately resulting in the realization of a working prototype IC. As a side benefit, considerable insight was garnered into the operation of complex signals, systems, and filters.

8.1 Thesis Summary

Chapter 2 provided a summary of the state-of-the-art of bandpass delta-sigma modulation, complex signals and complex filters, and radio-receiver spectra and architectures, and highlighted some of the current goals in communication-microelectronics research. The presentation of the material on complex signals and filters was meant to minimize the confusion caused by this esoteric topic.

Chapter 3 presented a new low-IF receiver architecture that provides a viable solution for realizing single-chip radio receivers. Furthermore, a new quadrature bandpass ΔΣ modulator was proposed as a tailor-made fit for the low-IF receiver. Quadrature ΔΣ modulators were investigated, and a general design methodology presented. Decimation and anti-alias filtering were discussed.

Chapter 4 examined the effects of mismatch in complex systems, first showing how differential mismatch affects a complex bandpass filter. This material offered intuition into the transfer functions created by differential mismatch, and allowed a investigative leap to be made into the more severe effects of mismatch on ΔΣ modulators.

Chapter 5 described an improved modulator design which proved quite robust. The design trade-offs and design procedure for such modulators were described in detail. The improved modulator easily out-performed a pair of standard bandpass modulators for the conversion of complex input signals in the face of mismatch.

Chapter 6 described the steps undertaken to realize a silicon implementation of the improved quadrature bandpass ΔΣ modulator. The overall switched-capacitor architecture was presented, constituent circuitry was discussed, and simulations presented. A code-driven layout methodology was presented, which was proven useful by its generation of modulator layouts for two dissimilar fabrication processes.

Chapter 7 described the experimental testing of the integrated circuit. The IC was shown to act as a true 10-bit analog-to-digital converter suitable for operating on complex input signals, and is proof, in silicon, of the propositions of the earlier theory.

Many of the techniques presented in this thesis, and its associated papers, have been acted upon by other researchers. These range from the low-IF architecture presented in Chapter 2 [49] (which was also proposed independently [42]), to the quadrature ΔΣ modulator presented in Chapter 3 [48][49][50] and the mismatch-battling technique presented in Chapter 5 [49]. The impact begins to influence industry as well, as next-generation transceiver architectures are examined for cellular telephony.

8.2 Suggestions for Future Work

Modulator image rejection is perhaps the performance specification that most merits further attention. Based on the discussion of single-feed-in STFs in Chapter 7, it is conceivable that very careful layout could produce modulators with image rejection on the order of 60 dB. Beyond that level, however, other techniques may be needed.

Swapping capacitors between channels, and between single-ended half-circuits — in a type of dynamic-element matching technique — might prove fruitful [50]. Post-modulator correction of *I/Q* errors in the DSP merits further investigation [49]. Other structures which produce STF bandpass regions with low amplitude and phase sensitivity might also prove beneficial — LC-ladder-simulation structures spring to mind.

New structures for the quadrature modulator in general, could be investigated, with the goal of reduced area and power, and increased speed and performance. Several suggestions for a next-generation IC were presented in detail in Chapter 7. Switched-capacitor ΔΣ modulators in the literature have reached sampling rates in the 50-MHz range [11][74], and even an impressive 160 MHz [17]. Similar circuit techniques could be used to increase the input frequency, bandwidth, or SNR — or some combination of the three — of the quadrature modulator. Implementing the modulator in faster technologies would help in this vein.

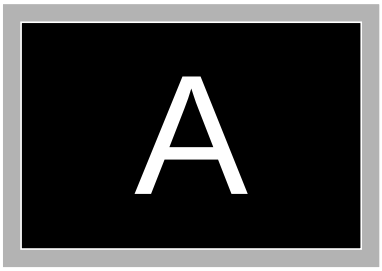
Circuits could be optimized for low power — and run with supplies of 3 V or lower — helping to realize the goal of a low-power transceiver. In a similar fashion to traditional ΔΣ modulators, higher-order noise-shaping functions, or finer-resolution internal quantizers and feedback DACs, could also be used to improve modulator performance. Due to the two-path nature of a quadrature modulator, new techniques may be needed to ensure necessary levels of linearity when using multi-bit quantizers and DACs.

Ultimately, the modulator is to be part of a complete transceiver, so a useful exercise would be to construct a prototype RF transceiver (or receiver) that utilizes a high-performance quadrature bandpass ΔΣ modulator. Investigation into the proper partitioning of image-rejection amongst the receiver blocks, and into the choice of system frequencies, would be useful.

Applications for quadrature ΔΣ modulators outside of the portable-communications theatre (instrumentation systems, for example) could be investigated. Quadrature ΔΣ digital-to-analog

modulators — the twins of the A/D modulators presented herein — could find use in the data-communications field. Complex modulators — such as QAM modulators used in cable modems — might be able to capitalize on the properties of a quadrature D/A converter.

APPENDIX



Structure Transfer Functions

The fourth-order structure from Fig. 3.10 is re-drawn in Fig. A.1. The modulator input feeds into each stage through the complex *A* coefficients, which set three zeros of the complex STF. The zeros of the complex NTF are set by the complex pole (integrator) positions, and thus by the *p* coefficients. The modulator outputs feed back into the four stages through the *B* coefficients, which set the positions of the NTF and STF poles.

A.1 The Noise and Signal Transfer Functions

A fourth-order NTF and an STF with a third-order numerator and fourth-order denominator (which is equal to the NTF denominator) are designed as outlined in Chapters 3 and 4, and Appendix B. They can be represented as listed in Eqs. (A.1) and (A.2), respectively. Of course, the modified STFs from Section 7.4.2 would have fewer numerator terms than listed here — either α_0 alone for the single-feed-in STF, or both α_0 and α_1 for the dual-feed-in STF.

Noise Transfer Function:

$$H(z) = \frac{Y(z)}{N(z)} = \frac{(z-p_4)(z-p_3)(z-p_2)(z-p_1)}{z^4 + \beta_3 z^3 + \beta_2 z^2 + \beta_1 z + \beta_0}. \tag{A.1}$$

Signal Transfer Function:

$$G(z) = \frac{Y(z)}{X(z)} = \frac{\alpha_3 z^3 + \alpha_2 z^2 + \alpha_1 z + \alpha_0}{z^4 + \beta_3 z^3 + \beta_2 z^2 + \beta_1 z + \beta_0}. \tag{A.2}$$

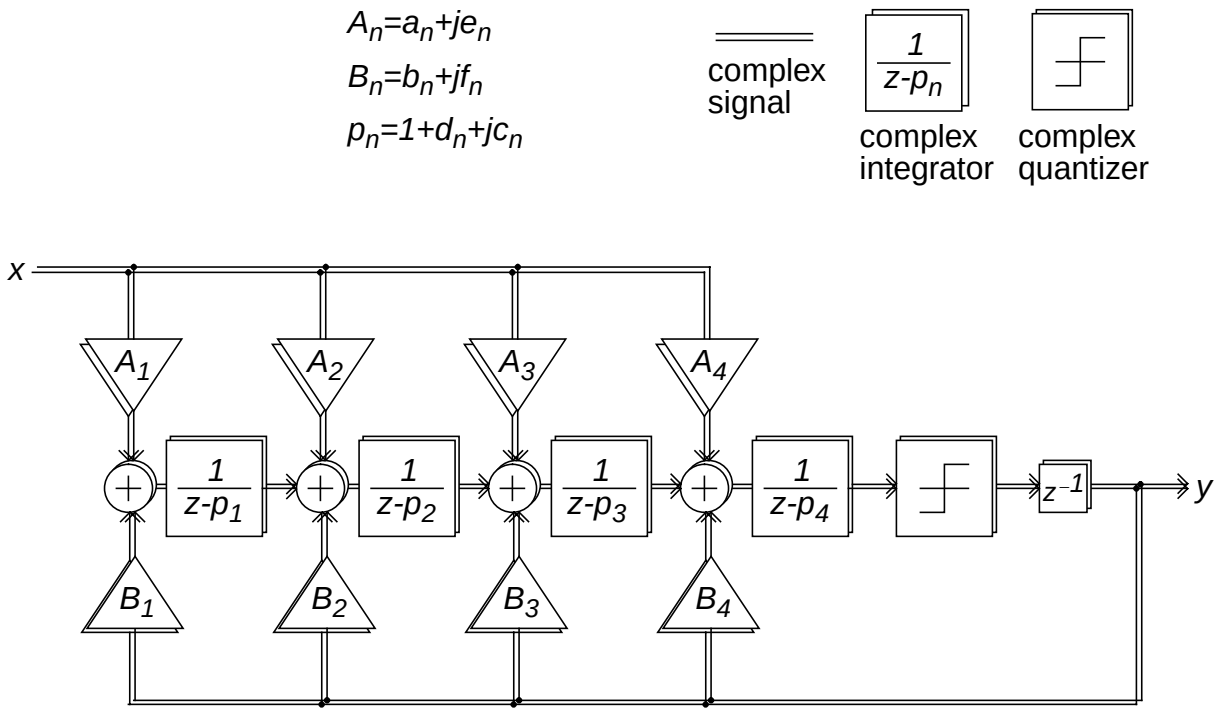


Fig. A.1 General structure for a fourth-order quadrature ΔΣ modulator.

A.2 Coefficient Determination

It is a simple matter to match desired transfer-function coefficients with structure coefficients — remembering that all are, in general, complex. These coefficients then set the capacitor ratios used in the circuit implementation.

The *d* and *c* coefficients, which set the numerator of the NTF, are trivial to determine, since they directly position the real and imaginary coordinates of the NTF zeros as:

$$p_1 = 1 + d_1 + jc_1, \quad \text{(A.3)}$$

$$p_2 = 1 + d_2 + jc_2, \quad \text{(A.4)}$$

$$p_3 = 1 + d_3 + jc_3, \text{ and} \quad \text{(A.5)}$$

$$p_4 = 1 + d_4 + jc_4. \quad \text{(A.6)}$$

The feed-back coefficients, B_1 - B_4, set the NTF and STF poles. They are determined as:

$$B_4 = -(p_4 + p_3 + p_2 + p_1) - \beta_3, \quad \text{(A.7)}$$

$$B_3 = B_4(p_3 + p_2 + p_1) + (p_4p_3 + p_4p_2 + p_4p_1 + p_3p_2 + p_3p_1 + p_2p_1) - \beta_2, \quad \text{(A.8)}$$

$$B_2 = -B_4(p_3p_2 + p_3p_1 + p_2p_1) + B_3(p_2 + p_1) - (p_4p_3p_2 + p_4p_3p_1 + p_4p_2p_1 + p_3p_2p_1) - \beta_1, \text{ and} \quad \text{(A.9)}$$

$$B_1 = B_4p_3p_2p_1 - B_3p_2p_1 + B_2p_1 + p_4p_3p_2p_1 - \beta_0, \quad \text{(A.10)}$$

where each *B* coefficient is complex:

$$B_N = b_N + jf_N. \quad \text{(A.11)}$$

The feed-in coefficients, A_1 - A_4, set the three STF zeros. They are determined as:

$$A_4 = \alpha_3 \quad \text{(A.12)}$$

$$A_3 = A_4(p_3 + p_2 + p_1) + \alpha_2, \quad \text{(A.13)}$$

$$A_2 = -A_4[p_3p_2 + p_3p_1 + p_2p_1] + A_3(p_2 + p_1) + \alpha_1, \text{ and} \quad \text{(A.14)}$$

$$A_1 = A_4p_3p_2p_1 - A_3p_2p_1 + A_2p_1 + \alpha_0, \quad \text{(A.15)}$$

where each *A* coefficient is complex:

$$A_N = a_N + je_N. \quad \text{(A.16)}$$

APPENDIX

B Modulator Design Examples

This Appendix summarizes the design procedure for the two major quadrature ΔΣ modulators discussed within the thesis. Design of the *4/0* modulator is only moderately more involved than standard bandpass ΔΣ modulator design, whereas the design of the *3/1* modulator has the added twist of an image-band pole-zero pair.

B.1 Specifications

The frequency and *z*-plane specifications for the modulators are listed in Table B.1. These specifications provide bandwidth suitable for the GSM specification [45], while placing the input frequency at an IF that avoids potential near-dc and $f_s/4$ problems.

Table B.1: Modulator Specifications

Specification	Symbol	Frequency	Symbol	Normalized Angular Frequency (radians)
sampling rate	f_s	13 MHz	θ_s	2π
center frequency	f_c	4.875 MHz	θ_c	$3\pi/4$
bandwidth	f_b	200 kHz	θ_b	$\pi/32$

B.2 Modulator-*4/0* Transfer-Function Design

B.2.1 Lowpass-Prototype NTF

A real, fourth-order, lowpass prototype was designed using filtorX [55 Jantzi], closed-form expressions [56], a ΔΣ design toolbox [57], and MATLAB [58] — to meet the listed specifications. The poles are positioned in the butterworth configuration that gives a peak out-of-band gain of 4 dB.

In the ΔΣ design toolbox, for example, the command line entry is:

```
> lpp40 = synthesizeNTF(4, 64, 1, 10^(4/20), 0)
```

The first argument of the `synthesizeNTF` command requests a fourth-order NTF, the second defines the desired oversampling ratio, the third requests optimized in-band NTF zeros, the fourth sets the peak out-of-band NTF gain at 4 dB, and the last requests a design centered at dc.

Note that the requested oversampling ratio for the lowpass prototype NTF is 64 — not 32, as might be expected from the normalized bandwidth of $\theta_b = \pi/32$ — since the entire bandwidth of the lowpass modulator is utilized once the real NTF is rotated to become a complex one.

The prototype NTF poles and zeros are listed in Table B.2 and plotted in Fig. B.1.

Table B.2: *4/0*-NTF LPP Pole-Zero Locations

Singularity	Zero	Pole
1	0.99986 + 0.01669j	0.8265 + 0.2794j
2	0.99986 - 0.01669j	0.8265 - 0.2794j
3	0.99911 + 0.04226j	0.7164 + 0.0959j
4	0.99911 - 0.04226j	0.7164 - 0.0959j

B.2.2 Shifting to Complex Frequencies

The lowpass-prototype NTF was frequency shifted to an angular center frequency of $3\pi/4$, by multiplying all pole and zero locations by $e^{j3\pi/4}$. This results in the pole-zero plot of Fig. B.2(a) and the magnitude response of Fig. B.2(b), which includes an expanded view of the in-band region. Note that the poles and zeros have no complex-conjugates and that the magnitude

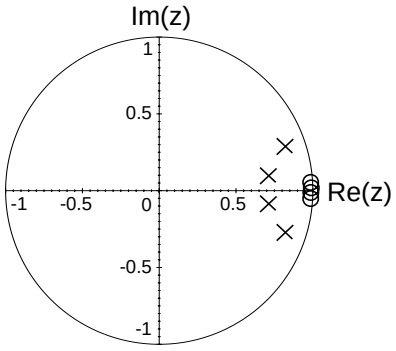


Fig. B.1 Fourth-order lowpass-prototype NTF pole-zero constellation.

response is not symmetric about dc (i.e. the transfer function is complex). The pole-zero locations are summarized in Table B.3.

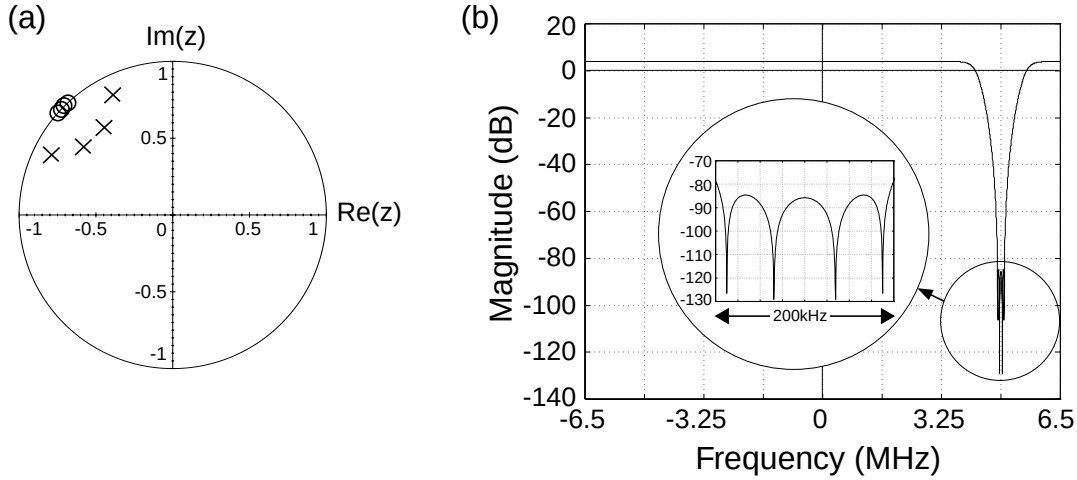


Fig. B.2 Fourth-order complex noise transfer function. (a) Pole-zero constellation. (b) Magnitude response, with an inset showing the 200-kHz wide in-band region.

Table B.3: *4/0*-Modulator NTF Pole-Zero Locations

Singularity	Zero	Pole
1	-0.71881 + 0.69521j	-0.78199 + 0.38687j
2	-0.69521 + 0.71881j	-0.38687 + 0.78199j
3	-0.73636 + 0.67659j	-0.57442 + 0.43877j
4	-0.67659 + 0.73636j	-0.43877 + 0.57442j

B.2.3 The Signal Transfer Function

The STF shares poles with the NTF in the structure shown in Fig. 3.10, which saves on hardware and presents no significant limitations. Four complex inputs to the structure allow three STF zeros to be positioned.

A possible STF pole-zero plot is shown in Fig. B.3(a), and its magnitude response in Fig. B.3(b). This STF has an in-band gain of 0 dB and out-of-band rejection of more than 40 dB. A complex bandpass filtering function is achieved by positioning zeros at $z = j$ (3.25 MHz), $z = -1$ (±6.5 MHz), and $z = 1/\sqrt{2} - j/\sqrt{2}$ (-1.625 MHz). The in-band STF has magnitude flat to within 0.04 dB and phase linear to within $\pm 0.02°$. The pole-zero locations are tabulated in Table B.4.

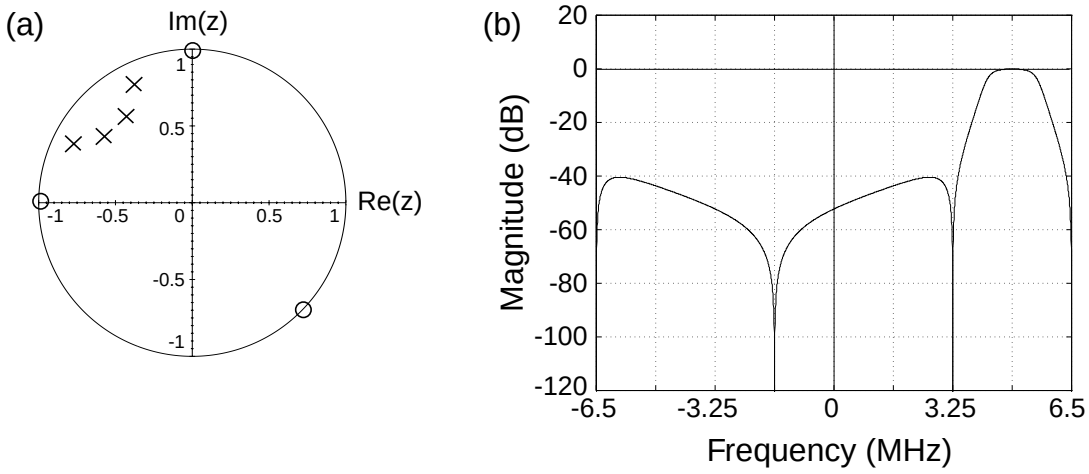


Fig. B.3 The signal transfer function (STF). (a) Pole-zero constellation. (b) Magnitude response.

Table B.4: *4/0*-Modulator STF Pole-Zero Locations

Singularity	Zero	Pole
1	j	-0.78199 + 0.38687j
2	-1	-0.38687 + 0.78199j
3	0.70711 - 0.70711j	-0.57442 + 0.43877j
4		-0.43877 + 0.57442j

B.3 Modulator-*3/1* Transfer-Function Design

B.3.1 Some Useful Equations

The design of this modulator is different from that above, because it is known *a priori* that an image-band pole-zero pair will be added to the three in-band pole-zero pairs. Thus, when the third-order transfer function is designed, its out-of-band gain must be limited so that the addition of the image-band pole and zero increases the overall gain to only 4 dB, for example.

A set of equations can be derived to relate the position of the image-band pole to the peak gain allowable in the third-order NTF. As was discussed in Chapter 5, the expectation is that an image-band pole closer to the unit-circle will allow a more aggressive third-order in-band NTF, and vice-versa.

The derivation follows several steps, which rely on Fig. B.4 and are listed below.

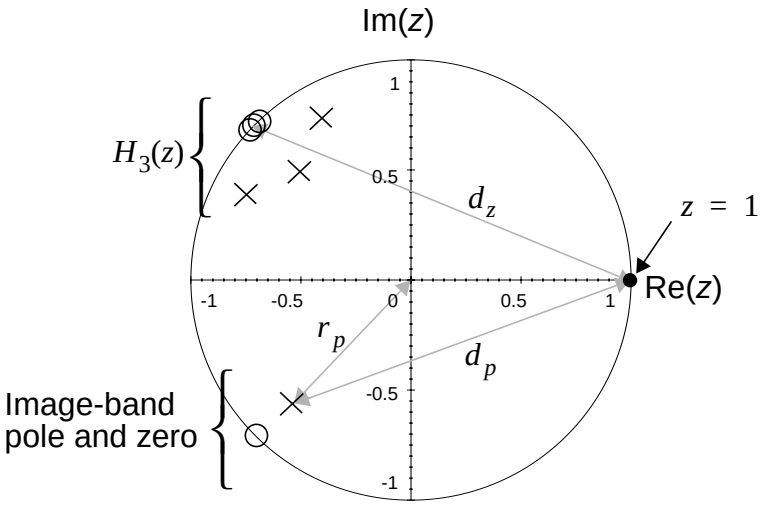


Fig. B.4 Determining image-band pole placement.

1. Assume the maximum out-of-band gain of $H_3(z)$ — which is called $\hat{H}_3$, for convenience — occurs at $z = 1$, which is a reasonable approximation since the butterworth pole placement makes the NTF-curve very flat out-of-band.

2. A peak out-of-band gain, $\hat{H}$, of 4 dB (1.585) is ultimately desired for the full (fourth-order) NTF, $H(z)$.

3. The distance from $z = 1$ to the image-band zero (which is the same as the distance from $z = 1$ to the centre in-band zero) is

$$d_z = \sqrt{\left(1 + \frac{1}{\sqrt{2}}\right)^2 + \left(\frac{1}{\sqrt{2}}\right)^2} = 1.848 . \qquad \text{(B.1)}$$

4. The distance from the image-band pole to $z = 1$ — which is labelled as d_p — is related to the pole radius, r_p, by the equation:

$$d_p^2 = \left(1 + \frac{r_p}{\sqrt{2}}\right)^2 + \left(\frac{r_p}{\sqrt{2}}\right)^2 = r_p^2 + \sqrt{2} r_p + 1 \text{ , so that:} \qquad \text{(B.2)}$$

5. The radius of the image-band pole is related to the pole's distance from $z = 1$, by the equation (using the quadratic formula on Eq. (B.2), and choosing the solution that gives a positive pole radius):

$$r_p = \frac{-\sqrt{2} + \sqrt{2 - 4(1 - d_p^2)}}{2} = \frac{-1 + \sqrt{1 - 2(1 - d_p^2)}}{\sqrt{2}} . \qquad \text{(B.3)}$$

6. $H(z)$ is constructed from $H_3(z)$ by adding the image-band pole and zero. Thus, the maximum gain of $H(z)$, $\hat{H}$ — which is again assumed to occur at $z = 1$ — is related to $\hat{H}_3$ by:

$$\hat{H} = \hat{H}_3\left(\frac{d_z}{d_p}\right). \qquad \text{(B.4)}$$

Eqs. (B.1) and (B.4), along with Point 2, allow the maximum out-of-band gain of the third-order transfer function to be related to the distance of the image-band pole from $z = 1$:

$$\hat{H}_3 = d_p\left(\frac{\hat{H}}{d_z}\right) = d_p\left(\frac{1.585}{1.848}\right) = 0.858 d_p . \qquad \text{(B.5)}$$

If this result is substituted into Eq. (B.3), a useful result appears:

$$r_p = \frac{-1 + \sqrt{1 + 2(1.358\hat{H}_3^{\,2} - 1)}}{\sqrt{2}}, \tag{B.6}$$

which can be rearranged as:

$$\hat{H}_3 = \sqrt{\frac{\frac{(\sqrt{2}r_p + 1)^2 - 1}{2} + 1}{1.358}} = \sqrt{\frac{2\left(r_p + \frac{1}{\sqrt{2}}\right)^2 + 1}{2.716}}. \tag{B.7}$$

Eqs. (B.6) and (B.7) are the desired result: the latter says that, for example, for a design with an image-band pole at radius 0.77, the third-order NTF must be designed with a peak out-band gain of 1.405 (2.96 dB). In actual fact, Eq. (B.7) is used as a (very close) starting point, and then the magnitude and angle of the image-band pole are adjusted slightly, as necessary.

As expected, the equation does predict that more aggressive third-order NTFs can be designed for poles close to the unit circle. For example, $\hat{H}_3$ can be calculated for a value of $r_p = 1$, which is the limiting case of an image-band pole on the unit circle, cancelling exactly with its zero. The result is $\hat{H}_3 = 1.585$ (4 dB), meaning that the third-order transfer function can be designed with the full 4-dB out-of-band gain (as opposed to, say, the 2.96-dB limit for a pole radius of 0.77), since the self-cancelling image-band pole-zero pair will not affect it.

The other limiting case is the minimum-allowable image-band pole radius, which defines how aggressive the image-band (and INTF) notch becomes. If the image-band pole moves too close to the unit circle, there is no stable third-order NTF design that will combine with the image-band root pair to give 4-dB out-of-band gain. Since the minimum out-of-band gain possible for the third-order NTF is unity, the minimum image-band pole radius can be determined from Eq. (B.6) by substituting $\hat{H}_3 > 1$. The result is $r_p > 0.219$.

Thus, the image-band pole can be placed at a radius from unity to about 0.22, with the corresponding in-band NTF worsening from the best possible, to a nearly useless one. Of course, as discussed thoroughly in Chapter 5, it is actually the *interaction* between the resulting NTF and INTF, in the face of mismatch, that determines the quality of a design.

B.3.2 The Third-Order Lowpass Prototype

A real, third-order, lowpass prototype was designed to meet the specifications listed in Section B.2.1, but for less out-of-band gain. Based on simulations, which show a desired image-band pole radius of 0.77,[1] the third-order NTF was designed for peak out-of-band gain of 1.4. The resulting prototype-NTF poles and zeros are listed in Table B.5 and plotted in Fig. B.5.

Table B.5: *3/1*-NTF LPP Pole-Zero Locations

Singularity	Zero	Pole
1	0.99930 + 0.03743j	-0.8110 + 0.2446j
2	0.99930 - 0.03743j	-0.8110 + 0.2446j
3	1	0.7106

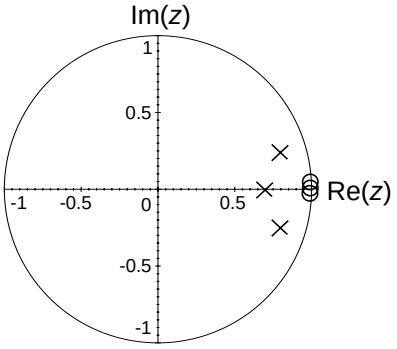


Fig. B.5 Third-order lowpass-prototype NTF pole-zero constellation.

B.3.3 Shifting to Complex Frequencies

This lowpass-prototype function was frequency shifted to an angular center frequency of $\theta = 3\pi/4$ — by multiplying all pole and zero locations by $e^{j3\pi/4}$ — resulting in the poles and zeros plotted in Fig. B.6.

1. Obviously there is some iteration here: a full NTF is designed (based on some image-band pole radius), and the design is simulated for performance in the face of mismatch. Other image-band pole radii are then chosen, corresponding NTF designs repeated, and resulting simulations examined. The “best” such design herein was shown to have a pole-radius of 0.77 (see Section 5.1).

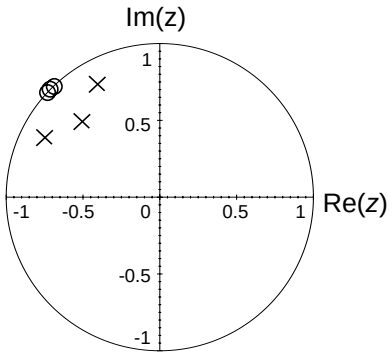


Fig. B.6 Third-order complex NTF pole-zero constellation.

B.3.4 Image-Band Roots

A single image-band notch was added at $z = -1/\sqrt{2} - j/\sqrt{2}$, for reasons discussed in Chapter 5. To maintain proper NTF characteristics in the presence of the added zero, the image-band pole was added nearby. The chosen pole has a radius of 0.77, placed at an angular frequency of -0.745π (i.e. very close to $-3\pi/4$, as was assumed throughout Section B.3.1).

The NTF pole-zero plot is shown in Fig. B.7(a), and its magnitude response is shown in Fig. B.7(b), which includes an expanded view of the in-band region. Its poles and zeros are tabulated in Table B.6. The peak NTF out-of-band gain is 4 dB, as required.

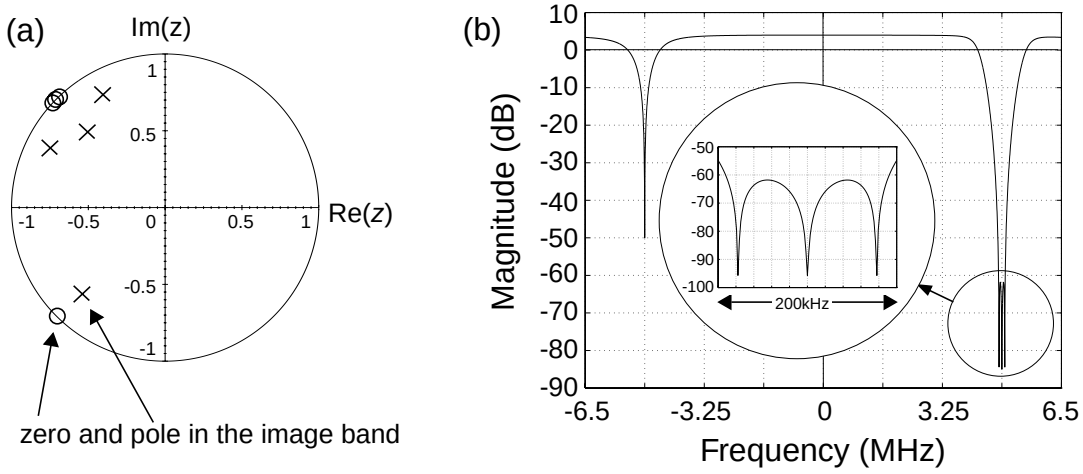


Fig. B.7 The *3/1* NTF. (a) Pole-zero constellation. (b) Magnitude response.

Table B.6: *3/1*-Modulator NTF Pole-Zero Locations

Singularity	Zero	Pole
1	-0.73308 + 0.68014j	-0.7464 + 0.4005j
2	-0.68014 + 0.73308j	-0.4005 + 0.7464j
3	-0.70711 + 0.70711j	-0.5025 + 0.5025j
4	-0.70711 - 0.70711j	-0.5359 - 0.5530j

B.3.5 The *3/1*-Modulator STF

The STF designed for the updated pole configuration is shown in Fig. B.8. As seen in the pole-zero plot of Fig. B.8(a), one STF zero is positioned over the image-band pole to null its response, leaving two zeros available to effect shaping of the input spectrum. In this case, a complex bandpass filtering function is achieved by placing a zero at $z = j$ (3.25 MHz) and another at $z = -1$ (±6.5 MHz).

The STF magnitude response is shown in Fig. B.8(b) and its pole-zero locations are tabulated in Table B.7. It has unity in-band gain and 30-dB out-of-band rejection. The in-band STF has magnitude flat to within 0.03 dB and phase linear to within ±0.02°.

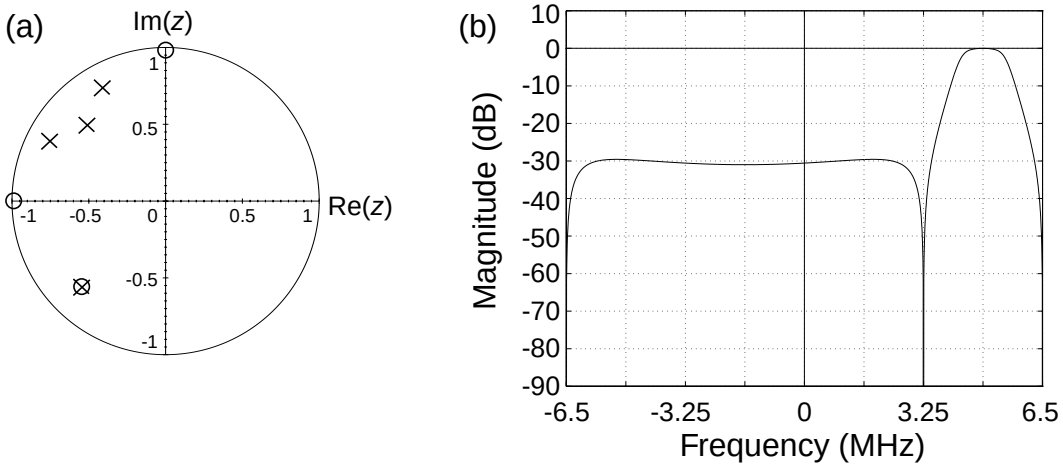


Fig. B.8 The new STF. (a) Pole-zero constellation. (b) Magnitude response.

Table B.7: *3/1*-Modulator STF Pole-Zero Locations

Singularity	Zero	Pole
1	-1	-0.7464 + 0.4005j
2	j	-0.4005 + 0.7464j
3	-0.5359 - 0.5530j	-0.5025 + 0.5025j
4		-0.5359 - 0.5530j

B.4 Modulator Coefficients

Once the NTF and STF for the modulator are known, the coefficients for the structure of Fig. 3.10 can be determined. The necessary relationships are listed in Appendix A. The NTF zero-placement coefficients, p_1 - p_4, are calculated first. Note that in the case of the *3/1* modulator, the fourth NTF in-band zero (i.e. the image-band notch) is realized as p_4, as per Section 5.1.3. Then, the NTF/STF pole-placement coefficients, B_4 - B_1, and the STF zero-placement coefficients, A_4 - A_1, are calculated.

Coefficients for the *3/1* modulator are listed below in Table B.8.

Table B.8: *3/1*-Modulator Coefficients

	Real Coefficient	Imaginary Coefficient
N	d_N	c_N
1	-1.733077748	0.6801448487
2	-1.707106781	0.7071067812
3	-1.680144849	0.7330777481
4	-1.707106781	-0.7071067812
N	b_N	f_N
1	0.03243441947	-0.01179704386
2	-0.265049198	-0.0903430879
3	0.5127556284	0.8766621403
4	0.642186028	-0.3167825683

Table B.8: *3/1*-Modulator Coefficients

	Real Coefficient	Imaginary Coefficient
N	a_N	e_N
1	-0.03378926977	-0.006708382725
2	0.01844479667	0.05687826628
3	0.02758681985	-0.07898762878
4	-0.04720351991	0

B.5 Modulator Simulations

Extensive Simulink and Switcap2 [75] simulations are used to ensure that correct modulator operation results from the calculated coefficients. Fig. B.9 shows the top-level of the system simulated in Simulink, and Fig. B.10 shows the internal workings of one stage (the third).

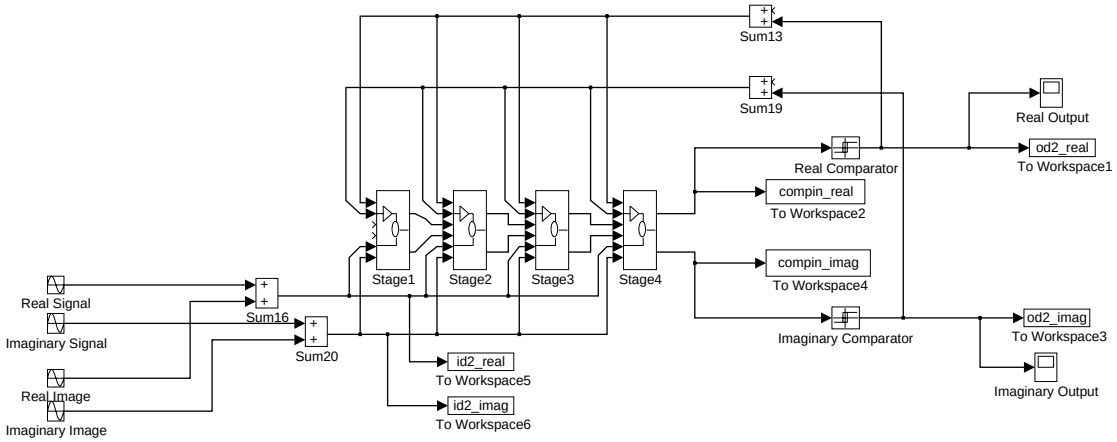


Fig. B.9 Top-level Simulink-system block diagram.

Modulator coefficients and amplifier gain values are stored in matrices, with separate entries for the real- and imaginary-channel components. This allows easy perturbation of coefficients within Matlab, for Monte-Carlo simulations, for example.

The output of an 8k-sample simulation is shown in Fig. B.11. Simulations throughout the thesis follow certain rules: all in-band and image-band inputs are chosen such that they fall entirely into one fft bin; Hann widowing is used in the fft'ing of the output sequence; SNR is

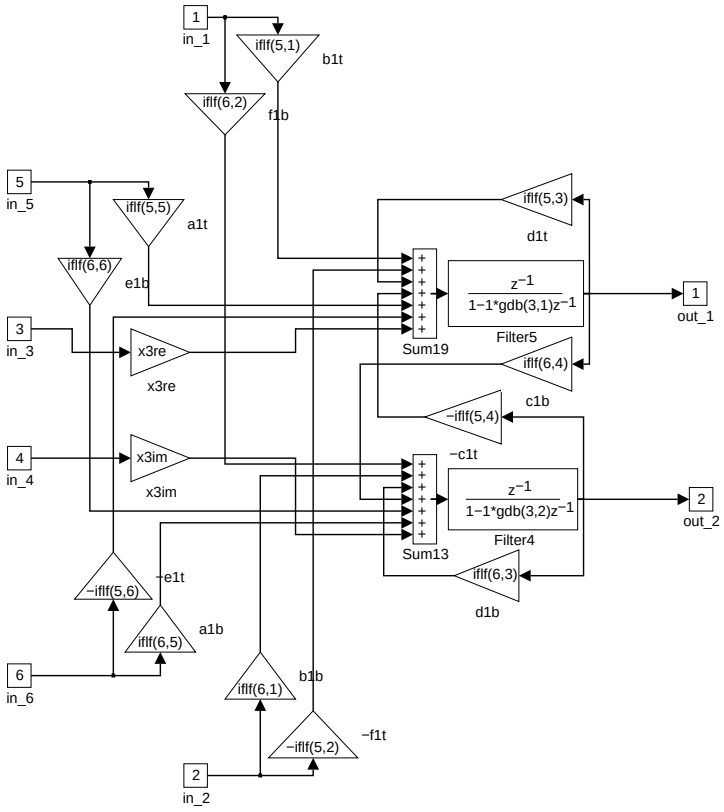


Fig. B.10 Third-stage Simulink-system block.

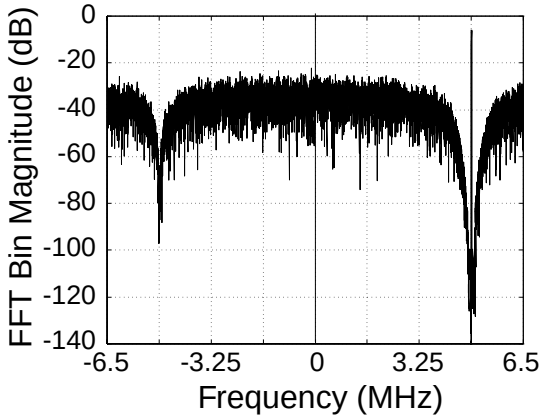


Fig. B.11 Output spectrum of the ideal modulator simulated in Simulink, for a half-scale tone input.

calculated by comparing the total in-band signal power to the integrated in-band noise power. The output-signal pair is converted to a complex signal in Matlab by combining the Simulink-system outputs as I+jQ.

B.6 Coefficient Scaling

System-level modulator simulations were run in Simulink, and in a C program, for 2^{20} time steps, using the optimized coefficients listed above in Table B.8. In an l_∞-scaling procedure, the peak values obtained for each state, multiplied by 1.1 for a 10% safety margin, were used to scale down the input coefficients of the appropriate state (and scale up its output coefficients) so that each amplifier output will never exceed the reference levels. The state-scaling values, including their 10% margins, are listed in Table B.9.

Table B.9: *3/1*-Modulator Maximum State Swings

State	State Maximum
1	0.31
2	2.26
3	7.56
4	5.25

Once the coefficients from Table B.8 are scaled with these state-swing values, those listed in Table B.10 result. These are the coefficients of the *3/1* modulator (stage-ordering: `umlo`) from Chapter 5 (i.e. prior to the 10x *a*- and *e*-coefficient scaling), which are also used for the IC of Chapter 6.

Table B.10: Scaled *3/1*-Modulator Coefficients

	Real Coefficient	Imaginary Coefficient
N	d_N	c_N
1	-1.733077748	0.6801448487
2	-1.707106781	0.7071067812
3	-1.680144849	0.7330777481
4	-1.707106781	-0.7071067812
	b_N	f_N
1	0.1046271596	-0.03805498019
2	-0.1172784062	-0.03997481766
3	0.06782481857	0.1159606006
4	0.1223211482	-0.06033953682
	a_N	e_N
1	-0.1089976444	-0.02163994427
2	0.008161414458	0.02516737446
3	0.003649050245	-0.01044809904
4	-0.008991146649	0
	Inter-Stage Coefficients, x_N	
2	0.1371681416	
3	0.2989417989	
4	1.44	
	Effective Quantizer Gain	
	5.25	

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