

Design of MOS Current-Mode Logic Standard Cells

Technology: NSC 0.18 μm CMOS9

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Abstract

This report describes how MOS Current-Mode Logic (MCML) standard cells were designed and created, in order to create a cell library. A short introduction about MCML circuits is given, as well as a complete description of the design process, including all the analysis involved in achieving the transistor sizing. Finally, the resulting cell layouts are shown and commented. Design was done in a 0.18 μm National Semiconductor CMOS9 technology.

1 Introduction

MOS Current-Mode Logic (MCML) is an alternative logic designing style that provides true differential operation, low noise level generation and noise immunity. The cells developed in this project will be used to create a complete library of MCML cells in order to implement a decoder circuit for analog-to-digital converters.

The technology used was a 0.18 μm CMOS9 by National Semiconductors. Spectre simulations were done in Cadence Analog Environment, and cells were drawn with Cadence Virtuoso Design Platform.

1.1 Project structure

In *chapter 2* we describe the basics of MCML technology. We will compare MCML with classical CMOS, and see the advantages and disadvantages of this circuits.

In *chapter 3* the design process is explained: How the library parameters were chosen, testbenches used, corners and multiple drive strengths analysis. We will talk about the reasons for including a guard ring in the final design.

In *chapter 4* we give the resulting layouts. They are organized by levels, and we will explain the reasons for drawing each different topology. Finally, definitive cell layouts are presented.

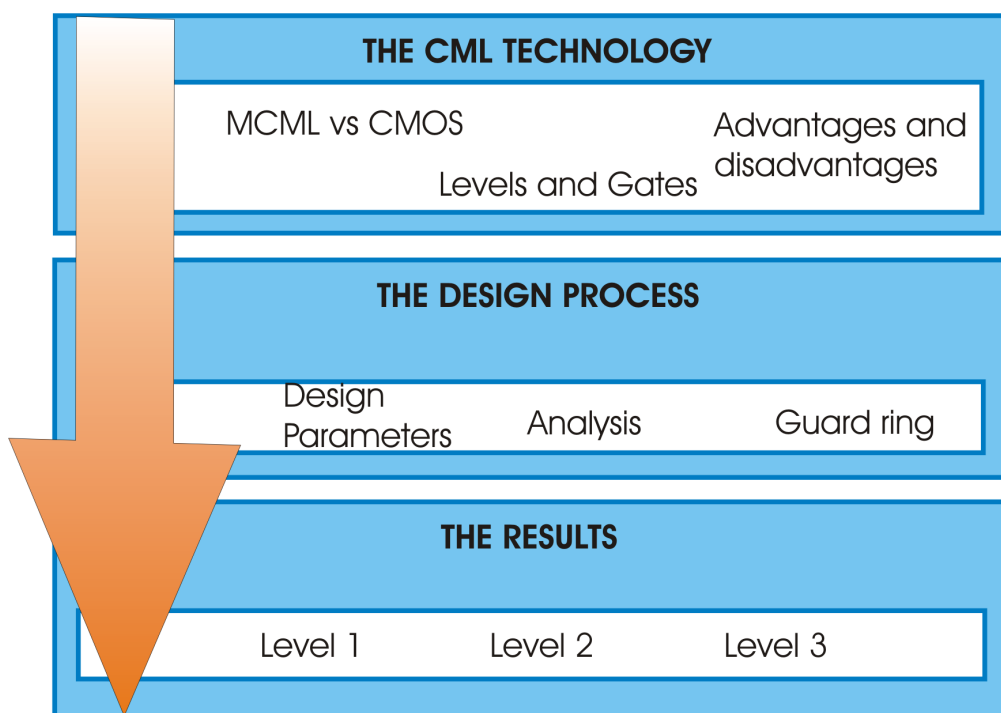


Figure 1.1: Project structure

2 The CML Technology

In this chapter, we will compare MCML to classical CMOS in order to see the advantages and disadvantages of this technology, we will see how design can be approached, and meet the basic gates that will be developed.

2.1 Basics of MCML

When designing High-Speed ICs with classical CMOS technology we encounter the problem that delay limits the switching speed of the gate. We can improve the propagation delay times via correctly sizing our transistor, as large W/L ratios will result in a faster switching gate, but also in a bigger power consumption, as we will see later.

Some techniques developed to improve the design of High-Speed circuits (as Complementary Pass-Transistor Logic (CPL) or Differential Cascode Voltage Switch Logic (DCVSL)) showed that when differential signals are used in the circuits, a compact design, a better noise immunity and, in short, a better gate for this kind of High-Speed operation can be obtained.

MOS Current-Mode Logic [MA05] circuits provide true differential operation, have the feature of low noise level generation, and have static power dissipation: the amount of current drawn from the power supply does not depend on the switching activity. Due to this, MCML gates have been discovered to be useful for analog and mixed-signal ICs.

2.2 MCML vs CMOS

We are going to develop both classical CMOS Logic Inverter and MOS Current-Mode Inverter to see the differences between these circuits. It is an useful and appropriate example since this inverter is a basic element for every technology used in IC design.

2.2.1 Classical CMOS Logic Inverter

This inverter[MC97]uses two MOS transistors, a PMOS and a NMOS, coupled as shown in figure 2.1. These two transistors operate as switches that have a non zero resistance when closed and a infinite resistance when opened.

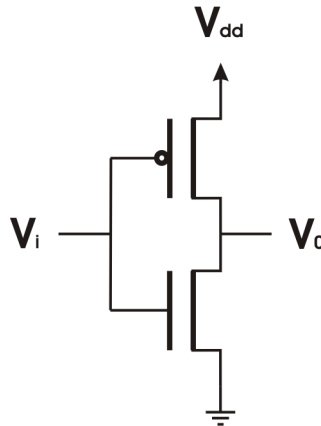


Figure 2.1: Classical MOS Logic Inverter

When v_i is equal to V_{DD} , which is a logic 1, as we see in figure 2.2 PMOS transistor is cut-off, and we can considerate the NMOS transistor as a resistor, as it operates in the linear or triode region. We can always calculate in a very straightforward way the resistance of the NMOS if we know the size and transconductance of it:

$$r_n = 1 / \left[k_n \left(\frac{W}{L} \right)_n (V_{DD} - V_{tn}) \right]$$

When v_i is linked to ground, which is a logic 0, as we see in figure 2.3 NMOS transistor is cut-off, and the PMOS transistor is operating in the triode region. This time we also calculate easily the resistance of

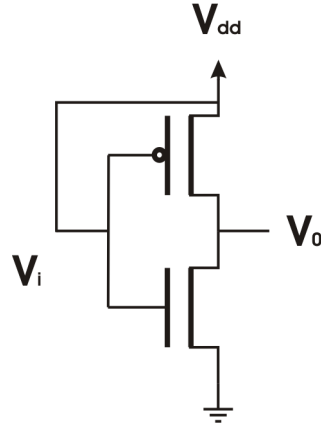


Figure 2.2: Classical MOS Logic Inverter when output is zero.

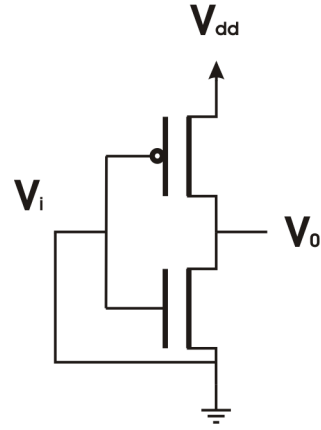


Figure 2.3: Classical MOS Logic Inverter when output is one.

the PMOS:

$$r_p = 1 / \left[k_p \left(\frac{W}{L} \right)_p (V_{DD} - |V_{tp}|) \right]$$

In both cases the static power consumption is zero, since the voltage difference between source and gate for the transistor in the triode region is zero, and so the current is zero and so is the static power.

Figure 2.4 shows the graph that relates v_o and v_i voltages.

This MOS inverter gate has a propagation delay, due to the fact that we need to charge the MOS capacitance (when creating the conduction channel). As we said, this delay will limit the speed of the gate.

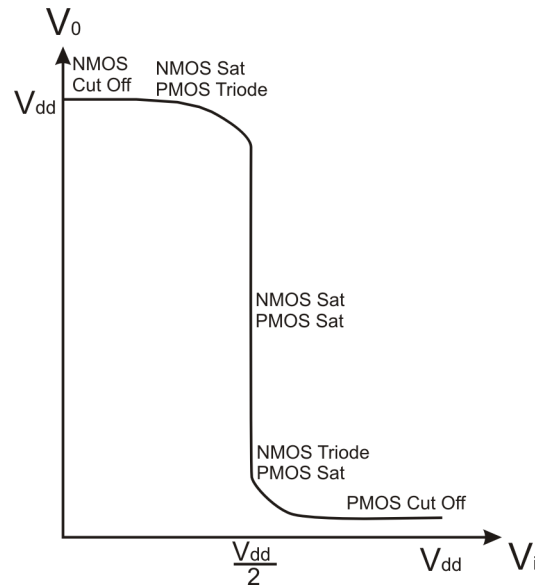


Figure 2.4: Transfer characteristic of a classical CMOS inverter

The dynamic power dissipation can be calculated if we determine the switching frequency and the transistor size:

$$P_{dynamic} = fCV_{DD}^2$$

As we see in figure 2.5 power consumption is zero when the output is logic 0 or 1.

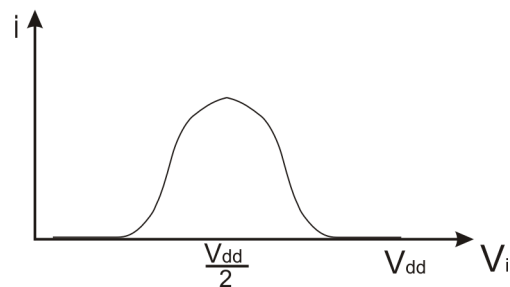


Figure 2.5: Current vs. Input Voltage for the Classical CMOS Inverter

For the classical CMOS inverter we can summarize:

- $V_{SWING} = V_{DD}$ (the maximum).
- Static power dissipated is zero, but dynamic depends on transistor size and V_{DD} .
- Output signal 0 or 1 is independent of W/L .

2.2.2 MOS Current-Mode Inverter

This inverter uses four MOS transistors, two PMOS and two NMOS, connected as shown in figure 2.6. This circuit does a current to voltage conversion.

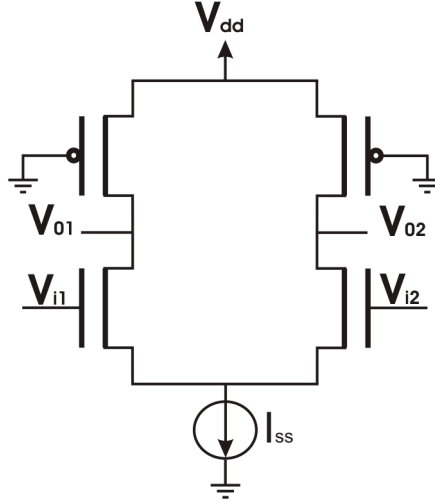


Figure 2.6: MOS Current-Mode Logic Inverter

When the inverter is operating, PMOS will operate in the triode region, this is, as if they were resistors, because $V_{sg} = V_{DD}$ and $V_{sd} < V_{sg}$. I_{SS} current will be divided between the two i_D of NMOS transistors. We can determine by circuit analysis [MA05] that the amount of current flowing through the transistor, being $v_i = v_{i1} - v_{i2}$, will be:

$$i_{D1}(v_i) = \begin{cases} 0 & \text{if } v_i < -\sqrt{\frac{2I_{SS}}{\mu_n C_{OX} \frac{W_n}{L_n}}} \\ \frac{I_{SS}}{2} + \frac{v_i}{2} \sqrt{\mu_n C_{OX} \frac{W_n}{L_n} I_{SS} - \left(\mu_n C_{OX} \frac{W_n}{L_n} \frac{v_i}{2} \right)^2} & \text{if } |v_i| \leq \sqrt{\frac{2I_{SS}}{\mu_n C_{OX} \frac{W_n}{L_n}}} \\ I_{SS} & \text{if } v_i > \sqrt{\frac{2I_{SS}}{\mu_n C_{OX} \frac{W_n}{L_n}}} \end{cases}$$

$$i_{D2}(v_i) = I_{SS} - i_{D1}(v_i)$$

Here, W_n and L_n are the effective NMOS transistor channel width and length, C_{OX} the oxide capacitance per area, and μ_n the NMOS carrier mobility.

2. The CML Technology

As PMOS transistors work in the linear region, their equivalent resistance will be written as:

$$R_D = V_{sd}/i_D$$

This calculation of the resistance can also consider other transistor parameters, resulting in a more accurate result, but through a more cumbersome calculation.

The output voltage transfer characteristics of this inverter can be calculated once we know the equivalent resistance R_D , so the differential voltage v_o is:

$$v_o = v_{o1} - v_{o2} = -R_D (i_{D1} - i_{D2})$$

We stated before the transistor current equations, so now we can evaluate the transfer characteristic of a MCML inverter:

$$v_o(v_i) = \begin{cases} R_D I_{SS} & \text{if } v_i < -\sqrt{\frac{2I_{SS}}{\mu_n C_{OX} \frac{W_n}{L_n}}} \\ -v_i R_D I_{SS} \sqrt{\mu_n C_{OX} \frac{W_n}{L_n} I_{SS} - \left(\mu_n C_{OX} \frac{W_n}{L_n} \frac{v_i}{2}\right)^2} & \text{if } |v_i| \leq \sqrt{\frac{2I_{SS}}{\mu_n C_{OX} \frac{W_n}{L_n}}} \\ -R_D I_{SS} & \text{if } v_i > \sqrt{\frac{2I_{SS}}{\mu_n C_{OX} \frac{W_n}{L_n}}} \end{cases}$$

This transfer characteristic is pictured in figure 2.7. As we see, tail PMOS and NMOS transistors will give us the limits of the V_{SWING} .

In order to keep NMOS transistors out of the triode region, we must keep $R_D I_{SS}$ low enough. This is achieved if the gate-drain voltage V_{gd} is lower than the threshold voltage, and this imposes an upper bound to $R_D I_{SS}$, and so for the logic swing:

$$V_{gd} = V_{DD} - [V_{DD} - R_D I_{SS}] = R_D I_{SS} \leq V_{T,n}$$

For the classical MCML inverter we can summarize:

- $V_{SWING} = 2R_D I_{SS}$
- Static power dissipated $P = V_{DD} I_{SS}$.
- Output signal 0 or 1 is dependent of W/L, because V_{SWING} is parameter dependent.

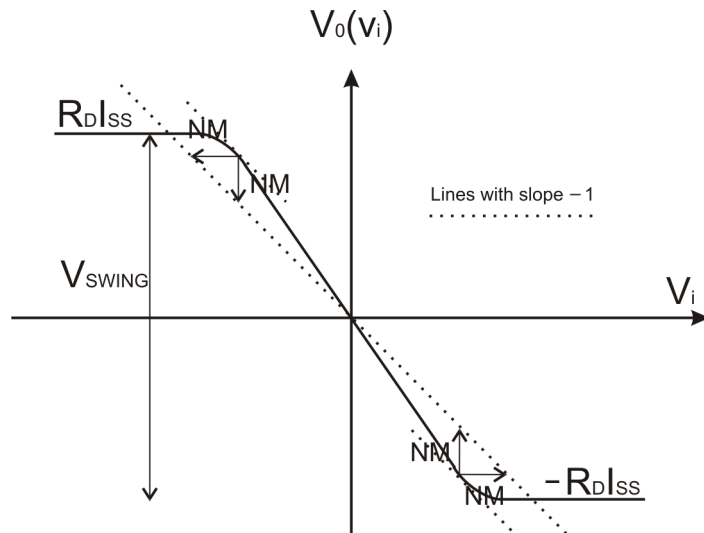


Figure 2.7: Transfer characteristic of a MCML inverter

2.2.3 Advantages and disadvantages of this technology

As said in Professor Leblebici's lecture notes [YL07]:

Advantages:

- Differential circuit operation.
- Low voltage swing - suitable for high speed.
- Weak dependence of propagation delay on fanout load capacitance (compared to CMOS).
- Robust performance and better noise immunity.
- Constant current drawn from the power source.
- Does not generate significant switching noise.
- Power dissipation superior to classical CMOS especially at high operating speeds.

Disadvantages:

- Static power dissipation.
- More elaborated design process.
- Larger number of design parameters.

- Larger layout area because of the PMOS (resistors).
- Larger interconnect area: differential routing.

2.3 Levels and gates

MCML circuits have a very nice characteristic: almost any cell can be obtained from 3 basic ones. We will give special names to this circuits: level 1, level 2 and level 3. The MCML inverter explained previously is level 1, because it has only one differential pair of transistors (figure 2.8). Level 2 has two levels of differential pairs, a first level with only one pair and a second level with two pairs, as we see in figure 2.9. It is like stacking new differential pairs to the previous level. Similarly, level 3 results from adding 4 new differential pairs over the two last of level 2, as shown in figure 2.10.

Some examples of gates that can be done with this three levels:

- *Level 1*: works as a buffer when $Y = A$.
- *Level 2*: can make an AND2 gate ($Y = A \times B$), and XOR2 ($Y = A \oplus B$) or a 2 to 1 multiplexer.
- *Level 3*: here there are many gates that can be done. Examples of these are an AND3 gate ($Y = A \times B \times C$) or a 4 to 1 multiplexer. We can think about lots of other functions that can be done with level 3, for example: $Y = A \times B + C$, and so on.

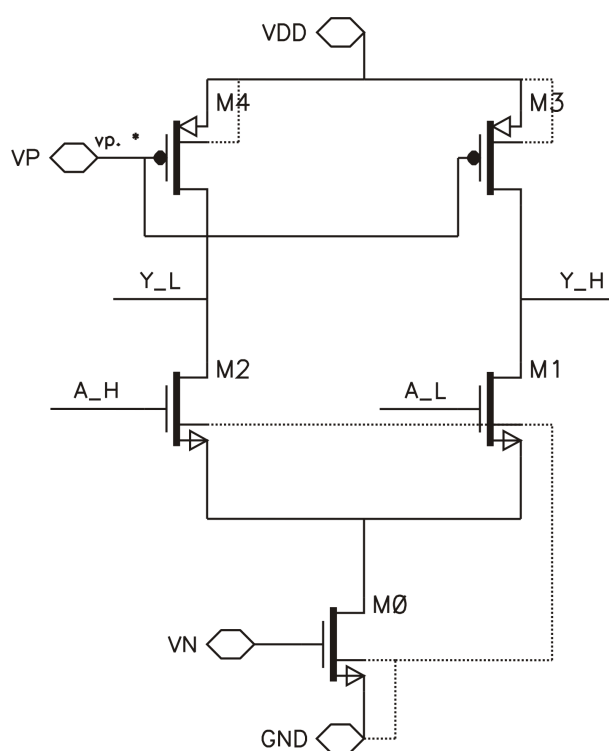


Figure 2.8: Schematic of Level 1



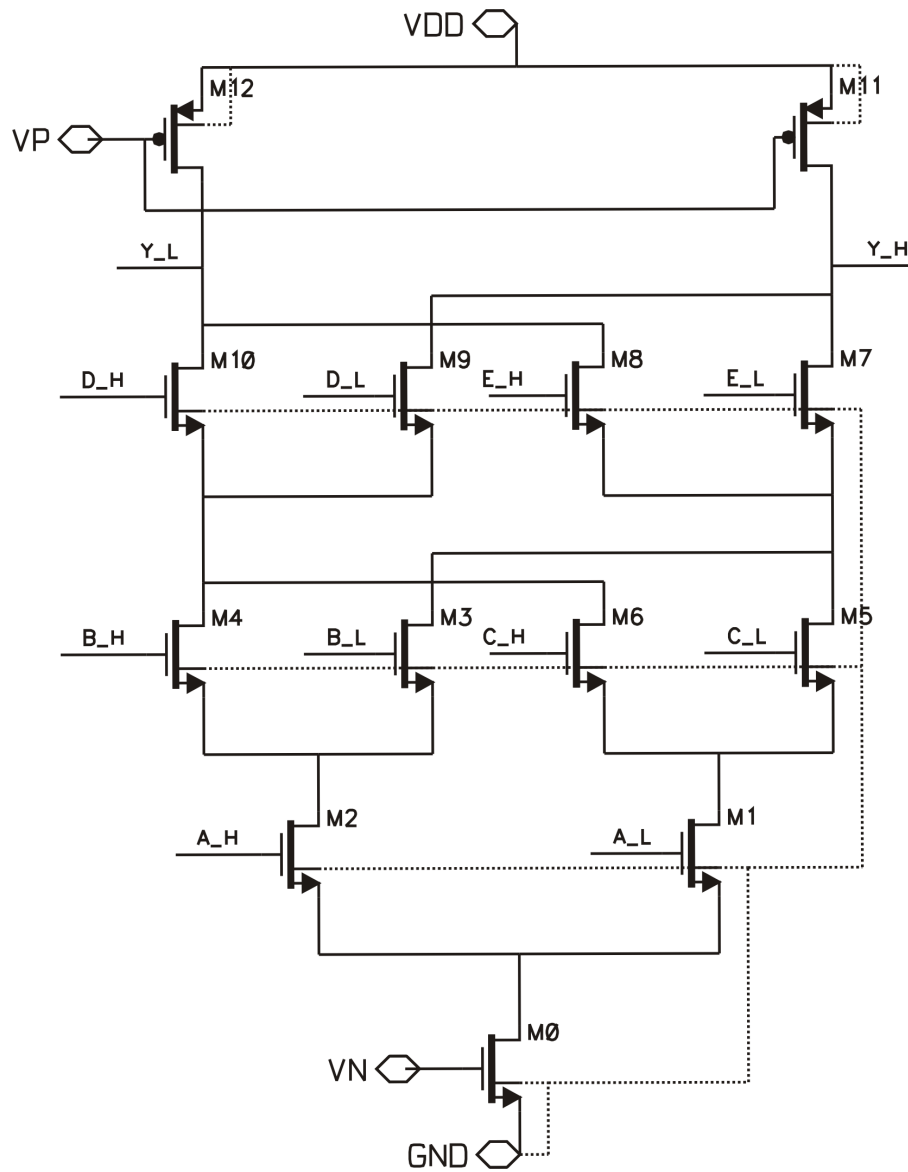


Figure 2.10: Schematic of Level 3

3 The design process

A standard library cell has many parameters that define its characteristics. Some of them will be decided a priori, like constraints that every cell must respect. Concerning our technology, such parameters are, for example, V_{SWING} , I_{bias} or the noise margin, NM. Other parameters, like the sizes of the differential pairs, will have to be obtained by simulation in order to draw the layouts.

After we are given the standard cell parameters, we will obtain through spectre-state simulations the sizes of the NMOS transistors. We will verify with corner analysis that the constraints are met, no matter how fast are the PMOS and NMOS transistors used.

Finally we will repeat the process for a multiple drive strengths design, in order to draw some cell layouts that can drive higher currents.

In this chapter we will also talk about the guard ring that was included in the last stage of the project.

3.1 Design parameters

For MCML cells there are three characteristic parameters: V_{SWING} , I_{bias} and NM. The values of these three parameters, as well as tail transistor sizes, and operating voltage of the cell, are given to us at the beginning of the design process. V_{SWING} was chosen so that the delays were reasonable. A smaller V_{SWING} will result in having more gate delay but less load delay, because for small V_{SWING} transistors are larger, and so is C_i :

$$\tau = RC = \frac{V_{SWING}}{I_{bias}} (C_i + C_L)$$

I_{bias} is related to the size of the transistors in our gate, as the NMOS tail transistors will determine the current driven by the gate. The noise margins are large enough to make the gate operate reliably.

All the parameters given to us are summarized in table 3.1.

V_{DD}	1.8 V
I_{bias}	20 μ A
V_{SWING}	320 mV
NM	100 mV
W_p	640 nm
L_p	660 nm
W_n	2 μ m
L_n	540 nm

Table 3.1: Library Parameters

3.2 Analysis

3.2.1 Testbench and analog environment

The sizes of the differential pairs were obtained by running testbench simulations using Cadence Analog Environment. This testbenches include an auxiliary circuit that ideally gives us the biasing voltages V_p and V_n needed to feed the level we are testing by adjusting I_{bias} and V_{SWING} of a reference gate. We can see pictures of the three testbenches used (one for each level) in our simulations in figures 3.1, 3.2 and 3.3.

3. The design process

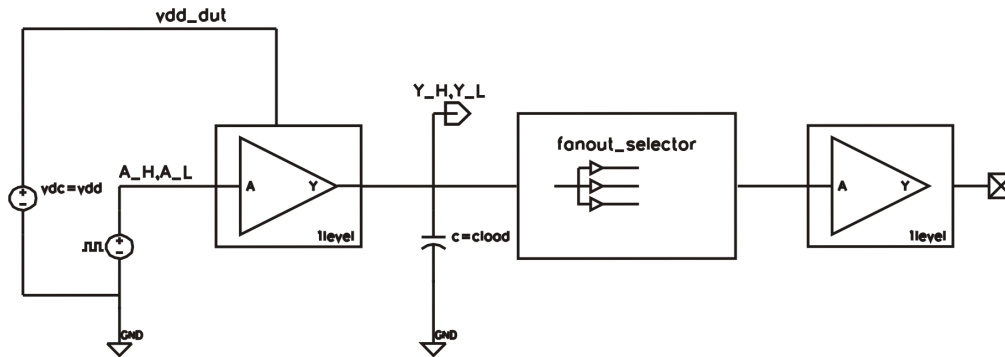


Figure 3.1: Testbench for level 1

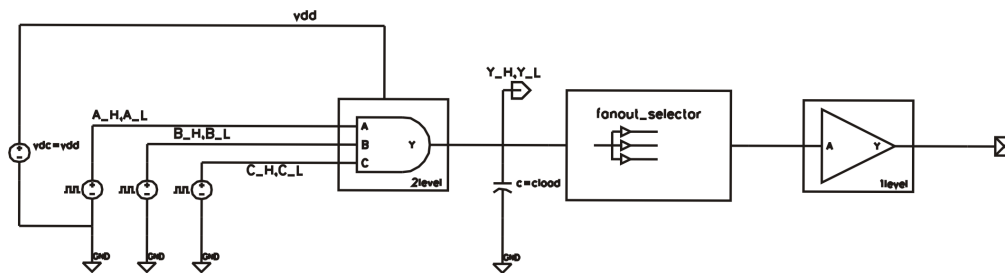


Figure 3.2: Testbench for level 2

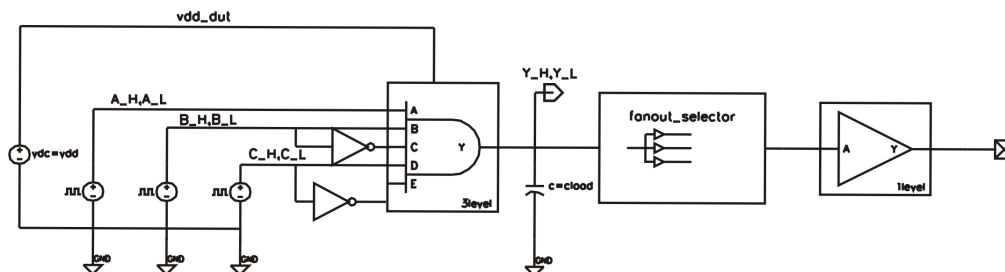


Figure 3.3: Testbench for level 3

3.2.2 Corners

This analysis consist in testing our level in the testbench considering the different possibilities for the transistor speeds, taking all the possible combinations and extreme situations for PMOS and NMOS. Under each analysis our recently sized differential pair transistors must keep the parameters into the specified limits. The most likely parameter to fail in this simulation is the noise margin. Transistors will be resized to meet the parameter constraints in every corner, so we guarantee the correct operation of the level.

Simulations pointed out that the trouble was always in the fast corner. This corner affects the transistors parameters so that they switch faster, and maybe this change in the tail transistor characteristics produces the decrease in the noise margin. We should do some simulations to see how the resistance of this PMOS and NMOS tail transistors changes, and how can this can interfere with the noise margin.

Once the size was adjusted by parametric analysis, we repeated the test for other corners, to verify the constraints.

After all the corners analysis, the final sizing for the transistors is in table 3.2.

	Level 3	Level 2	Level 1
W_3 (μm)	2.6	-	-
W_2 (μm)	3	3.4	-
W_1 (μm)	3.6	3.8	2.6

Table 3.2: Transistor Sizes for all levels

The following tables gather the data obtained in level 1, 2 and 3 corner simulations. For all levels, the power consumption of the gate is roughly $36 \mu\text{W}$.

Corners Level 1

The results for this level, found in table 3.3, were correct.

3. The design process

	V_{SWING} (mV)	NM (mV)	A_v	Delay (ps)	I_{bias} (μ m)
sf	326.6	110.4	2.108	303	20.07
typ	323.5	107.5	2.056	306	20.05
fs	322.9	109.2	2.088	308	20.07
fast	323.3	101.5	1.964	314	20.03
slow	323.7	112.8	2.149	299	20.09

Table 3.3: Corner analysis results for level 1

Corners Level 2

Analysis was done for signals a, b and c, to check the circuit symmetry. The results, found in tables 3.4, 3.5 and 3.6 were correct. Delay was almost the same for the three signals.

	V_{SWING} (mV)	NM (mV)	A_v	Delay (ps)	I_{bias} (μ m)
sf	320.3	115.0	2.317	207	19.92
typ	320.5	113.9	2.286	202	19.91
fs	320.3	115.9	2.324	198	19.92
fast	320.5	110.0	2.222	194	19.90
slow	320.5	116.8	2.349	209	19.94

Table 3.4: Corner analysis results for level 2, considering signal a

Corners Level 3

Analysis was again done for signals a, b and c, to check the circuit symmetry. For simplicity, we chose signal c = $\overline{signalb}$ and signal e = $\overline{signalc}$. This can be seen in figure 3.3, where we can see this two inverters. The results, shown in tables 3.7 , 3.8 and 3.9 were correct. Delay was almost the same for the three signals.

	V_{SWING} (mV)	NM (mV)	A_v	I_{bias} (μ m)
sf	320.9	110.1	2.185	19.93
typ	321.2	107.6	2.133	19.93
fs	320.9	109.5	2.166	19.93
fast	321.6	100.9	2.035	19.92
slow	321.1	112.7	2.228	19.95

Table 3.5: Corner analysis results for level 2, considering signal b

	V_{SWING} (mV)	NM (mV)	A_v	I_{bias} (μ m)
sf	320.9	110.1	2.187	19.93
typ	321.2	107.6	2.135	19.93
fs	320.9	109.5	2.168	19.93
fast	321.6	100.9	2.037	19.92
slow	321.1	112.7	2.231	19.95

Table 3.6: Corner analysis results for level 2, considering signal c

	V_{SWING} (mV)	NM (mV)	A_v	Delay (ps)	I_{bias} (μ m)
sf	317.8	110.5	2.267	659	19.89
typ	317.7	107.6	2.227	659	19.88
fs	318.3	111.9	2.283	659	19.89
fast	316.5	100.3	2.137	659	19.85
slow	318.5	112.7	2.305	659	19.91

Table 3.7: Corner analysis results for level 3, considering signal a

	V_{SWING} (mV)	NM (mV)	A_v	I_{bias} (μ m)
sf	317.6	110.8	2.228	19.93
typ	317.3	110.4	2.222	19.90
fs	318.1	114.4	2.228	19.93
fast	315.7	106.4	2.161	19.83
slow	318.3	112.3	2.254	19.97

Table 3.8: Corner analysis results for level 3, considering signal b

	V_{SWING} (mV)	NM (mV)	A_v	I_{bias} (μ m)
sf	317.8	107.3	2.104	19.95
typ	317.5	107.3	2.107	19.91
fs	318.2	111.2	2.169	19.95
fast	316.2	103.0	2.052	19.83
slow	318.4	108.9	2.125	19.99

Table 3.9: Corner analysis results for level 3, considering signal c

3.2.3 Multiple drive strengths

This test consists in allowing the current in the circuit to be increased 2, 4 or 8 times. This creates 3 new circuits for each level, where we increase consecutively by 2, 4 and 8 the tail transistors size, and after that we do spectre state and corner simulations to size the differential pair transistors and to check that the constraints are met, respectively.

Table 3.10 shows the sizes of the tail transistors for every cell, as well as the current that it will drive.

	W_p (μ m)	W_n (μ m)	I_{ref} (μ A)
1X	0.64	2	20
2X	1.28	4	40
4X	2.56	8	80
8X	5.12	16	160

Table 3.10: Variations in transistors sizes for multiple drive strenghts corners analysis

Table 3.11 gathers the sizes of the differential pair for level 1 cells. In figure 3.4 we can compare the sizes that were obtained by simulation with the sizes that we will expect if we just multiply 2, 4 and 8 times the size of 1X strength level 1. The calculated sizes tend to be on a line, while the simulated are more likely on a parabola.

	W_1 (μ m)
1X	2.6
2X	4.6
4X	7.6
8X	10.6

Table 3.11: Different transistor sizes for multiple drive strenghts in level 1

3. The design process

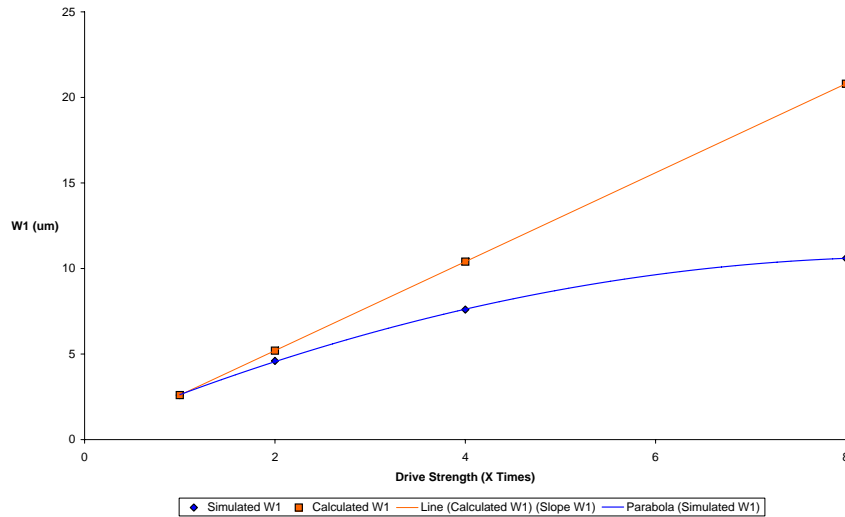


Figure 3.4: Multiple drive strengths - Level 1. Comparison of transistors sizes simulated vs calculated.

Table 3.12 gathers the sizes of the differential pair for level 1 cells. In figures 3.5 and 3.6 we can compare the sizes of the differential pairs that were obtained by simulation with the sizes that we will expect if we just multiply 2, 4 and 8 times the size of 1X strength level 2, as before. Here again, the calculated sizes tend to be on a line, while the simulated are more likely on a parabola.

	W_1 (μ m)	W_2 (μ m))
1X	3.8	3.4
2X	6.8	6.2
4X	11	10.8
8X	17	16.8

Table 3.12: Different transistor sizes for multiple drive strenghts in level 2

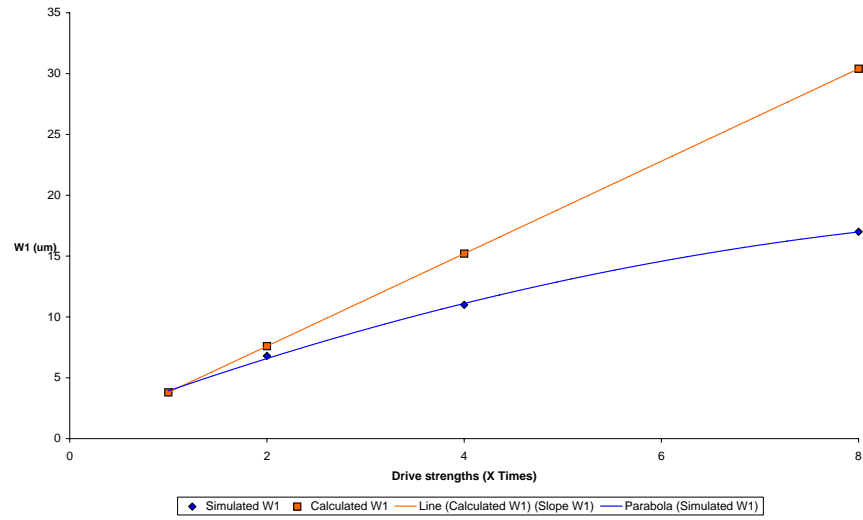


Figure 3.5: Multiple drive strengths - Level 2, W_1 . Comparison of transistors sizes simulated vs calculated.

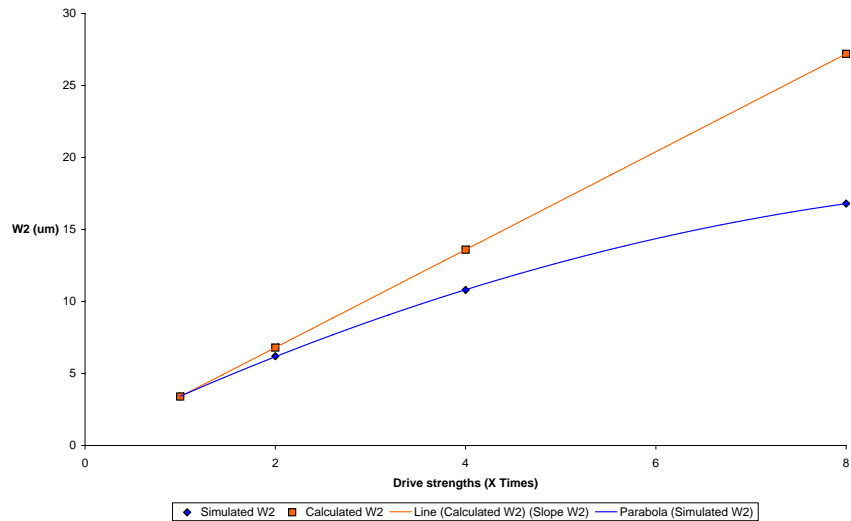


Figure 3.6: Multiple drive strengths - Level 2, W_2 . Comparison of transistors sizes simulated vs calculated.

3. The design process

Finally, table 3.13 has the sizes of the differential pair for level 3 cells. In figure 3.7 we can compare the sizes that were obtained by simulation with the sizes calculated, like before. In this case, sizes obtained by simulation were very close to calculated ones, tending to be on a line.

	W_1 (μ m)	W_2 (μ m)	W_3 (μ m)
1X	3.6	3.0	2.6
2X	7.2	6.0	5.2
4X	14.4	12.0	10.4
8X	28.8	24.0	20.0

Table 3.13: Different transistor sizes for multiple drive strenghts in level 3

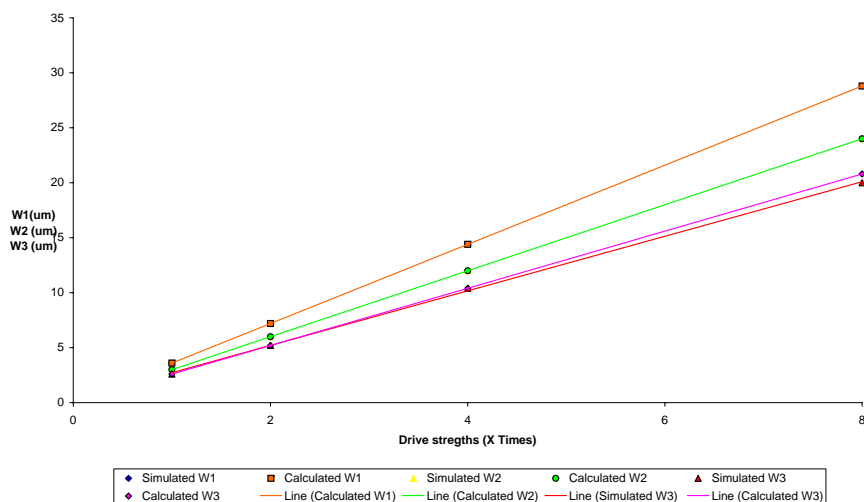


Figure 3.7: Multiple drive strengths - Level 3. Comparison of transistors sizes simulated vs calculated.

3.3 Guard ring

While developing the project, we were requested by National Semiconductors to introduce a guard ring around tail PMOS and NMOS transistors to prevent latchup. This modification will be done in the last layouts.

Guard rings [AH01] prevent minority carriers injected by one device from interfering with the operation of another device. These rings also block noise coupling that might otherwise interfere with the operation of low-power circuitry.

Latchup can be suppressed by enclosing each vulnerable device in a suitable minority carrier guard ring, and so are we doing for our cells. CMOS designs are more prone to latchup than standard bipolar. This vulnerability results in part from the smaller dimensions of modern CMOS processes and in part from differences between isolation systems.

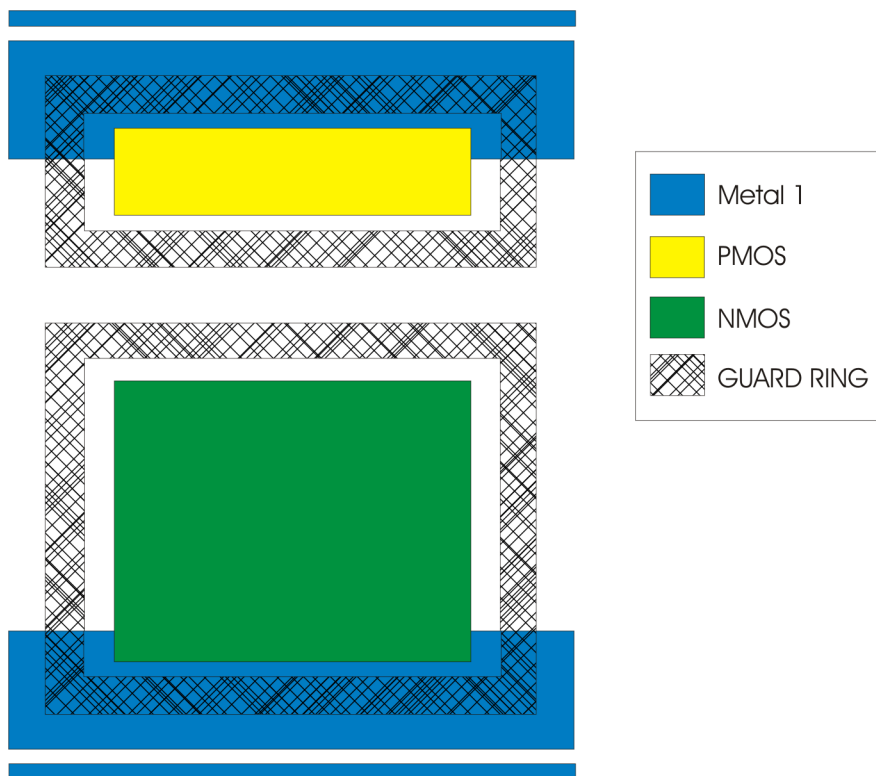


Figure 3.8: Placement of the guard rings

4 Results

When drawing basic cells for a library there are many decisions to make along the design process. These decisions include the cell size, placement of the rail and its size, among others. Another thing to keep in mind is that we will place our cell in a grid, with a given pitch that we will have to respect, and will define where our differential pins can be placed, as well as the cell width and cell height, because these two parameters must be a multiple of the vertical or horizontal routing pitch, respectively.

MCML cells are different from CMOS standard cells in:

- *Differential routing.* This means that every signal is doubled and so are the pins. The position of the pins will determine how many metal layers the router will use to complete the circuit.
- *Area.* CMOS standard cells are much more smaller. Their transistors have smaller W , and they don't use rails or V_p and V_n strips. The design rules are different and they allow, for example, smaller contact enclosures.
- *Guard ring.* Only MCML includes it. This also takes a lot of area.

For this MCML library we decided to use horizontal rails, having V_{DD} on top of the cell and GND at the bottom. After many trial layouts, we decided to keep as a parameter the height of the level 3 cell. We will talk about this decision later.

Multiple layouts were done for each level. For practical reasons we can classify the layouts in four different 'generations', depending on the reasons that led to that design.

The first generation are the very first drawn layouts. This layouts were done while learning how to use the tools, and resulted as a trial drawing of the different cells. Five different topologies were proposed after drawing level 3 layouts. The chosen topology was also drawn for level 1 and 2.

The second generation was done from the multiple drive strengths simulation results, in order to see the sizes that the tail transistors could reach, and how this would affect the distribution of the transistors in the cell. The height of the cell was chosen from the layout proposed for level 3 in the first generation. Transistors where placed like that because we were expecting a fast growth in size and area of the tail transistors as we increased the current of the gate. In the end we stated that the space given to the PMOS transistors was far too big, and that this had to be improved.

The third generation was done when we decided to stack all the transistors in level 3 and keep this height as a parameter for the other cells. Only level 2 and 3 were drawn for 2X and 4X drive strengths to make sure that tail transistors were not a problem for this topology because of their area.

The fourth generation is the last one. Here we introduced the guard ring in all layouts and also used the height of level 3 cell, as those cells are used more often than levels 1 and 2 cells.

4.1 Level 1

4.1.1 First generation

The design flow was different from the way we present the results. Normaly, level 3 was done first and it's height was used as a parameter for the other two levels. In the first generation, five different topologies were proposed for the level 3 layouts, and the last one was chosen. Then, level 2 and 1 where drawn, using the height of level 3 first generation topology 5 cell, that we can see in figure 4.17. In figure 4.1

4. Results

transistors were placed with their gates in vertical position to suit the space that was taken by the PMOS transistors.

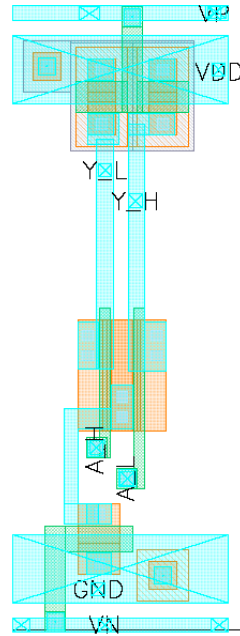


Figure 4.1: Level 1, first generation

4.1.2 Second generation

Second generation keeps the height of first generation circuits. In this generation the first multiple drive strength test was done for all levels, at strengths X2, X4 and X8.

As level 1 has the less transistors, the PMOS transistors defined the ideal maximum width of the cell. In figure 4.2 we see that gates were folded to adjust the width of the differential pair to the tail transistors width.

When drawing strength X4 the size of the PMOS forced us to leave a lot of empty space in the cell. For this strength, as well as for strength X8, another possible layout was proposed, in order to save space by putting the PMOS transistors in two columns, at the sides of the differential pair. This was an interesting option, but it was not useful for the other levels, and a guard ring could not be used with this topology.

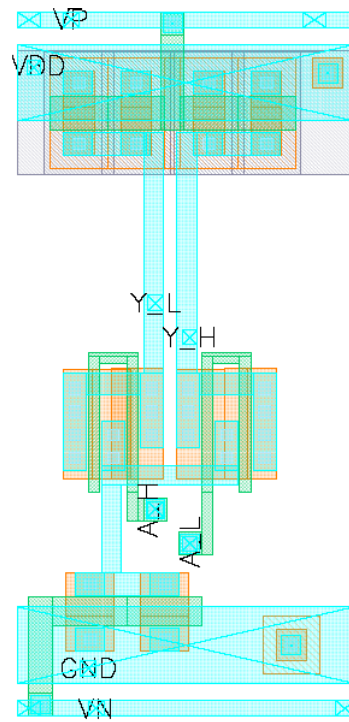


Figure 4.2: Level 1, second generation, strength X2

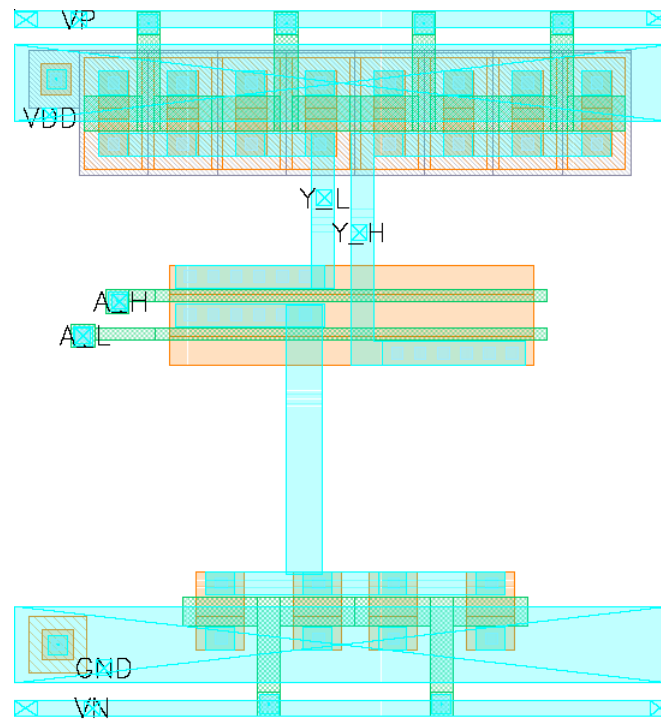


Figure 4.3: Level 1, second generation, strength X4

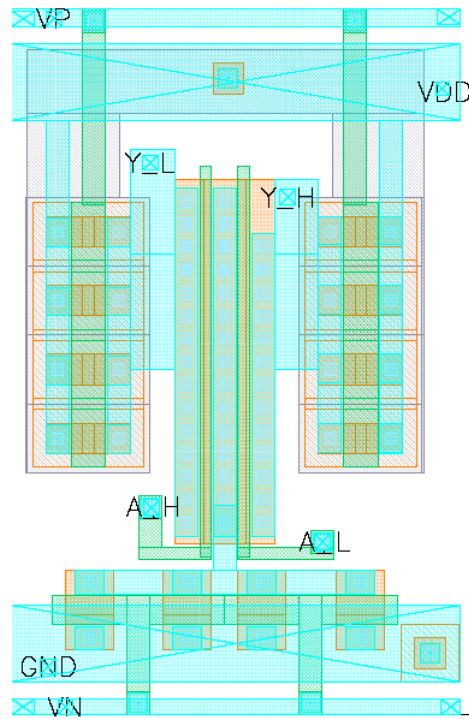


Figure 4.4: Level 1, second generation, strength X4 (another option)

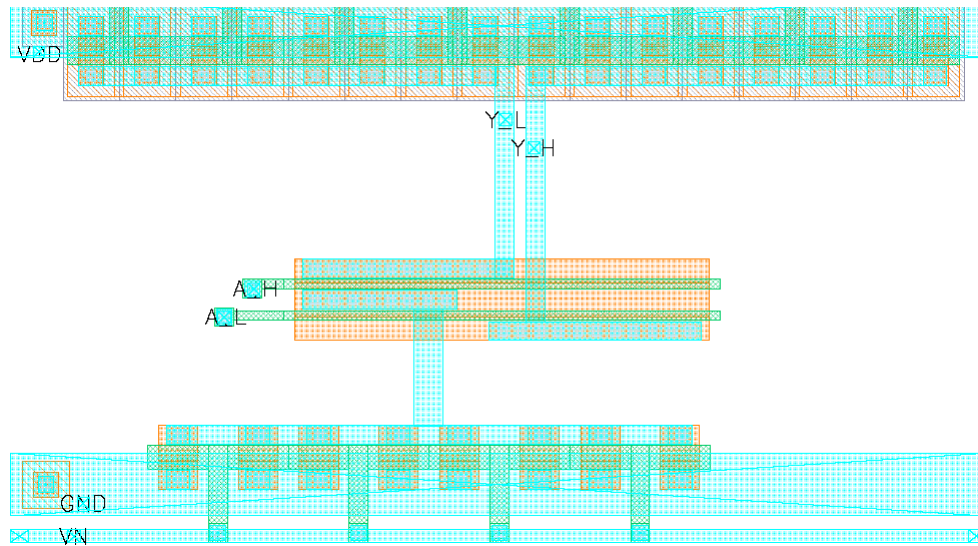


Figure 4.5: Level 1, second generation, strength X8

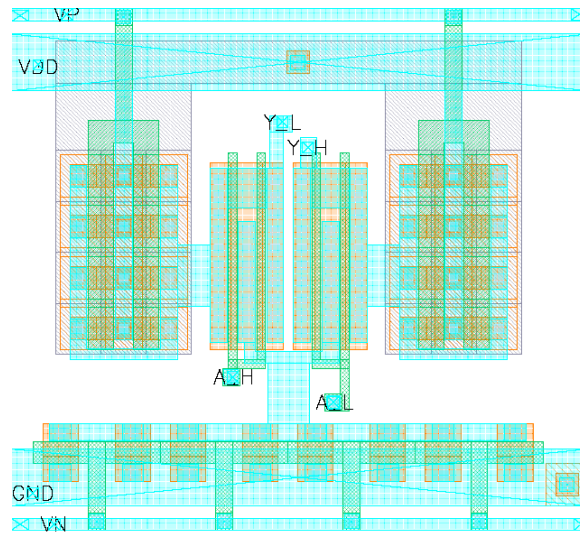


Figure 4.6: Level 1, second generation, strength X8 (another option)

4.2 Level 2

4.2.1 First generation

As we said before, this first generation circuit for the level 2 keeps the height of level 3 cell. The size of the differential pairs did not allow us to put the gates vertically as for level 1, but with them placed horizontally not much space was lost, as we can see in figure 4.7.

4.2.2 Second generation

There are three cells in this second generation, corresponding to the three strengths: X2, X4 and X8. For this cells the tail transistors width was not a problem, as the size of the differential pairs was big enough to fit under them, without having much empty space left.

4.2.3 Third generation

This third generation was a trial of a possible final design for the cells, and it was only done for level 2 and 3, as it was soon replaced by fourth generation circuits, that included the guard ring. The height of this cells was taken again from level 3 cell, but this time all differential pairs were stacked so the cell was higher but also thinner.

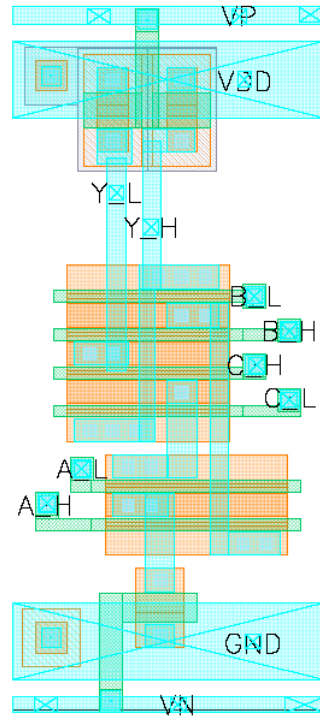


Figure 4.7: Level 2, first generation

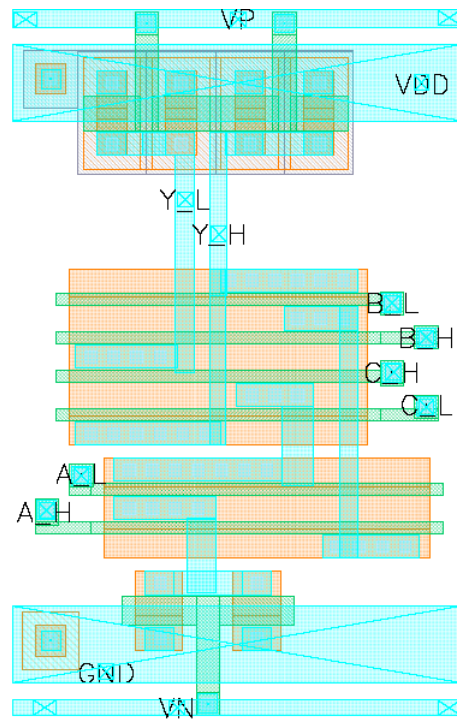


Figure 4.8: Level 2, second generation, strength X2

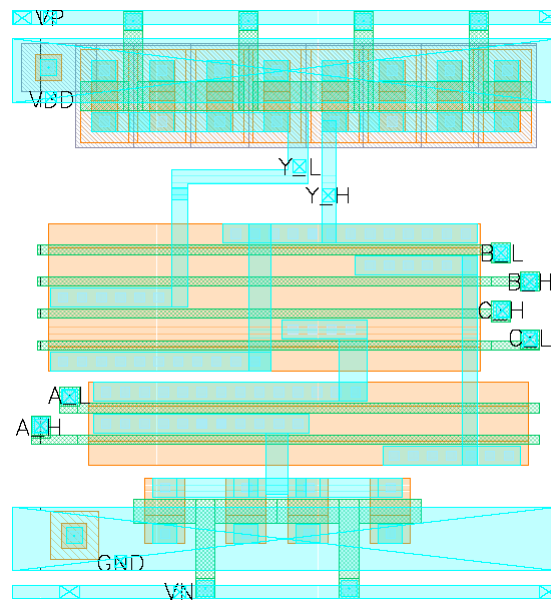


Figure 4.9: Level 2, second generation, strength X4

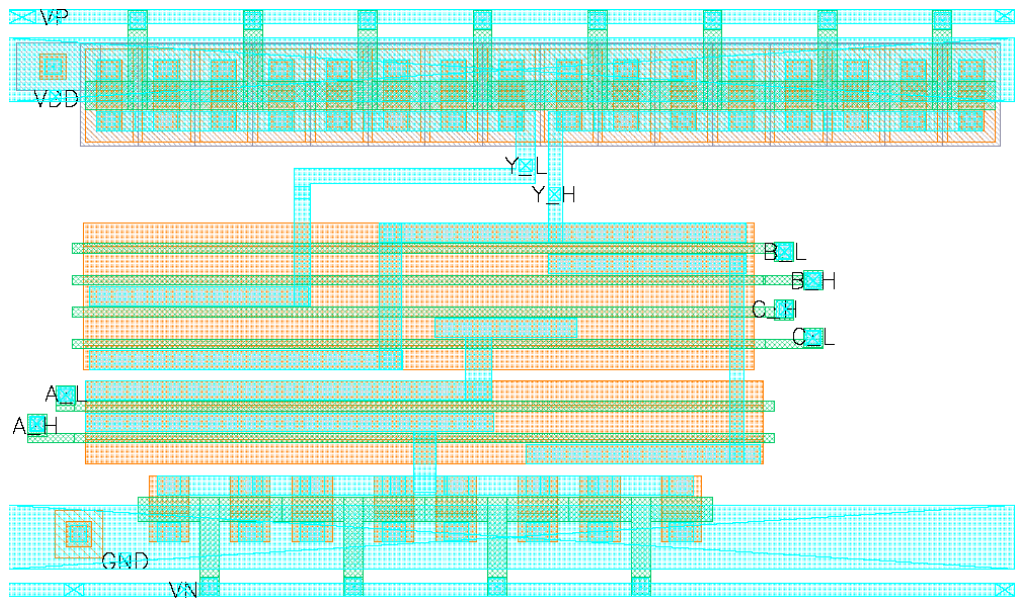


Figure 4.10: Level 2, second generation, strength X8

4. Results

Cells 4.11 and 4.12 have a lot of empty space under the PMOS because of the size of the differential pairs.

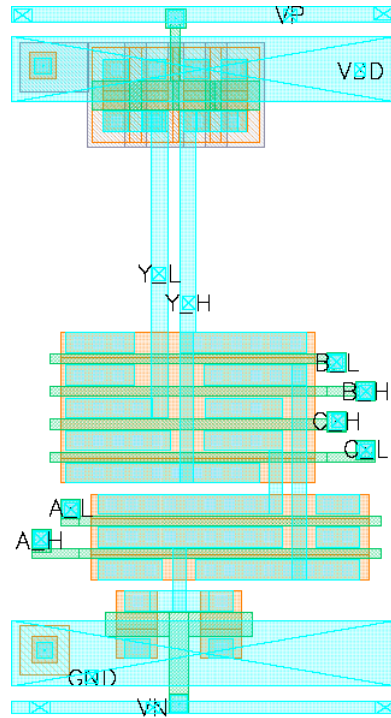


Figure 4.11: Level 2, third generation, strength X2

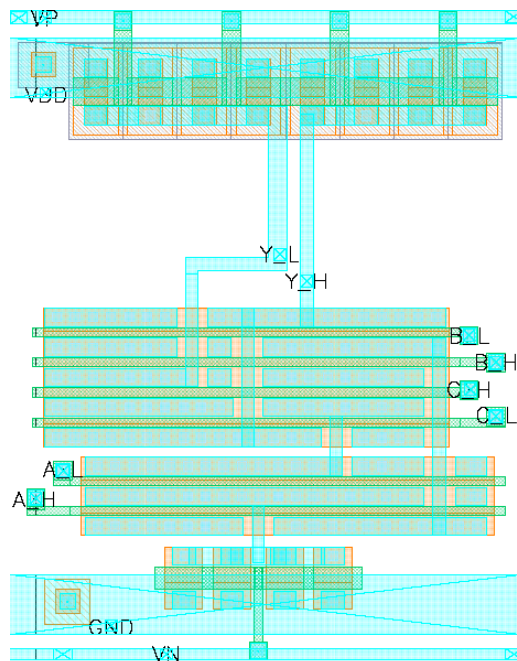


Figure 4.12: Level 2, third generation, strength X4

4.3 Level 3

4.3.1 First generation

For this generation many topologies were proposed. We are going to explain now why this five different ones were drawn.

- Topology 1 (figure 4.13): Here we put the levels in a row. This one was discarded because of the current flow in the circuit was going to the right and then to the left, so stacked designs were preferred.
- Topology 2 (figure 4.14): In this one we fold every gate to see how much space we can save, but we don't have as much transistors in the circuit to make this worthwhile.
- Topology 3 (figure 4.15): Here we use the space left next to the PMOS in the topology 2 to put the level 2 differential pair, and by placing gates in both vertical and horizontal directions we get a very compact design. This one is not chosen because placing the transistors like this will make it very difficult to scale the circuit for other strengths.
- Topology 4 (figure 4.16): In this design the transistors are arranged in two columns. This creates a very compact design also, but this one was discarded because there was no place where the tail transistors can expand as they grow for the bigger strength circuits.
- Topology 5 (figure 4.17): Here we make sure that there will be space for the tail transistors to grow, specially the PMOS. To save height we place two of the differential pairs side by side. In the end, the PMOS did not grow that fast, and this huge space left for them was never used. This topology will also be replaced in the third generation, after we state the area taken by the PMOS.

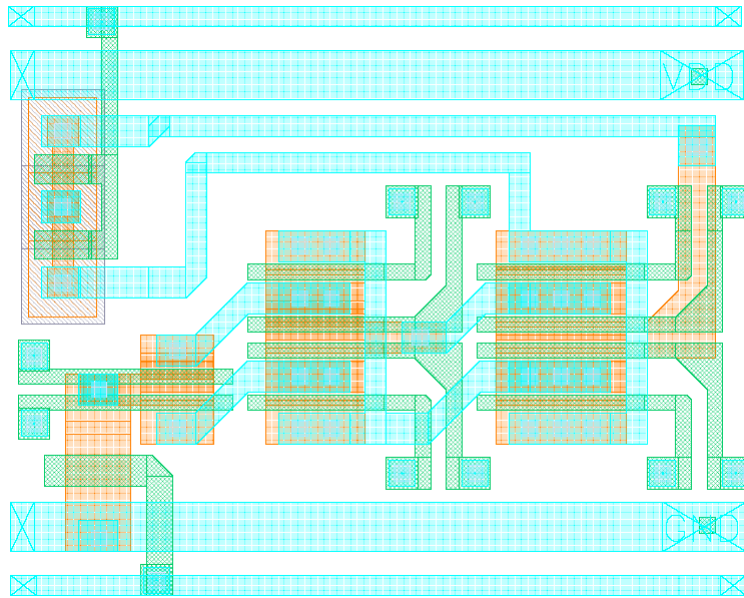


Figure 4.13: Level 3, first generation, topology 1

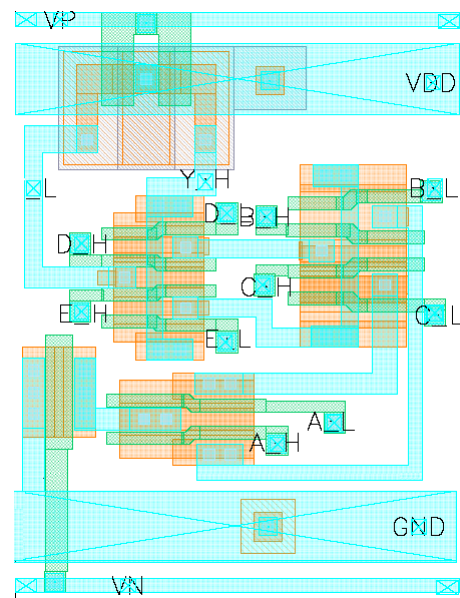


Figure 4.14: Level 3, first generation, topology 2

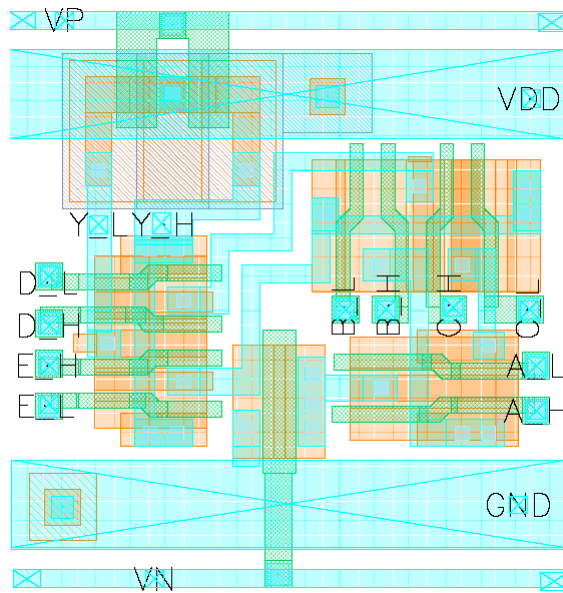


Figure 4.15: Level 3, first generation, topology 3

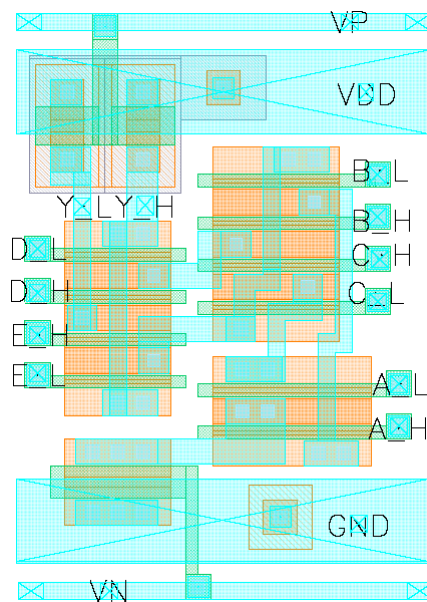


Figure 4.16: Level 3, first generation, topology 4

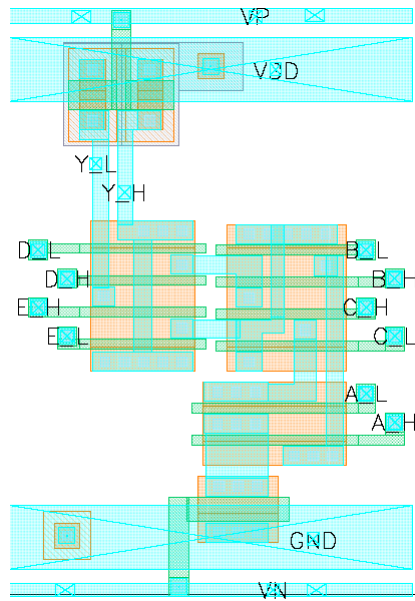


Figure 4.17: Level 3, first generation, topology 5

4.3.2 Second generation

With the multiple strength layouts of this generation we remark that it is not worthwhile to have those two differential pairs (the higher levels) side by side. A lot of area is wasted, so another topology will be proposed to correct this.

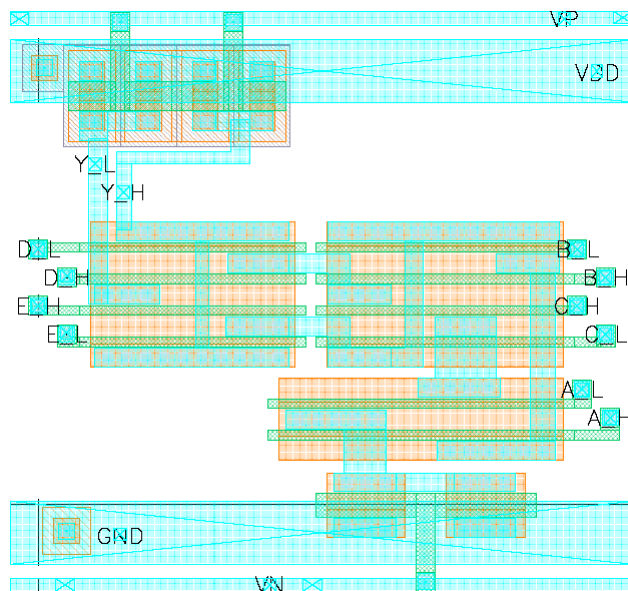


Figure 4.18: Level 3, second generation, strength X2

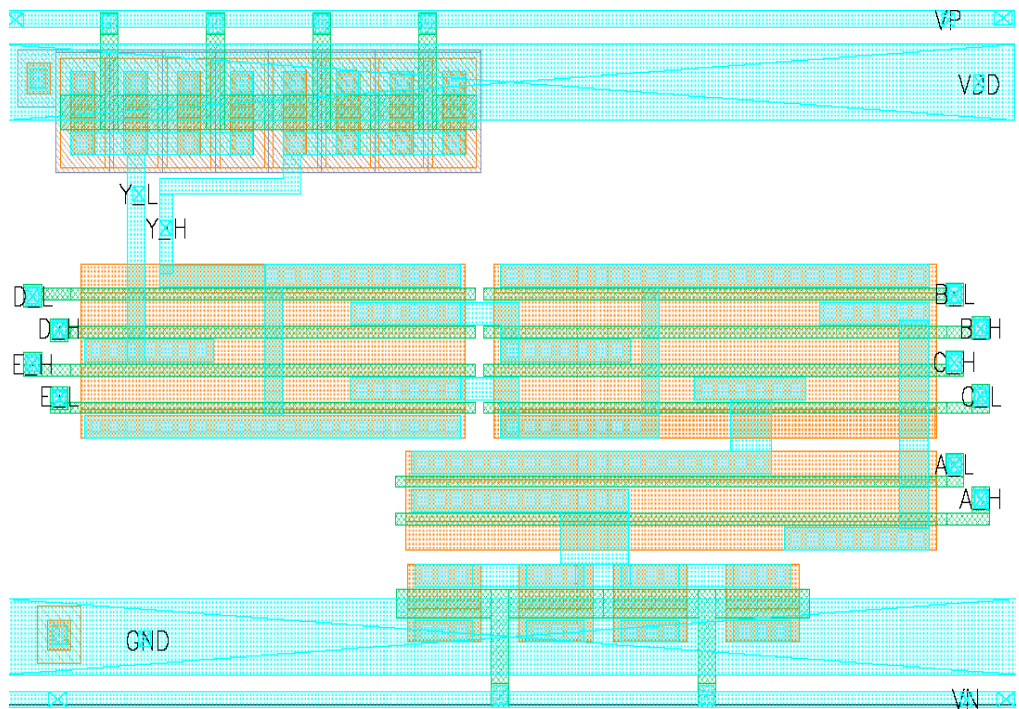


Figure 4.19: Level 3, second generation, strength X4

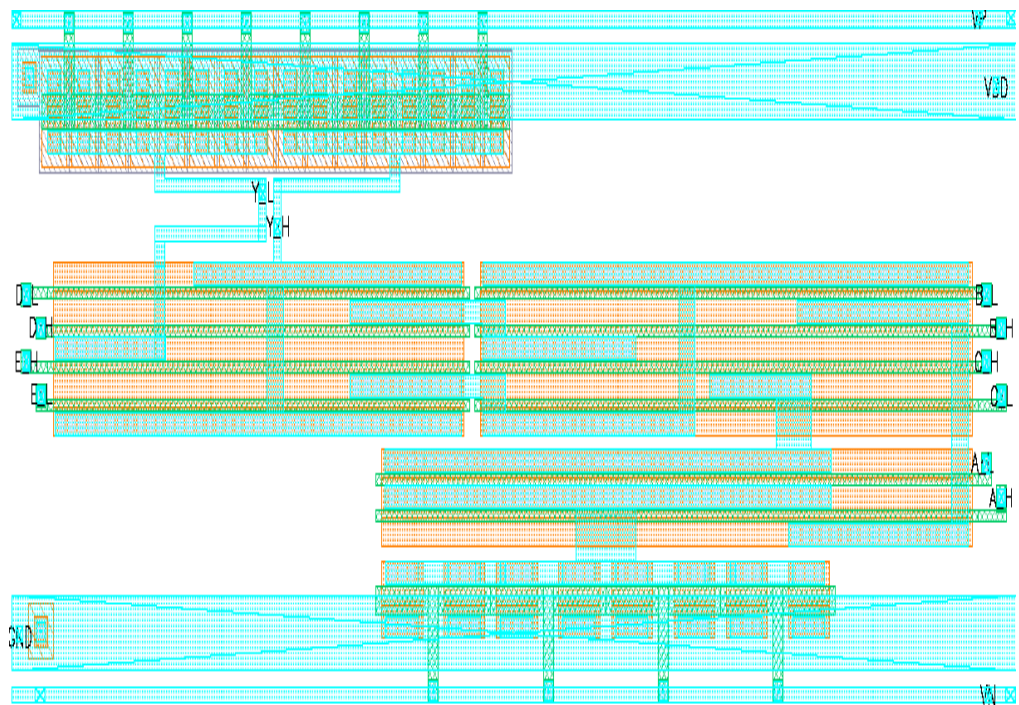


Figure 4.20: Level 3, second generation, strength X8

4.3.3 Third generation

Here we decide to stack the three differential pairs, due to the results of the last layouts. This comes out to be the best option so far, and final layouts will keep this characteristic. We just drew strengths X2 and X4 to make sure there was not many empty space left, and the result was very good, so final layouts have stacked levels as well.

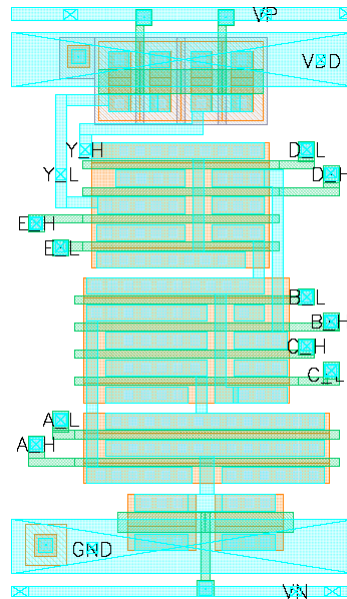


Figure 4.21: Level 3, third generation, strength X2

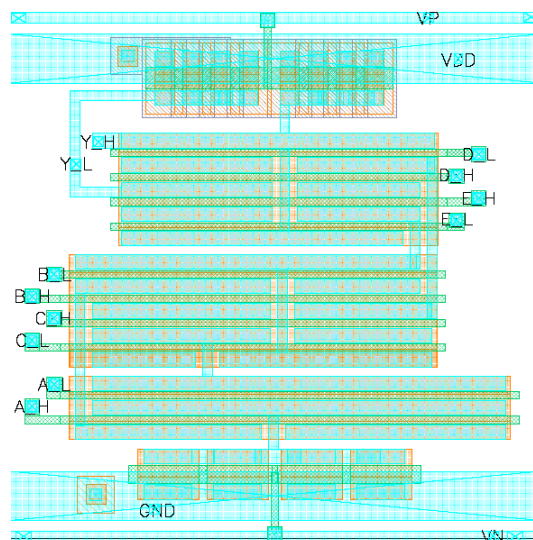


Figure 4.22: Level 3, third generation, strength X4

4.4 The final layouts

Here we present the result of this project. The last layouts include the guard ring requested by National Semiconductors, and have stacked levels to optimize the empty space. We also filled, when possible, the left empty area with extra contacts connected to the guard ring. The final design is compact and its topology is probably the best, due to the use of the guard ring.

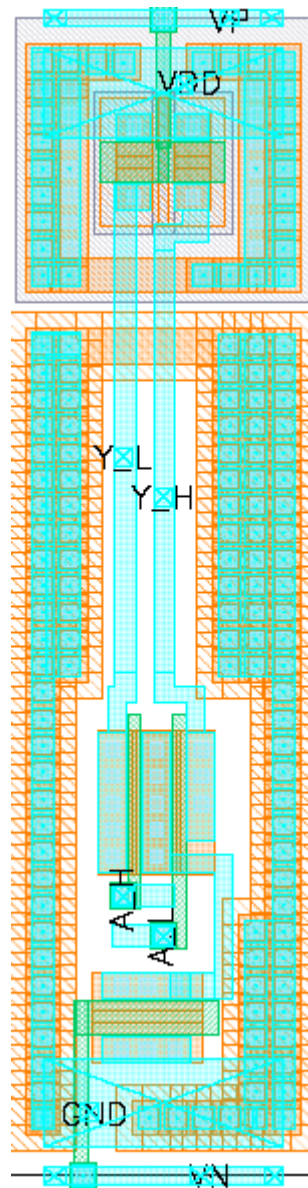


Figure 4.23: Level 1, strength X1

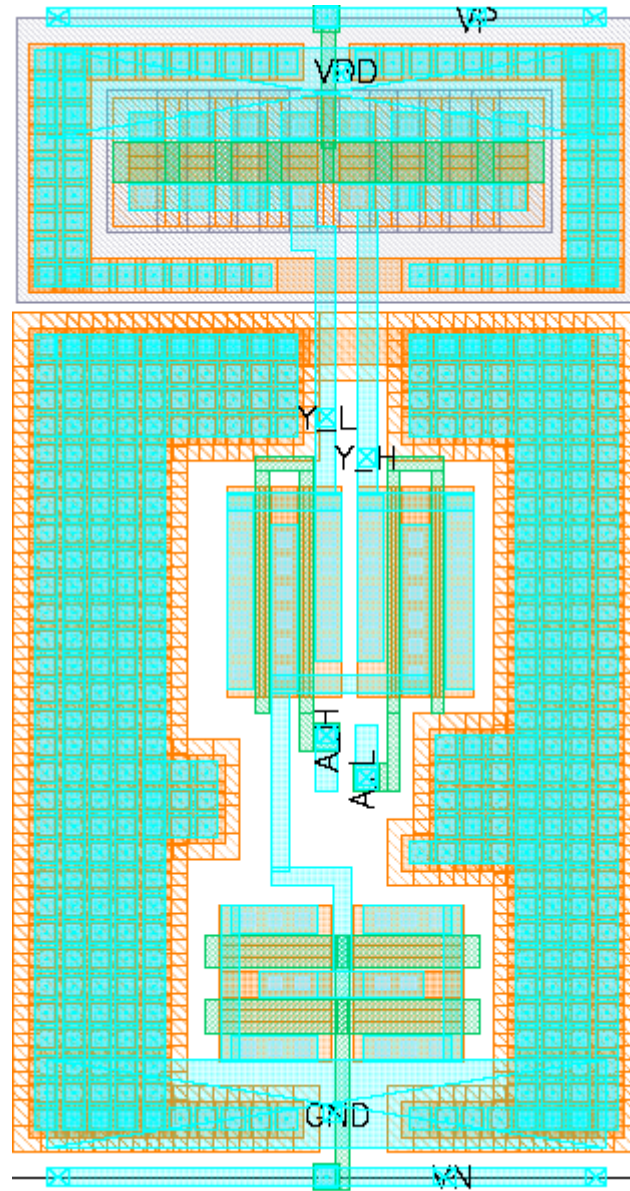


Figure 4.24: Level 1, strength X4

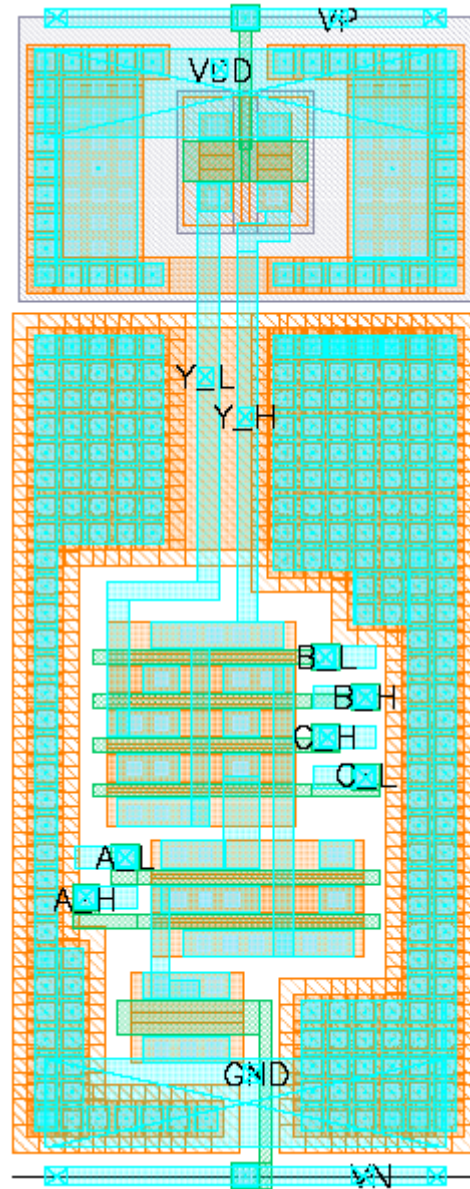


Figure 4.25: Level 2, strength X1

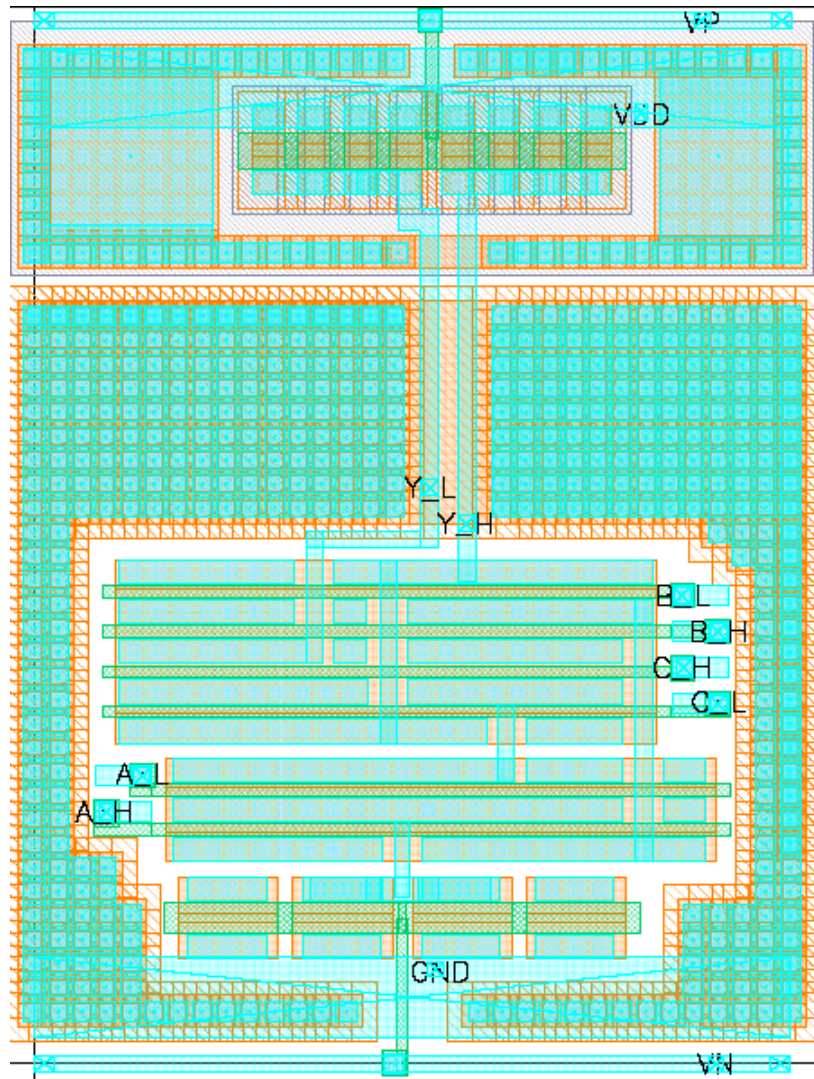


Figure 4.26: Level 2, strength X4

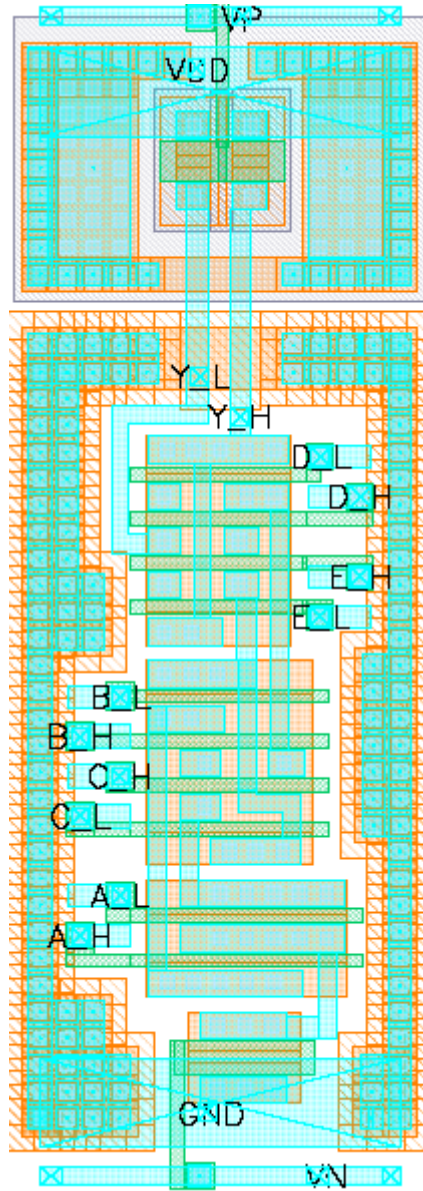


Figure 4.27: Level 3, strength X1

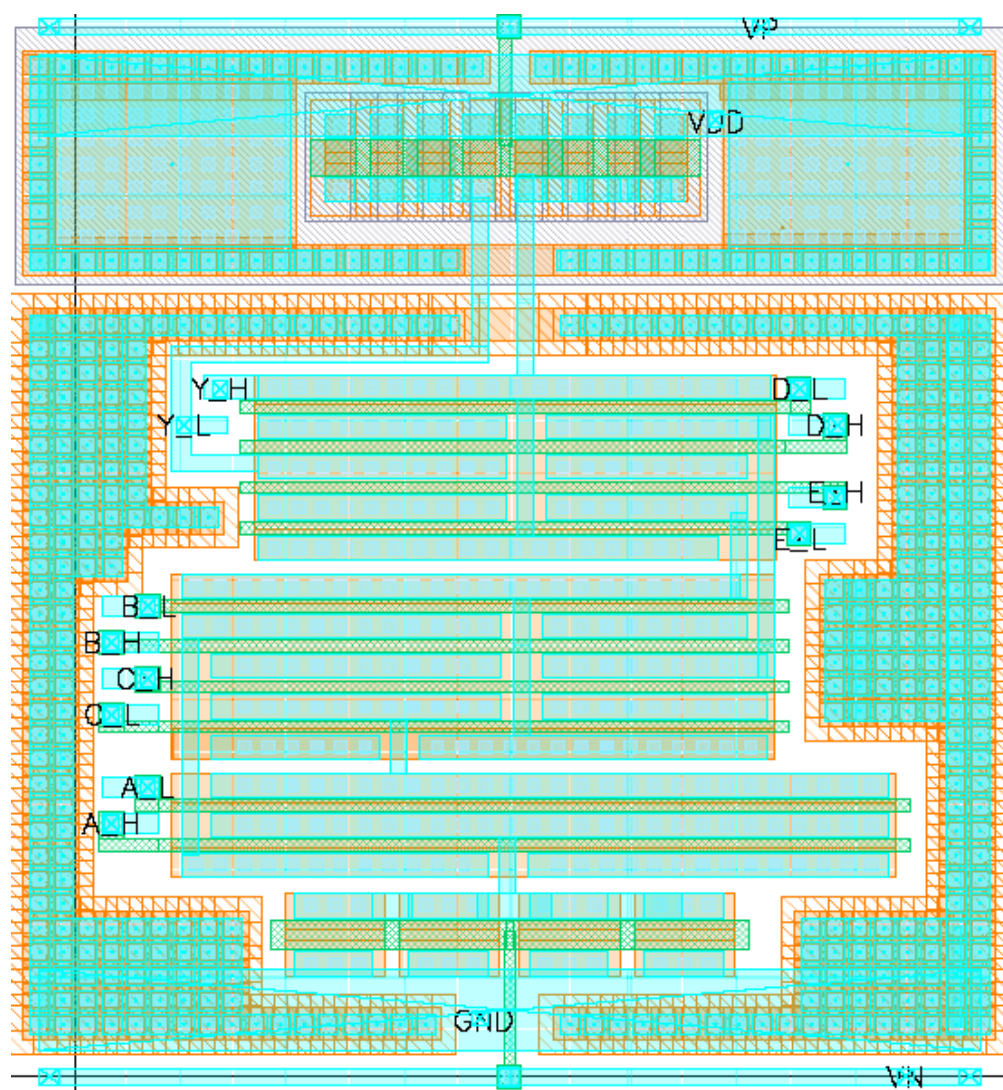


Figure 4.28: Level 3, strength X4

4.5 Sizes of the cells

Figure	Cell	Height(μ m)	Width (μ m)
4.1	Level 1 Generation 1	14.72	5.04
4.2	Level 1 Generation 2 X2	14.72	7.04
4.3	Level 1 Generation 2 X4	14.72	13.68
4.4	Level 1 Generation 2 X4B	14.72	9.36
4.5	Level 1 Generation 2 X8	14.72	25.28
4.6	Level 1 Generation 2 X8B	14.72	16.32
4.23	Level 1 Generation 4 X1	21.20	5.52
4.24	Level 1 Generation 4 X4	21.20	11.28

Table 4.1: Sizes of all level 1 layouts drawn

Figure	Cell	Height(μ m)	Width (μ m)
4.7	Level 2 Generation 1	14.72	6.48
4.8	Level 2 Generation 2 X2	14.72	9.36
4.9	Level 2 Generation 2 X4	14.72	13.68
4.10	Level 2 Generation 2 X8	14.72	25.28
4.11	Level 2 Generation 3 X2	17.28	9.36
4.12	Level 2 Generation 3 X4	17.28	9.36
4.25	Level 2 Generation 4 X1	21.20	8.40
4.26	Level 2 Generation 4 X4	21.20	16.32

Table 4.2: Sizes of all level 2 layouts drawn

Figure	Cell	Height(μ m)	Width (μ m)
4.13	Level 3 Generation 1 T1	9.04	11.20
4.14	Level 3 Generation 1 T2	12.96	9.92
4.15	Level 3 Generation 1 T3	10.32	9.92
4.16	Level 3 Generation 1 T4	11.12	7.76
4.17	Level 3 Generation 1 T5	14.72	10.08
4.18	Level 3 Generation 2 X2	14.72	15.92
4.19	Level 3 Generation 2 X4	14.72	27.36
4.20	Level 3 Generation 2 X8	14.72	48.96
4.21	Level 3 Generation 3 X2	17.80	10.08
4.22	Level 3 Generation 3 X4	17.80	17.28
4.27	Level 3 Generation 4 X1	21.20	7.68
4.28	Level 3 Generation 4 X4	21.20	19.92

Table 4.3: Sizes of all level 3 layouts drawn



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