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LPDDR5 System Training

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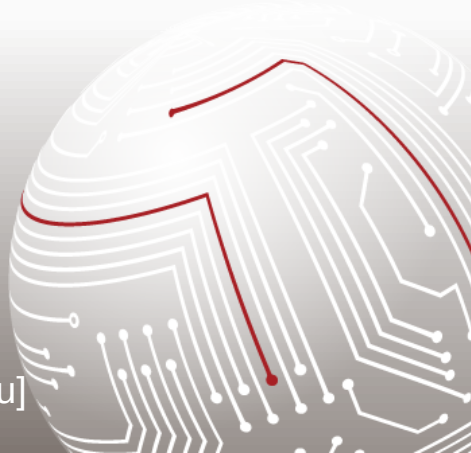


LPDDR5 Workshop

LPDDR5 Interface Training Agenda

- Overview
- Address/command interface
- WCK2CK leveling
- WCK DCA training
- Read gate training
- Data interface training – read and write

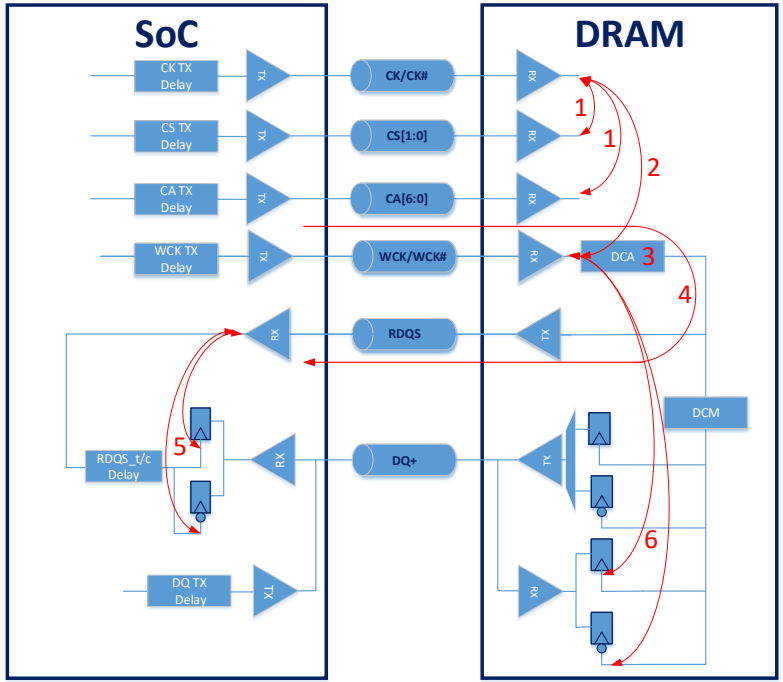
Introduction

- The new LPDDR5 SDRAM interface pushes data rates to **6400 Mbps**
- Boot up trainings are required to operate a parallel interface at such high data rates
- This presentation will focus on the boot trainings required to operate at up to 6400 Mbps
- The following will not be covered:
  - Re-training / drift tracking
  - Command Bus Training with DVFSQ

LPDDR5 training overview

- Critical timing relationships in LPDDR5 and their data rates in an LPDDR5-6400 system
- LPDDR5-6400 bit rates will be used as examples throughout this presentation

Training	Date rate / freq	Training target
1. Command bus training CK – CS CK – CA	800Mbps 1600Mbps	SoC : CA/CS delay DRAM : Vref(CA)
2. WCK2CK leveling CK – WCK	CK 800MHz WCK 3200MHz	SoC : WCK delay
3. WCK Duty cycle training	WCK 3200MHz	DRAM : DCA code
4. Read gate training	RDQS 3200MHz	SoC : Read gate delay
5. Read data training RDQS – DQ/DMI	6400Mbps	SoC : Rx delay, Vref(DQ)
6. Write data training WCK - DQ/DMI/RDQS_t	6400Mbps	SoC : Tx delay DRAM : Vref(DQ)

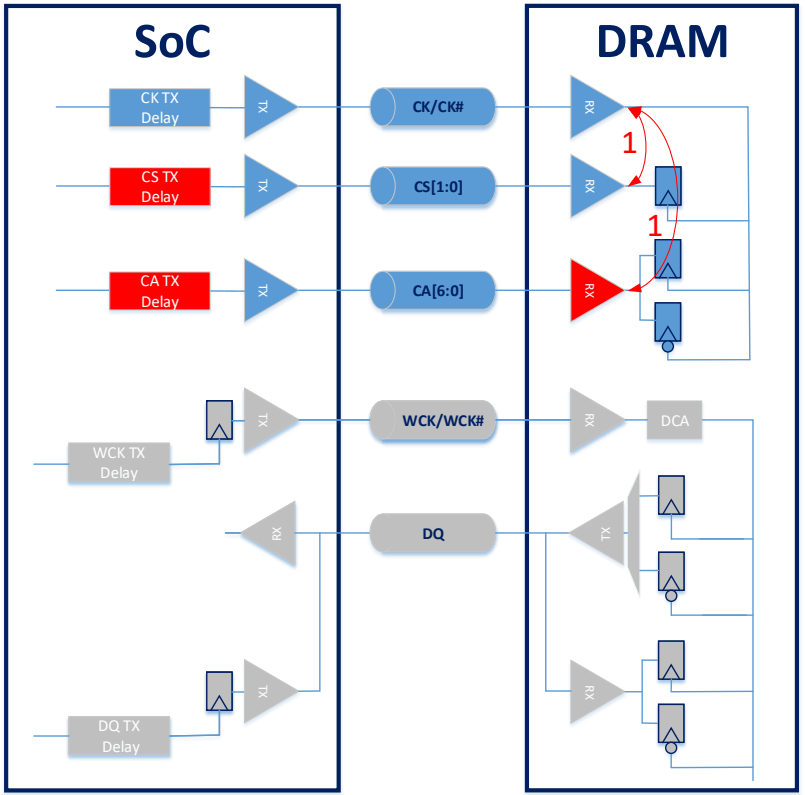


Command Bus Training

LPDDR5 Training: CA and CS

LPDDR5 CS and CA

- The revolutionary LPDDR5 interface decouples address/command clocking from the blisteringly fast data interface
  - CK (clock for address/command) runs up to 800 MHz, while data strobe can reach 3200 MH
- Command bus training is used to train SoC delay of CS and CA and DRAM Vref for CA receivers



LPDDR5 CS and CA training

CS training

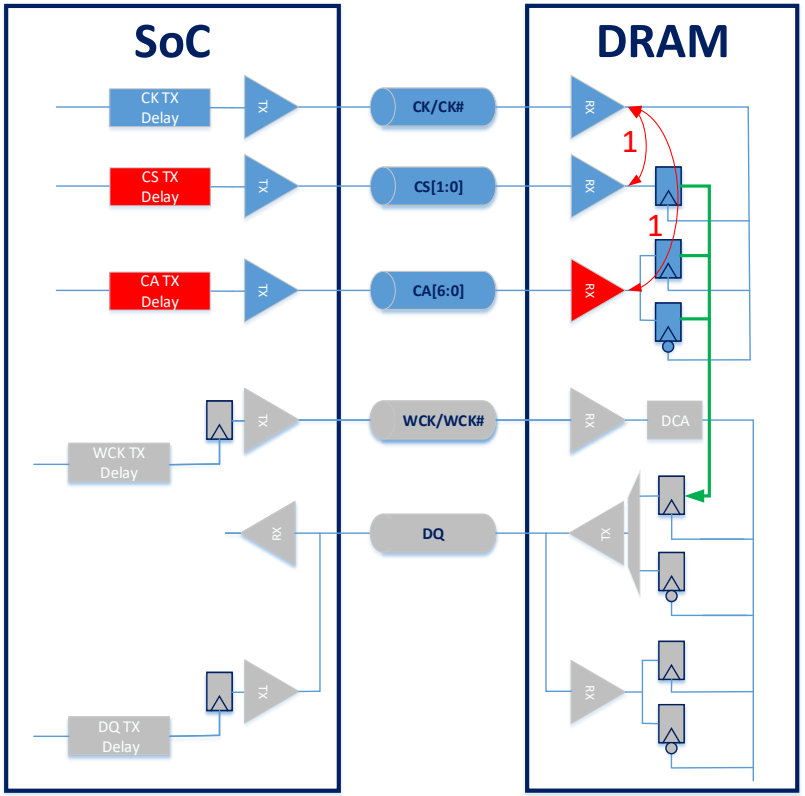
- CS is 800 Mbps, VSS-terminated or unterminated
- CS should be trained for delay to center it on rising edges of CK

CA training

- CA is 1600 Mbps, VSS-terminated or unterminated
- CA Vref should be trained to remove uncertainty in sampling level due to impedance uncertainties
- CA should also be trained for delay to center it on rising edges of CK

LPDDR5 Command Bus Training ("CBT")

- Conceptually similar to LPDDR4 Command Bus Training
- 2 available modes:
  - Mode 1 uses WCK & DQ[7:0] to train delay
  - Mode 2 also requires DMI pin and enables a means to train Vref also without exiting the training mode
- In these modes:
  - data sent on CS and CA and captured on one edge of CK
  - Sampled values are returned statically on DQ pins



LPDDR5 Setup for Command Bus Training

- Prior to entering Command Bus Training:
  - Program all pertinent settings (latencies, termination, Vref, etc.) for one inactive FSP
  - Set VRCG to enable rapid changes in DRAM Vref level
  - Send MRW-1 and MRW-2 “CBT Entry” commands and DQ[7] LOW to enter the training mode
  - Setting DQ[7] HIGH and toggling WCK will change the active FSP
  - The change clock frequency and begin training
- To exit the training mode:
  - Switch DQ[7] LOW to return to the original “known good” FSP
  - With DQ[7] LOW, send MRW-1 and MRW-2 “CBT Exit” commands at low speed

LPDDR5 CBT

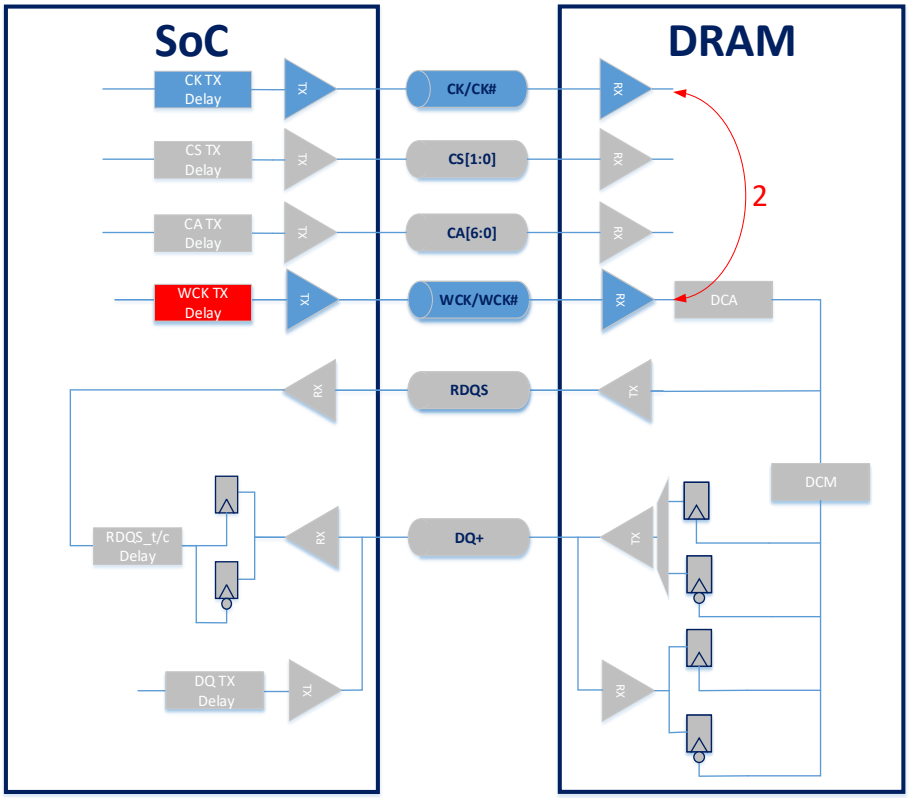
- Mode 1 Training
  - Write MRs to configure one of the unused FSPs
  - Enter Mode 1 training and switch to high frequency
    - New FSP will become active
  - Adjust delays and send commands with CS and CA to train them
    - Responses will be provided on DQ[6:0]
  - If training Vref, exit mode 1 training, change Vref, and re-enter mode 1 training
- Mode 2 Training
  - Write MRs to configure one of the unused FSPs
  - Enter Mode 2 training and switch to high frequency
    - New FSP will become active
  - Adjust delays and Vref(CA) and send commands with CS and CA to train them
    - Setting DMI[0] LOW allows host to provide Vref(CA) setting on DQ[6:0]
    - Responses will be provided on DQ[6:0]

WCK2CK Leveling Training

LPDDR5 Training: Aligning WCK to CK

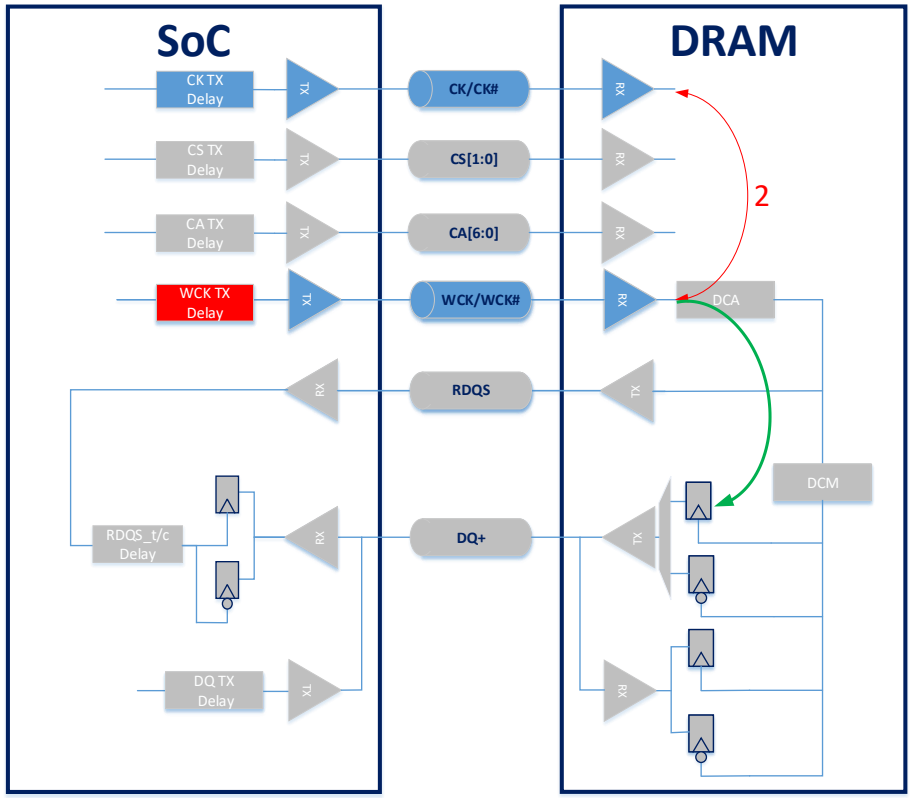
WCK2CK Leveling

- Write leveling aligns WCK strobes to data for each byte and each rank
- Host must adjust WCK delay to align WCK rising edge to CK

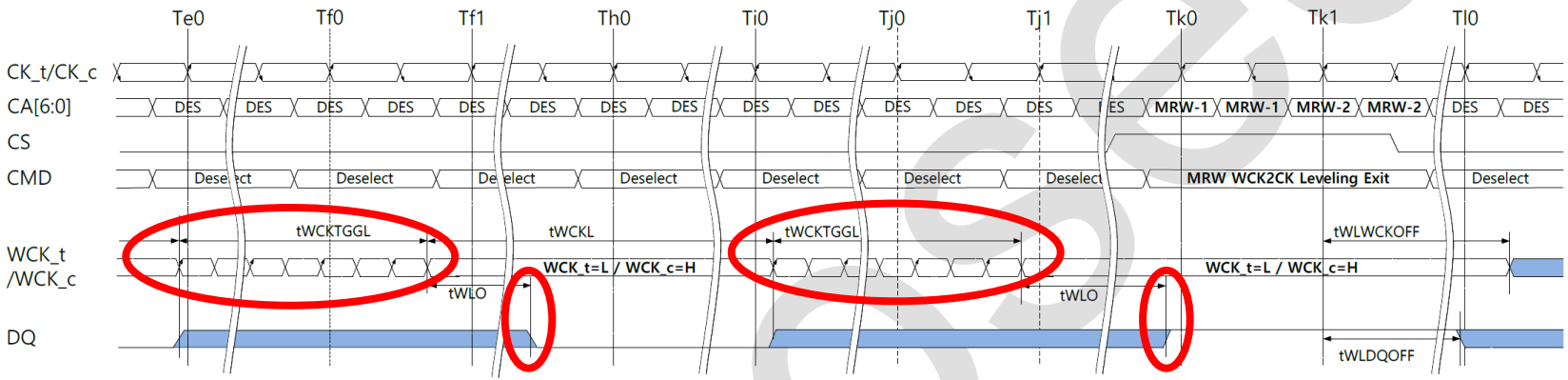


WCK2CK Leveling

- Writing MR18 OP[6]=1 puts the LPDDR5 DRAM into write leveling mode
- In this mode, host should toggle WCK for 8 pulses at a time and a response indicating alignment to CK will be provided on DQ
  - 0 indicates WCK is earlier than CK
  - 1 indicates WCK is later than CK
- SoC should adjust WCK phase delay until alignment is reached



WCK2CK Leveling Example



NOTE 1 DQ output transit from low to high when WCK phase starts to be later than CK phase.
NOTE 2 Controller is allowed to change WCK phase only when it is driving WCK_t=L/WCK_c=H.

Figure 34 — WCK2CK Leveling Exit

Multi-rank Sync-ing

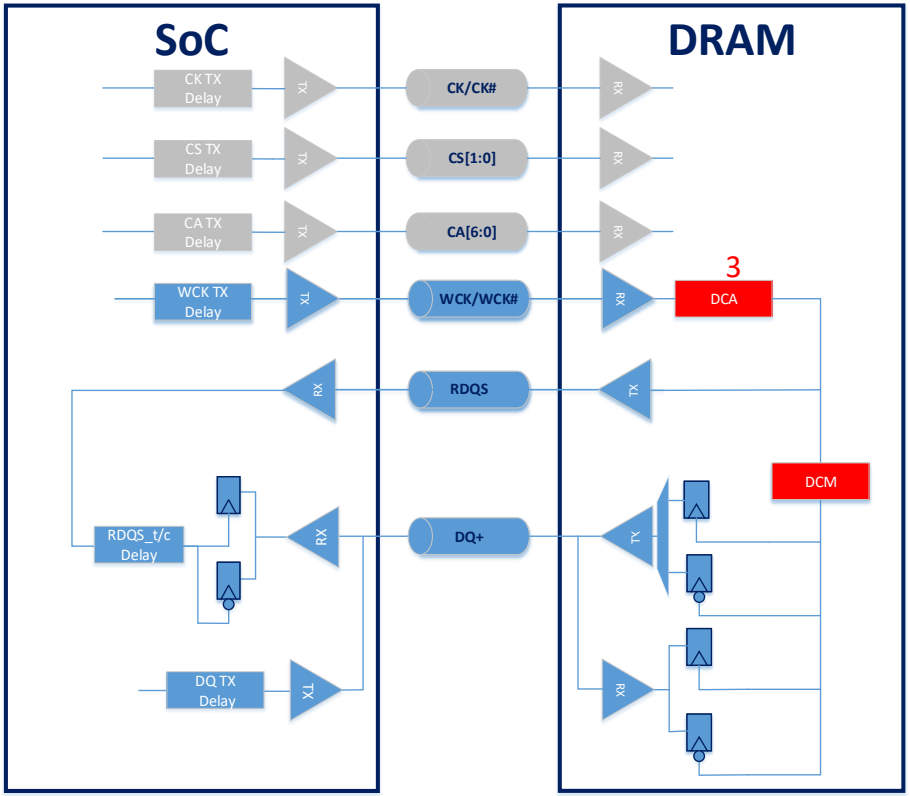
- In multi-rank systems in which performance is a higher priority than power, users may wish to sync WCK to both ranks and keep it always running
- This eats into timing margins, as the leveling requirements may be slightly different at each of the 2 ranks
  - Difference may be up to 100 ps, removing up to 50 ps of accuracy from each rank
  - Timing budgets for CK-WCK alignment must be carefully managed in this case
- To support this, train as described in previous slide and average the results
- Multi-rank systems can also be supported by sync'ing to only one rank at a time
- In this case, no averaging should be done; leveling results should be independent for each byte in each rank

WCK Duty Cycle Training

LPDDR5 Training

WCK Duty Cycle Training

- WCK duty cycle performance is critical to several aspects of performance:
  - RDQS duty cycle
  - Odd/even read DQ launch
  - Odd/even write DQ capture
- As such, LPDDR5 DRAM have built in facilities to support correction of duty cycle:
  - Duty Cycle Adjuster (“DCA”) to control duty cycle
  - Duty Cycle Monitor (“DCM”) to observe duty cycle
  - Ability to reverse inputs to the duty cycle monitor (or “flip”) the monitor in order to correct for asymmetry in the monitor itself



Duty Cycle Training

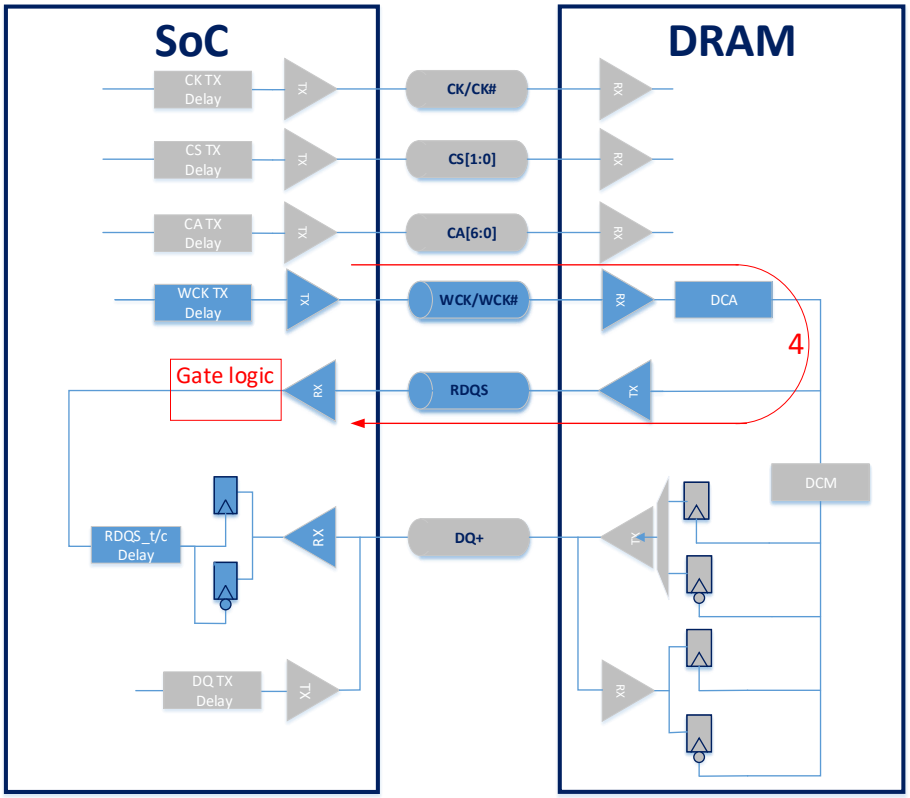
- Issue CAS command with WCK2CK Fast Sync
  - Run WCK at full rate
- Set MR26 OP[0]=1 to initiate DCM operation
- Wait tDCMM for measurement, then flip DCM by setting MR26 OP[1]=1
- Wait tDCMM than set MR26 OP[0]=0 to complete DCM measurement
- Read results for upper and lower bytes from both flip settings from MR26 OP[5:2]
- Adjust WCK duty cycle for both bytes by writing MR30
- Repeat the DCM measurement described at left
- After sweeping DCA and identifying optimal setting, program MR30 for mission mode operation
- In 2 rank systems, do this once for each rank

Read Gate Training

LPDDR5 Training

Read Gate

- The SoC PHY requires some mechanism to determine when to observe RDQS and DQ from DRAM – call this a “read gate”
  - Train the time from read command launch to response arriving at PHY
  - [Read gating logic represented by red box at right]

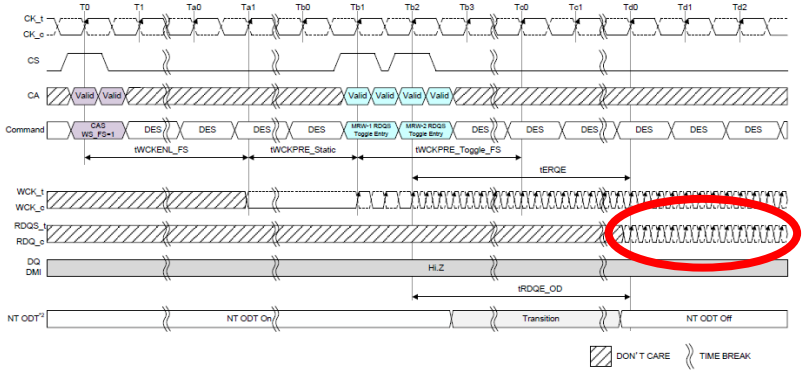


Read Gate Training

- It is useful to be able to train read gate before training read data or write data
- LPDDR5 provides 3 useful functions to that end:
  - RDQS toggle mode provides a continuous RDQS from LPDDR5 DRAM to host. This mode is entered by writing MR46 OP[0]=1.
  - Enhanced RDQS training mode maintains RDQS_t=0/RDQS_c=1 between read bursts. This mode is entered by writing MR46 OP[1]=1.
  - DQ calibration training patterns. Patterns are programmable via MRWs (to MR31 – MR34) without needing the DQ bus to program it.
- There are many possible approaches to training the read gate, but generally an ability to sample RDQS within the PHY without using DQ data is useful
  - With that, the PHY need only sweep the sampling mechanism timing to determine RDQS arrival timing and set the read gate delay accordingly

Read Gate Training Mode Examples

RDQS Toggle Mode (Entry Example)

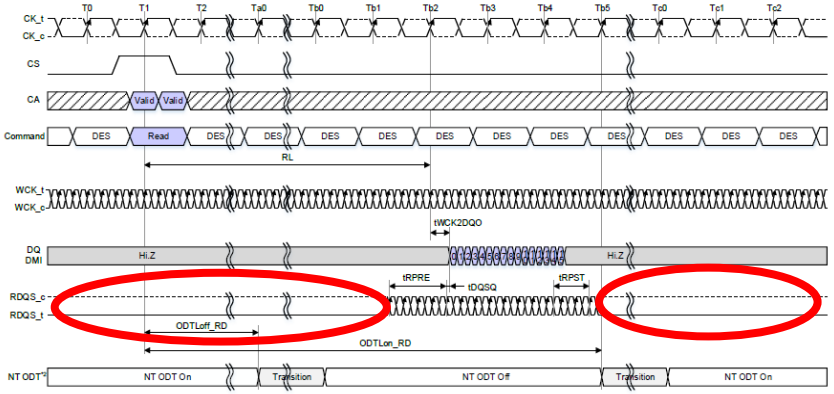


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 "NT ODT" illustrates the On/Off status of NT-ODT for RDQS_t/c, DQ and/or DMI in case of NT-ODT enabled.

Figure 47 — RDQS toggle mode entry timing example

Enhanced RDQS Training Mode (Read during this mode example)



NOTE 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 2. In case of NT ODT is enable case for RDQS_t/c, DQ and/or DMI.

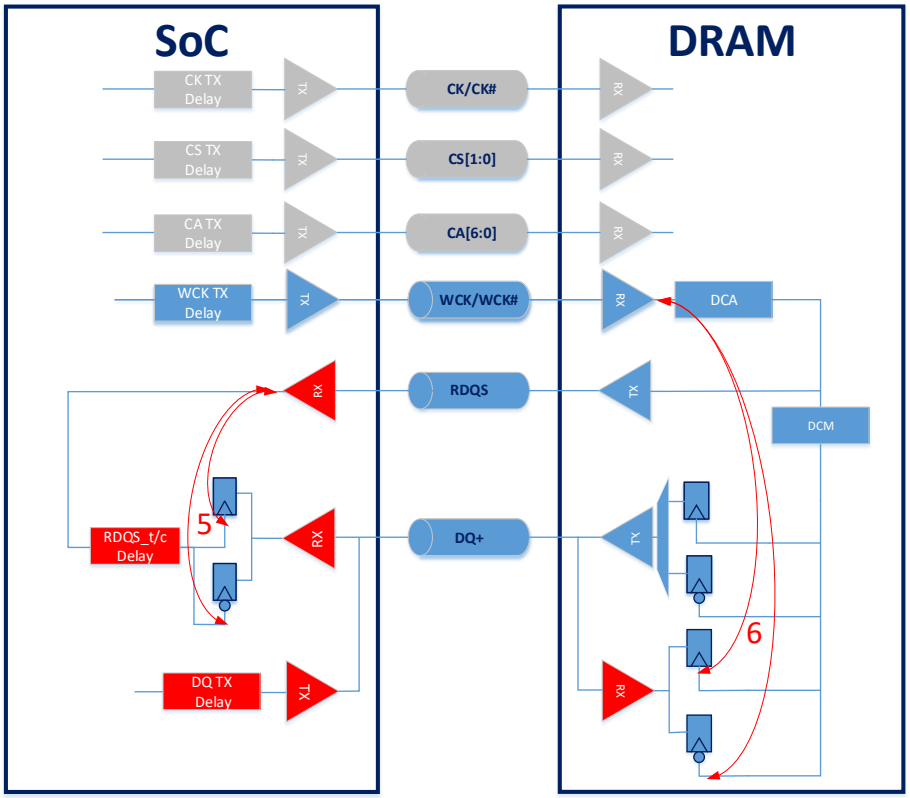
Figure 51 — Read operation during Enhanced RDQS training mode

Write and Read Data Training

LPDDR5 Training

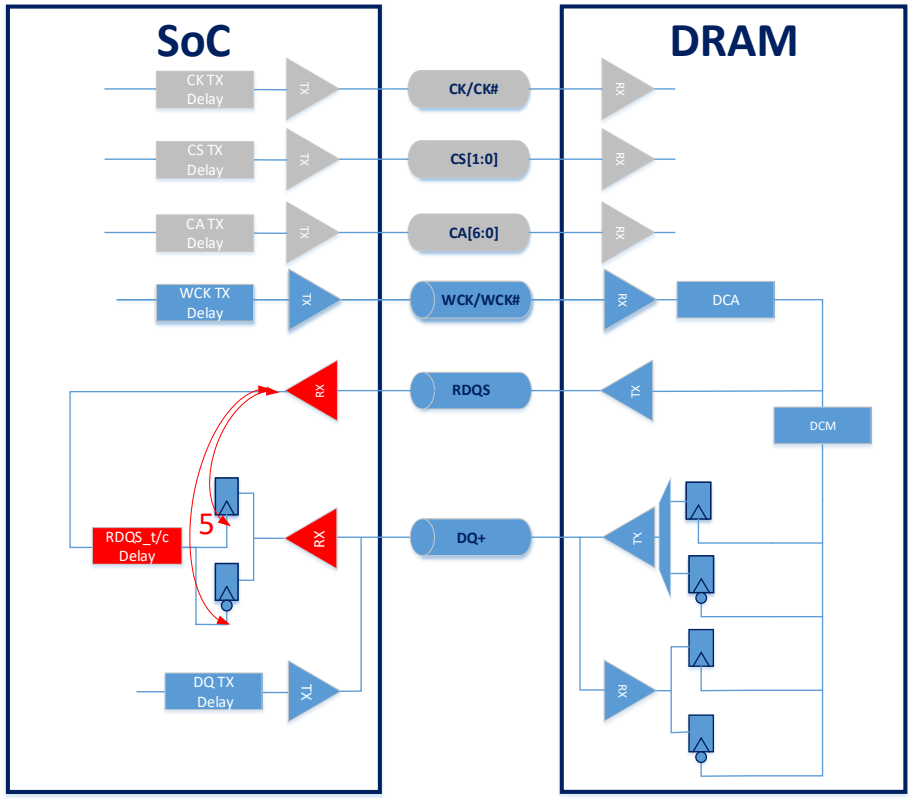
Data Training

- Data training will ensure adequate timing margins for write and read interfaces
  - Read data training consists of training host Vref, equalization (if supported) and delay
    - DQ and DMI are trained to RDQS
    - DQ calibration patterns allow reads to be trained before writes
  - Write data training consists of DRAM DFE and Vref per byte and host bit delay
    - DQ, DMI, and RDQS_t (linkECC) are trained to WCK



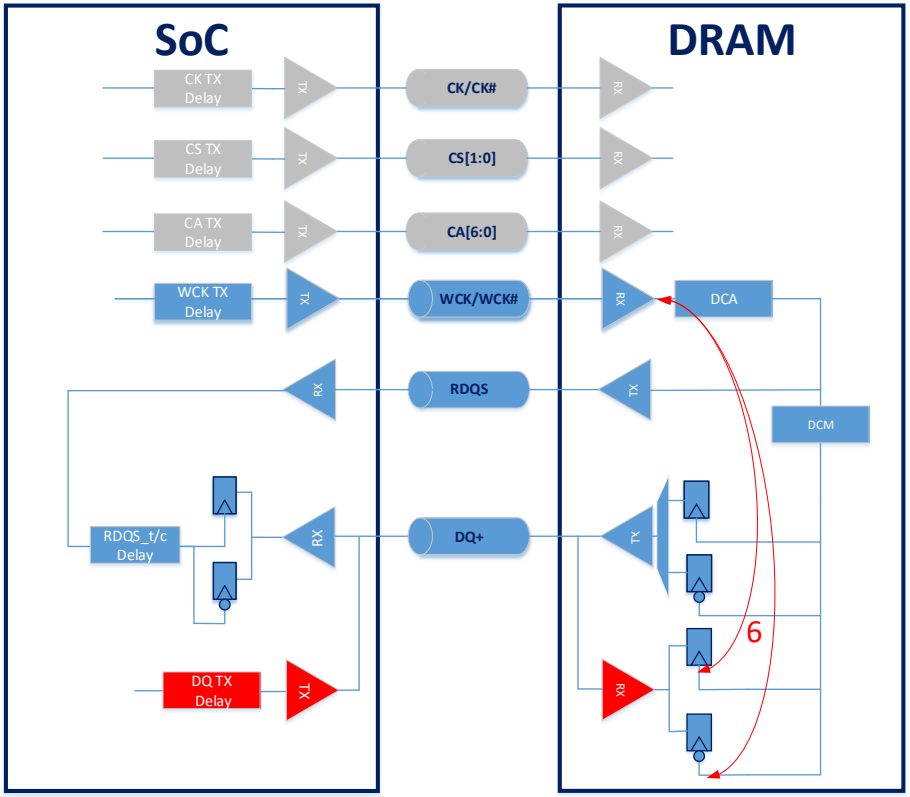
Read Data Training

- Write MR31 – MR34 to set desired DQ training patterns
- Issue Read DQ Calibration (RDC) commands to read the calibration patterns
  - SoC receive delays
  - SoC receive Vref
  - Other SoC receive characteristics, such as equalization



Write Data Training

- Train DQ output delays
  - Optionally, other SoC output characteristics may also be trained here
- With reads trained previously, writes may be trained
  - LPDDR5 includes a FIFO that may be used for training with less protocol overhead than DRAM
    - No activate, precharge, or refreshes required
    - FIFO is 8 x BL16 deep
  - Alternately, DRAM memory may also be used instead of the FIFO
    - Enables arbitrarily long training patterns for even more stressful training than the FIFO allows

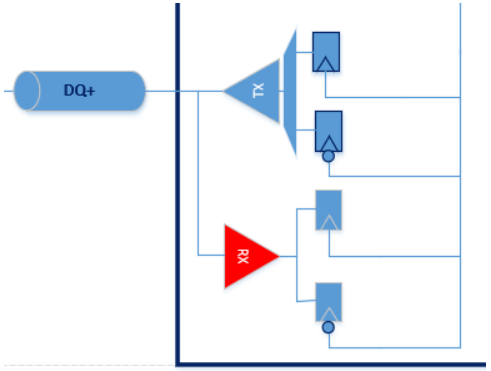


Write Data Training – DMI and RDQS_t

- Training DMI pin requires special consideration
  - Option 1 : Using LPDDR5's training FIFO DMI pin can be trained at the same time as DQ pins
    - Write data on DMI is written to FIFO, and these data can be read-out by Read FIFO command
  - Option 2 : Using main memory DMI pin can be trained after DQ
    - In this case, failures on DMI sampling with complex patterns may be difficult to discern from failures in other DQ bits
- Training RDQS_t (parity) also requires special considerations
  - Option 1 : Using LPDDR5's training FIFO with WCK-RDQS_t training mode (MR46 OP[2] = 1)
    - Write data on RDQS_t is written to FIFO, and these data can be read-out via DMI pin by Read FIFO command
    - RDQS_t cannot be trained at the same time as DQ/DMI. If both DMI and RDQS_t are used in a system, 2 iterations are required, once to train with DQ/DMI and another to train with RDQS_t
  - Option 2 : Using LPDDR5's Read/Write-based WCK-RDQS_t training mode (MR26 OP[7] = 1)
    - This mode is available only when DRAM supports it (MR26 OP[6] =1)
    - RDQS_t behaves like DMI pin, and DMI input is ignored. DRAM inverts write data on DQ inputs when RDQS_t is sampled High.

DRAM DFE Training

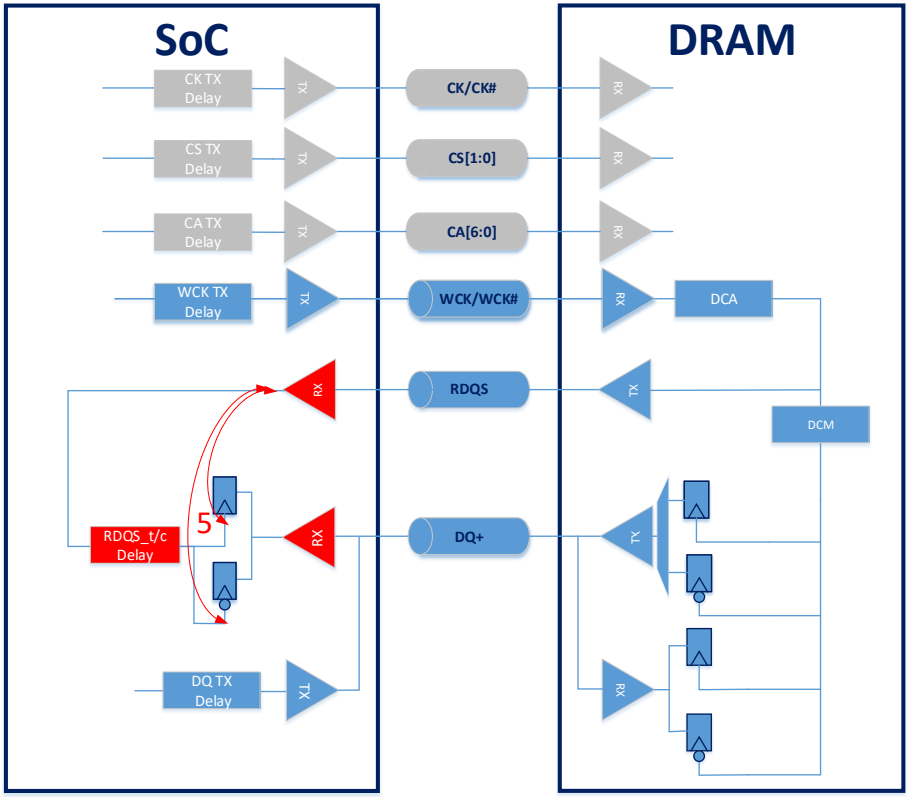
- LPDDR5 includes support for Decision Feedback Equalization (DFE)
- The DFE is 1 tap – equalization is based on the previous bit sent
- The 1 tap has 8 possible settings (3 bits programmability), independently programmable for each rank and byte
- Use of DFE is optional



- Training procedure:
  - Set the DFE quantity in MR24
  - Perform writes to DRAM and read back
    - DRAM memory or training FIFO may be used to do this
  - Adjust DFE quantity in MR24 and repeat training patterns

Read Data Refinement (Optional)

- Calibration training patterns restrict the complexity of data patterns that can be used for training
- After write training is completed, additional read training with more complex data patterns is possible
- The LPDDR5 FIFO or the DRAM array may be used for refining read training



LPDDR5 training mode summary

- User can select appropriate training mode to optimize performance in LPDDR5 system

Training	Training mode / command	MR : mode selection	Support Indicator	Note
1. Command bus training	- CBT mode1 - CBT mode2	MR13 OP[6] = 1 MR13 OP[6] = 0	Supported	Mode 1 is for DMI-less system
2. WCK2CK leveling	- WCK2CK leveling mode	MR18 OP[6] = 1	Supported	
3. WCK Duty cycle training	- MRW : DCM start	MR26 OP[0] = 1	Supported	
4. Read gate training	- Enhanced RDQS training mode - RDQS toggle mode	MR46 OP[1] = 1 MR46 OP[0] = 1	Supported	
5a. Write data training	- Training FIFO for DQ/DMI - Training FIFO for RDQS_t - Read/Write-based WCK-RDQS-t training mode	MR46 OP[2] = 0 MR46 OP[2] = 1 MR26 OP[7] = 1	Supported Supported MR26 OP[6]	
5b. DRAM DFE training	- MRW MR24 (DFE quantity)	no mode select	MR24 OP[7]	
6. Read data training	- RDC command - Training FIFO	no mode select	Supported	MR20, 31-34 define RDC data pattern

Periodic Retraining

- Some LPDDR5 DRAM timing parameters can drift over time with voltage and temperature
  - tWCK2DQO : Read response timing for RDQS + DQ
  - tWCK2DQI : Write WCK-to-DQ offset
- Consequently, periodic updates to the following trainings will be necessary to track temperature and low-frequency voltage changes:
  - Write data training to track tWCK2DQI
  - Read gate training to track tWCK2DQO

Thank You

- Question?