A 1.8-V 22-mW 10-bit 30-MS/s Pipelined CMOS ADC for Low-Power Subsampling Applications

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***Abstract*—This paper describes a 10-bit 30-MS/s subsampling pipelined analog-to-digital converter (ADC) that is implemented in a 0.18 μm CMOS process. The ADC adopts a power efficient amplifier sharing architecture in which additional switches are introduced to reduce the crosstalk between the two opamp-sharing successive stages. A new configuration is used in the first stage of the ADC to avoid using a dedicated sample-and-hold amplifier (SHA) circuit at the input and to avoid the matching requirement between the first multiplying digital-to-analog converter (MDAC) and flash input signal paths. A symmetrical gate-bootstrapping switch is used as the bottom-sampling switch in the first stage to enhance the sampling linearity. The measured differential and integral nonlinearities of the prototype are less than 0.57 least significant bit (LSB) and 0.8 LSB, respectively, at full sampling rate. The ADC exhibits higher than 9.1 effective number of bits (ENOB) for input frequencies up to 30 MHz, which is the twofold Nyquist rate (fs/2), at 30 MS/s. The ADC consumes 21.6 mW from a 1.8-V power supply and occupies 0.7 mm^2, which also includes the bandgap and buffer amplifiers. The figure-of-merit (FOM) of this ADC is 0.26 pJ/step.**

***Index Terms*—Analog-to-digital converter, opamp sharing, sample-and-hold, SHA-less, subsampling.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) used for subsampling applications are becoming popular because they allow a system designer to reduce the number of down-conversion stages in the receiver signal chain and thereby reduce system costs. Many of the applications such as battery-powered portable devices also require low power consumption. For example, in the digital video broadcasting over terrestrial (DVB-T) and handheld (DVB-H) systems, a low-power 10-bit ADC that runs at tens of mega hertz clock frequency and can deliver the required performance in a direct IF (intermediate frequency) sampling architecture is required [1]. Thus, optimized implementations of low-power ADCs play an important role when high-performances are targeted.

In this paper, a 1.8-V 10-bit 30-MS/s CMOS ADC with high dynamic performance for input signals much above the Nyquist rate and low power dissipation, is demonstrated. The ADC adopts a power efficient amplifier sharing architecture in which additional switches are introduced to reduce the crosstalk between the two opamp-sharing successive stages. A new configuration is used in the first stage of the ADC to avoid using a dedicated sample-and-hold amplifier (SHA) at the input and to avoid the matching requirement between the first multiplying digital-to-analog converter (MDAC) and flash input signal paths. In order to enhance the sampling linearity, a symmetrical gate-bootstrapping switch is used as the bottom-sampling switch in the first stage. The ADC also includes the on-chip current–voltage (I–V) references.

This paper is organized as follows. Section II presents the architectural considerations for the ADC. Section III describes the design of the ADC. Section IV shows the experimental results. This paper concludes with Section V.

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II. ADC Architecture

The design target is a low-power high-performance CMOS ADC with a resolution of 10 bits and a conversion speed of 30 MS/s. Among various ADC architectures, pipelined ADCs have proven to be very efficient architectures for meeting the low power dissipation, medium resolution and high input bandwidth requirements [1]–[8], [10]–[16], [18], [25]–[29].

There are many schemes used in the pipeline architecture to reduce the power consumption. However, the performance of the pseudo-differential architecture [2] is more sensitive to the common mode voltage and substrate or power supply noise compared with that of the fully differential one. Also, the performance of the time-interleaving architecture [3], [4] is sensitive to offset and gain mismatches as well as aperture errors between the interleaved channels. Complex calibration schemes [5] and/or circuit techniques [6] are usually needed to correct the mismatches. The opamp sharing architecture [7], [8] shares an opamp between two consecutive stages, so it only needs half the number of opamps and thereby significantly reduces power consumption.

In pipelined architectures, the number of bits converted per stage significantly affects the converter's overall performance. For fewer bits per stage, the subflash ADC requirements are more relaxed, and the speed of the stage is faster due to the larger feedback factor. However, more pipeline stages are required, and the noise and gain errors of the later stages contribute more to the overall converter inaccuracy. This means that as the number of bits per stage gets too small, the total power consumption may increase. Conversely, for more bits per stage, fewer pipeline stages are required, and the noise and gain errors of the later stages contribute less to the overall converter inaccuracy. Also, multiple bits in the first stage can reduce the ADC's

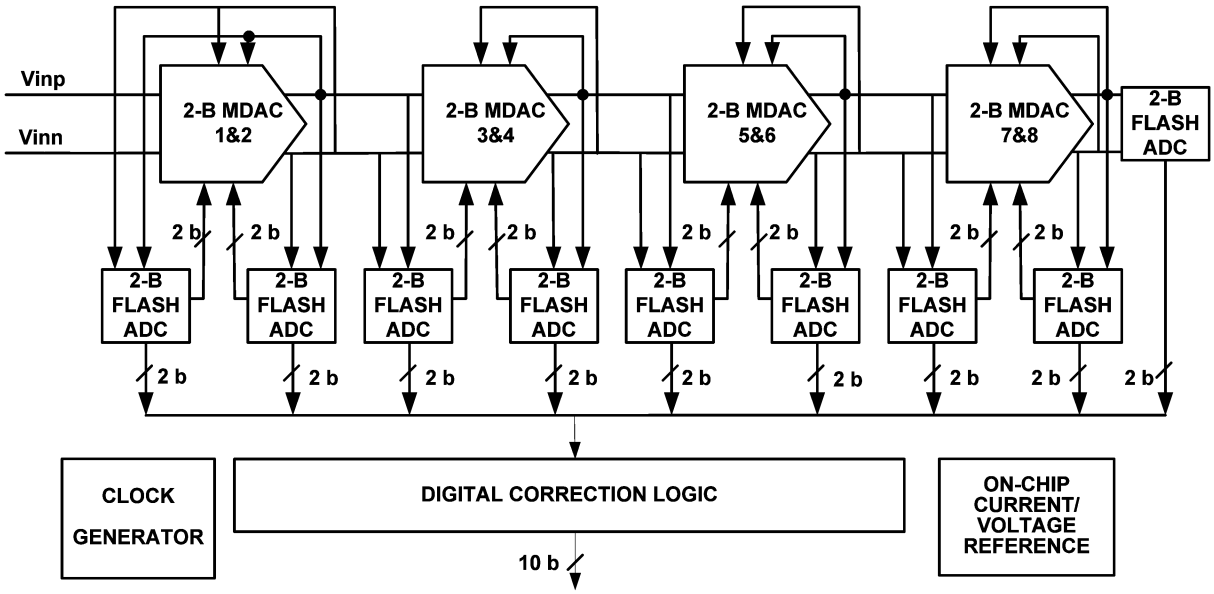

Fig. 1. Block diagram of the proposed ADC.

dependency on the capacitor matching [9]–[11]. However, more bits per stage also means that the subflash ADC needs to be more accurate and a higher number of comparators, and the opamp in the stage needs a larger gain bandwidth. Hence, as the number of bits per stage gets too large, the total power consumption also increases.

A detailed analysis about this topic has been done in [12]. It is shown that for high-speed conversions, a 2–3 bits per stage architecture is optimum when the design constraint is the signal-to-noise ratio (SNR). However, the problem is complex in practice and may not be easily modeled. So the actual choice depends on the overall ADC specifications, the particular process technology, and the layout. In this work, a resolution of 1.5 bits/stage [13], [14] is chosen because this architecture can maximize the bandwidth of the MDAC circuit and has the benefits of simplicity [14].

Consequently, the block diagram of the proposed 10b ADC is illustrated in Fig. 1. The ADC does not use a dedicated SHA at its input and is based on a 1.5 bits/stage [13], [14] pipeline with amplifier sharing architecture [7]. It consists of eight 2-bit multiplying digital-to-analog converters (2-B MDAC) with sharing amplifier between two consecutive ones, nine 2-bit subflash ADCs (2-B FLASH ADC), digital correction logic, clock generators and on-chip I–V references. The operation of the MDAC and the flash in the first stage is different from that of the other stages, which will be explained in Section III.

III. Circuit Design of the ADC

In this section, architectural as well as circuit design techniques are described to further reduce the power consumption and improve the performance of the ADC for inputs with frequencies much above the Nyquist rate.

A. First Stage With Sample-and-Hold Function

1) Motivation: A front-end SHA is widely used in high-speed ADCs because it minimizes the aperture error caused by the sampled signal mismatch between the MDAC and the comparators in the subflash ADC in the first stage. However, the SHA usually has very large power dissipation and contributes substantially to the distortion and noise of the whole ADC. Removing the SHA at the front end can save power dissipation and area. However, the aperture error may become unacceptably large without the SHA. Carefully matching the time constant between the two signal paths can reduce the aperture error [15], [16]. However, there are two potential problems with the matching technique.

1) The matching technique requires very careful layout and routing. This is because the aperture error is mainly caused by the sampling clock skew and the signal-path bandwidth mismatch between the MDAC and the comparators in the subflash ADC. So the clock buffers and routing as well as the sampling switches for the two signal paths should be well matched to minimize the sampling clock skew. Also, the input signal propagation for the two signal paths should be well matched.
   More importantly, the technique may not be available for high-speed and high-resolution applications in modern deep-submicron CMOS fabrication process due to the limited attainable level of matching, especially when parasitics and variations in temperature, supply voltage and process are considered.
2) The matching technique requires the flash to have a similar sampling network as the MDAC in the first stage. This limits the topology selection for the comparator used in the flash. For example, a high-speed dynamic comparator in [17] is not suitable to be used in the flash when the matching is required. However it is used in the proposed SHA-less architecture which will be explained next.

2) The Proposed Configuration: In order to avoid the matching requirement and thus eliminate the above potential problems in the traditional SHA-less ADC, a new configuration of the first stage (shown in Fig. 2) is developed [18]. The

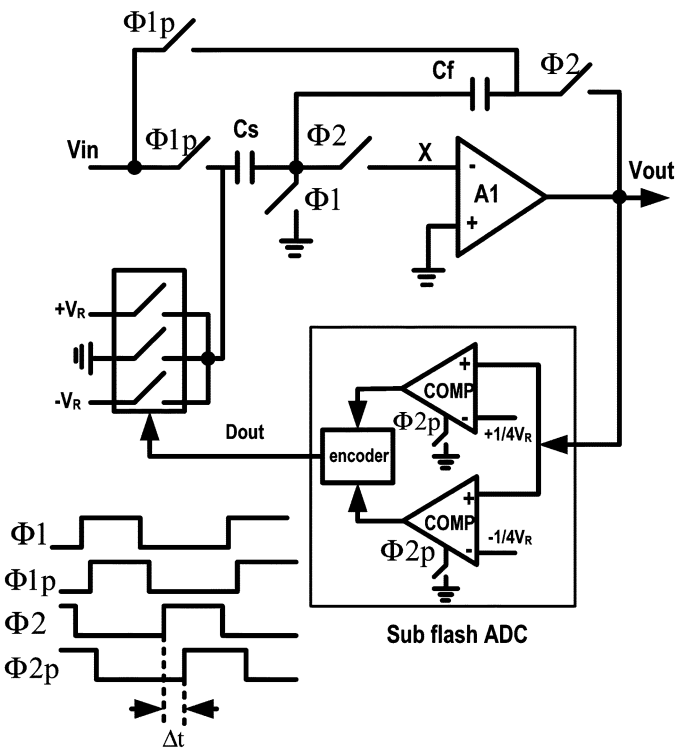

Fig. 2. Proposed first stage of the ADC.

development of the configuration is based on the observation that there actually exists a sample-and-hold operation in the traditional pipeline stages.

The operation of the stage can be described as follows. The input voltage $V_{\rm in}$ is sampled on capacitors Cs and Cf at the end of the phase $\Phi 1$. During phase $\Phi 2$, the capacitor Cf is placed around the amplifier A1. Since the amplifier's high gain requires that node X still be a virtual ground and because the charge on the capacitor Cf must be conserved, the output voltage $V_{\rm out}$ will reach to a value approximately equal to that of the input voltage $V_{\rm in}$. The comparator clock $\Phi 2p$ is enabled after the amplifier goes into the settling operation. So the output voltage $V_{\rm out}$, which is approximately equal to the input voltage $V_{\rm in}$, is quantized through the subflash ADC. The comparison error due to insufficient settling can be reduced to the required range by enlarging the Δt, which is the delay time between the rising edges of $\Phi 2$ and $\Phi 2p$ and can be recovered by the digital error correction. Depending on the resolved bits $D_{\rm out}$ of the subflash ADC, the left plate of Cs is switched to $+V_R$, $-V_R$ or ground to perform the digital-to-analog conversion, subtraction and amplification for the residue signal.

So the operation of the proposed first stage is the same as that of the traditional pipeline stage except for holding the input signal during Δt. Although Fig. 2 shows the single-ended 1.5-bits/stage architecture, the proposed first stage could be used in any bits per stage architecture, and the actual implementation is fully differential.

3) The Required Additional Time: From the operation of the proposed first stage, it can be inferred that the opamp used in the proposed first stage needs to be faster due to the delayed flash decisions (Δt in Fig. 2). This means that more power should be consumed by the first stage. However, the following calculation will show that the amount of the saved power due to removing the SHA is much larger than the additional power consumed by the first stage opamp.

For simplicity, assume that A1 is a single-pole opamp and the total settling time of the circuit is equal to the linear settling (i.e., exponential settling) time. The effect of the nonlinear settling (i.e., the slewing) time will be considered later. Consider the operation of the circuit in Fig. 2. Between phase $\Phi 2$ and $\Phi 2p$ (during Δt), the feedback factor of the circuit is approximately 1, so the closed-loop bandwidth $\rm BW_1$ is

$$\mathrm{BW}_1 = \frac{Gm}{C_L} \tag{1}$$

where Gm is the transconductance of the opamp, and C_L is the output load capacitance. Assume that $V_{\rm FS}$ is the full-scale signal range. The largest error ε_1 caused by the incomplete linear settling of the opamp during Δt is given by

$$\varepsilon_1 = V_{\rm FS} e^{-\mathrm{BW}_1 \Delta t}. \tag{2}$$

For correct operation, the incomplete settling error must not exceed the digital error correction range (assume 1 bit for redundancy, which is a typical case). That is

$$\varepsilon_1 \le \frac{V_{\rm FS}}{2^{B1+1}} \tag{3}$$

where $B1$ is the number of the resolved bits in the first stage (For 1.5-bits/stage architecture, $B1$ is 2). From (1), (2), and (3)

$$\Delta t \ge \frac{(B1+1)C_L}{Gm} \ln 2. \tag{4}$$

After $\Phi 2p$ is enabled, the feedback factor is approximately $1/2^{B1-1}$, so the closed-loop bandwidth $\rm BW_2$ is

$$\mathrm{BW}_2 = \frac{1}{2^{B1-1}} \frac{Gm}{C_L}. \tag{5}$$

In order to fulfill the resolution requirement, the largest incomplete settling error ε_2 within the required time t_s must not exceed LSB/2 referred to the remaining resolution [9]. For an N bit ADC, that is

$$\varepsilon_2 = V_{\rm FS} e^{-\mathrm{BW}_2 t_s} \le \frac{1}{2} \frac{V_{\rm FS}}{2^{N-B1+1}}. \tag{6}$$

Substituting (5) into (6) gives

$$t_s \ge \frac{(N-B1+2)2^{B1-1}C_L}{Gm} ln2. \tag{7}$$

The above calculation for t_s neglects the comparator's comparison time, because the time is usually very small compared with the period of the sampling clock. However the comparison time should be added into (7) when the time is comparable to the period of the clock.

Δt in (4) is the additional required time. t_s in (7) is the required time (necessary time for the traditional pipeline stage) for the circuit to generate the residue signal. Dividing the minimum

required Δt in (4) by the minimum required t_s in (7) gives the normalized additional time t_n:

$$t_n = \frac{\Delta t_{\min}}{t_{s_{\min}}} = \frac{(B1+1)}{(N-B1+2)2^{B1-1}}. \quad (8)$$

As shown in (8), t_n is decreased with increased ADC resolution N. This is because the required Δt in (4) is only dependent on the resolution of the first stage $B1$, and the required settling time t_s is proportional to N. Equation (8) also indicates that t_n is decreased with increased $B1$. This is because the required Δt in (4) is proportional to B1, whereas the required t_s in (7) is proportional to 2^{B1-1}. So for higher ADC resolution and/or higher resolution of the first stage, the normalized additional time t_n is smaller. In this work, where N is 10, and $B1$ is 2, the t_n is 0.15 (15%).

In the above analysis, the settling time is assumed to be equal to the linear settling time. In practice the settling time of the circuit is firstly determined by the nonlinear slew time and finally by the linear settling time. So the slew time should be added to the required linear settling time in the above analysis. But in this design, the slew time is small compared with the linear settling time. And it is pointed out in [19] that because the slew rate scales with the bandwidth, typically for high-bandwidth opamps the slew time is small compared with the linear settling time.

The front-end SHA consumes a significant amount of power, and contributes substantially to the distortion and noise of the whole ADC. So, generally, for pipelined ADCs more than half of the original ADC power can be saved by not using the SHA [20]. And according to the reported data from previous publications such as [2] and [29], the first-stage opamp (the opamp used in the MDAC of the first pipeline stage) generally consumes less than half of the total pipeline stages power (i.e., stages 1 and beyond). So the assumption can be made that if there is no power consumption due to the delayed Δt in the proposed SHA-less ADC, the first-stage opamp consumes half of the SHA-less ADC power, and the SHA-less ADC consumes half of the power consumed by the one with a SHA. Then when the additional power consumed by the first-stage opamp due to the delayed Δt is equal to the saved power by removing the SHA, the power consumed by the first-stage opamp is three times that of the original one. This means that the first-stage opamp in the proposed architecture could be approximately the square root of three times faster for the same size transistor (i.e., Δt could be approximately equal to 73% of t_s). So, based on the above estimations, the proposed architecture is advantageous (in terms of power) as compared to the traditional front-end SHA approach as long as Δt is less than 42% of the totally allowed settling time (the sum of Δt and t_s).

The traditional SHA-less architecture [15], [16], which employs the matching technique, also needs the opamp and comparator in the first stage to be faster than that in the traditional front-end SHA approach due to the absence of a held signal. This means more power consumed in the first stage. The comparison between the additional power consumption in the proposed first stage and that in the traditional SHA-less first stage depends on the architectures and designs of the opamp and comparator. Even if the power consumption of the amplifier in the proposed first stage is beyond what is needed with a traditional SHA-less structure, the excess power is not significant since the additional power in the proposed architecture is already relatively small as indicated by (8) for most applications. But the proposed architecture has the advantage of eliminating the matching requirement along with the potential problems.

Another point worth mentioning is that the feedback factor of the circuit is approximately 1 during Δt and becomes approximately $1/2^{B1-1}$ after $\Phi 2p$ is enabled. This, however, is not a problem in practice if the circuit is unity-gain stable. Actually, little ringing at the output due to the reduced phase margin because of the increased feedback factor during Δt can provide a fast settling as long as the overshoot of the ringing is within the digital error correction range of the stage. There is no other particular consideration of the opamp for being used for the subflash (during Δt) and the MDAC (after $\Phi 2p$ is enabled), since there is no other difference between the two situations. Because the opamp used in the proposed first stage needs to be faster than the one in the traditional first stage, the proposed structure may not be suitable for the ADCs that are expected to run at the maximum achievable sampling rate for a given resolution and technology. That can be considered as a drawback of the structure.

4) Another Possible Configuration: In fact during Δt, the loading capacitors, which are the sampling capacitors of the next stage, are not necessarily connected to the output of the amplifier. This is because during this time the output of the amplifier is taken for quantization by the subflash ADC of the first stage instead of being sampled by the next stage. So the value of the opamp output loading capacitor during Δt could be much smaller than the one after $\Phi 2p$ is enabled. This means that much more power could be saved. However, this configuration is not used in this work because the amplifiers used in the ADC employ a one-stage gain-boosting telescopic architecture [21], whose dominant pole is located at the output, which is sensitive to the value of the output loading capacitor. However, the configuration could be employed to save more power when other amplifier topologies, whose output pole is a non-dominant pole, are used. For example, if a two-stage miller-compensated opamp is employed, one can use a small compensation capacitor according to the small loading capacitor during Δt and switch to a large compensation capacitor according to the large loading capacitor after $\Phi 2p$ is enabled. Then the opamp could have a faster settling behavior during Δt since the biasing current is constant, and not only the loading capacitor but also the compensation capacitor is small during the time. This means that Δt could be smaller than the value predicted above, and thus the additional power consumption due to Δt can be reduced. This possible configuration may be useful when Δt predicted in Section III-A3 is relatively large.

B. The Symmetrical Gate-Bootstrapping Switch

The performance of the ADC with a relatively high frequency input signal is largely dependent on the performance of its front-end. In order to deal with high-frequency inputs, gate-bootstrapping switches shown in Fig. 3 [22] are used as the input-sampling switches (the switches controlled by $\Phi 1p$ in Fig. 2) to reduce signal distortion by keeping the gate-source voltage of the

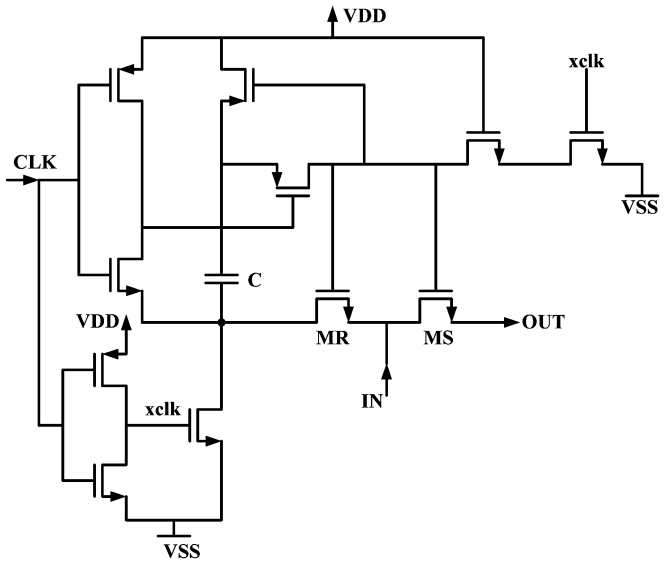

Fig. 3. Conventional gate-bootstrapping circuits used for input-sampling switches.

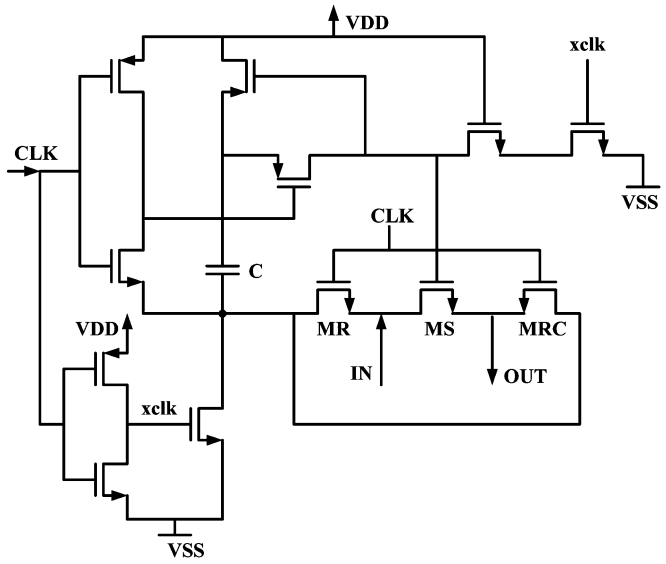

Fig. 4. Symmetrical bootstrapped switch with modified timing used for bottom-sampling switch.

sampling switches constant. The switch controlled by $\Phi 1$ shown in Fig. 2 is called a bottom-sampling switch. It is used for the purpose of providing a virtual ground during the sampling operation. But the virtual ground is not so perfect in practice because of the on-resistance of the bottom-sampling switch. As a result, the released charge is not totally signal-independent when the switch is turned off. So it is also preferred to use a gate-bootstrapping switch as the bottom-sampling switch to reduce the on-resistance as well as make the escaped charge less signal-dependent [23].

The implementation of the circuit shown in Fig. 2 is fully differential. And the two sets of the input sampling capacitors, which are used to sample the differential input signal, are connected by the bottom-sampling switch when they are sampling the input signal. So the traditional gate-bootstrapping switch such as the one in Fig. 3 is not suitable to be used as the bottom-sampling switch, because the switch is not symmetrical around the main switch MS. When the switch is turned off, the charge escaped from the circuit can not be equally distributed to IN and OUT in Fig. 3, and thus can distort the sampled signal charges. A symmetrical gate-bootstrapping switch [24] with modified timing is used as the bottom-sampling switch to mitigate the problem. The symmetrical gate-bootstrapping switch (shown in Fig. 4 [25]) has a symmetrical architecture. Thus, the charge escaped from the circuit can be evenly distributed to IN and OUT in Fig. 4. The amount of the released charge could be reduced if the transistors MR and MRC are turned off slightly before the switch transistor MS, which is realized by connecting the gates of MR and MRC to CLK.

Table I shows the simulated total harmonic distortions (THD) (first five harmonics are calculated) of a sample-and-hold circuit, whose bottom-sampling switch is realized by symmetrical gate-bootstrapping switch, nMOS switch, and traditional bootstrapping switch, respectively. The input signal frequency fin is 59 MHz and the sampling frequency fs of the sample-and-hold circuit is 30 MHz in the simulation. As shown in the table, the symmetrical gate-bootstrapping switch provides 5 and 15 dB improvement of linearity as compared to the nMOS switch and the traditional bootstrapping switch, respectively.

TABLE I
THD SIMULATION RESULTS OF A SAMPLE-AND-HOLD CIRCUIT

Type of the bottom-sampling switch	Symmetrical bootstrap switch	NMOS switch	Traditional bootstrap switch
THD (dBc)	84	79	69

C. Opamp Sharing

Fig. 5 shows the opamp-sharing architecture [7], opamp A1 is shared between the two successive stages (e.g., S-A and S-B), thereby significantly reducing power consumption. However, there is a potential crosstalk path between the two opamp-sharing successive stages due to the parasitic capacitors (e.g., Cp1 and Cp2) introduced by the switches which are used to implement amplifier sharing [12]. In Fig. 5, the switch is on when its corresponding control signal (i.e., $\Phi 1$, $\Phi 1p$, $\Phi 2$, or $\Phi 2p$) is high. The switch is off when its corresponding control signal is low. At first, ignore the switches in the dashed boxes. When $\Phi 1p$ is high (when the S-B stage is generating the residue signal), any signals (may be the settling signal from the previous stage or kickback noise generated by the subflash ADC etc.) appearing at node Vi of S-A will influence the signal fidelity in S-B through the crosstalk path (through C1, C2, and Cp1 to the input of A1). Similarly, when $\Phi 2p$ is high (when the S-A stage is generating the residue signal), any signals appearing at node Vo will influence the signal fidelity in S-A through the crosstalk path (through C3, C4, and Cp2 to the input of A1).

To mitigate the problem, additional switches (shown in the dashed boxes of Fig. 5) are introduced [18]. When $\Phi 1p$ is high, the right side of the parasitic capacitor Cp1 is tied to ground by the corresponding added switches to isolate the two

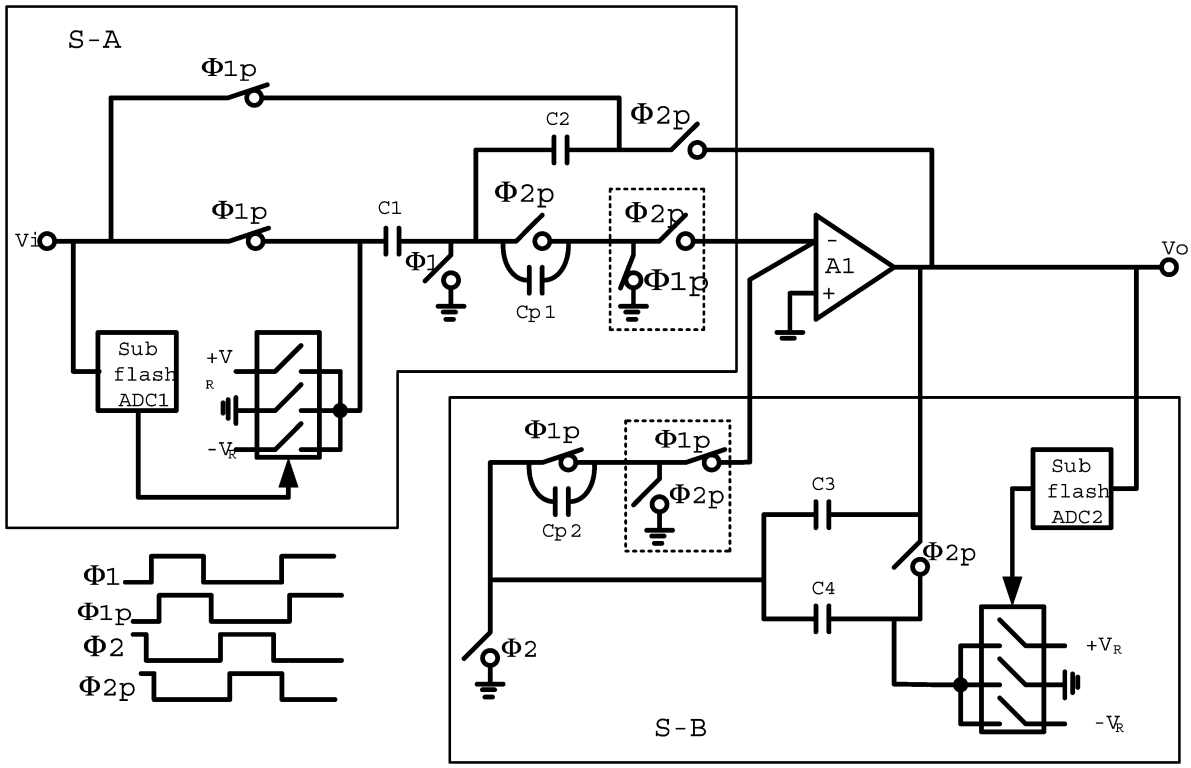

Fig. 5. Opamp-sharing architecture with the proposed additional switches.

opamp-sharing successive stages. Similarly, when $\Phi 2p$ is high, the right side of the parasitic capacitor Cp2 is tied to ground by the corresponding added switches. The added switches are controlled by $\Phi 2p$ and $\Phi 1p$, which are already employed in the circuit even before adding the additional switches, so no additional clock phases are needed. The added switches introduce series resistances, which can be reduced by using large switches at the expense of a potential increase in offsets due to charge feedthrough [7]. In the simulated ADC performance, there is about 1–2 dB signal-to-noise-and-distortion ratio (SNDR) improvement based on the introduced switches.

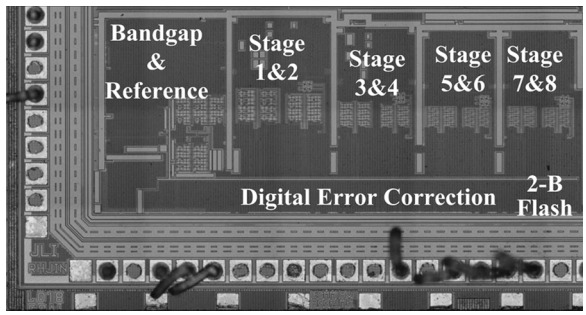

Fig. 6. Die photograph.

IV. Implementation and Measured Results

Gain-boosting telescopic opamps [21] are used in all opamp-sharing blocks to get a high open-loop gain and excellent bandwidth with low power consumption. By careful biasing [25], the gain-boosting telescopic opamp achieves 1.2-Vpp differential signal swing from 1.8-V power supply considering process, temperature and power supply variations. The comparators in all subflash ADCs (including the first stage) employ a high-speed mismatch-insensitive dynamic latch-type schematic [17] without any preamplifier.

The value of the sample and hold capacitor is scaled down in several of the pipeline stages to reduce power dissipation. The value of the sampling capacitance in the first stage is 1.2 pF, which is selected according to matching constraints based on technology data. For the next five stages in the pipelined ADC, the capacitance is 0.7, 0.5, 0.35, 0.25, and 0.175 pF, respectively. The rest of the stages in the pipeline use a sampling and holding capacitance of 0.175 pF.

The prototype ADC was fabricated in a 0.18-μm single-poly six-metal CMOS process with MiM capacitor. The die photograph is shown in Fig. 6, from which the detailed circuits can not be seen clearly due to the added dummy metals by the fabrication factory to pass the DRC (design rule check). So the layout of the ADC is provided in Fig. 7 to show more detail. The total active area is about 0.7 mm^2. The measured power consumption is 21.6 mW at 1.8-V power supply and 30 MS/s. The measured differential and integral nonlinearities (DNL and INL) with a 300-kHz 0-dB full-scale sine wave input are illustrated in Fig. 8. The DNL is within ± 0.57 LSB, the INL is within ± 0.8 LSB at 30 MS/s.

The measured output fast Fourier transform (FFT) spectrum with a 29.5-MHz sinusoidal input at 1.8-V power supply and 30 MS/s is plotted in Fig. 9. The measured SNR is 57.57 dB, the spurious free dynamic range (SFDR) is 65.96 dB, the THD is 65.41 dB, the SNDR is 56.91 dB, and the effective number of bits (ENOB) is 9.16. The measured dynamic performance

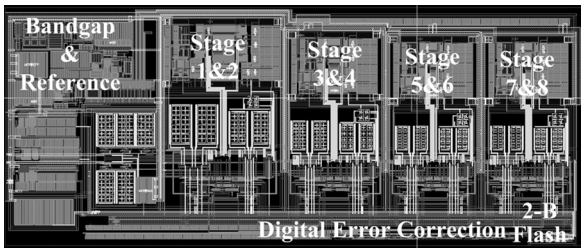

Fig. 7. Layout of the ADC.

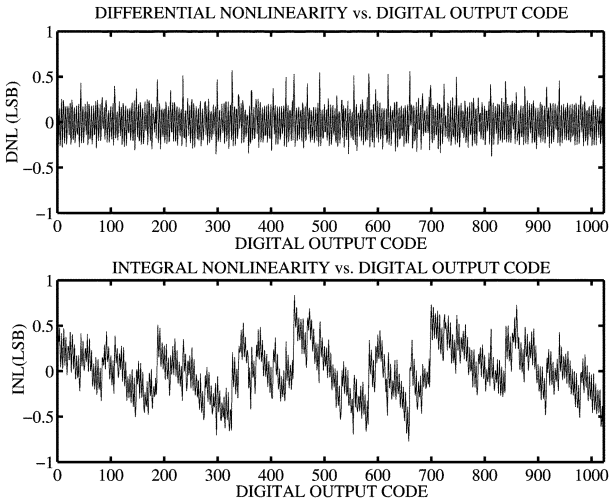

Fig. 8. Measured DNL and INL.

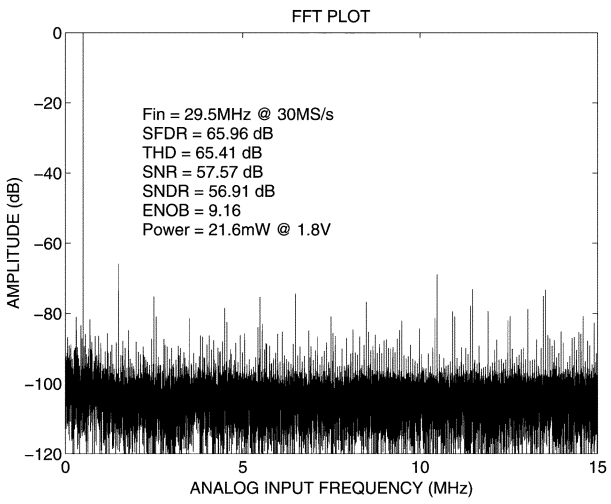

Fig. 9. Measured FFT spectrum.

versus input frequency at 1.8-V power supply and 30 MS/s is shown in Figs. 10 and 11. It exhibits higher than 9.1 ENOB for input frequencies up to twice the Nyquist rate (30 MHz) and 8.75 ENOB for a 70-MHz input. The measured ENOB versus the power supply voltage VDD with a 10.7-MHz sinusoidal input at 30 MS/s is shown in Fig. 12. The large power supply voltage range, over which the ADC works well, is due to the

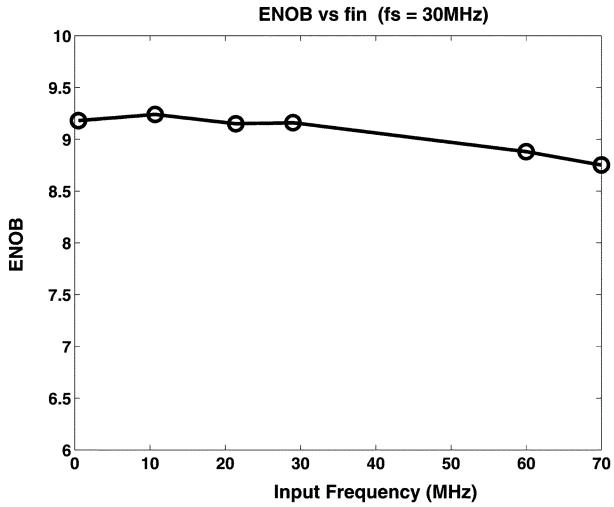

Fig. 10. Measured ENOB versus input frequency.

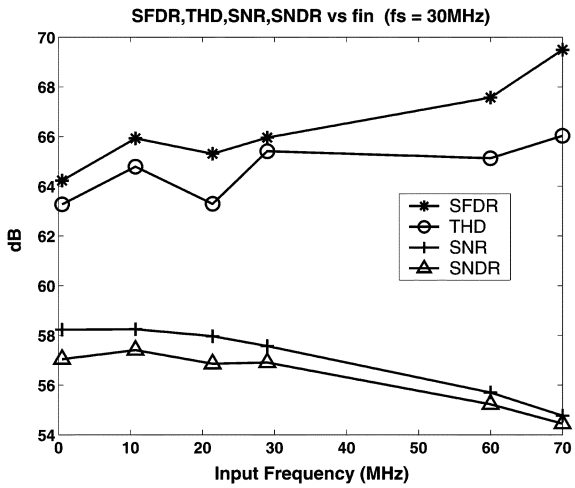

Fig. 11. Measured dynamic performance versus input frequency.

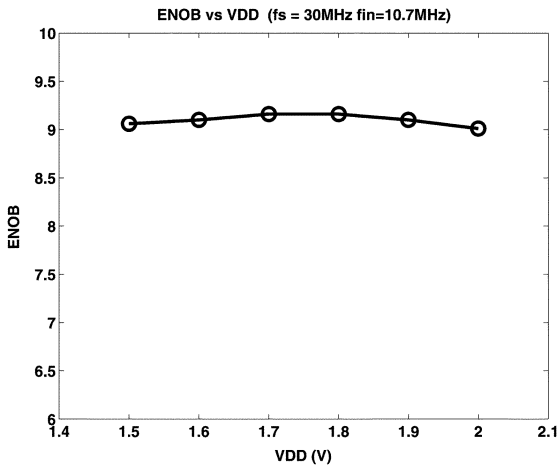

Fig. 12. Measured ENOB versus power supply voltage VDD.

stable biasing circuit and the overdesign. The measured performance of the prototype ADC is summarized in Table II.

TABLE III
FOM COMPARISONS

	Process	Sampling Rate (MS/s)	Resolution (bit)	Area (mm^2)	Power Consumption (mW)	FOM (pJ/step)
Mehr [15]	0.35-µm CMOS	40	10	2.6	55	0.38
Wang [27]	90-nm CMOS	12	10	0.3	3.3	0.8
Gupta [28]	0.13-µm CMOS	1000	11	3.5	250	0.5
Honda [29]	90-nm CMOS	100	10	4.0	33	0.34
This work	0.18-µm CMOS	30	10	0.7	21.6	0.26

TABLE II
SUMMARY OF EXPERIMENTAL RESULTS

Resolution	10 bit
Conversion rate	30 MHz
Technology	0.18-µm single-poly six-metal CMOS process with MiM capacitor
Power supply	1.8 V
Total power	21.6 mW@1.8 V
Area	0.7 mm^2
ENOB (fin=10.7 MHz)	9.24 bit
(fin=29.5 MHz)	9.16 bit
(fin=70.0 MHz)	8.75 bit
SNDR (fin=10.7 MHz)	57.41 dB
(fin=29.5 MHz)	56.91 dB
(fin=70.0 MHz)	54.45 dB
SNR (fin=10.7 MHz)	58.25 dB
(fin=29.5 MHz)	57.57 dB
(fin=70.0 MHz)	54.77 dB
SFDR (fin=10.7 MHz)	65.93 dB
(fin=29.5 MHz)	65.96 dB
(fin=70.0 MHz)	69.49 dB
THD (fin=10.7 MHz)	64.79 dB
(fin=29.5 MHz)	65.41 dB
(fin=70.0 MHz)	66.03 dB
Peak INL	0.8 LSB
Peak DNL	0.57 LSB

The figure-of-merit (FOM) of this ADC is 0.26 pJ/step. The FOM used in the calculation is [26]

$$\text{FOM} = \frac{P}{2^{\text{ENOB}} \times 2 \times \text{ERBW}} \tag{9}$$

where P is the power consumption of the ADC, the ERBW is the effective resolution bandwidth. As a reference, Table III shows the comparison of this work and some ADCs [15], [27]–[29] with similar resolutions. This design shows the best FOM in this category.

V. CONCLUSION

This paper describes a 1.8-V 10-bit 30-MS/s CMOS ADC, which can provide high dynamic performance for input signals much above Nyquist rate with low power dissipation. Low power consumption is obtained by employing the amplifier sharing architecture and by using the proposed SHA-less architecture, where the matching requirement along with the potential problems in the traditional SHA-less architecture is eliminated. High performance with relatively high-frequency input signal is achieved by employing a symmetrical bootstrapping switch as the bottom-sampling switch and by adding additional switches to reduce the crosstalk between the two opamp-sharing successive stages. The FOM of this ADC is 0.26 pJ/step, which makes the ADC among the most efficient ADCs.

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REFERENCES

[1] O. A. Adeniran, A. Demosthenous, C. Clifton, S. Atungsiri, and R. Soin, "A CMOS low-power ADC for DVB-T and DVB-H systems," in *Proc. IEEE ISCAS*, May 2004, vol. 1, pp. 209–212.
[2] D. Miyazaki, S. Kawahito, and M. Furuta, "A 10-b 30-MS/s low-power pipelined CMOS AD converter using a pseudodifferential architecture," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 369–373, Feb. 2003.
[3] J. Arias, V. Boccuzzi, L. Quintanilla, L. Enríquez, D. Bisbal, M. Banu, and J. Barbolla, "Low-power pipeline ADC for wireless LANs," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1338–1340, Aug. 2004.
[4] S. Limotyrakis, S. D. Kulchycki, D. K. Su, and B. A. Wooley, "A 150-MS/s 8-b 71-mW CMOS time-interleaved ADC," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1057–1067, May 2005.
[5] S. Jamal, D. Fu, N. Chang, P. Hurst, and S. Lewis, "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, Dec. 2002.
[6] S. C. Lee, K. D. Kim, J. K. Kwon, J. Kim, and S. H. Lee, "A 10-bit 400-MS/s 160-mW 0.13-mm CMOS dual-channel pipeline ADC without channel mismatch calibration," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1596–1605, Jul. 2006.
[7] K. Nagaraj, H. Fetterman, J. Anidjar, S. Lewis, and R. Renninger, "A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 312–320, Mar. 1997.
[8] P. C. Yu and H. S. Lee, "2.5-V, 12-b, 5-Msamples/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1854–1861, Dec. 1996.
[9] S. H. Lewis, "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no. 8, pp. 516–523, Aug. 1992.
[10] D. Nairn, "A 10-b 3 V 100 MS/s pipelined ADC," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 2000, pp. 257–260.
[11] W. Yang, D. Kelly, L. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1931–1936, Dec. 2001.
[12] Y. Chiu, P. R. Gray, and B. Nikolić, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2139–2151, Dec. 2004.
[13] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr, R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, Mar. 1992.
[14] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
[15] I. Mehr and L. Singer, "A 55-mW 10-bit 40-Msample/s Nyquist-rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 318–325, Mar. 2000.

[16] A. M. A. Ali, C. Dillon, R. Sneed, A. S. Morgan, S. Bardsley, J. Kornblum, and L. Wu, "A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1846–1855, Aug. 2006.
[17] L. Sumanen, M. Waltari, and K. Halonen, "A mismatch insensitive CMOS dynamic comparator for pipeline A/D converters," in *Proc. IEEE Int. Conf. Electronics, Circuits and Systems (ICECS)*, Dec. 2000, vol. 1, pp. 32–35.
[18] J. Li, X. Zeng, L. Xie, J. Chen, J. Zhang, and Y. Guo, "A 1.8-V 22-mW 10-bit 30-MS/s subsampling pipelined CMOS ADC," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2006, pp. 513–516.
[19] A. M. Abo, "Design for reliability of low-voltage, switched-capacitor circuits," Ph.D. dissertation, Univ. Calif., Berkeley, 1999.
[20] K. Gulati, M. S. Peng, A. Pulincherry, C. E. Muñoz, M. Lugin, A. R. Bugeja, J. Li, and A. P. Chandrakasan, "A highly integrated CMOS analog baseband transceiver with 180 MSPS 13-bit pipelined CMOS ADC and dual 12-bit DACs," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1856–1866, Aug. 2006.
[21] K. Bult and G. Geelen, "A fast-settling CMOS opamp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 4, pp. 1379–1384, Dec. 1990.
[22] M. Dessouky and A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits," *Electron. Lett.*, vol. 35, no. 1, pp. 8–10, Jan. 1999.
[23] M. Waltari, "Circuit techniques for low-voltage and high-speed A/D converters," Ph.D. dissertation, Helsinki Univ. Technol., Helsinki, Finland, 2002.
[24] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Delta\Sigma$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.
[25] J. Li, J. Zhang, B. Shen, X. Zeng, Y. Guo, and T. Tang, "A 10BIT 30 MSPS CMOS A/D converter for high performance video applications," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2005, pp. 523–526.
[26] A. Varzaghani and C.-K. Yang, "A 600-MS/s 5-bit pipeline A/D converter using digital reference calibration," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 310–319, Feb. 2006.
[27] R. Wang, K. Martin, D. Johns, and G. Burra, "A 3.3 mW 12 MS/s 10b pipelined ADC in 90 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 278–279.
[28] S. K. Gupta, M. A. Inerfield, and J. Wang, "A 1-GS/s 11-bit ADC with 55-dB SNDR, 250-mW power realized by a high bandwidth scalable time-interleaved architecture," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2650–2657, Dec. 2006.
[29] K. Honda, M. Furuta, and S. Kawahito, "A low-power low-voltage 10-bit 100-MSample/s pipeline A/D converter using capacitance coupling techniques," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 757–765, Apr. 2007.

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