A Capacitor-Free CMOS Low-Dropout Regulator With Damping-Factor-Control Frequency Compensation

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***Abstract*—A 1.5-V 100-mA capacitor-free CMOS low-dropout regulator (LDO) for system-on-chip applications to reduce board space and external pins is presented. By utilizing damping-factor-control frequency compensation on the advanced LDO structure, the proposed LDO provides high stability, as well as fast line and load transient responses, even in capacitor-free operation. The proposed LDO has been implemented in a commercial 0.6-μm CMOS technology, and the active chip area is 568 μm $\times$ 541 μm. The total error of the output voltage due to line and load variations is less than $\pm$0.25%, and the temperature coefficient is 38 ppm/°C. Moreover, the output voltage can recover within 2 μs for full load-current changes. The power-supply rejection ratio at 1 MHz is $-$30 dB, and the output noise spectral densities at 100 Hz and 100 kHz are 1.8 and 0.38 μV/$\sqrt{\text{Hz}}$, respectively.**

***Index Terms*—Damping-factor-control frequency compensation, loop-gain stability, capacitor-free low-dropout regulator (LDO), CMOS voltage reference.**

I. Introduction

POWER MANAGEMENT is necessary to reduce the standby power of portable applications such as cellular phones and PDAs. The low-dropout linear regulator (LDO) [1]–[4] is one of the most popular power converters widely used in power management. It is especially suitable for applications that require low-noise and precision supply voltages with few off-chip components. With the rapid development of system-on-chip designs, there is a growing trend toward power-management integration. On-chip and local LDOs are utilized to power up subblocks of a system individually [5], and this can significantly reduce crosstalk, improve the voltage regulation, and eliminate load-transient voltage spikes from the bondwire inductances. In addition, system-on-chip designs with on-chip and local LDOs can reduce both board space and external pins significantly.

Due to the emerging need of high-performance low-voltage LDOs for low-voltage mixed-signal systems, many researchers have recently proposed many advanced methods to improve the performance of LDOs. Rincon-Mora *et al.* proposed current-efficient voltage buffer [1], forward-biased power transistor [1], pole-zero doublet for load-regulation enhancement [2], and capacitance multiplication [3]. Heisley *et al.* proposed using a DMOS power transistor [4]. Chevalerias *et al.* proposed using an nMOS power transistor with charge-pumped gate drive [6]. The main aims of all the proposed methods are: 1) to enable low-voltage regulation; 2) to reduce slew-rate limit at the gate drive; and 3) to improve load regulation and transient response. However, the precision of output voltage and transient response are tradeoffs with LDO stability [2], [7]. The above reveals the fact that there are limitations on the structure and frequency compensation scheme of classical LDOs, especially for the low-voltage LDO designs. Moreover, the off-chip capacitor, which is the key for stability and high LDO performance, cannot be eliminated. This off-chip capacitor is the main obstacle to fully integrating LDOs in system-on-chip designs.

As a result, [redacted] Solving the correlated tradeoffs on stability, precision, and recovery speed is the main challenge of capacitor-free LDO design. In this paper, a CMOS LDO that is targeted for CMOS system-on-chip designs is presented [8]. The circuit architecture is [redacted], and it provides a capacitor-free feature to eliminate the need of bulky off-chip capacitor. Both fast load transient response and high power-supply rejection ratio (PSRR) are achieved due to the fast and stable loop gain provided by the proposed LDO structure and damping-factor-control (DFC) compensation scheme [9], [10]. The power pMOS transistor in the proposed LDO operates in linear region at dropout, and hence, the required transistor size can be reduced significantly for the ease of integration and cost reduction. In addition, a novel CMOS voltage reference based on weighted difference of gate–source voltages [11] enables full-CMOS implementation.

In this paper, a brief review on [redacted] will be given in Section II, and then the proposed LDO structure with DFC compensation will be introduced in Section III, where the stability conditions and circuit design considerations are explained in detail. Finally, the measurement results on some important specifications of the proposed LDO such as line and load transient responses, as well as PSRR, will be presented in Section IV.

II. Review of Classical LDO

The structure of a classical CMOS LDO, as shown in Fig. 1, is composed of an error amplifier, a voltage buffer, a power

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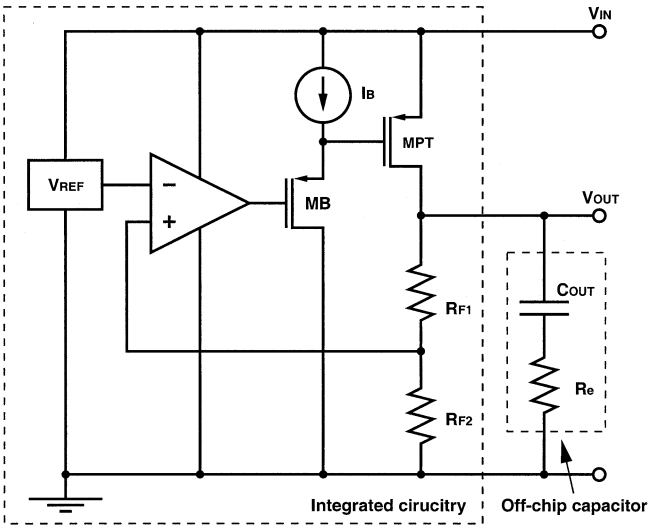


Fig. 1. Structure of classical LDO.

pMOS transistor operating in saturation region, a feedback-resistor network, and a voltage reference. The structure is intrinsically unstable because it has three low-frequency poles, which are generated at the outputs of LDO, the voltage buffer, and the error amplifier, respectively. Dominant-pole compensation with pole-zero cancellation scheme, which is achieved by the off-chip capacitor and its equivalent series resistance (ESR), is utilized for LDO stability [1]–[4], [7]. In addition, the design of high-output-swing voltage buffer is critical to low-voltage LDO design. Often, the voltage buffer is a source follower, which cannot provide a high output swing to fully turn on (for pMOS-implemented source follower) or off (for nMOS-implemented source follower) the power transistor in low-voltage supply efficiently. Approaches using depletion MOS transistor [4] and bipolar junction transistor (BJT) [1] cannot be realized in standard CMOS technologies.

The stability of classical LDOs based on dominant-pole compensation with pole-zero cancellation can be studied in Fig. 2. The second pole p_2 is cancelled by the zero z_1 created by the ESR of the output capacitor. With a large output capacitance, the LDO stability is achieved by locating p_3 beyond the unity-gain frequency of the loop gain to provide sufficient phase margin. However, when loop gain is too high, p_3 locates before the unity-gain frequency, and an even larger output capacitance is required to retain LDO stability.

Moreover, the power pMOS transistor in classical LDO must operate in saturation region due to the stability problem at different input voltages. The change in voltage gain due to different drain–source voltage is not substantial when the transistor operates in saturation region [12]–[14]. However, if the transistor operates in linear region at dropout, the transistor will operate in saturation region instead as the input voltage increases. As mentioned previously, when the loop gain increases, the classical LDO based on dominant-pole compensation may be unstable. Therefore, the power pMOS transistor needs to operate in saturation region throughout the entire range of input voltage, so a large transistor size is required to provide a small saturation voltage at the maximum output current.

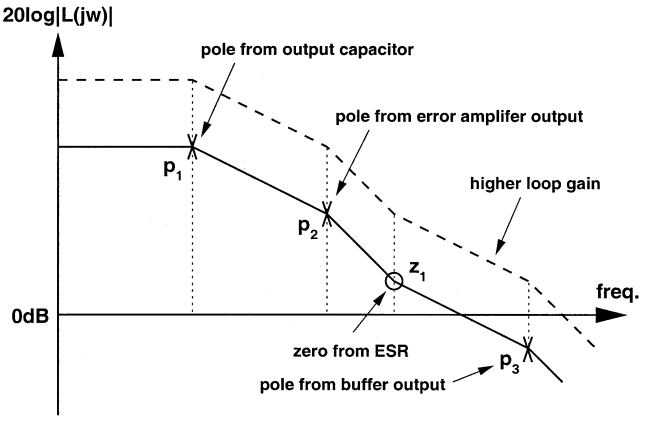


Fig. 2. Loop gain of classical LDO (magnitude plot only and not in scale).

[redacted]: 1) static-state specification; 2) dynamic-state specification; and 3) high-frequency specification. Line and load regulations, as well as temperature coefficient, are regarded as static-state specifications, while line and load transient responses, as well as ripple rejection ratio, are dynamic-state specifications. The high-frequency specifications are PSRR and output noise. All specifications are correlated, and they have tradeoffs with the LDO stability when dominant-pole compensation with pole-zero cancellation is used.

Line and load regulations are two important specifications that relate to the output-voltage accuracy. The dependences of line and load regulations are, respectively, given by [1], [2]

$$\text{Line Regulation} = \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \approx \frac{g_{mp} r_{op}}{L_o} + \frac{1}{\beta} \cdot \left(\frac{\Delta V_{\text{REF}}}{\Delta V_{\text{IN}}} \right) \tag{1}$$

$$\text{Load Regulation} = \frac{\Delta V_{\text{OUT}}}{\Delta I_{\text{OUT}}} = -\frac{r_{op}}{1 + L_o} \tag{2}$$

where L_o is low-frequency loop gain, $\beta = R_{F2}/(R_{F1} + R_{F2})$, and g_{mp} and r_{op} are the transconductance and output resistance of the power pMOS transistor, respectively. From the above equations, a high loop gain is required for a high-precision LDO output voltage, but the LDO stability is sacrificed when loop gain is too high. Thus, there is always tradeoff between precision and stability.

Load transient response is critical when there is a sudden change in load current, and a good load transient response results in minimal overshoot, as well as undershoot, and fast recovery time. In fact, the response time of an LDO, which depends on the slew rate at the gate drive of the power transistor and the loop-gain bandwidth, can be improved by a high slew-rate voltage buffer and advanced frequency compensation technique. Yet, more static power consumption is required, and dominant-pole compensation cannot effectively provide a wide loop-gain bandwidth.

PSRR depends highly on both loop-gain bandwidth and ESR. An LDO with a good PSRR and line transient response results in a good ripple rejection ratio, which is vital for an LDO as a post-regulator of switching-mode power converter.

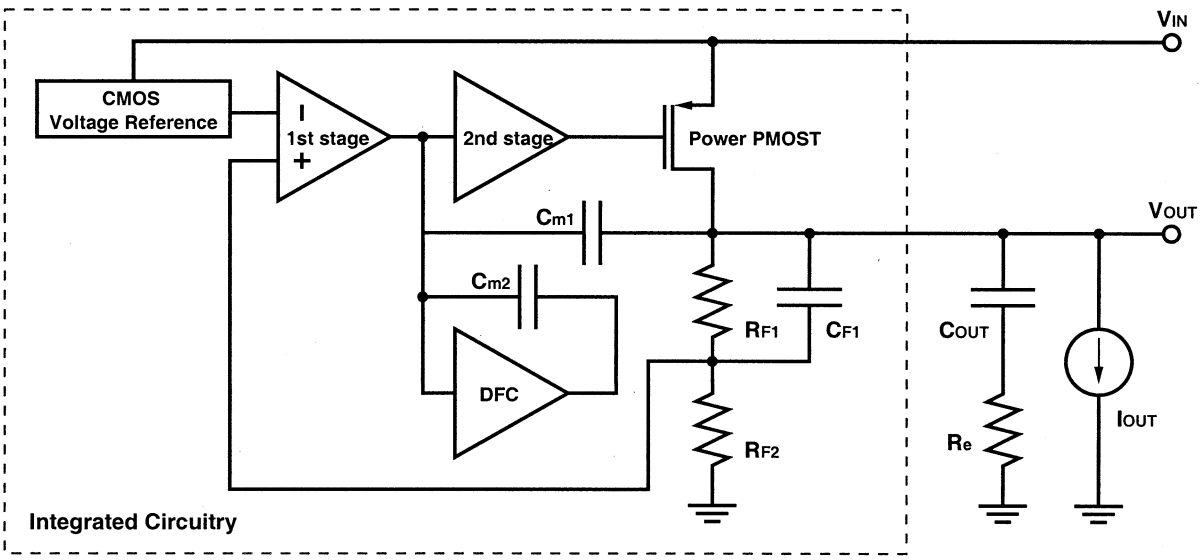


Fig. 3. Structure of the proposed LDO with capacitor-free feature.

From the above discussions on classical LDO using dominant-pole compensation, a high loop gain and a wide loop bandwidth are critical for the improvement of LDO performance, but static power consumption and stability are tradeoffs. It is further illustrated that classical LDOs cannot be applied effectively to system-on-chip designs due to the required large output capacitor for stability. Therefore, an advanced LDO structure with advanced frequency compensation, which solves the tradeoff problems of classical LDOs, is presented in next section.

III. Advanced LDO Structure With Damping-Factor-Control Compensation

From the previous discussion, the classical LDO suffers from a stability problem. This problem is due to the low-frequency poles, and hence, large off-chip capacitance and ESR are needed for closed-loop stability. In fact, this problem can be solved by pole splitting. However, classical two-stage-amplifier topology is not optimum since the power transistor cannot function as a high-gain stage in dropout condition. The pole-splitting effect is thus not effective and the output precision is also degraded. Instead, an LDO can be viewed as a three-stage amplifier with the power transistor as the last stage. When using this approach, as will be discussed later, the positions of the nondominant poles depend on the transconductance of the power transistor and the output capacitance. The larger transconductance and smaller output capacitance results in higher frequencies of the nondominant poles. Therefore, the worst case stability occurs at zero load-current condition as the transconductance is minimum (about 5–10 mA/V, typically) when only a current equaled to $V_{\rm OUT}/(R_{F1}+R_{F2}) \approx 1$–$5$ μA drains from the power transistor. Advanced frequency compensation techniques are required to generate a more effective pole-splitting effect incorporated with pole-zero cancellation. The pushed nondominant poles can be cancelled more effectively by extra zeros at higher frequencies. The required passive components to generate the zeros can be much smaller, and the coupling noise is, hence, reduced significantly. A stable and fast-response LDO can, therefore, be achieved. In this section, the novel LDO with DFC frequency compensation based on this novel idea is discussed.

The structure of the proposed LDO with DFC frequency compensation and a first-order high-pass feedback network is shown in Fig. 3. It is composed of a high-gain error amplifier, a high-gain high-output-swing second stage, a power pMOS transistor operating in linear region at dropout, a feedback resistive network with first-order high-pass characteristic, a CMOS voltage reference, and a DFC block with compensation capacitors C_{m1} and C_{m2}. The corresponding schematic diagram is illustrated in Fig. 4, and the utilized circuit structure is a cascade architecture, which is suitable for low-voltage operation.

The resulting structure can be viewed as a three-stage amplifier driving a large capacitive load, where the capacitive load is due to the power line in capacitor-free condition or due to the off-chip capacitor. This structure can be stabilized using DFC frequency compensation [9], [10], which is a pole-splitting compensation especially designed for compensating amplifier with large-capacitive load. The DFC block is composed of a negative gain stage with a compensation capacitor C_{m2}, and the DFC block is connected at output of the first stage. Another compensation capacitor C_{m1} is required to achieve pole-splitting effect. The feedback-resistive network creates a medium-frequency zero for improving the LDO stability. The analysis of this feedback network can be studied using Fig. 5, and the transfer function is given by

$$\frac{v_x(s)}{v_s(s)} = \left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right)\left[\frac{1+sC_{F1}R_{F1}}{1+sC_{F1}(R_{F1}//R_{F2})}\right]. \quad (3)$$

From the above analysis, it is shown that one pole (p_f) and one zero (z_f) are created, and p_f and z_f are, respectively, given by

$$p_f = \frac{1}{C_{F1}(R_{F1}//R_{F2})} \quad (4)$$

$$z_f = \frac{1}{C_{F1}R_{F1}}. \quad (5)$$

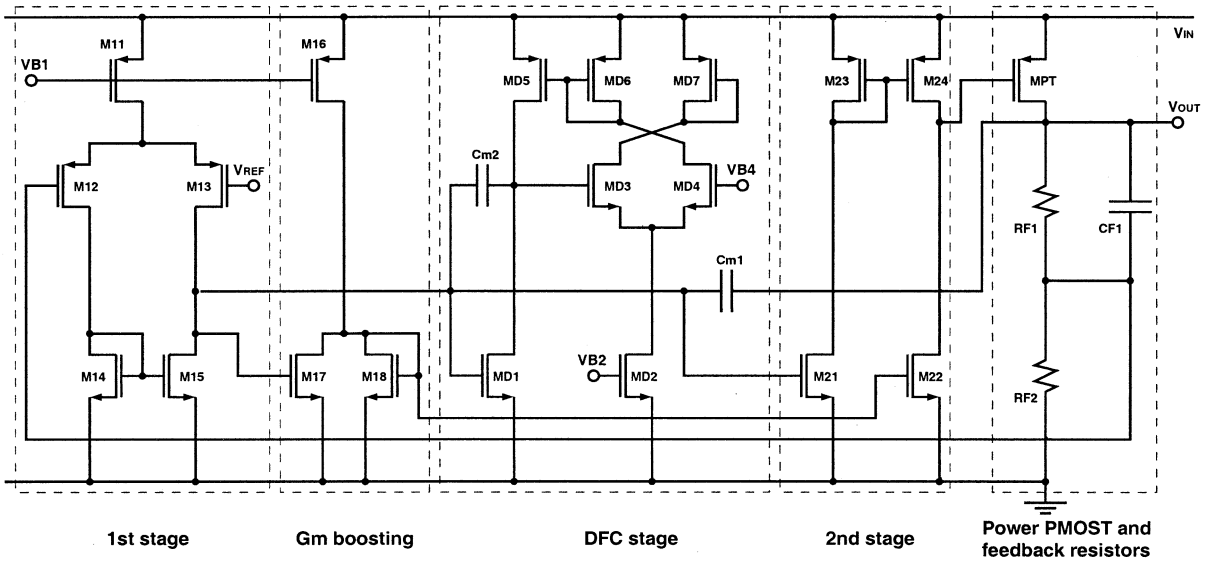


Fig. 4. Complete schematic of the proposed LDO.

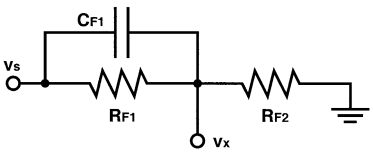


Fig. 5. Feedback-resistive network with first-order high-pass characteristic.

The zero frequency is lower than the pole frequency, and this zero, as will be discussed later, can be used to cancel the effect of nondominant poles created in the proposed LDO. In order to have $z_f \ll p_f$, R_{F2} should be much smaller than R_{F1}. This implies that the required reference voltage should be much smaller than LDO output voltage.

Due to the effective pole-splitting effect by DFC compensation, the nondominant-pole frequencies are high, and so the required C_{F1} is small and is about 5 pF in the current design. This capacitance can be easily integrated in CMOS technologies. In addition, the transient response will not be slowed down by C_{F1} because it is small and is connected at the LDO output.

Due to the advanced LDO structure and compensation scheme, the proposed LDO is stable in the full range of load current when an off-chip capacitor is connected at the LDO output. Better yet, it is also stable without a load capacitor from full load to a finite small output current. For different modes of operation, the proposed LDO has different loop-gain transfer functions, and the details of stability are discussed in the following.

A. Stability With Off-Chip Capacitor

The stability of the proposed LDO is studied for two cases: $I_{\rm OUT} = 0$ and $I_{\rm OUT} \neq 0$. When $I_{\rm OUT} = 0$, the transconductance g_{mp} and the output resistance r_{op} of the power pMOS is at the minimum and maximum, respectively. This is the worst case stability of the proposed compensation scheme. In this situation, the DFC scheme provides a transfer function, which is given by

$$L_{o(\rm cap)}(s)\,|_{I_{\rm OUT}=0} = \frac{L_o\left(1+\frac{s}{z_e}\right)\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left[1+s\left(C_{\rm OUT}R_e+\frac{C_gC_{\rm OUT}g_{m4}}{C_{m1}g_{m2}g_{mp}}\right)+s^2\frac{C_gC_{\rm OUT}}{g_{m2}g_{mp}}\right]\left(1+\frac{s}{p_f}\right)} \quad (6)$$

where C_g is the gate capacitance of the power pMOS transconductance and g_{m4} is the transconductance of the DFC stage. Moreover

$$L_o = ((R_{F2})/(R_{F1}+R_{F2}))g_{m1}R_{o1}g_{m2}R_{o2}g_{mp}r_{op}$$
$$p_1 = 1/C_{m1}R_{o1}g_{m2}R_{o2}g_{mp}r_{op}$$

and

$$z_e = 1/C_{\rm OUT}R_e$$

are the low-frequency loop gain of the proposed DFC scheme, the dominant pole, and the ESR zero, respectively, and $g_{m1}, g_{m2}, R_{o1}, R_{o2}$, and R_e are the transconductance of the error amplifier, the transconductance of the second gain stage, the output resistance of the error amplifier, the output resistance of the second gain stage, and the ESR of the output capacitance, respectively.

When $I_{\rm OUT} = 0$, the current drain from the power transistor is $V_{\rm OUT}/(R_{F1}+R_{F2})$, which is less than 1–5 μA for low-power LDO designs. Therefore, g_{mp} is very small, and this causes the effect of $C_{\rm OUT}R_e$ in the s term at the denominator of (6) to be negligible. As a result, (6) is approximated to

$$L_{o(\rm cap)}(s)\,|_{I_{\rm OUT}=0} \approx \frac{L_o\left(1+\frac{s}{z_e}\right)\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+s\frac{C_gC_{\rm OUT}g_{m4}}{C_{m1}g_{m2}g_{mp}}+s^2\frac{C_gC_{\rm OUT}}{g_{m2}g_{mp}}\right)\left(1+\frac{s}{p_f}\right)}. \quad (7)$$

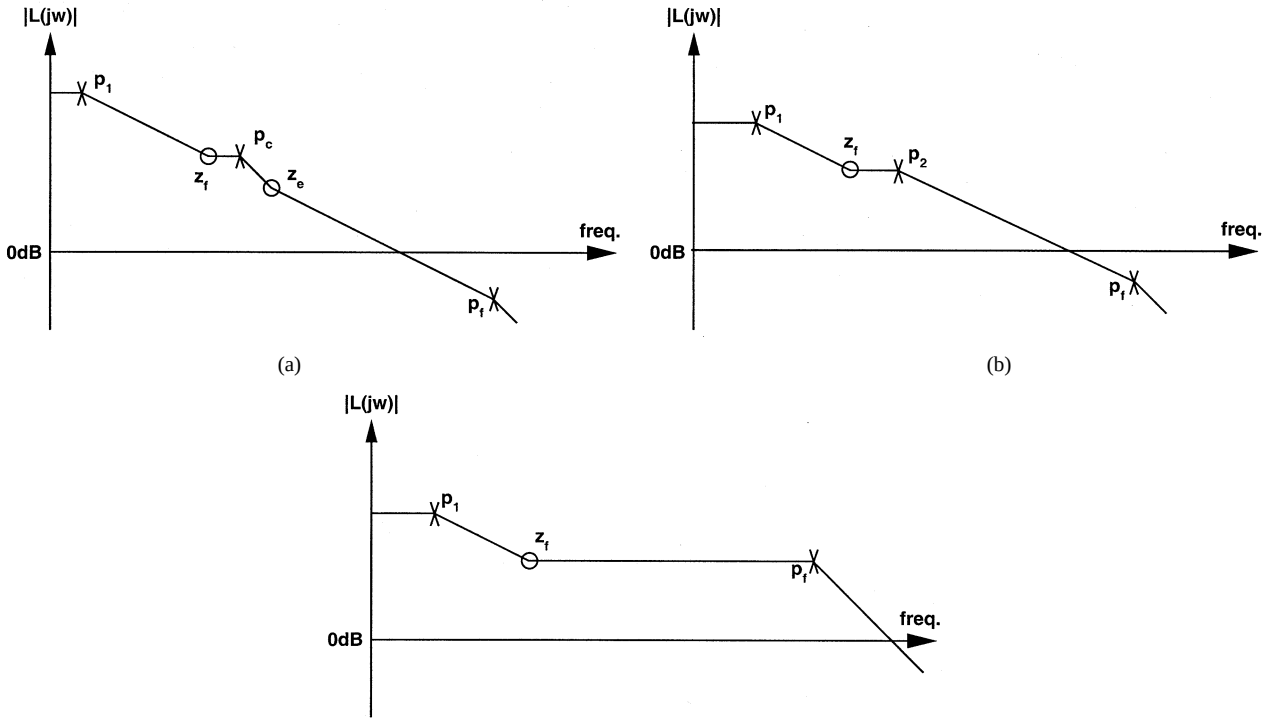


Fig. 6. Loop gain (magnitude plot only and not in scale) of the proposed LDO structure. (a) $C_{\rm OUT} \neq 0$ and $I_{\rm OUT} = 0$. (b) $C_{\rm OUT} \neq 0$ and $I_{\rm OUT} \neq 0$. (c) $C_{\rm OUT} = 0$ and $I_{\rm OUT} \neq 0$.

We compare the second-order function in (7) with a standard second-order function given by

$$F(s) = 1 + s\left(\frac{2\zeta}{p_c}\right) + \left(\frac{s}{p_c}\right)^2 \tag{8}$$

where ζ is the damping factor and p_c is the pole frequency of the complex poles. The value of p_c is given by

$$p_c = \sqrt{\frac{g_{m2}g_{mp}}{C_g C_{\rm OUT}}}. \tag{9}$$

Now, the damping factor is given by

$$\zeta = \frac{1}{2}\sqrt{\frac{C_g C_{\rm OUT}}{g_{m2}g_{mp}}} \times \left(\frac{g_{m4}}{C_{m1}}\right). \tag{10}$$

The damping factor is critical to the LDO stability. If the damping factor is too small, a frequency peak occurs and pole-zero cancellation by separated zeros is not effective. If the damping factor is too large, the complex poles become two separated real poles and the loop-gain bandwidth will be degraded. Therefore, the damping factor is set to $1/\sqrt{2}$ as a compromise under the conditions that

$$C_{m1} = g_{m1}\sqrt{\frac{8C_g C_{\rm OUT}}{g_{m2}g_{mp}}} \tag{11}$$

and

$$g_{m4} = 4g_{m1}. \tag{12}$$

It is noted that $C_{m2} = C_{m1}$ is set for proper operation of the DFC scheme [9], [10].

As shown in Fig. 6(a), the effect of the complex poles can be cancelled by z_e and z_f. Since the complex poles are split to a high frequency (several kilohertz) by the DFC scheme, z_e and z_f are at high frequencies. This implies that a low ESR, which is the key to a better load transient response and PSRR, is required. Moreover, p_f is designed to be higher than the unity-gain frequency of the loop gain for a good phase margin.

When there is a little increase of load current, as shown in (9), the complex poles will shift to a little higher frequency due to the increase of g_{mp}. The LDO is still stable since the pole-zero cancellation is still effective for pole-zero separation of less than a half of a decade.

When the load current increases significantly, g_{mp} also increases significantly and the second-order function at the denominator of (6) is altered. The transfer function in the case of $I_{\rm OUT} \neq 0$ is given by

$$L_{o({\rm cap})}(s)|_{I_{\rm OUT}\neq 0} = \frac{L_o\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+s\frac{C_g}{g_{m2}g_{mp}R_e}\right)\left(1+\frac{s}{p_f}\right)}. \tag{13}$$

In this case, the ESR zero has no effect since an ESR pole is created simultaneously. The LDO is reduced to a one-zero three-pole system, where the new pole $p_2 = (g_{m2}g_{mp}R_e)/(C_g)$ is created. As shown in Fig. 6(b), z_f can be used to cancel p_2 to make the system stable. As a remark, the low-frequency loop gain decreases and p_1 shifts to a higher frequency since $g_{mp}r_{op}$ is inversely proportional to $\sqrt{I_{\rm OUT}}$.

B. Stability Without Off-Chip Capacitor

When the proposed LDO is used in system-on-chip designs without an off-chip capacitor, the LDO is also stable. There is a minimum load current (about 100 μA to 10 mA depending

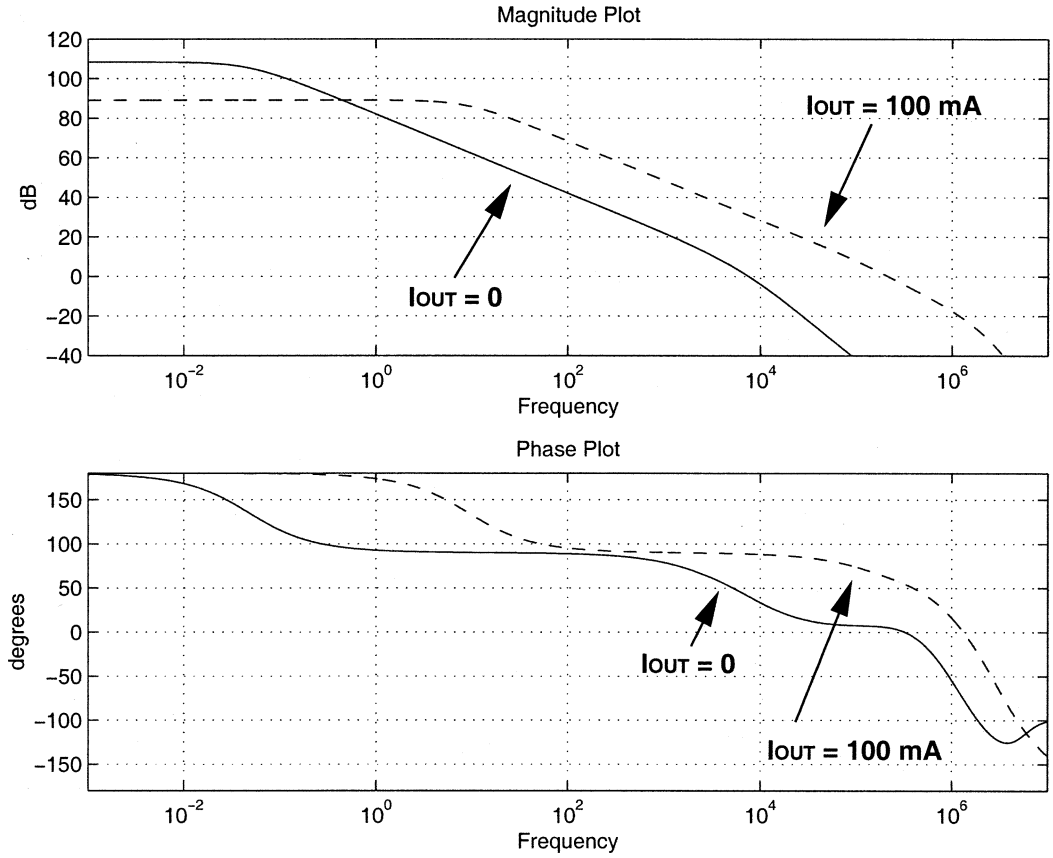


Fig. 7. Simulated loop gain of the proposed LDO with an output capacitor.

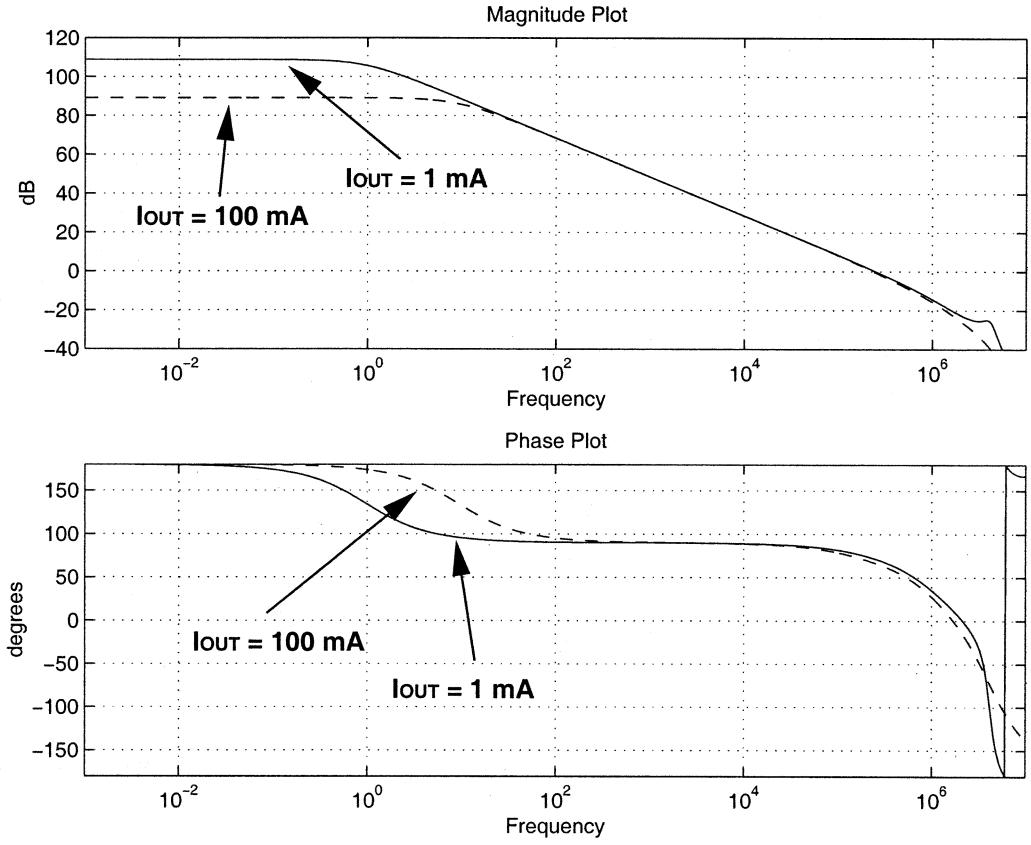


Fig. 8. Simulated loop gain of the proposed LDO without an output capacitor.

on design) such that the LDO is still stable. The output capacitance comes from the power line, and the required minimum load current is larger for a larger load capacitance. Under such circumstance without the off-chip capacitor, ESR does not exist. Moreover, the second and third poles are pushed to frequencies that are higher than the unity-gain frequency of loop gain due to a large g_{mp}. The transfer function is given by

$$L_{o(\text{capfree})}(s) \approx \frac{L_o\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_f}\right)}. \tag{14}$$

As shown in Fig. 6(c), pole-zero cancellation is automatically achieved by z_f and p_f, and thus, the theoretical phase margin is 90°. However, parasitic poles and zeros will degrade the phase margin.

The simulated loop gain with and without an off-chip capacitor are shown in Figs. 7 and 8, respectively. From the results, the proposed LDO is absolutely stable under any operational condition with an off-chip capacitor, and it is also stable with a minimum load current for capacitor-free condition.

From the above discussion on stability, the proposed LDO structure with the associated compensation scheme is completely different from the classical LDO. In classical LDO, the power loss in the power transistor does not provide any benefit to performance. However, in the proposed scheme, the power used in the power transistor can further improve the LDO stability and the loop-gain bandwidth. This, in turn, enhances the transient responses and PSRR, simultaneously.

The power transistor in the proposed LDO is much smaller since it operates in linear region at dropout. The smaller size results in a smaller gate capacitance. This helps to increase the frequencies of the nondominant poles and hence a better stability can be achieved. Moreover, the smaller gate capacitance improves the slew rate at gate drive and a faster transient response can be obtained.

The stability of the proposed LDO is not affected when the supply voltage increases from dropout. When the input voltage increases, the operation region of the power transistor change from linear to saturation region. The voltage gain $(g_{mp}r_{op})$ contributed by the power transistor increases and the whole loop gain increases. Since the first pole of the loop gain is given by $p_1 = 1/C_{m1}R_{o1}g_{m2}R_{o2}g_{mp}r_{op}$, the first pole p_1 will shift to a lower frequency automatically and the LDO stability can be maintained.

The PSRR is effectively improved due to the wide loop-gain bandwidth. When an off-chip capacitance is used, the required ESR is much smaller than that in classical LDO. This, as mentioned before, also enhances the PSRR at high frequencies.

C. Circuit Design

In the schematic shown in Fig. 4, the error amplifier and the high-gain second stage are formed by M11–M15 and M21–M24, respectively. MPT is the power pMOS transistor and MD1–MD7 form the DFC block with operation-point control [10]. There are in total three on-chip capacitors C_{m1}, C_{m2}, and C_{F1}, and the total value is less than 12 pF. This will not limit the slew rate at the error amplifier for low-power design of the proposed LDO.

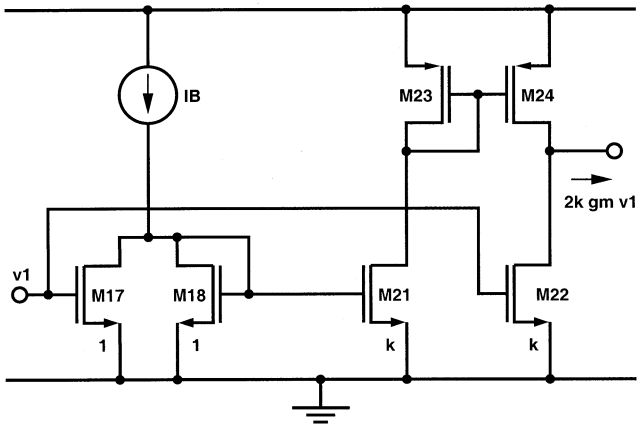


Fig. 9. Transconductance-boosting circuitry.

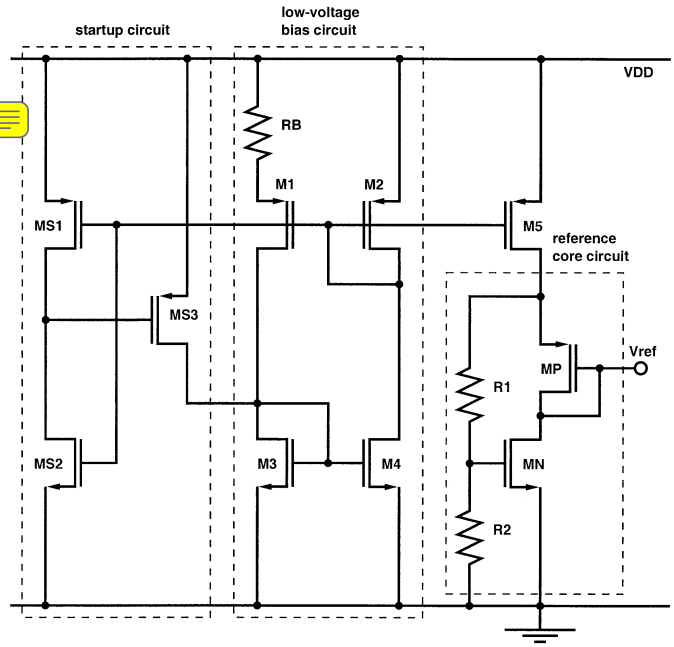


Fig. 10. CMOS voltage reference.

The error amplifier of the proposed LDO is a simple differential pair with active load. The offset voltage due to the error amplifier should be minimized since the temperature- and supply-dependent offset voltage introduces additional errors to the LDO output voltage.

From (9), the DFC compensation scheme can be more effective when the transconductance of the second stage is large. Thus, a simple circuitry to boost g_{m2} is utilized. The detail can be explained using Fig. 9. The function of M17 and M18 is to create a signal $-v_1$ from the input signal v_1, and these two signals v_1 and $-v_1$ are applied to M21 and M22, respectively. With k-times current mirror, the effective transconductance is increased by $2k$ times. The simple circuitry can enhance the DFC scheme to provide a wider loop-gain bandwidth. Since the bias current is increased by k times, a push-pull output stage, formed by M22 and M24, can charge and discharge the gate capacitance more effectively during the transient responses.

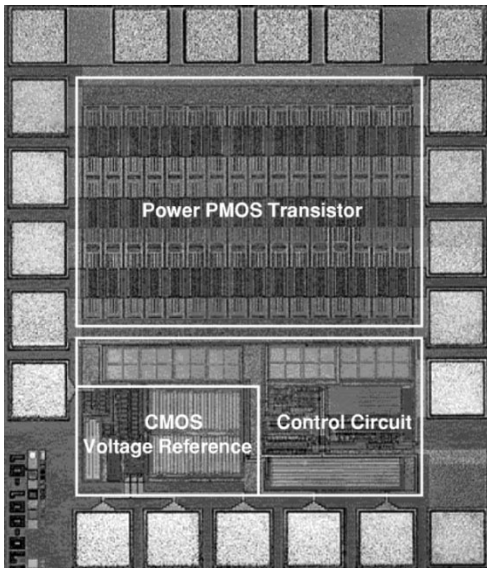


Fig. 11. Micrograph of the proposed CMOS LDO.

TABLE I
SUMMARY OF PERFORMANCE OF PROPOSED CMOS LDO

	Capacitor Free	With Capacitor
Technology	0.6-μm CMOS	
Threshold voltage	$V_{thn} \approx \lvert V_{thp}\rvert \approx 0.85V$	
Chip area	568 μm × 541 μm	
Supply voltage	1.5 to 4.5 V	
Supply current	38 μA	
Dropout voltage	200 mV@100 mA	
Preset Output voltage	1.3 V	
Temperature coefficient	38 ppm/°C	
Error due to line and load changes	±0.25%	
Settling time (worst case)	~2.0 μs	~1.6 μs
PSRR	-60 dB@10 Hz	-60 dB@10 Hz
(V_{IN} = 1.5 V, I_{OUT} = 100 mA)	-60 dB@1 kHz	-60 dB@1 kHz
	-30 dB@1 MHz	-38 dB@1 MHz
Output spectral noise density	1.8 μV/sqrt Hz@100 Hz	1.8 μV/sqrt Hz@100 Hz
(V_{IN} = 1.5 V, I_{OUT} = 100 mA)	0.38 μV/sqrt Hz@100 kHz	0.02 μV/sqrt Hz@100 kHz

Bandgap voltage references are generally used in LDO design. Although there exists many low-voltage high-accuracy bandgap references [15]–[18], accurate modeling of the parasitic BJT is required. In fact, a voltage reference can be implemented based on the principle of threshold voltage difference [19]–[22], but additional fabrication steps are required. To develop the whole LDO in CMOS technologies, the utilized voltage reference is a CMOS voltage reference based on the weighted difference of gate–source voltages [11]. The concept is based on the differences in temperature coefficients of threshold voltages of an nMOS and a pMOS transistor. The schematic of the CMOS voltage reference is shown in Fig. 10. The reference voltage is given by

$$V_{\mathrm{REF}} = \left(1 + \frac{R_1}{R_2}\right) V_{\mathrm{GS}\,n} - |V_{\mathrm{GS}\,p}|. \tag{15}$$

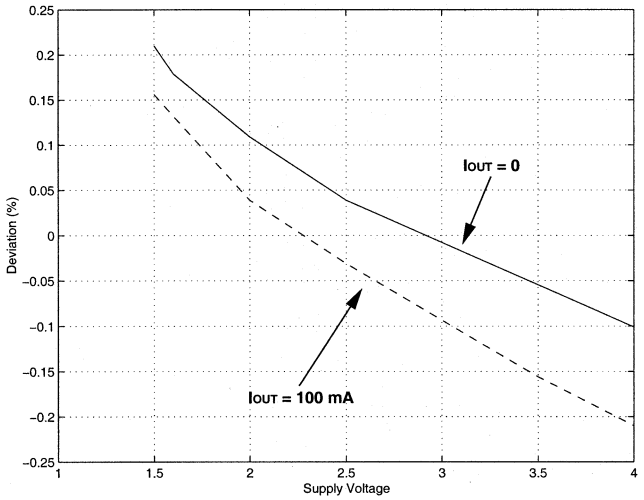


Fig. 12. Measured line and load regulations.

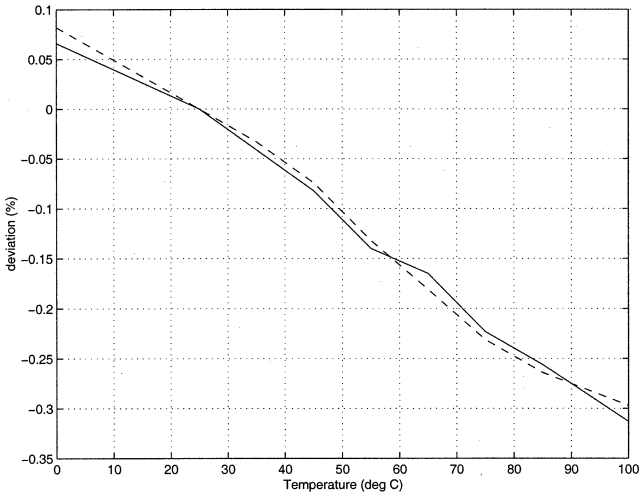


Fig. 13. Measured temperature dependence at $V_{\mathrm{IN}} = 1.5$ V (solid line: $I_{\mathrm{OUT}} = 100$ mA; dashed line: $I_{\mathrm{OUT}} = 0$).

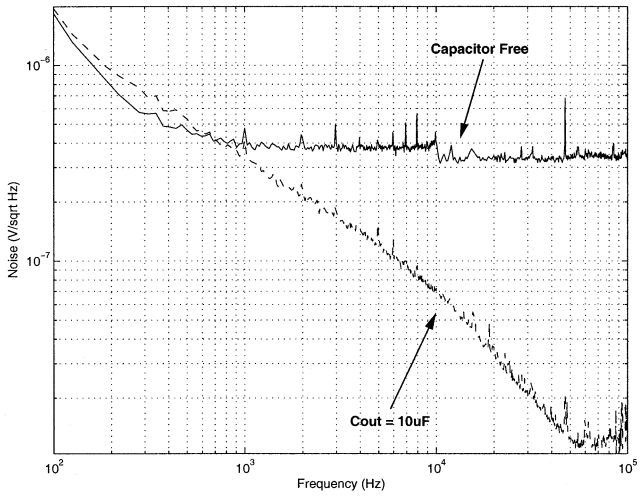


Fig. 14. Measured output spectral noise density at $V_{\mathrm{IN}} = 1.5$ V and $I_{\mathrm{OUT}} = 100$ mA.

A zero temperature coefficient of the reference voltage can be obtained by an appropriate resistance ratio of R_1/R_2 and tran-

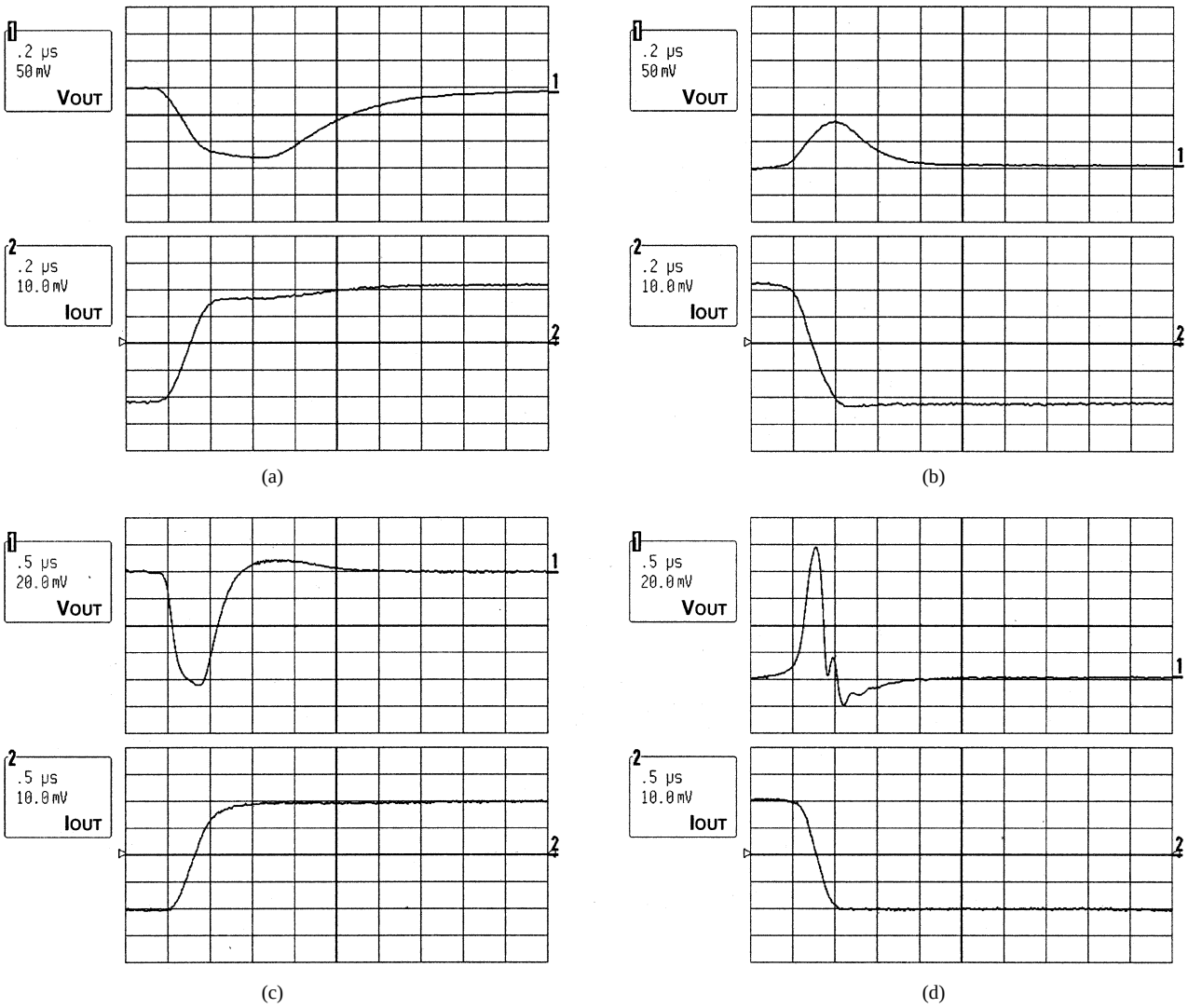


Fig. 15. Load transient responses at $V_{\rm IN} = 1.5$ V (a) 0 to 100 mA with $C_{\rm OUT} = 10\ \mu$F and ESR $= 1\Omega$ (b) 100 to 0 mA with $C_{\rm OUT} = 10\ \mu$F and ESR $= 1\Omega$ (c) 10 to 100 mA with $C_{\rm OUT} = 0$ (d) 100 to 10 mA with $C_{\rm OUT} = 0$.

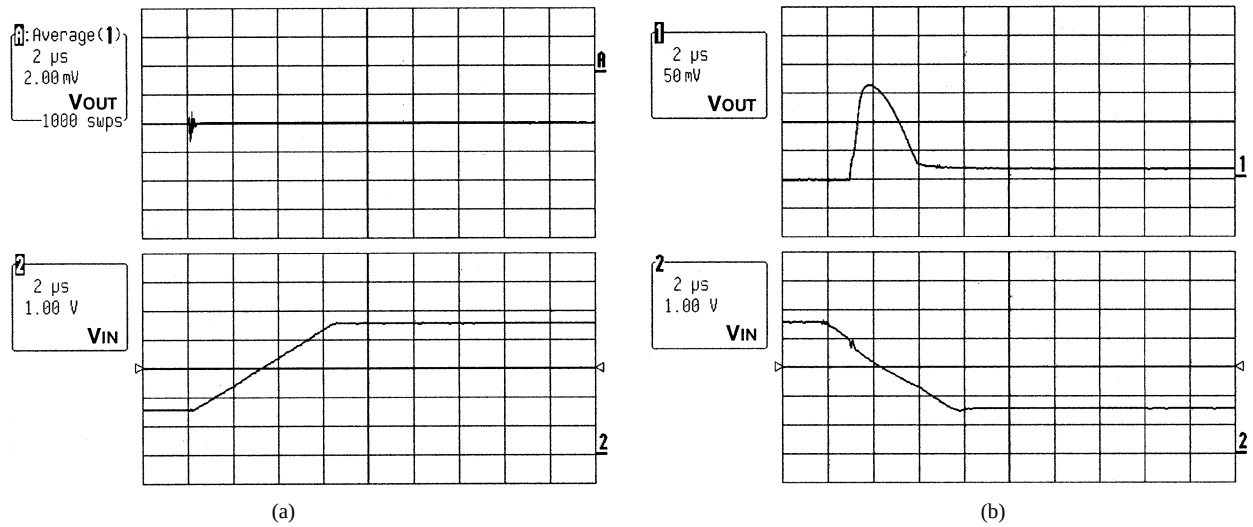
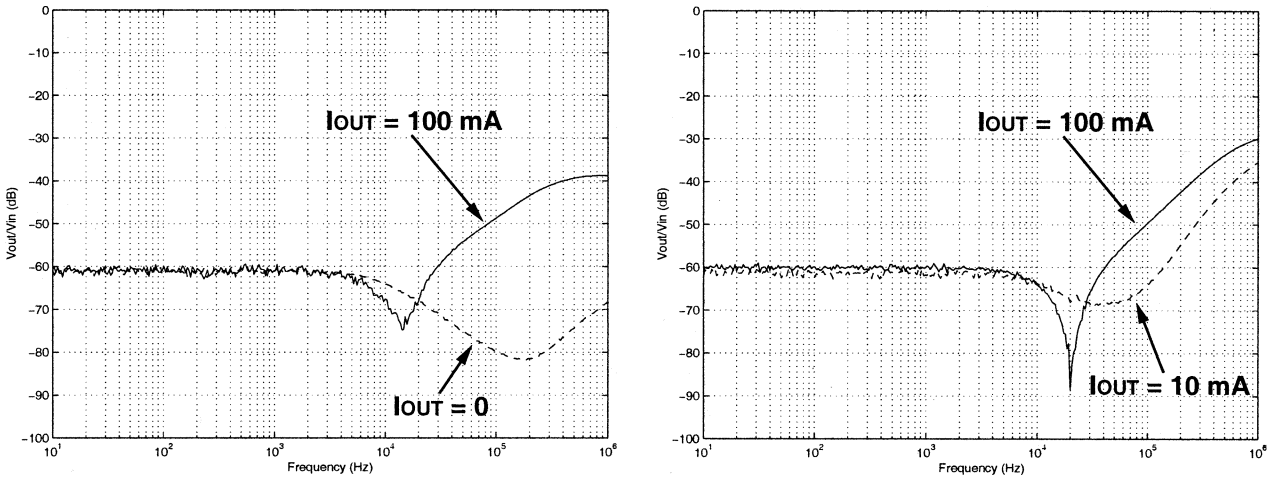


Fig. 16. Measured line transient response with $C_{\rm OUT} = 0$. (a) $V_{\rm IN} = 1.5$ to 4.5 V. (b) $V_{\rm IN} = 4.5$ to 1.5 V.

sistor-size ratio, based on the theoretical analysis in [11]. Both ratios are functions of device parameters and can be optimized on the circuit level.

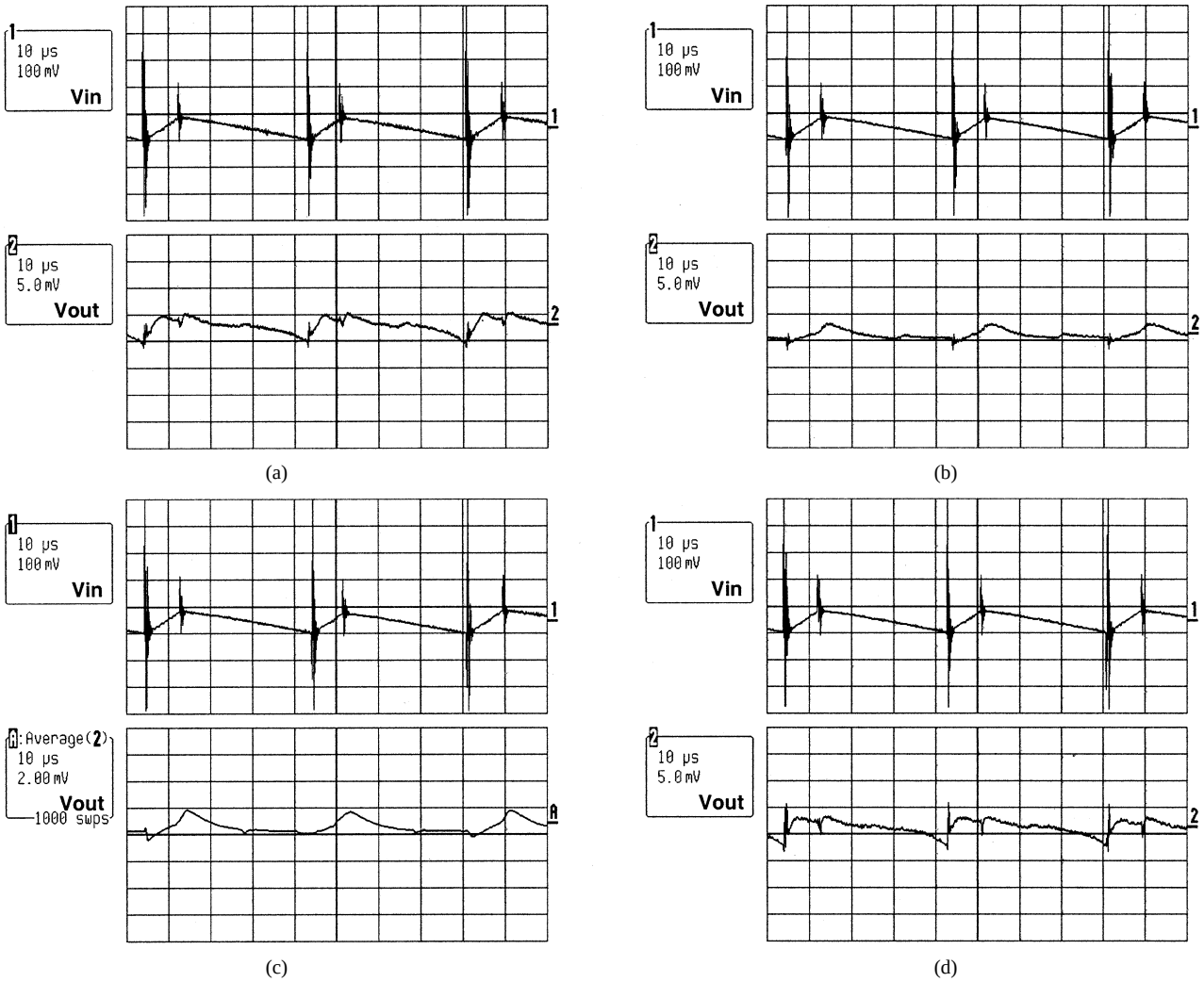
IV. Experimental Results

The proposed LDO shown in Fig. 4 has been implemented in AMS (Austria Mikro Systeme Group, Austria) 0.6-μm CMOS



(a) (b)

Fig. 17. Measured PSRR at $V_{\rm IN} = 1.5$ V. (a) $C_{\rm OUT} = 10\ \mu$F and ESR $= 1\Omega$. (b) $C_{\rm OUT} = 0$.



(a) (b) (c) (d)

Fig. 18. Measured ripple rejection. (a) $C_{\rm OUT} = 10\ \mu$F, ESR $= 1\ \Omega$, and $I_{\rm OUT} = 0$. (b) $C_{\rm OUT} = 10\ \mu$F, ESR $= 1\ \Omega$, and $I_{\rm OUT} = 100$ mA. (c) $C_{\rm OUT} = 0$ and $I_{\rm OUT} = 1$ mA. (d) $C_{\rm OUT} = 0$ and $I_{\rm OUT} = 100$ mA.

technology, which has threshold voltage of about 0.85 V. The micrograph of the LDO is shown in Fig. 11, and the chip area is 568 μm $\times$ 541 μm. The LDO is capable of operating down to 1.5 V and consumes only 38-μA ground current. The maximum output current is 100 mA with a dropout voltage of 200 mV. Table I summarizes the performance of the proposed LDO.

The measured line and load regulations are shown in Fig. 12. The total error of the output voltage due to line and load variations is just $\pm 0.25\%$. It is due to the high loop gain provided by the two high-gain stages. Moreover, as illustrated in Fig. 13, the measured temperature coefficient is 38 ppm/°C for both the minimum and maximum load current.

The measured output spectral noise density of the proposed LDO is shown in Fig. 14. There is no great difference at low frequencies for the proposed LDO with or without an off-chip capacitor, but the case with an off-chip capacitor shows a lower high-frequency noise. Therefore, the proposed LDO without an off-chip capacitor can be used for some digital and memory subblocks while an additional off-chip capacitor can be embedded to power up some noise-sensitive analog subblocks.

The measured load transient responses of the proposed LDO are measured under two conditions: with a 10-μF ESR$= 1\Omega$ off-chip capacitor and capacitor-free condition. The case with an off-chip capacitor is shown in Fig. 15(a) and (b) while the capacitor-free case is illustrated in Fig. 15(c) and (d). The load current changes between the minimum and the maximum for both cases. Experimental results show that the proposed LDO can respond quickly within 0.5 μs and can recover to the preset output voltage within 2 μs. This is due to the fast loop-gain response provided by the DFC compensation and the fast slew rate at the gate of the power pMOS transistor. Moreover, the fast response time is beneficial for reducing the overshoot and undershoot, and a less than 150-mV deviation is recorded for the worst case scenario.

The measured line transient responses in the capacitor-free condition are shown in Fig. 16. The supply voltage changes between 1.5 and 4.5 V in 6 μs. The LDO responds immediately and recovers the output voltage.

In addition, the proposed LDO provides good performance on PSRR at high frequencies. As shown in Fig. 17(a) and (b), the LDO has at least -30 dB rejection ability at 1 MHz when functioning with or without an off-chip capacitor. This good performance is important for the LDO as a post-regulator of high-efficiency switching-mode power converters. Fig. 18 shows the proposed LDO with and without an off-chip capacitor as a post-regulator of a buck converter. The input voltage ripple is as large as 100 mV, and the LDO can suppress the voltage ripple to about 7 mV.

V. Conclusion

A CMOS LDO, which has the capacitor-free feature, based on the architecture of a three-stage amplifier and DFC frequency compensation, has been presented. The advanced structure, theoretical analysis on the stability, and the experimental results have been provided. The performance of the proposed LDO is proven to be much better than the counterparts based on dominant-pole compensation with pole-zero cancellation.

The proposed LDO structure is beneficial for system-on-chip designs since it helps to eliminate many off-chip capacitors while preserving high static-state, frequency, and transient performances. The simple structure and small chip area are additional advantages for on-chip local voltage regulators of integrated systems.

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