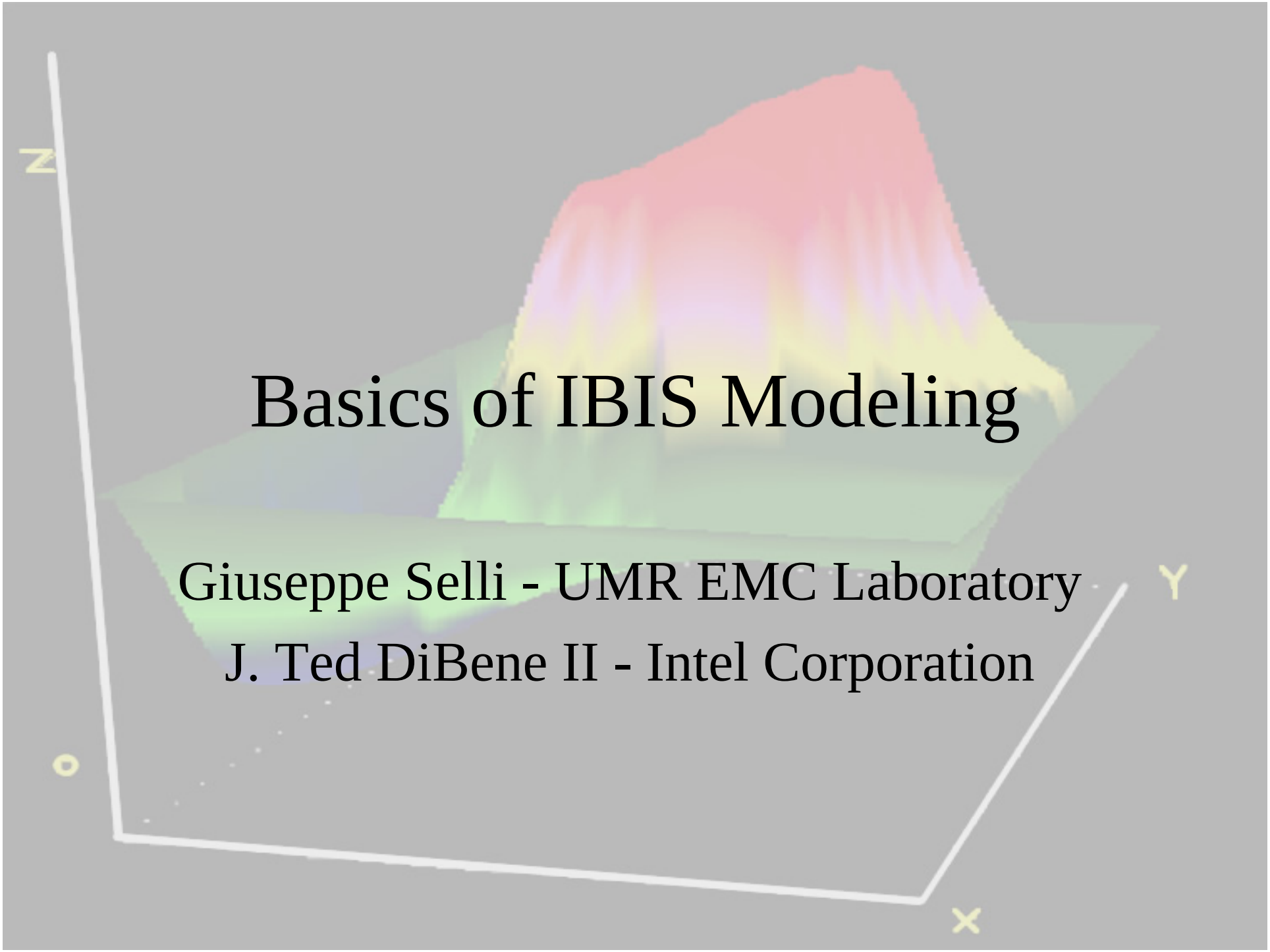
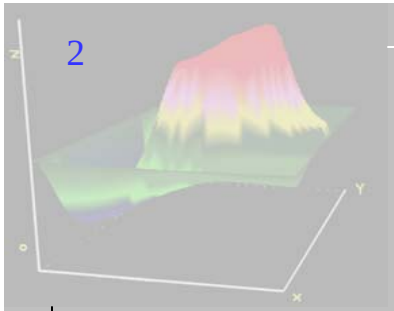


Basics of IBIS Modeling

Giuseppe Selli - UMR EMC Laboratory

J. Ted DiBene II - Intel Corporation



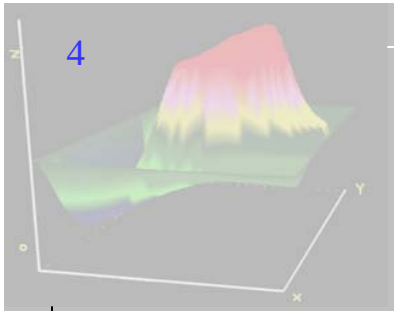
Outline

- SPICE *vs.* IBIS
- Why IBIS ?
- IBIS Output/Input Models
- Simple Circuit Example

What is SPICE and IBIS?

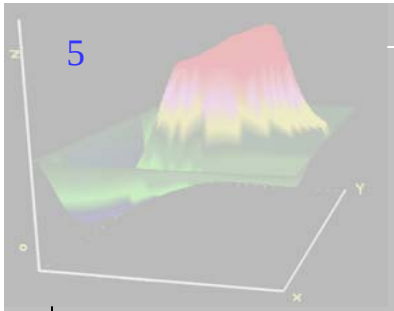
SPICE (***S***imulation ***P***rogram with ***I***ntegrated ***C***ircuit ***E***mphasis) is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses.

IBIS (***I***nput/Output ***B***uffer ***I***nformation ***S***pecification) is a standard for describing the analog behavior of the buffers of digital devices using plain ASCII text formatted data.



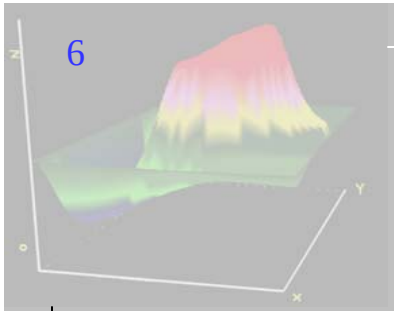
SPICE *vs.* IBIS

- SPICE allows analysis of complex circuit elements for signal integrity – very versatile
  - Usually very accurate
  - Very common
  - Portable: virtually every platform



SPICE *vs.* **IBIS**

- IBIS handles large numbers of I/O circuit cells for understanding complex interaction of signal timing and interaction.
  - Usually computationally fast
  - Circuit models typically fairly simple: behavioral
  - Good for complex digital signal circuit analysis



When IBIS? -- When SPICE?

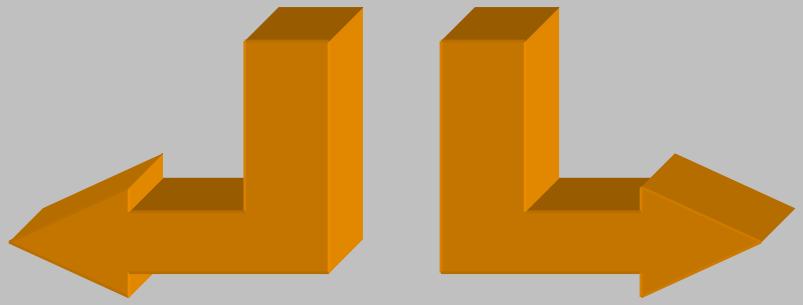
Fetures	IBIS	SPICE
Computational Efficiency	Good	From good to poor
Model Complexity	Usually fairly simple	Complex, but it depends
Accuracy	From good to poor	Typically good
Applications	Signal Integrity	Signal and power integrity
Programs	Small number	Large number
I/O Circuit Cells	Very large	Limited

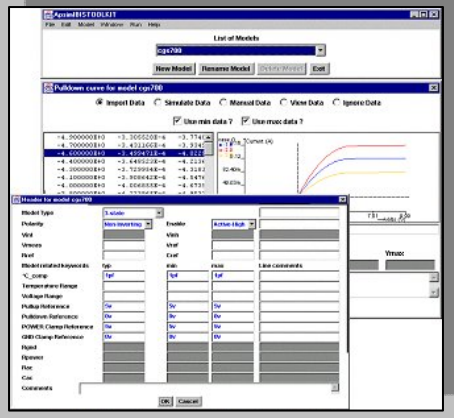
Why IBIS ?

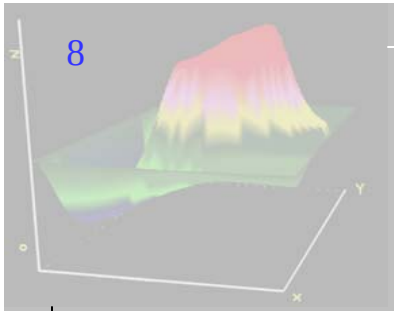
- PCB and device level Signal Integrity
  - SI issues gaining more attention in past decade pushing IC vendors and users to understand complex device and PCB level signal interactions in shorter and shorter timeframes.

✓ Keep proprietary information residing in the IC recipes

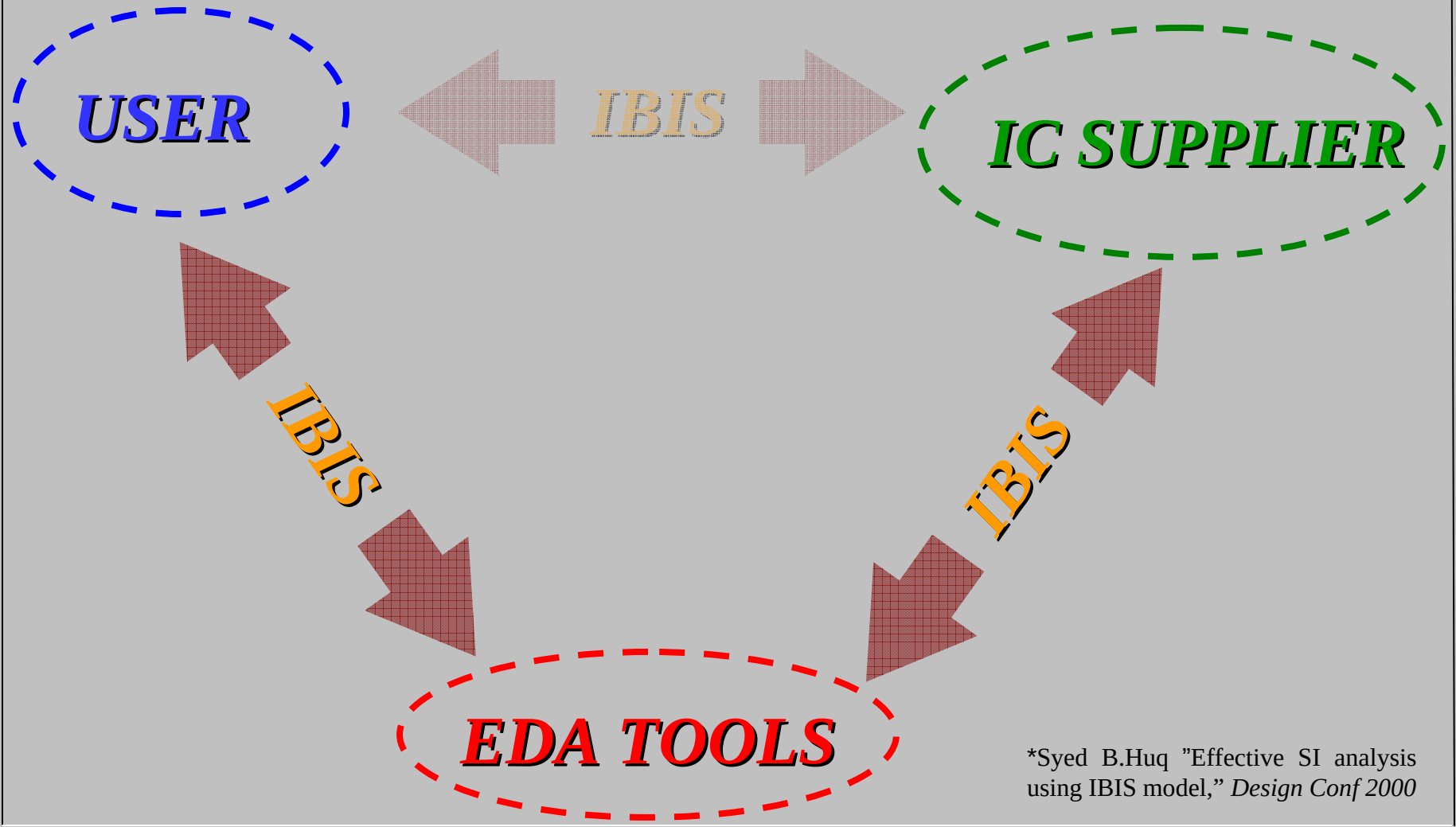
✓ Common tool for users



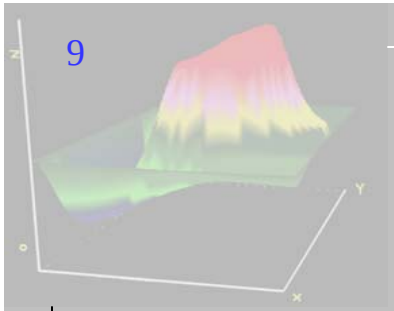




Golden Triangle*

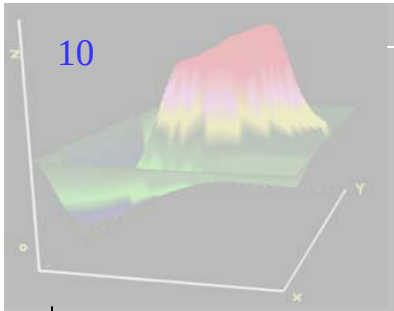


*Syed B.Huq "Effective SI analysis using IBIS model," *Design Conf 2000*



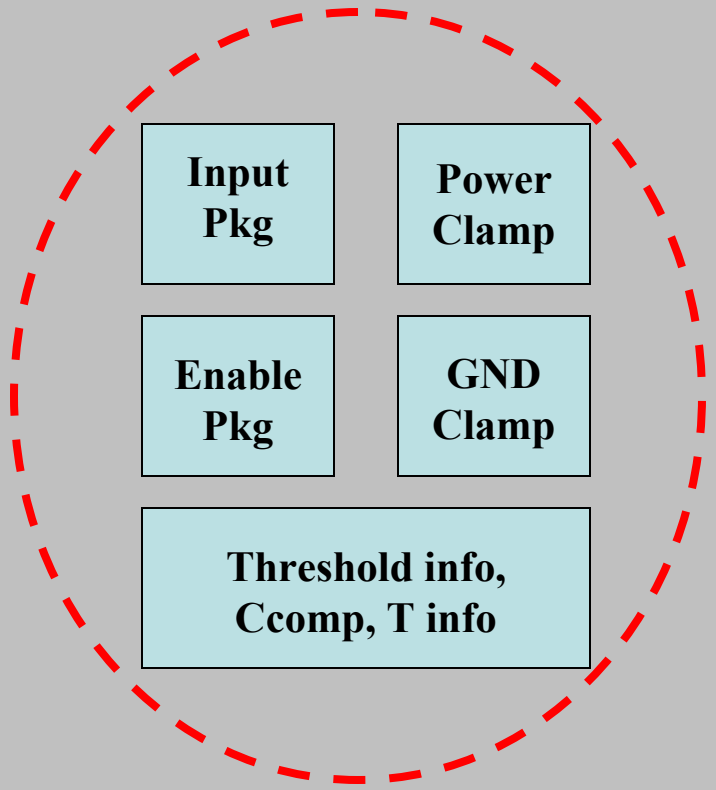
Why IBIS ?

- SPICE not suitable for large circuit
- Modeling circuit without getting proprietary information
- The first IBIS specifications were written in 1993 and Intel played a major role
- Many EDA tool vendors and companies participate to the IBIS Open Forum today

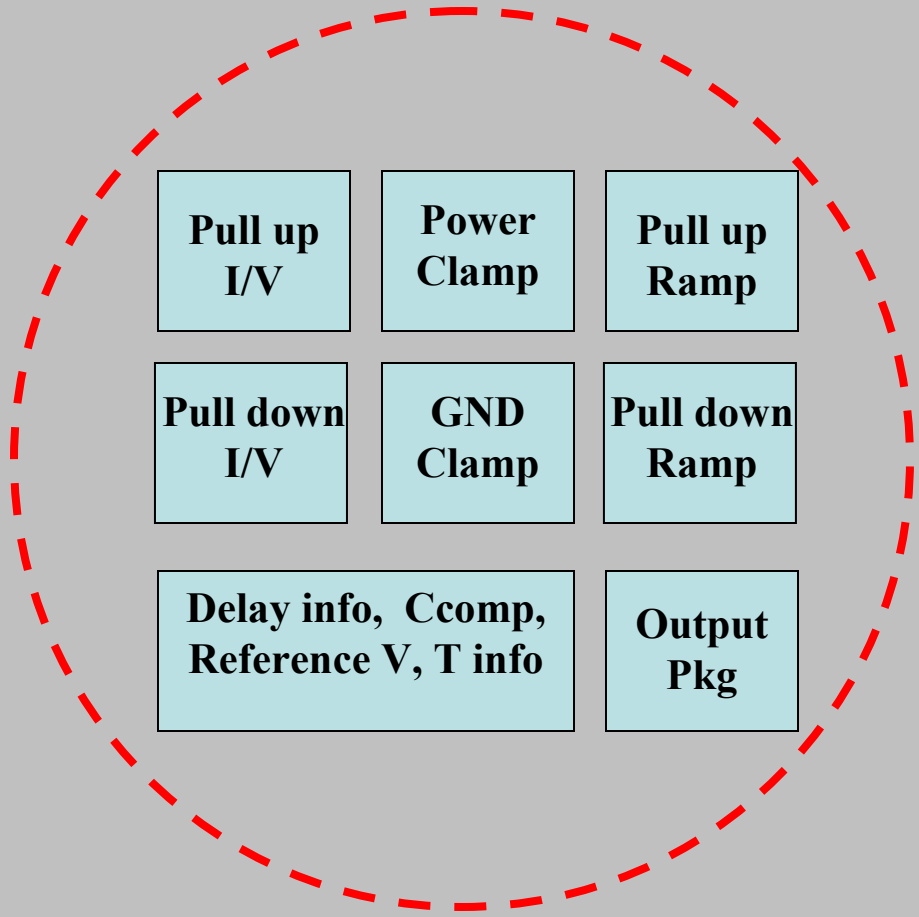


Blocks for Simple I/O Buffer

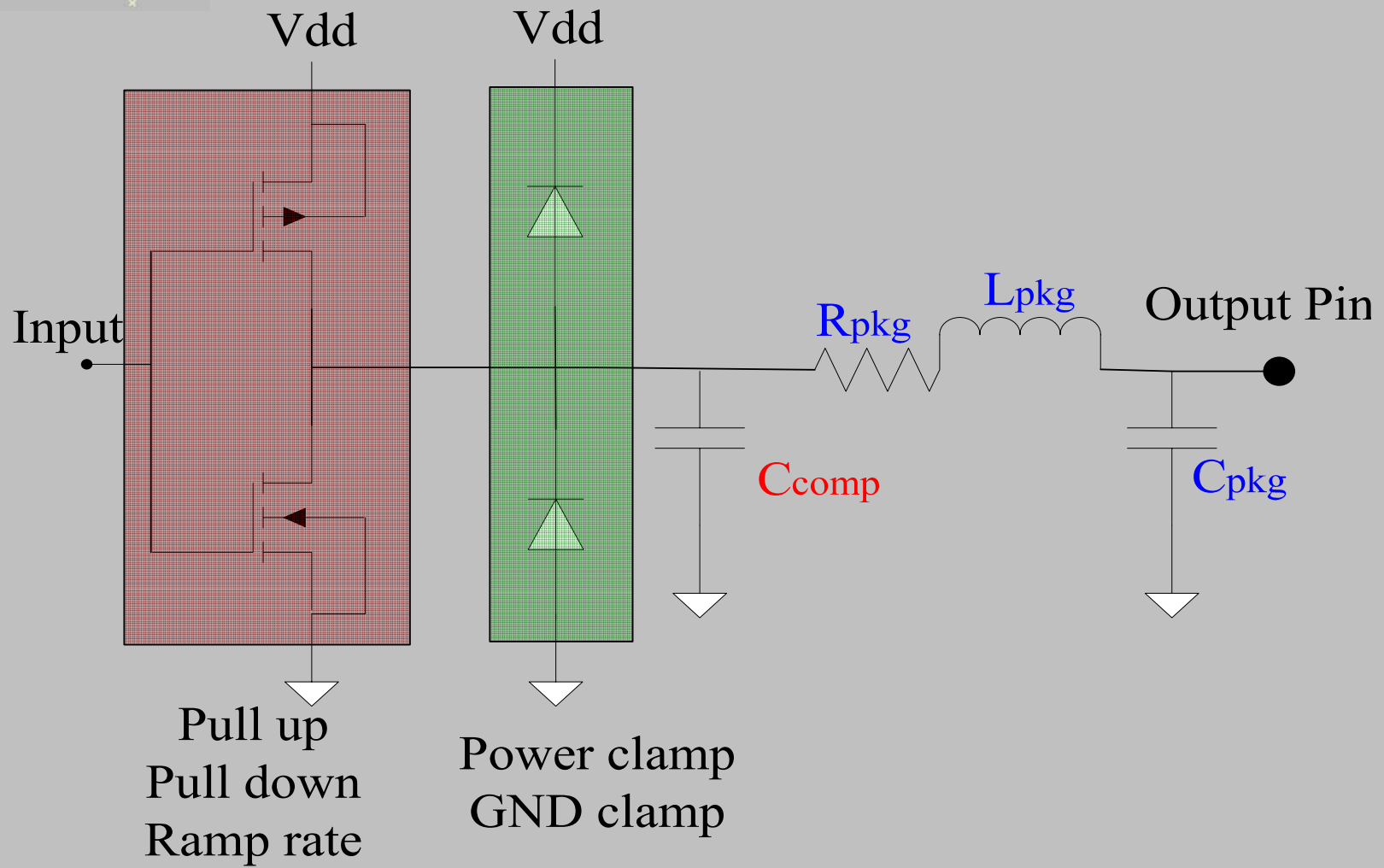
INPUT MODEL



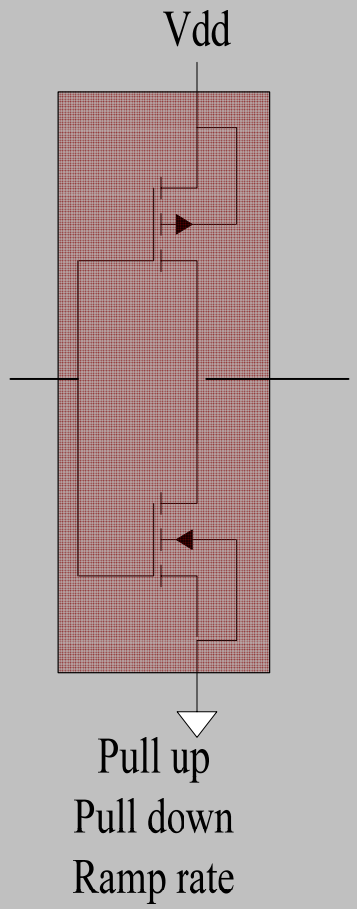
OUTPUT MODEL



Output Model

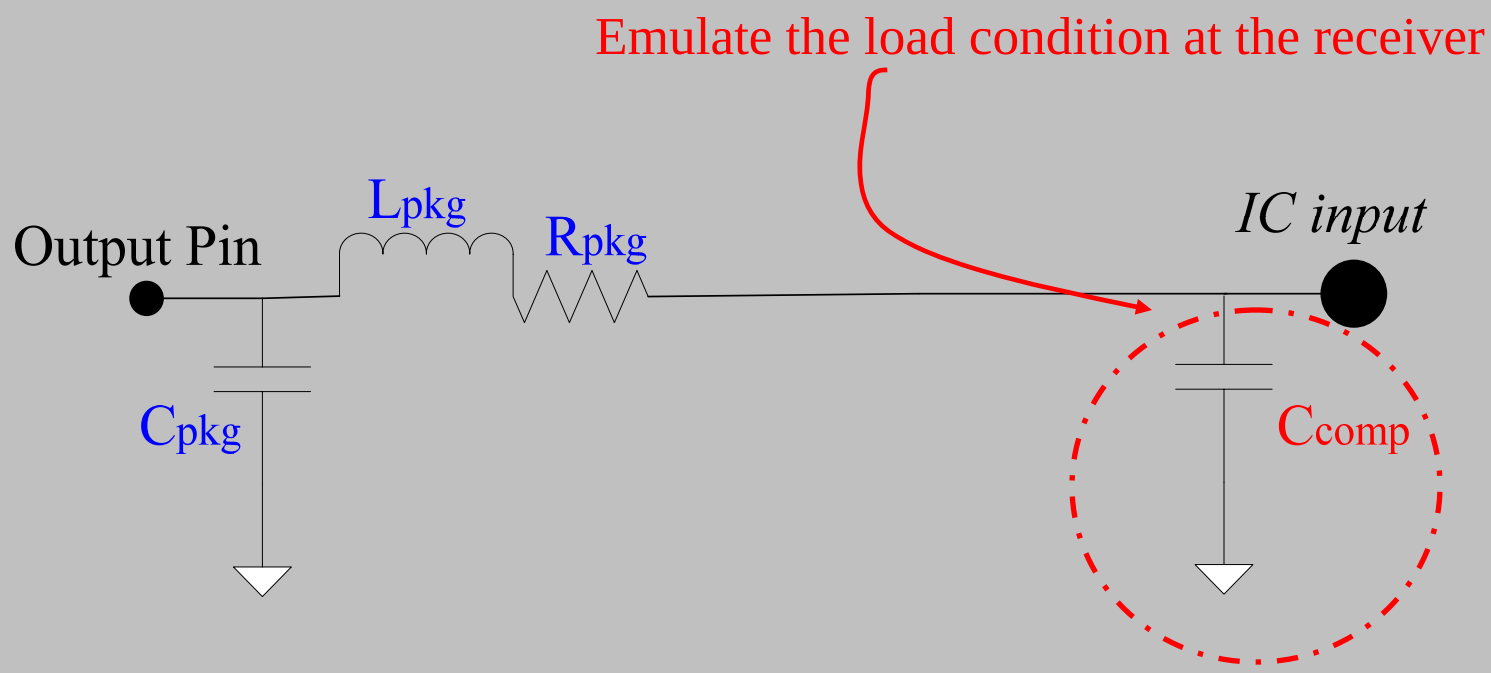


Common Output Configuration

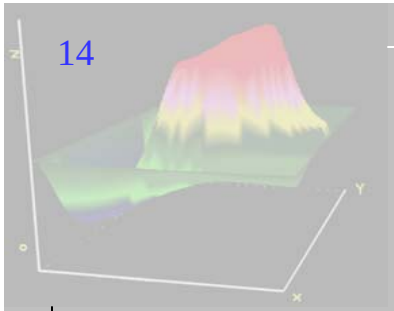


- The Push-Pull configuration driving behavior is identical to a I/O buffer for IBIS purpose [3].
- Two I/V characteristics are needed to describe this device according to the IBIS specifications, i.e., Pullup, Pulldown.
- Some models do not need all four I/V characteristics, i.e., Output Only Buffer (Pullup and Pulldown), Open Source Buffer + ESD protection (Pullup, GND Clamp and PWR Clamp).
- If the ESD protection circuit is present - two diodes - the GND/PWR clamp curves are also needed.

Input Model



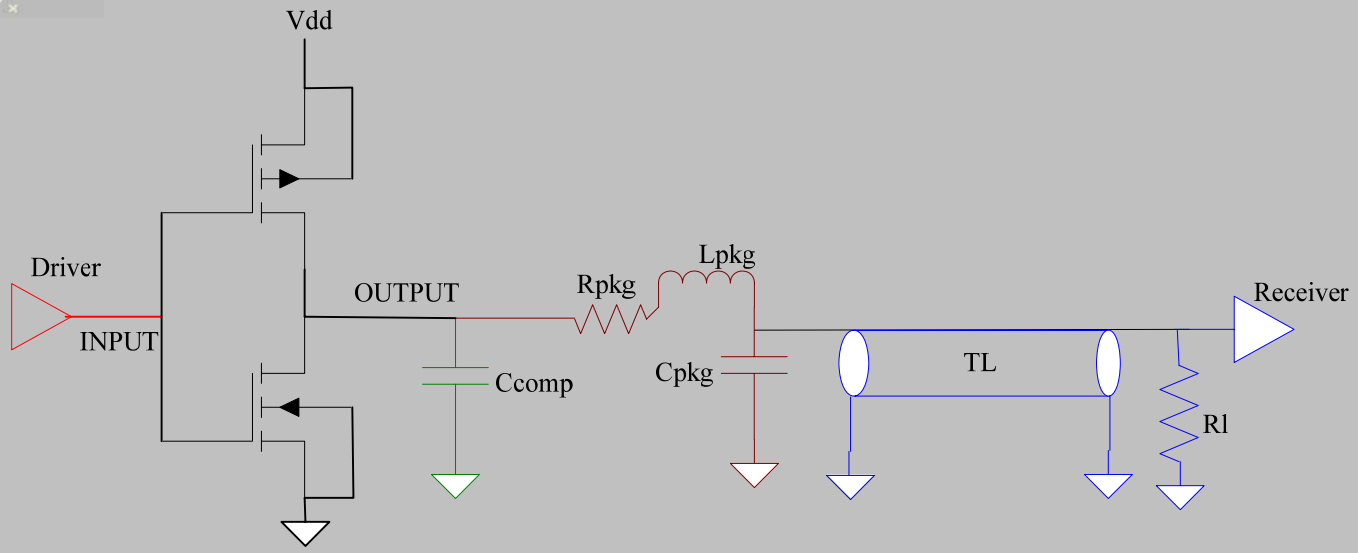
- If the ESD protection circuit is present - two diodes - GND/PWR clamp curves are needed as for the output model.
- The ESD protection circuit is used when the device is simulated beyond the nominal voltage conditions.



Common Features

- The GND/PWR Clamp curves are obtained in the same fashion as for the output model.
- The C_{comp} represents the capacitance associated with the transistors, the pad die and the on die interconnect: load condition at the receiver
- The parasitics associated with the package are represented through the keywords : Cpkg, Lpkg and Rpkg.

Simple I/O Circuit

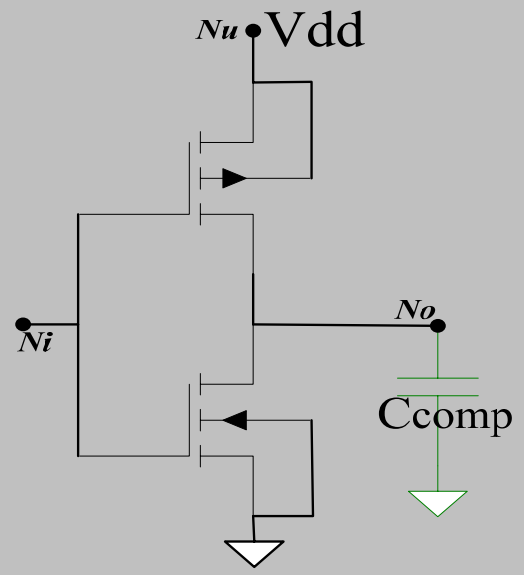


- Generic I/O only buffer realized by using several NMOS/PMOS models downloaded from www.mosis.org and enclosed into a “component.inc” model
- The driver swings between 0 and Vdd.
- When the input is HIGH the output is LOW and vice versa

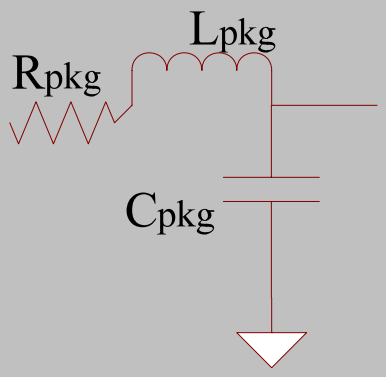
SPICE Model

.include component.inc
X_totem Ni No Nu 0 component
Ccomp No 0 5pF

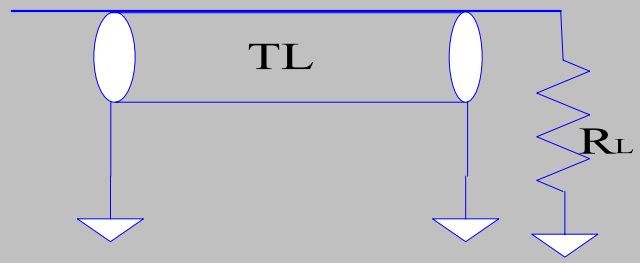
High Level SPICE Keywords: the NMOS and PMOS models are Level 49 HSPICE models



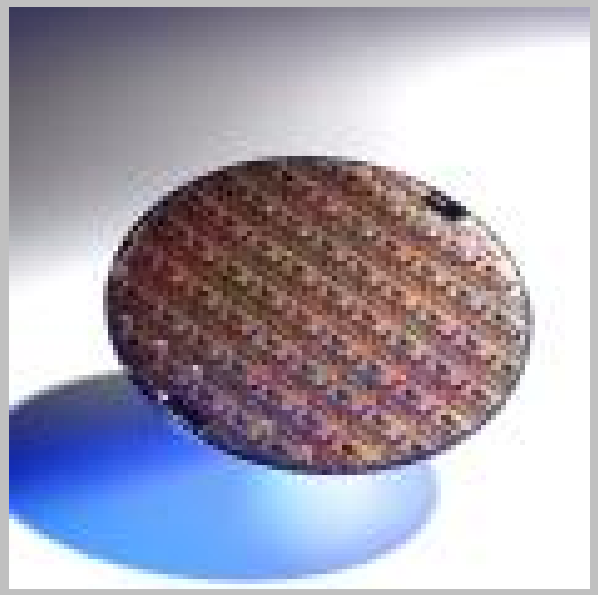
L_{pkg} → 4nH
R_{pkg} → 4mΩ
C_{pkg} → 4pF



TL → 50Ω & 1ns time delay
R_L → 50Ω



Extracting a SPICE/IBIS Models from a Wafer



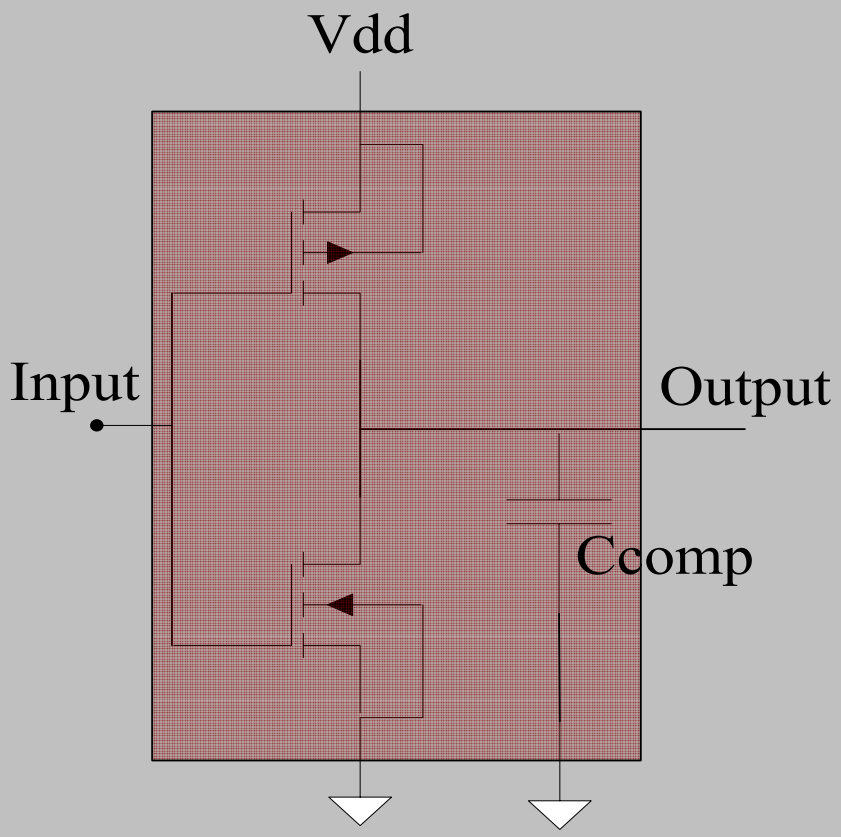
On Wafer Measurements

SPICE MODELS

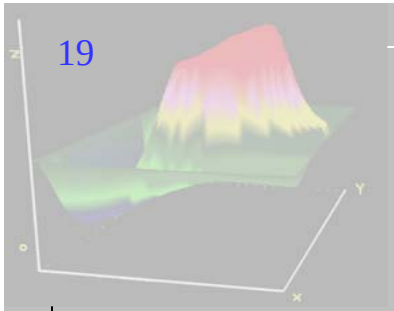
SPICE simulations

IBIS MODELS

Translating SPICE into IBIS

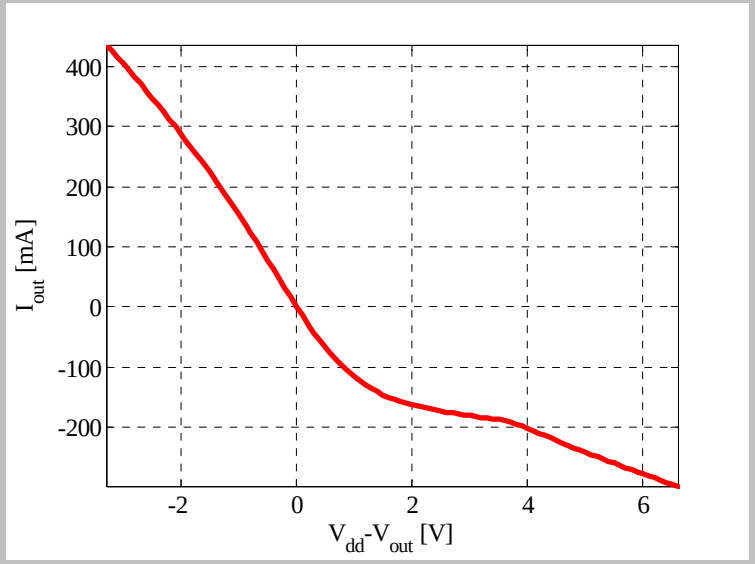


- The device under test is an only output buffer
- Pullup & Pulldown I/V tables are needed.
- No ESD protection is considered, therefore no GND or PWR Clamp I/V tables

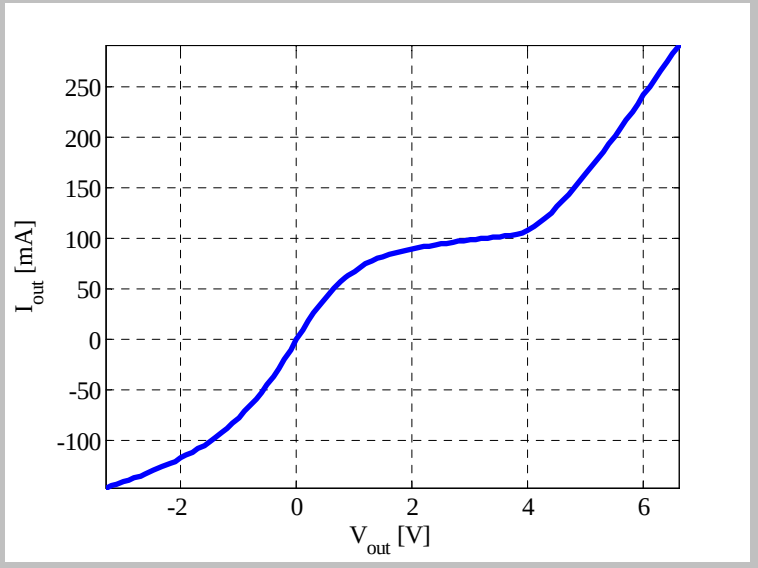


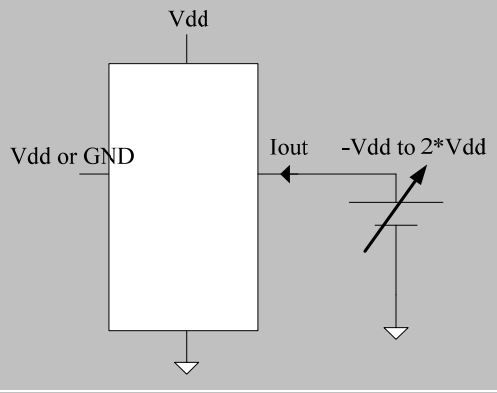
I/V Tables from SPICE Models

PULLUP



PULLDOWN

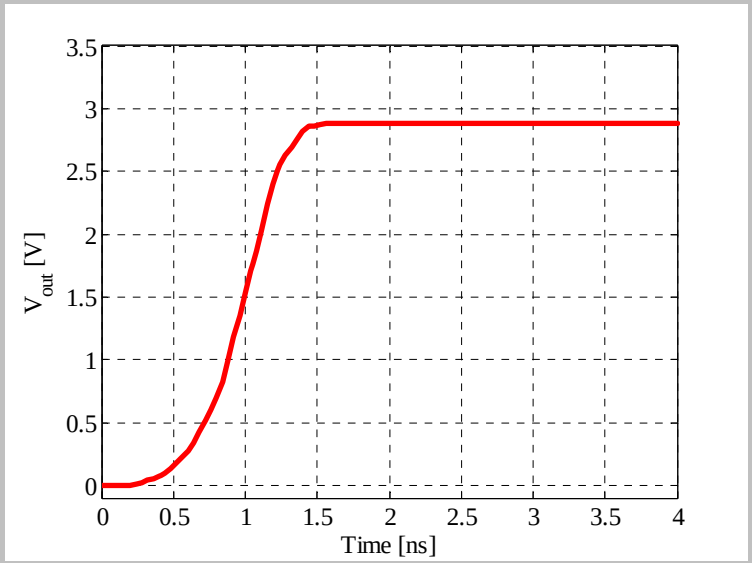




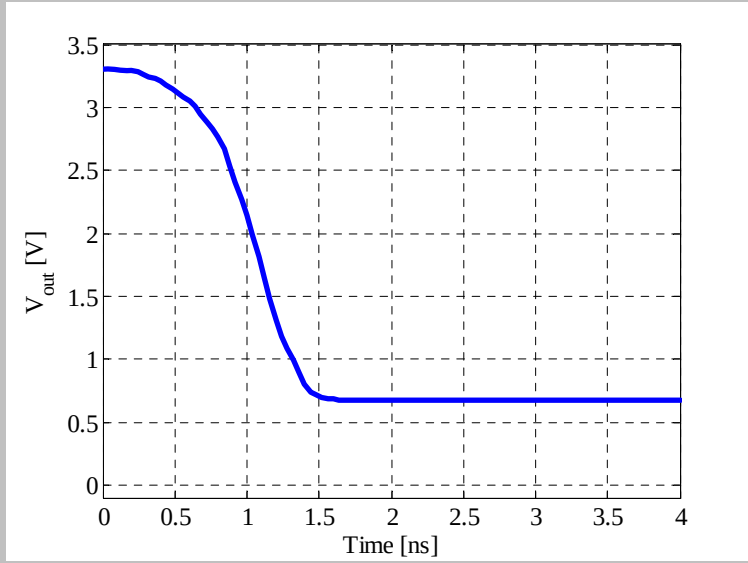
- The two characteristics are obtained by connecting a sweeping a DC source from minus V_{dd} to $2*V_{dd}$ and observing current flowing at the output terminal.
- Current is considered positive when it flows into the device

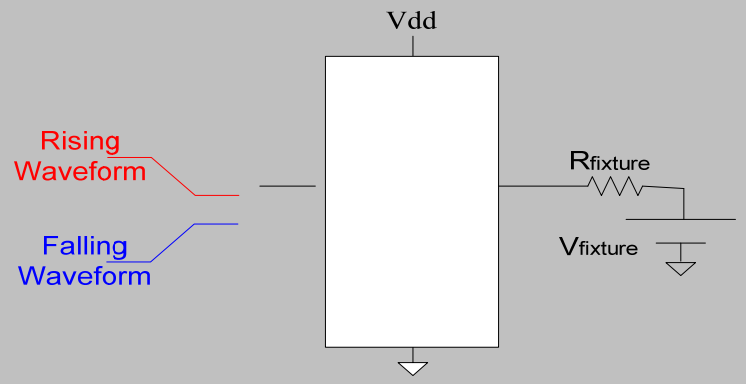
Rising/Falling Waveforms from SPICE Models

RISING

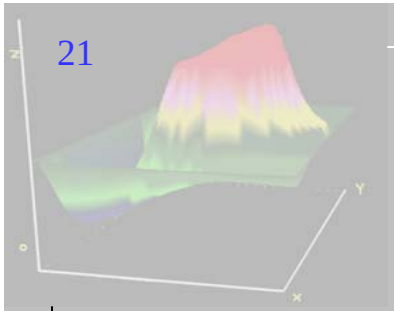


FALLING



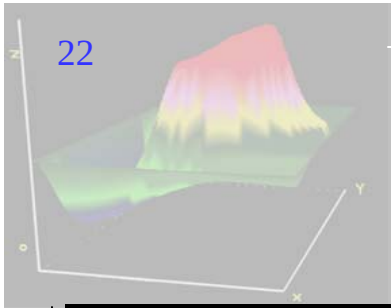


- The two characteristics are obtained by sweeping the input from 0 to Vdd or vice versa and inserting a Rfixture and Vfixture at the output



IBIS File : Header

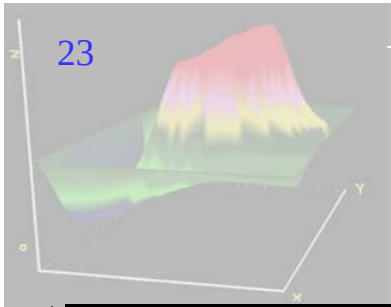
Keyword	Attribute	Req/Opt
[IBIS ver]	3.1	Required
[File name]	iobuffer.ibs	Required
[File Rev]	7.0	Required
[Date]	August, 14th 2006	Optional
[Source]	UMR EMC LAB	Optional
[Notes]	Notes for clarification	Optional
[Disclaimer]	Test Purpose	Optional
[Copyright]	UMR EMC LAB	Optional



IBIS File : Component

[Component]	IOBUFFER	Required
[Manufacturer]	UMR EMC LAB	Required
[Package] Rpkg 10m NA NA Lpkg 0.5nH NA NA Cpkg 5pF NA NA		Required
[Pin] signal_name model_name Sout Pout driver		Required

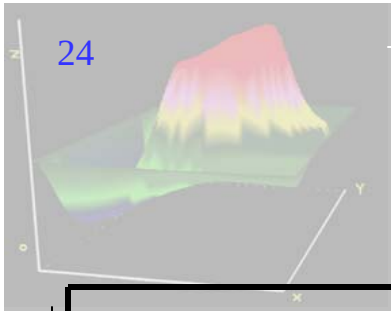
- The package is described by means of a series inductance, a series resistance and shunt capacitance



IBIS File : Model

[Model] driver Model_Type output C_comp 5pF NA NA		Required
[Temperature Range]	27 NA NA	Required
[Voltage Range]	3.3 NA NA	Required
[Pullup] V I(typ) I(min) I(max)		Required [model]
[Pulldown] V I(typ) I(min) I(max)		Required [model]

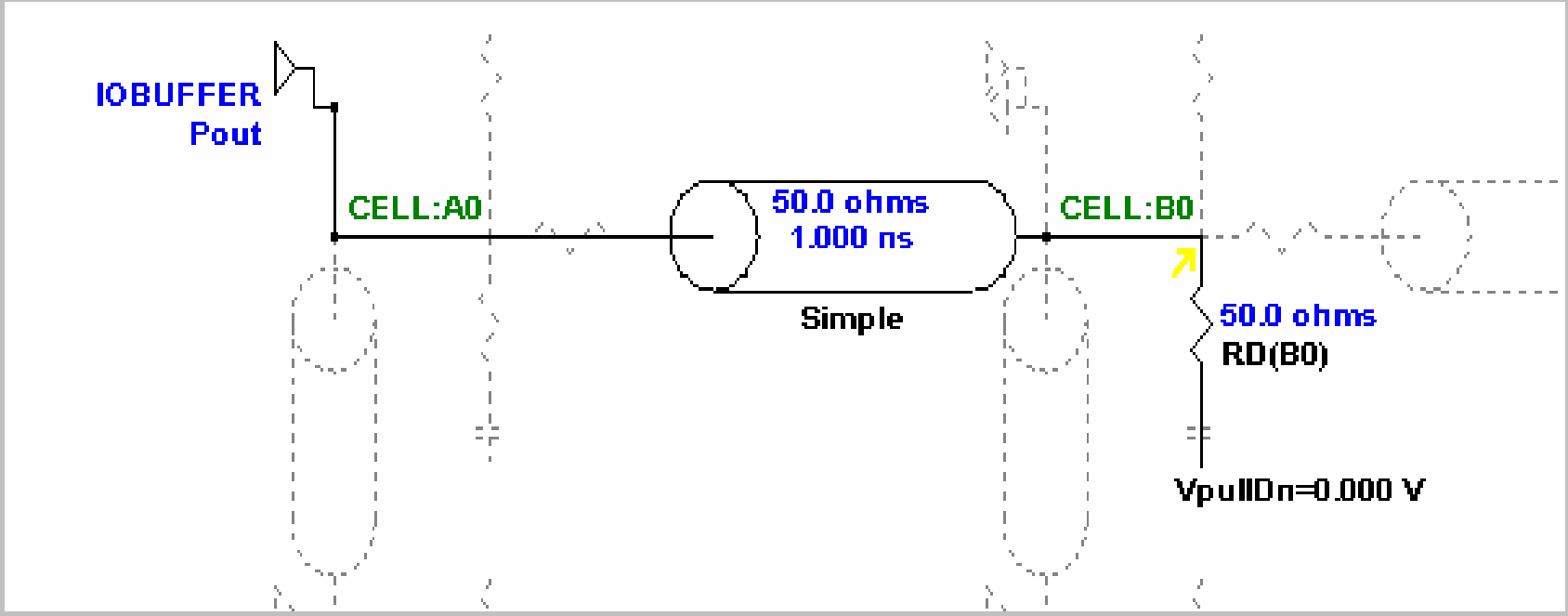
- C_{comp}, Temperature and Voltage require 3 values: typical (required), min (optional) and max (optional).



I/V & Switching Tables

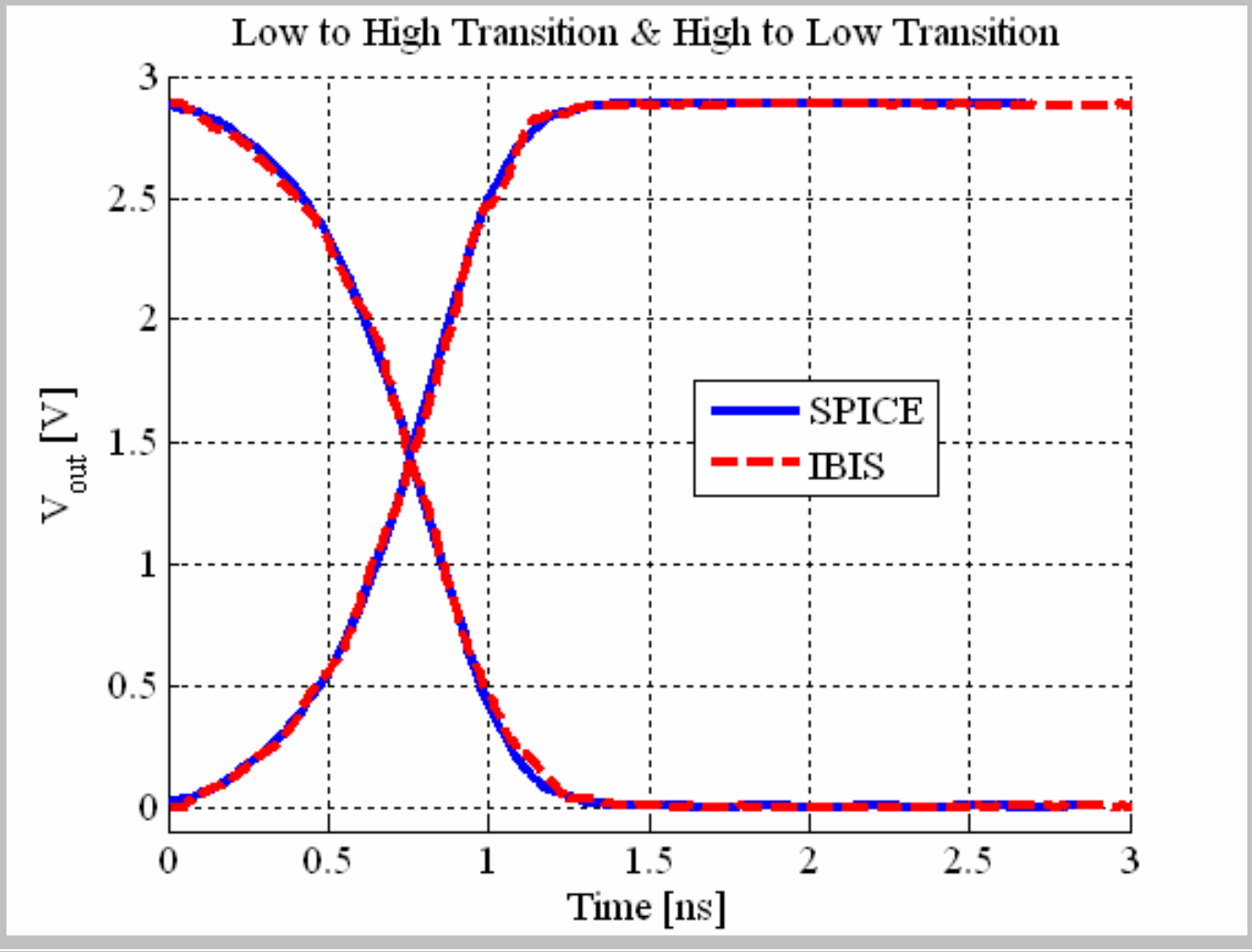
[Ramp] dV/dt_r 1/500p NA NA dV/dt_f 1/500p NA NA	Required
[Rising Waveform] R_fixture = 50 V_fixture = 0.0 Time V(typ) V(min) V(max)	Optional
[Falling Waveform] R_fixture = 50 V_fixture = 3.3 Time V(typ) V(min) V(max)	Optional
[End]	Required

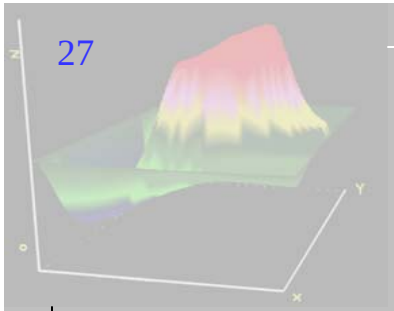
IBIS Simulator and Schematics



- The behavioral model data of the active device are then enclosed into a macro-model containing other components, i.e., resistors, transmission lines, etc., and this macro-model is simulated in a IBIS simulator, e.g. such as Hyperlinx.
- The active device is a output buffer characterized by one pin (Pout).

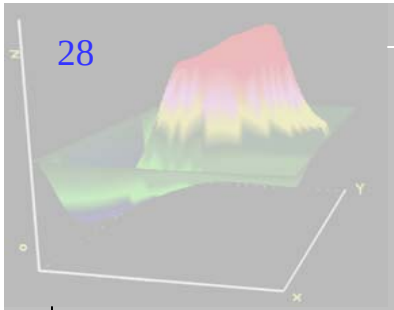
IBIS vs. SPICE Simulation Comparison





In Conclusion

- Use SPICE when accuracy warrants it.
- Use IBIS when complexity and circuit quantity warrants it.
- Some Do Not's
  - Do not rely on behavioral models under all circumstances.
  - Do not create modeling efforts without some understanding of expectations of results
- Some Do's
  - Understand the source of the models you have received.
  - Always verify models with test data.



References

[1] **IBIS Specifications available at http://www.eigroup.org/ibis/**

[2] **IBIS Open Forum, "IBIS modeling cookbook for IBIS version 4.0", 2004.**

[3] Bob Ross, "IBIS present and future", 7th IEEE Workshop on Signal Propagation on Interconnects, Siena, Italy, May 11th-14th 2003

[4] Mercedes Casamayor, "A first approach to IBIS models: what they are and how are they generated", AN-715Application Note, Analog Device.

[5] Arpad Muranji, "Introduction to IBIS models and IBIS model making", Intel Corporation, Folsom CA, November 3rd-4th 2003.

[6] "Validating and using IBIS files", Revision 1.0, National Semiconductor Corporation, Interface Product Group, January 2003.

[7] Vadym Heyfitch, " What makes a better I/O driver model", International Cadence Usergroup.

[8] Microelectronics, Millman-Grabel, McGraw-Hill, 2nd Ed. 1984

[9] Syed B. Huq, " Understanding and using IBIS models for Signal Integrity Analysis, High Level System Electronic Conference (HLSEC)1997.