A Novel CMOS OTA Based on Body-Driven MOSFETs and its Applications in OTA-C Filters

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***Abstract*— The operational transconductance amplifier (OTA) is one of the most significant building-blocks in integrated continuous-time filters. Traditional OTAs suffer linearity reduction as a result of the MOSFET scaling trend. In this paper, a body-driven (BD) CMOS triode-based fully balanced OTA is proposed to achieve low distortion and linear frequency tuning. In contrast to the gate-driven based OTAs (that have the tradeoff of input and tuning range), BD-based OTAs operate under a wide input range over a large tuning interval. Common-mode (CM) feedforward and CM feedback schemes have been developed so that the CM voltage varies only 7 mV over a tuning range of 1.2 V $\leq V_{\rm tune} \leq$ 1.58 V. Using the 0.18-μm N-well CMOS process, a third-order elliptic low-pass filter is implemented with the aid of the proposed OTA. The total harmonic distortion (is $-45\ dB$ for 0.8-V peak–peak ($V_{\rm pp}$) fully differential input signals. A dynamic range of 45 dB is obtained with the OTA's noise integrated over 1 MHz.**

***Index Terms*—Body driven (BD), continuous-time filters, operational transconductance amplifier (OTA), OTA-C filter.**

I. Introduction

OPERATIONAL transconductance amplifier (OTA) is one key building block in integrated continuous-time filters. Due to the scale-down of device sizes, traditional saturation-based OTAs face design challenges to overcome poor linearity and limited output impedance. Fully balanced topologies, such as source degeneration [1] and adaptive biasing techniques [2], are used to improve the linearity performance. However, each output current still suffers from significant second-order harmonics resulted from the saturation operation of MOSFETs. Moreover, if there is any mismatch due to process parameter tolerance and temperature gradient, the second-order harmonics will inevitably exist at the output of the OTA. [3], [4] utilize saturation-based MOSFETS to implement wide-range highly linear OTAs. The stacked transistor configuration demands high power supplies. Unfortunately, low-voltage supplies and scaled devices make the stacked transistor implementation no longer feasible.

Alternative OTA implementations have been developed to reduce the performance degradation [5]–[7]. For example, OTAs using grounded-source triode MOSFETs (i.e., triode-based OTAs) have been introduced in an attempt to utilize the inherent linear *V–I* property of triode MOSFETs. These OTAs normally incorporate regulation cascode-topology to stabilize $V_{\rm DS}$ of the triode transistor in order to perform transconductance tuning as well as enhance the output impedance without sacrificing the bandwidth. However, using triode MOSFETs inevitably induces a tradeoff, that is, wider input range leads to smaller transconductance tuning interval and vice versa. This is especially obvious in low-voltage applications. Furthermore, OTA implemented by short-channel devices shows distortion that is dominated by mobility degradation effects.

Another challenge exists in designing differential-mode grounded-source triode OTAs, such as pseudodifferential OTAs. Due to the inherent lack of common-mode (CM) rejection, pseudodifferential OTAs require effective approaches to suppress CM components. Yang and Enz [6] combined CM feedforward (CMFF) and CM feedback (CMFB) techniques to suppress CM input and output signals, respectively. However, by using the same topology in both CMFF and CMFB, the proposed differential OTA consumes significant power and heavily relies on high-resolution current mirrors and good-matching MOSFETS to achieve the cancellation of CM components. In contrast, without using CMFF, De Lima and Dualibe [7] proposed an adaptive bias CMFB to stabilize the CM components. Nevertheless, this technique demands large CM loop gain to impel the propagation of CM signals. In addition, the developed CMFB seriously limits the signal swing in low-voltage applications as an error amplifier with a tail current structure is employed.

In this paper, a triode-based OTA with enhanced transconductance linearity is presented. By using the BD technique, the tradeoff between input and tuning ranges is relaxed. In addition, a new CMFB technique is developed to stabilize the CM output voltage upon transconductance tuning without appreciably increasing the total power consumption.

The paper is organized as follows. In Section II, the novel differential BD triode OTA is proposed and the principle of operation is provided. In Section III, the applications of the proposed OTA, including an integrator and a third elliptic filter, are discussed. Results are discussed in Section IV and conclusions are drawn in Section V.

II. Principle of Operation

The proposed differential OTA is shown in Fig. 1.

The OTA core, which consists of MOSFETs M_1–M_8 and regulation amplifiers A, provides differential outputs ($V_{\rm out+}$ and $V_{\rm out-}$). As M_1 and M_2 operate in triode region, the

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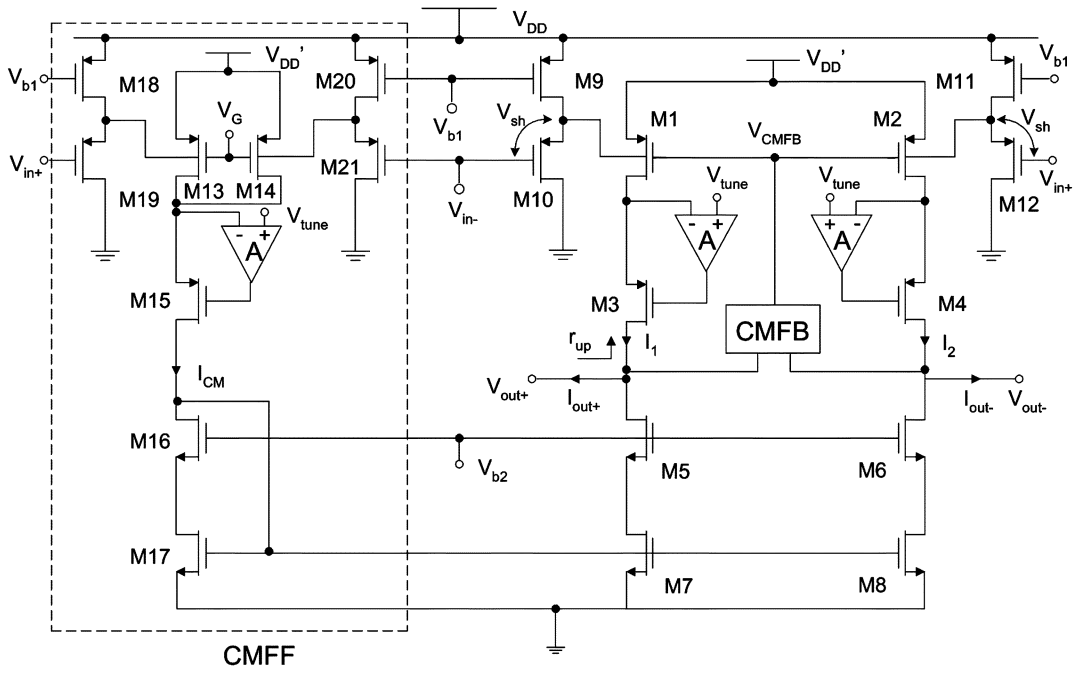

Fig. 1. Schematic of the proposed differential OTA.

transconductance tuning of the OTA is managed by controlling the source–drain voltages ($V_{\rm SD}$) of M_1–M_2. This is realized by the negative FB loop that is comprised of the regulation amplifier A and the cascode MOSFETs M_3–M_4. Ideally, $V_{\rm SD}$ is ensured to be $V'_{\rm DD} - V_{\rm tune}$. Besides offering the tuning capability, the local FB boosts the output impedance, thus enhancing the dc gain.

Compared to the conventional pseudodifferential transconductors [6] and [7], M_1 and M_2 are BD to achieve lower distortion [8]–[10]. The p-type MOSFETs are chosen to be BD in this design because n-well CMOS process is used. The sources of other p-type MOSFETs are tied to their own substrates, respectively.

The OTA core itself does not suppress CM signal. Inherently, it has the same gain for both differential-mode and CM signals. In order to suppress the input CM component, CMFF circuit (shown within the dotted block in Fig. 1.) is employed to adjust the bias of the OTA core. Except for M_{13} and M_{14} whose widths are half of the widths of M_1 and M_2, the rest of the CMFF transistors match the OTA core. By applying differential input signals ($V_{\rm in+} = V_{\rm CM} + V_{\rm in}/2$ and $V_{\rm in-} = V_{\rm CM} - V_{\rm in}/2$) to CMFF circuit, the transconductance current induced by $V_{\rm CM}$ is sensed and then cancelled out at the OTA outputs. M_9–M_{12} and M_{18}–M_{21} constitute level shifters to bring the output CM voltage and input CM voltage to the same level. This is necessary for unity-gain FB systems and filter designs, where the outputs of one OTA are normally the inputs of the next OTA stage. The biasing voltages V_{b1} and V_{b2} are provided externally for easy tuning. Their typical values are $V_{b2} = 1.2$ V, $V_{b2} = 1$ V. In the actual implementation, these bias voltages can be easily generated from bandgap reference circuits and poly resistors. Tuning bits may be added to the resistors for extra tunability.

A. Transconductance and Output Impedance Analysis

Using first-order approximation [11], the triode behavior of the p-MOSFET is described by

$$I_D = \beta\Bigg(V_{\rm SG} - |V_{T0}| - \gamma\sqrt{2|\phi_F| - V_{\rm SB}} + \gamma\sqrt{2|\phi_F|} - \frac{n}{2}V_{\rm SD}\Bigg)V_{\rm SD} \quad (1)$$

where $\beta = \mu C_{\rm ox}W/L$, ϕ_F refers to body Fermi potential whose typical value is 0.35 V, V_{T0} is zero bias threshold voltage, and n is the slope factor. For M_1 and M_2, $V_{\rm SB} = V'_{\rm DD} - (V_{\rm sh} + V_{\rm CM} \pm V_{\rm in}/2)$, respectively, where $V_{\rm sh}$ denotes the level-shifting voltage. Based on the fact that $V_{\rm in}/2 \ll 2|\phi_F| - V'_{\rm DD} + (V_{\rm sh} + V_{\rm CM})$, Taylor series expansion is performed on (1) to get the simplified expression

$$I_D = \beta\left(V_0 \pm K\frac{V_{\rm in}}{2} - \frac{n}{2}V_{\rm SD}\right)V_{\rm SD}. \quad (2)$$

V_0 refers to the saturation voltage that is expressed as

$$V_0 = V_{\rm SG} - |V_{T0}| - \gamma\sqrt{2|\phi_F| - V_{\rm SB0}} + \gamma\sqrt{2|\phi_F|} \quad (3)$$

where $V_{\rm SB0} = V'_{\rm DD} - (V_{\rm sh} + V_{\rm CM})$ denotes the source–body voltages of M_1 and M_2 at the dc operating point. K is defined as $K = \gamma/2\sqrt{2|\phi_F| - V_{\rm SB0}}$. If $I_{\rm CM}$ is equal to $\beta\,(V_0 - (n/2)V_{\rm SD})\,V_{\rm SD}$, the output currents are obtained as

$$I_{\rm out+,out-} = I_{1,2} - I_{\rm CM} = \pm\beta K V_{\rm SD}\frac{V_{\rm in}}{2}. \quad (4)$$

As shown in (4), the output currents are linearly related to $V_{\rm in}$ and the transconductance ($g = \beta K V_{\rm SD1}$) linearly depends on

the tuning voltage. Assuming that the dc gain of the regulation amplifier equals to A, the impedance seen into the drain of M_3 is approximately expressed as

$$r_{\rm up} = A\frac{g_{m3}}{g_{\rm DS1}g_{\rm DS3}}. \tag{5}$$

B. Distortion Analysis

Total harmonic distortion (THD) of a triode-mode MOSFET is dominated by the mobility degradation effect. Since the proposed OTA is differential, the third harmonic distortion dominates. By adopting the mobility model $\mu_{1,2} \approx \mu_0/[1+\theta(V_0 \pm KV_{\rm in}/2)]$ and applying Taylor series expansion on (1), the third harmonic distortion is obtained as

$$\mathrm{HD}_3 = \frac{1}{16}\frac{\theta^2}{(1+\theta V_0)^2}(KV_{\rm in})^2 \tag{6}$$

where μ_0 is the zero-field carrier mobility, θ is the mobility degradation coefficient. As the typical value of K is less than one, the proposed BD OTA has better linearity than the conventional GD triode-based OTAs [6], [7] and [12], whose third harmonic distortion is expressed as

$$\mathrm{HD}_3 = \frac{1}{16}\frac{\theta^2}{(1+\theta V_0)^2}(V_{\rm in})^2.$$

Moreover, V_0 in (6) can be easily set to a higher value than that of the gate-driven counterpart. Equation (3) reveals $V_{\rm SG}$ has much larger influence on V_0 than $V_{\rm SB0}$ does. Hence, by connecting the gates of M_1 and M_2 to the ground or the negative power supply, V_0 can be easily maximized for the BD OTA.

C. Input and Tuning Ranges

Assuming the differential input voltages equal to $V_{\rm CM} \pm V_{\rm in}/2$, the maximum tuning range for the conventional GD triode-based OTA is given by

$$V_{\rm SD,max,}{}_g = V_{\rm DD} - V_{\rm CM} - \frac{1}{2}V_{\rm in} - |V_T|. \tag{7}$$

Equation (7) reveals that the tuning interval is bound by the input range and vice versa. In contrast, the maximum tuning range of the proposed BD OTA is expressed as

$$\begin{aligned} V_{\rm SD,max,}{}_b =& V\prime_{\rm DD} - V_G - (|V_{T0}| \\ &+ \gamma\sqrt{2|\phi_F| - \left(V\prime_{\rm DD} - V_{\rm CM} - V_{\rm sh} - \frac{1}{2}V_{\rm in}\right)} \\ &- \gamma\sqrt{2\,|\phi_F|}). \end{aligned} \tag{8}$$

Since $V_{\rm SD,max,}{}_b$ has much weaker relationship with $V_{\rm in}$ than $V_{\rm SD,max,}{}_g$ does, the tuning range of the proposed OTA is less limited by the input range. By using the typical values of $|V_{T0}| = 0.48$ V, $|\phi_F| = 0.44$ V, $\gamma = 0.65$ V$^{1/2}$, $V_{\rm DD} = 1.8$ V, $V'_{\rm DD} = 1.6$ V, $V_{\rm sh} = 0.6$ V, $V_{\rm CM} = 0.8$ V, $V_G = 0.7$ V, $V_{\rm SD,max}$ for both OTAs is plotted as a function of the input peak-to-peak value $V_{\rm pp}$ in Fig. 2. It shows $V_{\rm SD,max,}{}_g$ declines much faster than $V_{\rm SD,max,}{}_b$ as $V_{\rm pp}$ increases. For instance,

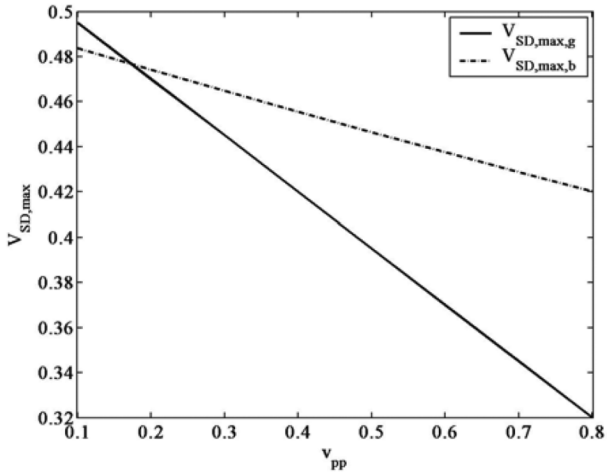

Fig. 2. Tuning range versus input range for the conventional and proposed OTAs.

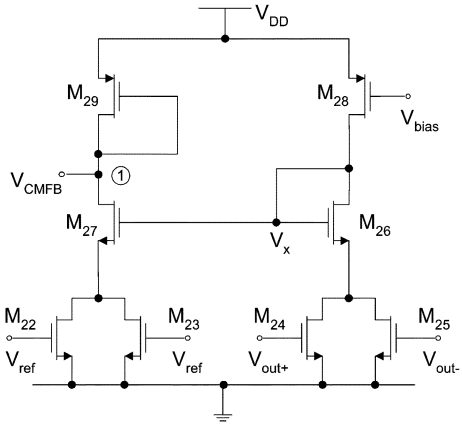

Fig. 3. Schematic of the CMFB block.

when $V_{\rm pp}$ varies from 0.1 to 0.8 V, $V_{\rm SD,max,}{}_g$ decreases by 35% of its original value while $V_{\rm SD,max,}{}_b$ only decreases by 13%. Hence, although the input and tuning ranges exhibit strong tradeoff for the conventional OTA, the compromise is not apparent in the BD topology. This property enables the proposed OTA to achieve high input range and high tuning range, simultaneously. However, caution should be given to the source–body diode turn-on voltage (typically 0.6 V). Maximum $V_{\rm SB}$ for M_1/M_2 is suggested to be always kept below 0.4 V to avoid large leakage current.

D. CMFB Design

Fully balanced topology requires CMFB to stabilize the CM output voltage. It is essential to design a CMFB circuit such that it will not reduce the output signal swing of the OTA. To achieve this goal, CMFB topology employing triode-based transconductor is used [13] (shown in Fig. 3). M_{24} and M_{25} sense the CM output voltage. Any variation of the CM output voltage affects V_x. Then M_{27}, which is degenerated by M_{22} & M_{23} and loaded by diode-connected M_{29}, amplifies the variation of V_x. $V_{\rm CMFB}$ is then fed to the gates of M_1 and M_2, through which $V_{\rm CMFB}$ is converted to current and finally the CM output voltage is adjusted to its desired reference value. The effectiveness of this CMFB structure

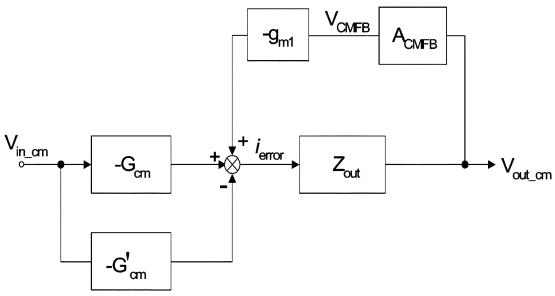

Fig. 4. CMFB signal flow diagram.

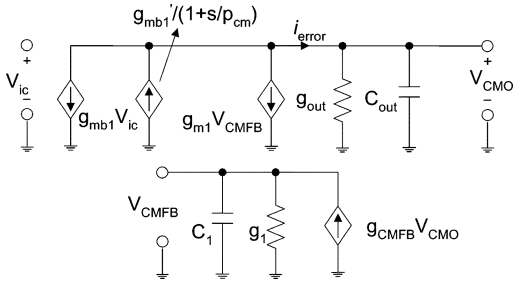

Fig. 5. Small-signal model of the CMFB scheme.

can be better understood with the aid of the signal-flow diagram shown in Fig. 4. Since the CM signal appears symmetrically at the fully-balanced outputs, considering single-ended topology is sufficient for the analysis. In Fig. 4, $G_{\rm CM} = g_{mb1}$ refers to the transconductance of the proposed OTA core, $G'_{\rm CM} = gmb1'$ denotes the transconductance of the CMFF block, and $Z_{\rm out}$ is the output impedance of the proposed OTA.

Based on Fig. 4, the single-ended CM gain is calculated to be

$$A_{\rm CM} = Z_{\rm out}\frac{-G_{\rm CM} + G'_{\rm CM}}{1 + A_{\rm CML,DC}} \tag{9}$$

where

$$A_{\rm CML,DC} = Z_{\rm out} g_{m1} A_{\rm CMFB}$$
$$A_{\rm CMFB} = \{(V_{\rm GS29} - |V_{T29}|)/(V_{\rm GS27} - |V_{T27}|) + V_{\rm DS22}\} \cdot \{V_{\rm DS24}/V_{\rm GS24} - V_{T24}\}.$$

Since the second term of $A_{\rm CMFB}$ is less than one due to the triode operations of M_{24} and M_{25}, $A_{\rm CMFB}$ can be increased by minimizing the saturation voltage of M_{27}. Given the single-ended differential-mode gain $A_{\rm DM}$ is $g_{mb1}Z_{\rm out}/2$, the single-ended CM rejection ratio (CMRR) as

$$\text{CMRR} = \frac{A_{\rm DM}}{A_{\rm CM}} \approx \frac{g_{mb1}}{(-g_{mb1} + g'_{mb1})}\frac{A_{\rm CML,DC}}{2}. \tag{10}$$

Due to the CMFF topology that cancels out the CM input signal under ideal matching condition (i.e., $G_{\rm CM} \approx G'_{\rm CM}$), the proposed OTA can achieve very high CMRR. Hence, the requirement for large $A_{\rm CML,DC}$ is greatly relaxed. This is an obvious advantage over relying on large CM loop gain to impede the propagation of CM signals [7]. In addition, it should be emphasized that, by taking advantage of the unused fourth terminal (i.e., the gate terminal) of the BD M_1 and M_2, the CMFB block is easily incorporated in the proposed OTA without adding extra devices. Therefore, the power consumption as well as the chip size are reduced. This is superior to [6] where an extra single-ended OTA topology has to be employed to construct the CMFB block.

To evaluate the frequency response of the CMFB block, the simplified small-signal diagram is shown in Fig. 5. $g_{\rm CMFB}$ refers to the transconductance of the CMFB block, g_1 and C_1 are the equivalent conductance and parasitic capacitance at the output node of the CMFB block, i.e., node ① in Fig. 3. $p_{\rm CM}$ refers to the pole that is associated with the cascode current mirror in the CMFF block. The transfer function is derived as

$$\frac{V_{\rm CMO}}{V_{ic}} = \frac{\frac{-g_{mb1}+g'_{mb1}}{\frac{(1+s}{p_{\rm CM})}}}{g_{\rm out} + sC_{\rm out}}\frac{1}{1 + A_{\rm CML}(s)} \tag{11}$$

where $A_{\rm CML}(s) = \{g_{\rm CMFB}/g_1 + sC_1\}\{g_{m1}/g_{\rm out} + sC_{\rm out}\}$, $g_{\rm CMFB} = \{g_{m27}/1 + g_{m27}/(2g_{\rm DS22})\}\{g_{m24}/g_{\rm DS24}\}$, $g_1 = g_{m29}$, $C_1 \approx 2C_{\rm GS1} + C_{\rm GS29}$, $g_{\rm out} = 1/r_{\rm out} = g_{\rm up} + g_{\rm down}$, $g_{\rm up} = 1/r_{\rm up}$. Here $r_{\rm up}$ is given in (5), and $g_{\rm down}$ is the conductance seen into the drain of M_5, $g_{\rm down} = (g_{\rm DS5}g_{\rm DS7})/g_{m5}$.

The closed-loop poles take the complex form. The center frequency ω_0 and quality factor Q are given by

$$w_0 \approx \sqrt{\frac{g_{\rm CMFB}g_{m1}}{(C_1 C_{\rm out})}} \tag{12}$$

$$Q = \frac{\sqrt{A_{\rm CML,DC}p_1p_2}}{(p_1 + p_2)} \tag{13}$$

where $p_1 = g_{\rm out}/C_{\rm out}$ (dominant pole), $p_2 = g_1/C_1$ (nondominant pole).

Typically, ω_0 is larger than the unity-gain bandwidth of the differential-mode frequency response. Except from the complex conjugate poles originated from CMFB loop, (11) also has a nondominant real pole $p_{\rm CM}$ contributed by the CMFF block.

E. Frequency Response of the OTA Core

For simplicity but without losing generality, half-circuit of the differential OTA core is studied. The regulation amplifier is modeled as a one-pole system with $C_{\rm in}$ and $C_{\rm out}$ as its input and output capacitors, g_{mA} and $g_{\rm out}$ as its transconductance and output conductance. The active loads of the OTA (i.e., M_5 and M_7 or M_6 and M_8) are assumed to be ideal. Then, the small-signal half-circuit diagram of the proposed OTA is shown in Fig. 6. $C_{\rm load}$ is the load capacitor. C_1, which refers to the parasitic capacitance associated with node ①, is expressed as $C_1 = C_{gd1} + C_{\rm in}$. $C_{{\rm GS}i}, C_{gdi}, C_{dbi}$ are gate–source, gate–drain, and drain–body capacitances of $M_i (i = 1, 3)$, respectively. After fundamental analysis and simplification, the OTA is modeled as a 3-pole, 3-zero system and its transfer function is approximately expressed as

$$\frac{V_{\rm out}(s)}{V_{\rm in}(s)} = -\frac{N_3s^3 + N_2s^2 + N_1s + N_0}{D_3s^3 + D_2s^2 + D_1s + D_0} \tag{14}$$

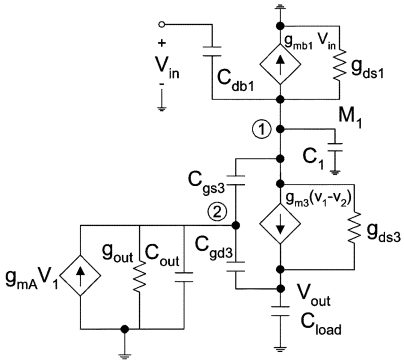

Fig. 6. Small-signal half-circuit of the differential OTA.

where

$$
\begin{aligned}
D_0 &= g_{\mathrm{DS1}}g_{\mathrm{DS3}}g_{\mathrm{out}};\\
D_1 &= g_{m3}g_{mA}C_{\mathrm{load}};\\
D_2 &= C_{\mathrm{load}}[(C_{gd3}+C_{\mathrm{out}})(g_{\mathrm{DS1}}+g_{m3})+C_{\mathrm{GS3}}(g_{\mathrm{DS1}}+g_{mA})];\\
D_3 &= C_{\mathrm{load}}[C_{db1}C_{\mathrm{GS3}}+C_1(C_{gd3}+C_{\mathrm{GS3}}+C_{\mathrm{out}})];\\
N_0 &= g_{m3}g_{mA}g_{mb1};\\
N_1 &= -g_{m3}g_{mA}C_{db1};\\
N_2 &= -C_{db1}[C_{\mathrm{out}}g_{m3}+C_{gd3}(g_{m3}-g_{mA})];\\
N_3 &= -C_{db1}C_{gd3}C_{\mathrm{GS3}}.
\end{aligned}
$$

To achieve better phase error performance, OTA having conjugate nondominant poles is preferable. A simple and effective way to realize this is to increase g_{mA} by increasing the bias current of the regulation amplifier. Further increasing g_{mA} will push these conjugate poles to higher frequency. However, a good tradeoff between the integrator phase error and power consumption is necessary for an optimal design. The dominant zero located at $z_1 = -N_0/N_1 = g_{mb1}/C_{db1}$ is associated with the FF path created by C_{db1}. The other two zeros appear at high frequencies.

F. Noise Analysis

Upon taking the assumptions of uncorrelated noise sources and perfect matching between matched transistor pairs [15], the input referred voltage noise of the proposed OTA is given as

$$
\overline{V_{n,\mathrm{in}}^2} \approx 2\left[\overline{V_{n1}^2}+\overline{V_{n10}^2}+\left(\frac{g_{m9}}{g_{m10}}\right)^2\overline{V_{n9}^2} + \left(\frac{g_{\mathrm{DS1}}}{g_{mb1}}\right)^2\overline{V_{nA}^2}+\left(\frac{g_{m7}}{g_{mb1}}\right)^2\overline{V_{n7}^2}\right] \quad (15)
$$

where $g_{\mathrm{DS1}}/g_{mb1} \approx (V_{\mathrm{SG1}}-|V_{T1}|)/V_{\mathrm{SD1}}$, $\overline{V_{n1}^2} \approx \{1/K^2\}\{8kT(1+K+g_{\mathrm{DS1}}/g_{m1})/3g_{m1}\}\{1+\eta+\eta^2/1+\eta\}+\{1/K^2\}KF(1+C_FK^2)/f^{AF}C_{\mathrm{ox}}^2W_1L_1$, $\overline{V_{n10}^2} = 8/3kT/g_{m10} + KF/\left(f^{AF}C_{\mathrm{ox}}^2W_{10}L_{10}\right)$, $\overline{V_{n9}^2} = 8/3kT/g_{m9} + KF/\left(f^{AF}C_{\mathrm{ox}}^2W_9L_9\right)$, $\overline{V_{n7}^2} = 8/3kT/g_{m7} + KF/\left(f^{AF}C_{\mathrm{ox}}^2W_7L_7\right)$, $\eta = g_{mb1}/g_{m1}$, K is a process-dependent constant, KF is the flicker noise coefficient, AF is the flicker noise exponent.

The noise contributed from cascode M_3–M_6 and M_{15}–M_{16} is neglected due to the small value. The noise generated from CMFF block is cancelled out due to the symmetrical and matching topology. Since M_1–M_2 operate in triode region, g_{DS1}/g_{mb1} is larger than 1. This also holds true for g_{m7}/g_{mb1}. Therefore, the major noise sources of the proposed OTA are the regulation amplifier A and M_7–M_8. Thus, designing a regulation amplifier with low input-referred noise significantly helps to decrease the overall OTA noise.

G. Regulation Amplifier Design

Without the regulation amplifier, the dc gain of the proposed OTA is simply $A_{\mathrm{DC}} = g_{mb1}/g_{\mathrm{out}}$. Since g_{mb1} is relatively smaller than g_m, a regulation amplifier with high dc gain is desired. In submicron technologies, conventional simple one-stage amplifiers typically have low dc gain and therefore not sufficient for this design. Although two-stage amplifiers have the potential to provide much higher dc gain, it may induce serious instability issue. In addition, the required Miller compensation drastically reduces the OTA bandwidth. On the other hand, one-stage cascode amplifiers can achieve high dc gain without sacrificing the unity-gain bandwidth. Therefore, a suitable cascode configuration needs to be determined to implement the regulation amplifier.

In Fig. 1, to guarantee M_3/M_4 operating in saturation region, these relationships should hold, $V_{\mathrm{tune,max}} - V_{\mathrm{DS\,min\,3,4}} - |V_{T3,4}| \le V_{g3,4} \le V_{\mathrm{tune,min}} - |V_{T3,4}|$, where $V_{\mathrm{DS\,min\,3,4}} = V_{\mathrm{tune,max}} - (V_{\mathrm{CM}} + V_{\mathrm{out,swing}})$, $V_{\mathrm{out,swing}}$ is the AC magnitude of the single-ended output voltage (typically 0.2). By taking the typical values, it yields $0.55\ \mathrm{V} < V_{g3,4} < 0.75\ \mathrm{V}$.

As shown in Fig. 7, the telescope-cascode amplifier and folded-cascode amplifier can be used as the regulation amplifier. In Fig. 7(a), since V_{tune} is close to the positive power supply, level shifters $(M_{A10}$–$M_{A13})$ are necessary to properly bias the p-type inputs. Since the level-shifters add extra noise to the telescope configuration, the folded-cascode topology with lower noise is preferable as the regulation amplifier. The amplifier noise can be further decreased by the following methods: 1) increasing both the bias current and the aspect ratios of M_{A1}/M_{A2} tends to reduce thermal noise; and 2) increasing the lengths of M_{A4} and M_{A10} reduces the flicker noise.

The dc gain of the folded-cascode topology is $A_{DC,A} \approx \sqrt{2\beta_{A1}I_{A1}}\sqrt{2\beta_{A7}}/\lambda^2 I_{A7}^{3/2}$. To increase the dc gain, more bias current is assigned to the input stage than to the output stage in this design. Specifically, we choose $I_{A1,2} = 2/3I_b, I_{A6,7} = 1/3I_b$. This method, however, slows down the large-signal settling time. To alleviate this problem, M_{A12} and M_{A13} are added [16]. Under quiescent condition, these two MOSFETs do not conduct currents. When a large step signal is applied to the inputs, M_{A12}/M_{A13} becomes activated to conduct extra current. This helps to speed up the recovery process.

III. Realization of a Third-Order Elliptic Filter

An integrator with a nominal unity-gain frequency around 1.2 MHz for 5-pF load capacitor has been sized based on the design parameters of a standard 0.18-μm n-well CMOS technology using 1.8-V power supply ($V_{\mathrm{DD}} = 1.8$ V). Typical process parameters are $C_{\mathrm{ox}} = 846\ \mathrm{nF/cm^2}$, $V_{THN} = 0.43$ V,

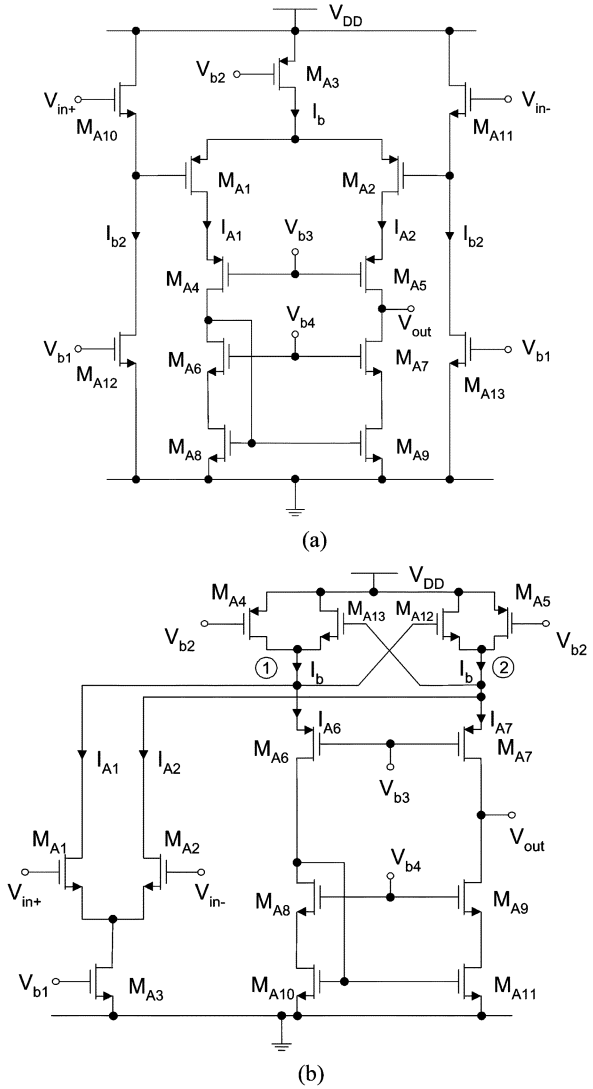

Fig. 7. Regulation amplifier topologies. (a) Telescope-cascode topology. (b) Folded-cascode topology.

TABLE I
MOSFET DIMENSIONS OF THE PROPOSED OTA

MOSFET Name	Aspect Ratio (W/L)	MOSFET Name	Aspect Ratio (W/L)
M_1, M_2	20μm/0.8μm	M_{13}, M_{14}	10μm/0.8μm
M_3, M_4, M_{15}	20μm/0.4μm	M_5, M_6, M_{16}	32μm/2μm
M_7, M_8, M_{17}	8μm/1μm	M_9, M_{11}, M_{18}, M_{20}	2μm/0.6μm
M_{10}, M_{12}, M_{19}, M_{21}	3μm/0.6μm	M_{22}, M_{23}, M_{24}, M_{25}	0.22μm/0.2μm
M_{26}, M_{27}	0.5μm/0.2μm	M_{28}, M_{29}	0.22μm/0.2μm

$V_{\rm THP} = -0.48$ V, $\gamma_n = 0.65$ $\rm V^{1/2}$, $\gamma_p = 0.66$ $\rm V^{1/2}$, $\mu_n = 438$ $\rm CM^2/Vs$, and $\mu_p = 104$ $\rm CM^2/Vs$. In order to maximize the input and output signal swing range, $V'_{\rm DD} = 1.6$ V and $V_{\rm CM}$ is chosen to be 0.8 V. With $V_{\rm CMFB} = 0.7$ V, $V_{\rm tune}$ can be tuned in the interval of $1.2\ {\rm V} < V_{\rm tune} < 1.58$ V, within which M_1 and M_2 are guaranteed to operate in triode-region. Transistor dimensions are listed in Table I.

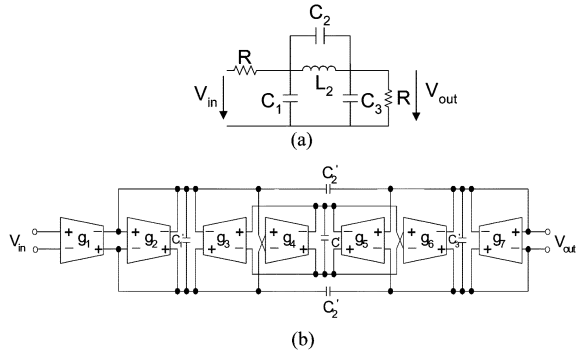

Fig. 8. Third-order elliptic low-pass filter. (a) *RLC* ladder prototype (b) OTA-C implementation.

TABLE II
COMPONENT VALUES OF THE THIRD-ORDER ELLIPTIC LOW-PASS FILTER

Device Name	Value	Device Name	Value
g_1, g_3, g_6	2g	g_2,g_4, g_5, g_7	G
C_1'	$[gC_1$-$(2C_{in}+3C_{out})]/2$	C_2'	gC_2
C_3'	$[gC_3$-$(2C_{in}+2C_{out})]/2$	C'	$[g_3g_4L_2/g$-$(2C_{in}+2C_{out})]/2$

The proposed OTA is utilized to implement an OTA-C filter. Synthesized from a doubly terminated passive *LC* ladder, a third-order elliptic low-pass filter with nominal cutoff frequency of 1 MHz and stopband frequency of 2 MHz is depicted in Fig. 8. The specifications require less than 1-dB passband attenuation and more than 34-dB stopband attenuation. The inductor is simulated using gyrator–capacitor combination [17]. While designing the filter, parasitic capacitances are taken into account to improve the accuracy of the filter characteristics. Those include 2-fF input capacitance and 70-fF output capacitance for the proposed OTA. An identical tuning voltage is applied to all the OTAs. The design parameters of the filter components are listed in Table II, where $g = 48.12\,\mu$S, $C_1 = 2.86423 * 10^{-7}$F, $C_2 = 3.58136 * 10^{-8}$F, $C_3 = 2.86423 * 10^{-7}$F, $L_2 = 1.38253 * 10^{-7}$H, $C_{\rm in} = 2$ fF (input capacitance of the proposed OTA), $C_{\rm out} = 70$ fF (output capacitance of the proposed OTA).

IV. SIMULATION RESULTS

Fig. 9 displays the OTA transconductance as a function of $V_{\rm in}$ for different values of $V_{\rm tune}$. In order to compare the performance of the proposed BD OTA with the conventional gate-driven counterpart (shown in Fig. 9), the transconductance of each OTA topology is shown in Fig. 10(a) and (b), respectively. Fig. 10(a) reveals that, for the proposed BD OTA, high linearity is preserved within full differential input range regardless of $V_{\rm tune}$. As $V_{\rm tune}$ is adjusted from 1.58 to 1.2 V, g_m varies from 8 to 131 μS. Fig. 10(b) illustrates that the linear range of the transconductance diminishes as $V_{\rm tune}$ decreases for GD OTA.

The simulated frequency response of the OTA CMRR is shown in Fig. 11, where 1% mismatch and $V_{\rm tune} = 1.4$ V are assumed. 95-dB CMRR is achieved at dc condition and

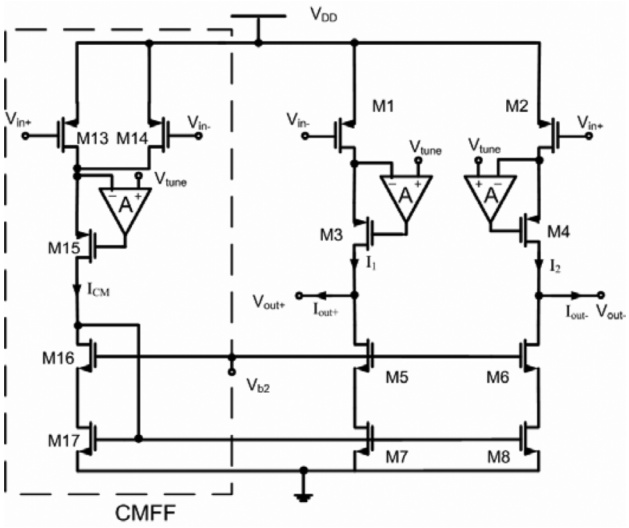

Fig. 9. Schematic of differential GD OTA.

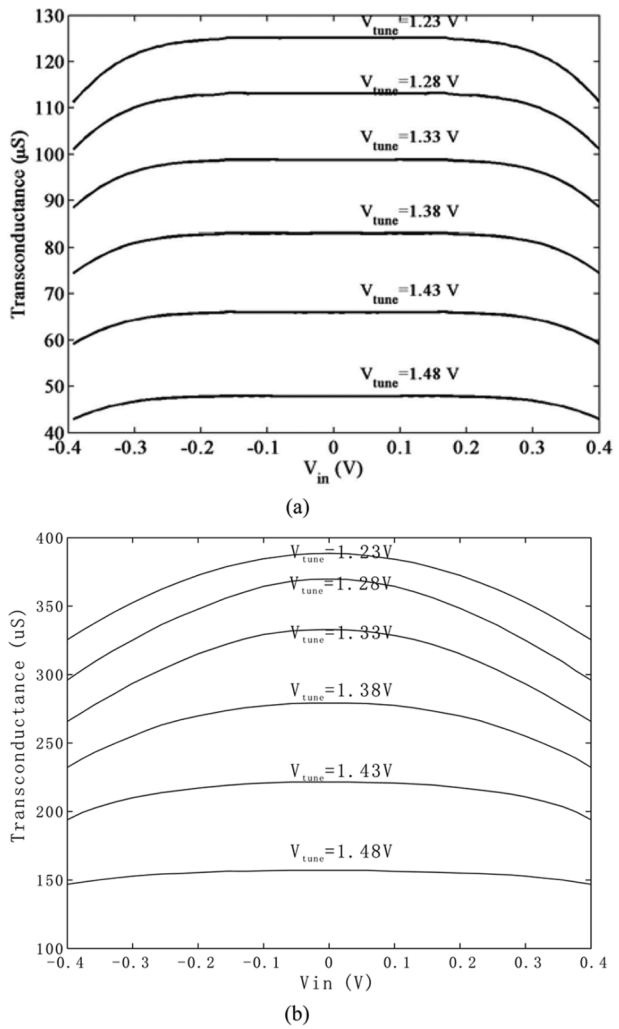

Fig. 10. OTA transconductance versus $V_{\rm in}$ for different $V_{\rm tune}$. (a) BD OTA. (b) GD OTA.

37.8 dB is obtained at unity-gain frequency. At low-frequency, CMRR is largely limited by the mismatch. After the frequency surpasses the OTA dominant pole, differential-mode gain

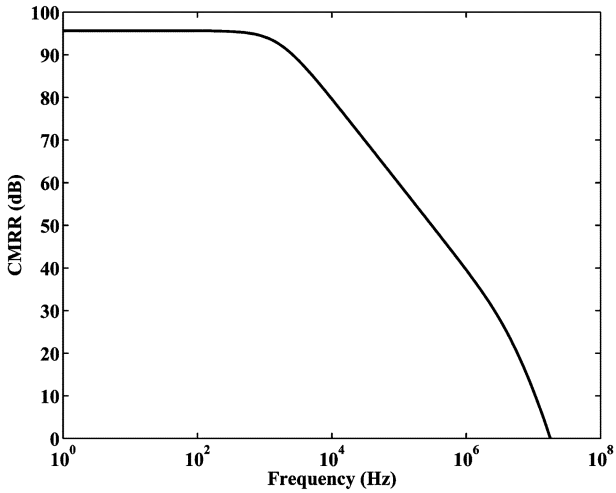

Fig. 11. Frequency response of CMRR for the proposed OTA.

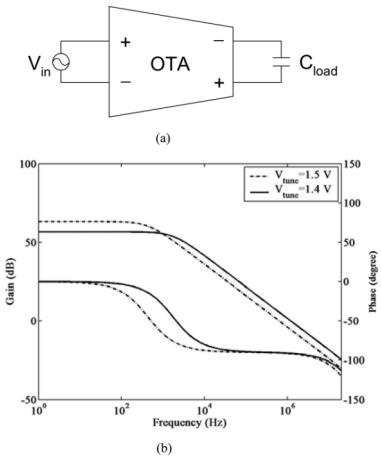

Fig. 12. Frequency response of the $g_m - C$ integrator with $C_{\rm load} = 5$ pF. (a) $g_m - C$ integrator. (b) Frequency response.

decreases, which leads to the roll-off of CMRR. At higher frequency that is above ω_0 ((12)), CMRR magnitude drops faster. With 5-pF load capacitor, the frequency response for different $V_{\rm tune}$ is shown in Fig. 12. When $V_{\rm tune} = 1.4$ V, the integrator has dc gain of 57-dB, unity-gain bandwidth of 1.2 MHz and 1.3° excess phase. When $V_{\rm tune} = 1.5$ V, the dc gain increases to 63 dB and the phase error improves to 0.9°. In this case, unity gain bandwidth becomes 636 K due to smaller transconductance.

Fig. 13 shows the filter tuning within the interval 1.2 V $\leq V_{\rm tune} \leq$ 1.58 V around a rate of 5.65 kHz/mV. When $V_{\rm tune} =$ 1.5 V, $f_p = 1.05$ MHz, $f_s = 1.959$ MHz, $A_{\max} = 0.922$ dB, and $A_{\min} = 34.32$ dB.

For $V_{\rm out} = 800$ $V_{\rm pp}$ and $V_{\rm tune} = 1.5$ V, a THD of -45 dB is achieved. A maximum deviation of 7 mV at filter outputs has been measured over the tuning span. The quiescent dissipation is 4.07 mW@ $V_{\rm tune} = 1.5$ V. The power consumption of individual OTA is 581 uW. The simulated performance of the filter is summarized in Table III. Compared with the triode-based OTA proposed in [7], this work achieves much better linearity for the same input swing range. However, due to smaller g_{mb}, the noise associated with the proposed OTA is relatively higher

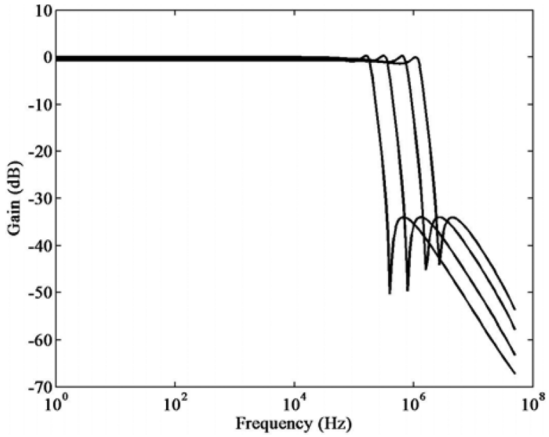

Fig. 13. Filter characteristics for different tuning voltages.

TABLE III
PERFORMANCE OF THE THIRD-ORDER ELLIPTIC LOW-PASS FILTER

Performance	Value	Performance	Value
Cutoff frequency	1.05MHz	Tuning range	462KHz-2.61MHz
V_{CM} variation over tuning	7mV	Maximum signal swing	$0.8V_{pp}$
THD	-45dB @ $800mV_{pp}$	Dynamic range	45dB
Area	$0.159mm^2$	Power dissipation	4.07mW

than [7]. Moreover, similar dynamic range is achieved for both OTAs.

Due to smaller g_{mb}, it should be noted that the proposed OTA has smaller bandwidth than the gate-driven triode-based OTA counterpart.

V. CONCLUSION

We present a 1.8-V BD, triode-mode differential CMOS OTA with CMFF and CMFB in this paper. The BD technique leads to higher linearity as well as higher tuning range and signal swing than the traditional triode-mode OTAs. The CMFB signal is fed into the gate terminals of the BD MOSFETs to adjust the CM output signal. This structure simplifies the overall circuit design and saves power consumption. The detailed circuit structures along with frequency analyses have been presented. Finally, using the proposed OTA, a third-order elliptic low-pass filter features high linearity, wide signal swing and tuning ranges has been implemented.

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