Ultra-Sensitive Capacitive Detection Based on SGMOSFET Compatible With Front-End CMOS Process

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Abstract—**Capacitive measurement of very small displacement of nano-electro-mechanical systems (NEMS) presents some issues that are discussed in this article. It is shown that performance is fairly improved when integrating on a same die the NEMS and CMOS electronics. As an initial step toward full integration, an in-plane suspended gate MOSFET (SGMOSFET) compatible with a front-end CMOS has been developed. The device model, its fabrication, and its experimental measurement are presented. Performance obtained with this device is experimentally compared to the one obtained with a stand-alone NEMS readout circuit, which is used as a reference detection system. The 130 nm CMOS ASIC uses a bridge measurement technique and a high sensitive first stage to minimize the influence of any parasitic capacitances.**

Index Terms—**Capacitance measurement, front-end CMOS co-integration, in-plane suspended-gate MOSFET, lateral SG-MOSFET, nanodisplacement measurement, NEMS devices.**

I. INTRODUCTION

DURING the past twenty years, a continuing series of advances have been realized to merge circuitry, sensors and actuators, entire micro-instrumentation systems on a common silicon substrate. Such micro-electro-mechanical systems (MEMS) device can now be found in our everyday life as their industrialization is meeting more and more the market needs [1]. For example, airbag systems using MEMS accelerometers are now widely used by the automotive industry. Today, with the improvement of microelectronics technologies, it becomes possible to scale down MEMS devices to the nanometer size using standard microelectronic process. With nanomechanical systems (NEMS), a variety of new applications ranging from sensors and actuators to signal processing and communication

can be addressed specifically. Nanofabricated high frequency electromechanical resonators are good candidates for future high-Q resonator for frequency generation and conversion in wireless communication system. NEMS resonators' high operating frequencies, small mass, and high-Q, also make them natural choices for resonant mass and force sensors with unprecedented sensitivities [2]. However, to industrialize the above merging applications, tremendous efforts are still necessary. In particular, it is desirable to fabricate on a same die the nanomechanical structure and the associated electronics for local signal processing, so that the signal-to-noise ratio, the power consumption, the global system compactness, and its assembling facility are improved [3]. A complete integration of a NEMS and its CMOS electronics is presented in [4], [5] and can be considered as pioneer works that go in that direction. In [6], a 10 μm long, 600 nm wide and 750 nm cantilever used as a mass sensor integrated in a CMOS oscillator circuit has achieved a mass resolution of 1ag within a completely portable device. All these research works use a home-made post-CMOS process which makes them difficultly acceptable in an industrial context due to cost purposes. Indeed, the nano-fabrication of the mechanical devices should share as much as possible process steps with a standard CMOS process so that very little or even no additional step processes would be required. Thin SOI [7] and Silicon On Nothing (SON [8]) technologies are good candidates to fabricate at the same time the NEMS structure and the associated electronic. Furthermore, to offer compatibility with a standard CMOS process, a capacitive actuation and detection technique for controlling the nano-mechanical structure and measuring its displacement is preferred to other transducers that use optic, piezoresistive or piezoelectric effects: intrinsically a capacitive detection is noise free, naturally CMOS compatible and highly sensitive with gap reduction.

As a first step toward the co-integration of the NEMS and electronic circuits, this paper focuses on the capacitive detection of nanometer mechanical displacement thanks to a so-called suspended-gate MOS field-effect transistor (SGMOSFET) that is fully compatible with a standard CMOS technology. SG-MOSFET models have been recently reported for out-of-plane [9] and in-plane [10] device geometries. In this work we essentially exploit results validated in [10] and extend the model with a small signal equivalent circuit, useful for circuit design and evaluation of signal detection and noise investigation.

The paper is organized as follows. To clearly state the challenges when measuring small capacitance variation, the paper
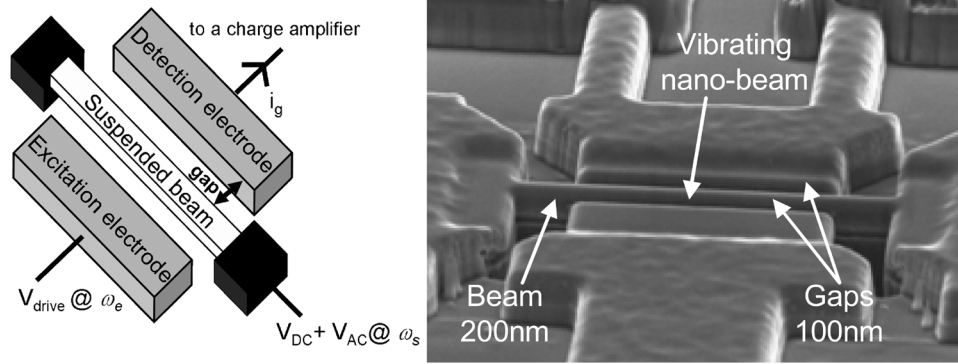
Fig. 1. Clamped-clamped nanobeam.

presents in Section II the issues that must be circumvent to achieve an accurate capacitive measurement. In Section III, a stand-alone circuit to measure capacitive NEMS variation is explained. Some reasonable performance is obtained with this hybrid approach at a cost of power consumption. Finally, Section III describes the proposed SGMOSFET device. Details concerning its working principle and its fabrication are given. Finally, experimental results based on SGMOSFET are discussed and compared to the measurement obtained with the hybrid approach, which serves as reference.

II. CAPACITIVE NEMS DETECTION ISSUES

For a general discussion and for simplicity, we consider throughout the paper the in-plane displacement detection of a clamped-clamped nano-beam under equilibrium (Fig. 1). Issues induced with that structure can be extended to other suspended mechanical structures. The left-side electrode is used to control the beam displacement thanks to electrostatic forces. The right-side electrode serves as a detection electrode. Let us apply a V_{drive} voltage at a given frequency ω_e on the excitation electrode and a V_{DC} voltage on the beam so that the beam moves linearly with V_{drive} by $dx(t) \ll g$ from its initial position.

The capacitance variation $dC(t)$ between the beam and the detection electrode around the NEMS DC capacitance C_0 is roughly expressed as

$$\frac{dC(t)}{dx(t)} = \frac{\varepsilon_0 lh}{g^2} \qquad (1)$$

where g is the air gap, l the beam length, h the beam thickness, ε_0 the air permittivity, and $dC(t) \ll C_0$ to avoid pull-in effect.

In order to measure $dC(t)$, a carrier voltage V_{AC} at frequency ω_s is superposed to the DC voltage applied on the beam so that the current flowing though the detection electrode comes from the mixing of the capacitance variation $dC(t)$ and the V_{AC} voltage. This current modulation can be converted by connecting the detection electrode to a readout device. In the case where a suspended gate MOSFET (see Section IV for its complete description) is used, it results in a voltage modulation V_{OX} at the oxide surface of the MOS channel (which acts as a virtual gate) resulting in a drain current variation I_D. (Fig. 2). When this MOS is loaded, this drain current is converted into an output
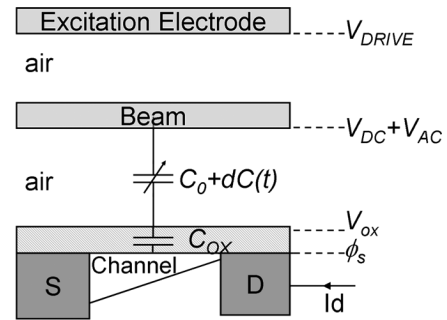

Fig. 2. Capacitive detection model of the lateral SGMOSFET.

voltage. The overall structure works exactly as a transimpedance device. In the case where a stand-alone circuitry is used, the transimpedance function is made thanks to a charge amplifier at a cost of adding some parasitic capacitance C_p due to the layout and in/out pads.

An identical macro-model of the read-out electronic as the one in Fig. 3 can be applied when either a stand-alone circuitry or a suspended gate MOSFET is used. This macro-model focuses only on the detection of $dC(t)$ and the excitation of the beam (i.e. its dynamic) has been voluntary omitted. The total current i_g flowing through the detection electrode is the sum of a background current i_{bg} and a dynamical current i_s. The current i_{bg} which is due to the NEMS DC capacitance C_0 works at the frequency ω_s. The current i_s which is due to the mixing property between $dC(t)$ and V_{AC} works at the frequency $\omega_s - \omega_e$. Considering only the harmonic of interest (i.e. $\omega_s - \omega_e$), the small signal representation of the detection chain in Fig. 4 can be used. The capacitances C_{in}, C_{out} represent respectively the total input capacitance (C_0 NEMS DC capacitance, C_{gs} transimpedance input capacitance and all C_p parasitic capacitance e.g. readout pad capacitance when a stand-alone circuitry is used) and the transimpedance output capacitance. Note that C_{in} is minimal in the case of the suspended gate MOSFET since there is no readout pad connected to the MOS gate. The parameters C_{fb}, g_m and $1/g_{ds}$ represent respectively the equivalent transimpedance feedback capacitance, its transconductance, and its output resistive load. The electronic noise is taken into account through the current source $\overline{i^2_{noise}} = 8k_B T/3 \cdot g_m \cdot \Delta f$. Assuming that the frequency of derivation is smaller than
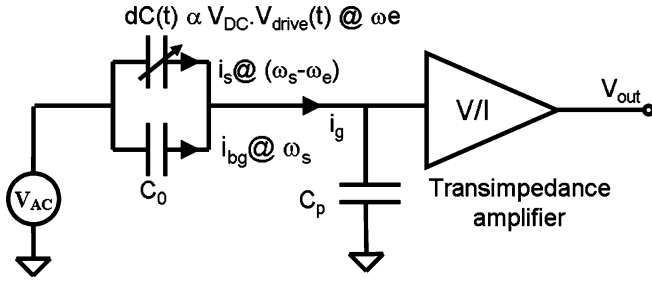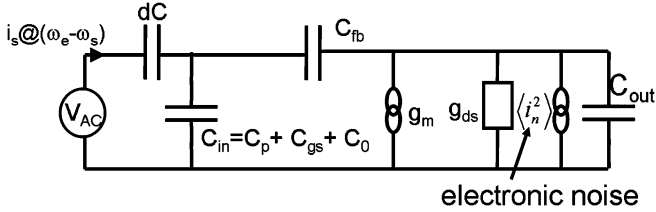
Fig. 3. Capacitive NEMS read-out electronic macro-model.

Fig. 4. Small-signal representation of the read-out electronic at $\omega_s - \omega_e$.

Fig. 5. Noise due to the electronic circuitry.

the bandwidth of the transimpedance amplifier, the equivalent noise capacitance in F/$\sqrt{\text{Hz}}$ is then equal to

$$C_{noise} = \frac{C_{in} + C_{fb}}{V_{AC}} \sqrt{\frac{8k_B T}{3 \cdot g_m}} \qquad (2)$$

where T is the temperature, k_B is the Boltzmann constant, and V_{AC} is the readout measurement voltage.

To minimize the influence of the electronic noise, the total input capacitance should be minimized, and its transconductance maximized. The feedback capacitance C_{fb} should be reduced up to the minimum realizable with the CMOS process and adapted to the transimpedance output dynamic range so that in any case $C_{fb} \ll C_{in}$.

Fig. 5 shows the power spectral density of the equivalent noise expressed in terms of the capacitance to be read where:

- g_m has been swept from few μS (MOS in weak inversion) to few mS (amplifier with several stages of amplification);
- C_{in} has been swept from few fF (a MOS gate capacitance; co-integration of the electronic circuitry and the NEMS, e.g. SGMOSFET device) to few pF (capacitance of a readout pad; stand-alone electronic circuitry).

An additional ambient capacitance noise of 0.2 zF/$\sqrt{\text{Hz}}$ is inserted in the model corresponding to the mechanical noise of the structure. The capacitance measurement performance is optimal in the so-called "co-integration" configuration since the C_{in} capacitance is negligible: noise is better than 1 zF/$\sqrt{\text{Hz}}$. However in the hybrid approach configuration, the noise level (better that 1 aF/$\sqrt{\text{Hz}}$) is still acceptable particularly with high g_m at the cost of more power consumption. Moreover using a very selective measurement bandwidth (long integration time) thanks to a lock-in measurement technique, one can achieve a very accurate absolute measurement.

From previous discussions, it is obvious that the optimal detection system is achieved with a co-integrated electronic circuitry with the NEMS. However, the circuit detection macro-model has demonstrated that some reasonable performance can
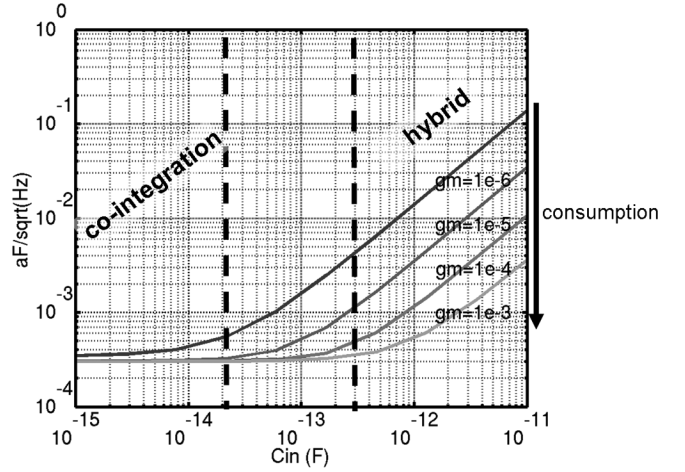
be achieved with a stand alone electronic circuitry at a cost of reducing the measurement bandwidth, and increasing the electronic complexity and/or the consumption to have high g_m. In the next paragraph, an ASIC that takes into account these issues, is presented while with the SGMOSFET device presented in Section IV we go on one step further for integrating the NEMS and its electronic on a same wafer level in order to reduce any parasitic capacitances.

III. A STAND-ALONE ASIC FOR A HYBRID APPROACH

A. ASIC Overall Description

Fig. 6 presents an architecture overview of the designed ASIC that has been fabricated using a 130 nm CMOS technology. The beam displacement is controlled with the $V_{drive}(t)$ signal. The time-varying capacitance $dC(t)$ is measured thanks to the dynamical current flowing through it when a V_{AC} signal is applied on the beam. C_{par} represents the cross-coupling parasitic capacitance due to the NEMS itself and its interconnections. The parasitic capacitance C_{par} might be a several order greater in magnitude than $dC(t)$. It is therefore necessary to reduce dramatically the measurement voltage V_{AC} to avoid the saturation of the low noise amplifier (LNA). In this case, as is demonstrated in the formula (2), this voltage reduction is responsible of a background noise that can be much higher than the signal. To cancel this background noise, a bridge measurement technique is used in the ASIC to cancel the charge due to the C_{par} capacitance. It is achieved thanks to the ASIC internal capacitance C_b and by adjusting the negative gain G so that the bridge equilibrium is reached:

$$V_{AC} \cdot C_{par} = V_{AC} \cdot G \cdot C_b. \qquad (3)$$

Therefore, V_{AC} amplitude can be enhanced to increase the measurement sensitivity.

In the detection chain, the LNA used like a transimpedance amplifer is the key building block since it governs the overall signal-to-noise ratio of the measurement. So a particular attention has to be carried out on this stage to find a trade-off between the transconductance value, the parasitic capacitances,
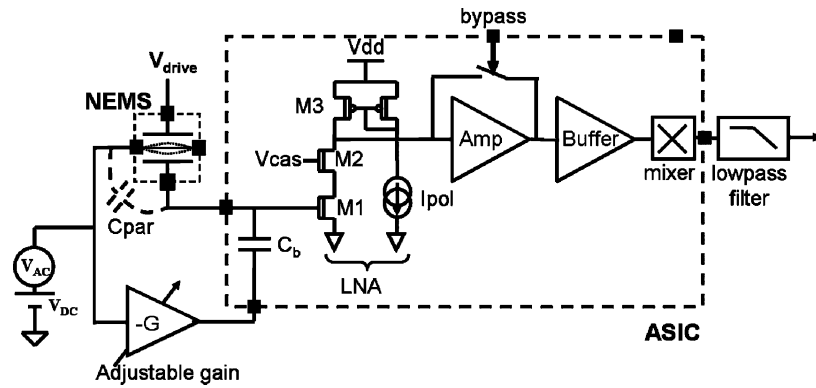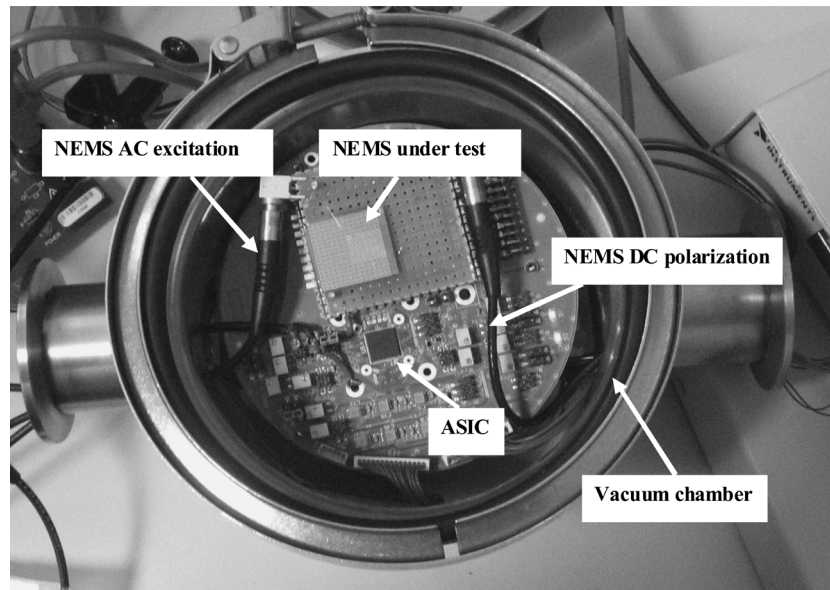
Fig. 6. ASIC schematic overview.

Fig. 7. Photograph of the test bench.

the voltage gain and the output dynamic range. In spite of polarization difficulties, a single-ended structure is preferred to a differential amplifier because with only one input transistor against two in a differential structure the noise could be reduced by a factor $\sqrt{2}$ assuming that the MOS noise in the differential structure is uncorrelated. The design of the LNA is optimized in the following way. The length L of M1 is chosen to the minimum length L_{min} of the CMOS process so that g_{m1} is large enough and the capacitance C_{gs} is minimized. The transconductance of transistor M3 is set as low as possible using a large transistor length in order to reduce its noise contribution and its source-drain conductance. Finally to have a high transimpedance gain so that charges injected in C_{in} are reduced, the LNA voltage gain should be as large as possible. To do so, M1 is cascoded with the transistor M2 to compensate its low source drain conductance due to the fact that the length of M1 is set to L_{min}. The LNA biasing current is set to 100 μA given a 2 mS transconductance with a bandwidth close to 20 MHz with an acceptable output dynamic range. After the LNA, a second amplification stage has been inserted that can be bypassed when enough signal is available at the LNA output. At the end of the chain, a mixer is implemented using sampling switches so that a lock-in tech-

nique can be used to suppress the 1/f noise. Finally, the measurement bandwidth is controlled by the 1 Hz off-chip low-pass filter. Using a very selective measurement bandwidth, i.e. a very selective low pass filter, one can achieve a very accurate absolute measurement with a trade-off on the integration time.

B. Experimental Results

Measurements have been performed on the test bench shown on Fig. 7. A silicon die containing thousands of clamped-clamped beam structures is placed very close to the ASIC. Tests are performed on one of those NEMS. The V_{drive} signal used to control the capacitance variation dC is adjusted externally as well as the V_{AC} signal used to read the capacitance. The NEMS detection electrode is connected to the ASIC input using short wirebonding to limit parasitic capacitance. The capacitance bridge is equilibrated by tuning the negative gain G for a given V_{drive} signal and V_{AC} signal. Fig. 8 shows the noise spectral density at the output of ASIC for different amplitudes of the V_{AC} signal.

Two main sources of noise are clearly identified: the thermo-mechanical noise of the structure and the electronic noise. The output noise is constant whatever the amplitude of V_{AC} is. It
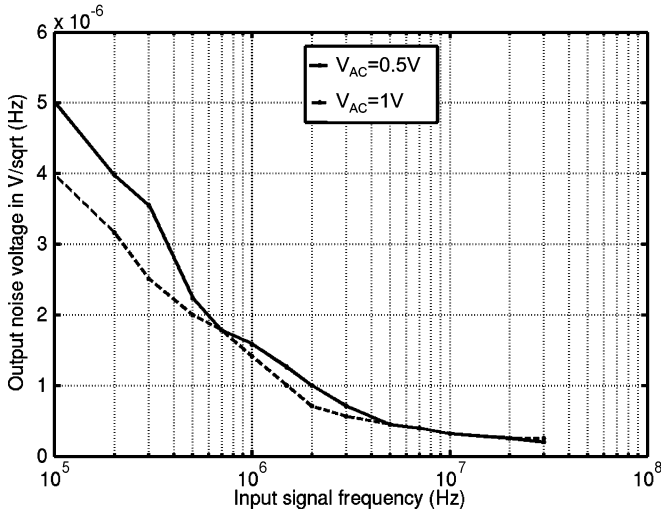
Fig. 8.   ASIC output noise voltage.

Fig. 9.   Equivalent input capacitance noise.

means that the electronic noise is predominant (ASIC and measurement chain). In fact, when increasing the V_{AC} signal, the capacitance measurement becomes more sensitive and one can expect to measure the influence of the mechanical noise which is obviously not the case here. (It was not possible to test with V_{AC} higher than 1 V due to pad ESD protection). To evaluate the absolute capacitance variation dC that the ASIC can measure, the following test protocol was followed:

1) The V_{drive} signal is set to 2 different DC values V_1 and V_2.
2) For each DC value, the bridge is equilibrated and using (3), the overall capacitance Cp can be extracted knowing G and $C_0 = 30$ fF. The capacitance variation dC when V_{drive} changes from V_1 to V_2 can then be computed.
3) The V_{drive} signal is set back at V_1 and the bridge is once again equilibrated. The output noise spectral density P_{noise} can be measured at the vicinity of V_{AC} working frequency. The V_{drive} is then set to V_2 without modifying the bridge electrical configuration and the bridge is therefore not anymore equilibrated. By measuring on a bandwidth Δf the resulting output signal power P_{signal} (corresponding to the capacitance variation dC previously computed), the equivalent capacitance noise can be evaluated:

$$C_{noise} = dC \sqrt{\frac{P_{noise}}{\Delta f \times P_{signal}}}. \qquad (4)$$

This expression assumes that there is a linear conversion between the capacitance variation dC and the corresponding output signal.

Fig. 9 shows the capacitance noise measured according to the previous experimental protocol for different V_{AC} working frequencies and amplitudes. As expected the measurement resolution increases with V_{AC} amplitude. Table I summarizes the ASIC performance. The optimal working frequency is around 2 MHz. Below 500 kHz and above 10 MHz, the measurement resolution decreases due to respectively the electronic 1/f noise and the LNA cut-off frequency. The capacitance resolution achieved is 250 zF/$\sqrt{\text{Hz}}$ with a measured C_{in} capacitance of 4 pF, which, for a 1 kHz measurement bandwidth, gives a SNR of 1 for a dC
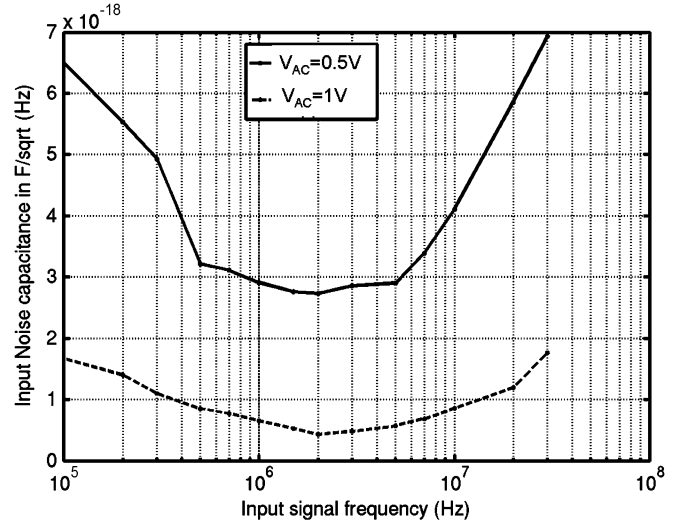
of 7.9 aF. This result is consistent with spice simulation of the ASIC and is better than commercial solutions such as [11] where a 4 aF/$\sqrt{\text{Hz}}$ capacitance resolution is achieved. However, this capacitance resolution can be highly insufficient for very challenging applications.

IV. SGMOSFET

A. Description and Model

As a further step toward the full co-integration of the electronics and the NEMS, a first "co-integration" approach is proposed by associating an in-plane suspended NEMS to a single detection MOS, compatible with a standard front-end CMOS technology. The main advantage of using a front-end NEMS CMOS technology is that there is more latitude in processing the NEMS in terms of materials, temperature, fabrication cost, etc. One can realize NEMS in monocrystal silicon and its electronic sharing the same process than the CMOS technology. Moreover, monocrystal silicon is mechanically (quality factor, residual stress, etc.) and electronically better than polysilicon used in early works with a post-CMOS process. The proposed approach called lateral suspended-gate MOSFET (LSGMOSFET) uses the nanomechanical device as a gate of a lateral MOS transistor. The geometry of the component and the notations are shown in the Fig. 10. Recent works have demonstrated the feasibility of the approach for out-of plane displacement measurement, but they are not yet compatible with front-end CMOS technology [14]. The electro-mechanical structure is made of a beam moving in the wafer plane, and doped areas acting as source and drain of a lateral MOS transistor. The beam itself is used as a movable gate, which controls the charge of the MOS channel. The dielectric between the channel and the gate is the air gap whose size varies with the beam displacement. As the beam moves, the electrical potential used to control the channel varies along the channel. The charge density in the channel is therefore modulated along the channel. When loaded, this electromechanical structure acts as a free capacitance attached to its first amplification stage

TABLE I
PERFORMANCE

|	Hybrid ASIC (130nm bulk technology)	In-plane suspended gate MOSFET (SON technology)
LNA total input capacitance C_{in}	5.3pF (with pad)	<100fF
LNA transconductance gm	gm=2mS	<< 1μS
Capacitance resolution (noise floor)	250zF/√Hz @[500kHz-10MHz]	130zF/√Hz @ 13MHz
Power dissipation	100μA (LNA),100mA (total) 1.2V power supply	275nA with V_{DS}=3V
Silicon area (without pads)	45umx20um without the NEMS	15umx10um with the NEMS
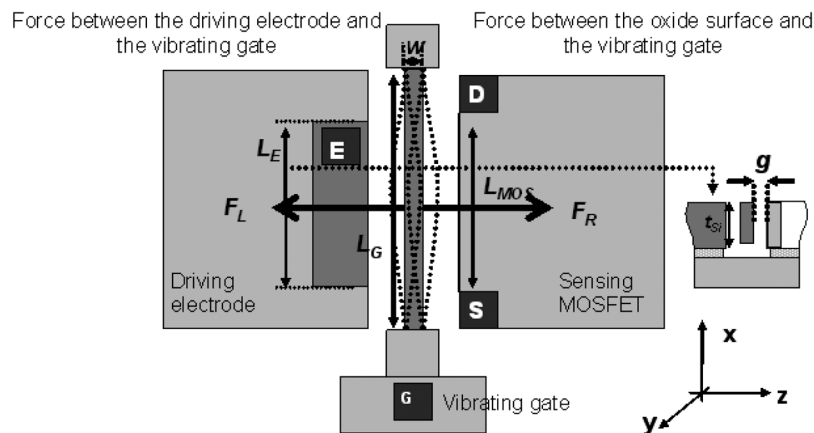
Fig. 10. Schematic of the lateral SGMOSFET. F_L and F_R are the electrostatic forces on each side of the vibrating gate; L_E and L_{MOS} are respectively the electrode length and the channel length; g is the air gap; t_{Si} is the thickness of the top layer; w is the gate width.

except that in this case the C_{in} capacitance has been reduced to its minimal value.

In previous resonant gate MOSFET, the gate moved along the channel width [12]. The drain current was then easily calculated by considering N basic transistors placed in parallel along its width. Here, as the suspended gate moves along the channel length, a new self-consistent electromechanical model is developed. It is based on an explicit formulation of the surface potential to determine all charge densities in the MOSFET. The fringe effect and the mode shape of the beam are included in the computation of the electrostatic forces. More details concerning the device model can be found in [10].

B. Devices Fabrication

Devices were fabricated using the Silicon On Nothing (SON) technology [8] to achieve sub-100 nm gaps and 400 nm thick single crystal silicon resonators using only front-end processes and materials, ensuring in-IC integration capabilities. The fabrication process flow presented in [8] is resumed in Fig. 11. It starts with the patterning of active areas through a thermal SiO_2 layer. A SiGe sacrificial layer is then grown by selective

epitaxy, followed by a low boron doped (10^{16} at/cm^3) non-selective single-crystal silicon epitaxy (Fig. 11(a)). Phosphorous dopants are implanted (10^{19} at/cm^3) to define gate, source and drain. E-beam lithography is used to define gaps and the resonator structure leading to a 47 nm gap resolution (Fig. 11(b)). The 400 nm thick silicon structural layer is then etched by an anisotropic plasma to define air gaps (Fig. 11(c)). After dopants diffusion and activation annealing steps, structures are released by an isotropic plasma etch of the SiGe sacrificial layer (Fig. 11(d)). The released structures were protected by a non-conformal SiO_2 deposition (Fig. 11(e)). Pads are then formed by a NiSi salicidation and aluminium deposition (Fig. 11(f)). Fig. 12 shows a picture of a suspended lateral SGMOSFET.

C. Devices Characterization—Comparison Between Experiment and Theory

Static Regime: Static characterization of the lateral SG-MOSFET is performed using a DC parameter analyser HP 4155A with four DC probes. The aim was to extract the lateral SGMOSFET static characteristics so as to find the operating point for dynamic characterization. Fig. 13(a) and (b) gives
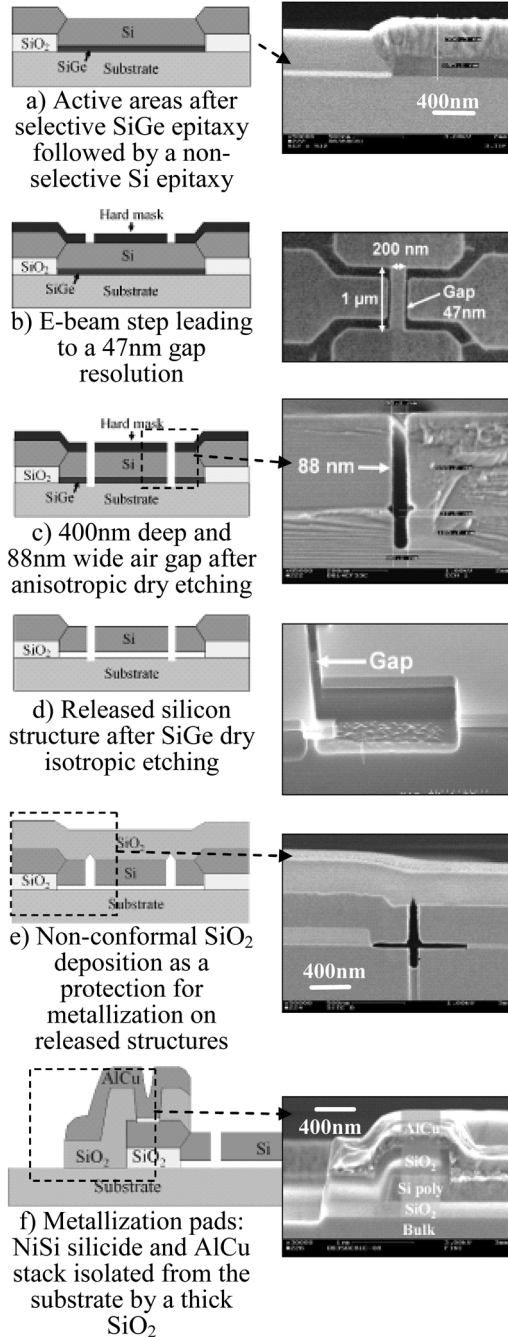
a) Active areas after selective SiGe epitaxy followed by a non-selective Si epitaxy

b) E-beam step leading to a 47nm gap resolution

c) 400nm deep and 88nm wide air gap after anisotropic dry etching

d) Released silicon structure after SiGe dry isotropic etching

e) Non-conformal SiO_2 deposition as a protection for metallization on released structures

f) Metallization pads: NiSi silicide and AlCu stack isolated from the substrate by a thick SiO_2

Fig. 11.   Fabrication process flow and SEM illustrations.

Fig. 12.   Perspective SEM picture of a beam (L = 10 Qm, w = 165 nm, d = 120 nm).

respectively the static characteristics $I_d(V_g)$ and $g_m(V_g)$. The theoretical results are superimposed in each case. Regarding the measurements, the threshold voltage, V_{th}, is 2 V. An off-state leakage current of 0.1 to 1.3 μA depending quasi linearly of V_{ds} is observable at $V_g = 0$ V. It is attributed to a photolithography misalignment when protecting channel from phosphorous implants. Indeed, channel surface was partially implanted on a few nanometers width, generating a 2.1 MΩ short-circuit resistor in parallel of the transistor, explaining the high leakage current and its quasi linearly dependence with V_{ds}. Optimal operating points were defined from static characteristics: V_g being 4.6 V corresponding to the maximum of transconductance, and V_{ds} being 3 V corresponding to saturation region, with an off-state
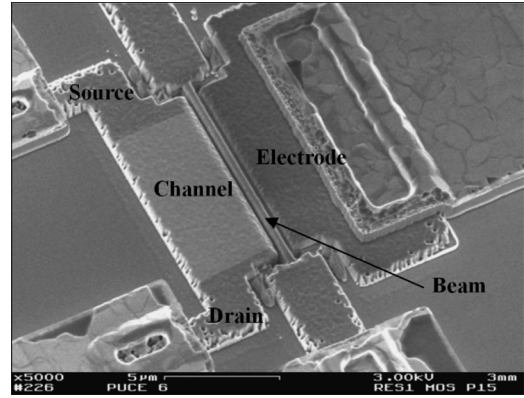
leakage of 1.4 μA. To fit the model with the experimental results, the doping level of the channel N_a, and the charge density at the gate oxide Q_i are respectively fixed at $5.5.10^{15}$ at/cm^3 and 5.10^{10} cm^{-2}. In the Fig. 13(a) theory and measurement are well in agreement. For $V_{ds} = 1.55$ V and $V_{ds} = 2.75$ V, the charge densities at the interface silicon/oxide Q_{ox} are changed from 10^{12} cm^{-2} to 10^{13} cm^{-2}. It means that the charge traps at the surface of the MOSFET channel are gradually filled inducing a threshold voltage variation and a slope variation as well. In the Fig. 13(b), we observe a quite large dispersion of raw data which makes the comparison difficult. Anyway, the computed values are in the good order of magnitude.

Dynamic Regime: RF characterizations are performed using an Agilent 8753E vector network analyser (VNA). Fig. 14 shows the two measurement configurations for comparing capacitive and MOSFET detection on the same device. For a capacitive detection measurement, the transmitted signal through the resonator is measured between the vibrating beam and the electrode of the device. A bias voltage V_{dc} is applied on the electrode; the beam and the substrate being grounded to avoid any pull-in effect of the structure. A more detailed study of the same devices using only capacitive detection was done in [13]. For a MOSFET detection measurement, three bias voltages are applied: the electrode V_{dc}, the gate voltage V_g and the drain voltage V_{ds}. Optimal V_g and V_{ds} values for dynamic characterization were extracted from the static MOSFET characteristics $I_d(V_g)$ and $I_d(V_{ds})$. A more detailed study with MOSFET detection was done in [14]. Fig. 15 compares the resonant amplitude response between capacitive and MOSFET detection, on the same structure ($L = 10$ μm, $w = 165$ nm, $d = 120$ nm). The fundamental resonance frequency was measured to be 14.33 MHz and 14.31 MHz with capacitive and MOS detection respectively. The slight discrepancy between the two measurements is explained by the different bias conditions of actuation between the MOS and the capacitive detection. The frequency shift is mainly due to the MOSFET channel surface potential which is set to zero in the case of the capacitive detection. The MOSFET detection yields a +4.3 dB signal amplification compared to the capacitive detection, due to the MOSFET intrinsic gain.

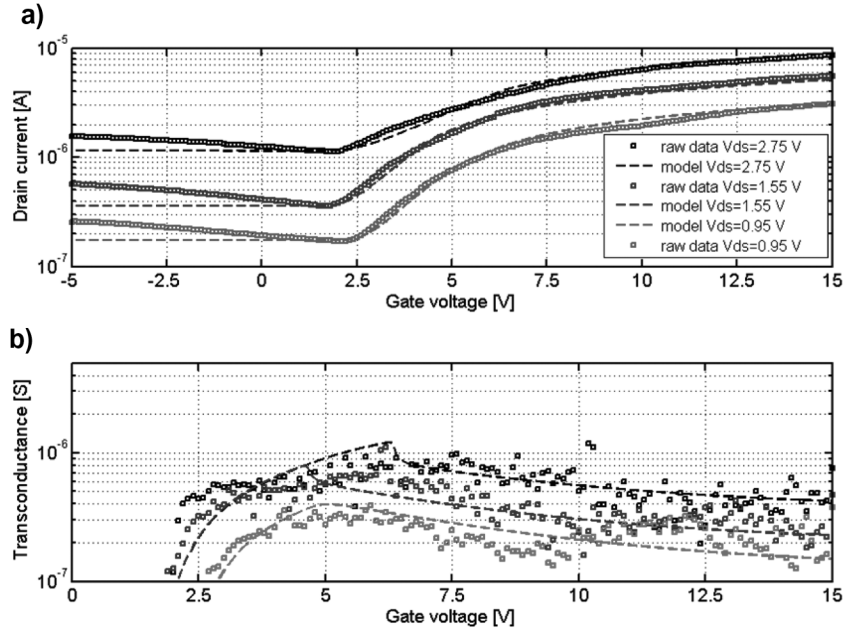More details are available in [13] and [14].

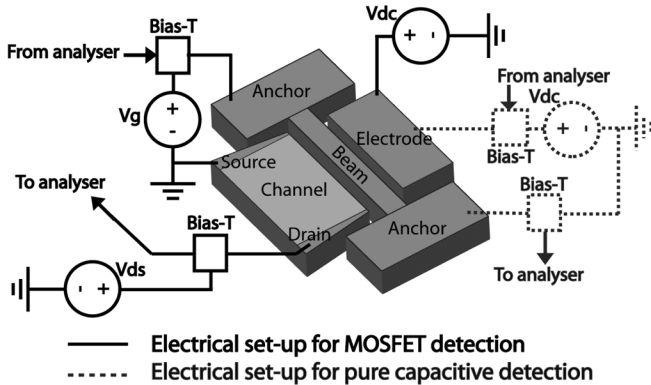Fig. 13. Static MOS characteristics $I_d(V_g)$ and $g_m(V_g)$—Comparison between measurement and theory.

Fig. 14. RSG-MOSFET electrical characterization set-up.

Regarding the lateral SGMOSGET curves, the model is well in agreement with the experiment. The theoretical resonance frequency is quite close to the experimental frequency. The difference between the theoretical level and the measured level is only of 1 dB higher. The background noise is due to the VNA that was determined through an open loop calibration without device (~ 380 pA/$\sqrt{\text{Hz}}$). The theoretical curve for the capacitive transduction is also compared with the measurement results. The agreement is again quite well.

Out of the resonant amplitude response and the associated electromechanical model, the capacitance resolution can be evaluated as follows. From the electro-mechanical model of the lateral SGMOSFET, one can extract at resonance the capacitance variation $dC(f_0)$ according to the power transmitted in the NEMS. Assuming a linear conversion between the capacitance variation and the output signal, it is then possible to estimate the equivalent capacitance noise:

$$C_{noise}(f) = \frac{dC(f_0)}{\sqrt{2}\sqrt{\Delta f}} \sqrt{10^{[S_{12}(f)]_{\text{dB}} - [S_{12}(f_0)]_{\text{dB}}}} \quad (5)$$

where $dC(f_0)/\sqrt{2}$ is the RMS value of the capacitance variation at resonance extracted from the NEMS electromechanical model, Δf is the measurement bandwidth, $S_{21}(f)$ is the transmission gain at frequency f, and $S_{21}(f_0)$ is the transmission gain at resonance. Please note that the capacitance noise resolution extracted takes into account the VNA noise and it is not therefore the pure intrinsic capacitance noise resolution of the lateral SGMOSFET.

D. Observed Improvements With SGMOSFET and Discussion

Measured performance obtained using SGMOSFET is compared in Table I to that obtained with the ASIC and shows improvement in terms of measurement resolution, silicon area and power consumption. However, the robustness of the device is not so good. The reason might be a poor control at the bulk potential because the body of the MOSFET was kept floating. Other reasons could be a strong surface density of charge traps and a strong roughness of the lateral interface silicon/oxide. That may induce a large instability of the measurements according to the device and the surrounding. Next generation of component is in progress to improve the field effect (improvement of gate oxide and of silicon/oxide interface) and the responsivity to the beam movement. The gap and the channel length are scaled down. A bulk pad is added to avoid any body effect. Future works will be also focused on reliability issues such as fatigue [15] packaging and in-IC integration for industrial perspectives.

V. CONCLUSION AND PERSPECTIVES

This paper has presented a first nano-electromechanical structure that is compatible with a standard CMOS process. Advantages of this compact device are considerable and have been compared to a stand-alone circuit. Power consumption, silicon area, capacitance measurement resolution are improved. This is mainly due to the fact that parasitic capacitances are
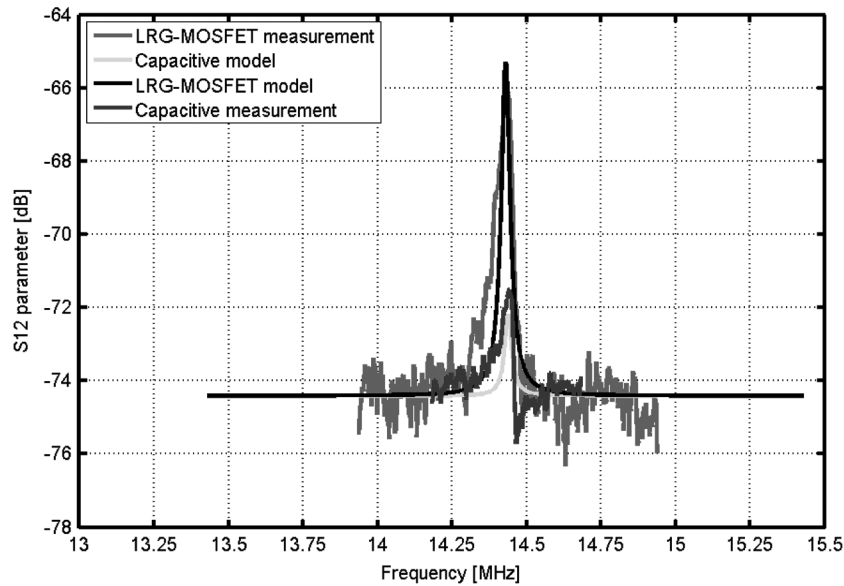
Fig. 15. Capacitive and MOSFET detection comparison on the dynamic response of the NEMS ($L = 10 \ Q\mathrm{m}$, $w = 165$ nm, $d = 120$ nm).

drastically reduced. Today, efforts are on the way to go beyond such simple electromechanical structure so that we can offer a complete monolithic CMOS-NEMS technology. Overall, the paper suggests that the integration of SGMOSFETs in MOS front-end can enable the realization of more sophisticated system-on-chip architectures, including NEMS-based oscillators, low power switches and sensors.

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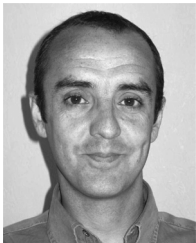
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