Low-voltage LDO Compensation Strategy based on Current Amplifiers

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***Abstract*—In this communication, we propose a Miller compensation technique for low voltage LDO regulators which makes use of a current amplifier. The analysis shows how to design the compensation network when no voltage buffer is placed between the LDO error amplifier and power device and suggests a low supply voltage circuit topology that allows to compensate with a reasonably low integrated capacitance, to avoid oscillations due to the complex-conjugate poles at high output currents and to obtain acceptable under/overshoots during fast transient load variations. The designed LDO regulator can work with a supply voltage down to 1.2 V with a drop-out voltage of 200 mV at maximum load current of 100 mA; the integrated compensation capacitance is 25 pF, the load capacitor being equal to 1 μF. Simulations in good agreement with the theoretical results are also shown.**

I. Introduction

In recent years low-dropout voltage regulators (LDOs) have been widely used in battery-powered portable equipment where power management is essential. Linear regulators are based on a feedback topology (made up of a voltage reference, an error amplifier and a power device) which requires frequency compensation to achieve closed-loop stability. Although conceptually similar to two- (or multi-) stage amplifiers, they are harder to be compensated because of the wider output current range, which causes poles to vary, and the large values of involved capacitances. The requirements of low drop-out and low quiescent current lead to commonly use a PMOS as power device, which makes compensation even more critical.

Dominant-pole frequency compensation achieves stability by means of a zero due to the output capacitor equivalent series resistance (ESR) [1], [2]. Besides requiring a big external capacitor, this compensation technique is critical since stability relies on the ESR value, which changes both with temperature and frequency. On the other hand, Miller-based compensation techniques present the drawback of requiring very large on-chip capacitors. For this reason, the scientific community has been investigating on the feasibility of a current buffer approach in the compensation network [3]–[8]. The solutions proposed in [6], [7] and [8] are stable for load capacitor values within $100\,\mathrm{pF}$ or $1\,\mathrm{nF}$ and are suitable just for SoC applications. The compensation strategies presented in [3]–[5] require output capacitors in the μF range and integrate capacitors of some pF to guarantee stability at load currents ranging some orders of magnitude (from some to some hundreds mA). They all make use of a voltage buffer (typically a source-follower) between the error amplifier and the power device. Besides increasing speed, it helps stability by decoupling the high EA output resistance from the high capacitance at the power MOS gate. Unfortunately, a voltage buffer decreases the power device gate swing of a V_{GS} with respect to the maximum allowable by the supply voltage. Such a structure cannot thus be used in low voltage applications.

The proposed LDO uses a simple class AB error amplifier (EA) to directly drive the power device in order to work down to $1.2\,\mathrm{V}$ supply voltage. Compensation is achieved by means of a capacitor whose effect is magnified by a current amplifier. A very high current gain is obtained with 2 multiplying stages, one of which is shared with the EA. Note that the use of a current amplification in the EA and the choice of class AB topology are due to the large capacitive load of the EA. Furthermore, attention is focused on the current buffer input impedance, which has been properly increased to smooth the peak in the frequency response due to the complex-conjugate poles at high load currents.

The basic structure of the proposed LDO is explained in section II. Theoretical analysis is conducted in section III. Section IV and V show, respectively, the proposed LDO circuit implementation and the simulation results. Conclusions are given in section VI.

II. The Proposed LDO Structure

The schematic of the proposed LDO is shown in Fig. 1. The error amplifier is a multi-mirror class AB OTA. The adaptive biasing, represented by the variable current source I_{AB}, helps the transient response at load variations while keeping the DC consumption low. The transconductance of the error amplifier is $G_{m_1} = B_2 G_{m_{\mathrm{diff}}}$, where $G_{m_{\mathrm{diff}}}$ is the transconctance of the differential pair transistors. The compensation network consists of capacitor C_{C} and a current buffer/amplifier of input impedance $R_{in_{\mathrm{B}}}$ and current gain B_1. However, the overall current gain is $B = B_1 B_2$ since the signal flowing through C_{C} is further amplified by a factor B_2 while passing through the EA. A high value of G_{m_1} is desirable to increase speed but it is critical for stability, as it will be shown in equation (9). Nevertheless, increasing G_{m_1} by means of B_2 allows to amplify compensation at the same time. I_{NL} allows to maintain regulation also at no load.

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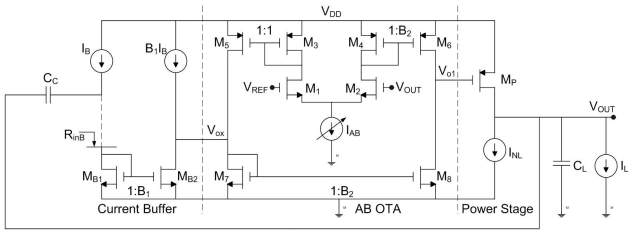

Fig. 1. Low voltage LDO with current amplifier Miller compensation: basic structure.

III. Stability Analysis

The open-loop transfer function of the described LDO may be analyzed through the small-signal circuit depicted in Fig. 2. Elements C_{in}, G_{m_1}, R_{o_1} and C_{o_1} model the error amplifier and its equivalent output load. C_{o_1} is mainly due to the gate-source and gate-bulk capacitances of the power MOS while its gate-drain capacitance is referred as $C_{\rm gd}$. Elements G_{m_2}, R_{o_2} and $C_{\rm L}$ model the power stage and the overall output load. G_{m_2}, R_{o_2}, C_{o_1} and $C_{\rm gd}$ depend on the load current $I_{\rm L}$; particularly, G_{m_2} changes within several orders of magnitude. Normally, LDOs are designed to work with output currents in a specified range: it is important to have high phase margin at all the operating loading conditions ($I_{\rm L}^{\rm min} < I_{\rm L} < I_{\rm L}^{\rm max}$) and at no load ($I_{\rm L} \approx 0$), which may represent the stand-by condition of the loading circuits. We will thus conduct our analysis for $G_{m_2}^{\rm min} < G_{m_2} < G_{m_2}^{\rm max}$ and we will then consider the case of no load ($I_{\rm L} = I_{\rm NL}$). The current buffer/amplifier is represented by its input resistance $R_{in_{\rm B}}$ and the current-controlled current source $Bi_{\rm B}$. It is worth noting that capacitors $C_{\rm gd}$ and $C_{\rm C}$ with the current amplifier perform an internal loop inside the overall open-loop gain. This internal loop is responsible for the two complex-conjugate poles mentioned in section I and must be properly compensated.

Using the SapWin symbolic circuit simulator [9], we obtain the complete transfer function of the circuit in Fig. 2 which takes the form

$$T(s) = T(0)\frac{\left(1-\frac{s}{z_{\rm LHP}}\right)\left(1-\frac{s}{z_{\rm RHP}}\right)}{1+a_1 s+a_2 s^2+a_3 s^3} \tag{1}$$

where

$$T(0) = G_{m_1}R_{o_1}G_{m_2}R_{o_2} \tag{2a}$$
$$z_{\rm LHP} = -1/R_{in_{\rm B}}C_{\rm C} \tag{2b}$$
$$z_{\rm RHP} = G_{m_2}/C_{\rm gd} \tag{2c}$$
$$a_1 \approx [G_{m_2}R_{o_1}(BC_{\rm C}+C_{\rm gd})+C_{\rm L}]R_{o_2} \tag{2d}$$
$$a_2 \approx R_{o_1}R_{o_2}C_{\rm L}(C_{\rm gd}+C_{\rm o1})+ +C_{\rm C}R_{in_{\rm B}}\left(C_{\rm gd}G_{m_2}R_{o_1}R_{o_2}+C_{\rm L}R_{o_2}\right) \approx \approx R_{o_1}R_{o_2}C_{\rm L}(C_{\rm gd}+C_{o_1}) \tag{2e}$$
$$a_3 \approx R_{o_1}R_{o_2}R_{in_{\rm B}}C_{\rm L}C_{\rm C}(C_{\rm gd}+C_{o_1}) \tag{2f}$$

If $T(s)$ has a dominant pole, we may simplify (1) into

$$T(s) \approx T(0)\frac{\left(1-\frac{s}{z_{\rm LHP}}\right)\left(1-\frac{s}{z_{\rm RHP}}\right)}{\left(1-\frac{s}{p_D}\right)\left(1+\frac{s}{\omega_{GBW_{\rm int}}}+\frac{s^2}{\omega_{GBW_{\rm int}}^2 K_{\rm I}}\right)} \tag{3}$$

where

$$p_D \approx -1/a_1 \tag{4a}$$
$$\omega_{GBW_{\rm int}} \approx a_1/a_2 \tag{4b}$$
$$K_{\rm I} \approx \frac{a_2^2}{a_1 a_3} \tag{4c}$$

If the internal loop can be described by an open-loop transfer function having a dc gain, $T_{\rm int}(0)$, a dominant pole, $p_{D_{\rm int}}$, and a second pole, $p_{2_{\rm int}}$, the term $\omega_{GBW_{\rm int}}$ represents the gain-bandwidth product of the internal loop (i.e., $\omega_{GBW_{\rm int}} = T_{\rm int}(0)p_{D_{\rm int}}$). Similarly, the term $K_{\rm I}$ represents the ratio between the second pole and the gain-bandwidth product of the internal loop (i.e., $K_{\rm I} = p_{2_{\rm int}}/\omega_{GBW_{\rm int}}$) [10], [11]. If $K_{\rm I} \approx 1$, the internal loop is stable with a phase margin of about 52° and a small peak is present in the frequency domain. If $K_{\rm I} \approx 2$ the phase margin is about 65° and the frequency response is maximally flat. Finally, for $K_{\rm I} > 4$ the non-dominant poles of $T(s)$ become real.

Under the assumption that the internal loop is stable, the stability of the external loop depends on the ratio between the equivalent second pole of the external loop, $p_{2_{\rm ext}}$, and the overall gain-bandwidth product, $\omega_{GBW} = T(0)|p_D|$. The equivalent second pole depends on the closed loop transfer function of the internal loop and is approximately equal to $\omega_{GBW_{\rm int}}$. Consequently, we may define

$$K_{\rm E} = \frac{p_{2_{\rm ext}}}{\omega_{GBW}} \approx \frac{\omega_{GBW_{\rm int}}}{\omega_{GBW}} = \frac{a_1^2}{a_2 T(0)} \tag{5}$$

If the phase contributions of the two zeroes in (1) are negligible, the stability of the overall amplifier is guaranteed if $K_{\rm I} \geq 1$ and $K_{\rm E} \geq 1$.

In general, a convenient choice is setting $K_{\rm I} = K_{\rm E} = 2$ so to obtain a maximally flat response in the closed-loop gain (i.e., no peak due to complex-conjugate poles [10], [11]). However, in LDO regulators, both $K_{\rm I}$ and $K_{\rm E}$ change over a wide range due to the variation of G_{m_2}. In such a situation, it is difficult to guarantee the stability at every value of load current and a detailed analysis of both $K_{\rm I}$ and $K_{\rm E}$ as a function of G_{m_2} (i.e., of $I_{\rm L}$) is required.

A. External loop stability

Substituting (2) into (5) and equating

$$\frac{\partial K_{\rm E}}{\partial G_{m_2}} = 0 \tag{6}$$

we find that $K_{\rm E}$ has a minimum for

$$G_{m_2}^{(\rm K_E)} \approx \frac{C_{\rm L}}{R_{o_1}(BC_{\rm C}+C_{\rm gd})} \tag{7}$$

In order to obtain a high phase margin at all the loading conditions, we should impose $K_{\rm E}^{\rm min}$ equal to a target value

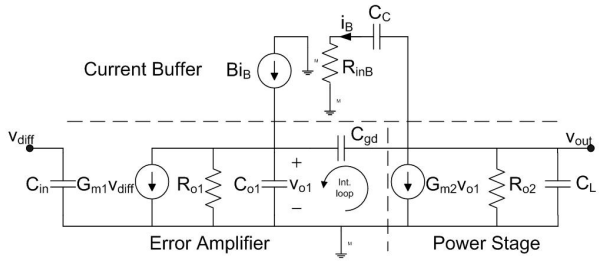

Fig. 2. Small-signal schematic of LDO with current amplifier Miller compensation.

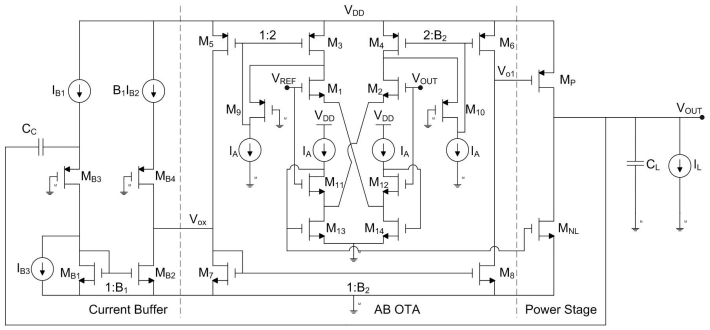

Fig. 3. Low voltage LDO with current amplifier Miller compensation: circuit implementation.

$K_{\rm ET}$ (e.g., in a pure 2 poles system, $K_{\rm ET} = 2$ leads to a phase margin of about $65°$), as in [5]. However, since for typical values $G_{m_2}^{(\rm K_E)} \ll G_{m_2}^{\min}$,

$$\frac{\partial K_{\rm E}}{\partial G_{m_2}} > 0 \qquad \forall G_{m_2} > G_{m_2}^{\min} \tag{8}$$

Therefore, it is sufficient to impose $K_{\rm E}(G_{m_2}^{\min})$ at least equal to the chosen value $K_{\rm ET}$. This constraint leads to a condition for the equivalent compensation capacitor $BC_{\rm C}$

$$BC_{\rm C} > \frac{\sqrt{K_{\rm ET} G_{m_1} G_{m_2}^{\min} R_{o_1}^2 (C_{o_1} + C_{\rm gd}) C_{\rm L}} - C_{\rm L}}{G_{m_2}^{\min} R_{o_1}} - C_{\rm gd} \tag{9}$$

From (9), it is clear that a high current gain B is especially important when the capacitance at the error amplifier output node is high.

Since $K_{\rm E} > 0$ for $I_{\rm L} \approx 0$, current $I_{\rm NL}$ must be chosen small enough so to guarantee adequate phase margin also at no load.

B. Internal loop stability

Substituting (2) into (4c), it is easy to show that

$$\frac{\partial K_{\rm I}}{\partial G_{m_2}} < 0 \qquad \forall G_{m_2} > 0 \tag{10}$$

which means that the minimum value of $K_{\rm I}$ is obtained for the maximum transconductance, $G_{m_2}^{\max}$, that is

$$K_{\rm I}^{\min} = K_{\rm I}|_{G_{m_2}^{\max}} \tag{11}$$

If we impose $K_{\rm I}^{\min}$ at least equal to a target value $K_{\rm IT}$, we stabilize the internal loop of our circuit for any value of G_{m_2}. In order to meet this condition, the input resistance of the current buffer must verify the following relationship

$$R_{in_{\rm B}} < \frac{R_{o_1} C_{\rm L} (C_{o_1} + C_{\rm gd})}{K_{\rm IT} C_{\rm C} (G_{m_2}^{\max} R_{o_1} (BC_{\rm C} + C_{\rm gd}) + C_{\rm L})} \tag{12}$$

where the values of $C_{\rm C}$ and B have been chosen according to (9). It is clear that the more $C_{\rm C}$ and B are high, the more constraint (12) is strict; however, a high current gain B helps relaxing it.

IV. LDO Design

The circuit implementation of the proposed LDO is shown in Fig. 3. The regulator has been designed in a standard 0.35-µm CMOS technology ($V_{T_{\rm n}} \approx 0.55\,{\rm V}$, $V_{T_{\rm p}} \approx 0.65\,{\rm V}$, $k_{\rm n} \approx 175\,\mu{\rm A/V^2}$, $k_{\rm p} \approx 60\,\mu{\rm A/V^2}$) to work with a load current ranging from $1\,{\rm mA}$ to $100\,{\rm mA}$ with a minimum drop-out voltage of $200\,{\rm mV}$. The load capacitor has been set to $1\mu{\rm F}$. Since the buffer configuration represents the most critical condition for stability, we have assumed a regulated output voltage equal to the reference voltage of $1\,{\rm V}$. The minimum power supply has been set to $1.2\,{\rm V}$. In order to improve the transient response, a class AB error amplifier has been used [12]: at steady state, the differential pair bias current is forced to be equal to $I_{\rm A}$ while it increases with the differential signal. This adaptive biasing also doubles the EA small signal transconductance. From the mirror factors shown in Fig. 3 results that the overall first stage transconductance is $G_{m_1} = 2G_{m_{\rm diff}}(B_2/2) = B_2 G_{m_{\rm diff}}$. Transistors M_9 and M_{10} have been added to avoid M_1 and M_2 entering the triode region, being the reference voltage equal to $1\,{\rm V}$. Bias current $I_{\rm A}$ and current gain B_2 have been set, respectively, to $1\,\mu{\rm A}$ and 5, leading to $G_{m_{\rm diff}} \approx 25\,\mu{\rm A/V}$ and $G_{m_1} \approx 125\,\mu{\rm A/V}$. In compliance with the considerations made in section I and the results found in section III-A, a high overall gain of the current amplifier ($B = 25$) has been obtained by means of two cascaded multiplying stages ($B_1 = B_2 = 5$). Imposing $K_{\rm ET} = 2$, the value of capacitor $C_{\rm C}$ has been chosen equal to $25\,{\rm pF}$, according to (9). Imposing $K_{\rm IT} = 1$, from (12), would lead to $R_{in_{\rm B}} \approx 7.5k\Omega$. Note that we used the common gate stage $M_{\rm B3}$ (driven by $I_{\rm B1}$) with the current source $I_{\rm B3}$ ($I_{\rm B3} = I_{\rm B1} - I_{\rm B2}$) in order to lower the input resistance of the current buffer without increasing the DC current of $M_{\rm B2}$ at the same time. Currents $I_{\rm B1}$ and $I_{\rm B2}$ have been set, respectively, to $6\,\mu{\rm A}$ and $1\,\mu{\rm A}$, leading to $R_{in_{\rm B}} \approx 8k\Omega$. $I_{\rm NL}$ has been chosen equal to $2\,\mu{\rm A/V}$ to obtain a phase margin of about $60°$ at no load.

It is worth noting that the regulator is stable also in the non-operating load current range (i.e. $0 < I_{\rm L} < 1mA$), although with a lower phase margin. The minimum phase margin is about $36°$.

TABLE I
LDO TRANSISTORS ASPECT RATIOS.

Transistors	Aspect Ratios
M_1, M_2, M_{11}, M_{12}	9.6/0.6
M_{13}, M_{14}, $M_{\rm NL}$	4.8/0.6
M_3, M_4	24/1
M_5, M_7, $M_{\rm B1}$,	12/1
M_6, M_8, $M_{\rm B2}$, $M_{\rm B3}$	60/1
$M_{\rm B4}$	72/1
$M_{\rm P}$	40000/0.6

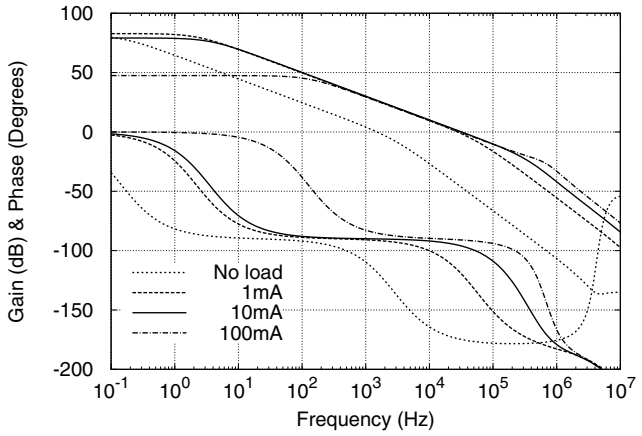

Fig. 4. Bode plots of the LDO open loop transfer function in buffer configuration and at minimum power supply ($V_{\rm DD} = 1.2\,{\rm V}$, $V_{\rm OUT} = V_{\rm REF} = 1\,{\rm V}$) for different values of $I_{\rm L}$.

Transistor aspect ratios are reported in Table I.

V. CIRCUIT SIMULATIONS

The circuit has been simulated in Cadence environment using Spectre simulator. Fig. 4 shows the Bode plots of the LDO open loop transfer function at minimum power supply ($V_{\rm DD} = 1.2\,{\rm V}$) for different output current values (drop-out condition at $I_{\rm L} = 100\,{\rm mA}$, $V_{\rm drop-out} = 200\,{\rm mV}$). Phase margin is about 60° both at minimum operating load current and at no load. The difference with the target value of section III-A (65°) may be due to the fact that high frequency poles have been neglected.

Fig. 5 displays the transient response of the output voltage for load current stepping from $1\,{\rm mA}$ to $100\,{\rm mA}$ (at time $t = 10\,\mu{\rm s}$) and vice versa (at time $t = 50\,\mu{\rm s}$). Dotted line refers to $V_{\rm DD} = 1.2\,{\rm V}$ (drop-out condition), while solid line refers to $V_{\rm DD} = 1.5\,{\rm V}$, which represents a more critical condition for stability since the power MOS works in full saturation region. Note that no oscillations are present even in this case. The rise/fall time of the current step is $1\,\mu{\rm s}$. The undershoots and overshoots are less than 5% and 7%, respectively.

VI. CONCLUSIONS

In this paper, we have analyzed an approach for compensating low voltage LDO regulators which exploits a current amplifier to effectively multiply the Miller capacitor. The proposed procedure takes into account the stability of both internal and external loops to achieve proper compensation for a wide range of loading conditions. A suitable circuit topology has been proposed that allows working at low supply voltages. Extensive simulations validated the analysis proving stability at all the operating output current and at no load and showed a good transient response.

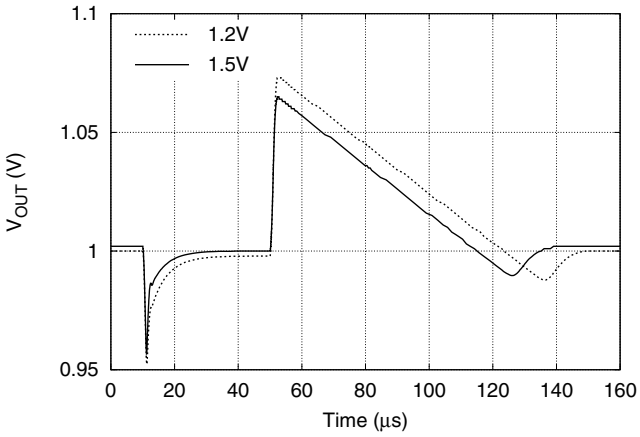

Fig. 5. $V_{\rm OUT}$ transient response for $I_{\rm L}$ going from $1\,{\rm mA}$ to $100\,{\rm mA}$ and back to $1\,{\rm mA}$ at different supply voltages.

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