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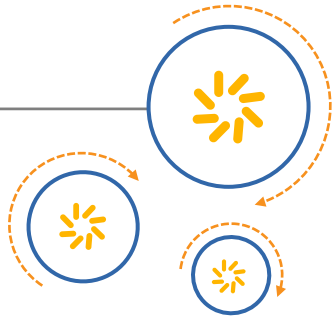

PMI8952 Power Management IC

Device Specification

80-NT391-1 Rev. H

May 27, 2016

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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Revision history

Revision	Date	Description
A	November 2014	Initial release
B	April 2015	■ Table 1-1 Primary PMI8952 device documentation: Updated reference document information ■ Section 1.2 PMI8952 introduction: Added PM8956 as a companion device along with PM8956 for PMI8952 ■ Figure 1-1 High-level PMI8952 functional block diagram: Removed MUIC signals ■ Table 1-2 Summary of PMI8952 features: Made multiple updates to the entire table ■ Table 1-3 Terms and acronyms: Updated the ERM definition ■ Figure 2-1 PMI8952 pin assignments (top view): Updated pads 24, 94, 95, 96, 98, and 135 ■ Table 2-2 Pad descriptions – input power management functions: Updated pad names for pads 94, 95, 96, 98, and 135 ■ Table 2-3 Pad descriptions – general housekeeping functions: Updated the functional description for pad 50 ■ Table 2-5 Pad descriptions – IC-level interface functions: Made multiple updates to pads 134, 69, 55, 103, and 68 ■ Table 2-6 Pad descriptions – configurable input/output functions: Updated the pad name/configurable function information for pads 34 and 75 ■ Section 4.1 Part marking: Added TBD DnD links ■ The following content is included in this document for the first time: □ Chapter 3 Electrical specifications □ Section 4.2 Part marking, Section 4.3 Device ordering information, Section 4.4 Device moisture-sensitivity level, and Section 4.5 Thermal characteristics □ Chapter 5 Carrier, storage, & handling Information □ Chapter 6 PCB mounting guidelines □ Chapter 7 Part reliability

Revision	Date	Description
C	August 2015	■ Updated references to Qualcomm CreatePoint website ■ Table 1-2, Summary of PMI8952 features: Fixed typo ■ Table 3-2, Operating conditions: Updated thermal conditions and added a new footnote regarding junction temperature ■ Table 3-3, DC power supply currents: Updated IDD_ACTIVE, IDD_OFF and footnotes ■ Figure 3-1, Input power management functional block diagram: Updated figure ■ Figure 3-2, USB_IN charging efficiency plot, measured on PMI8952 v2.0: Updated with v2.0 data ■ Added: □ Figure 3-3, USB_IN charging power dissipation plot, measured on PMI8952 v2.0 □ Figure 3-4, Typical SOC accuracy (charging) □ Figure 3-5, Typical SOC accuracy (discharging) ■ Table 3-5, Battery charger specifications: Updated absolute input current specification, clarified fast charge current accuracy comments, updated peak efficiency numbers, added Power Dissipation specification, fixed typo regard VCHG, updated automatic shutdown threshold, updated D+/- specifications, updated ideal diode regulation specification, updated pre-charge current specification, updated SYSOK Rpull specification, and updated SYSOK low battery detection threshold accuracy specification ■ Table 3-6, Fuel gauge performance specifications: Completely revised, updated BATT_ID and BATT_THERM specifications ■ Table 3-12, Internal voltage regulator connections: Removed GPIOs from supported circuits for VPH_PWR voltage supply ■ Table 3-14, Display plus bias performance specifications: Updated load and line regulation, total output voltage variation, switching frequency, and soft start time specifications ■ Table 3-17, WLED boost converter and driver performance specifications: Updated line transient specification ■ Table 3-20, Multipurpose pin performance specifications: Updated footnotes ■ Table 4-2, Device identification code/ordering information details: Updated to include ES2/CS part marking information ■ Section 7.1, Reliability qualifications summary: Added reliability data in Table 7-1, Section A: Silicon reliability results and Table 7-2, Section B: Package reliability results
D	September 2015	■ Table 1-2 Summary of PMI8952 features: Updated capability of MPPs ■ Table 3-17 WLED boost converter and driver performance specifications: Updated Output voltage range of WLED Boost converter in AMOLED mode ■ Section 3.9.2 MPP specifications: Updated description about Odd and Even MPPs
E	October 2015	■ Table 1-2 Summary of PMI8952 features: Updated to add Qualcomm Quick Charge 3.0 support. ■ Table 3-5 Battery charger specifications: Updated VCHG analog output specification ■ Table 3-16 Flash and torch LED driver performance specifications: Updated voltage source for VDD_FLASH and VDD_TORCH ■ Table 4-1 PMI8952 device marking line definitions and Section 7.2 Qualification sample descriptions: Added the country names to the assembly site information.

Revision	Date	Description
F	December 2015	■ Table 2-2 Pad descriptions – input power management functions: Updated pad type for Pad # 123 to AI, AOI ■ Table 3-11 Voltage reference performance specifications: Updated typical value for nominal internal VREF to 1.25 ■ Table 3-18 UVLO performance specifications: Updated typical values for UVLO rising/falling threshold ■ Table 4-1 PMI8952 device marking line definitions: New assembly site added
G	March 2016	■ Table 1-2 Summary of PMI8952 features: Corrected typo by removing 'USB_ID' as it is not measured by FG ADC ■ Table 2-2 Pad descriptions – input power management functions: Updated functional description for Pad #80 - USB_ID ■ Table 4-1 PMI8952 device marking line definitions and Section 7.2 Qualification sample descriptions: Added SMIC as the fab source ■ Table 4-2 Device identification code/ordering information details: Updated source configuration code to 1 ■ Table 4-3 Source configuration code: Added SMIC and updated S value ■ Updated Table 7.1 Reliability qualifications summary ■ Updated Table 7-2 Package reliability results
H	May 2016	■ Table 3-17 WLED boost converter and driver performance specifications: Updated the output voltage and DC accuracy specifications

Contents

Figures

Tables

1 Introduction

1.1 Documentation overview

Technical information for the PMI8952 is primarily covered by the documents listed in Table 1-1; these documents should be studied for a thorough understanding of the IC and its applications. Released PMI8952 documents are available from the Qualcomm® CreatePoint website at https://createpoint.qti.qualcomm.com.

Table 1-1 Primary PMI8952 device documentation

Document number	Title/description
80-NT391-1 (this document)	*PMI8952 Power Management IC Device Specification* Provides all PMI8952 electrical and mechanical specifications. Additional material includes pin assignment definitions, shipping, storage, and handling instructions, printed circuit board (PCB) mounting guidelines, and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-NT391-4	*PMI8952 Power Management IC Device Revision Guide* Provides a history of PMI8952 revisions. This document explains how to identify the various IC revisions and discusses known issues (or bugs) for each revision and how to work around them.
80-NT390-5	*PM8952/PM8956 + PMI8952 Power Management IC Design Guidelines/training Slides* ■ Detailed functional and interface description ■ Key design guidelines are illustrated and explained, including: □ Technology overviews □ DC power distribution □ Interface schematic details □ PCB layout guidelines □ External component recommendations □ Ground and shielding recommendations
80-NT665-3	*MSM8952 Chipset Layout Guidelines* This document presents layout guidelines for the MSM8952 chipset and its individual ICs. PCB designers can use this single document for mechanical and layout instructions rather than researching each device individually.

This PMI8952 device specification is organized as follows:

Chapter 1 Provides an overview of PMI8952 documentation, shows a high-level PMI8952 functional block diagram, lists the device features, and lists terms and acronyms used throughout this document.

Chapter 2 Defines the IC pin assignments.

Chapter 3 Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of PMI8952 devices.

Chapter 6 Presents procedures and specifications for mounting the PMI8952 onto PCBs.

Chapter 7 Presents PMI8952 reliability data, including definitions of the qualification samples and a summary of qualification test results.

1.2 PMI8952 introduction

The PMI8952 device (Figure 1-1), plus its companion PM8952/PM8956 (80-NT390-x) device, integrates all wireless handset power management, general housekeeping, and user interface support functions into a two IC solution. The versatile design is suitable for multimode, multiband phones, and other wireless products such as data cards and PDAs.

The PMI8952 mixed-signal BiCMOS device is available in the 144-pin wafer nanoscale package (144 WLNSP) that includes ground pins for improved electrical ground, mechanical stability, and thermal continuity.

Since the PMI8952 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the PMI8952 document set is organized by the following device functionality:

- Input power management
- General housekeeping
- User interface
- IC interfaces
- Configurable pins: either multipurpose pins (MPPs) or general-purpose input/output (GPIOs) that can be configured to function within some of the other categories

Most of the information contained in this device specification is organized accordingly including the circuit groupings within the block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3). Refer to the *PM8952/PM8956 + PMI8952 Power Management IC Design Guidelines/training Slides* (80-NT390-5) for more detailed diagrams and descriptions of each PMI8952 function and interface.

Five major functional blocks:

1) Input power management
2) General housekeeping
3) User interfaces
4) IC-level interfaces
5) Configurable I/Os

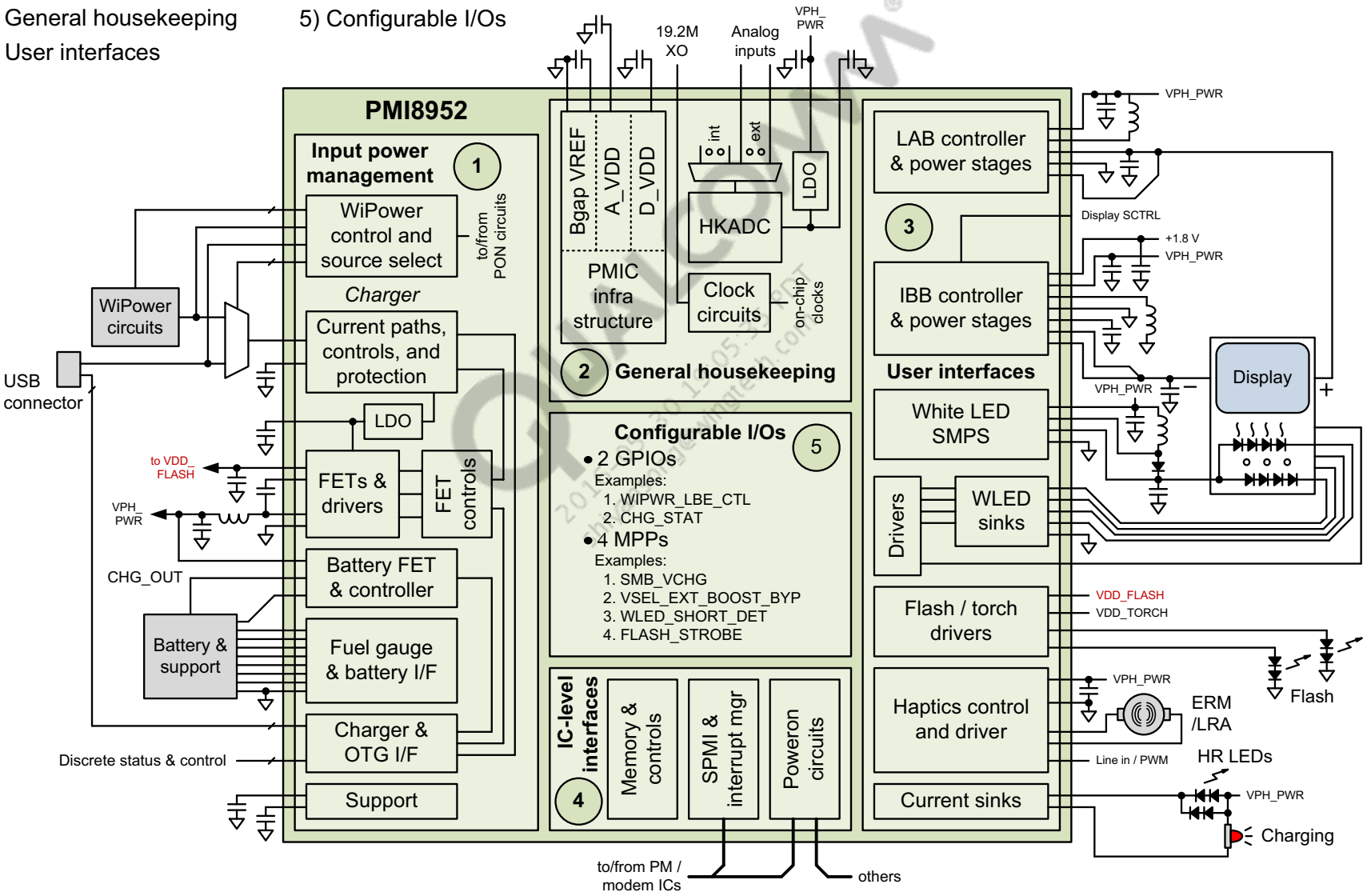


Figure 1-1 High-level PMI8952 functional block diagram

1.3 PMI8952 features

NOTE Some hardware features integrated within the PMI8952 must be enabled through the IC software. Refer to the latest version of the applicable software release notes to identify the enabled PMIC features.

Table 1-2 Summary of PMI8952 features

Feature	PMI8952 capability
Input power management	
Input source selection	■ Supports USB and Qualcomm® WiPower™ (MSM8956 only) power sources with voltage sensors that validate each input source ■ Control bits select the desired source using an external power multiplexer ■ Automatic and programmable input current limit for USB compatibility
Battery charger	Switched-mode battery charger/boost (SCHG) – battery charger with reverse-boost mode ■ Highly efficient (~91% peak efficiency) power conversion and optional parallel charging using the SMB1351 companion IC eliminates heat issues ■ 4–10 V operating input voltage range ■ 28 V over-voltage protection (OVP), non-operating ■ Automatic power source detection (APSD), prioritization, and programmable input current limiting per USB charging specification 1.2 (USB 2.0/3.0 compliant) ■ High charging current, up to 3.0 A (subject to thermal and efficiency requirements) ■ Current path control allows system operation with deeply discharged or missing battery ■ Trickle, precharge, and constant current/voltage charging ■ Integrated BATFET; also functions as current sense element for charging control ■ TurboCharge™ – 750 mA charge from 500 mA USB port ■ JEITA and JISC 8714 support ■ Supports Qualcomm® Quick Charge™ 2.0 and 3.0 technology for fast charging ■ 1.0 MHz, 1.5 MHz, 2.0 MHz, or 3.0 MHz switching frequency – tiny external parts ■ Real-time charge and discharge current measurement ■ USB On-The-Go (OTG) support up to 1 A (USB OTG standard compliant and USB-IF ACA specification compliant) ■ Reverse-boost support for flash LED current, up to 2 A (supports concurrency cases for USB OTG and flash LED) ■ Comprehensive protection features

Table 1-2 Summary of PMI8952 features (cont.)

Feature	PMI8952 capability
Fuel gauge	■ Optimized mixed algorithm with current and voltage monitoring ■ Highly accurate battery state-of-charge estimation ■ 16-bit dedicated current ADC (15 bits plus sign bit) ■ 15-bit dedicated voltage ADC for measuring the VBAT, BATT_THERM, and BATT_ID ■ Operates independently of software and reports state of charge without algorithms running on the modem IC: □ No external non-volatile memory required □ No external configuration required ■ Precise voltage, current temperature, and aging compensation ■ Complete battery cycling is not required to maintain accuracy ■ Missing battery detection ■ One-time programmable (OTP) for default, non-volatile settings ■ Supports multiple battery profiles
WiPower support	■ Based upon the A4WP interface specification ■ IC-level interfacing signals for WiPower ICs such as the Stark DIV2 charge pump IC
BIF support	Battery interface (BIF) support for MIPI-BIF enabled battery packs via the BATT_ID pin
General housekeeping	
On-chip ADC	Housekeeping (HK) ADC supports internal and external (via MPPs) monitoring
Internal clocks	Internal 19.2 MHz clock on PMI8952
Over-temperature protection	Multistage smart thermal control
Programmable boot sequence	Programmable boot sequence (PBS) with OTP memory and user programmable RAM for customizable poweron, poweroff, and reset sequences
User interfaces	
Display bias supplies	Dual synchronous SMPS topology: Boost and inverting buck-boost ■ Supports thin film transistor LCD (TFT-LCD) and AMOLED ■ 86% efficiency converters for both rails with compact BOM ■ 2.5 V to 4.75 V input voltage range ■ Independently programmable positive and negative output voltages ■ S-Wire interface for programming negative rail ■ Programmable output voltage range of ±4.6 V to ±6.0 V (default = ±5.5 V) ■ 100 mV resolution on both bias rails ■ 150 mA (LCD) and 350 mA (AMOLED) output current capability on both supplies ■ Auto output disconnect and active discharge on module shutdown ■ Short circuit protection ■ Auto power sequencing on module enable/disable ■ Anti-ringing compensation on both rails ■ Light load mode for high efficiency

Table 1-2 Summary of PMI8952 features (cont.)

Feature	PMI8952 capability
White LED (WLED) backlighting	Switched-mode boost supply to adaptively boost voltage for series WLEDs plus four regulated current sinks ■ Four LED strings of up to 30 mA each, configurable in 2.5 mA steps ■ 28 V maximum boost voltage ■ Hybrid dimming mode (analog dimming at high LED currents, digital dimming for low currents) ■ 12-bit analog dimming; 9-bit digital dimming ■ Each current sink can be independently controlled via a combination of the brightness control register, full-scale current setting register, and an external CABC pulsewidth modulation (PWM) input ■ 85% efficiency under typical conditions and 15 mA per string ■ High efficiency always-on mode ■ Short circuit detection (with optional external circuit) and light load efficiency mode ■ Isolation of output from input using an external FET ■ Fixed voltage regulation mode for AMOLED panels, supports 7.75 V AMOLED reference
Flash/torch drivers	Two independent high-side current sources for driving LEDs ■ Up to 1.0 A per channel for flash (up to 200 mA for torch) ■ Flexible to support one LED or two LEDs with 2.0 A maximum current ■ Fully programmable LED currents (0~1.0 A per LED, with 12.5 mA/step) ■ PWM dimming at current set at ≤ 100 mA ■ Current ramp up/down control (programmable ramp rate) ■ Current mask upon Tx_GTR_THRESHinput (over SPMI) ■ Thermal current derate ■ Short/open circuit detection ■ Max-on safety timer, watchdog timer, and thermal shutdown safety
Haptics driver	One full H-bridge power stage for driving haptics ■ Bidirectional drive capability with support for active braking ■ Support for eccentric rotating machines (ERM) and linear resonant actuators (LRA) ■ Programmable internal PWM frequency from 250–1000 kHz in ~250 kHz steps ■ Programmable LRA frequency from 50 Hz to 300 Hz, with a 0.5 Hz tuning resolution ■ 5-bit output control from 0 V to Vmax; Vmax configurable from 1.2–3.6 V in 116 mV steps ■ Support for internal 8-bit LUT to store haptics pattern, repeat, and loop ■ Dual PWM for double the effective switching frequency ■ Automatic resonance tracking ■ External input for audio/PWM mode support ■ Short circuit detection and current limit protection ■ Supports fixed DC output for simple vibration patterns
Other current sinks	■ Charging indicator ■ Two MPP can function as a static current sink ■ Support for up to 40 mA current in 5 mA steps; ±20% accuracy

Table 1-2 Summary of PMI8952 features (cont.)

Feature	PMI8952 capability
IC-level interfaces	
Primary status and control	Two-line serial power management interface (MIPI SPMI)
Interrupt managers	Supported by SPMI
BUA	Battery UICC alarm for graceful shutdown to prevent corruption of UICC on a battery disconnection event
BIF	Battery interface (BIF) support for MIPI-BIF enabled battery packs via the BATT_ID pin
Configurable I/Os	
MPPs	Four MPPS, all configurable as digital inputs or digital outputs; one configurable as analog multiplexer input; two configurable as current sinks; two configurable as analog outputs
GPIO pins	Two GPIO pins, configurable as digital inputs or outputs
Fabrication technology and package	
Fabrication technology	Mixed-signal BiCMOS
Size	5.11 × 4.77 × 0.55 mm
Pin count and package type	144-pin wafer-level nanoscale package (144 WLNSP)

1.4 Terms and acronyms

Table 1-3 defines terms and acronyms used throughout this document.

Table 1-3 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
API	Application programming interface
APSD	Automatic power source detection
ATC	Auto-trickle charger
AVS	Adaptive voltage scaling
CDMA	Code Division Multiple Access
DVS	Dynamic voltage scaling
ERM	Eccentric rotating mass
GPIO	General-purpose input/output
GSM	Global system for mobile communications
HK	Housekeeping
IBB	Inverting buck/boost converter
ID	Identification
LDO	Low dropout (linear regulator)

Table 1-3 Terms and acronyms (cont.)

Term or acronym	Definition
LAB	LCD/AMOLED boost
Li	Lithium
LRA	Linear resonance actuator
MPP	Multipurpose pin
MUX	Multiplexer
NSP	Nanoscale package
OTG	On-the-go
OTP	One-time programmable
PA	Power amplifier
PBS	Programmable boot sequence
PCB	Printed circuit board
PDA	Personal digital assistant
PLL	Phase-locked loop
PM	Power management
PMI	Power management interface
PWM	Pulse width modulation
QTI	Qualcomm Technologies, Inc
SDP	Standard downstream port (USB)
SCHG	Switched mode battery boost/charger
SMPS	Switched mode power supply (DC-to-DC converter)
SPMI	Serial power management interface
SVS	Static voltage scaline
TCXO	Temperature-compensated crystal oscillator
UICC	Universal integrated circuit card
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
VCO	Voltage-controlled oscillator
WLED	White LED (high voltage)
WLNSP	Wafer-level nanoscale package
XO	Crystal oscillator

1.5 Special marks

Special marks used in this document are defined below.

Table 1-4 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA [7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, PON_RESET_N.
0x0000	Hexadecimal numbers are identified with an x in the number, (for example, 0x0000). All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, [for example, 0011 (binary)].
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin definitions

The PMI8952 is available in the 144 WLNSP. See Chapter 4 for package details. Figure 2-1 shows a high-level view of the pin assignments for the PMI8952.

1 VDIS_ N_OUT	2 VSW_ DIS_N	3 VDD_ DIS_N	4 GND_ DIS_P	5 VDIS_ P_OUT	6 VREG_ WLED	7 VDD_ WLED	8 GND_ WLED	9 VSW_ WLED	10 MPP_3	11 HAP_ PWM_IN	12 HAP_ PWM_IN
13 VDIS_ N_OUT	14 VSW_ DIS_N	15 DIS_N_ CAP_REF	16 VSW_ DIS_P	17 VSW_ DIS_P	18 NC	19 NC	20 WLED_ SINK2	21 WLED_ SINK1	22 MPP_1	23 GNDC	24 HAP_ OUT_N
25 VDD_1P8 _DIS_N	26 GND_ DIS_N _REF	27 VDIS_ N_FB	28 VDD_ DIS_P	29 VDIS_ P_FB	30 WLED_ CABC	31 GND_ WLED_I	32 WLED_ SINK3	33 WLED_ SINK4	34 MPP_2	35 HAP_ OUT_P	36 GND_ HAP
37 GNDC	38 SPMI_ CLK	39 SPMI_ DATA	40 NC	41 NC	42 VDD_ MSM_IO	43 BUA	44 NC	45 GNDC	46 VREG_ ADC_LDO	47 MPP_4	48 VDD_ HAP
49 GNDC	50 CLK_IN	51 DIS_ SCTRL	52 GNDC	53 AVDD _BYP	54 DVDD _BYP	55 SHDN_N	56 GNDC	57 VDD_ ADC_LDO	58 REF_ BYP	59 GND_ REF	60 VDD_ TORCH
61 CS_ PLUS	62 BATT_ PLUS	63 GPIO_2	64 GNDC	65 GNDC	66 GNDC	67 GNDC	68 RESIN_N	69 PS_HOLD	70 GNDC	71 FLASH _LED1	72 VDD_ FLASH
73 CS_ MINUS	74 BATT_ MINUS	75 GPIO_1	76 GNDC	77 GNDC	78 GNDC	79 GNDC	80 USB_ID	81 WIPWR_ DIV2_EN	82 GNDC	83 FLASH _LED2	84 VDD_ FLASH
85 R_BIAS	86 BATT_ID	87 GNDC	88 DC_EN	89 WIPWR _RST_N	90 USB_ID _RVAL1	91 CHG_LED	92 USB_SNS	93 SYSON	94 FLASH _OUT	95 FLASH _OUT	96 FLASH _OUT
97 BATT_ THERM	98 VAA_ CAP	99 GNDC	100 USB_EN	101 USB_CS	102 CHG_EN	103 PGOOD _SYSOK	104 DC_SNS	105 BOOT_ CAP	106 VSW_ CHG	107 VSW_ CHG	108 VSW_ CHG
109 GNDC	110 GND_FG	111 USB_DP	112 USB_ID _RVAL2	113 CHG_OUT	114 VPH_ PWR	115 GNDC	116 VSW_ CHG	117 VSW_ CHG	118 VSW_ CHG	119 VSW_ CHG	120 VSW_ CHG
121 GNDC	122 GND_ REF_CHG	123 USB_DM	124 CHG_ VBAT _SNS	125 CHG_OUT	126 CHG_OUT	127 VPH_ PWR	128 GND_ CHG	129 GND_ CHG	130 USB_ MID	131 USB_ MID	132 USB_ MID
133 GNDC	134 KYPD_ PWR_N	135 V_ARB	136 GNDC	137 CHG_OUT	138 VPH_ PWR	139 VPH_ PWR	140 WIPWR_ CHG_OK	141 GND_ CHG	142 USB_IN	143 USB_IN	144 USB_IN

Configurable IOs | General Housekeeping | Ground | IC-level Interfaces | Input Power Management | No Connect | Power | User Interfaces

Figure 2-1 PMI8952 pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
GNDC	Common ground; a pad that does not handle a significant amount of current flow, typically used for grounding digital circuits and substrates.
GNDP	Power ground; a pad that handles 10 mA or more of current flow returning to ground. Layout considerations must be made for these pads.
PI	Power input; a pad that handles 10 mA or more of current flow into the device [1]
PO	Power output; a pad that handles 10 mA or more of current flow out of the device [1]
Z	High-impedance (high-Z or Hi-Z) output
GPIO pins, when configured as outputs, have configurable drive strengths that depend upon the GPIO pad's supply voltage. See the electrical specifications in Chapter 3 for details.	

1. The maximum current levels expected on PI and PO type pads are listed in Chapter 3.

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2 Input power management

Table 2-3 General housekeeping

Table 2-4 User interfaces

Table 2-5 IC-level interfaces

Table 2-6 Configurable input/output – MPPs and GPIOs

Table 2-7 No connect pins

Table 2-8 Power supply pins

Table 2-9 Ground pins

Table 2-2 Pad descriptions – input power management functions

Pad #	Pad name	Pad type [1]	Functional description
Wireless power (WiPower) control and source select			
140	WIPWR_CHG_OK	DO-Z	Requests WiPower to source charger power when high-Z; logic low indicates charging is done and/or WiPower source was not requested
81	WIPWR_DIV2_EN	DI	WiPower front-end indication of charge-pump divide-by-2 (H) or pass through (L) mode; PMI then selects appropriate current limit
104	DC_SNS	AI	WiPower voltage sense to determine in or out of valid range
88	DC_EN	DO	Enable WiPower path from external power multiplexer
92	USB_SNS	AI	USB input voltage sense pin from external power multiplexer
100	USB_EN	DO	Enable USB path from external power multiplexer
Switched mode battery charger/boost			
142, 143, 144	USB_IN	PI, PO	Input power from selected source (USB or WiPWR), or output during USB-OTG. This input powers charger via OVP circuitry.
130, 131, 132	USB_MID	AO	Node between OVP FET and the high-side switching FET; mid-FET capacitor node for accurate current level sensing through OVP FETs
93	SYSON	AO	LDO output that supplies SCHG FET drivers; connect bypass capacitor
94, 95, 96	FLASH_OUT	PO	PMI-generated supply voltage for flash drivers
105	BOOT_CAP	AO	Bootstrap power for charger bias networks before SCHG starts
106, 107, 108, 116, 117, 118, 119, 120	VSW_CHG	PI, PO	Charger SMPS switching node
114, 127, 138, 139	VPH_PWR	PI, PO	Primary system power supply node; SCHG's regulation node
113, 125, 126, 137	CHG_OUT	PI, PO	Battery FET output during charging; FET input when battery is VPH_PWR source
128, 129, 141	GND_CHG	GNDP	SCHG power ground; specific layout instructions must be followed
122	GND_REF_CHG	GNDP	Ground for SCHG's dedicated master bandgap; specific layout instructions must be followed
124	CHG_VBAT_SNS	AI	Sensed battery voltage for charger circuits

Table 2-2 Pad descriptions – input power management functions (cont.)

Pad #	Pad name	Pad type [1]	Functional description
Fuel gauge and battery interface			
61	CS_PLUS	AI	Current sense resistor—plus side (high side)
73	CS_MINUS	AI	Current sense resistor—minus side (low side)
85	R_BIAS	AO	Dedicated voltage source for battery-related resistor networks
86	BATT_ID	AI	Battery ID input to ADC and MIPI BIF interface; also detects missing battery
97	BATT_THERM	AI	Battery temperature input to ADC (measures pack temperature); used by FG and by charger to ensure safe operation
62	BATT_PLUS	AI	Battery plus (+) terminal sense input; connect directly
74	BATT_MINUS	AI	Battery minus (-) terminal sense input; connect directly
98	VAA_CAP	AO	LDO output #1 that supplies fuel gauge circuits; connect bypass capacitor only—*do not load externally*
135	V_ARB	AO	LDO output #2 that supplies fuel gauge circuits; connect bypass capacitor only—*do not load externally*
110	GND_FG	GNDP	Fuel gauge analog ground; connect to LDO load capacitors
Charger and OTG interface			
123	USB_DM	AI, AO	USB data minus for power source detection only; modem IC handles data transactions
111	USB_DP	AI, AO	USB data plus for power source detection only; modem IC handles data transactions
80	USB_ID	AI, AO	Dual function: ■ OTG mode enable (programmable polarity; can also be controlled by OTG enable bit) ■ OTG ID monitor to detect the OTG attach
101	USB_CS	DI	USB default current limit control for when an SDP is connected and detected by APSD while in its pin control mode
102	CHG_EN	DI	Charger enable (factory option with programmable polarity; can also be activated by a register bit)
90	USB_ID_RVAL1	DO	Two bits indicate USB_ID resistor value (and therefore attached USB device-type); also identifies MCPC audio or factory boot mode
112	USB_ID_RVAL2	DO	

1. See Table 2-1 for parameter and acronym definitions.

Table 2-3 Pad descriptions – general housekeeping functions

Pad #	Pad name [3]	Pad type	Functional description
HK ADC circuits			
57	VDD_ADC_LDO	PI	Power supply for dedicated HK ADC LDO
46	VREG_ADC_LDO	AO	LDO output that supplies HK ADC circuits; connect bypass capacitor only—*do not load externally*
Clock circuits			
50	CLK_IN	AI	19.2 MHz clock input (from PM8952/PM8956, not planned to be used. PMI8952 will use its internal clock)
PMIC power infrastructure			
58	REF_BYP	AO	Master bandgap regulator output; connect bypass capacitor only—*do not load externally*
59	GND_REF	GNDP	Master bandgap regulator ground; specific layout instructions must be followed
53	AVDD_BYP	AO	LDO output that supplies analog infrastructure circuits; connect bypass capacitor only—*do not load externally*
54	DVDD_BYP	AO	LDO output that supplies digital infrastructure circuits; connect bypass capacitor only—*do not load externally*
GPIOs may be configured for general housekeeping functions not listed here. [1] MPPs may be configured for general housekeeping functions not listed here. [2]			

1. GPIOs may be configured for user interface functions. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function carefully—avoiding assignment conflicts. All GPIOs are listed in Table 2-6.
2. Other user interface MPP functions are possible. To assign an MPP a particular function, identify all of your application's requirements and map each MPP to its function carefully—avoiding assignment conflicts. All MPPs are listed in Table 2-6.
3. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pad descriptions – user interface functions

Pad #	Pad name	Pad type [3]	Functional description
± Display bias for LCD/AMOLED			
28	VDD_DIS_P	PI	Power supply for LDC/AMOLED boost (LAB) circuits
16, 17	VSW_DIS_P	PO	LAB switching node for the display's positive bias
5	VDIS_P_OUT	PO	LAB regulated output for the display's positive bias
29	VDIS_P_FB	AI	LAB sense point (feedback)
4	GND_DIS_P	GNDP	LAB power ground; specific layout instructions must be followed
51	DIS_SCTRL	DI	SWIRE interface for LCD and AMOLED displays; used to enable positive and/or negative bias outputs and to set their voltages
25	VDD_1P8_DIS_N	PI	1.8 V power supply for inverting buck boost (IBB) circuits
3	VDD_DIS_N	PI	Power supply for IBB circuits
2, 14	VSW_DIS_N	PO	IBB switching node for the display's negative bias
26	GND_DIS_N_REF	GNDP	IBB power ground; specific layout instructions must be followed
15	DIS_N_CAP_REF	AO	Voltage reference capacitor; cap value tunes IBB slew rates
27	VDIS_N_FB	AI	IBB sense point (feedback)
1, 13	VDIS_N_OUT	PO	IBB regulated output for the display's negative bias
White LED SMPS			
7	VDD_WLED	PI	Power supply for WLED boost SMPS
9	VSW_WLED	PO	WLED boost SMPS switching node
6	VREG_WLED	AI	WLED boost SMPS sense input
8	GND_WLED	GNDP	WLED boost SMPS power ground; specific layout instructions must be followed
21	WLED_SINK1	AO	WLED low-side current sink input, string 1
20	WLED_SINK2	AO	WLED low-side current sink input, string 2
32	WLED_SINK3	AO	WLED low-side current sink input, string 3
33	WLED_SINK4	AO	WLED low-side current sink input, string 4
31	GND_WLED_I	GNDP	Shared WLED low-side current sink's power ground
30	WLED_CABC	DI	Content adaptive backlight control (CABC); PWM signal from display controller for dynamic dimming of LCD
Flash and torch LED drivers			
60	VDD_TORCH	PI	Power supply for torch-mode drivers (to 5 V)
72, 84	VDD_FLASH	PI	Power supply for flash-mode drivers (to 5 V)
71	FLASH_LED1	AO	High-side current source for flash/torch LED1 anode
83	FLASH_LED2	AO	High-side current source for flash/torch LED2 anode

Table 2-4 Pad descriptions – user interface functions (cont.)

Pad #	Pad name	Pad type [3]	Functional description
Haptics			
48	VDD_HAP	PI	Power supply for Haptics circuits
36	GND_HAP	GNDP	Haptics power ground
35	HAP_OUT_P	AO	Haptics H-bridge driver output positive
24	HAP_OUT_N	AO	Haptics H-bridge driver output negative
11, 12	HAP_PWM_IN	DI	PWM input for haptic control
Other current sinks			
91	CHG_LED	AO	Current sink for charging indication
GPIOs may be configured for user interface functions. [1]			
MPPs may be configured for user interface functions not listed here. [2]			

1. GPIOs may be configured for user interface functions. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function carefully—avoiding assignment conflicts. All GPIOs are listed in Table 2-6.
2. Other user interface MPP functions are possible. To assign an MPP a particular function, identify all of your application's requirements and map each MPP to its function carefully—avoiding assignment conflicts. All MPPs are listed in Table 2-6.
3. See Table 2-1 for parameter and acronym definitions.

Table 2-5 Pad descriptions – IC-level interface functions

Pad #	Pad name	Pad type [3]	Functional description
IC-level interfacing power supply			
42	VDD_MSM_IO	PI	Power supply for digital I/Os to/from the modem IC
Power on/off/reset control			
134	KYPD_PWR_N	DI	Exits ship mode when pressed; does not trigger PMI8952 device poweron
69	PS_HOLD	DI	Power supply hold; driven by the PM8952/PM8956 PON_RESET_N signal and shared with the modem IC's RESIN_N; PM instructs PMI to keep its power supplies on, and can initiate a modem IC reset or powerdown when low.
55	SHDN_N	DI	The only PMI poweron trigger; connected to the PM8952/PM8956 device's VREG_L5 output that goes high during the poweron sequence; when input power is absent and SHDN_N is low, the charger enters a low-power shutdown mode
103	PGOOD_SYSOK	DO	Power good/system okay; initiates PM8952/PM8956 poweron sequence at charger attachment; also initiates a graceful transition to a low power state when power source is removed or a graceful shutdown when VBAT falls below VLOWBATT.
68	RESIN_N	DI	Reset; initiates various types of resets, clear faults, and clear interrupts.
43	BUA	DO, DI	Battery UICC alarm; as output, informs the modem IC of a battery removal; as input, receives UICC removal alarm
89	WIPWR_RST_N	DO	WiPower reset; used by PMI when the battery is dead to hold the modem IC in reset until adequate power is available
System power management interface			
38	SPMI_CLK	DO	SPMI communication bus clock signal
39	SPMI_DATA	DI, DO	SPMI communication bus data signal
GPIOs may be configured for IC-level interface functions not listed here. [1]			
MPPs may be configured for IC-level interface functions. [2]			

1. Other IC-level interface GPIO functions are possible. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function carefully—avoiding assignment conflicts. All GPIOs are listed in Table 2-6.
2. MPPs may be configured for IC-level interface functions. To assign an MPP a particular function, identify all of your application's requirements and map each MPP to its function carefully—avoiding assignment conflicts. All MPPs are listed in Table 2-6.
3. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Pad descriptions – configurable input/output functions

Pad #	Pad name/configurable function	Pad type [1]	Functional description
MPP functions			
22	MPP_1 SMB_VCHG	AO-Z AO	Configurable MPP Reports charger input current to SMB during parallel charging; this function is only available on MPP_1
34	MPP_2 VSEL_EXT_BOOST_BYP (or HR_LED_SINK)	AO-Z DO	Configurable MPP Selects voltage set-point of external boost-bypass SMPS; L = 3.15 V, H = 3.60 V
10	MPP_3 WLED_SHORT_DET	AO-Z DO	Configurable MPP External FET control signal for WLED short circuit protection
47	MPP_4 FLASH_STROBE	AO-Z DI	Configurable MPP Signal that triggers and synchronizes PMI flash with camera sensor
GPIO functions			
75	GPIO_1 WIPWR_LBE_CTL (or PWM_OUT)	DI-PD DO	Configurable GPIO WiPower long beacon extension (LBE) control
63	GPIO_2 CHG_STAT	DI-PD DO	Configurable GPIO Connect to SMB_EN for parallel charging

1. See Table 2-1 for the parameter and acronym definitions.

NOTE All GPIOs default to digital input with a 10 µA pulldown. All MPPs default to high-Z.

NOTE Configure unused MPPs as 0 mA current sinks (high-Z) and GPIOs as digital inputs with their internal pulldowns enabled.

Table 2-7 Pad descriptions – no connect

Pad #	Pad name	Functional description
18, 19, 40, 41, 44	NC	Not connected internally, do not connect externally

Table 2-8 Pad descriptions – DC power supply voltages

Pad #	Pad name	Functional description
General housekeeping		
See Table 2-3 Includes VDD_ADC_LDO		
User interfaces		
See Table 2-4 Includes VDD_1P8_DIS_N, VDD_DIS_N, VDD_DIS_P, VDD_FLASH, VDD_HAP, VDD_TORCH, and VDD_WLED		
IC-level interfaces		
See Table 2-5 Includes VDD_MSM_IO		

Table 2-9 Pad descriptions – grounds

Pad #	Pad name	Functional description
General purpose (common) ground pins		
23, 37, 45, 49, 52, 56, 64, 65, 66, 67, 70, 76, 77, 78, 79, 82, 87, 99, 109, 115, 121, 133, 136	GNDC	Ground for non-specialized circuits
Input power management		
See Table 2-2 Includes GND_CHG, GND_FG, and GND_REF_CHG		
General housekeeping		
See Table 2-3 Includes GND_REF		
User interfaces		
See Table 2-4 Includes GND_DIS_N_REF, GND_DIS_P, GND_HAP, GND_WLED, GND_WLED_I		

3 Electrical specifications

3.1 Absolute maximum ratings

Operating the PMI8952 under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Input power management functions				
DC_SNS	WiPower voltage sense	-0.3	28	V
USB_SNS	USB input voltage sense	-0.3	28	V
USB_IN	Input power from USB source	-0.3	28	V
USB_MID	Input power from USB source (unprotected connection to USB_IN, not for general use)	-0.3	28	V
VSW_CHG	Switching node of charger buck	-0.3	12	V
CHG_VBAT_SNS, CHG_OUT (VBAT)	Main-battery voltage Steady state Transient (< 10 ms)	 -0.3 -0.3	 6.0 7.0	 V V
VPH_PWR	Handset power-supply voltage	-0.3	7.0	V
Power supply pads				
VDD_FLASH	Camera flash, video torch supply voltage	-0.3	12 (flash disabled)	V
VDD_xxx	All power supply pads not listed elsewhere in this table (see Table 2-8)	-0.5	6.0	V
Signal pins				
V_IN	Voltage on any non-power supply pin [1]	-0.5	V_{XX} + 0.5	V
ESD protection and thermal conditions – see Section 7.1 and Section 4.5.				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the user: power supply voltage and ambient temperature (Table 3-2). The PMI8952 meets all performance specifications listed in Section 3.3 through Section 3.9 when used and/or stored within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Input power management functions					
DC_SNS	WiPower voltage sense	3.7	–	10	V
USB_SNS	USB input voltage sense	3.7	–	10	V
USB_IN	Input power from USB source	3.7	–	10	V
USB_MID	Input power from USB source (unprotected connection to USB_IN, not for general use)	3.7	–	10	V
CHG_VBAT_SNS, CHG_OUT (VBAT)	Main battery voltage	2.5	3.6	4.75	V
VPH_PWR	Handset power-supply voltage	2.5	3.6	4.75	V
Power supply pads					
VDD_MSM_IO	Pad voltage for digital I/Os to/from the IC	1.75	1.80	1.85	V
VDD_1P8_DIS_N	Inverting buck boost controller circuits	1.75	1.80	1.85	V
VDD_FLASH, VDD_TORCH	Camera flash, video torch supply voltage	2.5	3.6	5.5	V
VDD_xxx	All power supply pads not listed elsewhere in this table (see Table 2-8)	2.5	3.6	4.75	V
Signal pins					
V_IN	Voltage on any non-power-supply pin [1]	0	–	V_{XX} + 0.5	V
Thermal conditions					
T_A	Ambient operating temperature	-30	25	85	°C
T_J	Junction operating temperature [2]	-30	25	125	°C

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.
2. Junction temperature specification supersedes ambient temperature specification if the die power dissipation is high enough to cause an on-die temperature rise of more than 40°C.

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default settings.

Table 3-3 DC power supply currents

Parameter		Comments	Min	Typ	Max	Units
IDD_ACTIVE	Supply current, active mode [1]		–	300	700	µA
IDD_SLEEP	Supply current, sleep mode [2]		–	130	175	µA
IDD_OFF	Supply current, off mode [3]		–	45	85	µA
IDD_SHIP	Supply current, ship mode [4]		–	17	25	µA
IDD_USB	USB charger current in suspend mode [5]		–	600	2000	µA
IDD_DC	DC charger current in suspend mode [6]		–	600	2000	µA
IDD_OTG	OTG supply current	OTG mode, 3.6 V VBATT, 5.0 V VUSB, no load	–	30	40	mA

1. I_ACTIVE is the total supply current from the battery with the PMI8952 on, fuel gauge in active state, charger in standby, and with WLED, flash, torch, LAB, IBB, Haptics circuits all off.
2. I_SLEEP is the total supply current from the battery with the PMI8952 on after executing its sleep sequence. In this state the fuel gauge is in its sleep state, charger in standby, and WLED, flash, torch, LAB, IBB, and Haptics circuits are all off. In this condition BATT_ID pull down = 240 W while the BATT_THERM = 68.1 kW and VBAT = 3.6 V.
3. I_OFF is the total supply current from the battery with PMI8952 off. This only applies when the temperature is between -30°C and +60°C.
4. I_SHIP is the total supply current from the battery with PMI8952 in ship mode and BATFET is open. This only applies when the temperature is between -30°C and +60°C.
5. I_USB is the total supply current from a USB charger when the phone has a good battery (VBAT > 3.2 V and not being charged). During USB suspend, current from a PC is limited to 2.5 mA.
6. I_DC is the total supply current from a DC charger (power multiplexer installed and WiPower source selected) when the phone has a good battery (VBAT > 3.2 V and not being charged).

3.4 Digital logic characteristics

The charger has unique digital signaling characteristics as listed within Section 3.5.2; all other PMI8952 digital I/O characteristics are specified in Table 3-4.

Table 3-4 Digital I/O characteristics

Parameter		Comments [4]	Min	Typ	Max	Units
V_{IH}	High-level input voltage		0.65 · V_{IO}	–	V_{IO} + 0.3	V
V_{IL}	Low-level input voltage		-0.3	–	0.35 · V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage		15	–	–	mV
I_L	Input leakage current [1]	V_{IO} = max, V_{IN} = 0 V to V_{IO}	-0.20	–	+0.20	µA
V_{OH}	High-level output voltage	I_{out} = I_{OH}	V_{IO} - 0.45	–	V_{IO}	V
V_{OL}	Low-level output voltage	I_{out} = I_{OL}	0	–	0.45	V
I_{OH}	High-level output current [2]	V_{out} = V_{OH}	3	–	–	mA
I_{OL}	Low-level output current [2]	V_{out} = V_{OL}	–	–	-3	mA
C_{IN}	Input capacitance [3]		–	–	5	pF

1. MPP and GPIO pins comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.
2. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as MPP and GPIO pins).
3. Input capacitance is guaranteed by design but is not 100% tested.
4. V_{IO} is the supply voltage for the modem IC/PMIC interface (most PMIC digital I/Os).

3.5 Input power management

Input power management performance specifications are split into two functional categories as defined within its block diagram (Figure 3-1): battery charger and fuel gauge.

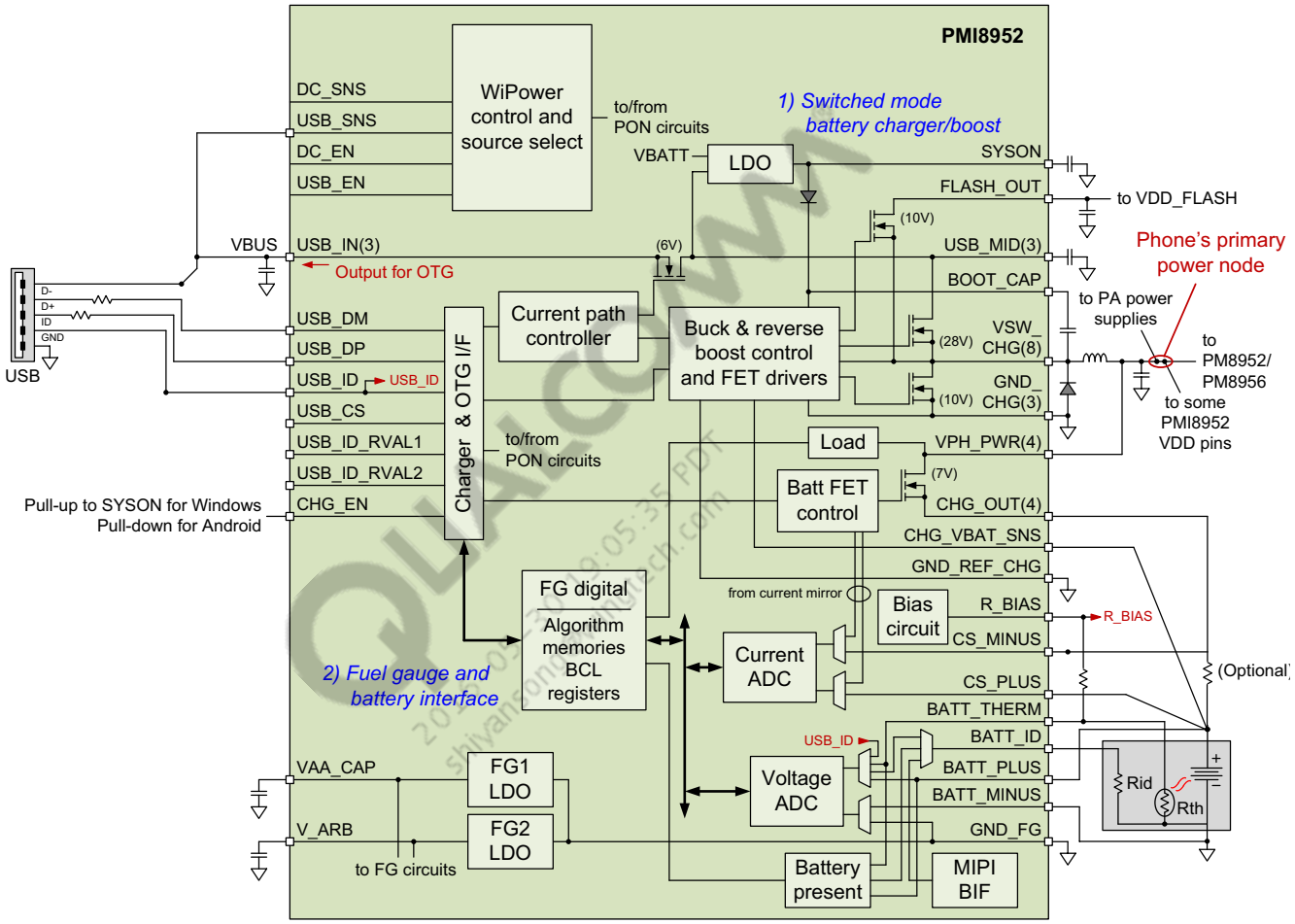


Figure 3-1 Input power management functional block diagram

3.5.1 Battery charger

The PMI8952 features a fully programmable switch-mode Li-ion battery charger, input power and output power controller for portable devices. The device is designed to be used in conjunction with systems using single-cell Li-ion and Li-polymer battery packs. The PMI8952 provides three major functions to the end-system: input selection and arbitration, system output supply and control, and battery charging. The device is fully programmable via the SPMI interface.

Table 3-5 Battery charger specifications

Parameter	Comments [8]	Min	Typ	Max	Units
Input source control, protection, and CurrentPath power path management					
Input voltage ranges	V_FLOAT = 4.2 V				
DC_SNS		3.70	–	10.0	V
USB_SNS		3.70	–	10.0	V
USB_IN		3.70	–	10.0	V
Input voltage lockout					
Under-voltage (UVLO)					
Threshold, falling V, option A		3.50	3.60	3.70	V
Threshold, falling V, option B		6.70	7.00	7.30	V
USB_FAIL low threshold		4.00	4.15	4.30	V
Over-voltage (OVLO) [1]					
Threshold, rising V, option A		6.20	6.40	6.50	V
Threshold, rising V, option B		6.85	7.15	7.45	V
Threshold, rising V, option C		10.0	10.3	10.6	V
Hysteresis					
UVLO, OVLO		–	0.15	–	V
USB_FAIL		–	0.20	–	V
USBIN absolute input current limit [2]	USB2.0 option: USBCS = HIGH, VOUT > 2.1 V, T = 0°C to +70°C	400	450	500	mA
	USB2.0 option: USBCS = GND, VOUT > 2.1 V, T = 0°C to +45°C [9]	50	80	100	mA
	USB2.0 option: USBCS = GND, VOUT > 2.1 V, T = +45°C to +70°C [9]	0		100	mA
	USB3.0 option: USBCS = HIGH, VOUT > 2.1 V, T = 0°C to +70°C	775	838	900	mA
	USB3.0 option: USBCS = GND, VOUT > 2.1 V, T = 0°C to +70°C [9]	102	125	150	mA
	USBCS floating (programmable 300 mA–3000 mA), $I_{LIM-USBIN}$ = 1000 mA, T = 0°C to +70°C	890	1000	1100	mA
	T= 0°C to +70°C, $I_{LIM-USBIN}$ = all other settings [10]	-80 mA -6.0%	–	+80 mA +6.0%	
Thermal protection – see Table 3-6					
AICL					
AICL threshold accuracy	HC mode, USB_IN falling, V_CL set to 4.25 V	–	–	±3.5	%
AICL hysteresis		–	200	–	mV
AICL glitch filter (rising/falling)		–	20	–	ms
AICL auto-timer; eight settings	Re-initiates AICL algorithm	2.8	11.3	360	sec

Table 3-5 Battery charger specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
APSD [3]					
D+ source voltage	Loaded with 125 µA	0.5	0.6	0.7	V
D- source voltage	Loaded with 125 µA	0.5	0.6	0.7	V
Data detect voltage		0.250	0.325	0.400	V
D+ pull-up voltage		3.0	–	3.6	V
D+ sink current		50	–	125	µA
D- sink current		50	–	125	µA
Data contact detect current source		7	–	13	µA
Timing characteristics					
D+ source on time		100	–	–	ms
D+ source off to high current		40	–	–	ms
D+ source off to connect		40	–	–	ms
DCD Timeout, option 1		321	328	335	ms
DCD Timeout, option 2		642	656	670	ms
Dead battery charging timer			30	45	min
Charger detect debounce		10	–	–	ms
WiPower					
Input impedance limiter	±1 divided by input current limit accuracy	-5.6	–	6.38	%
Input power limiter	Maximum power drawn from PMI; smartphone setting	–	–	5	W
USB_IN voltage comparator					
Threshold	DIV2_EN = high	–	6.5	–	V
Hysteresis		–	320	–	mV
DIV2_EN falling-edge de-glitch timer	Four programmable settings; DIV2_EN high-to-low; AICL disabled-to-enabled	0	–	500	µs
Battery Charging with Switching Charger (SCHG)					
Float voltage (V_FLT) range and nominal	20 mV steps	3.60	4.20	4.50	V
Float voltage accuracy	T = 0 to 70°C				
V_FLT = 4.2 V, 4.35 V, 4.4 V		–	–	±0.5	%
Other settings	Programmable 3.60–4.50 V, 20 mV steps,	–	–	±1.0	%
Fast charge current accuracy	T = 0 to 70°C				
Set for 1000 mA	VBAT > VSYS_MIN	890	1000	1110	mA
Error at all other settings [10]	Programmable 300 to 3000 mA	-100 mA -2.5%	–	+100 mA +2.5%	
Charge termination current accuracy [4]	T = 0 to 70°C				
Set for 50/100/150/200 mA		–	–	±50	mA
Error at all other settings [10]	Programmable 50 to 600 mA	–	–	±20	%

Table 3-5 Battery charger specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
Charge termination glitch filter		–	1	–	sec
Recharge threshold voltage (V_FLT - VBAT)	Only two valid settings	50	–	200	mV
Pre-charge to fast charge threshold accuracy	VBAT rising; 2.8 V setting Programmable 2.4 to 3.0 V	–	–	±4	%
Pre-charge current	Programmable 100 mA–250 mA and 550 mA, 5 steps				
	T = 25°C	-20	–	40	%
	T = 0°C to +70°C[7]	-40	–	50	%
Trickle to pre-charge voltage threshold		2.0	2.1	2.2	V
Trickle charge current	VBAT = 1.7 V	–	45	–	mA
Charger buck regulator					
FET on-resistance					
USBIN front porch FET, 6 V		–	41	–	mΩ
USBIN high-side FET, 28 V		–	88	–	mΩ
Low-side, 10 V		–	54	–	mΩ
Peak switching current	USB_IN = 9.0 V	–	4	–	A
Maximum DC output current	USB_IN = 9.0 V	–	3.5	–	A
Switching frequency (default) [5]		0.95	1.0	1.05	MHz
Duty cycle	Over stated frequency range	0	–	99.1	%
Maximum regulated output voltage	Charging disabled	–	4.6	–	V
Minimum regulated output voltage	Charging, 3 settings	3.15	3.45	3.60	V
Regulated output voltage accuracy	I_SYS = 0 A, VPH = 3.6 or 4.3 V				
USB_SNS or DC_SNS = 5 V	Room temperature	–	–	±2.0	%
USB_SNS or DC_SNS = 5 to 10 V	Over temperature range	–	–	±2.5	%
Regulated output voltage	VPH = VPH_PWR				
Charging	IR = IR drop, VPH to VBAT				
VPH_MIN < VPH < VPH_MAX		–	VBAT + IR	–	V
VBAT < VPH_MIN		–	VPH_MIN	–	V
Not charging					
VBAT > VPH_MIN option A		–	VBAT + 0.1	–	V
VBAT > VPH_MIN option B		–	VBAT + 0.2	–	V
Output load regulation	Load steps from 0–1 A in 15 µs	VBAT - 0.2	VBAT - 0.1	–	V
Regulated BATFET voltage offset from VBAT (ideal diode)	V_OUT falling, VBAT > V_OUT, I_OUT = 300 mA	–	VBAT - 65	VBAT - 125	mV
Peak efficiency	USB_IN = 5 V, VBATT = 4.35 V, Fsw = 1.0 MHz, 1 µH DFE252012F	–	93	–	%
	USB_IN = 9 V, VBATT = 4.35 V, Fsw = 1.0 MHz, 1 µH DFE252012F	–	89.2	–	%

Table 3-5 Battery charger specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
Power dissipation					
1.5 A charge current, 5 V input	See Figure 3-3 for typical power dissipation curves	–	572	–	mW
1.5 A charge current, 7 V input		–	638	–	mW
1.5 A charge current, 9 V input		–	730	–	mW
SYSON analog output					
SYSON output voltage	I_OUT = 50 mA; USB_IN or DC_IN > 5.0 V	4.7	5.0	5.3	V
Battery FET					
Battery FET on resistance [10]		–	12	–	mΩ
Battery FET continuous current [10]	Pad limited	–	–	6	A
Battery FET peak current [10]	Pad limited, 10% duty cycle	–	–	8	A
USB-OTG, HDMI, MHL modes					
OTG output voltage		4.75	5.00	5.25	V
OTG battery UVLO accuracy, VBAT falling	2.70 to 3.30 V settings	–	–	±4	%
OTG-specific UVLO hysteresis	T = 0 to 70°C	–	200	–	mV
OTG-specific standby current	See *Current consumption* below	–	–	–	mA
Protection					
VBAT over-voltage lockout	VBAT rising	–	V_FLT + 0.05	–	V
Automatic charger shutdown threshold					
Voltage (falling)					
	DC_SNS - VBAT	120	220	300	mV
	USB_SNS - VBAT	120	180	240	mV
Hysteresis			80	–	mV
Charge inhibit threshold voltage (V_FLT - VBAT)	Four steps, after power applied	50	–	300	mV
Pre-charge timeout accuracy	48 to 191 min settings	–	–	±20	%
Complete charge timeout accuracy	382 to 1527 min settings	–	–	±20	%
System startup holdoff timer					
USB_SNS		200	–	–	msec
DC_SNS		5	10	15	msec
Charger startup holdoff timer, enabled		250	–	–	msec
Battery voltage glitch filter		–	175	–	msec
Watchdog timer					
Option A		–	36	–	sec
Option B		–	18	–	sec
Option C		–	64	–	sec

Table 3-5 Battery charger specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
Charger thermal protection					
Charging current reduction, option A		–	100	–	°C
Charging current reduction, option B		–	110	–	°C
Charging current reduction, option C		–	120	–	°C
Charging current reduction, option D		–	130	–	°C
Shutdown		–	150	–	°C
Shutdown hysteresis		–	20	–	°C
See Table 3-6 for battery thermistor monitoring specifications.					
Low battery (SYSOK output pin)					
Low battery voltage/SYSOK detection					
Threshold range (VBAT falling)	15 programmable steps	2.50	–	3.70	V
Threshold accuracy					
$V_{LOWBATT}$ = 2.8 V		–	–	±1	
$V_{LOWBATT}$ = other settings		–	–	±2	%
Threshold hysteresis (rising)		–	200	–	mV
VCHG analog output					
R = ratio of VCHG to I_CHG	V = I_CHG × 0.84 Ω	–	0.84	–	Ω
VCHG accuracy	T = 0 to 70°C				
I_CHG = 500 mA		-10	–	+10	%
I_CHG = 1000 mA		-8	–	+8	%
I_CHG = 1500 mA		-6	–	+6	%
Charger-specific digital I/O characteristics (different from general characteristics given in Section 3.4)					
High-level input voltage (V_{IH})	All charger digital interface pads except CHG_EN	1.4	–	–	V
Low-level input voltage (V_{IL})		–	–	0.6	V
CHG_EN high-level input voltage (V_{IH})		1.2	–	–	V
CHG_EN low-level input voltage (V_{IL})		–	–	0.4	V
Output low-level (V_{OL}), 3 mA sink	PGOOD_SYSOK, JIG, BOOT, WIPWR_RST_N	–	–	0.3	V
R_{PULL} (push-pull configuration)	PGOOD_SYSOK, VDD = 1.8 V	–	0.5	–	kΩ
Time for KYPD_PWR_N assertion to exit ship mode		–	10	–	ms

Table 3-5 Battery charger specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
Current Consumption					
I_{LEAK} (CHG_EN, USB_CS)	V_IN = 3.3 V	–	–	1.0	µA
Ground current					
Standby (battery) [6]	Input not present, SHDN = H	–	45	70	µA
Shutdown (battery) [6]	Input not present, SHDN = L	–	18	40	µA
Suspend (WiPower source) [7]		–	–	–	mA
Suspend (USB source) [7]		–	–	–	mA
Active					
PFM mode, no load	USB_IN = 5 V, VPH_PWR = 3.6 V	–	6	20	mA
PWM mode, no load [10]	USB_IN = 5 V, VBAT = 4.35 V	–	15	24	mA
OTG-specific standby current (no load)		–	30	40	mA

1. Over-voltage lockout depends on the allowed input adapter type selection. Refer to the *PM8952/PM8956 + PMI8952 Power Management IC Design Guidelines* (80-NT390-5) for more details.
2. ICHG is overridden by the input current limit (ILIM).
3. Go to http://www.usb.org/developers/devclass_docs for USB battery charging specifications 1.1 and 1.2.
4. Charge termination current sensed by charger analog sensor.
5. The oscillator frequency can be programmed to 1.0, 1.5, 2.0, and 3.0 MHz.
6. The battery current specifications are based on simulation for charger module only. For chip level battery current specification, see Table 3-3.
7. See Table 3-3 for USB_IN suspend current consumption.
8. T = -30 to +85°C, DC_SNS or USB_SNS = 5.0 V, V_FLT = 4.2 V, and VBAT = 3.7 V, unless otherwise noted.
9. When VBATT falls below VSYS the corresponding status register indicates a low battery condition.
10. Not 100% production tested. Guaranteed by design and/or characterization.

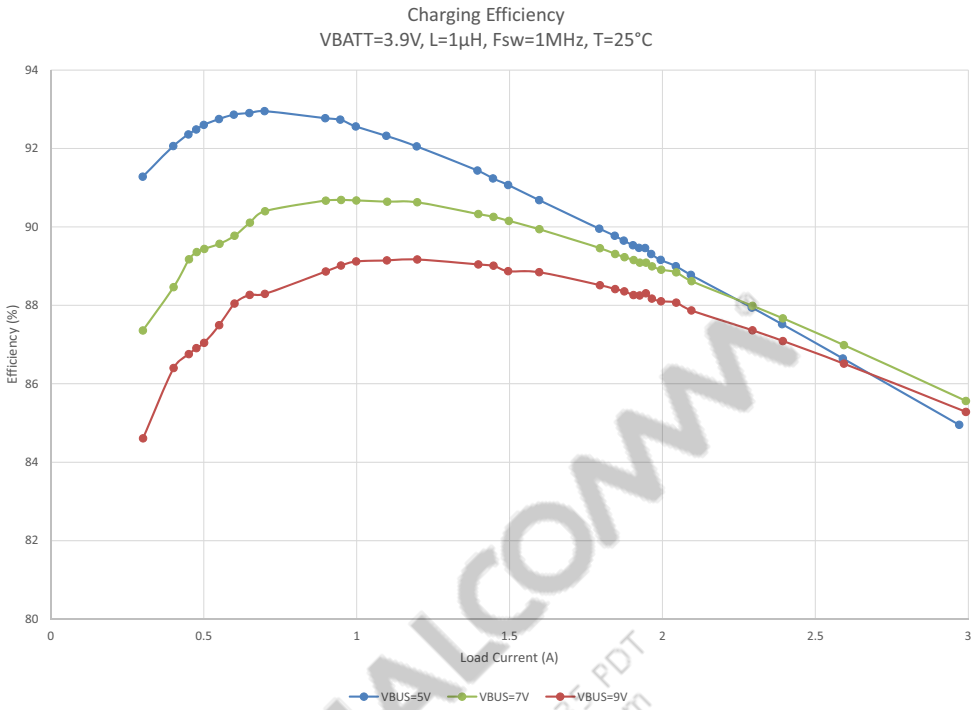


Figure 3-2 USB_IN charging efficiency plot, measured on PMI8952 v2.0

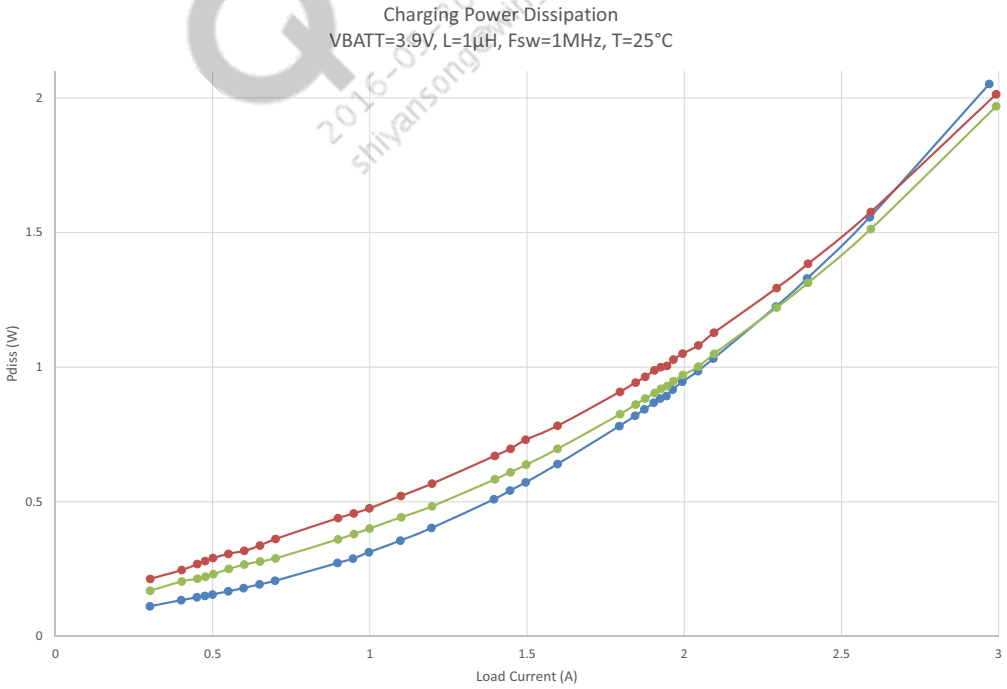


Figure 3-3 USB_IN charging power dissipation plot, measured on PMI8952 v2.0

3.5.2 Fuel gauge

The fuel gauge module offers a hardware based algorithm that is able to accurately estimate the battery's state of charge by utilizing current monitoring and voltage based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.

Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

A low level of interaction with the system is required. A broad range of configuration registers are provided to fit the requirements various applications.

Table 3-6 Fuel gauge performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Battery voltage ADC conversion					
Battery voltage resolution		–	–	15	Bits
Battery voltage LSB		–	152.6	–	µV
Battery voltage conversion time	15 bits conversion	–	163.84	–	ms
Battery voltage input guaranteed range		2.8	–	4.7	V
Battery voltage absolute accuracy	T_{amb} = 25°C 3.4 V < VBATT < 4.4 V No input connected	-0.15	–	0.15	%
	T_{amb} = 0°C to +70°C 3.4 V < VBATT < 4.4 V No input connected	-0.2	–	0.2	%
	T_{amb} = 25°C 3.4 V < VBATT < 4.4 V 5 V USB Input	-0.25	–	0.25	%
	T_{amb} = 0°C to +70°C 3.4 V < VBATT < 4.4 V 5 V USB Input	-0.3	–	0.3	%
Thermistor ADC conversion					
Thermistor voltage resolution	Programmable	9	–	12	Bits
Thermistor voltage input range	% of RBIAS	0	–	91.2	%
Thermistor voltage LSB	VRBIAS = 2.7 V	659	–	5273	µV
Thermistor voltage absolute accuracy	$T_{junction}$ =- 20°C to +70°C VRBIAS = 2.7 V VBAT_THERM > 1 V	-1.33	–	1.33	%
	$T_{junction}$ = -20°C to +70°C VRBIAS = 2.7 V VBAT_THERM < 1 V	-13.3	–	13.3	mV
Supported thermistor value range		10	–	100	kΩ

Table 3-6 Fuel gauge performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Unit
Supported thermistor accuracy		–	0.50	–	%
Supported thermistor beta value range		3200	–	4400	
Supported thermistor capacitor value	R_{BATT_THERM} = 10 k	–	4.7	–	µF
Recommended thermistor capacitor value		–	0	–	µF
Battery temperature measurement accuracy	T_{Batt} = -0°C to +50°C Therm accuracy = 0.8% Ibatt < 50 mA Thermistor β = 3200	-2	–	2	°C
	T_{Batt} = -20°C to +60°C Therm accuracy = 0.8% Ibatt < 50 mA Thermistor β = 3200 Thermistor value = 68 K	-3	–	3	°C
Time between updates		1.47	–	392	s
Biasing voltage value	T_{amb} = 25°C During ADC conversion	–	2.7	–	V
Biasing voltage variation	T_{amb} = 0°C to +70°C During ADC conversion	-10	–	10	%
Battery ID ADC conversion					
Battery ID voltage reading resolution		–	9	–	Bits
Battery ID voltage reading LSB		–	9.8	–	mV
Battery ID voltage reading conversion time		–	2.6	–	ms
Battery ID voltage reading input range	VAA= 2.7 V	0	–	2.5	V
Battery ID voltage reading gain accuracy	T_{amb} =0°C to +70°C BATTID > 1 V	-1.96	±0.98	1.96	%
Battery ID voltage reading offset	T_{amb} =0°C to +70°C BATTID < 1 V	-19.6	–	19.6	mV
Current ADC conversion– external sensing resistor					
Battery current resolution	Sign + N bits	–	15	–	N Bits
Battery current input voltage range		-50	–	50-LSB	mV
Battery current input voltage LSB		–	1.5	–	µV
Conversion time		–	163	–	ms
Battery current accuracy	T = 0°C to +70°C 4.4 V ≥ Vbatt ≥ 3.0 V | IBATT | > 1 A	-1.5	–	1.5	%
	T =0°C to +70°C 4.4 V ≥ Vbatt ≥ 3.0 V | IBATT | < 1 A	-15	–	15	mA
Termination current accuracy	T = 0°C to +70°C VBATT = 4.4 V IBATT = -0.3 A	-15	–	15	mA
Current sensing resistor	Supported values	–	10	–	mΩ

Table 3-6 Fuel gauge performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Unit
Minimum required accuracy	Supported values	–	0.5	1	%
Battery current LSB	10 mΩ RSENSE	–	152.6	–	µA
Battery current guaranteed range	10 mΩ RSENSE	-5.0	–	5.0	A
Battery voltage conversion time	N bits = 15	–	163	–	ms
Current ADC conversion– internal current sense					
Battery current resolution	Sign + N bits	–	15	–	N Bits
Battery current accuracy	T = 0°C to +70°C VBATT = 3.4 to 4.4 V VSYS_MIN = 3.0 V | IBATT | > 1 A No OTG	-7	–	7	%
	T =0°C to +70°C VBATT = 3.4 to 4.4 V VSYS_MIN = 3.0 V | IBATT | < 1 A No OTG	-70	–	70	mA
Termination current accuracy	T = 0°C to +70°C VBATT = 4.4 V IBATT = -0.3 A	-40	–	40	mA
Battery current LSB		–	152.6	–	µA
Battery current guaranteed range		-5.0	–	5.0	A
Battery current conversion time	N bits = 15	–	163	–	ms
Online ESR estimation					
Low pulldown value	T_{amb} =0 °C to +70°C	–	60	–	mA
Med-low pulldown value	T_{amb} =0 °C to +70°C	–	120	–	mA
Med-high pulldown value	T_{amb} =0 °C to +70°C	–	180	–	mA
High pulldown value	T_{amb} =0 °C to +70°C	–	240	–	mA
Battery ID bias current					
Bias current value		–	150	–	µA
Bias current tolerance	T_{amb} =0 °C to +70°C	-4	–	4	%
Bias current value		–	15	–	µA
Bias current tolerance	T_{amb} =0 °C to +70°C	-6	–	6	%
Bias current value		–	5	–	µA
Bias current tolerance	T_{amb} =0 °C to +70°C	-8	–	8	%
Battery ID capacitor (optional)					
Optional capacitor in parallel with battery ID	BATT_ID_res = 1 k to 15 k	–	10	47	nF
	BATT_ID_res = 19 K to 140 k	–	4.7	10	nF
	BATT_ID_res = 240 k to 450 k	–	0.470	1	nF

Table 3-6 Fuel gauge performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Unit
Current consumption					
Peak instantaneous FG current consumption	Fuel gauge is measuring both VADC and IADC	–	1000	–	µA
Estimated FG module average current consumption during sleep	PMI sleep asserted FG in Active2_Sleep8 mode	–	30	–	µA
FG rock bottom sleep current	PMI sleep asserted	10	–	–	µA

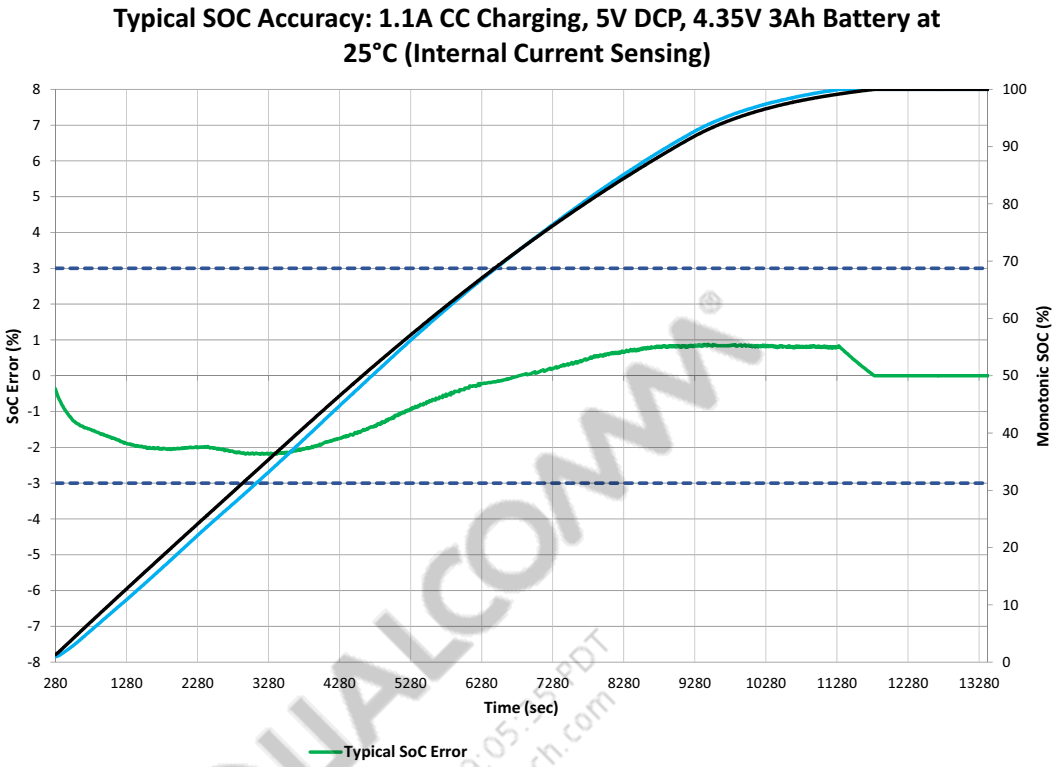


Figure 3-4 Typical SOC accuracy (charging)

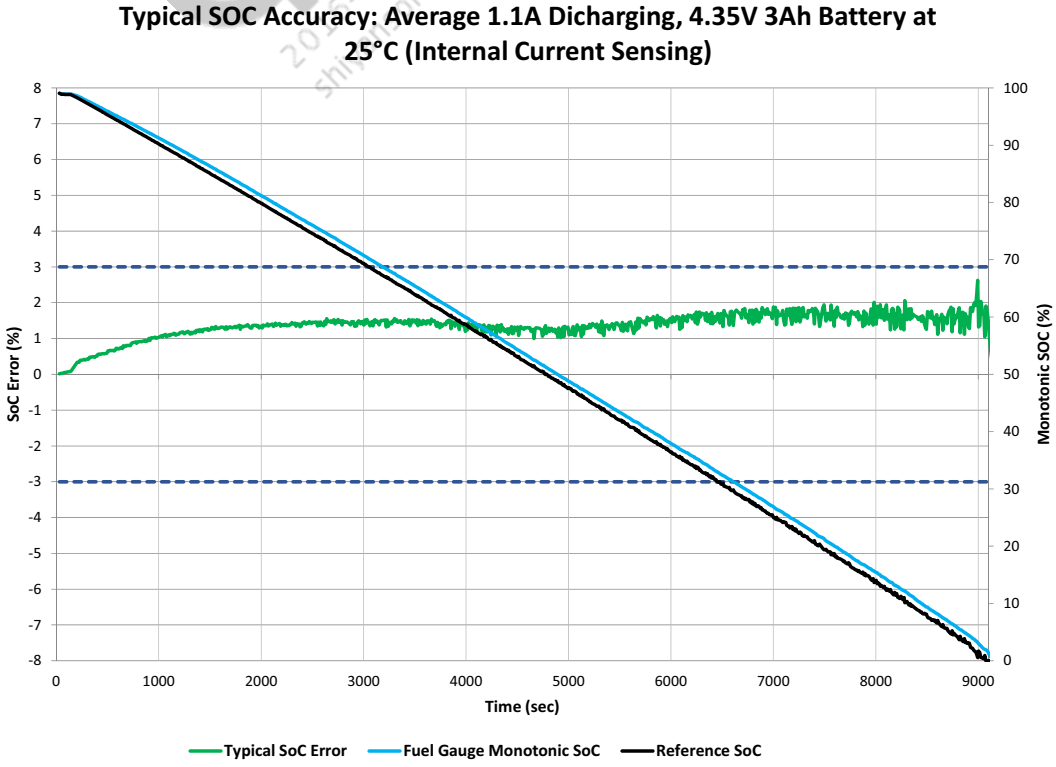


Figure 3-5 Typical SOC accuracy (discharging)

3.5.2.1 Battery serial interface

Battery serial interface implements the physical layer of MIPI battery interface (BIF) to connect either low cost or smart battery pack. When interfaced with a smart battery, BSI enables a single wire serial interface which allows digital communication between mobile device (host) and battery (slave) over battery communication line (BCL) or battery ID (BATT_ID) line. The purpose of BIF is to provide a method to communicate battery characteristics information to ensure safe and efficient charging control under all operating conditions. The SW detects if a smart battery is connected and enables digital communication over BCL. BIF also provides battery authentication through digital unique ID (UID) so that host device can take appropriate action when an unauthorized battery is connected to the phone.

Table 3-7 BSI performance specifications

Parameter	Comments [1]	Min	Typ	Max	Unit
MIPI-BIF I/O electrical specifications					
BCL logic high or idle voltage	R_ID = 240 to 450 kΩ, I_PU = 5 µA	1.2	–	2.25	V
BCL logic low voltage	R_ID = 450 Ω	–	–	0.1	V
Internal ID pull-up current source - See Table 3-6 for battery ID specifications					
Internal fast pull-up resistor		7	9	11	kΩ
BCL idle DC voltage for low cost battery	R_ID = 19.6 to 140 kΩ				
Programmable range		0.294	–	2.1	V
Accuracy		–	–	±4	%
MIPI-BIF I/O timing specifications for smart battery					
BIF time base range	Based on SW programming	2	–	150	µs
Rise time	0 to 1.1 V, R_ID = 240 kΩ, C_BCL = 50 pF	–	–	500	ns
Fall time	VOH_BCL(max) to 0.1, R_ID = 450 kΩ, C_BCL = 50 pF	–	–	50	ns
MIPI-BIF timing specifications for battery removal detection					
Battery removal de-bounce filter time	SW programmable, 31 µs step (32 kHz sleep clock)				
Programmable range		0	–	1	ms
Accuracy		–	–	±16	%

1. T = -30 to +85°C, +2.7 V < VBAT < +4.5 V, unless otherwise noted. All voltages are relative to GND.

3.6 General housekeeping

General housekeeping performance specifications are split into four functional categories as defined within its block diagram (Figure 3-6).

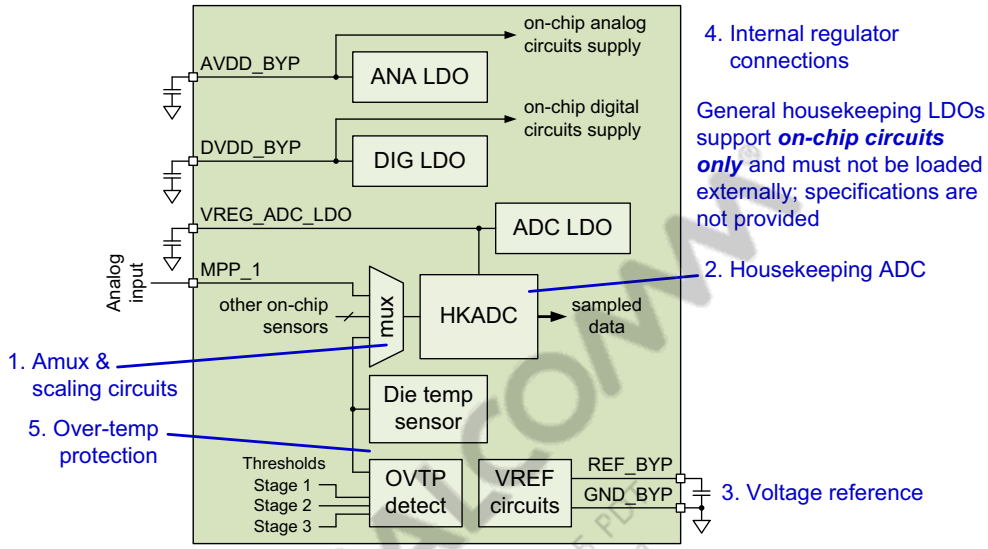


Figure 3-6 General housekeeping functional block diagram

3.6.1 Analog multiplexer and scaling circuits

Analog switches, multiplexers, and voltage-scaling circuits select and condition a single analog signal for routing to the on-chip HKADC. Available multiplexer and scaling functions are summarized in Table 3-8.

Table 3-8 Analog multiplexer and scaling functions

Ch #	Description	Typical input range (V) [2]	Scaling	Typical output range (V)
0	USB_IN	3 to 10	1/20	0.15 to 0.50
1	DS_SNS	3 to 10	1/20	0.15 to 0.50
3	VCHG	–	1/3	–
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
13	Charger temperature monitor	0.4 to 0.9	1	0.4 to 0.9
14	GND_REF	Direct connection to ADC for calibration		
15	VDD_ADC	Direct connection to ADC for calibration		
16	MPP_1	0.05 to 1.5	1	0.05 to 1.5
32	MPP_1	0.3 to VPH_PWR	1/3	0.1 to 1.70
67	USB_DP	0.3 to VPH_PWR	1/3	0.1 to 1.70
68	USB_DM	0.3 to VPH_PWR	1/3	0.1 to 1.70
255	Module power off [1]	–	–	–

1. Channel 255 should be selected when the analog multiplexer is not being used; this prevents the scalers from loading the inputs.
2. Input voltage must not exceed the ADC reference voltage generated by VREG_ADC_LDO (1.8 V).

NOTE Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-9.

Table 3-9 Analog multiplexer performance specifications

Parameter	Comments [2]	Min	Typ	Max	Units
Operational input voltage (Vadc)	Connected internally to VREG_ADC	–	1.8	–	V
Output voltage range					
Full specification compliance		0.10	–	Vadc – 0.10	V
Degraded accuracy at edges		0.05	–	Vadc – 0.05	V
Input referred offset errors					
Channels with x1 scaling		–	–	±2.0	mV
Channels with 1/3 scaling		–	–	±1.5	mV
Channels with 1/20 scaling		–	–	±2.0	mV
Gain errors, including scaling	Excludes VREG_ADC output error				
Channels with x1 scaling		–	–	±0.20	%
Channels with 1/3 scaling		–	–	±0.15	%
Channels with 1/20 scaling		–	–	±0.28	%
Integrated nonlinearity (INL)	Input referred to account for scaling	–	–	±3	mV
Input resistance	Input referred to account for scaling				
Channels with x1 scaling		10	–	–	MΩ
Channels with 1/3 scaling		1	–	–	MΩ
Channels with 1/20 scaling		0.77	–	–	MΩ
Channel-to-channel isolation	1 V AC input at 1 kHz	50	–	–	dB
Output settling time [1]	C_{load} = 28 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	$\mu V/Hz^{1/2}$

1. The AMUX output and a typical load is modeled in Figure 3-8. After S1 closes, the voltage across C2 settles within the specified settling time.

2. Multiplexer offset error, gain error, and INL are measured as shown in Figure 3-7. Supporting comments:
   - The non-linearity curve is exaggerated for illustrative purposes.
   - Input and output voltages must stay within the ranges stated in Table 3-8; voltages beyond these ranges result in nonlinearity, and are beyond specification.
   - Offset is determined by measuring the slope of the endpoint line (m) and calculating its Y-intercept value (b):
     Offset = b = $y_1 - m \cdot x_1$
   - Gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage):
     Gain_error = [(slope of endpoint line)/(slope of ideal response) - 1]·100%
   - INL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:
     INL(min) = min[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
     INL(max) = max[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]

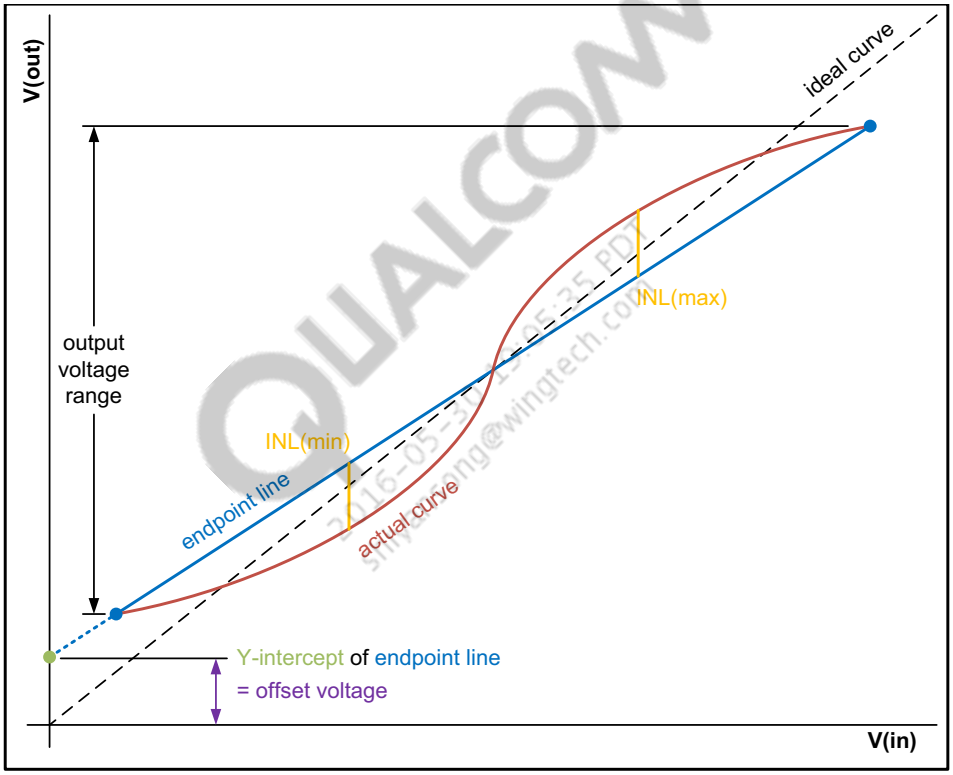


Figure 3-7 Multiplexer offset and gain errors

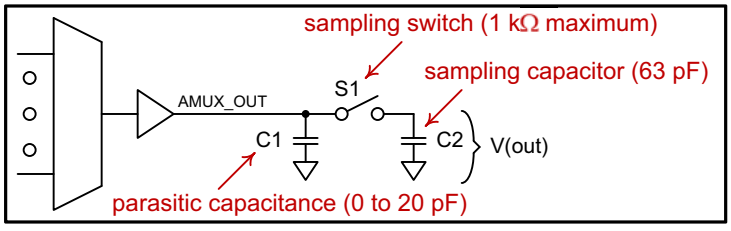


Figure 3-8 Analog multiplexer load condition for settling time specification

3.6.2 HKADC circuit

Any of the four multipurpose pins can be used as an ADC input. Their input voltages must not exceed the ADC's reference voltage (1.8 V, generated by the on-chip ADC LDO). HKADC performance specifications are listed in Table 3-10.

Table 3-10 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Operational input voltage	Connected to internal LDO	–	1.8	–	V
Resolution		–	–	15	bits
Analog-input bandwidth		–	100	–	kHz
Sample rate	CLK_IN/8	–	2.4	–	MHz
Offset error	Relative to full-scale	–	–	±1	%
Gain error	Relative to full-scale	–	–	±1	%
INL	15-bit output	–	–	±8	LSB
DNL	15-bit output	–	–	±4	LSB

3.6.3 Reference circuit

All PMIC regulator circuits, and some other internal circuits, are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a low-pass function that filters the reference voltage distributed throughout the device.

NOTE Do not load the REF_BYP pin. Use an MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage reference performance specifications are given in Table 3-11.

Table 3-11 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF	At REF_BYP pin	–	1.25	–	V
Output voltage deviations					
Normal operation	Over temperature only, -20 to +120ºC	–	–	±0.32	%
Normal operation	All operating conditions	–	–	±0.50	%
Sleep mode	All operating conditions	–	–	±1.00	%

3.6.4 Internal voltage-regulator connections

Some regulator supply voltages and/or outputs are connected internally to power other PMIC circuits. These circuits will not operate properly unless their the source voltage regulators are

enabled and set to their proper voltages. These requirements are summarized in Table 3-12.

Table 3-12 Internal voltage regulator connections

Voltage supply or regulator output	Default	Supported circuits
VDD_MSM_IO	1.8 V	GPIOs and MPPs; SPMI
VPH_PWR	3.6 V	MPPs
VREG_ADC_LDO	1.8 V	AMUX/HKADC (dedicated; do not alter)

3.6.5 Over-temperature protection (smart thermal control)

The PMIC includes over-temperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions.
- Stage 1 – 90 to 100°C (configurable threshold); an interrupt is sent to the modem IC without shutting down any PMI circuits.
- Stage 2 – 100 to 130°C (configurable threshold); an interrupt is sent to the modem IC and unnecessary high-current circuits are shut down. Charger reduces charging current.
- Stage 3 – greater than 150°C; an interrupt is sent to the modem IC, and the PMI is completely shut down.

Temperature hysteresis is incorporated, such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMI will power up immediately.

3.7 User interfaces

User interfaces performance specifications are split into six functional categories as defined within its block diagram (Figure 3-9).

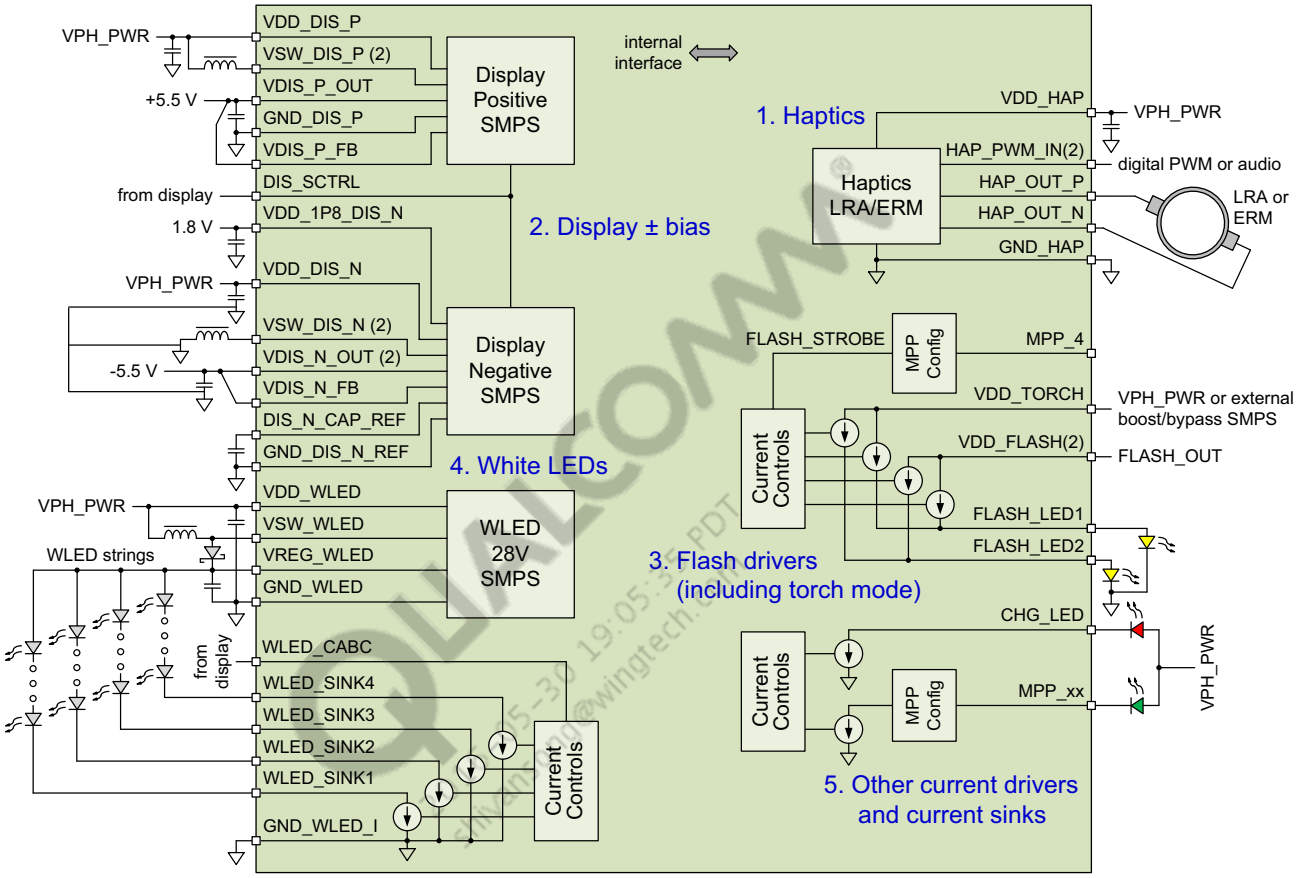


Figure 3-9 User interfaces functional block diagram

3.7.1 Haptics

Haptics uses vibration to communicate an event or action through human touch. In a mobile phone, haptics is used to simulate the feeling of a real mechanical key by providing tactile feedback to the user as confirmation of touchscreen contact, or dynamic feedback to enhance the user's gaming experience. Pertinent performance specifications are listed in Table 3-13.

Table 3-13 Haptics performance specifications

Parameter	Comments [3]	Min	Typ	Max	Units
Operational input voltage	Connected at VDD_HAP (VH below)	2.50	3.6	4.75	V
Output voltage [1]					
Peak, no load	At HAP_OUT_P and HAP_OUT_N	–	–	VH	V
Average (V_HA)	Differential, over one PWM cycle	0	–	3.6	V
Maximum drive [2]	Differential, over one PWM cycle	1.2	–	3.6	V
Accuracy	Duty cycle ≤ 95%	–	50	–	mV
Output current limit	Cycle-to-cycle limit				
R_ERM or R_load = 20 Ω		300	400	500	mA
R_ERM or R_load = 10 Ω		600	800	1000	mA
On resistance					
R_ON_P	High side switch	0.25	0.50	1.25	Ω
R_ON_N	Low side switch	0.25	0.50	1.25	Ω
Internal PWM frequency					
Programmable options	253 kHz, 505 kHz, 739 kHz, 1076 kHz	253	503	1076	kHz
Accuracy		–	–	±16	%
LRA resonance					
Programmable period	5 µs (±16% due to internal oscillator) steps	3.33	–	20	ms
Accuracy	Auto resonance detection	–	–	10	µs
LRA self resonance capture		–	±20	–	Hz
HAP_PWM_IN voltage		0	–	1.8	V
Start-up time	Enable to full output drive voltage	–	–	100	µs
Ground current					
Active		–	3.0	–	mA
Shutdown		–	1.0	–	µA

1. Output voltage is programmable in steps of 116 mV. 'VH' = VDD_HAP (3.6 V typical).
2. VDD_HAP > V_HA + I_out x (R_ON_P + R_ON_N).
3. All specifications apply at VDD_HAP = 3.6 V, T = -30 to +85ºC, and F_pwm = 505 kHz, unless noted otherwise.

3.7.2 Display ± bias

The PMIC generates the plus and minus bias voltages for LCD and AMOLED displays; pertinent performance specifications are listed in Table 3-14 and Table 3-15, respectively.

Table 3-14 Display plus bias performance specifications

Parameter	Comments	Min	Typ	Max	Units
Specifications for LCD applications [1]					
Operational input voltage	Connected at VDD_DIS_P	2.50	–	4.75	V
Output voltage (VDIS_P_OUT)	Programmable				
Range, no load to 150 mA		5.0	5.5	6.1	V
Resolution		–	100	–	mV
Total output voltage variation	V_out = 5.0 to 6.0 V, I_load = 50 mA	–	–	±50	mV
Output current		–	–	150	mA
Load regulation	I_load = 10 to 150 mA; V_out = 5.5 V	–	1	2	mV
Line regulation	VDD = 2.5 to 4.75 V; I_load = 50 mA; V_out = 5.5 V	–	1	2	mV
Load transient	I_out = 3 to/from 30 mA in 150 µs	–	±20	–	mV
Line transient	VDD = 3.6 to/from 3.1 V in 10 µs; I_out = 50 mA	–	±20	–	mV
Output ripple	V_out = 5.5 V; F_sw = 1.6 MHz				
Disabled pulse skipping	I_out = 5 mA	–	10	–	mV
Enabled pulse skipping	I_out = 5 mA	–	15	–	mV
Efficiency	I_out = 30 mA	–	92	–	%
Switching frequency (default)		–	1.6	–	MHz
Discharge resistance					
Fast discharge		–	70	–	Ω
Slow discharge		–	140	–	Ω
NFET minimum on-time		–	40	–	ns
Soft start time (no load)	VDD = 3.6 V, V_out = 0 to 6.1 V	–	400	–	µs
Output slew time, 100 mV step	V_out_new = 0.9 × V_out_old	–	50	–	µs
Short circuit protection					
Threshold	VDD - V_out	–	0.6	–	V
Debounce	2 (default), 4, 16, or 32 µs	–	2	–	µs
Ground current					
Active, no load	VDD = 2.5 to 4.75 V, Vout = 5.5 V, pulse skipping active	–	500	1000	µA
Shutdown		–	–	1.0	µA

Table 3-14 Display plus bias performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Specifications for AMOLED applications [2]					
Operational input voltage	Connected at VDD_DIS_P	2.50	–	4.75	V
Output voltage (VDIS_P_OUT)	Programmable				
Range, no load to 350 mA	VDD = 2.5 to 4.75 V	4.6	–	5.0	V
Resolution		–	100	–	mV
Total output voltage variation	VDD = 2.5 to 4.75 V, V_out = 4.6 V, I_load = 150 mA, T = 0°C to 85°C	–	–	±0.8	%
Output current		–	–	350	mA
Load regulation	I_load = 10 to 350 mA	–	1	5	mV
Line regulation	VDD = 2.5 to 4.75 V at I_load = 150 mA	–	1	5	mV
Load transient	I_out = 30 to/from 300 mA in 150 μs	–	±20	–	mV
Line transient	VDD = 3.6 to/from 3.1 V in 10 μs; I_out = 150 mA	–	±30	–	mV
Output ripple	V_out = 4.6 V; F_sw = 1.6 MHz				
Disabled pulse skipping	I_out = 150 mA	–	10	–	mV
Enabled pulse skipping	I_out = 5 mA	–	15	–	mV
Efficiency	I_out = 150 mA	–	94	–	%
Switching frequency (default)		–	1.6	–	MHz
Discharge resistance					
Fast discharge		–	70	–	Ω
Slow discharge		–	140	–	Ω
NFET minimum on-time		–	40	–	ns
Soft start time (no load)	Programmable range and nominal, 200 μs step; VDD = 3.6 V, V_out = 0 to 6.1 V	–	400	–	μs
Output slew time, 100 mV step	V_out_new = 0.9 × V_out_old	–	50	–	μs
Short circuit protection					
Threshold	VDD - V_out	–	0.6	–	V
Debounce	2 (default), 4, 16, or 32 μs	–	2	–	μs
Ground current					
Active, no load	VDD = 2.5 to 4.75 V, Vout = 4.6 V, pulse skipping active	–	500	1000	μA
Shutdown		–	–	1.0	μA

1. All specifications apply at VDD_DIS_x = 3.6 V, F_sw = 1.6 MHz, T = -30 to +85ºC, VDIS_P_OUT = 5.5 V, L = 4.7 μH, and C = 10 μF (capacitance value de-rated from 22 μF nominal), unless noted otherwise.
2. All specifications apply at VDD_DIS_x = 3.6 V, F_sw = 1.6 MHz, T = -30 to +85ºC, VDIS_P_OUT = 4.6 V, L = 4.7 μH, and C = 10 μF (capacitance value de-rated from 22 μF nominal), unless noted otherwise.

Table 3-15 Display minus bias performance specifications

Parameter	Comments	Min	Typ	Max	Units
Specifications for LCD applications [1]					
Operational input voltage	Connected at VDD_DIS_N	2.50	3.6	4.75	V
Output voltage (VDIS_N_OUT) Range, no load to 100 mA Resolution	Programmable	 -1.4 –	 – 100	 -6.0 –	 V mV
Total output voltage variation	V_out = -5.0 to -6.0 V, I_load = 50 mA	–	–	±60	mV
Output current		–	–	150	mA
Load regulation	I_load = 10 to 150 mA	–	10	–	mV
Line regulation	VDD = 2.5 to 4.75 V at I_load = 50 mA	–	10	–	mV
Load transient	I_out = 3 to/from 30 mA in 150 µs	–	±20	–	mV
Line transient	VDD = 3.6 to/from 3.1 V in 20 µs; I_out = 50 mA	–	±20	–	mV
Output ripple Disabled pulse skipping Enabled pulse skipping	V_out = -5.5 V; F_sw = 1.6 MHz I_out = 50 mA I_out = 5 mA	 – –	 10 30	 – –	 mV mV
Efficiency	I_out = 50 mA	–	84	–	%
Switching frequency (default)	Programmable	–	1.48	–	MHz
Discharge resistance Fast discharge Slow discharge		 – –	 50 100	 – –	 Ω Ω
Power-up/power-down delay [2]	Programmable range, 8 ms default	1	–	8	ms
Soft start time (no load)	0–90% of VREG_DISN, C_ext = 47 nF	–	1.0	–	ms
Short circuit protection Threshold Debounce	 V_out - VDD 2, 4 (default), 16, or 32 µs	 – –	 0.6 4	 – –	 V µs
Ground current Active, no load Shutdown	 VDD = 2.5 to 4.75 V V, Vout = -5.5 V, pulse skipping active	 – –	 600 –	 1200 1.0	 µA µA
Specifications for AMOLED applications [3]					
Operational input voltage	Connected at VDD_DIS_N	2.50	3.6	4.75	V
Output voltage (VDIS_N_OUT) Range Resolution	Programmable VDD = 2.5 to 4.75 V	 -1.4 –	 – 100	 -5.4 –	 V mV
Total output voltage variation	VDD = 2.5 to 4.75 V, V_out = -1.4 to -4.4 V, I_load = 150 mA	–	–	±60	mV

Table 3-15 Display minus bias performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Output current	V_out = -4.0 V				
VPH_PWR = 2.85 to 4.75 V		–	–	350	mA
VPH_PWR = 2.65 to 4.75 V		–	–	300	mA
VPH_PWR = 2.50 to 4.75 V		–	–	250	mA
Load regulation	I_load = 10 to 350 mA	–	–	10	mV
Line regulation	VDD = 2.5 to 4.75 V at I_load = 150 mA	–	–	10	mV
Load transient	Transition in 150 µs				
I_out = 10 to/from 100 mA		–	±25	–	mV
I_out = 30 to/from 300 mA		–	±40	–	mV
Line transient	VDD = 3.6 to/from 3.1 V in 20 µs; I_out = 150 mA	–	±20	–	mV
Output ripple					
Disabled pulse skipping	I_out = 50 mA	–	10	–	mV
Enabled pulse skipping	I_out = 5 mA	–	30	–	mV
Efficiency	I_out = 50 mA	–	84	–	%
Switching frequency (default)		–	1.48	–	MHz
Discharge resistance					
Fast discharge		–	50	–	Ω
Slow discharge		–	100	–	Ω
Power-up/power-down delay	Programmable range, 8 ms default	1	–	8	ms
Soft start time (no load)	0-90% of VREG_DISN, C_ext = 1.5 nF	–	1.0	–	ms
Short circuit protection					
Threshold	GND - V_out	–	0.6	–	V
Debounce	2, 4 (default), 16, or 32 µs	–	4	–	µs
Output slew time, 100 mV step	V_out_new = 0.9 × V_out_old; C_ref = 1.5 nF; t_slew = 3 × (300 kΩ × C_ref)	–	1.35	–	ms
Ground current					
Active, no load	VDD = 2.5 to 4.75 V, Vout = -4.4 V, pulse skipping active	–	600	1200	µA
Shutdown		–	–	1.0	µA

1. All specifications apply at VDD_DIS_x = 3.6 V, T = -30 to +85ºC, VDIS_N_OUT = -5.5 V, L = 4.7 µH, C = 10 µF (capacitance value de-rated from 22 µF nominal), and F_sw = 1.48 MHz, unless noted otherwise.
2. Power-up delay is defined as the time from when VREG_DISP has reached steady state (~90% of final value) to when VREG_DISN is enabled during power-up. Power-down delay is defined as the time from when VREG_DISN has discharged (to < ~| 500 mV |) to when VREG_DISP is disabled during power-down.
3. All specifications apply at VDD_DIS_x = 3.6 V, T = -30 to +85ºC, VDIS_N_OUT = -2.4 V, L = 4.7 µH, C = 10 µF (capacitance value de-rated from 22 µF nominal), and F_sw = 1.48 MHz, unless noted otherwise.

3.7.3 Flash drivers (including torch mode)

This high current (2.0 A) driver supports different input sources for flash and torch modes, works in various concurrency scenarios, and allows different LED configurations. Pertinent performance specifications are listed in Table 3-16.

Table 3-16 Flash and torch LED driver performance specifications

Parameter	Comments [2]	Min	Typ	Max	Units
Driver input voltage					
VDD_FLASH	Expected source is FLASH_OUT				
Flash disabled		2.5	–	10	V
Flash enabled		–	–	5.8	V
VDD_TORCH		–	3.6	5.5	V
Output current per LED					
Flash		–	–	1000	mA
Torch		–	–	200	mA
Output current steps	Both flash and torch modes	–	12.5	–	mA
Absolute current accuracy	VPH_PWR = 3.0 V to 4.75 V				
Each flash LED ≥ 100 to 1000 mA	VDD_FLASH = V_LED + (0.5 to 1.5 V)	–	–	±8.5	%
Each torch LED ≥ 12.5 to 200 mA	VDD_TORCH = V_LED + (0.5 to 1.5 V)	–	–	±7	%
LED current matching accuracy [1]	VDD_FLASH = V_LED + (0.5 to 1.5 V);				
Each LED = 0.1 - 1.0 A	VDD_TORCH = V_LED + (0.5 to 1.5 V)	–	–	+7	%
Current regulator dropout voltage	VDD – V_LED; range and default		500		mV
Detection thresholds					
Short circuit	Current output enabled	–	1.0	–	V
Open circuit (VDD – V_LED)	Current output enabled	–	100	–	mV
VDD droop	Programmable range and default; 0.1 V step	2.5	3.1	3.2	V
Timers					
Flash max-on safety	Programmable range (10 ms steps)	10	–	1280	ms
Video watchdog	Programmable range (1 sec steps)	2	–	33	sec
Deglitch	For flash strobe, mask 1/2/3, VDD, and fault	0	–	128	µs
Current ramp					
Step, LED current 0 to 1000 mA		–	12.5	–	mA
Step duration		0.2	6.7	27	µs
Current derating					
Threshold (junction temperature)	Programmable range, default	95	105	125	°C
Slope	Programmable range, 2.0 default	1	5	5	%/°C
Ground current					
Off state	VDD_FLASH ≤ 9 V, VDD_TORCH ≤ 5 V, V_LED = 0 V	–	0.25	2	µA

1. I_LED matching accuracy is determined by the following formula: abs(max(I1 - I2)) / (1/2 sum(I1:I2))
2. All specifications apply at VPH_PWR = 3.6 V, T = -30 to +85ºC, unless noted otherwise.

3.7.4 White LEDs

White LEDs (WLED) generate backlighting for the handset's LCD. The PMIC supports WLEDs with a boost converter that generates the high voltage needed for powering a string of WLEDs, plus four output drivers for sinking the current from WLED strings. Brightness can be controlled via SPMI or externally via content adaptive backlight control (CABC). Other useful features include over-voltage protection, over-current protection, soft-start, and adaptive output voltage (as the WLED forward-voltage drop changes with temperature, the boost output voltage changes appropriately). Pertinent performance specifications are listed in Table 3-17.

Table 3-17 WLED boost converter and driver performance specifications

Parameter	Comments [2]	Min	Typ	Max	Units
Common to boost converter and current drivers					
Operational input voltage	VPH_PWR	2.5	–	4.75	V
Input voltage for full brightness	I_led = 20 mA per string				
2 strings (~16 WLEDs)	V_out = 28 V across panel	2.8	–	–	V
4 strings (~28 WLEDs)	V_out = 24 V across panel	3.6	–	–	V
Boost converter					
Output voltage		6.0	–	28.5	V
Over-voltage protection (OVP)	Programmable, 4 settings				
30.0 V setting		29.3	31	31.7	V
29.5 V setting		28.8	29.5	30.3	V
19.5 V setting		18.7	19.4	20.1	V
18.0 V setting		17.1	17.8	18.5	V
Hysteresis	29.5 V OVP setting	–	1.1	–	V
Over-current protection	Programmable, set to 980 mA	830	980	1200	mA
Switching frequency		0.6	0.8	1.6	MHz
Efficiency	VDD = 3.6 V, 25°C, F_sw = 0.8 MHz				
Peak	I_out = 15 mA/string (x4), 13.5 V out	–	86	–	%
Average	I_out = 5 to 25 mA/string (x4)	–	80	–	%
Light load	I_out = 1 to 5 mA/string (x4); PSM en	–	75	–	%
Current sinks [1]					
Full-scale current range	Programmable range, 2.5 mA step	0	–	30	mA
Absolute accuracy, hybrid dimming	Combined CABC duty cycle and internal dimming control; I_led = 30 mA/string full-scale; headroom = 0.4 V; VPH_PWR = 2.50 to 4.75 V				
100% setting		-2.1	–	+5.2	%
50% setting		-3.5	–	+3.0	%
25% setting		-3.5	–	+2.5	%
10% setting		-6.5	–	+4.5	%
5% setting		-12.0	–	+8.0	%
2% setting		-12.5	–	+8.0	%
1% setting		-15.5	–	+12.0	%
0.4% setting		-18.0	–	+14.5	%

Table 3-17 WLED boost converter and driver performance specifications (cont.)

Parameter	Comments [2]	Min	Typ	Max	Units
Matching accuracy, hybrid dimming	Any 2 strings; combined CABC duty cycle and internal dimming control; I_led = 30 mA/string full-scale; headroom = 0.4 V; VPH_PWR = 2.50 to 4.75 V				
100% setting		–	–	3.0	%
50% setting		–	–	3.2	%
25% setting		–	–	3.6	%
10% setting		–	–	6.0	%
5% setting		–	–	10.0	%
2% setting		–	–	10.0	%
1% setting		–	–	12.5	%
0.4% setting		–	–	12.5	%
Absolute accuracy, analog dimming	Combined CABC duty cycle and internal dimming control; I_led = 30 mA/string full-scale; headroom = 0.4 V; VPH_PWR = 2.50 to 4.75 V				
100% setting		-2.1	–	+5.2	%
50% setting		-3.5	–	+3.0	%
25% setting		-3.5	–	+2.5	%
10% setting		-6.5	–	+4.5	%
5% setting		-11.0	–	+13.5	%
2% setting		-30.0	–	+40.0	%
1% setting		-65.0	–	+75.0	%
Matching accuracy, analog dimming	Any 2 strings; CABC duty cycle control only; I_led = 30 mA/string full-scale; headroom = 0.4 V; VPH_PWR = 2.50 to 4.75 V				
100% setting		–	–	2.5	%
50% setting		–	–	2.5	%
25% setting		–	–	3.5	%
10% setting		–	–	5.5	%
5% setting		–	–	12.0	%
2% setting		–	–	30.0	%
1% setting		–	–	70.0	%
Absolute accuracy, digital dimming	Combined CABC duty cycle and internal dimming control; I_led = 30 mA/string full-scale; headroom = 0.4 V; VPH_PWR = 2.50 to 4.75 V; F_PWM = 2.34 kHz				
100% setting		-1.2	–	+4.3	%
50% setting		-1.2	–	+4.3	%
25% setting		-1.2	–	+4.3	%
10% setting		-1.6	–	+4.3	%
5% setting		-4.0	–	+2.0	%
2% setting		-6.0	–	+0.0	%
1% setting		-6.0	–	+1.5	%
0.4% setting		-10.0	–	+3.0	%
Matching accuracy, digital dimming	Any 2 strings; combined CABC duty cycle and internal dimming control; I_led = 30 mA/string full-scale; headroom = 0.4 V; VPH_PWR = 2.50 to 4.75 V; F_PWM = 2.34 kHz				
100% setting		–	–	3.0	%
50% setting		–	–	3.0	%
25% setting		–	–	3.0	%
10% setting		–	–	3.0	%
5% setting		–	–	3.0	%
2% setting		–	–	3.0	%
1% setting		–	–	3.5	%
0.4% setting		–	–	5.0	%

Table 3-17 WLED boost converter and driver performance specifications (cont.)

Parameter	Comments [2]	Min	Typ	Max	Units
CABC frequency		20	20	40	kHz
CABC duty cycle	WLED is regulating, no flicker, no visual artifacts, no segment switching, hybrid dimming is enabled	0.4	–	100	%
Ground current	All current sinks are disabled				
Pulse skipping enabled, no load		–	0.5	–	mA
Force PFM, no load		–	0.5	–	mA
Leakage into switch node	VSW_WLED = 30 V, device is disabled	–	0.2	–	μA
Leakage into current sink input	WLED_x = 10 V, device is disabled	–	0.01	–	μA
AMOLED MODE					
Operational input voltage	Module operational range	2.5	–	4.75	V
Output voltage (six options)	Software programmable range	5.58	7.56	7.84	V
DC accuracy	Vph_pwr = 2.5–4.75 V, Iout = 10–60 mA, Vout = 7.56 V				
Room temperature	TA = 25°C	-1.2	–	1.2	%
Across temperature	TA = -30°C ~ 85°C	-2.0	–	1.6	%
Output current		–	–	60	mA
Switching frequency	Programmable	0.6	1.6	1.6	MHz
Efficiency	Vin = 3.6 V, Iout = 20 mA	–	88	–	%
Soft start time		–	700	–	μs
Discharge time		–	1.6	7	ms
Output voltage ripple					
CCM mode	Iout = 60 mA	–	20	–	mVpp
Pulse-skipping	Iout = 10 mA	–	50	–	mVpp
Line transient	Vph_pwr = 4 V to/from 3.5 V (500 mV drop), Tr = Tf = 20 μs, Iout = 30 mA, simulates GSM burst	–	±200	–	mV
Load transient	Iout = 0 mA to/from 60 mA, slew = 1 mA/μs, Vph_pwr = 3.6 V, ESR = 4 mΩ at 1.6 MHz	-130	–	+100	mV
Ground current					
No load, pulse skip enabled		–	0.5	–	mA

1. I_LED matching accuracy is determined by the following formula: abs(max(Ix - Iy)) / (1/n sum(I1:In)), where (x, y = LED1, 2, 3, 4, n = 1,2,3,4 (number of strings enabled))
2. All specifications apply at VPH_PWR = 3.6 V, T = -30 to +85ºC, L = 10 μH, C ≥ 0.5 μF (WLED mode, capacitance value de-rated from 4.7 μF nominal), C ≥ 4 μF (AMOLED mode, capacitance value de-rated from 22 μF nominal), and F_sw = 800 kHz (WLED) F_sw = 1.6 MHz (AMOLED), unless noted otherwise.

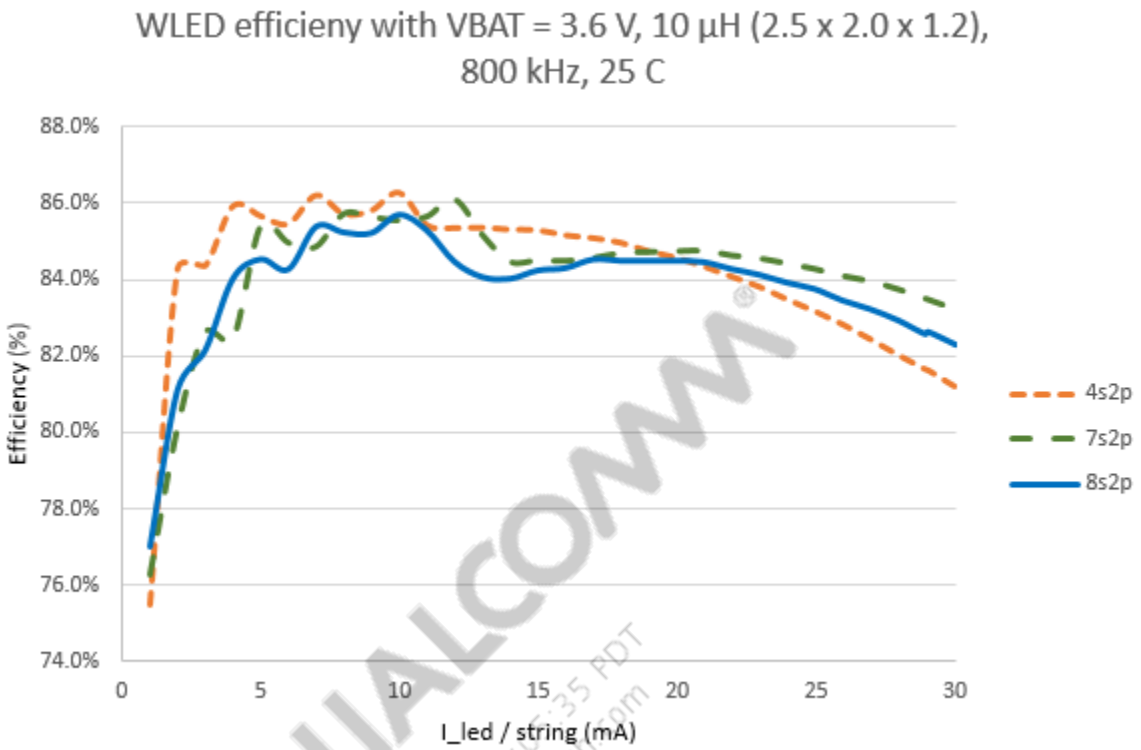


Figure 3-10 WLED efficiency plot with various WLED string configurations, measured on PMI8952 v1.0

3.7.5 Other current sinks and current drivers

Several types of low-voltage LED current drivers are available:

- Charging indicator with four different patterns on the notification LED
- MPPs can be configured as current sinks that operate off VPH_PWR

For other current sinks and drivers performance specifications, see Table 3-20.

3.8 IC-level interfaces

General housekeeping performance specifications are split into three functional categories as defined within its block diagram (Figure 3-11).

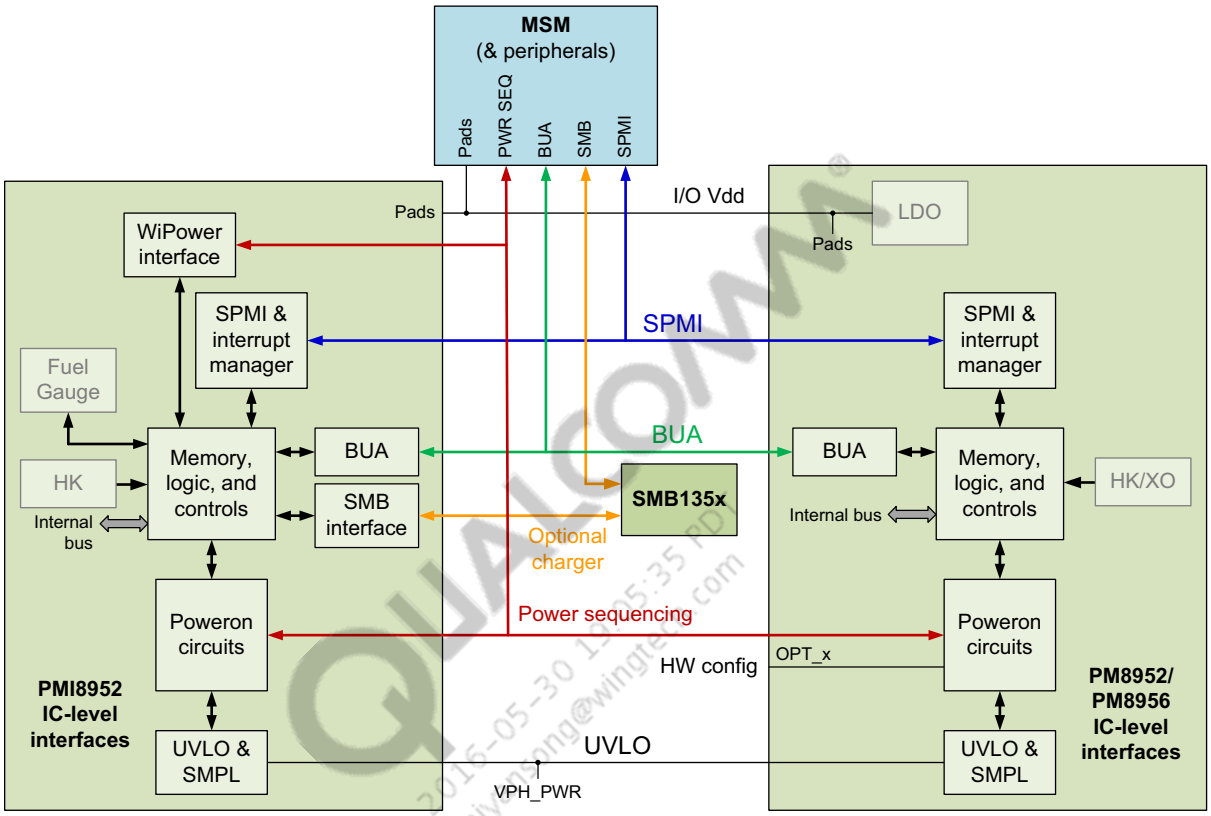


Figure 3-11 IC-level interfaces functional block diagram

3.8.1 Poweron circuits and power sequences

The PMI8952 complements the PM8952/PM8956 to meet the system's power management needs. Power sequencing details are shared between the two ICs, so this topic is addressed in the *PM8952/PM8956 + PMI8952 Power Management IC Design Guidelines/training Slides* (80-NT390-5), including:

- Poweron circuit block diagrams and descriptions
- Types of triggers and turn on and off trigger events
- Power sequencing and detailed descriptions
  - Concise summary: Dedicated circuits continuously monitor several events that might trigger a poweron sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the modem IC is taken out of reset.

3.8.1.1 UVLO and low battery detection

The PMI monitors CHG_VBAT_SNS and VPH_PWR continuously to detect low and severely low supply voltage conditions. CHG_VBAT_SNS is compared with the Vlowbatt threshold to determine low battery status and permit system operation. Vlowbatt is the primary threshold setting for system operation. VPH_PWR is compared with the UVLO threshold and will prevent operation of PMI during a UVLO condition. Related voltage specifications are listed in Table 3-18.

Table 3-18 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Low battery rising threshold	Vlowbatt programmable ranges, 75 mV steps; default values are listed as typical. 200 mV fixed hysteresis	2.500	3.000	3.580	V
Low battery falling threshold		–	2.800	–	V
Low battery accuracy		–	100	–	mV
UVLO rising threshold	Programmable ranges, 50 mV steps; default values are listed as typical. Hysteresis programmable from 175 mV to 425 mV; 175 mV is the default setting.	1.675	2.725	3.225	V
UVLO falling threshold		–	2.55	–	V

3.8.2 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage and current level requirements stated in Section 3.4. PMIC interrupt managers support the chipset modem and its processors, and communicate with the modem IC via SPMI. Since the interrupt managers are entirely embedded functions, additional performance specifications are not required.

3.9 Configurable I/Os

3.9.1 GPIO specifications

The 10 GPIO ports are digital I/Os that can be programmed for a variety of configurations (Table 3-19). General digital I/O performance specifications for the different configurations are included in Section 3.4.

NOTE Unused GPIO pins should be configured as inputs with 10 µA pull-down (their default state).

Table 3-19 Programmable GPIO configurations

Configuration type [1]	Configuration description
Input	■ No pull-up ■ Pull-up (1.5, 30, or 31.5 μA) ■ Pull-down (10 μA) ■ Keeper
Output	Open-drain or CMOS Inverted or non-inverted Programmable drive current

1. Available pad voltage is VDD_MSM_IO (1.8 V)

GPIOs default to digital input with 10 μA pull-down at poweron; they must be configured properly for their desired purposes after poweron.

GPIOs are designed to run at a 4 MHz rate to support high-speed applications. The supported rate depends on the load capacitance and IR drop requirements. If the application specifies load capacitance, then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage, and adjusting the drive strength according to the actual load capacitance.

3.9.2 MPP specifications

The PMI8952 includes four MPPs, and they can be configured for any of the functions specified within Table 3-20 with the following exceptions:

- Odd MPPs (MPP_1 and MPP_3) cannot be used as current sinks
- Even MPPs (MPP_2 and MPP_4) cannot be used as analog outputs

NOTE Only MPP_1 can be used as analog input. See Table 3-8 for the proper AMUX channel connection.

All MPPs default to high-Z at power on and when disabled.

NOTE Unused MPP pins should be configured to the high-Z state (their default state).

Table 3-20 Multipurpose pin performance specifications

Parameter	Comments	Min	Typ	Max	Units
MPP configured as digital input [1]					
Logic high-input voltage		0.65·V_M	–	–	V
Logic low-input voltage		–	–	0.35·V_M	V
MPP configured as digital output [1]					
Logic high-output voltage	$I_{out} = I_{OH}$	V_M- 0.45	–	V_M	V
Logic low-output voltage	$I_{out} = I_{OL}$	0	–	0.45	V
Drive strength					
Logic high (V_M > 2.5 V)		5.1	7.3	15.2	mA
Logic high (V_M < 2.5 V)		3.3	4.9	9.9	mA
Logic low		5.9	11.3	36.0	mA
MPP configured as analog input (analog multiplexer input)					
Input current		–	–	100	nA
Input capacitance		–	–	10	pF
MPP configured as analog output (buffered VREF output)					
Output voltage error	-50 µA to +50 µA	–	–	30	mV
Temperature variation	Due to buffer only; does not include VREF variation (see Table 3-11.)	–	–	± 0.03	%
Load capacitance		–	–	25	pF
Ground current		–	0.17	0.20	mA
MPPs configured as current sinks					
Power supply voltage		–	VDD	–	V
Output current	Programmable in 5 mA increments	0	–	40	mA
Output current accuracy	Any non-zero programmed current value; V_{out} = 0.5 to (V_{DD} - 1 V)	–	–	± 20	%
Dropout voltage	V_IN - V_OUT while I_OUT stays within its accuracy limits	–	–	500	mV
Ground current	Driver disabled	–	105	115	µA

1. Available pad voltages are:
   – VIN0 = VPH_PWR
   – VIN1 = VDD_MSM_IO (1.8 V)
   – VIN2 = VDD_MSM_IO (1.8 V)
   – VIN3 = VDD_MSM_IO (1.8 V)
   Other digital I/O specifications are included in Table 3-4.

4 Mechanical information

4.1 Device physical dimensions

The PMI8952 is available in the 144-pin wafer-level nanoscale package (144 WLNSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 144 WLNSP has a 5.11 × 4.77 mm body with a maximum height of 0.55 mm. Pin 1 is located by an indicator mark on the top of the package, and by the pad pattern when viewed from below. Figure 4-1 shows a simplified version of the 144 WLNSP outline drawing.

NOTE Click the link below to download the *144 WLNSP Outline Drawing 144 WLNSP, 5.11X4.77X0.55MM, D280, B25* (NT90-NT126-1) from the CreatePoint website:

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-NT126-1

https://createpoint.qti.qualcomm.com/chipcenter/download/title/0901003981b53cfb

After successfully logging in, the document is downloaded.

NOTE Make this drawing a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

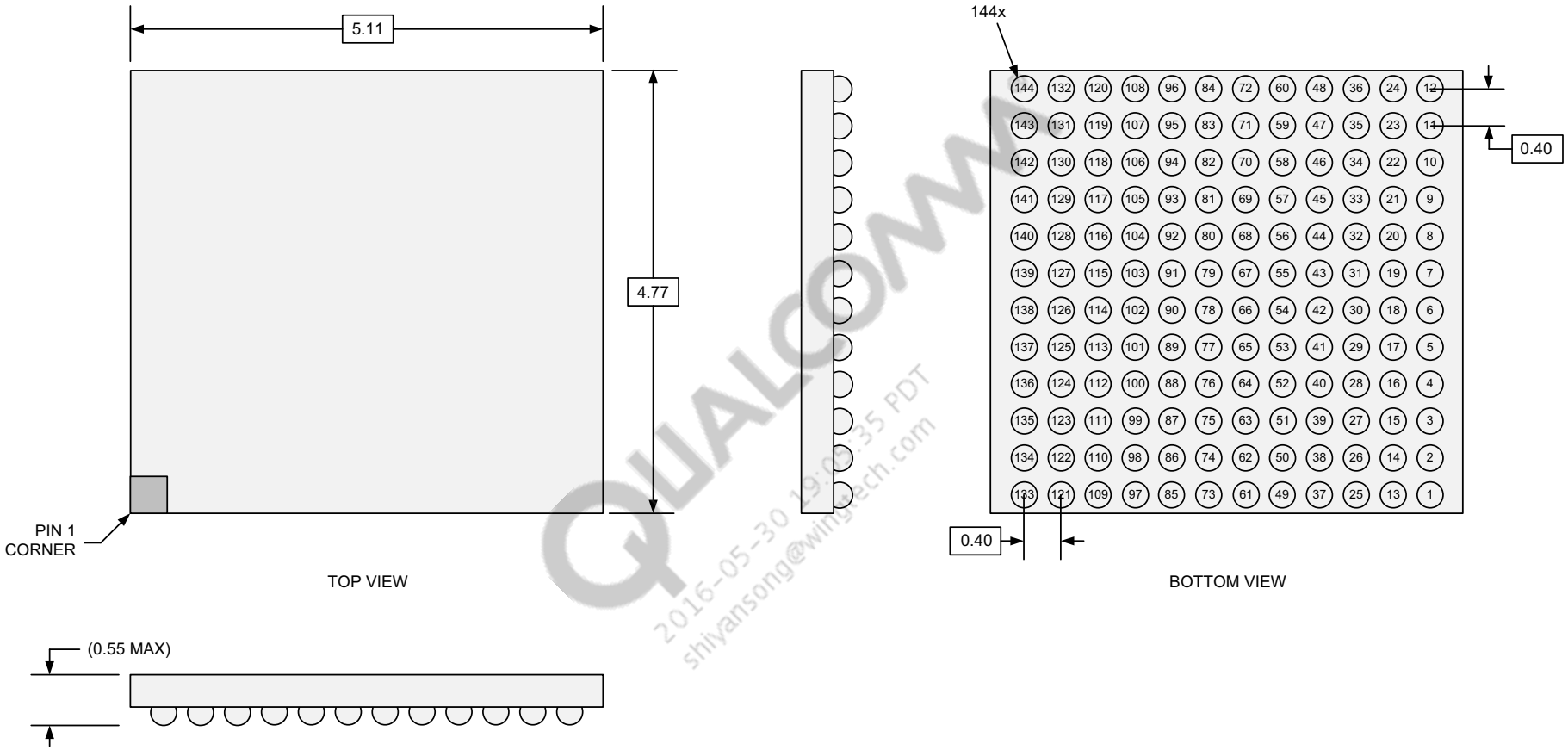


Figure 4-1 5.11 × 4.77 × 0.55 mm outline drawing

NOTE This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-NT126-1

https://createpoint.qti.qualcomm.com/chipcenter/download/title/0901003981b53cfb

4.2 Part marking

4.2.1 Specification compliant devices

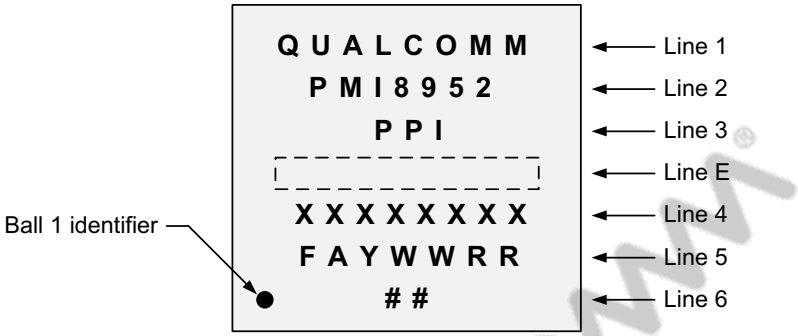


Figure 4-2 PMI8952 device marking (top view, not to scale)

Table 4-1 PMI8952 device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm Technologies, Inc. (QTI) company name or logo
2	PMI8952	QTI product name
3	PPI	P = Product configuration code – see Table 4-2 PI = Program ID code – see Table 4-2
E	Blank or random	Additional content as necessary
4	XXXXXXXX	XXXXXXXX = traceability information
5	FAYWWRR	F = wafer fab source of supply code ■ F = H for GlobalFoundries ■ F = P for SMIC A = assembly (ball drop) code ■ A = U for Amkor, China ■ A = M for Stats ChipPac, Singapore ■ A = E for ASE, Taiwan ■ A = Y for Amkor, Taiwan Y = single-digit year code WW = workweek (based upon calendar year) RR = product revision – see Table 4-2
6	• ##	• = ball 1 identifier ## = 2-digit wafer number

NOTE For complete marking definitions of all PMI8952 variants and revisions, refer to the *PMI8952 Device Revision Guide* (80-NT391-4).

4.3 Device ordering information

4.3.1 Specification compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— PI
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product version	Source code	Program ID
Example ►	PMI-8952	— 0	— 144	WLNSP	— HR	— 00	— 0	— 00

Figure 4-3 Device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

PMIC variant	P value	RR value	HW ID #	S value [1]	PI value [2]
ES sample type					
PMI8952 ES1	0	00	V1.0	0	00
PMI8952 ES2	0	02	V2.0	0	00
PMI8952 CS [3]	0	02	V2.0	0 or 1	00
Other sample types will be included in future revisions of this document, if needed.					

1. S is the source configuration code that identifies all the qualified die fabrication source combinations available at the time a particular sample type were shipped. S values are defined in Table 4-3.
2. PI is the Program ID code that identifies an IC's specific OTP programming that distinguishes it from other versions or variants.
3. CS parts have the same PPI and RR code as ES2. All devices with date code YWW = 528 (and later) are CS quality.

Table 4-3 Source configuration code

S value	Die	F value
0	BiCMOS	H = Global Foundries
1	BiCMOS	H = Global Foundries or P = SMIC
Other columns and rows will be added in future revisions of this document if needed.		

4.4 Device moisture-sensitivity level

Surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL, Table 4-4) indicates its ability to withstand exposure after it is removed from its shipment bag, while it's on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device.

Table 4-4 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH; PMI8952 rating
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hrs.	≤ 30°C/60% RH
4	72 hrs.	≤ 30°C/60% RH
5	48 hrs.	≤ 30°C/60% RH
5a	24 hrs.	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PMI8952 devices are classified as MSL1; the qualification temperature was 255°C +5°/-0°C***. This qualification temperature (255°C +5°/-0°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for further discussion).

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through QTI's CDMA Tech Support website. A thermal model for each device is provided within the "Power_Thermal" subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the link below to download the *PMI8952 144 WLNSP Thermal Package Model Icepak* (HS11-NT391-5HW) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-NT391-5HW

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

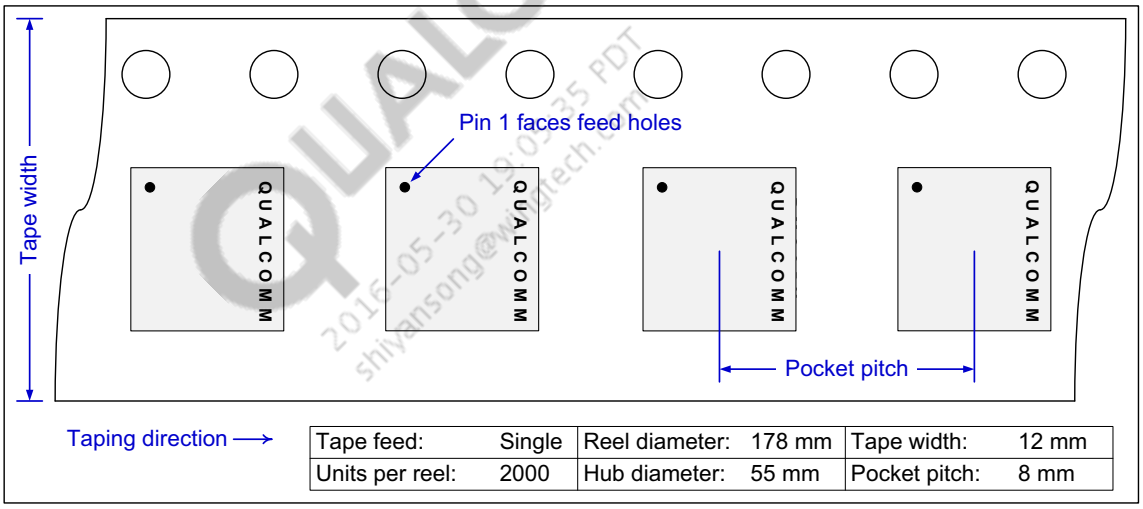
For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

5 Carrier, storage, & handling Information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards. A simplified sketch of the PMI8952 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	178 mm	Tape width:	12 mm
Units per reel:	2000	Hub diameter:	55 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

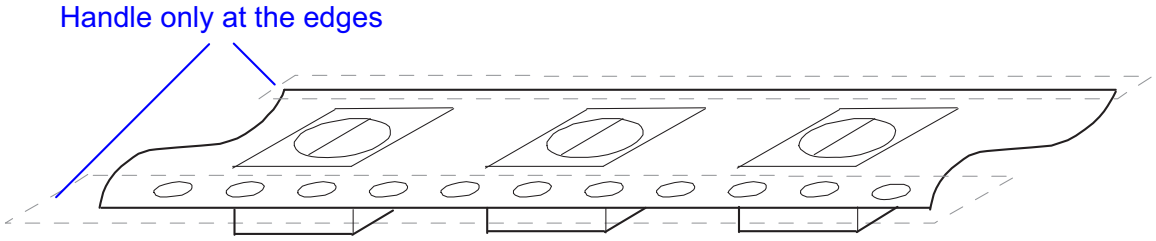


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PMI8952 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

Unlike traditional IC devices, the die within a wafer-level package is not protected by an overmold and there is no substrate; hence, these devices are relatively fragile.

To avoid damage to the die due to improper handling, these recommendations should be followed:

- Do not use tweezers; a vacuum tip is recommended for handling the devices.
- Carefully select a pickup tool for use during the SMT process.
- Do not make contact with the device when reworking or tuning components located near the device.

For more complete handling information, refer to *Wafer Level Package Device Handling Guidelines* (80-ND595-1).

5.3.1 Baking

Wafer-level packages such as this 144 WLNSP device should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Section 7.1 for the PMI8952 ESD ratings.

5.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC405 composition. A Product Material Declaration (PMD), which provides RoHS and other product environmental governance information, will be published when the data is available.

6.2 SMT parameters

This section describes QTI board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land-pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

QTI provides an example PCB land pattern and stencil design for the 144 WLNSP package.

NOTE Click the link below to download the 144 WLNSP land/stencil drawing (LS90-NG134-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/LS90-NG134-1

After successfully logging in, the document is downloaded.

NOTE Make this drawing a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.2.2 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1, and are shown in Figure 6-1.

Table 6-1 QTI typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

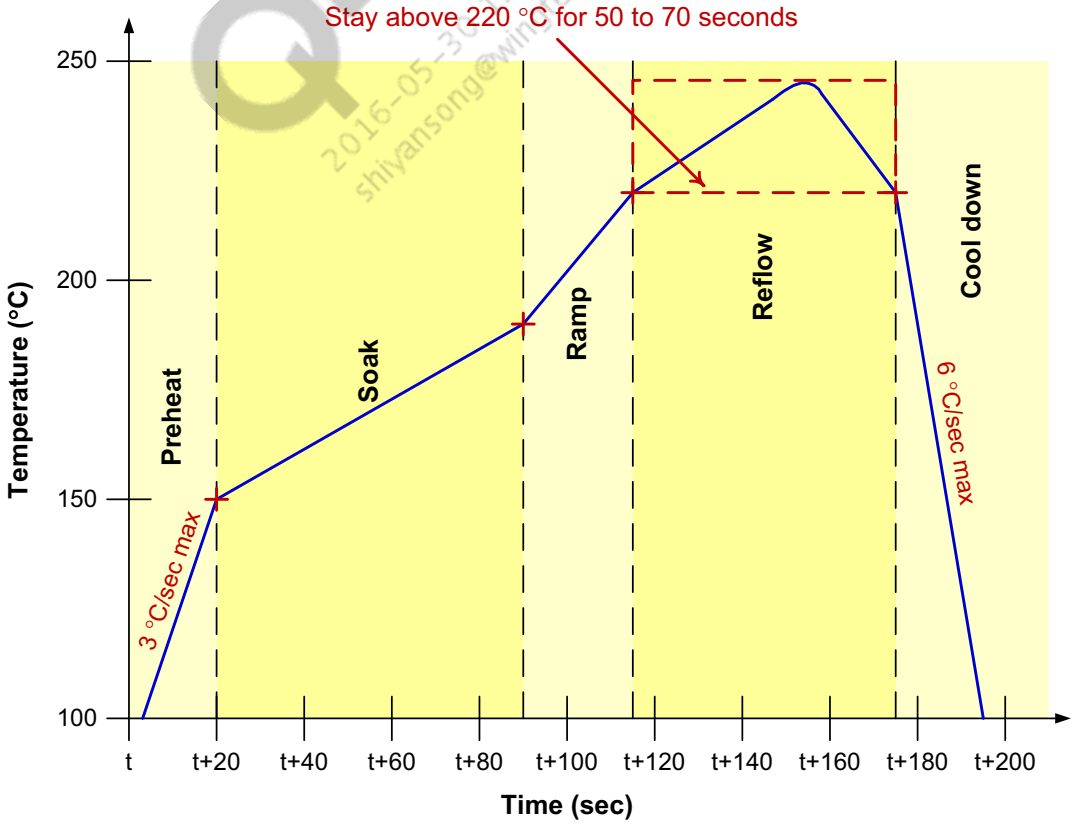


Figure 6-1 QTI typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document, and without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Section 4.4 – *Device moisture-sensitivity level*

   PMI8952 devices are classified as MSL1 at 255°C. The temperature (255°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Section 7.1 – *Reliability qualifications summary*

   One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5 °C (255°C to 260 °C).

3. Section 6.2.2 – *Reflow profile*

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections. However, it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C to 260°C).

6.2.4 SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow-profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations discussed above can be performed using daisy-chain components.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the link below to download the 144 WLNSP daisy-chain interconnect drawing (DS90-NT126-1) from the CreatePoint website.

This link will be included in future revisions of this document.

After successfully logging in, the document is downloaded.

NOTE Make this drawing a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.4 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)

Board-level reliability data is available for download.

NOTE Click the link below to download the 144 WLNSP board-level reliability data (BR80-NJ707-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/BR80-NJ707-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability qualifications summary

PMI8952 reliability qualification report for device from GF and SMIC in WLNSP package

Table 7-1 Silicon reliability results

Device qualification tests, standards and conditions	Sample # lots GF	Sample # lots SMIC	Results
ELFR in DPPM HTOL: JESD22-A108-A	462 (77 × 6 fab lots)	231 (77 × 3 fab lots)	Pass DDPM < 1000
Average failure rate (AFR) in FIT (λ) failures per billion device-hours; functional HTOL JESD22-A108-A	462 (77 × fab lots)	231 (77 × 3 fab lots)	<50 FIT
Mean time to failure (MTTF) t = 1/λ (million hours)	462 (77 × 3 fab lots)	231 (77 × 3 fab lots)	>20
ESD – Human body model (HBM) rating JESD22-A114-F	6 (3 × 2 fab lots)	3 (3 × 1 fab lot)	1500 V
ESD – Charged device model (CDM) rating JESD22-C101-E	6 3 × 2 fab lots	3 (3 × 1 fab lot)	500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C	6 (3 × 2 fab lots)	3 (3 × 1 fab lot)	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C	6 (3 × 2 fab lots)	3 (3 × 1 fab lot)	Pass

Table 7-2 Package reliability results

Package qualification tests, standards and conditions	Sample # lots	Results (ASET)	Results (ATC)	Results (SCS)	Results (ATT1)
Moisture resistance test (MRT): MSL 1; J-STD-020-D 3x reflow cycles at 255 +5/-0°C	462 154 × 3 assembly lots	Pass	Pass	Pass	Pass
Temperature cycle: JESD22-A104-D Temperature: -55 to +125°C; number of cycles: 1000 Min soak time at min/max temperature: 5 minutes Cycle rate: 2 cycles per hour (cph) MSL1 preconditioning: JESD22-A113-F Reflow temperature: 255 +5/-0°C	231 77 × 3 assembly lots	Pass	Pass	Pass	Pass
Unbiased highly accelerated stress test (uHAST) JESD22-A118 MSL1 preconditioning: JESD22-A113-F Reflow temperature: 255 +5/-0°C	231 77 × 3 assembly lots	Pass	Pass	Pass	Pass
High temperature storage life: JESD22-A103-D Temperature 150°C, 1000 hours	231 77 × 3 assembly lots	Pass	Pass	Pass	Pass
Physical dimensions: JESD22-B100-A Package outline drawing; NT90-NT126-1	15 1 assembly lot	Pass	Pass	Pass	Pass
Solder ball shear: JESD22-B117-B (Total samples from three assembly lots at each SAT)	45 15 × 3 assembly lots	Pass	Pass	Pass	Pass

7.2 Qualification sample descriptions

Device characteristics

Device name:	PMI8952
Package type:	144 WLNSP
Package body size:	5.11 × 4.77 × 0.55 mm
Lead count:	144
Lead composition:	SAC405
Fab process:	0.18 μm BiCMOS
Fab sites:	GlobalFoundries, SMIC
Assembly sites:	Amkor, China STATS ChipPAC, Singapore ASE, Taiwan Amkor, Taiwan
Solder ball pitch:	0.4 mm