A Multidrop Bus Design Scheme With Resistor-Based Impedance Matching on Nonuniform Impedance Lines

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***Abstract*—In this paper, a bus design scheme that achieves both impedance matching and uniform power distribution for a multidrop bus is presented. In contrast to conventional schemes, the proposed scheme lets the line impedance of each segment of the bus vary, and the impedance-matching resistance values are determined accordingly, thereby providing higher degrees of freedom for optimization. General formulas for determining the optimal line impedances and matching resistances are derived. The voltage and power ratios between the master driver and branch receivers are also established, showing that such ratios depend only on the master-to-branch impedance ratio and the number of branches. Similar relations are also derived for the backward direction. The measurement results of the fabricated FR4 printed circuit boards demonstrate good agreement with the theoretical results, and show reliable performance up to a bit rate of 5 Gbps.**

***Index Terms*—Impedance matching, multidrop bus, transmission line.**

I. Introduction

A multidrop bus is a convenient signaling configuration where data transfer occurs between a central master and several slave modules via a common medium. A typical application is a parallel bus between a memory controller and multiple DRAM modules. The main disadvantage of multidrop buses is the signal reflection that occurs at the impedance discontinuities caused by the multiple branches, resulting in degradation of the signal margin at the receiver side and hence increased bit error rates (BERs). Therefore, to avoid these undesired signal reflections, the line impedance should be matched at every branching node, calling for a new bus configuration.

Another consideration for a multidrop bus is the ability to distribute the signal power uniformly. In other words, it is desired that each end receiver receives the same signal amplitude and power from the master driver. Provided that all the receivers are identical, this can be satisfied by making all the side branch currents have the same amplitude. This necessitates the optimal setting of the current division ratio and the incoming-to-outgoing impedance ratio at each branching node.

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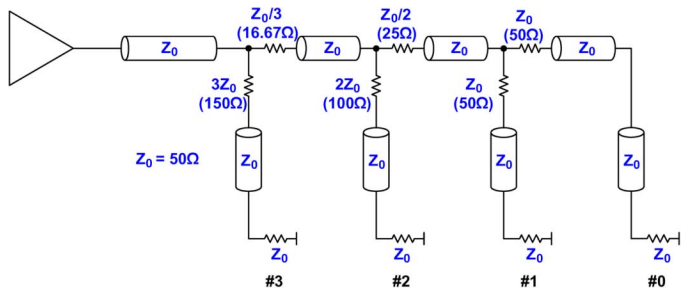


Fig. 1. 4-drop bus with resistor-based impedance matching.

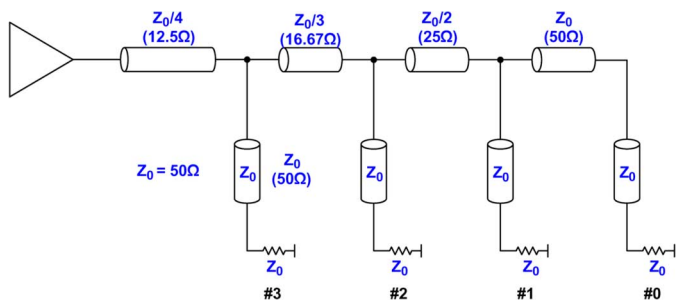


Fig. 2. 4-drop bus with resistorless impedance matching using variable line impedance.

There are some previous works dealing with the signal distortion in multidrop buses without relying on exact impedance matching at the branching nodes. In [1], a passive resonance mitigation technique is proposed, where signal reflections in an unmatched multidrop bus are weakened by means of a frequency selective attenuation using coupled transmission lines. On the other hand, in [2] signal reflection is minimized using a new bus topology, which is based on partial impedance matching, but the maximum number of branches is limited to 2 or 3. In either work, the fundamental issue of impedance matching is not resolved, and therefore the received signals are not completely free from reflection-caused distortions.

A simple approach to achieving both impedance matching and uniform power distribution on standard impedance lines is to cure the impedance discontinuities by inserting proper resistors at each branching node (Fig. 1). However, the main drawback of this approach is the excessively large resistance values that result unavoidably from the increased number of branches. These large matching resistances can cause excessive power and signal amplitude loss, degrading the overall performance.

An alternative approach ([3], [4]) is to match the impedances by adjusting the line impedance values themselves (Fig. 2). At

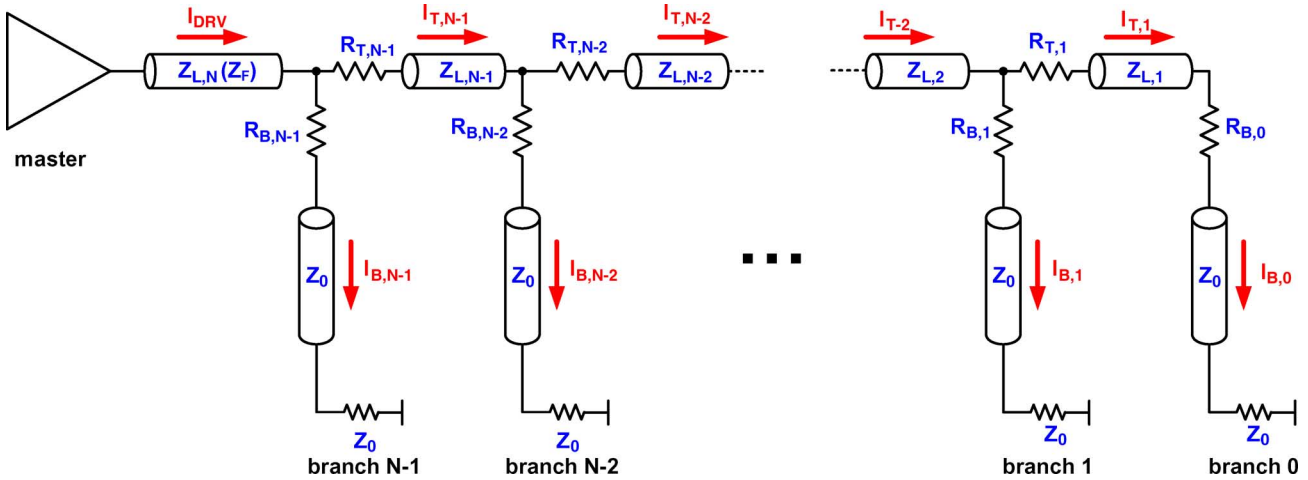


Fig. 3. General model for impedance matched N-drop bus with uniform power delivery.

each node, the incoming line impedance value is set equal to the combined parallel impedance value of the outgoing lines. The power dividing ratio is determined by the ratio between the outgoing line impedances. Although this approach does not have power loss issues since no resistors are used, its main drawback is that the required line impedance values can become excessively low even with a moderate number of branches. For example, in [3], the lowest line impedance value is 25 Ω with a 2× scaled branch line impedance of 100 Ω. When using a nominal branch line impedance of $Z_0 = 50\,\Omega$, the lowest line impedance value becomes $Z_0/4 = 12.5\ \Omega$, which may require prohibitively large line widths for practical printed circuit board (PCB) implementations.

The aforementioned approaches are two extreme cases of multidrop buses, one with fixed line impedance and the other without any matching resistors. As both approaches have practicality issues, we examined a hybrid approach that can find a balance between the two extremes. In other words, we considered an approach where a bus employs both variable line impedances and matching resistors. This approach aims to achieve the advantages of both schemes, namely reduced power loss and relaxed requirement for low impedance lines.

In this paper, we will first present a general analytical model for deriving the optimal line impedances and matching resistance values at each bus segment. Next, we will analyze the power delivery based on this generalized model and provide a set of equations for estimating the power performance of multidrop buses. Finally, we will provide experimental results for several multidrop bus configurations.

II. A General Model for Impedance-Matched Multidrop Buses

In this section, we will present a general model for impedance matched multidrop buses, and use it for providing a generalized approach to achieving impedance matching under any given configuration of transmission line impedance values.

Fig. 3 depicts a generalized multidrop bus with N equal side branches. For simplicity, the side branch line impedance is fixed at Z_0, and all the receiver terminations are properly matched. For convenience, we will denote the signal propagation direction from the master to the branches as "*forward*", and the opposite direction from any branch to the master as "*backward*". Also, we will number the branches and nodes in increasing order from the bus end towards the master, so that the farthest one becomes branch 0 $(k = 0)$, and the nearest one becomes branch $N-1$ $(k = N-1)$. Furthermore, we will denote the line just adjacent to the master as the "*front line*", and accordingly denote its impedance $(Z_{L,N})$ as Z_F. We will maintain these conventions throughout this paper.

Here the goal is to find all the resistances, given the line impedances, so as to satisfy two conditions: elimination of reflections and uniform power delivery. We should note that when forward impedance matching is achieved, backward impedance matching is not necessary even for the backward signals. All the reflections caused by the backward impedance mismatch would be forward-directed, and since the forward impedance is matched the reflected signals would not cause backward-directed secondary reflections. Eventually, all the reflected signals would be absorbed at the matched branch terminations. Thus the backward signal received at the master does not suffer from distortion caused by reflected signals. Therefore, from now on we will focus solely on forward impedance matching.

At node k $(1 \le k \le N-1)$ (Fig. 4), the impedance is matched for the forward signal propagation when

$$Z_{L,k+1} = (R_{T,k} + Z_{L,k})//(R_{B,k} + Z_0). \tag{1}$$

For the final branch $(k = 0)$, this condition becomes

$$Z_{L,1} = R_{B,0} + Z_0. \tag{2}$$

For uniform power distribution to all end receivers, the signal current amplitude at each side branch should be equal. This can be written as

$$I_{B,k} = I_{B0} \quad (0 \le k \le N-1). \tag{3}$$

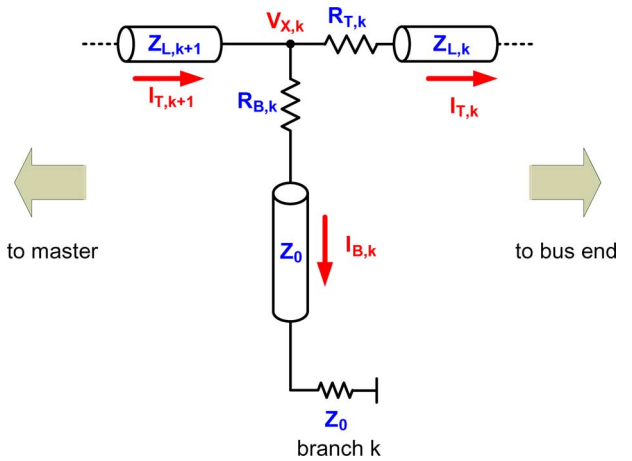


Fig. 4. Detailed view of node and branch k $(1 \leq k \leq N-1)$.

In turn, this implies that the trunk line current at each segment becomes

$$I_{T,k} = \sum_{j=0}^{k-1} I_{B,j} = k \cdot I_{B0} \quad (1 \leq k \leq N-1) \tag{4}$$

and thus

$$I_{T,k} = k \cdot I_{B,k} \quad (1 \leq k \leq N-1). \tag{5}$$

Since

$$I_{B,k} = \frac{V_{X,k}}{R_{B,k} + Z_0} \tag{6}$$

$$I_{T,k} = \frac{V_{X,k}}{R_{T,k} + Z_{L,k}} \tag{7}$$

(5) becomes

$$k \cdot (R_{T,k} + Z_{L,k}) = R_{B,k} + Z_0. \tag{8}$$

From (1), (2), and (8), the resistance values can be derived as

$$R_{T,k} = \left(\frac{k+1}{k}\right) \cdot Z_{L,k+1} - Z_{L,k} \quad (1 \leq k \leq N-1) \tag{9}$$

$$R_{B,k} = (k+1) \cdot Z_{L,k+1} - Z_0 \quad (0 \leq k \leq N-1). \tag{10}$$

Since these resistance values cannot be negative, this imposes some constraints on the possible values for the line impedances. This can be summarized as

$$Z_{L,k} \leq \left(\frac{k+1}{k}\right) \cdot Z_{L,k+1} \quad (1 \leq k \leq N-1) \tag{11}$$

$$Z_{L,k} \geq \frac{Z_0}{k} \quad (1 \leq k \leq N-1). \tag{12}$$

Thus, the line impedances for each segment cannot be set freely to an arbitrary value, but should be set to feasible values within the valid range given by (11) and (12).

Note that in the particular case of $Z_{L,1} = Z_0$, the final segment comprising branches 0 and 1, line $Z_{L,1}$, and resistors $R_{B,1}$ and $R_{T,1}$ results in a symmetrical structure. This can be reduced to a simpler structure using only one resistor $(R_{TX,1})$ instead

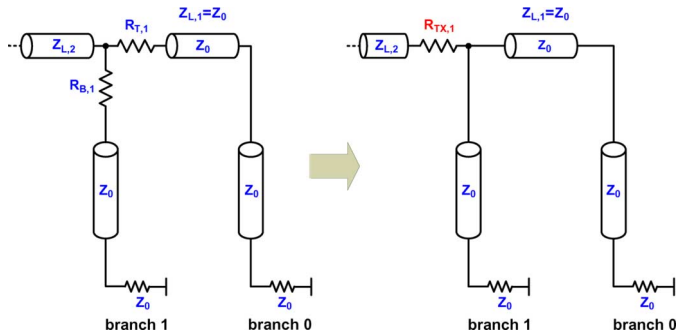


Fig. 5. Reduction of final symmetrical branches 0 and 1.

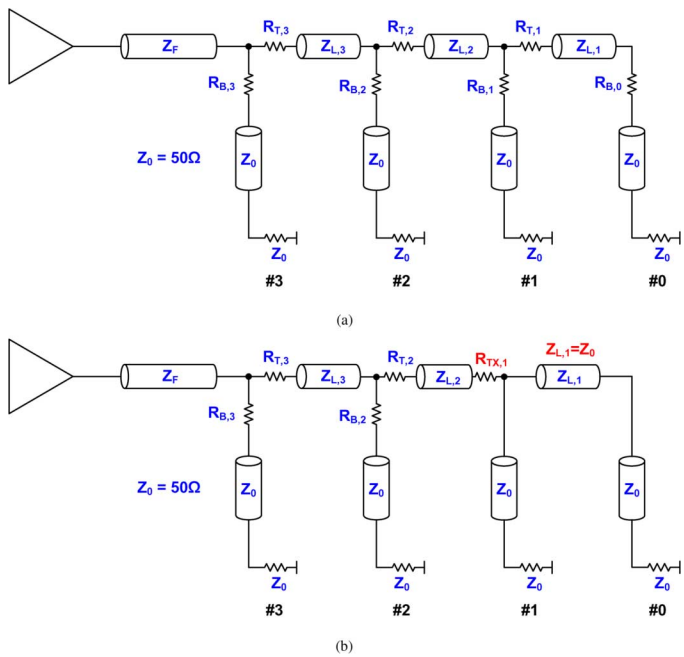


Fig. 6. General 4-drop bus (a) without final branch reduction and (b) with final branch reduction.

of two (Fig. 5), which simplifies the circuit board implementation. The resulting resistance $R_{TX,1}$ becomes half of the original value $R_{B,1}$ and $R_{T,1}$, since

$$R_{TX,1} = Z_{L,2} - (Z_{L,1} // Z_0) = Z_{L,2} - \frac{Z_0}{2} = \frac{R_{B,1}}{2} = \frac{R_{T,1}}{2}. \tag{13}$$

In practical implementations, we should first determine the front line impedance, and then set the remaining segment line impedances to implementation-feasible values satisfying (11) and (12), and finally calculate the matching resistance values using (9) and (10).

Fig. 6 and Table I depict several 4-drop bus implementation examples using line impedances of $(1/4)Z_0$ (12.5 Ω), $(1/3)Z_0$ (16.7 Ω), $(1/2)Z_0$ (25 Ω), $(2/3)Z_0$ (33.3 Ω), and Z_0 (50 Ω), both with and without final branch reduction.

III. Bidirectional Power Delivery in Multidrop Buses

In this section, we will derive the voltage and power delivery relationship for both the forward and backward signal propagation cases. In particular, we will show that the ratio between the

TABLE I
RESISTANCE VALUES FOR 4-DROP BUS IMPLEMENTATIONS WITH AND WITHOUT FINAL BRANCH REDUCTION

Line configuration	$R_{T,3}$	$R_{B,3}$	$R_{T,2}$	$R_{B,2}$	$R_{T,1}$	$R_{B,1}$	$R_{Tx,1}$	$R_{B,0}$
12.5–16.7–25–50 (Resistorless)	0	0	0	0	0	0	0	0
16.7–16.7–25–50	5.56	16.7	0	0	0	0	0	0
25–33.3–50–50	0	50	0	50	50	50	25	0
33.3–33.3–33.3–50	11.1	83.3	16.7	50	16.7	16.7	8.33	0
33.3–33.3–50–50	11.1	83.3	0	50	50	50	25	0
50–50–50–50 (Fixed line impedance)	16.7	150	25	100	50	50	25	0

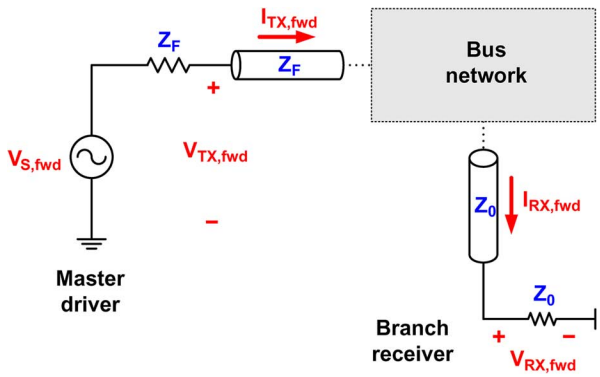


Fig. 7. Circuit model for the forward propagation case.

transmitted and received voltage swing values, and also the ratio between the emitted and received power, are determined solely by the ratio of the front line and branch line impedance values (Z_0/Z_F), and the number of branches (N).

A. Forward Propagation Case

In the previous section we have already described the constraints on the impedance and resistance values for uniform power delivery. Under this condition all the branch currents are equal, and thus all the branch receivers receive the same amount of power. We will denote this branch current as $I_{RX,\mathrm{fwd}}$.

Assuming that the master-side driver's output impedance is properly terminated in Z_F (Fig. 7), the driving current and the voltage at the front line input can be expressed as

$$I_{TX,\mathrm{fwd}} = \frac{V_{S,\mathrm{fwd}}}{2 \cdot Z_F} \tag{14}$$

$$V_{TX,\mathrm{fwd}} = \frac{V_{S,\mathrm{fwd}}}{2} \tag{15}$$

respectively. On the other hand, the received voltage at the branch side can be expressed as

$$V_{RX,\mathrm{fwd}} = I_{Rx,\mathrm{fwd}} \cdot Z_0. \tag{16}$$

Since there are N branches

$$\begin{aligned} I_{TX,\mathrm{fwd}} &= N \cdot I_{RX,\mathrm{fwd}} \\ &= N \cdot \frac{V_{RX,\mathrm{fwd}}}{Z_0}. \end{aligned} \tag{17}$$

Combining (14) and (17) results in

$$\left.\frac{V_{RX}}{V_S}\right|_{\mathrm{fwd}} = \frac{Z_0}{2N \cdot Z_F}. \tag{18}$$

Accordingly, the power ratio with respect to the driver's voltage source becomes

$$\left.\frac{P_{RX}}{P_S}\right|_{\mathrm{fwd}} = \frac{Z_0}{2N^2 \cdot Z_F} \tag{19}$$

where P_S and P_{RX} denote the power delivered by the voltage source and the received power, respectively.

In many cases, the termination resistance is embedded within the driver circuitry, making it difficult to measure $V_{S,\mathrm{fwd}}$ directly. In these cases, we can modify (18) and (19) so that it can be calculated using $V_{TX,\mathrm{fwd}}$. Substituting (15) into (18) we get the measured voltage ratio

$$\left.\frac{V_{RX}}{V_{TX}}\right|_{\mathrm{fwd}} = \frac{Z_0}{N \cdot Z_F}. \tag{20}$$

Accordingly, the power ratio with respect to the front line input, excluding losses at the driver's output resistance, becomes

$$\left.\frac{P_{RX}}{P_{TX}}\right|_{\mathrm{fwd}} = \frac{Z_0}{N^2 \cdot Z_F}. \tag{21}$$

From (20) and (21) we can see that the delivered voltage and power ratio is determined solely by the impedance ratio Z_0/Z_F and the number of branches N, regardless of the individual impedance values of the intermediate segment lines.

We should note that the ratios in (20) and (21) are exactly double the values in (18) and (19), respectively, which accounts

for the voltage drop and power loss in the matched source resistance of Z_F. However, since no signal is reflected back to the master side, there is no need of such matched source termination. Thus, the output impedance can have any value other than Z_F, including zero. When setting the output resistance to zero, it is possible to eliminate the power loss at the output resistance. In this case the ratios in (18) and (19) are doubled. Nevertheless, (20) and (21) are still valid in those cases, since they deal with quantities measured just outside of the output resistance, and thus they are not subject to its effect.

The power efficiency of the multidrop bus can be assessed by comparing the power ratio in (21) with the lossless value of $1/N$. Eq. (21) shows that the best power efficiency can be achieved only by making the front line impedance $Z_F N$ times smaller than the branch line impedance Z_0. For larger Z_F values, the bus will have losses, meaning that it needs matching resistors for matched impedances and uniform power delivery.

B. Backward Propagation Case

In the backward propagation case, the signal launched at the branch-side driver suffers from reflections at the branching nodes while propagating towards the master side. However, since all reflected signals are eventually absorbed in the branch terminations, the signal received at the master side does not suffer from distortion caused by these reflections.

Due to these reflections, for a direct analysis we should perform a step-by-step calculation using the transmission coefficient values at each impedance discontinuity point. A detailed calculation using this approach is presented in the Appendix.

A much simpler analysis is possible using the reciprocity theorem ([6], [7]). Since the multidrop bus circuit is composed entirely of passive linear components, we can apply the reciprocity theorem, and then derive the received voltage in the backward propagation case from the already calculated ones in the forward propagation case. We will assume a matched termination of Z_F at the master-side receiver.

The circuit for the forward propagation case (Fig. 7) can be redrawn as shown in Fig. 8(a). Here, the relationship between V_S and I_{RX} can be derived from (16) and (18) as

$$\left.\frac{I_{RX}}{V_S}\right|_{\text{fwd}} = \frac{1}{2N \cdot Z_F}. \tag{22}$$

In the backward propagation case [Fig. 8(b)], the driver and receiver ports are reversed. Nevertheless, by reciprocity the relationship between V_S and I_{RX} is still valid. Thus

$$\left.\frac{I_{RX}}{V_S}\right|_{back} = \frac{1}{2N \cdot Z_F}. \tag{23}$$

The relation between the master-side voltage and current is given as

$$V_{RX,back} = I_{Rx,back} \cdot Z_F. \tag{24}$$

Thus, from (23) and (24), the voltage ratio with respect to $V_{S,back}$ can be expressed as

$$\left.\frac{V_{RX}}{V_S}\right|_{back} = \frac{1}{2N}. \tag{25}$$

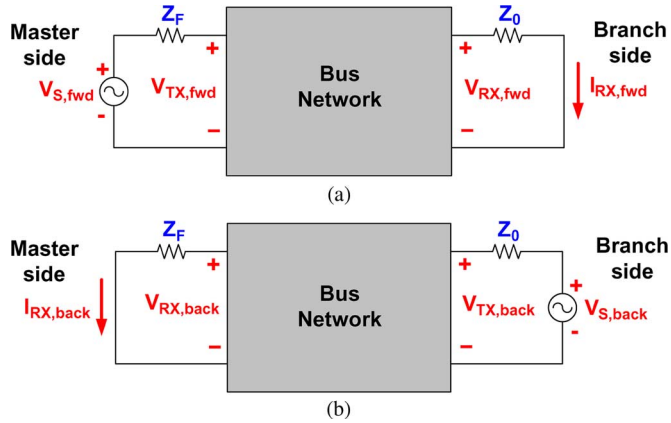


Fig. 8. Application of the reciprocity theorem on the bus circuit: (a) forward propagation case and (b) backward propagation case.

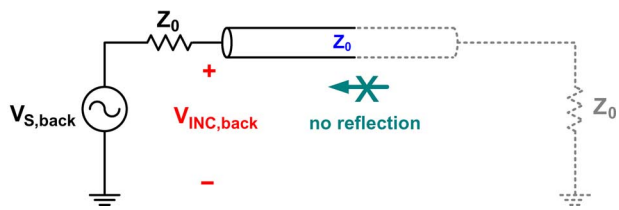


Fig. 9. Circuit model for the definition of $V_{INC,\text{back}}$.

This shows that the backward voltage ratio is determined solely by the number of branches N, regardless of the line impedance values and Z_0/Z_F.

Similarly as in the forward propagation case, it would be more practical to express (25) using the voltage at the line input ($V_{TX,\text{back}}$). Unfortunately, $V_{TX,\text{back}}$ suffers from unavoidable reflections at the branching nodes, so it cannot be used directly for calculation. Therefore, we will instead define a new quantity $V_{INC,\text{back}}$ as *the incident voltage at the branch line input assuming that there is no reflection* (Fig. 9). By this definition, $V_{INC,\text{back}}$ can be expressed as

$$V_{INC,\text{back}} = \frac{V_{S,\text{back}}}{2}. \tag{26}$$

This quantity is readily measurable, albeit not directly, using a matched termination of Z_0 in a separate replica circuit. Using this quantity, (25) can be rewritten as

$$\left.\frac{V_{RX}}{V_{INC}}\right|_{\text{back}} = \frac{1}{N}. \tag{27}$$

Using the same approach, the nominal power delivery ratio for the backward case can be expressed as

$$\left.\frac{P_{RX}}{P_{INC}}\right|_{\text{back}} = \frac{Z_0}{N^2 \cdot Z_F} \tag{28}$$

where P_{INC} denotes the emitted power at the branch line input assuming that there is no reflection. In reality, the emitted power will deviate from this value due to reflections, but the received power will remain the same, and thus (28) is still valid as an estimation of the power delivery ratio.

Interestingly, comparing (28) with (21) we can see that the power delivery ratios for both the forward and backward propagation cases are equal.

TABLE II
THEORETICALLY ESTIMATED VALUES OF RECEIVED VOLTAGE AND POWER RATIOS FOR SEVERAL BUS LINE CONFIGURATIONS

Bus line configuration	Z_0/Z_F	Forward case			Backward case	
		Voltage ratio	Received power ratio	Resistive power loss ratio	Voltage ratio	Received power ratio
12.5−16.7−25−50	4.0	1.0	0.25	0.0	0.25	0.25
16.7−16.7−25−50	3.0	0.75	0.1875	0.25	0.25	0.1875
25−33.3−50−50	2.0	0.5	0.125	0.5	0.25	0.125
33.3−33.3−33.3−50	1.5	0.375	0.09375	0.625	0.25	0.09375
33.3−33.3−50−50	1.5	0.375	0.09375	0.625	0.25	0.09375
50−50−50−50	1.0	0.25	0.0625	0.75	0.25	0.0625

Resistive power loss ratio: ratio of power dissipated in the impedance matching resistors

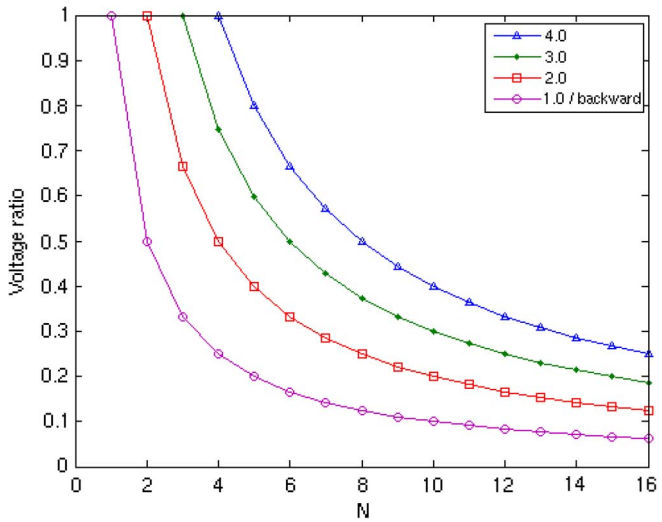


Fig. 10. Plot of voltage ratio vs number of branches N for several values of Z_0/Z_F in the forward signal case. Denoted value in the legend is Z_0/Z_F. Plot for the backward signal case is equal to that for $Z_0/Z_F = 1.0$.

C. Application of the Voltage and Power Equations

The derived signal delivery equations show that for a given bus configuration the signal delivery ratios for both directions are determined solely by the number of branches N and the impedance ratio Z_0/Z_F. Moreover, the power delivery ratios for both directions have the same value. Since the voltage ratio is independent of the line impedances other than Z_F, there is some degree of freedom on their values, and thus they can be varied freely provided that (11) and (12) are still valid. For example, the line impedances can be selected so that the number of impedance matching resistors is minimized.

In a complete system with transceiver circuits, there is a minimum detectable input swing at the receiver for proper operation. This value is determined by the sensing circuit in the receiver, and thus it imposes a lower limit on the voltage swing arriving at the receiver. In turn, this sets a lower limit on the voltage ratio for a given value of the driver voltage swing. Therefore, for proper bus design, the voltage ratios for both forward and backward propagation cases should exceed the lower limits set by the sensitivity of the detector circuits and the driver swing.

Fig. 10 shows the plots of the voltage ratio versus the number of branches N for several values of Z_0/Z_F in the forward signal case. The plot for the backward signal case is equal to that for $Z_0/Z_F = 1.0$. It should be noted that the forward signal voltage ratio is inversely proportional to N and directly proportional to Z_0/Z_F, whereas the backward voltage ratio is inversely proportional to N only.

Thus, for a given number of branches N, we can adjust the front line impedance Z_F so that the forward signal voltage ratio is within the desired or tolerable range. However, since the backward signal voltage ratio is independent of Z_0/Z_F, it cannot be improved by increasing the value of Z_0/Z_F for a given value of N. Thus, the minimum tolerable value of the backward voltage ratio imposes a practical limit on the maximum possible number of branches N. This somewhat overshadows the advantage of the proposed scheme, but, as it will be explained later, we can use some other techniques to overcome this. Table II shows the theoretically estimated voltage and power ratios for several 4-drop bus configurations.

D. Implementation Considerations

The feasibility of the proposed scheme depends on the implementation feasibility of nonstandard impedance lines. These lines can be implemented by varying the line trace width according to values determined by simulation or equations such as those given in [8] and [9]. By using these equations we can also verify that the sensitivity of line impedance to deviations in dimensional parameters such as line width, thickness and dielectric height is similar for low impedance lines to that for standard 50 Ω lines. Therefore, under equal conditions the nonstandard low impedance lines can be implemented with a similar precision as standard 50 Ω lines.

Even in cases where there are slight deviations (e.g. 10% or less) in the actual impedance values, the reflections caused by the resulting impedance mismatch are not so significant. Denoting the deviation as ε ($|\varepsilon| \ll 1$), the relationship between the ideal (Z_1) and actual (Z_2) impedance values can be written

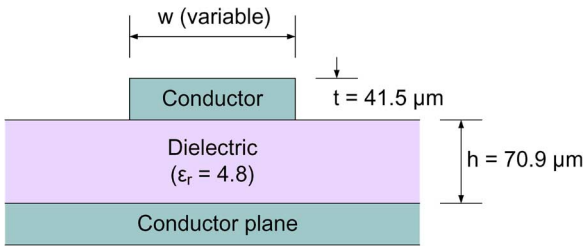


Fig. 11. Cross section of the microstrip line structure on the test PCB. Denoted dimensions are expected values upon PCB fabrication.

as

$$Z_2 = (1+\varepsilon)\cdot Z_1 \tag{29}$$

and, from the telegrapher's equation ([10]–[12]), the resulting reflection coefficient at the junction (with Z_1 as the source side) becomes

$$\begin{aligned}\Gamma &= \frac{Z_2 - Z_1}{Z_2 + Z_1} \\ &= \frac{(1+\varepsilon)\cdot Z_1 - Z_1}{(1+\varepsilon)\cdot Z_1 + Z_1} \\ &\cong \frac{\varepsilon}{2} \qquad (|\varepsilon| \ll 1)\end{aligned} \tag{30}$$

which is roughly half of the impedance deviation. This shows that the reflected signal caused by impedance deviations of 10% or less is smaller than 5% of the original signal, and thus it has only a minor effect.

For efficient implementation of the proposed scheme, the resistors for impedance matching must be located as close to the branching node as possible. However, in real implementations the traces on the PCB are already crowded with parallel connections of the connectors, so it would be hard to find any room to attach two resistors to a single branching node. Also, the signal transmission path is disturbed by discontinuities caused by the physical size of the resistors in addition to parasitic inductances and capacitances. A solution to this problem would be using a component-embedded PCB ([13]), where passive components are embedded into the dielectric layers, thereby reducing the required space and parasitic effects, and thus improving the signal integrity.

One variation to the proposed bus scheme is using the dynamic on-die termination (ODT) ([14]) feature. When using this feature, the master raises the termination resistance value, making an open or high impedance circuit when it is expected to receive data from the branch side, and thus increases the amplitude of the received signal, up to double the normal value in case of an open circuit. Although termination is broken at the master, no signal degradation occurs since the resulting reflected signals propagate away from the master, and they do not cause any secondary reflections returning back to the master. This is especially useful since, from (20) and (27), for the same driver strength the received signal amplitude in the backward propagation case is smaller than that in the forward propagation case by a factor equal to the impedance ratio Z_0/Z_F. Unfortunately, the dynamic ODT feature cannot be applied to the branch side, since the reflected signal at the branch receiver would be reflected again immediately at the branching node and mixed with the incoming signal.

E. Skin Effect

The skin depth at frequency f for a conductor having a conductivity value of σ is given as ([15])

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}. \tag{31}$$

Thus, the effective resistance per unit length of the conductor has a frequency dependence of

$$R \propto \frac{1}{\delta} \propto \sqrt{f}. \tag{32}$$

However, the characteristic impedance

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{33}$$

remains roughly the same since the inductive term has a frequency dependence of

$$j\omega L \propto f. \tag{34}$$

Thus, it becomes more dominant than the resistive term at higher frequencies. Therefore, the skin effect does not significantly affect impedance matching at high frequencies.

Moreover, since the conductor resistance is inversely proportional to the line width, the resistive term R becomes smaller for lower impedance lines, and therefore the low impedance lines used in the proposed scheme undergo less frequency-dependent loss compared to ordinary 50 Ω lines.

IV. Test Circuit Board Implementation

For testing and verification of the aforementioned properties, we implemented several test circuit boards with different line configurations. The test boards were implemented using the topmost routing layer and upper ground plate (the topmost two layers) on a standard 6-layer FR4 PCB. This PCB type was chosen in order to test the feasibility of the proposed multidrop bus design scheme on general circuit boards. The cross section of the microstrip structure is depicted in Fig. 11. The nonstandard impedance lines were implemented by varying the line width according to the values given in Table III. This data was determined through simulation by courtesy of the board manufacturer, and further verification was performed using the equations given in [8] and [9]. For the matching resistances we used chip resistors with the closest available resistance values to those given in Table I.

For ease of measurement, all external connector ports were matched to 50 Ω, and for Z_F values lower than 50 Ω an additional series resistor with value $Z_0 - Z_F$ was inserted between

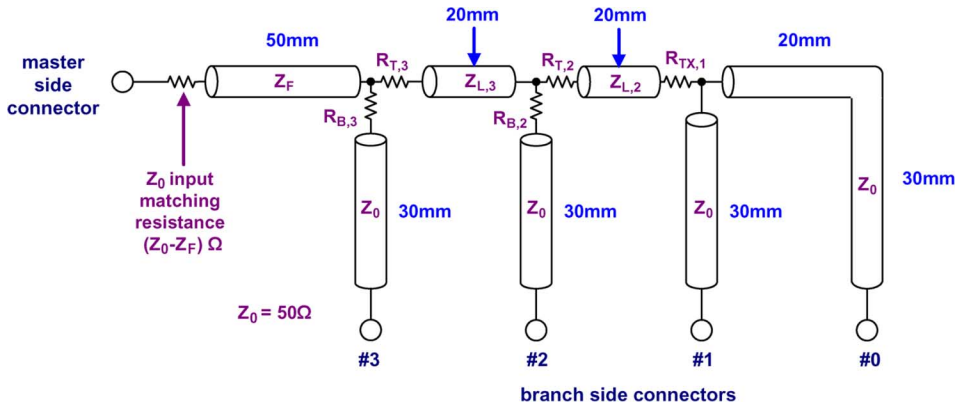


Fig. 12. Length of transmission line traces on the test boards.

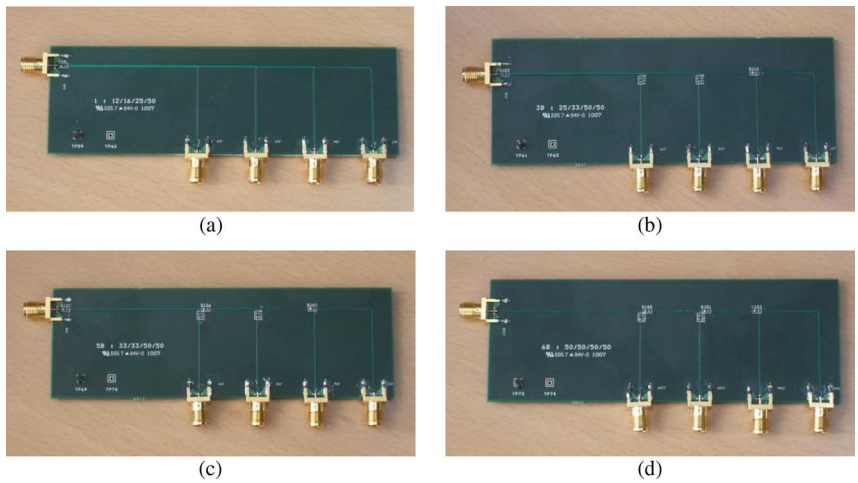


Fig. 13. Photographs of implemented test boards: (a) 12.5-16.7-25-50, (b) 25-33.3-50-50, (c) 33.3-33.3-50-50, and (d) 50-50-50-50. Note that the front line width is largest in (a).

TABLE III
MICROSTRIP WIDTHS FOR DIFFERENT LINE IMPEDANCES

Line impedance (Ω)	Line width (mm)
50	0.1
33.3	0.22
25	0.34
16.7	0.57
12.5	0.81

the master-side input connector and the front line. The dimensions of the transmission line traces are shown in Fig. 12. Photographs of the implemented test boards are given in Fig. 13.

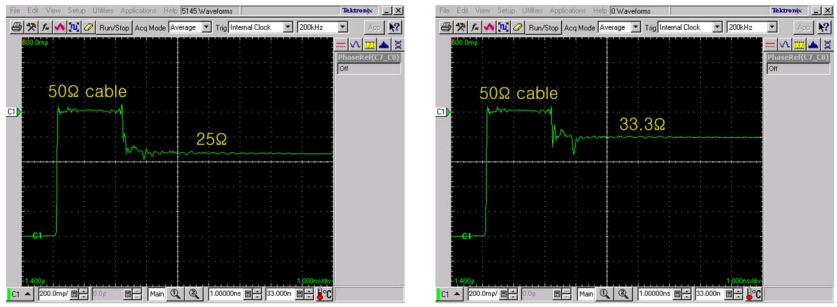
V. MEASUREMENT RESULTS

Prior to the main signal measurements we performed a time-domain reflectometry (TDR) measurement on the test boards for verification of the test board impedances. For the voltage swing measurement we fed the test board input with a 1 Gbps PRBS $2^{31}-1$ 1.2 Vp-p signal provided by a pulse/pattern generator, and measured the output signals using a digital sampling oscilloscope. A moderate data rate of 1 Gbps was chosen due to bandwidth limitations on the active probe used for measurement. For high frequency measurement we connected the test board to a bit error rate tester (BERT) and measured the received signal eye diagrams for a 5 Gbps PRBS $2^{31}-1$ 1.2 Vp-p signal. The measurements were carried separately for the forward and backward propagation cases, respectively, with additional modification on the test boards when needed.

A. Time-Domain Reflectometry (TDR) Measurement

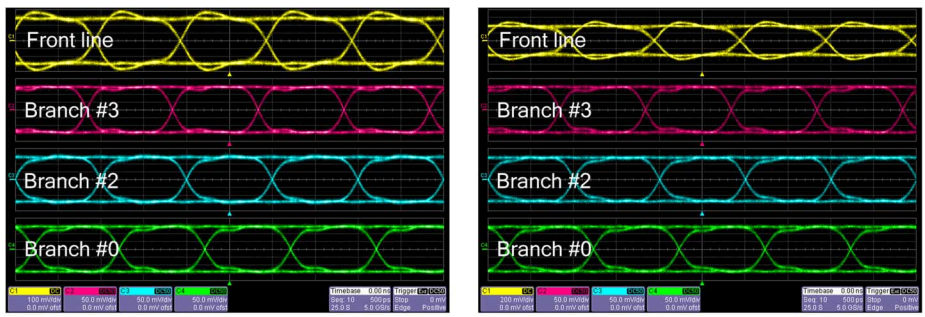
In order to measure the raw front line impedance and to verify if any reflections occur, we performed a TDR measurement directly on the front line with the master-side matching resistor ($Z_0 - Z_F$ in Fig. 12) short-circuited. The TDR measurement results are presented in Fig. 14. The plateau and flat portions in the waveform correspond to the 50 Ω connecting cable and the lines on the test board beyond the input connector, respectively. Once the step signal enters the front line, there are no further reflections for the forward propagating signal, so the flat portion is maintained afterwards.

Although the measured waveforms display some minor reflections caused by the connectors and the short stubs around the matching resistors, it can be seen that the overall bus impedances are matched well without severe reflections.



(a) (b)

Fig. 14. TDR measurement waveforms without master-side impedance matching for selected bus configurations: (a) 25-33.3-50-50 and (b) 33.3-33.3-50-50. The vertical axis represents the measured reflection coefficient (scale 200 m/div, offset 2 div).



(a) (b)

Fig. 15. Measured waveforms of the forward propagation case signals for selected bus configurations: (a) 25-33.3-50-50 and (b) 33.3-33.3-50-50. Front line signal scale: (a) 100 mV/div and (b) 200 mV/div. Branch signal scale: 50 mV/div.

TABLE IV
MEASURED VOLTAGE SWINGS AND RATIOS

Bus line configuration	Z_0/Z_F	Forward case			Backward case		
		Source swing	Receiver swing	Voltage ratio	Source swing	Receiver swing	Voltage ratio
12.5−16.7−25−50	4.0	0.286	0.289	1.01	1.14	0.272	0.239
25−33.3−50−50	2.0	0.579	0.290	0.501	1.14	0.280	0.246
33.3−33.3−50−50	1.5	0.771	0.289	0.375	1.14	0.281	0.246
50−50−50−50	1.0	1.16	0.286	0.247	1.14	0.283	0.248

Voltage swings are in volts (p-p). Ratios are dimensionless.

B. Forward Propagation Case

For the signal measurement in the forward propagation case, we connected the signal generator output to the master-side input port, and measured the output signals coming out from branches 3, 2 and 0. The unused branch 1 was properly terminated in 50 Ω.

The voltage swing of the source signal was measured at the front line input (contact point between the matching resistor and the front line itself) using an active probe. Two instances of the measured waveforms for the forward propagation case (25-33-50-50 and 33.3-33.3-50-50, respectively) are given in Fig. 15. The measured voltage swing values from the waveforms are summarized on the left side of Table IV. Fig. 16 shows the measured eye diagrams for the 25-33-50-50 bus configuration at 5 Gbps.

C. Backward Propagation Case

For the signal measurement in the backward propagation case, we connected the signal generator output to each branch port one by one, and measured the received signal at the master port. In order to facilitate the measurement, the master-side connection was modified so that the master-side received signal at the front line could be measured using a standard 50 Ω cable. The front line was connected directly to the master-side connector, and the resulting impedance mismatch was resolved through an additional parallel resistance to ground. No modification was done on the test board with $Z_F = 50\ \Omega$.

Since the source signal at the branch end suffers from reflections caused by impedance mismatch, we cannot measure the source voltage swing directly using an active probe, so instead we performed an indirect measurement using the inverting output of the signal generator (inverted replica). The measured

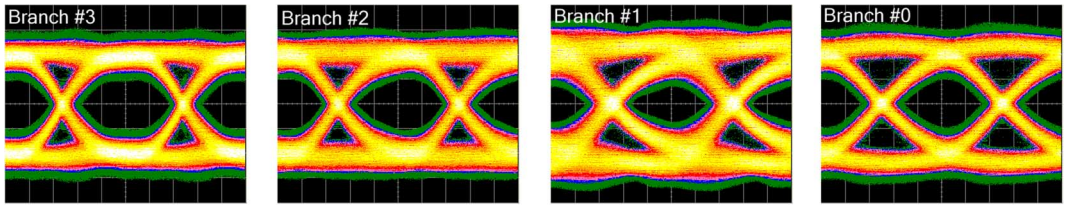


Fig. 16. Measured eye diagrams of the forward propagation case for the 25-33.3-50-50 line configuration ($Z_F = 25\ \Omega$) at 5 Gbps: (a) branch #3, (b) branch #2, (c) branch #1, and (d) branch #0.

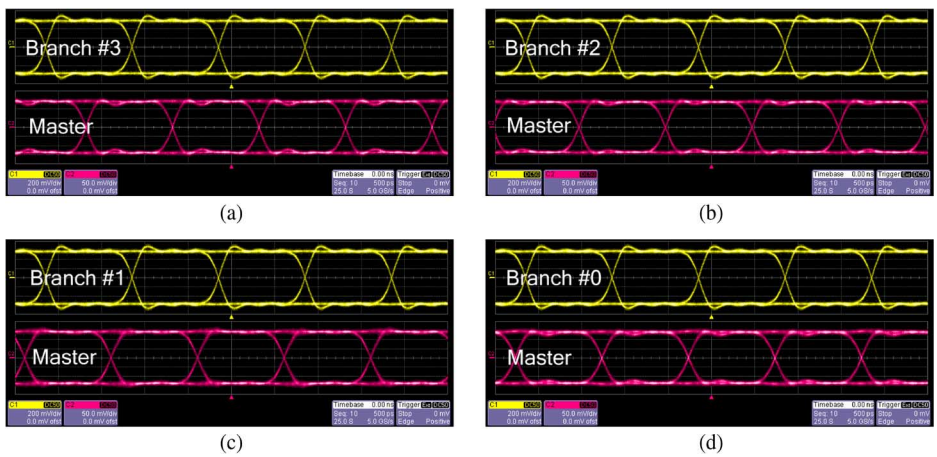


Fig. 17. Measured waveforms of the backward propagation case signals for the 25-33.3-50-50 line configuration ($Z_F = 25\ \Omega$): (a) branch #3, (b) branch #2, (c) branch #1, and (d) branch #0. The branch source signals were measured using the inverted replica output signal. Branch source signal scale: 200 mV/div. Master received signal scale: 50 mV/div.

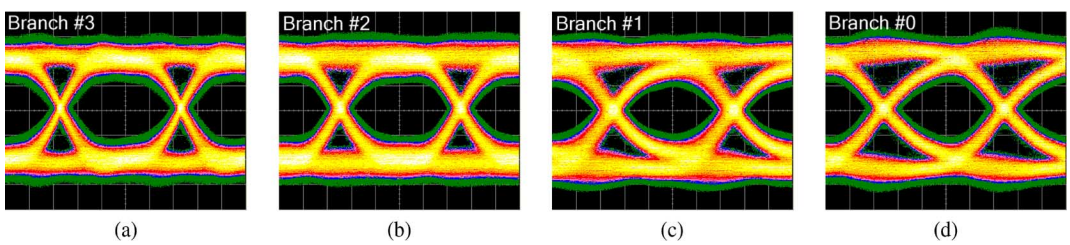


Fig. 18. Measured eye diagrams of the backward propagation case for the 25-33.3-50-50 line configuration ($Z_F = 25\ \Omega$) at 5 Gbps: (a) branch #3, (b) branch #2, (c) branch #1, and (d) branch #0.

waveforms for the backward propagation case are given in Fig. 17. Since the results for all test boards are similar, we present the waveforms for only one test board (25-33.3-50-50). The measured voltage swing values from the waveforms are summarized on the right side of Table IV. Fig. 18 shows the measured eye diagrams for the 25-33-50-50 bus configuration at 5 Gbps.

D. Evaluation of the Measurement Results

Comparing the measured voltage swing ratios given in Table IV with those in Table II, we can verify that the measured results show good agreement with the theoretically estimated values given by (20) and (27). Moreover, the measured voltage swing ratio for the backward propagation case has approximately the same value regardless of Z_F, which also agrees with the result expected from (27).

The eye measurement results show clear eye openings at 5 Gpbs, which means that we can use the proposed bus scheme without pre-emphasis or equalization up to 5 Gbps. This result is better than those shown in [1] and [2] (3.2–3.3 Gbps), which clearly shows the significant benefits of impedance matching. The data rate may be extended beyond 5 Gbps by reducing the parasitic effects with the use of a component-embedded PCB, in addition to incorporating pre-emphasis and equalization.

VI. Conclusion

In this paper, we presented a bus design scheme aimed at both impedance matching and uniform power delivery using non-uniform impedance lines. The scheme achieves this both by varying the line impedances and by inserting matching resistors. The analysis shows that the overall power efficiency of the bus is determined solely by the number of branches and the ratio between the master-side and branch-side line impedances. For any given power efficiency point, the derived equations can calculate the optimal set of resistance and line impedance values. In general, there is a trade-off between the master-side line impedance (thus the line width) and the power efficiency,

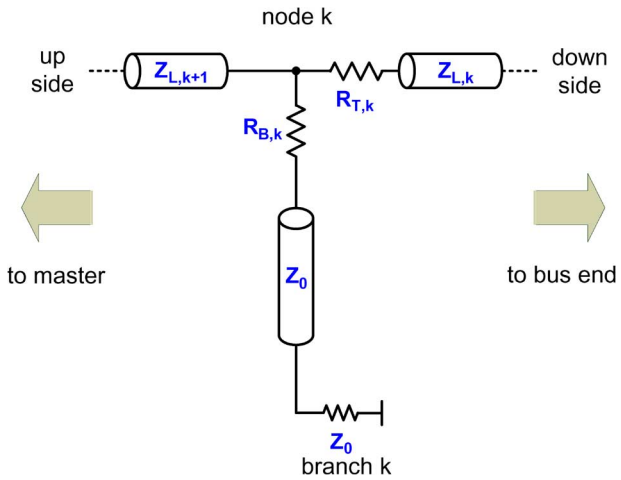


Fig. 19. Definition of "*up*" and "*down*" sides at a branching node.

and the proposed multidrop bus scheme allows circuit designers to find a proper balance best suited for the application.

For verification of the feasibility of the presented scheme and the validity of the derived equations, we implemented several test boards with different line impedance configurations. The voltage swing measurement results show good agreement with the theoretically estimated values, and the high frequency eye measurement results show reliable performance up to a bit rate of 5 Gbps, clearly showing the significant benefits of impedance matching.

Appendix
Detailed Derivation of the Voltage and Power Relationship in the Backward Propagation Case

In this appendix, we will present a thorough step-by-step derivation of the voltage relationship for the backward propagation case without applying the reciprocity theorem.

A. Conventions and Definitions

Before proceeding into the detailed derivation, we will first present some conventions and definitions used in this appendix.

In order to simplify the notation of the signal transmission path, we will denote the master and bus end sides at each branching node as the "*up*" and "*down*" sides, respectively (Fig. 19).

Also, since every branching node circuit has a similar T-shaped structure, we will define a general "*T-node*" circuit (Fig. 20) in order to simplify the calculations.

B. Transmission Coefficient at a T-node

The transmission coefficient upon impedance discontinuities (with Z_1 as the source side) is given by the telegrapher's equation ([10]–[12]) as

$$T = \frac{2Z_2}{Z_1 + Z_2}. \tag{35}$$

A general branching node can be modelled as a T-node circuit (Fig. 20). Ports S and T denote the signal source and destination

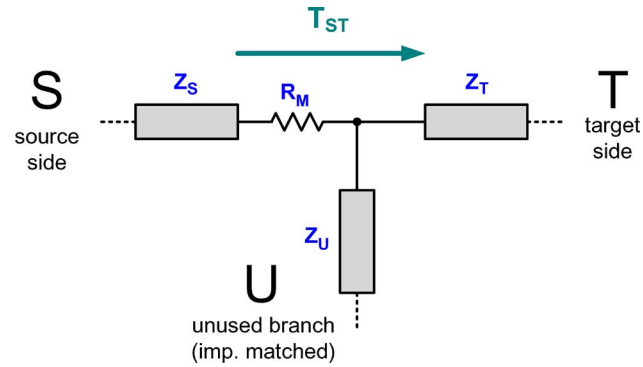


Fig. 20. Circuit model for a general T-node.

ports, respectively, and port U represents the unused branch. Applying (35) to this circuit the transmission coefficient from ports S to T becomes

$$T_{ST} = \frac{2(Z_T//Z_U)}{(Z_T//Z_U) + (Z_S + R_M)}. \tag{36}$$

Using this equation with appropriate mapping of ports S, T, and U we can derive the transmission coefficients for either source or intermediate nodes.

C. Node k as Source (Branch to Up)

Branch k $(1 \le k \le N-1)$ as signal source can be modelled as a general T-node with the source branch k as S, the up side as T, and the down side as U [Fig. 21(a)]. Thus, the individual terms in (36) become

$$\begin{aligned} Z_S + R_M &= Z_0 + R_{B,k} \\ &= (k+1) \cdot Z_{L,k+1} \end{aligned} \tag{37}$$

$$\begin{aligned} Z_T//Z_U &= Z_{L,k+1}//(Z_{L,k} + R_{T,k}) \\ &= \left(\frac{k+1}{2k+1}\right) \cdot Z_{L,k+1} \end{aligned} \tag{38}$$

and (36) is reduced to

$$T_{B,k} = \frac{1}{k+1} \quad (1 \le k \le N-1). \tag{39}$$

In the special case of branch 0 (final branch) [Fig. 21(b)], we can treat as $Z_U = \infty$, and thus $Z_T//Z_U = Z_{L,1}$ and $T_{B,0} = 1$, which is equal to (39) with $k = 0$. Thus the source branch transmission coefficient can be simply written as

$$T_{B,k} = \frac{1}{k+1} \quad (0 \le k \le N-1) \tag{40}$$

for all branches.

D. Node j as Intermediate Node (Down to Up)

An intermediate node j $(1 \le j \le N-1)$ can be modelled as a general T-node with the down side as S, the up side as T, and the non-target branch j as U [Fig. 21(c)]. Thus, the individual

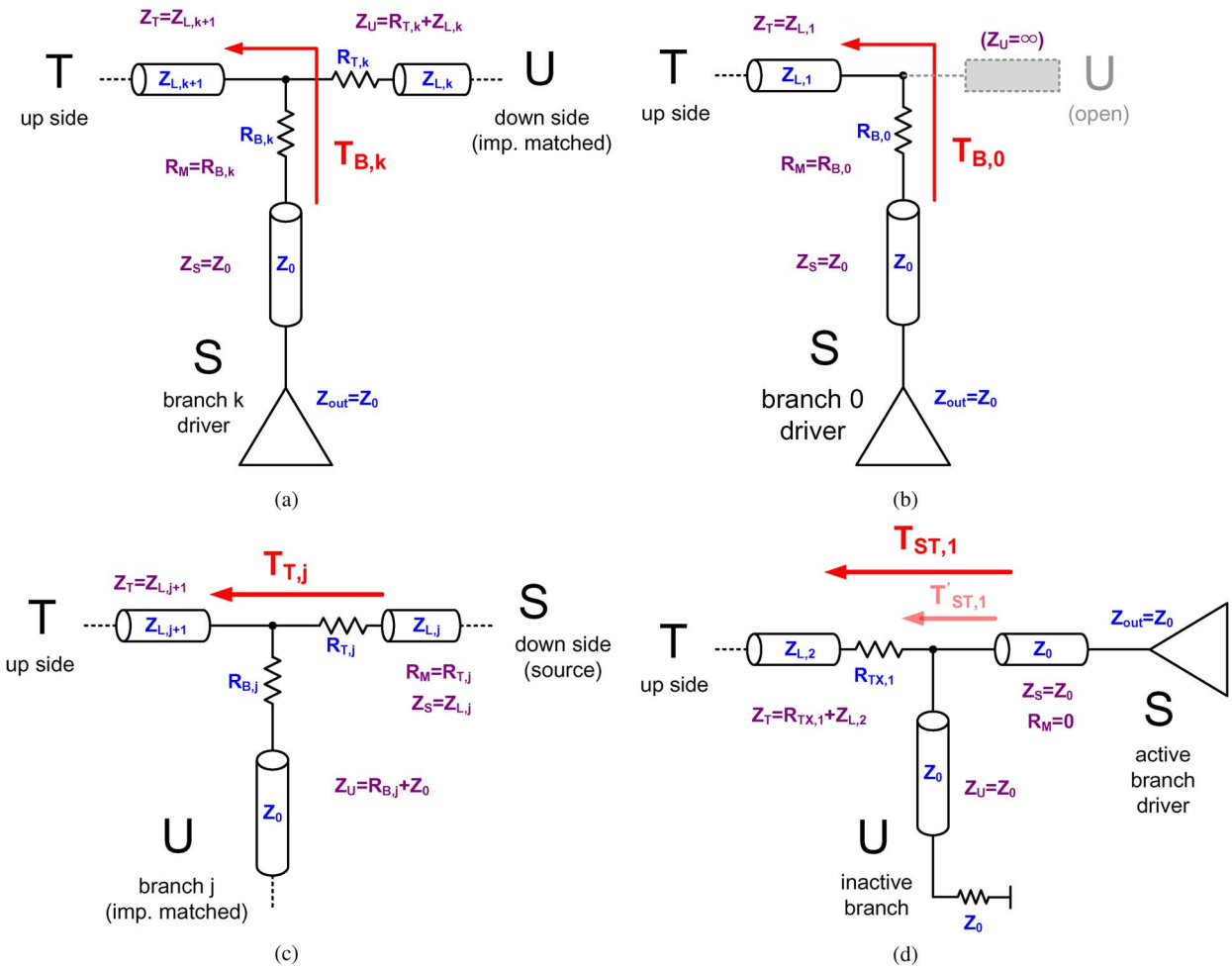


Fig. 21. Modelling of (a) source branch k ($k > 0$), (b) final branch ($k = 0$) as signal source, (c) intermediate node j, and (d) symmetrical final branches (branches 0 and 1) with reduction. The arrows show the signal transmission paths of interest.

terms in (36) become

$$\begin{aligned} Z_S + R_M &= Z_{L,j} + R_{T,j} \\ &= \left(\frac{j+1}{j}\right) \cdot Z_{L,j+1} \end{aligned} \tag{41}$$

$$\begin{aligned} Z_T//Z_U &= Z_{L,j+1}//(Z_0 + R_{B,j}) \\ &= \left(\frac{j+1}{j+2}\right) \cdot Z_{L,j+1} \end{aligned} \tag{42}$$

and (36) is reduced to

$$T_{T,j} = \frac{j}{j+1} \quad (1 \le j \le N-1). \tag{43}$$

E. Final Segment With Symmetrical Branch Reduction

A final segment with symmetrical branch reduction can be modelled as a modified T-node with $R_M = 0$ and an additional voltage divider on the T side output [Fig. 21(d)]. Since there is no difference whether which exact branch (0 or 1) is the source, we can model either case using the same circuit, with the source branch as S, the inactive one as U, and the up side as T. Thus, the individual terms in (36) become as follows:

$$Z_S + R_M = Z_S = Z_{L,1} = Z_0 \tag{44}$$

$$Z_T = Z_{L,2} + R_{TX,1} = 2Z_{L,2} - \frac{Z_0}{2} \tag{45}$$

$$Z_T//Z_U = Z_T//Z_0. \tag{46}$$

Using these terms, (36) is reduced to

$$T'_{ST,1} = \frac{2(Z_T//Z_0)}{(Z_T//Z_0) + Z_0}. \tag{47}$$

Taking into consideration the effect of the voltage divider, the overall transmission coefficient is calculated as

$$\begin{aligned} T_{ST,1} &= T'_{ST,1} \cdot \frac{Z_{L,2}}{Z_{L,2} + R_{TX,1}} \\ &= \frac{2(Z_T//Z_0)}{(Z_T//Z_0) + Z_0} \cdot \frac{Z_{L,2}}{Z_T} \\ &= \frac{2Z_0 Z_{L,2}}{2Z_T Z_0 + Z_0^2} \\ &= \frac{2Z_0 Z_{L,2}}{2(2Z_{L,2} - \frac{Z_0}{2})Z_0 + Z_0^2} \\ &= \frac{1}{2} \end{aligned} \tag{48}$$

and thus

$$T_{B,1} = T_{B,0} \cdot T_{T,1} = T_{ST,1} = \frac{1}{2}. \tag{49}$$

This is equal to the value calculated from the individual terms given by (40) and (43) with appropriate values of k and j. Thus, we can verify that (40) and (43) are valid also in the case of reduced symmetrical final branches.

F. Overall Transmission Coefficient

Using (40) and (43), the overall backward transmission coefficient can be calculated as

$$T_{\text{back}}|_{N-1} = T_{B,N-1} = \frac{1}{N} \tag{50}$$

for the foremost branch $(k = N-1)$ and

$$\begin{aligned} T_{\text{back}}|_k &= T_{B,k} \cdot \prod_{j=k+1}^{N-1} T_{T,j} \\ &= T_{B,k} \cdot \prod_{j=k+1}^{N-1} \frac{j}{j+1} \\ &= \frac{1}{N} \quad (0 \le k \le N-2) \end{aligned} \tag{51}$$

for all other branches. Since this value is independent of k, it can be simply written as

$$T_{\text{back}} = \frac{1}{N}. \tag{52}$$

Assuming matched termination at the receiver (master), this value is equal to the received voltage swing ratio

$$\left.\frac{V_{RX}}{V_{INC}}\right|_{\text{back}} = T_{\text{back}} = \frac{1}{N}. \tag{53}$$

This result is the same as (27), which was derived by applying the reciprocity theorem.

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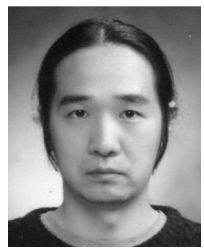

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