A 2.9-to-4.0GHz Fractional-N Digital PLL with Bang-Bang Phase Detector and 560fsrms Integrated Jitter at 4.5mW Power

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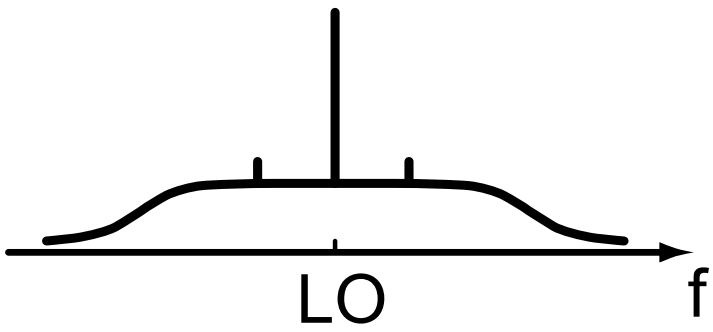
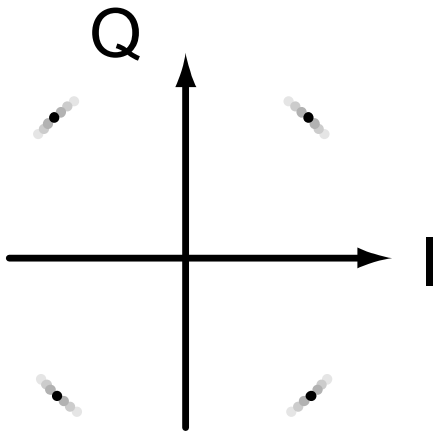
Motivation

- Wideband radios with **higher SNR** (e.g. WiMax)
- Lower **absolute jitter** of LO
- Both **fractional spurs** and **phase noise** contribute to jitter
- Target is efficiency **(low jitter at low power)**

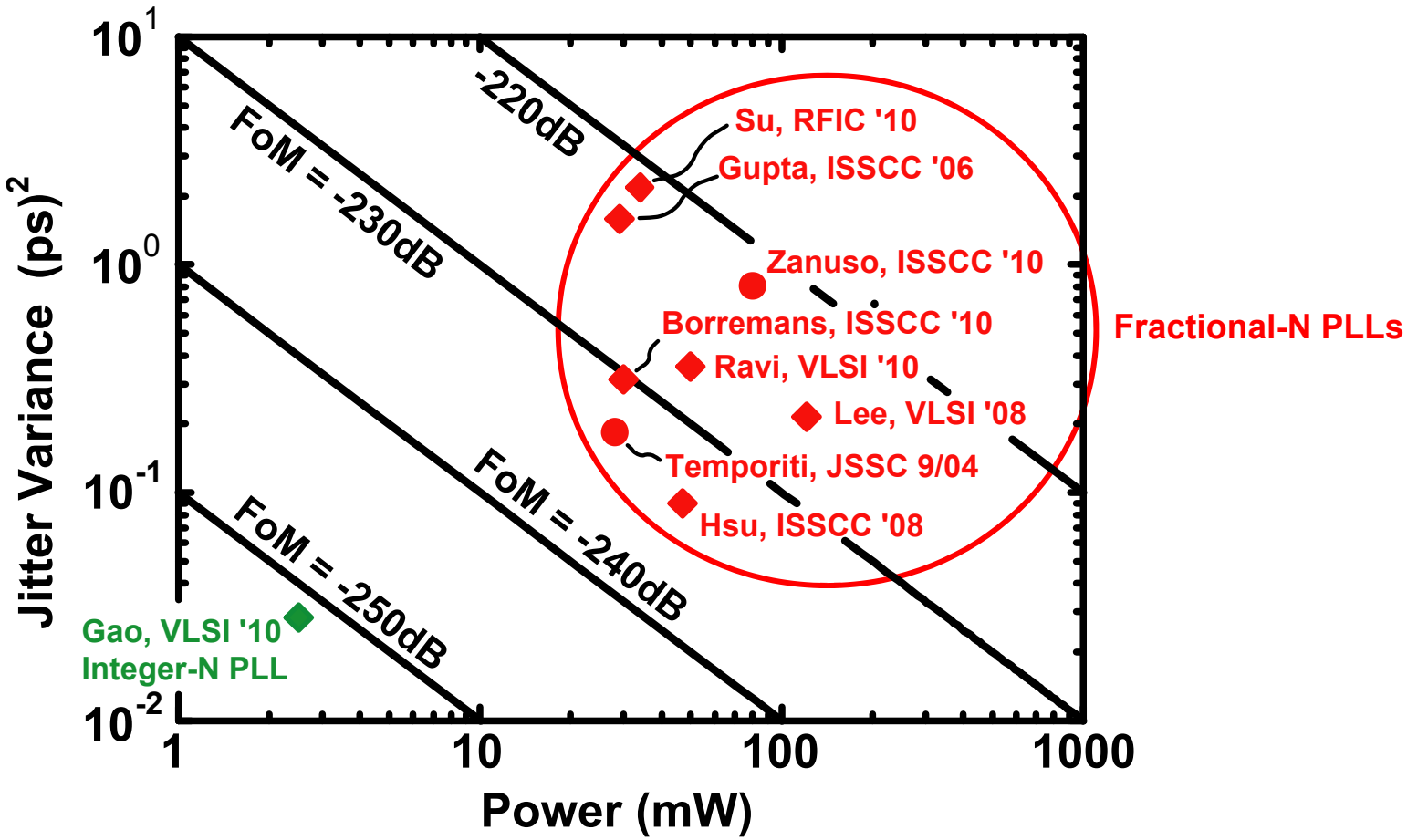




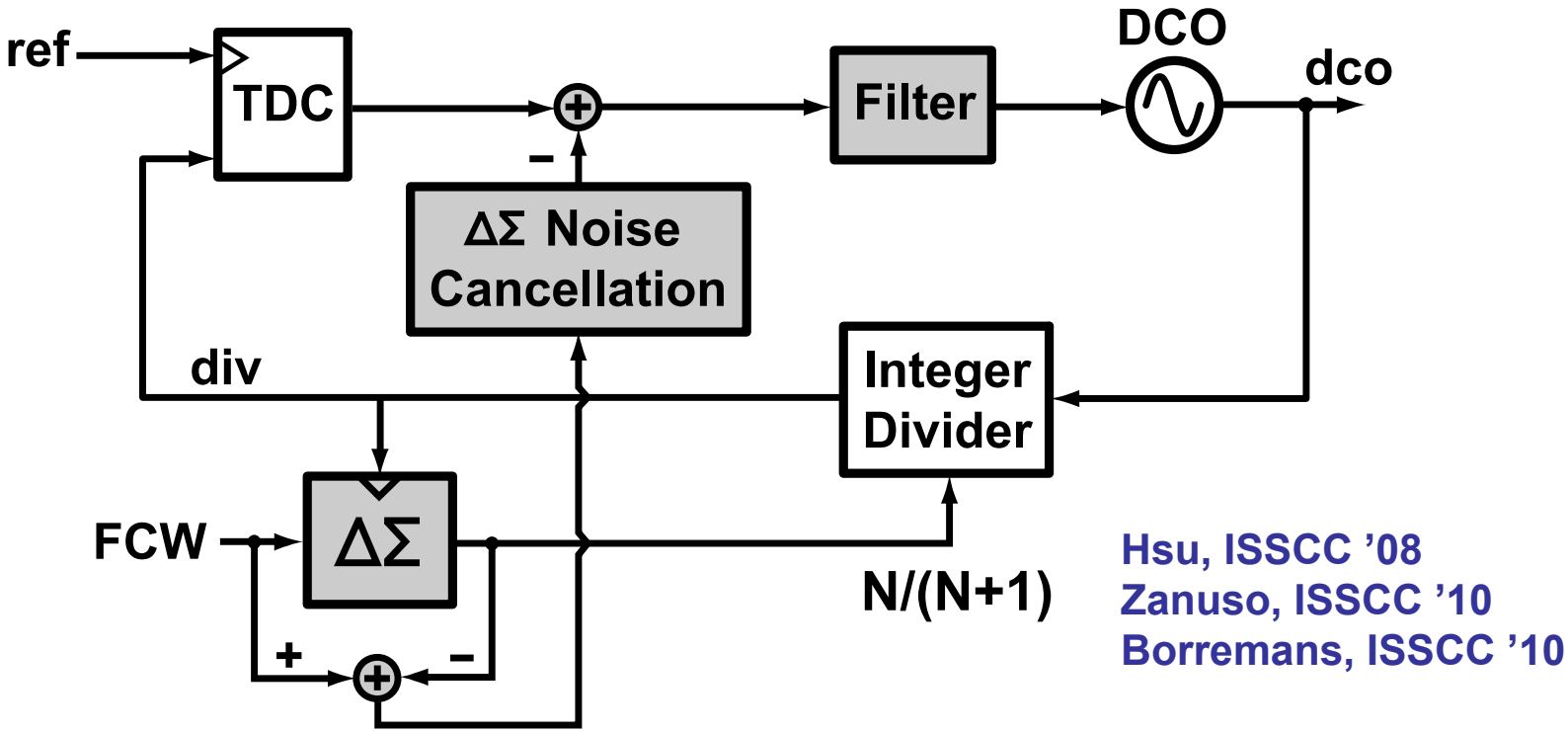
Efficiency: Figure of Merit

$$FoM = 10 \cdot \log\left[\left(\frac{Jitter}{1s}\right)^2 \cdot \left(\frac{Power}{1mW}\right)\right]$$

Gao, TCAS-II, 2009



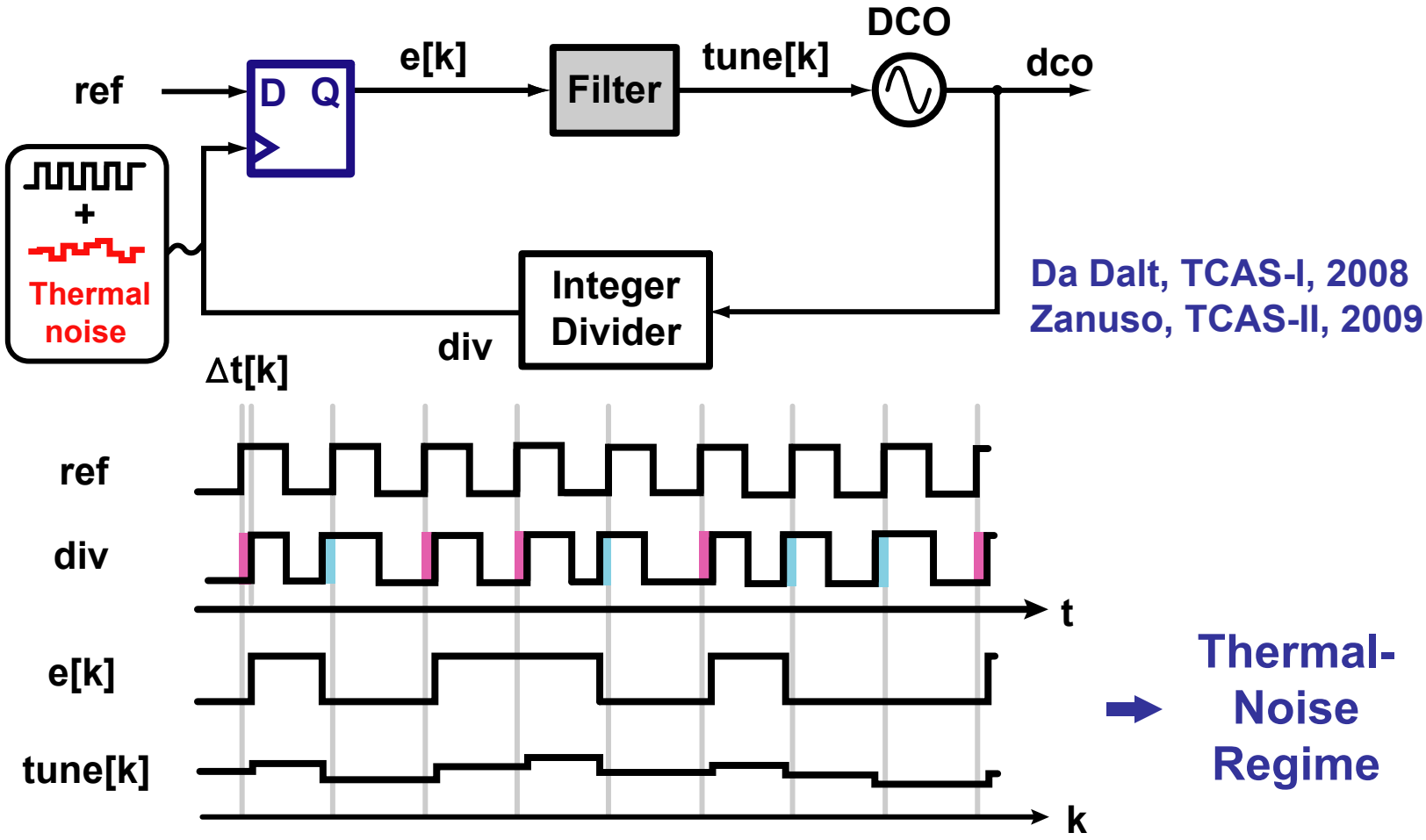
Digital Fractional-N PLLs



- Low spur and low noise require **TDC with high resolution and linearity**
- High-performance TDCs burn **large power**

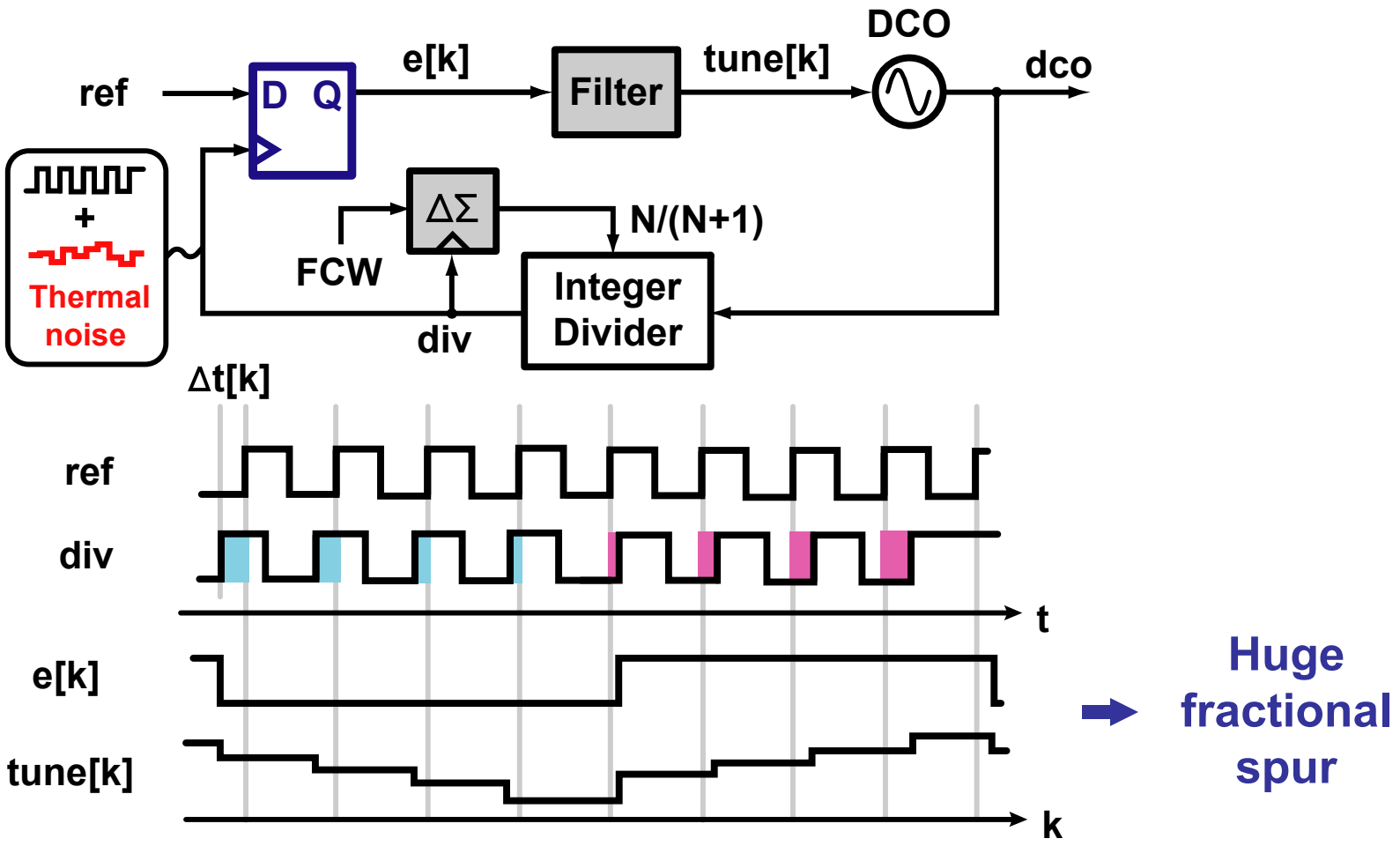
Can we use a single-bit TDC?

Integer-N PLL with 1b-TDC



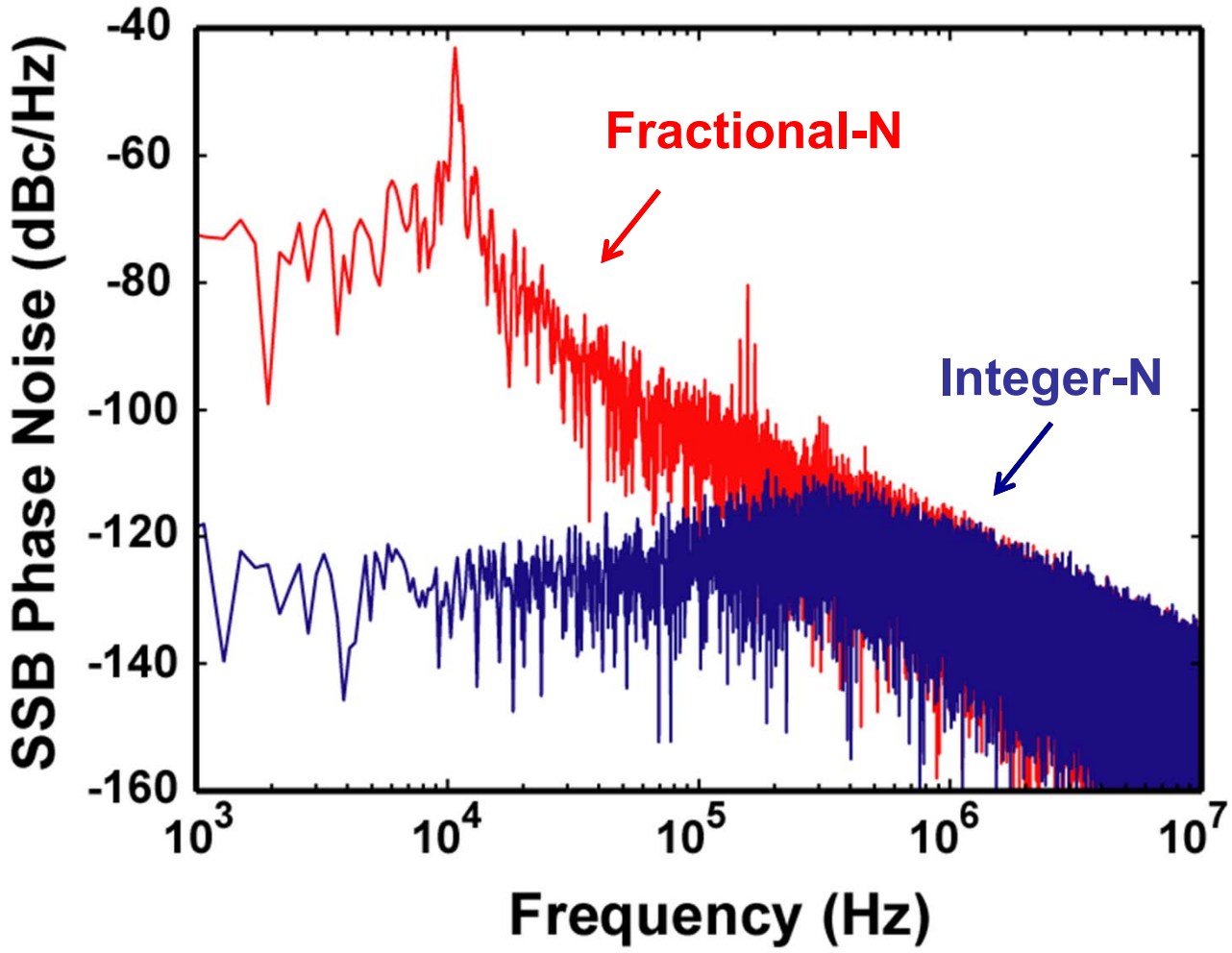
- The time average of e[k] **accurately** and **linearly** measures Δt

Is Fractional-N PLL with 1b-TDC feasible?

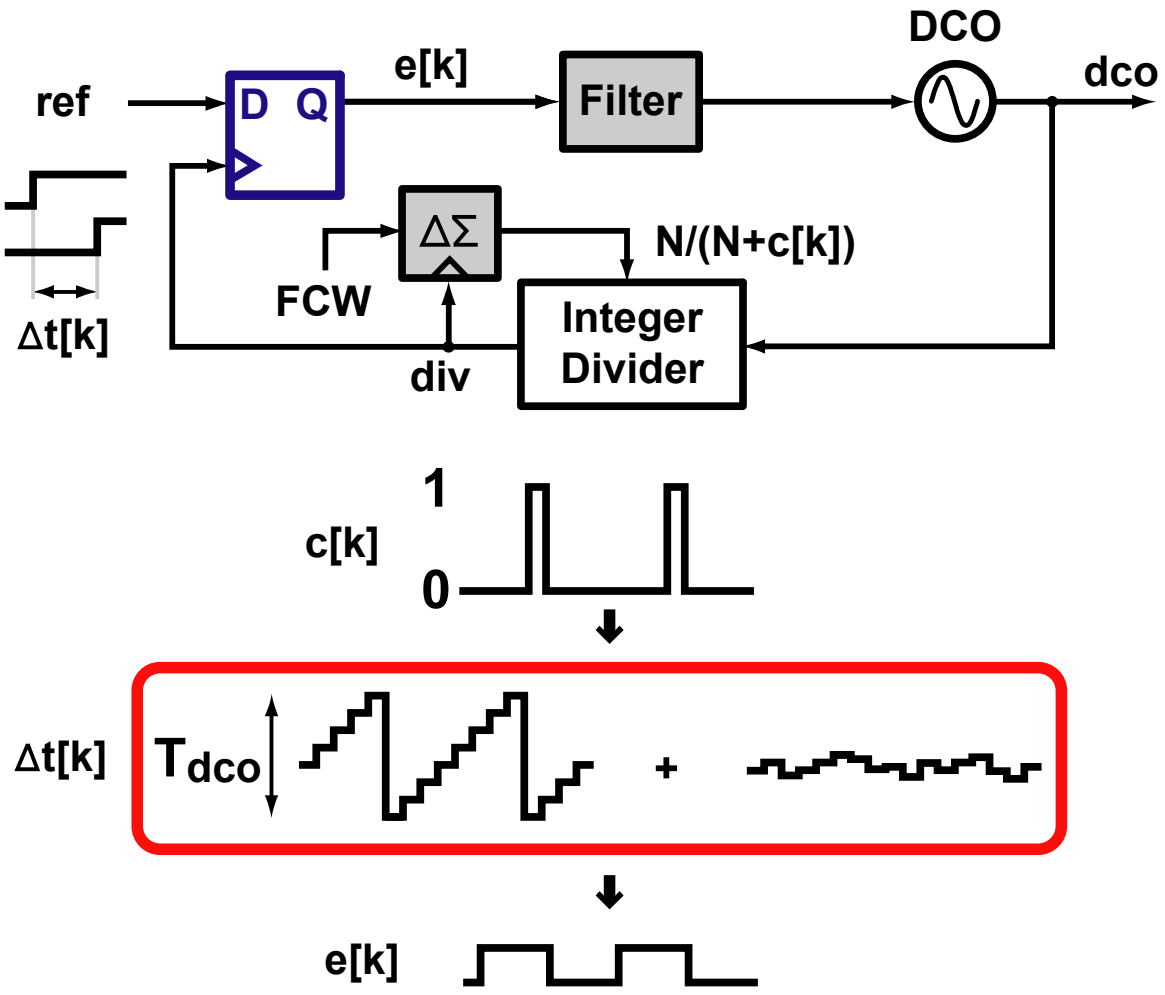


- Divider dithering would produce Δt much larger than thermal component

Phase Noise Spectra of PLLs with 1b-TDC



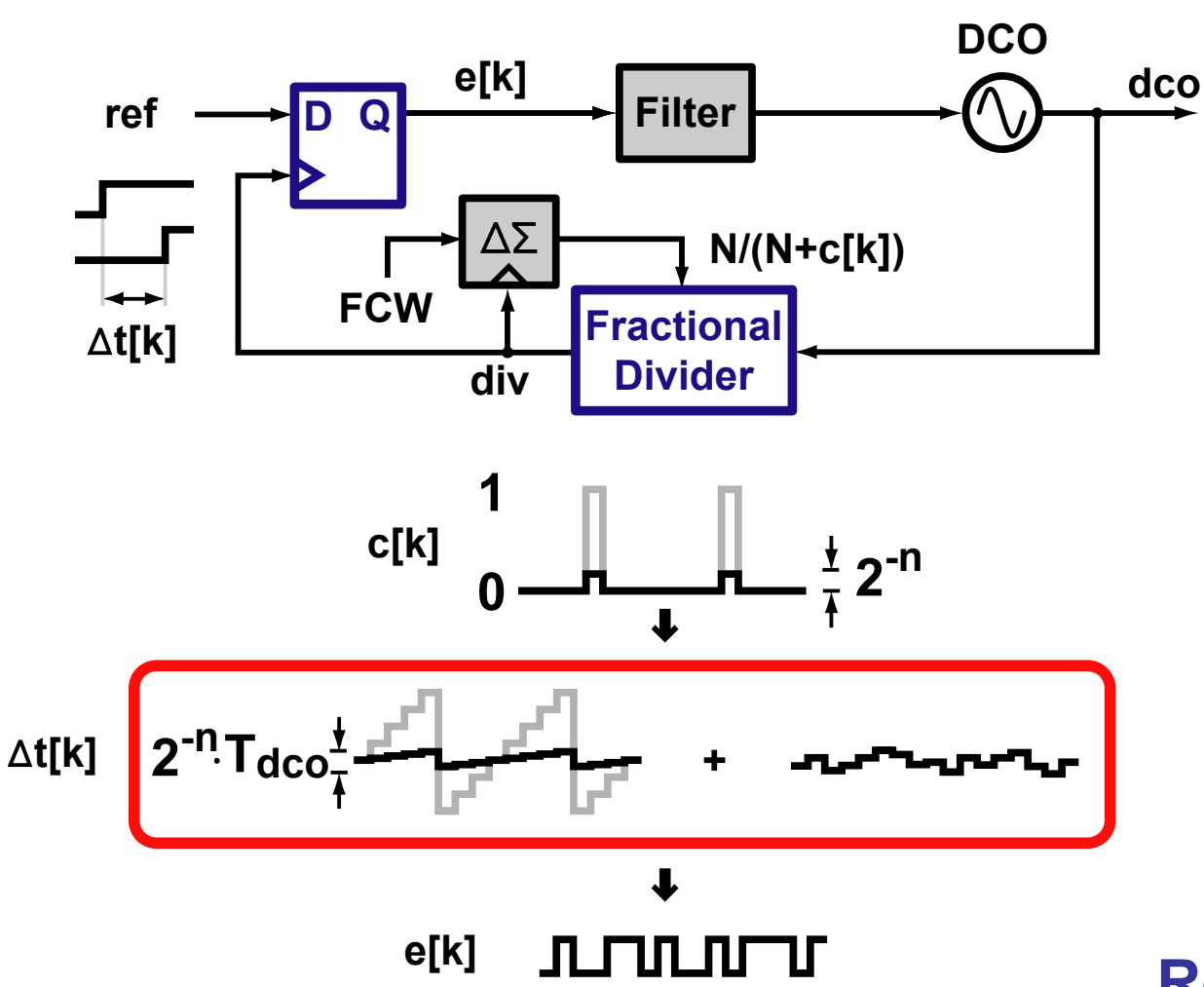
Dominating ΔΣ Dithering Signal



The deterministic ΔΣ dithering wide as T_{dco} **(100's of ps)** dominates over thermal noise **(100's of fs_{rms})**

Fractional periodicity

Introduction of Fine Fractional-N Divider



Fine n-bit Fractional-N Divider

⬇

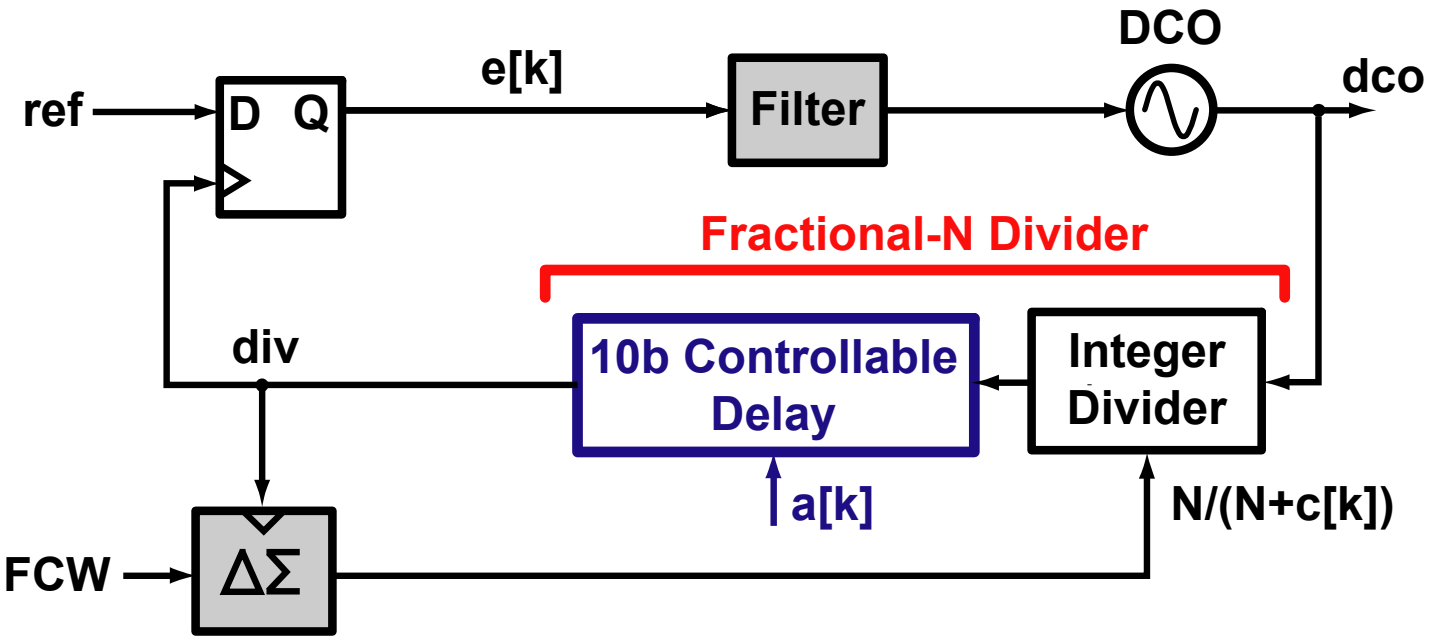
The deterministic ΔΣ dithering is reduced by about 1,000 **(if n=10)**

⬇

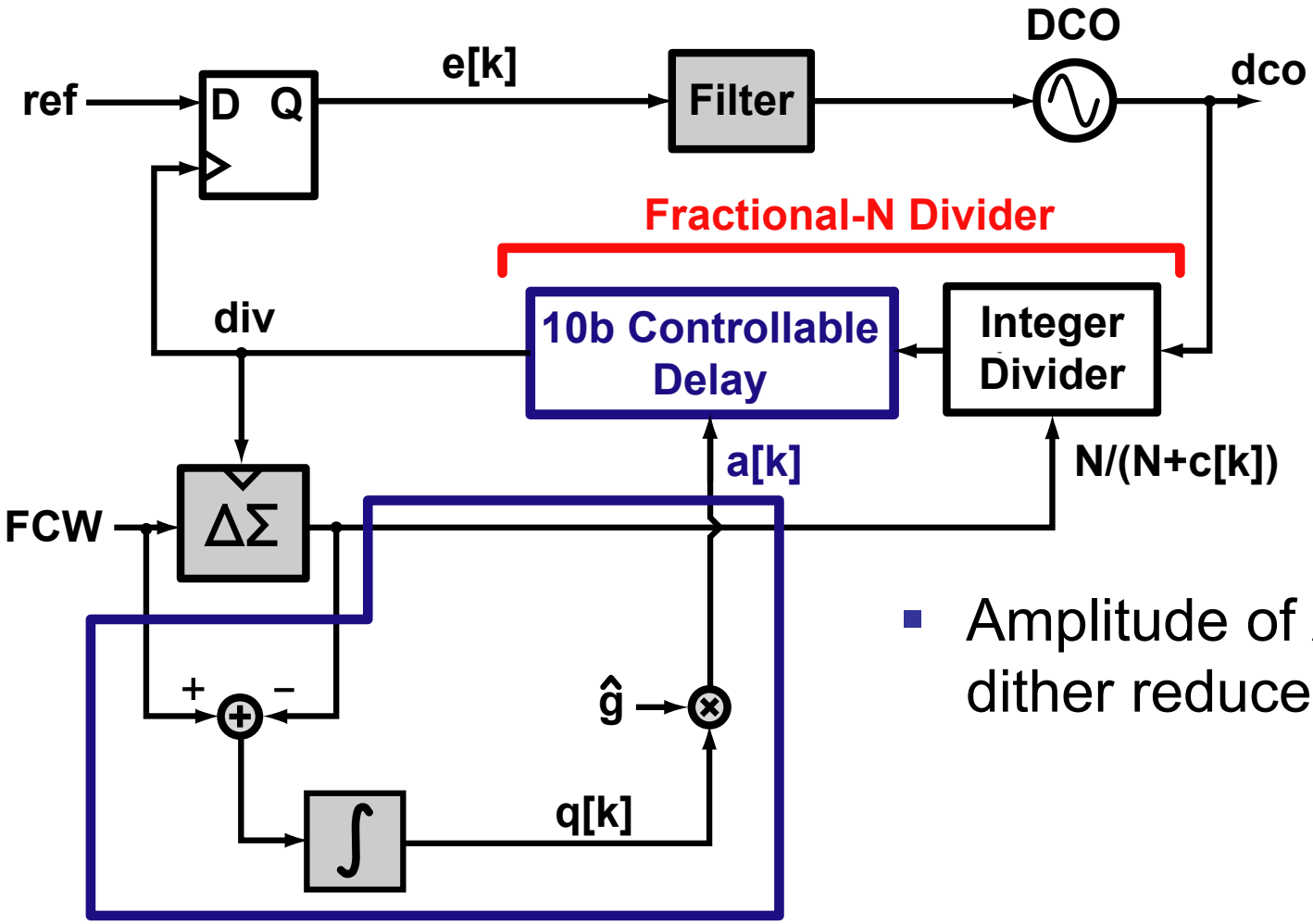
Thermal-Noise Regime is recovered

How can we achieve 10b equivalent resolution in a fractional-N divider?

Proposed Architecture

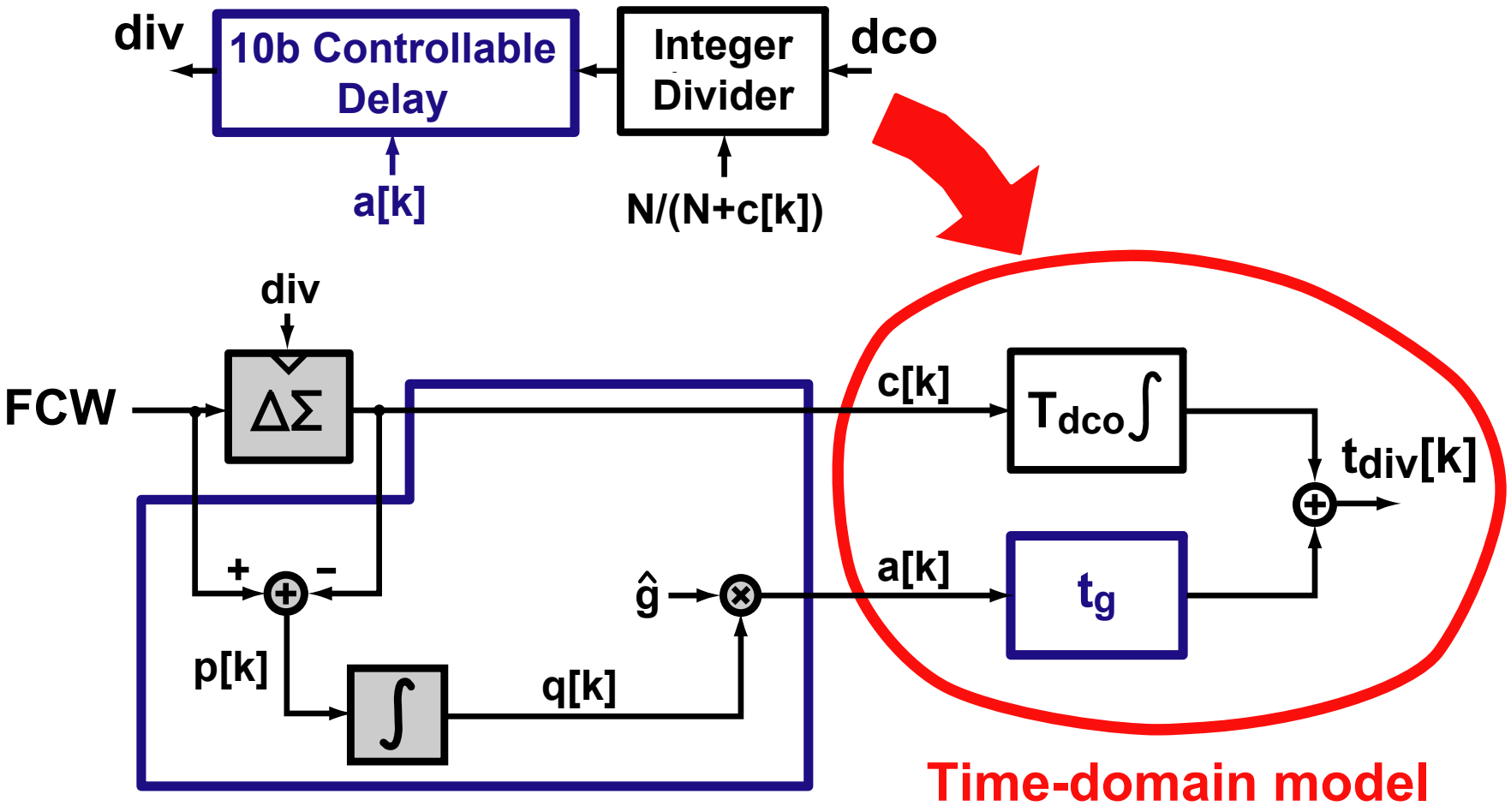


Proposed Architecture (cont'd)

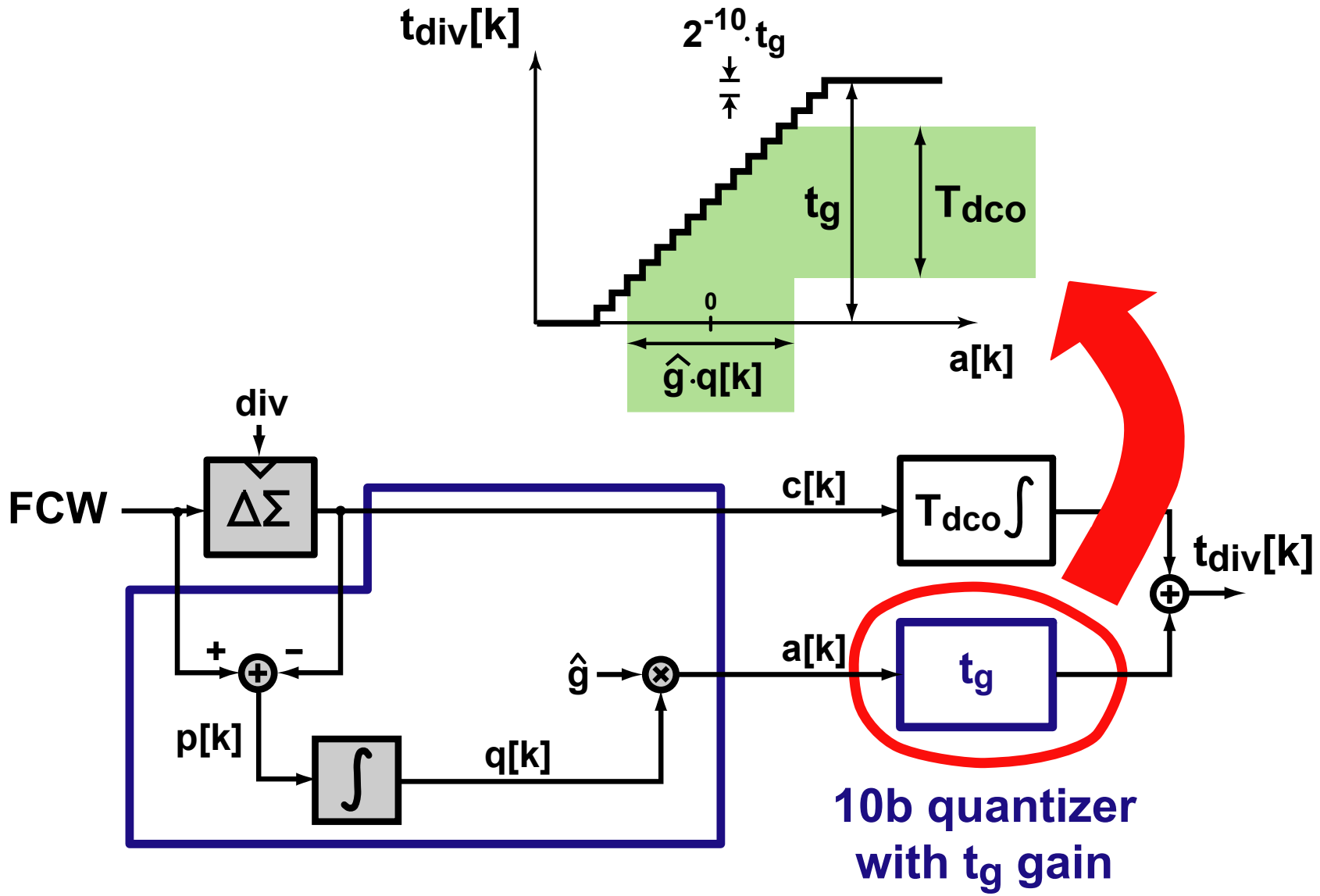


- Amplitude of ΔΣ dither reduced by 2^{10}

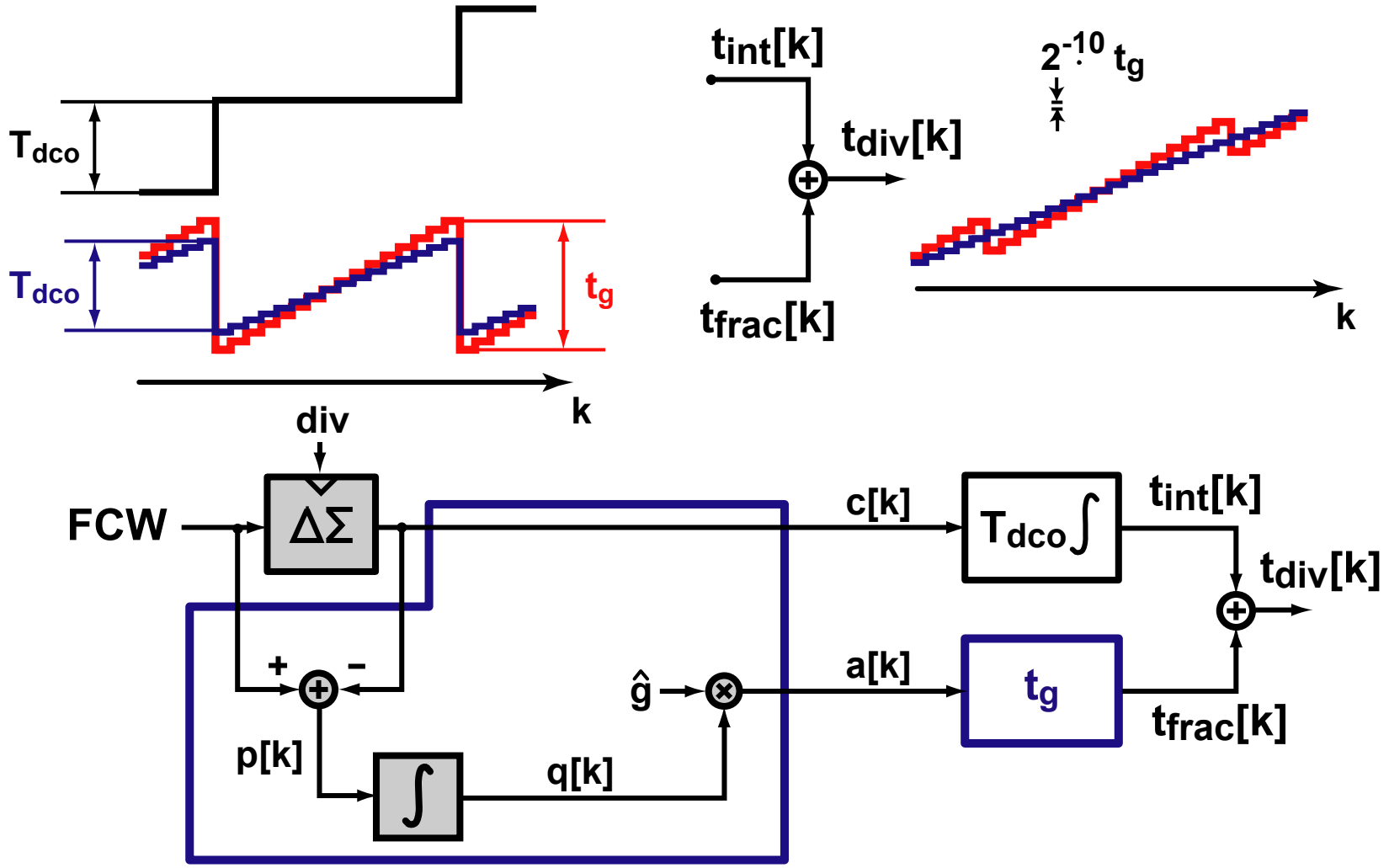
Basic Principle of Proposed Architecture



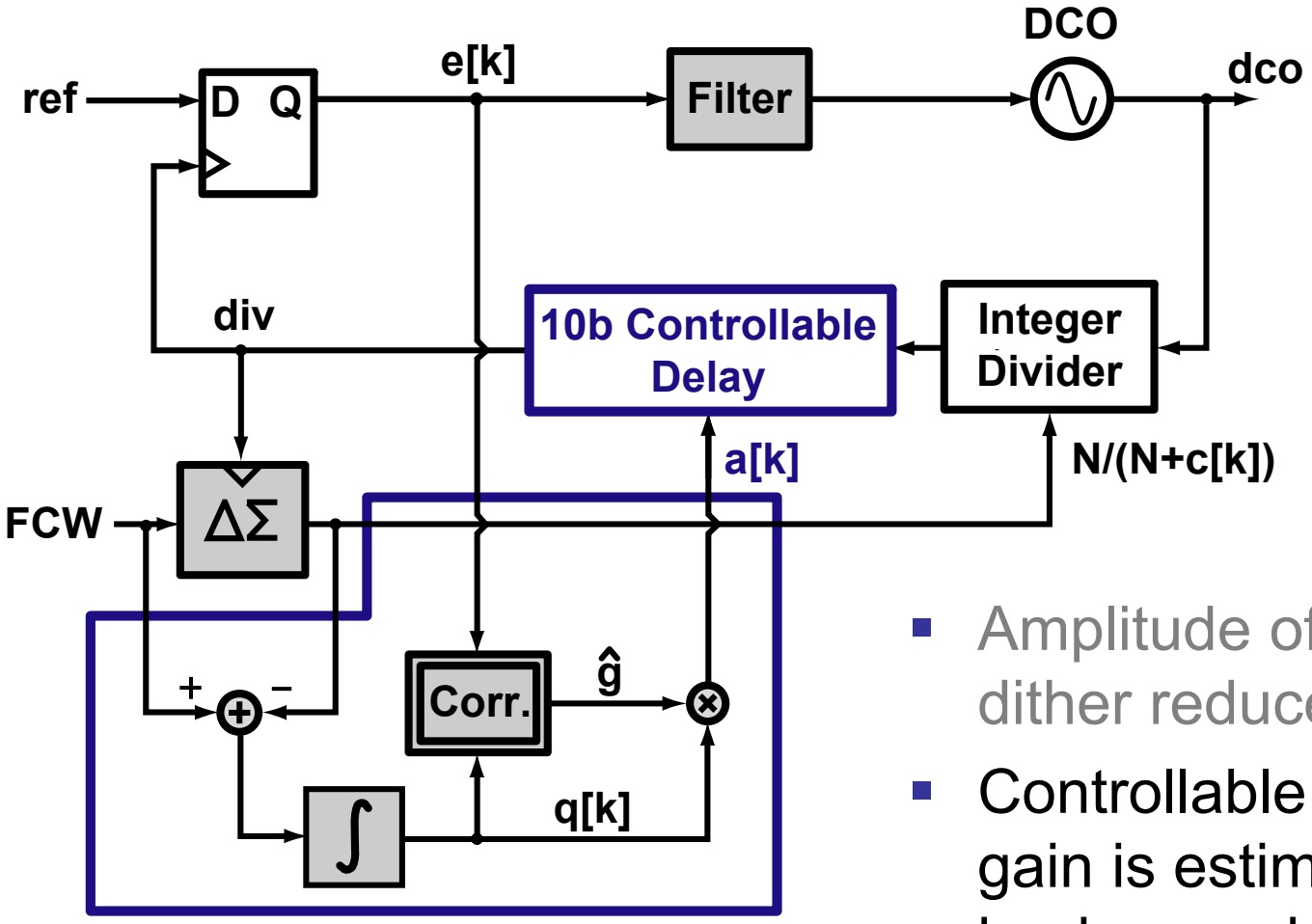
Range Adaptation of Controllable Delay



Correct Interpolation of Phase Ramp



Proposed Architecture with Gain Estimation



- Amplitude of ΔΣ dither reduced by 2^{10}
- Controllable delay gain is estimated in background

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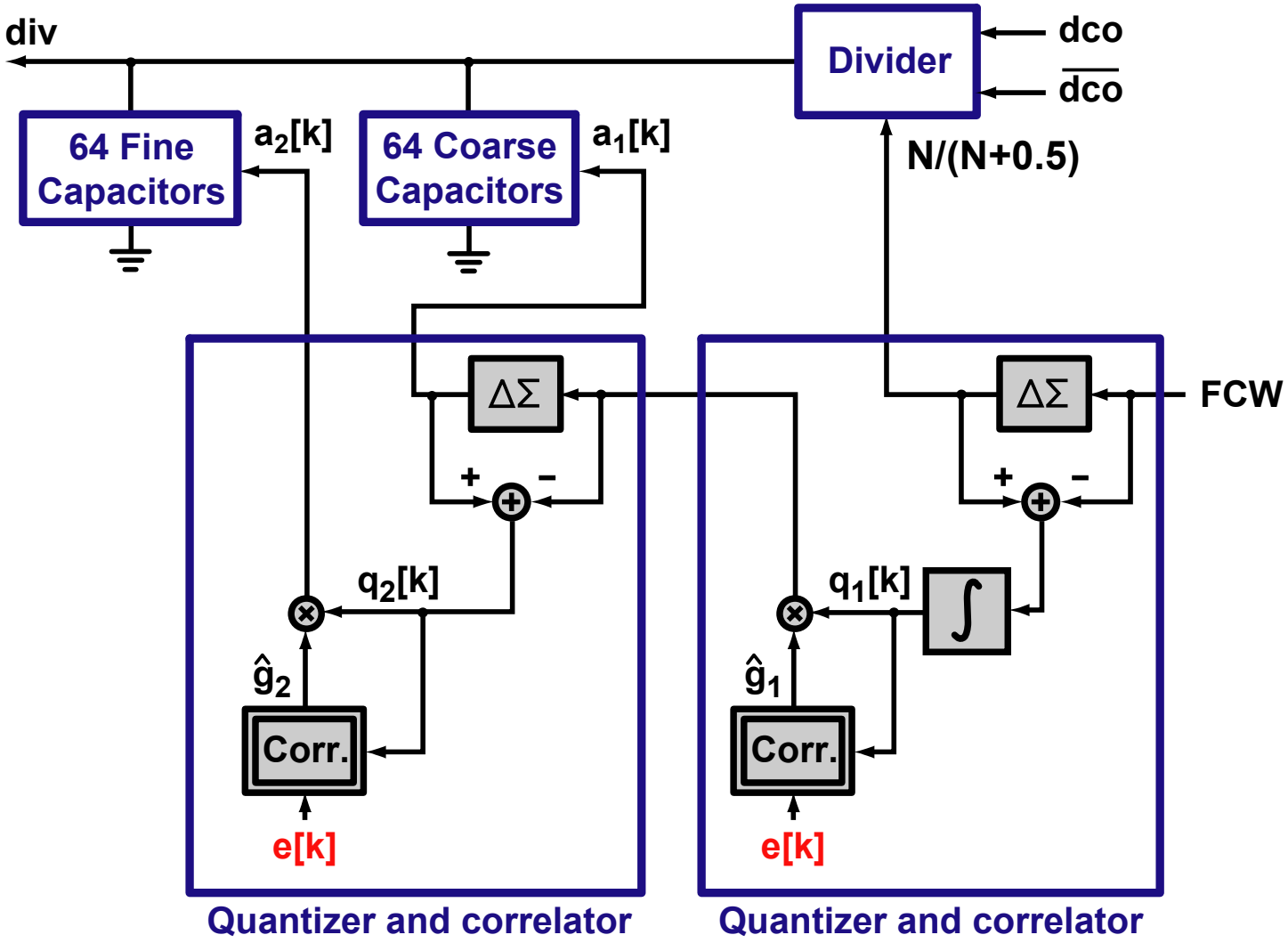
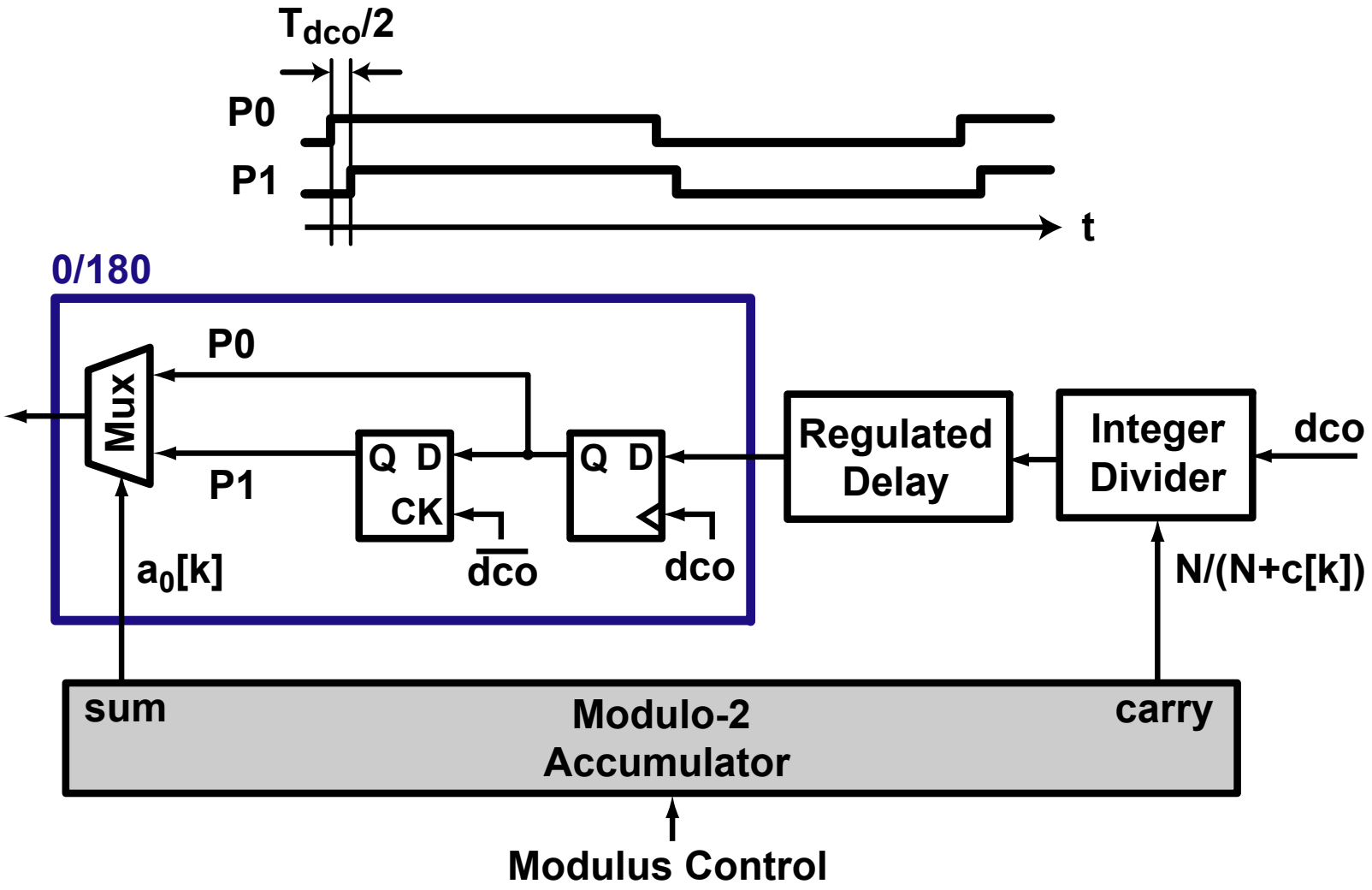
Controllable Delay Implementation

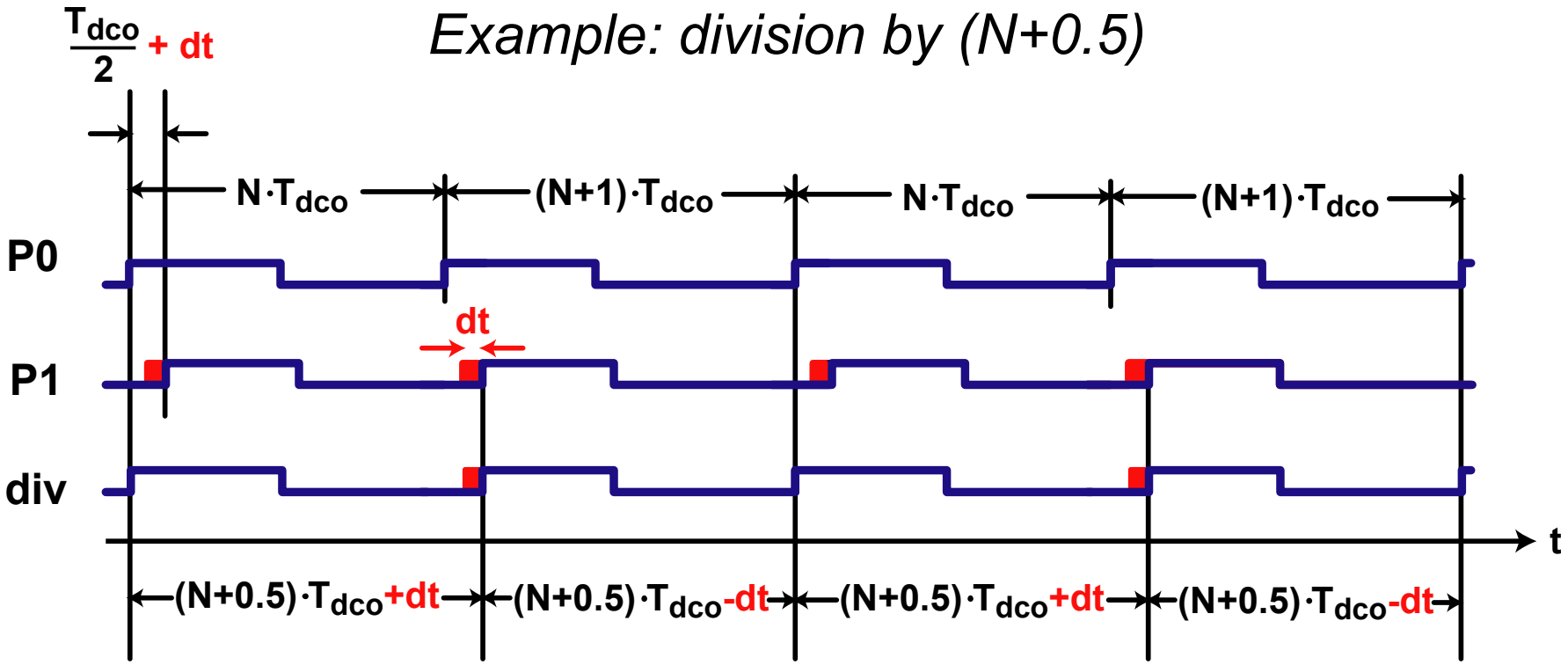
Segmented Implementation



Dual-Modulus N/(N+0.5) Divider

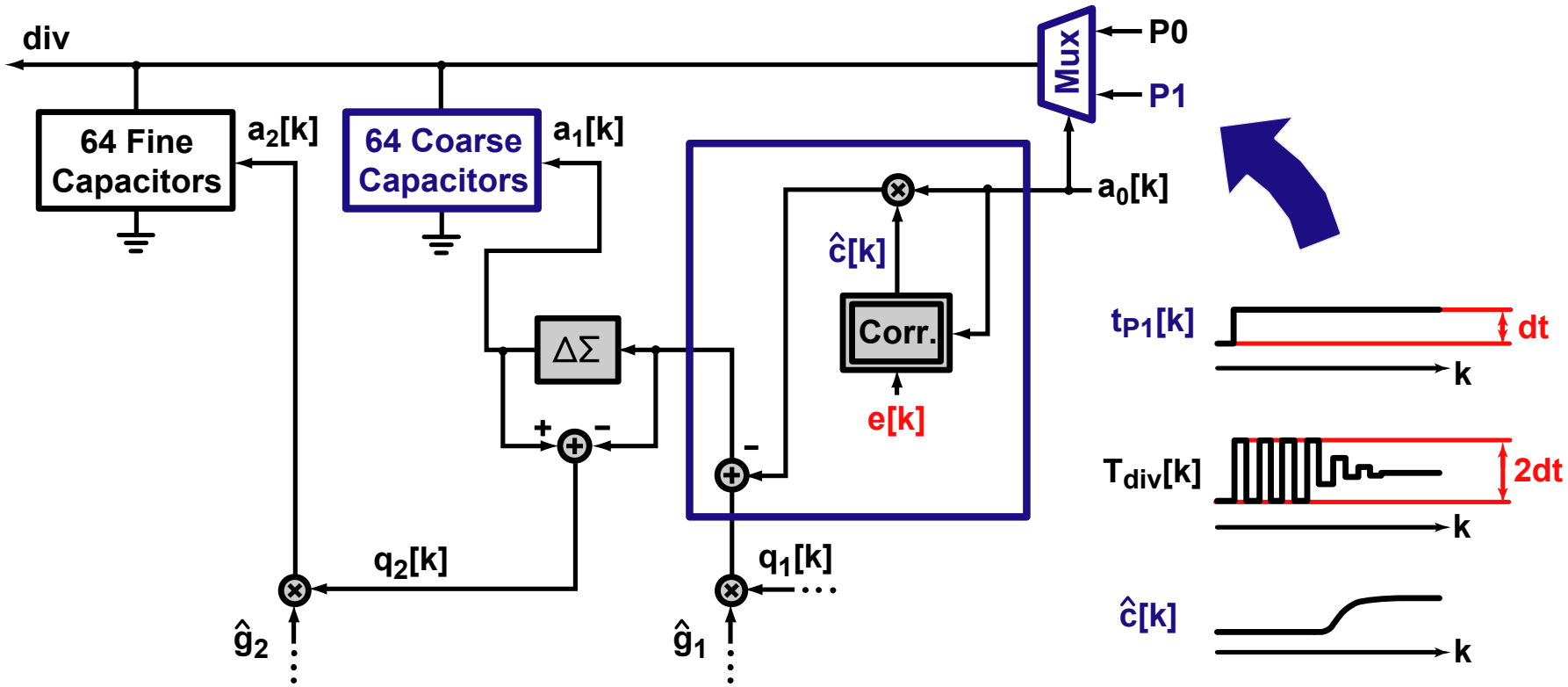


Phase Mismatch Impairments



- Unwanted frequency modulation
- E.g. 10% mismatch produces –20dBc spur

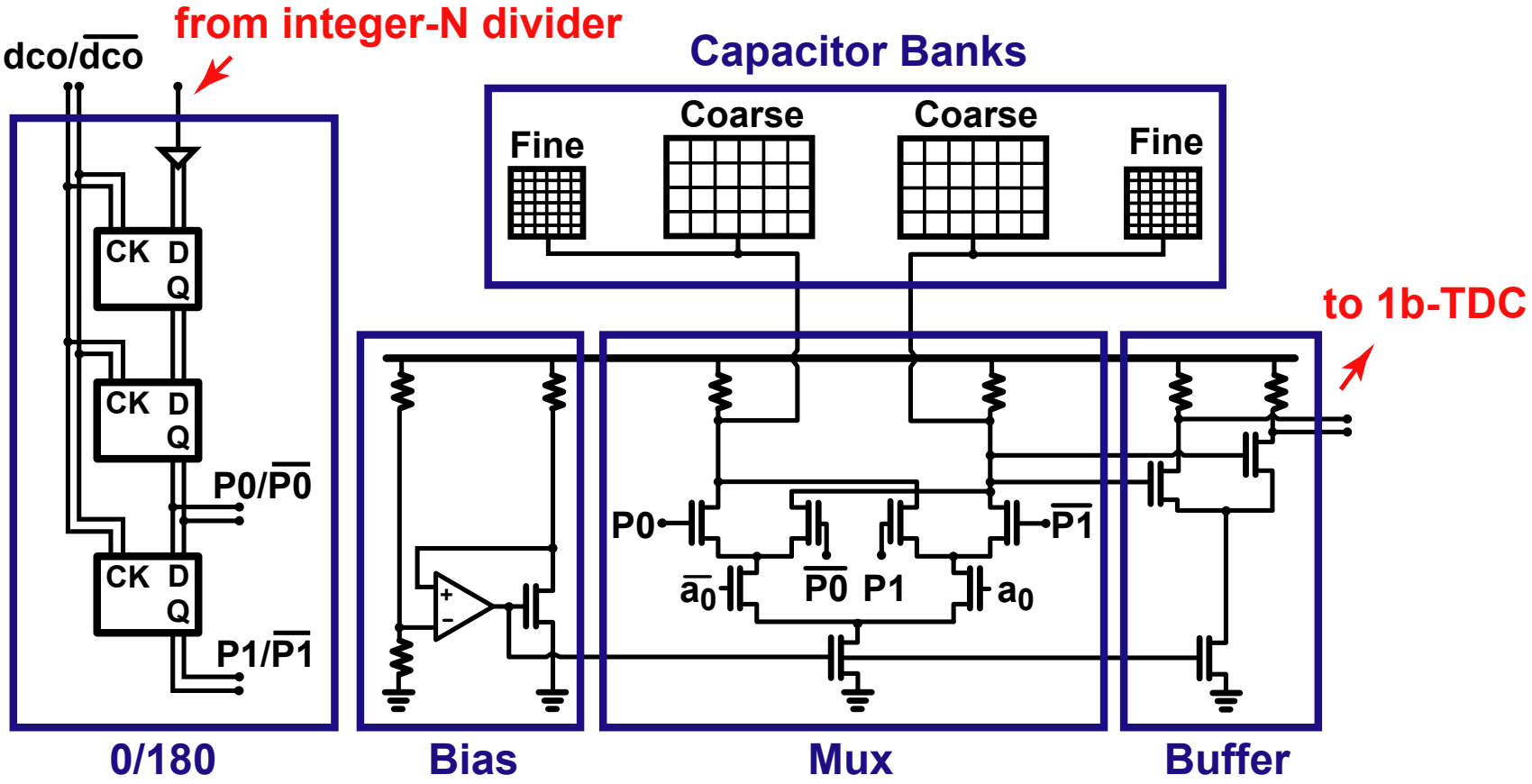
Background Mismatch Correction



- Same correction for capacitor mismatches

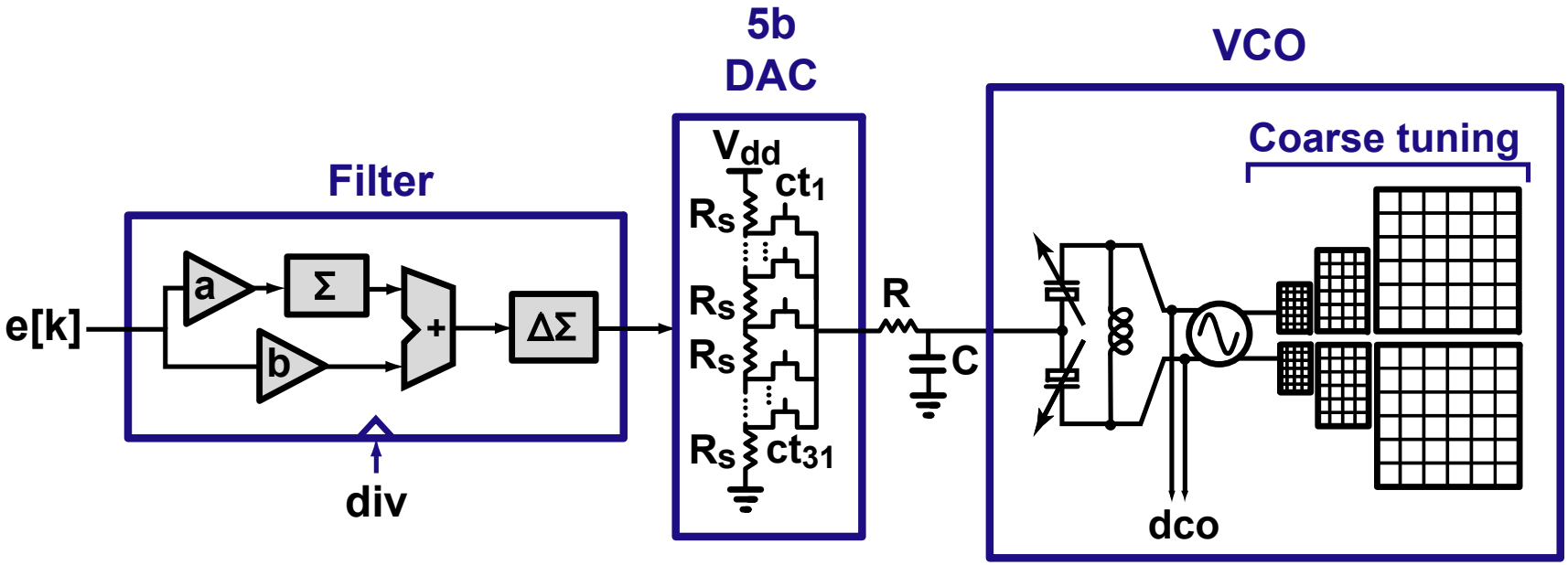
Circuit details

Circuit Design: Feedback Path



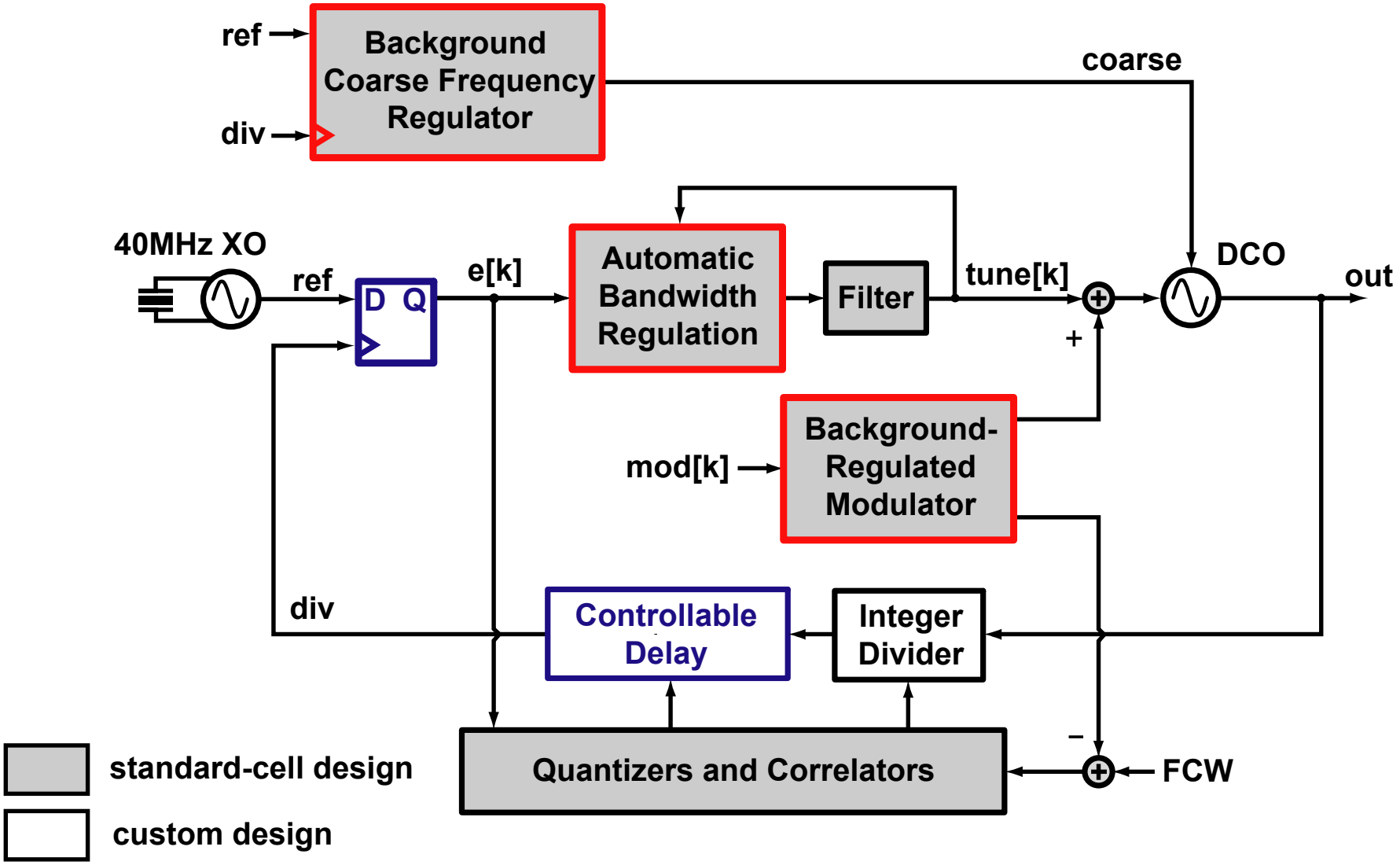
- Differential logic for better supply rejection
- Smaller area/higher power consumption

Circuit Design: Forward Path

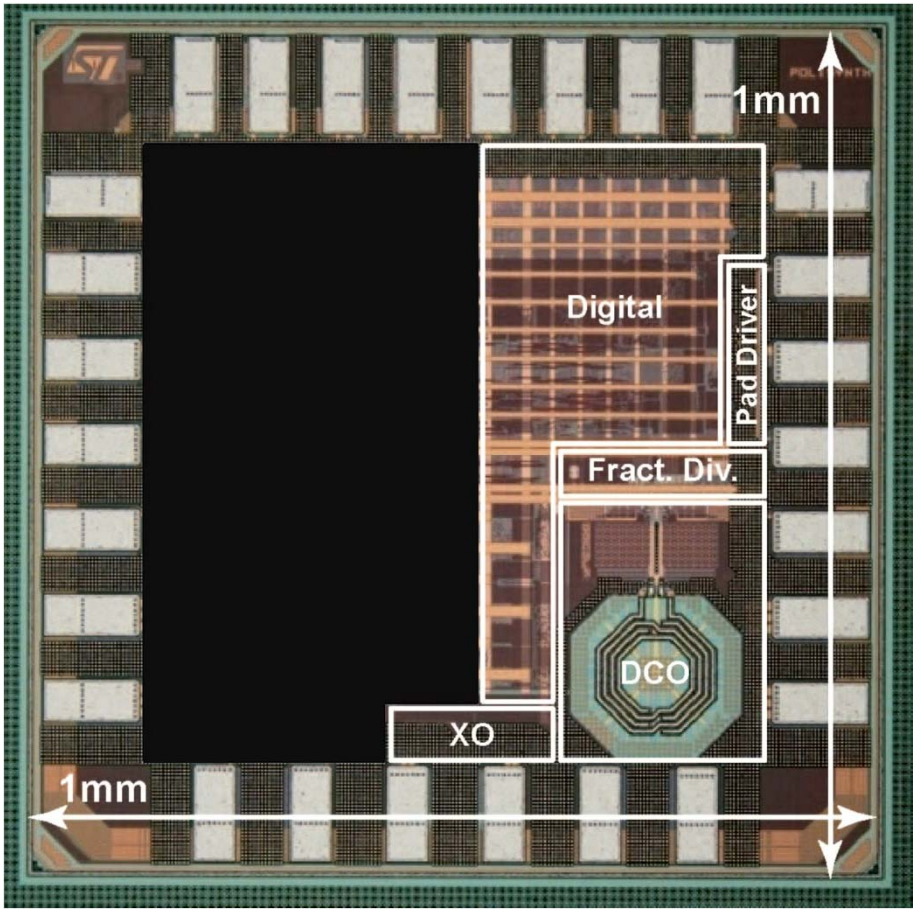


- Proportional/Integral filter with 1st-order ΔΣ
- 5b-DAC (with 1st-order RC filter) driving a VCO

Implemented Synthesizer

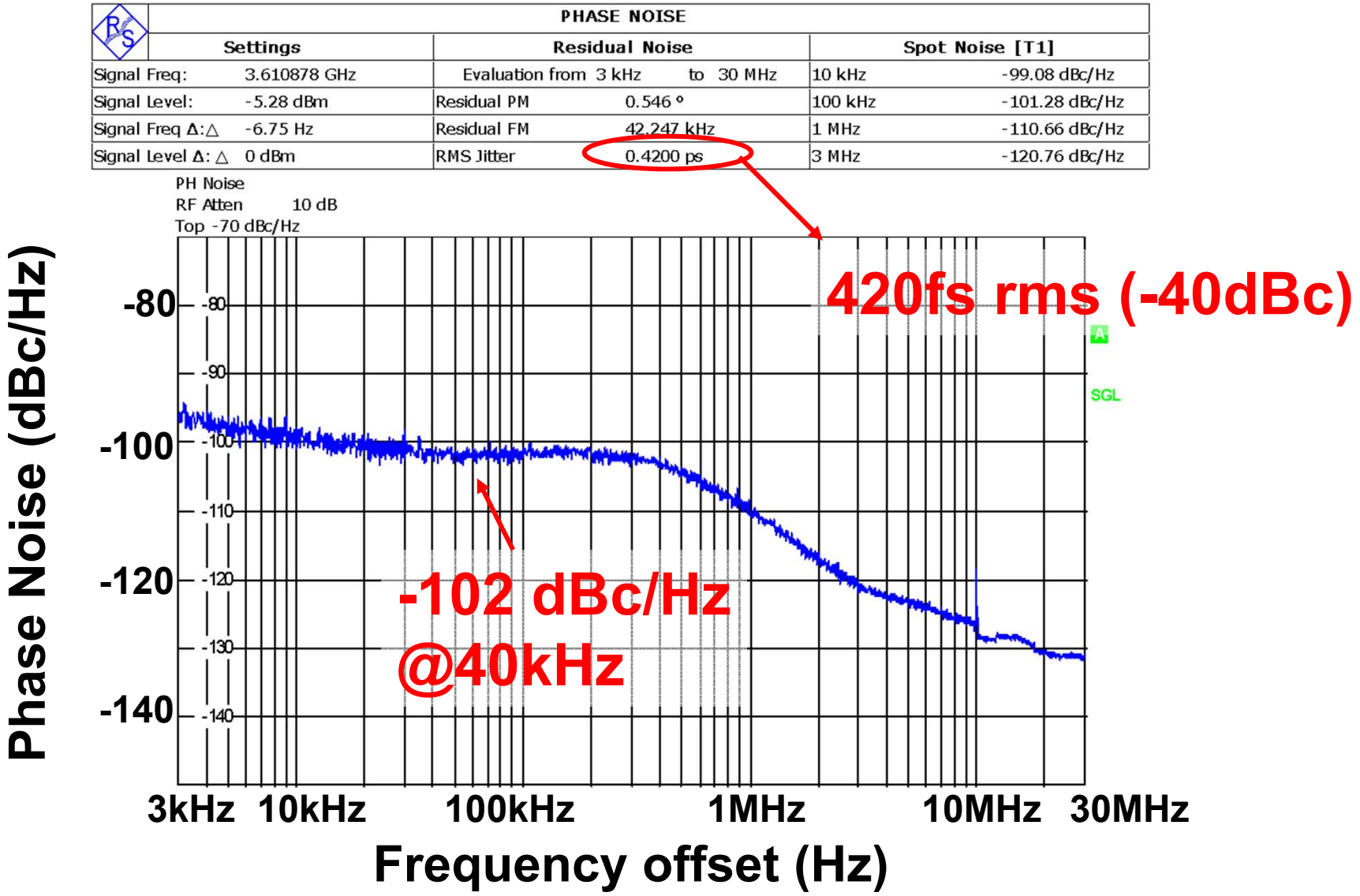


Die Photograph

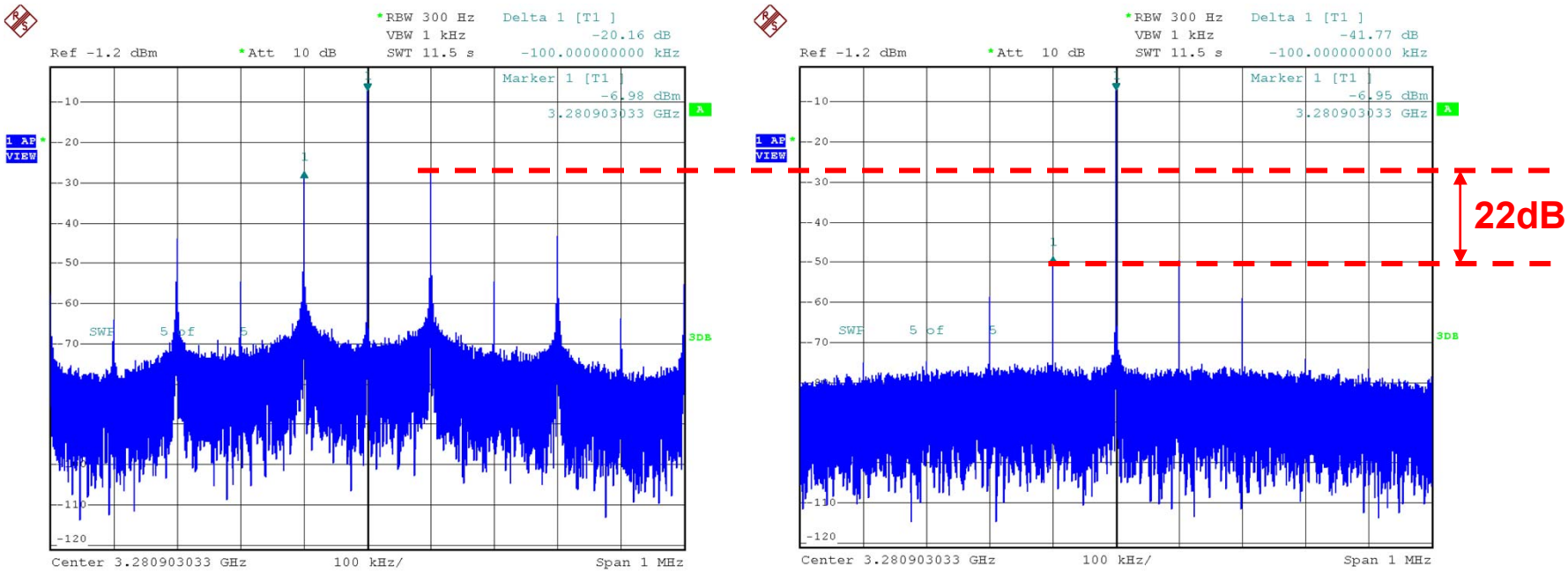


- 65nm CMOS
- Active area: 0.22mm^2
- Chip area: 1.0mm^2
- Power: 4.5mW
- Supply voltage: 1.2V

Measured Jitter with Out-of-Band Spurs

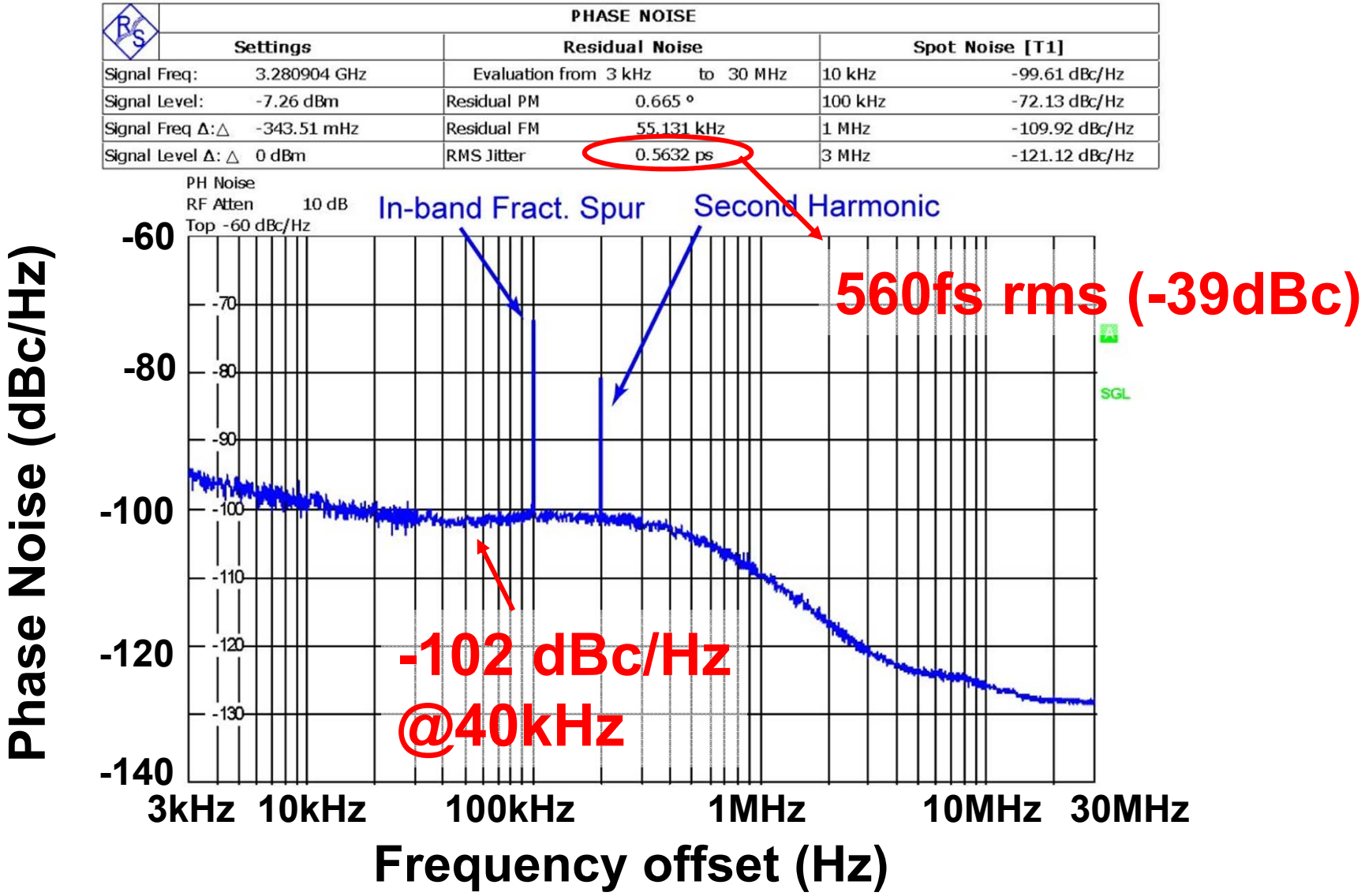


Mismatch Correction

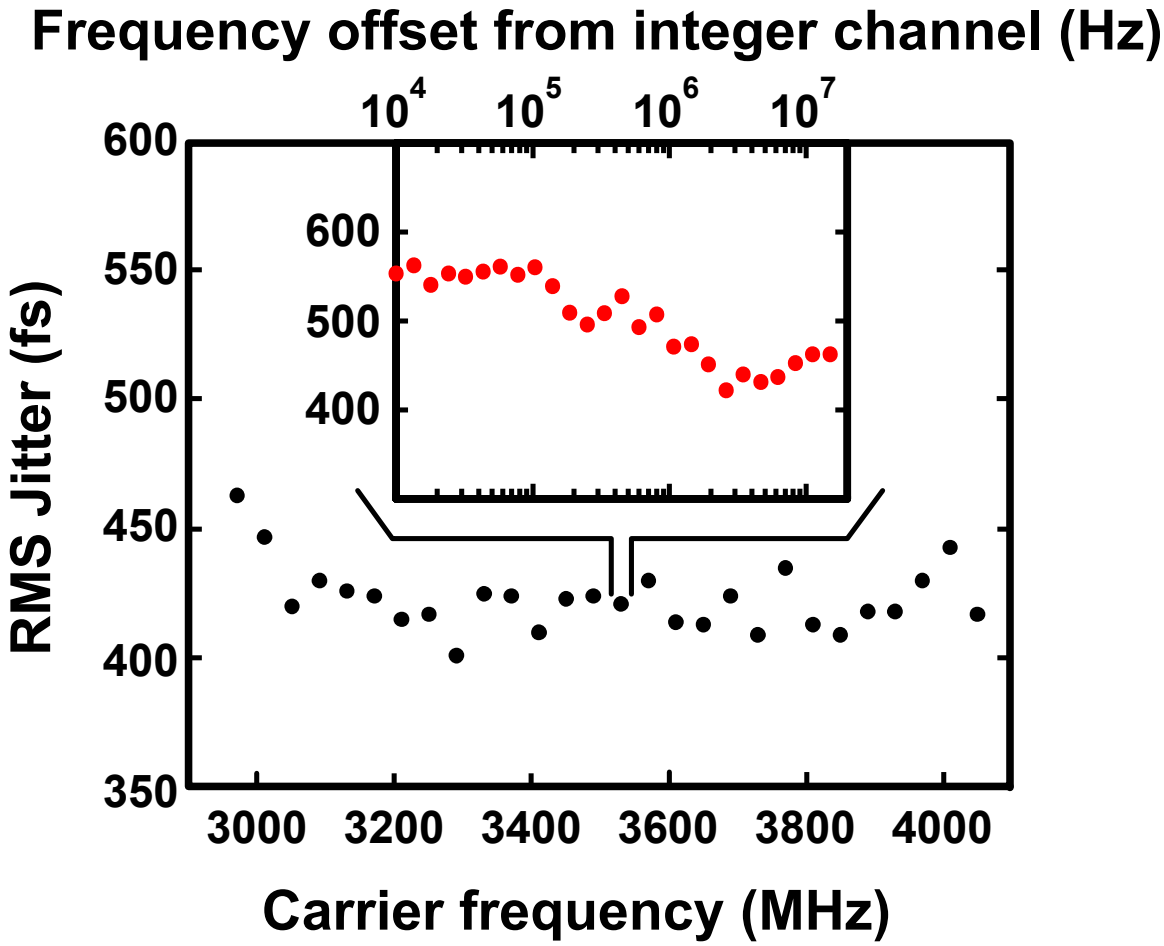


- Worst-case fractional spurs are in band
- Phase mismatch correction provides 22-dB spur reduction

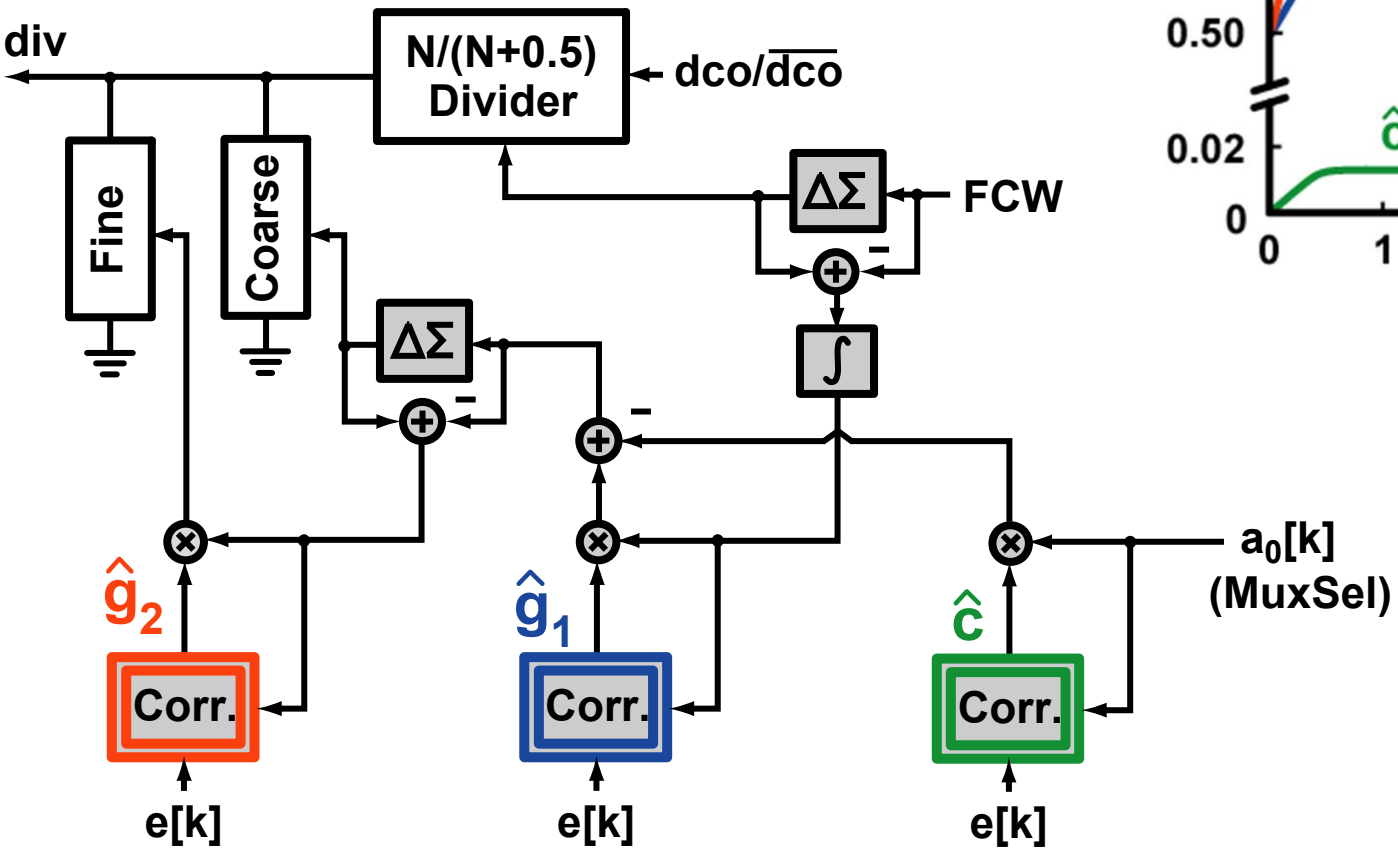
Measured Jitter with In-Band Spur at 100kHz

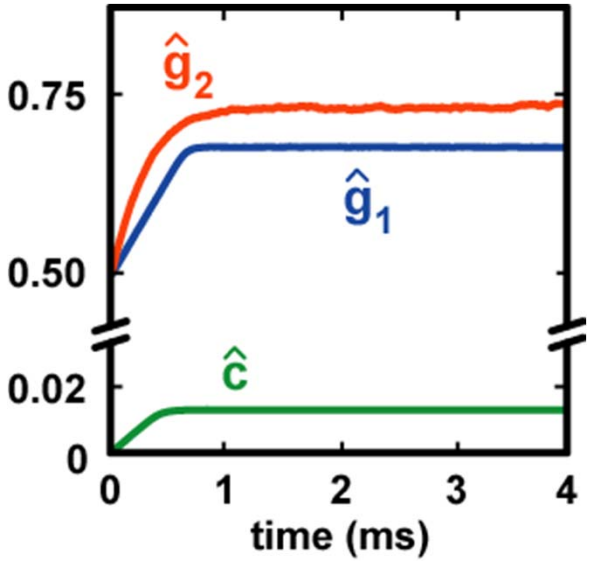


Measured Jitter vs. Channels



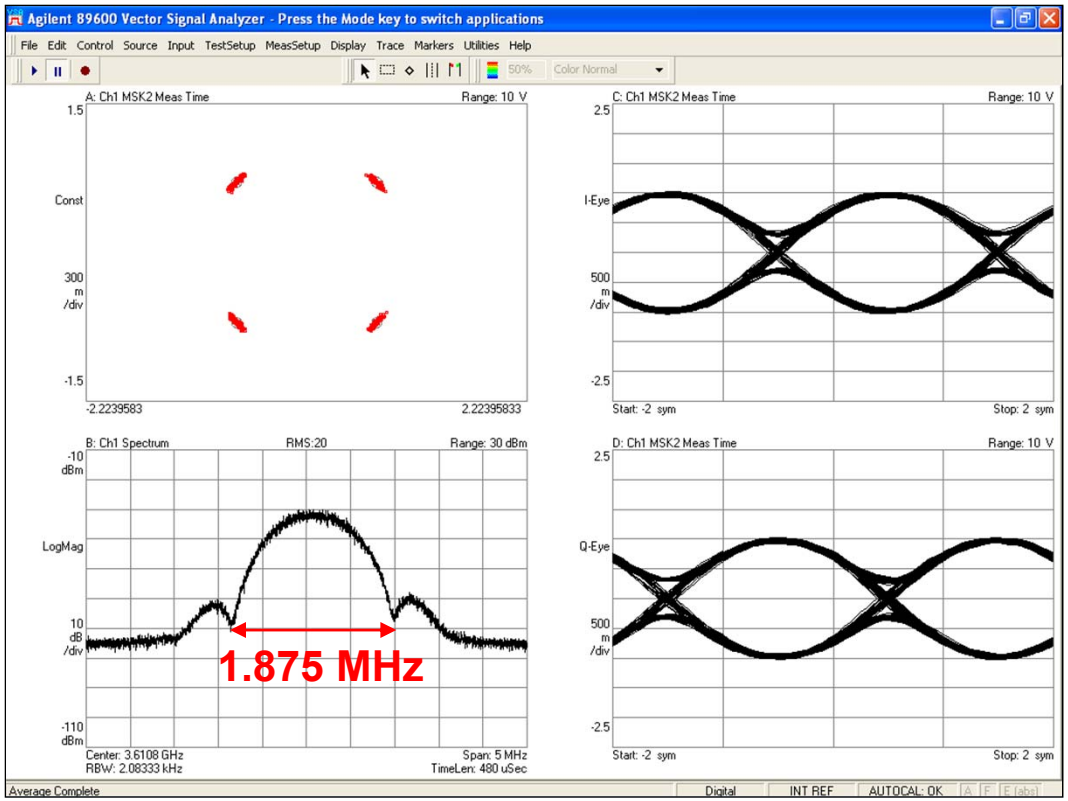
Measured Convergence of LMS Coefficients





GMSK modulation

- 1.25 Mb/s bit rate (BT = 0.5) with 300kHz PLL BW
- Demonstrates direct digital PM with bang-bang PLL



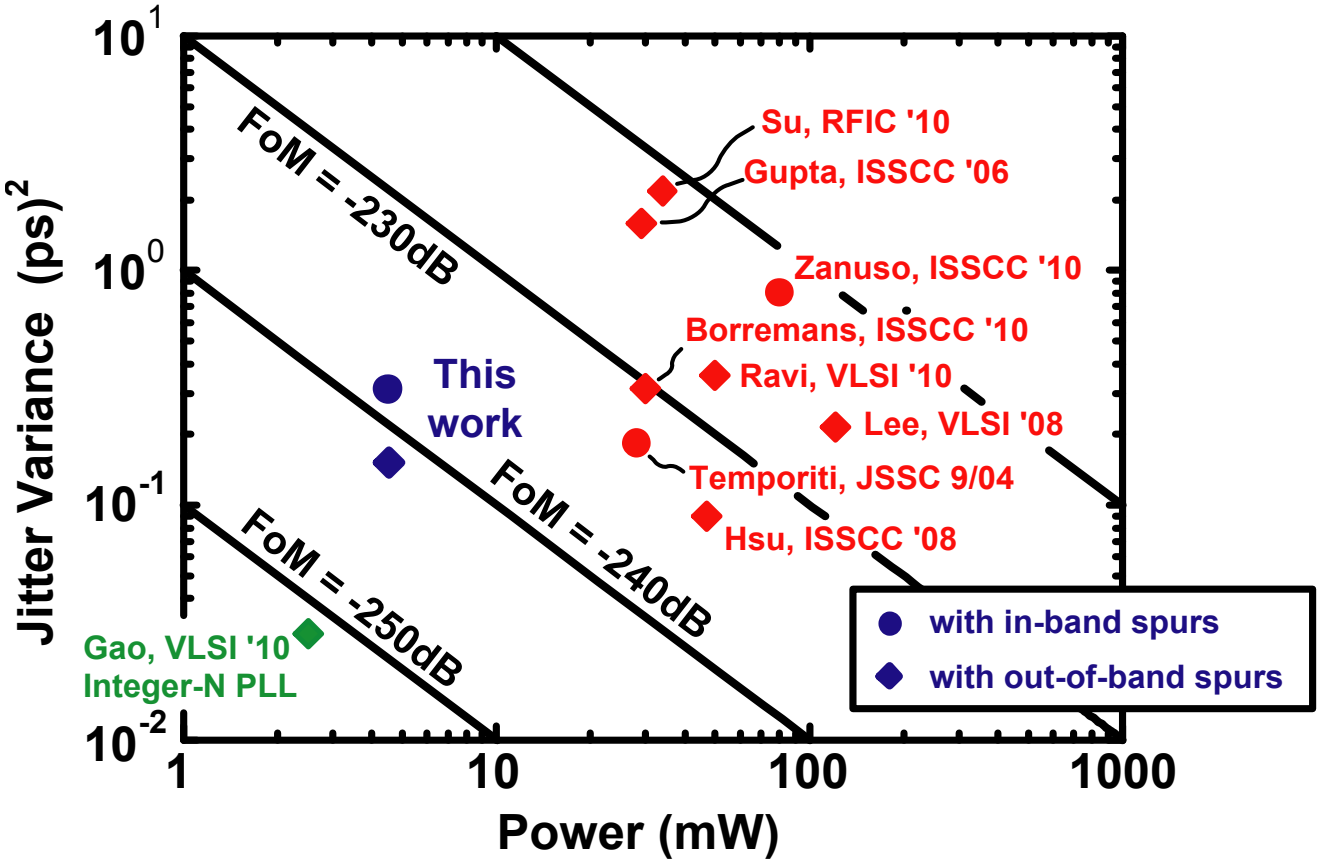
Performance Summary

	Borremans ISSCC '10	Ravi VLSI '10	Hsu ISSCC '08	Temporiti JSSC 9/04	This work
Architecture	Digital	Digital	Digital	Analog	Digital
Reference (MHz)	N/A	40	50	35	40
Output (GHz)	5-12	9.2-12	3.67	2.1	2.9-4.0
Tuning Range	82.3%	26.4%	N/A	N/A	31.9%
RMS Jitter (fs) min-max	560* - N/A	597* - N/A	300* - N/A	426* - 426	400* - 560
Bandwidth (kHz)	500	500	500	700	312
Out-of-band Fract. (dBc)	-48 (2MHz)	N/A	-53 (1MHz)	N/A	-53 (1MHz)
In-band Fract. (dBc)	N/A	N/A	-42	-60	-42
Ref. Spur (dBc)	-56	N/A	-65	N/A	-72
Power Diss. (mW)	30	50	47	28	4.5
Area occup. (mm^2)	0.28	1.2	0.9	N/A	0.22
Process (nm)	40	90	130	180	65

*Jitter measured when fractional spurs fall out of band

Figure-of-Merit

$$\text{FoM} = 10 \cdot \log\left[\left(\frac{\text{Jitter}}{1\text{s}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$$



Conclusions

- Low-power low-noise digital ΔΣ fractional-N frequency synthesizer is achieved with
  - elimination of power-hungry multi-bit TDC
  - introduction of a 10b segmented fractional-N divider
  - use of digital adaptation of delay range and digital correction of mismatches in background
- First demonstration of high-performance bang-bang fractional-N PLL with digital modulation capability

<-39dBc integrated noise at 4.5mW power