Pipelined A/D Converters

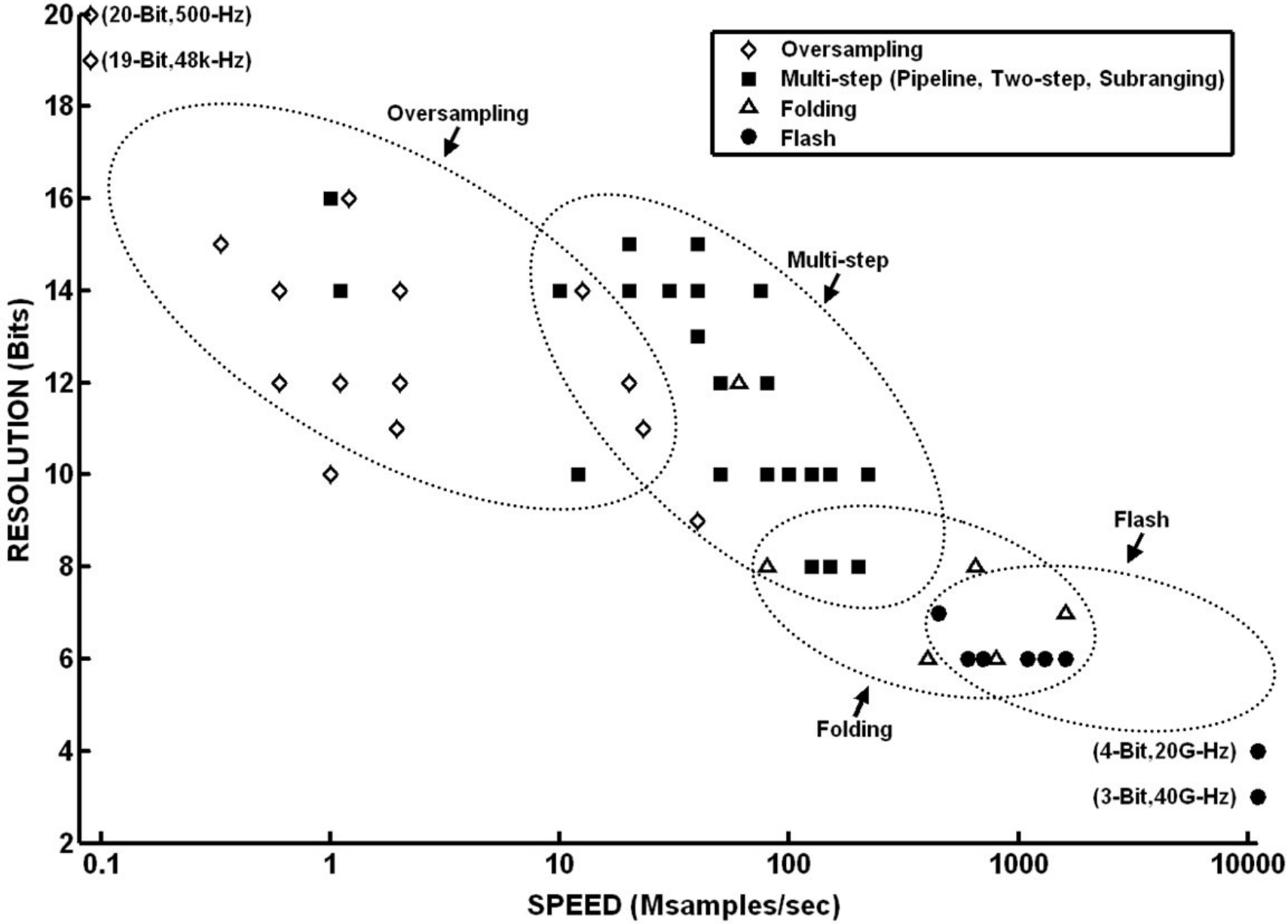
February 9th, 2006
San Francisco

Bang-Sup Song, Professor
Electrical and Computer Engineering
University of California, San Diego

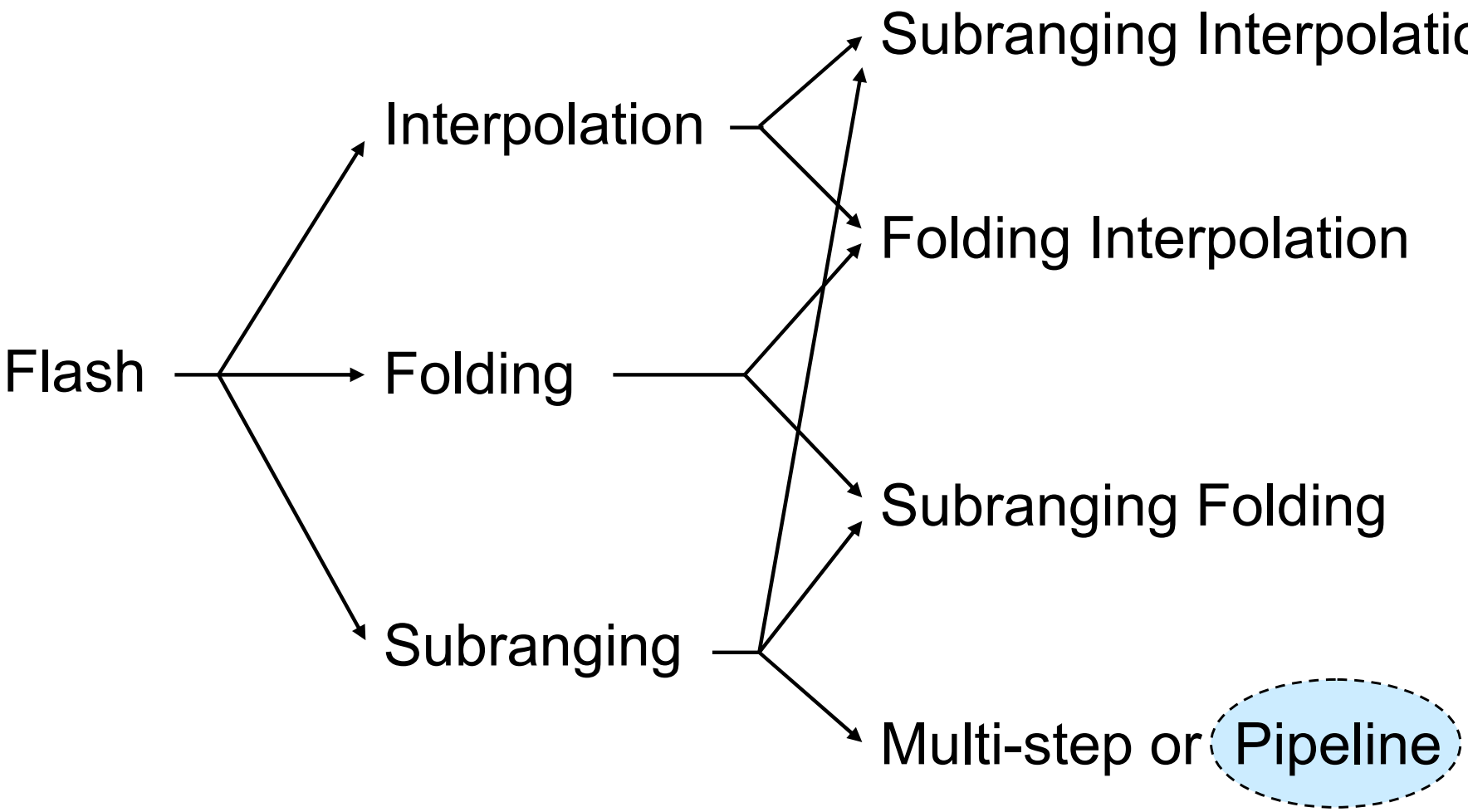
Outline

- Introduction to pipelined architectures
- MDAC-based pipelined ADC
- High-resolution techniques
- Other variations of pipelined ADC
- Circuit design issues
  - Sampling nonlinearity
  - Dynamic comparator
  - Opamp design
- Conclusions

ADC Resolution vs. Speed



Nyquist-Rate ADC Family

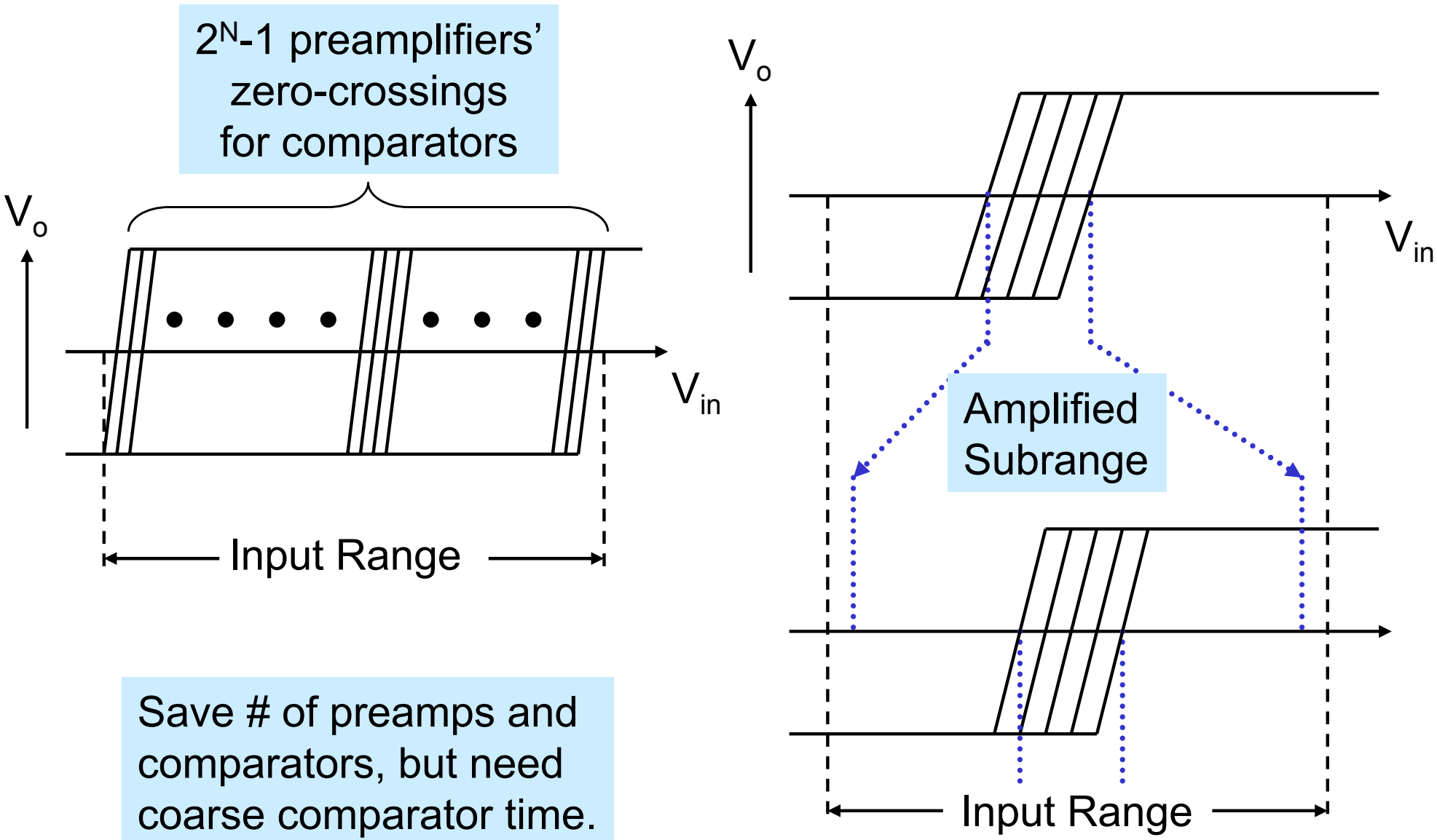


- Averaging, pipelining, and time-interleaving are common techniques for all.

Design Solutions

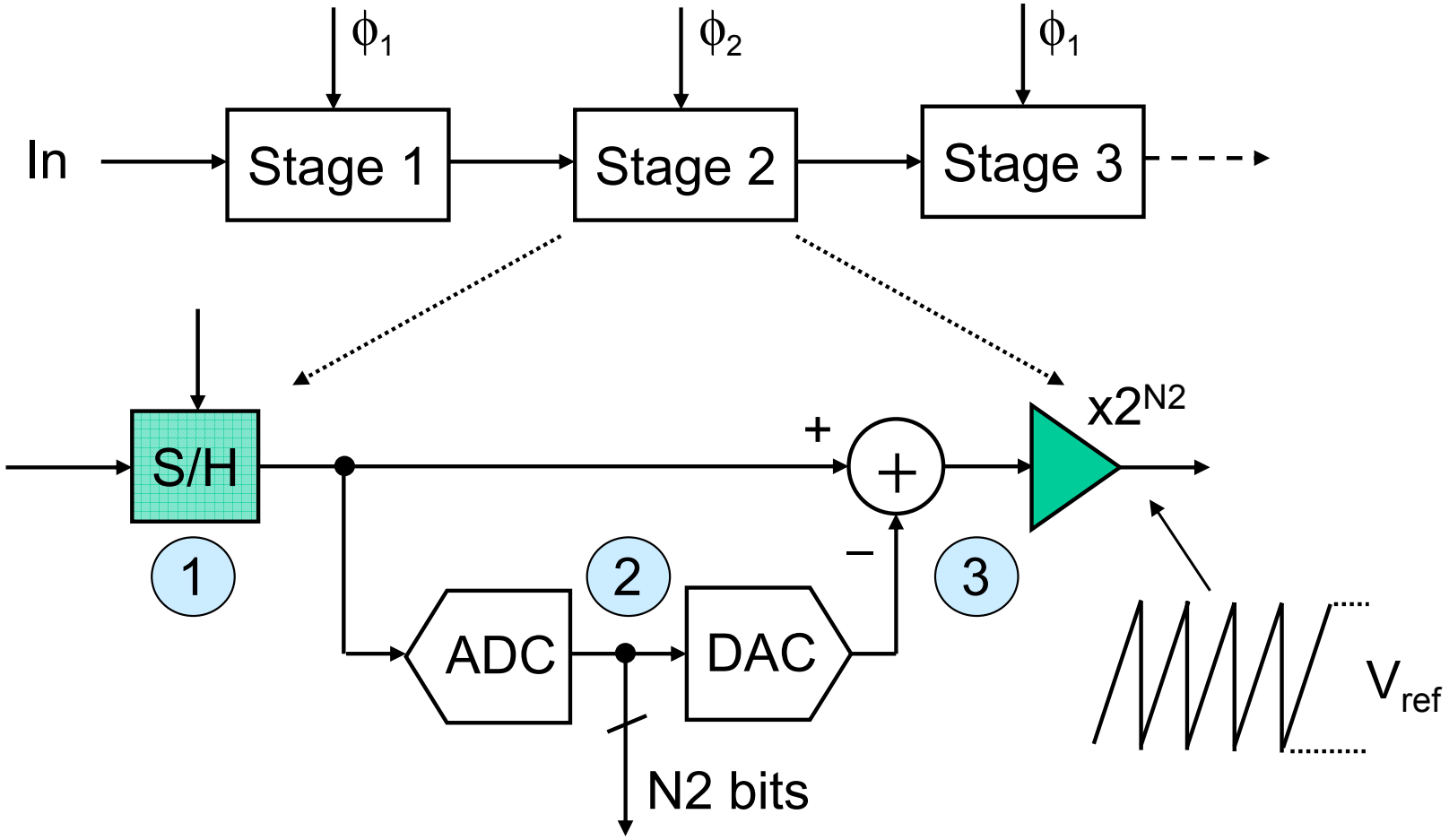
What to do	How to do
To save # of preamps	Interpolation
To save # of comparators	Folding
To save # of both	Subranging
To reduce preamp offsets	Averaging
To speed up conversion	Interleaving
To speed up subranging	Pipelining
To improve linearity	Calibration

Flash vs. Subranging



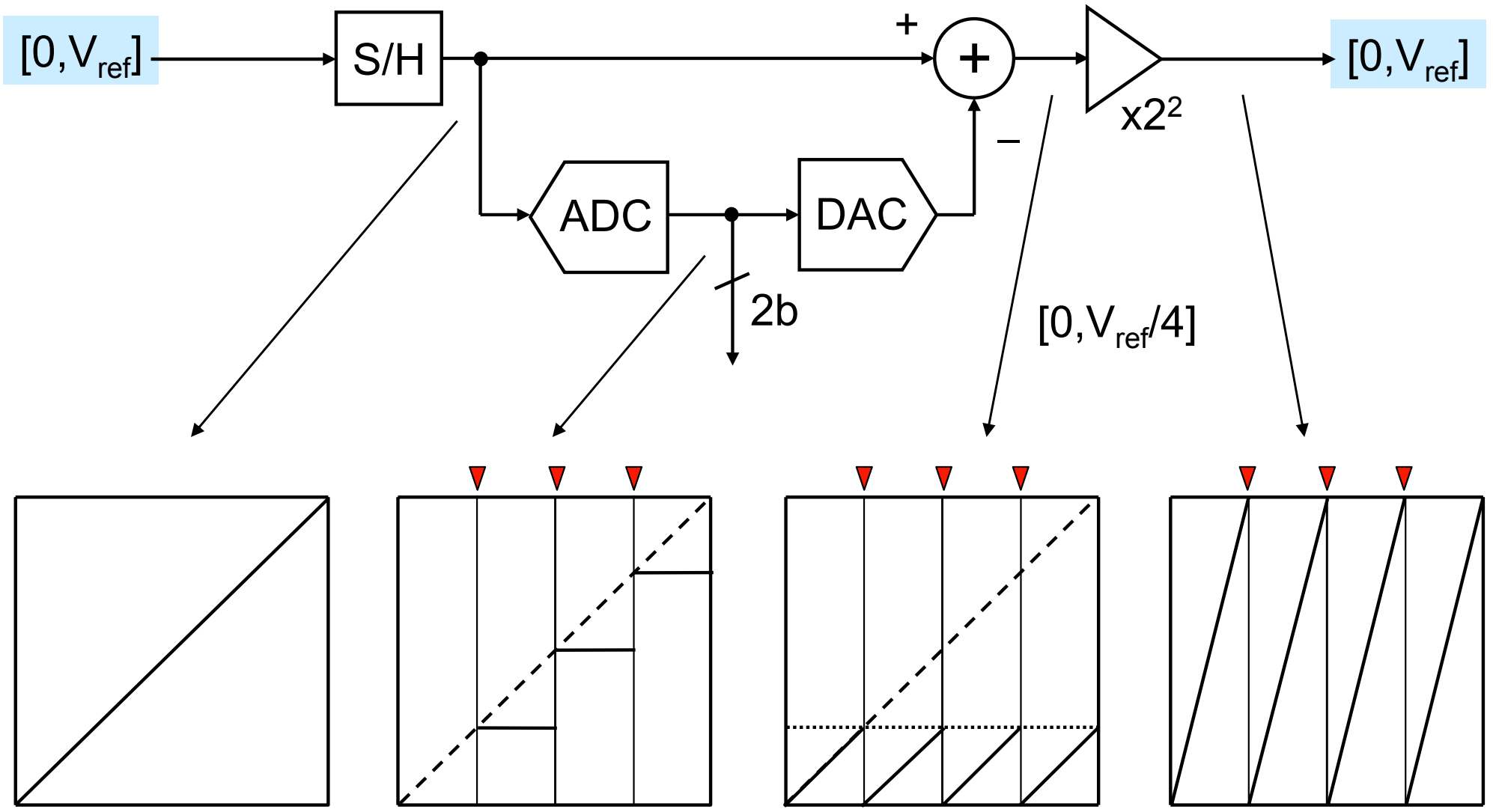
Save # of preamps and comparators, but need coarse comparator time.

Pipelined ADC Architecture

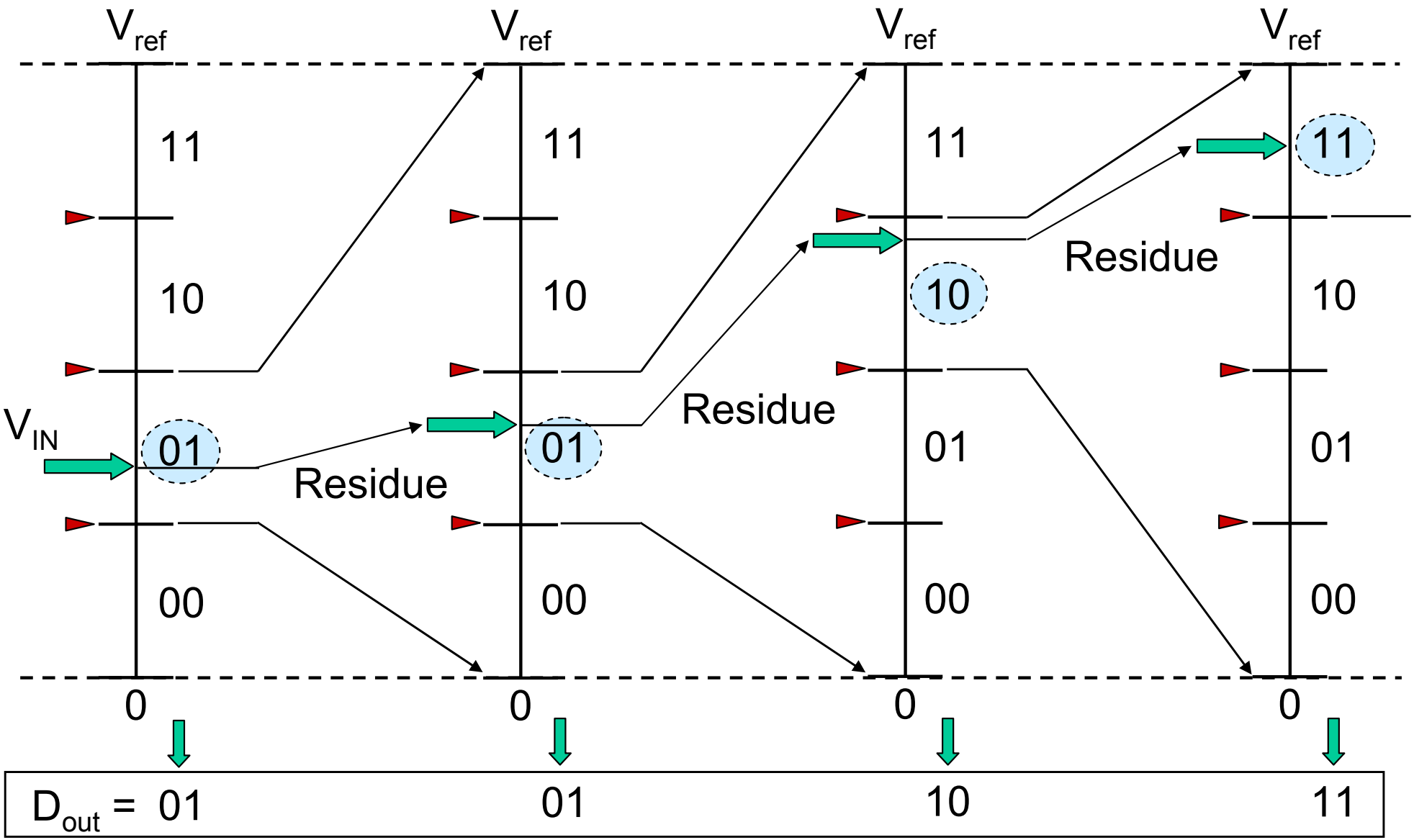


- S/H in every stage using non-overlapping 2-phase clocks.
- ADC should work between the sampling and amplification phases.
- More time for residue amplification than in subranging.

2b Pipelined Stage Example

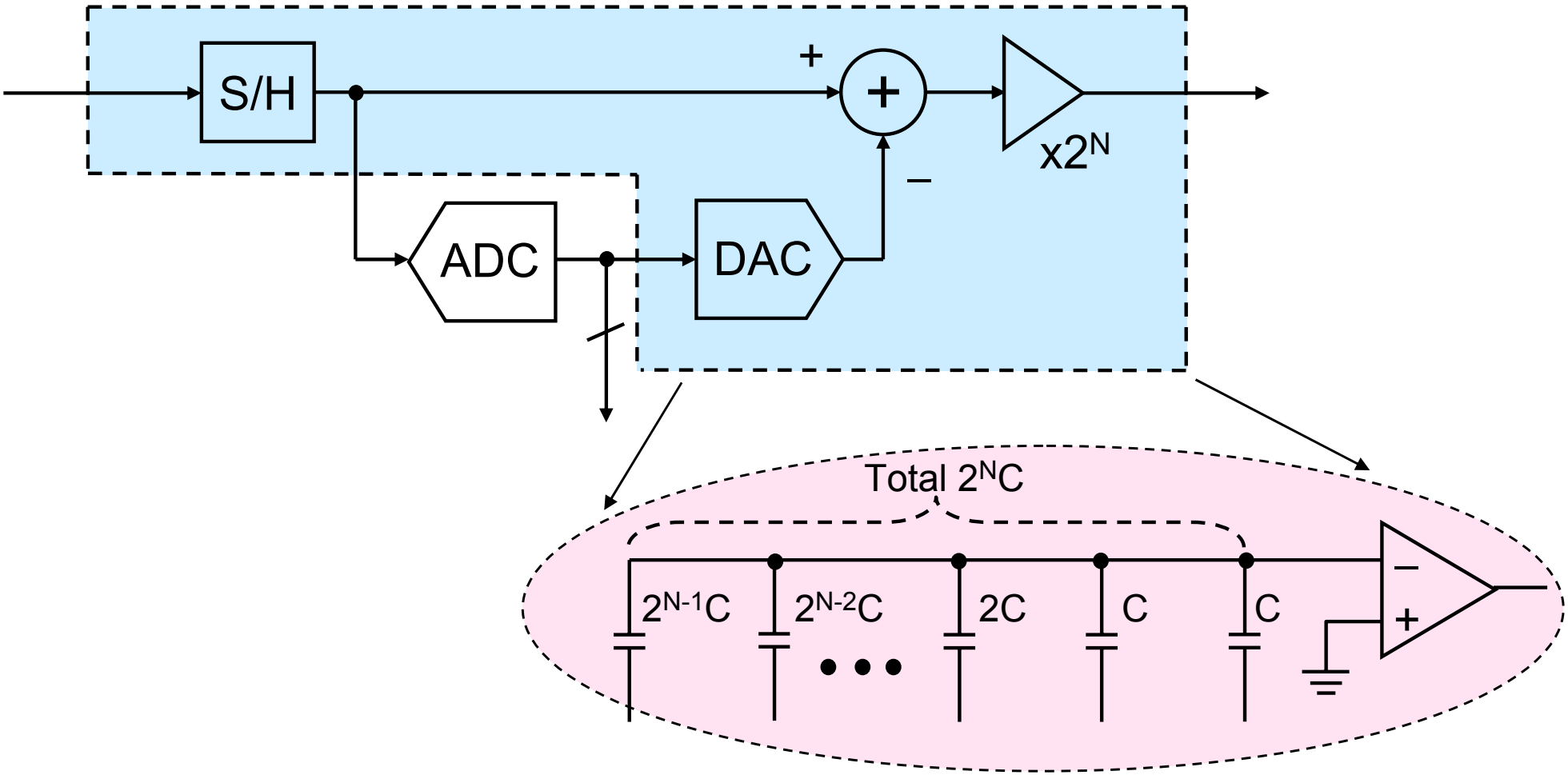


2b Pipelined Residues



Capacitor-Array MDAC

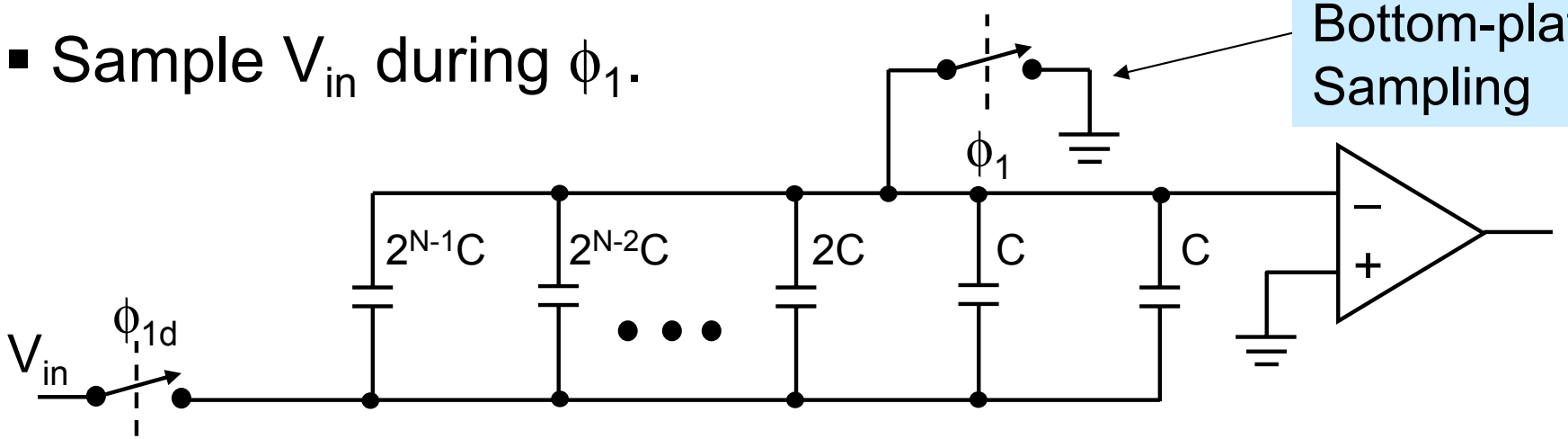
(Song, JSSC, Dec. 1990)



- Capacitor-array MDAC replaces S/H, DAC, and residue amp.
- Capacitor array can be either binary or thermometer coded.

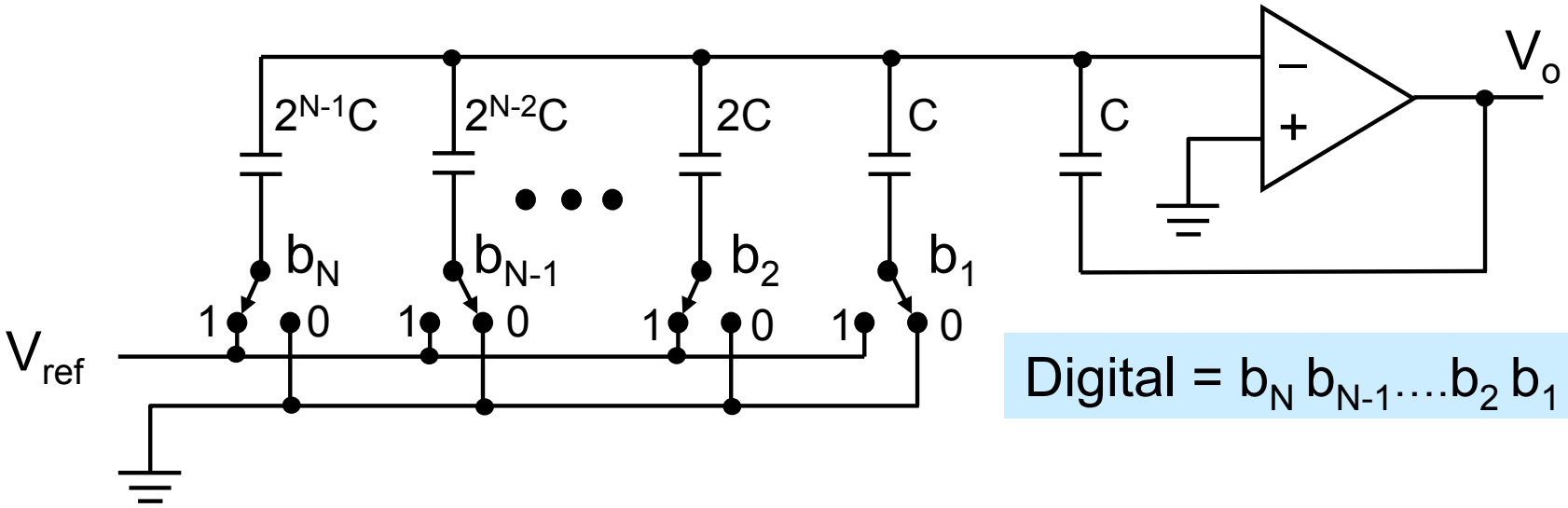
MDAC Operation

- Sample V_{in} during ϕ_1.



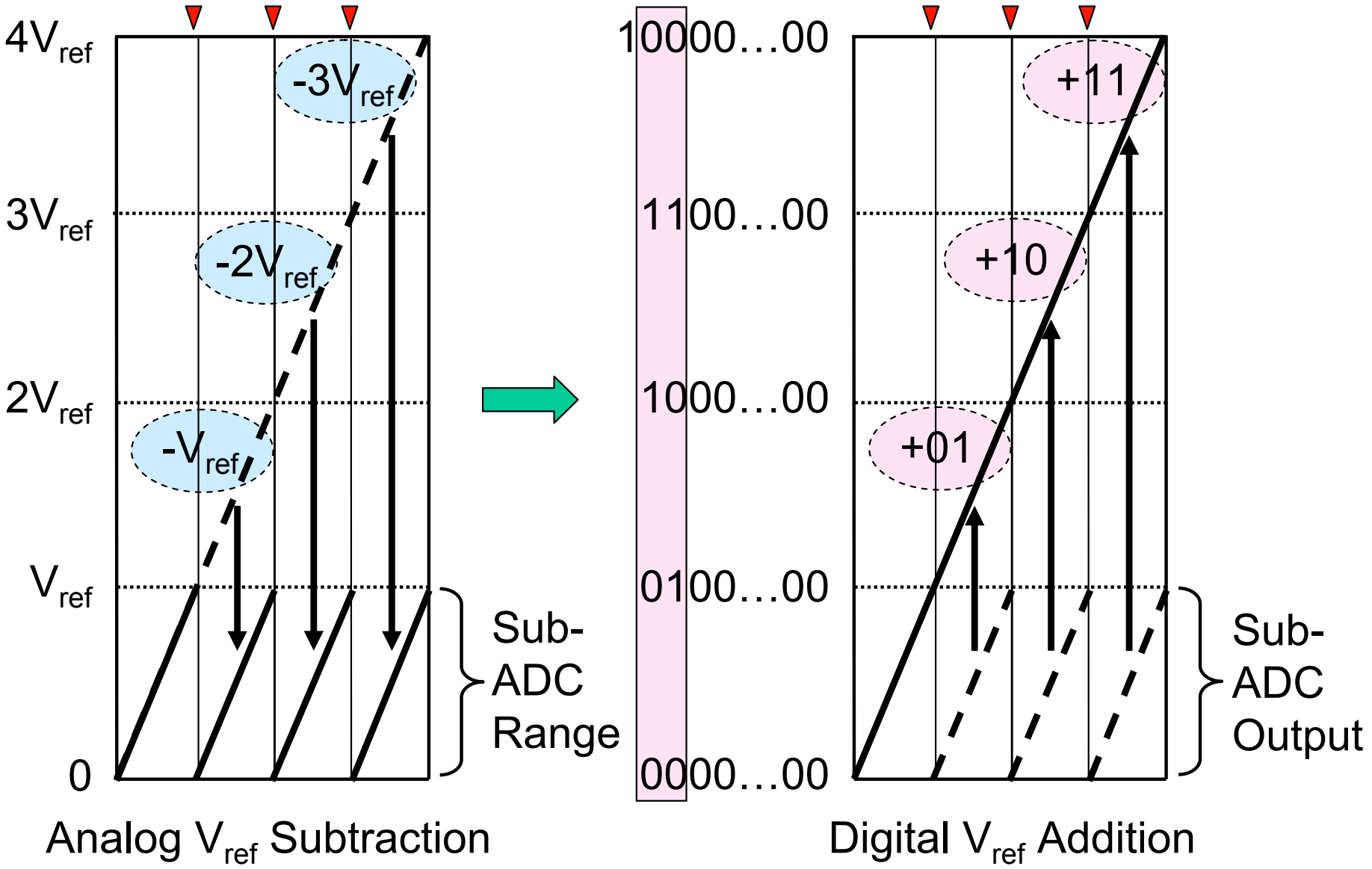
- Amplify residue during ϕ_2.

$$V_o = 2^N \left(V_{in} - \sum_{i=1}^{N} b_i \frac{2^{i-1}}{2^N} V_{ref} \right)$$

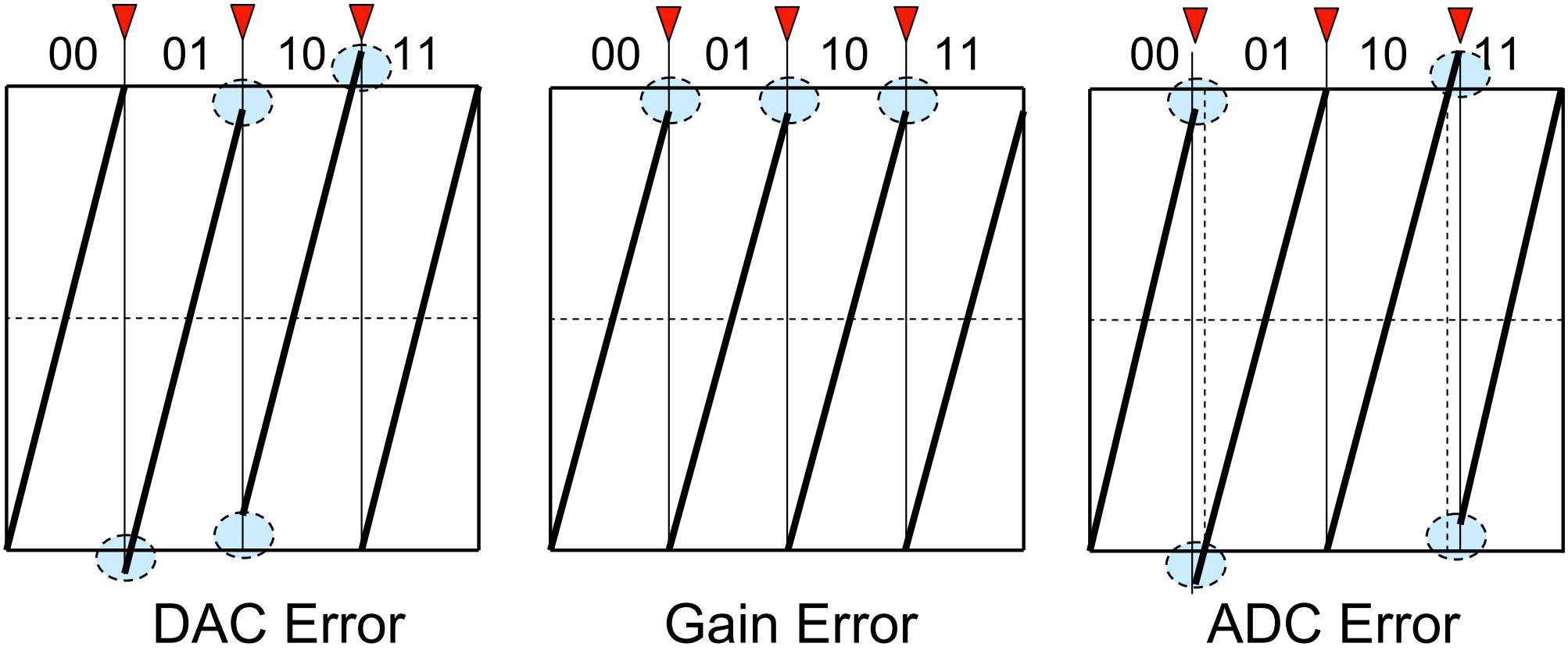


Digital = $b_N\, b_{N-1} \ldots b_2\, b_1$

Restore Subtracted V_{ref} Digitally



Three Residue Errors

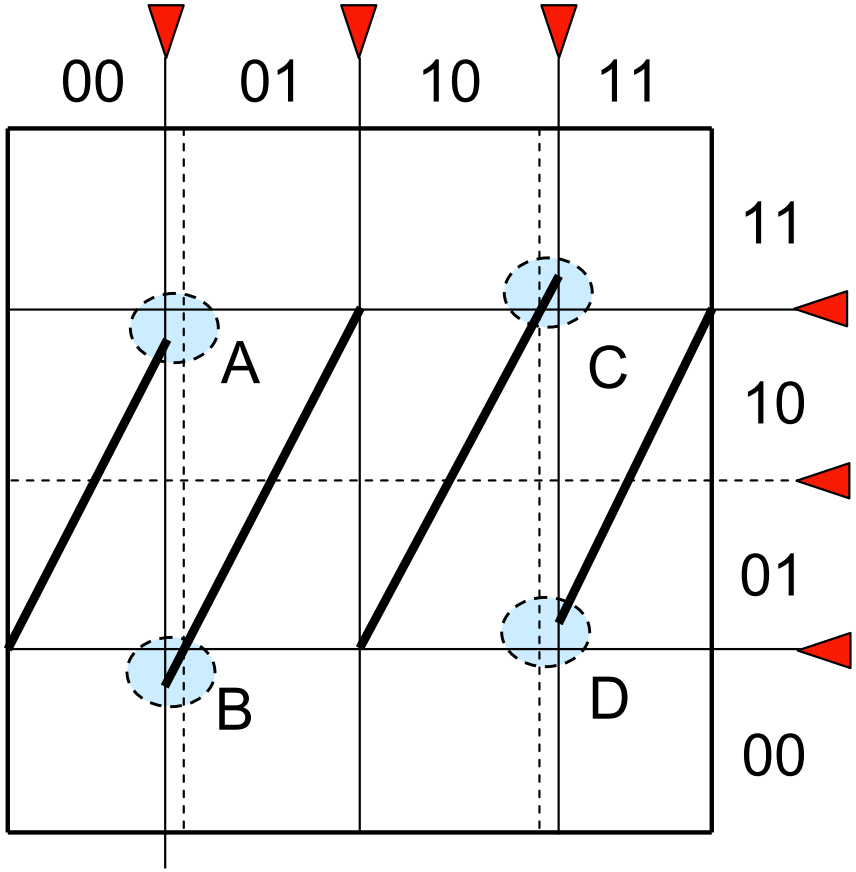


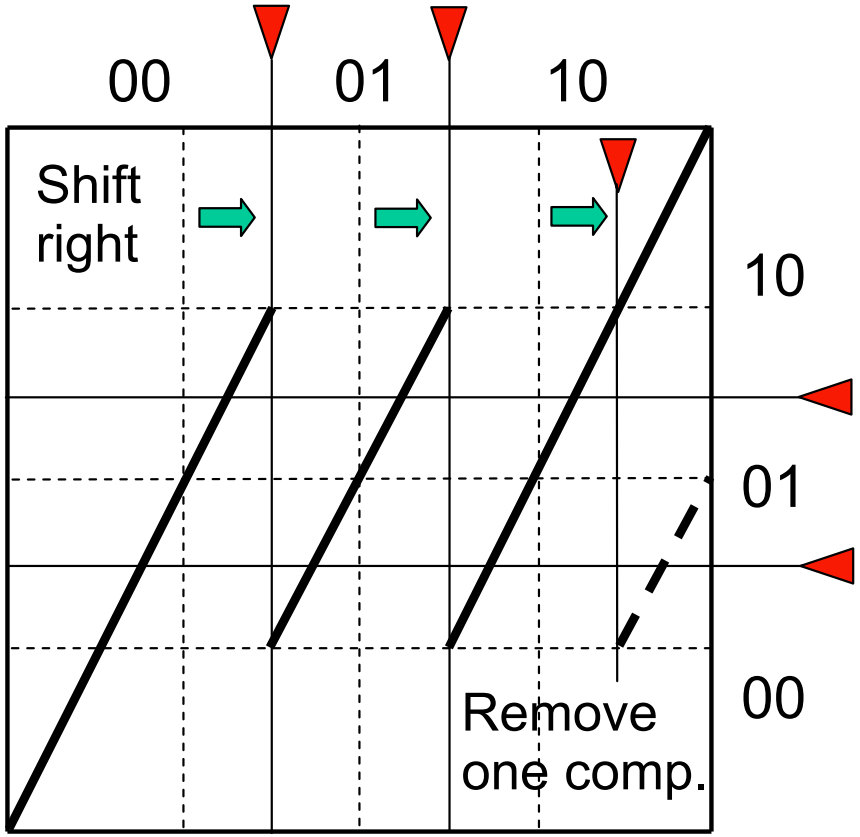
DAC Error Gain Error ADC Error

- Subtracted analog V_{ref}'s are not accurate.
- Errors should be smaller than the following-stage resolution.
- If over-ranged, ADC error can be recovered.

Digital Correction

(Lewis, JSSC, Mar. 1992)

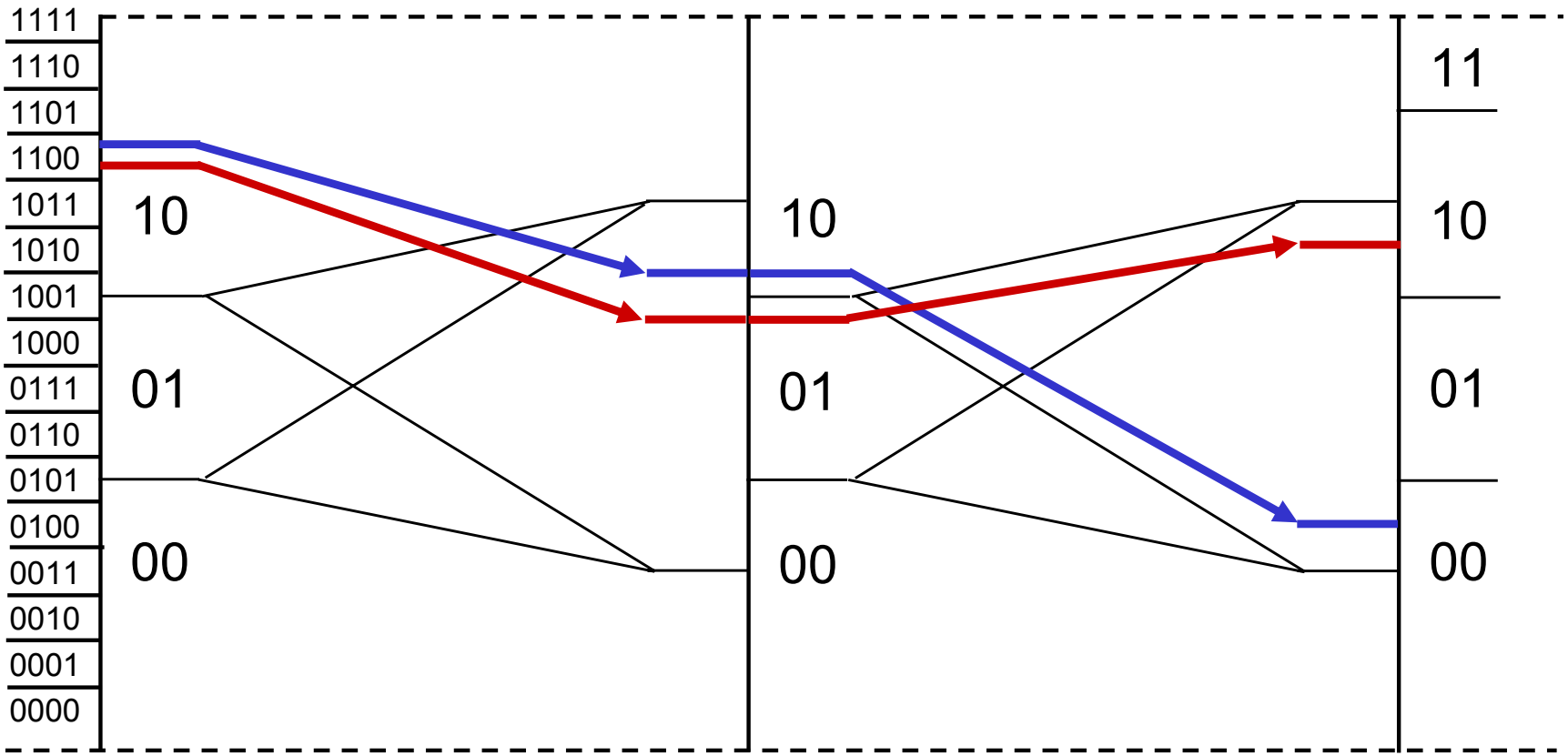


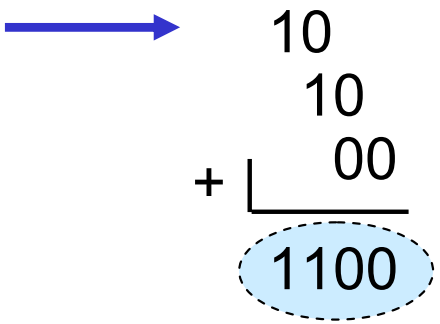


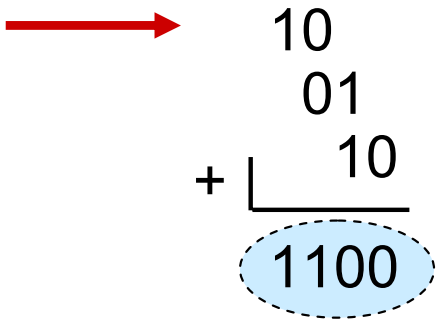
@A	@B	@C	@D
00	01	10	11
10	00	11	01
010	010	111	111

Digital output increases monotonically across any digital transitions.

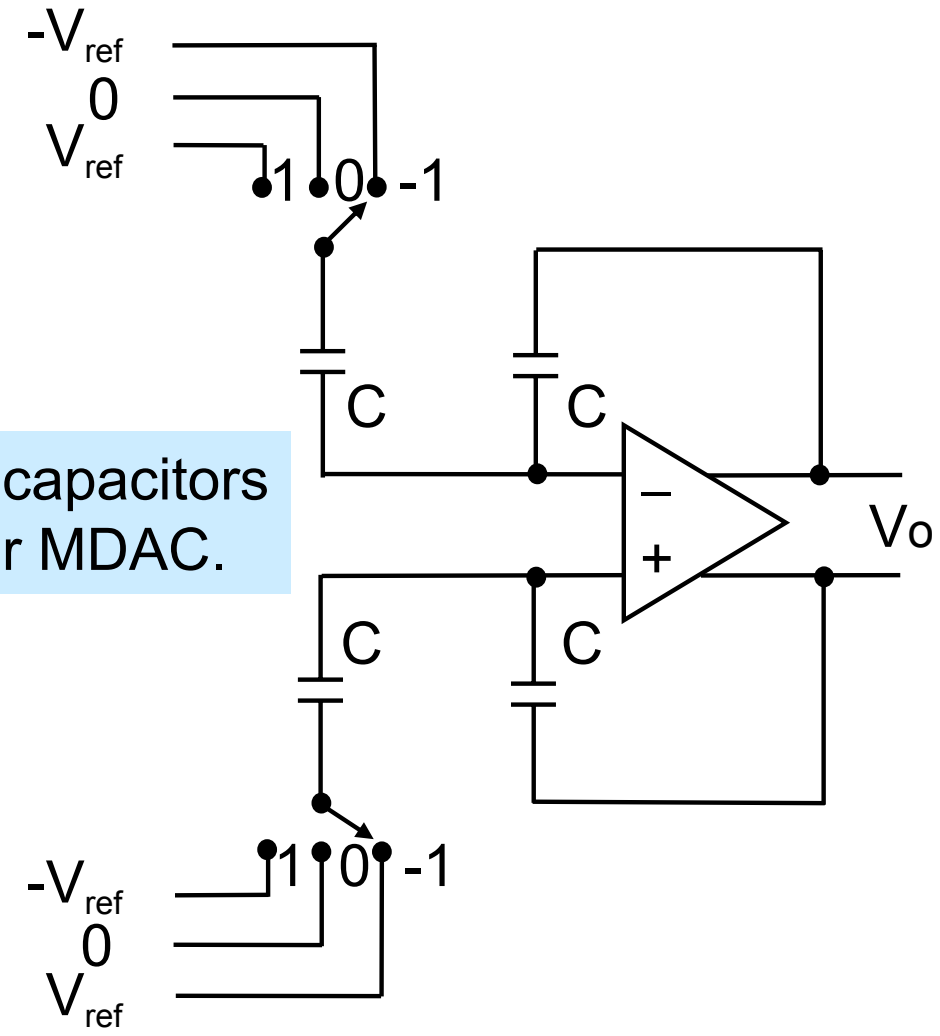
Digital Correction for 4b ADC



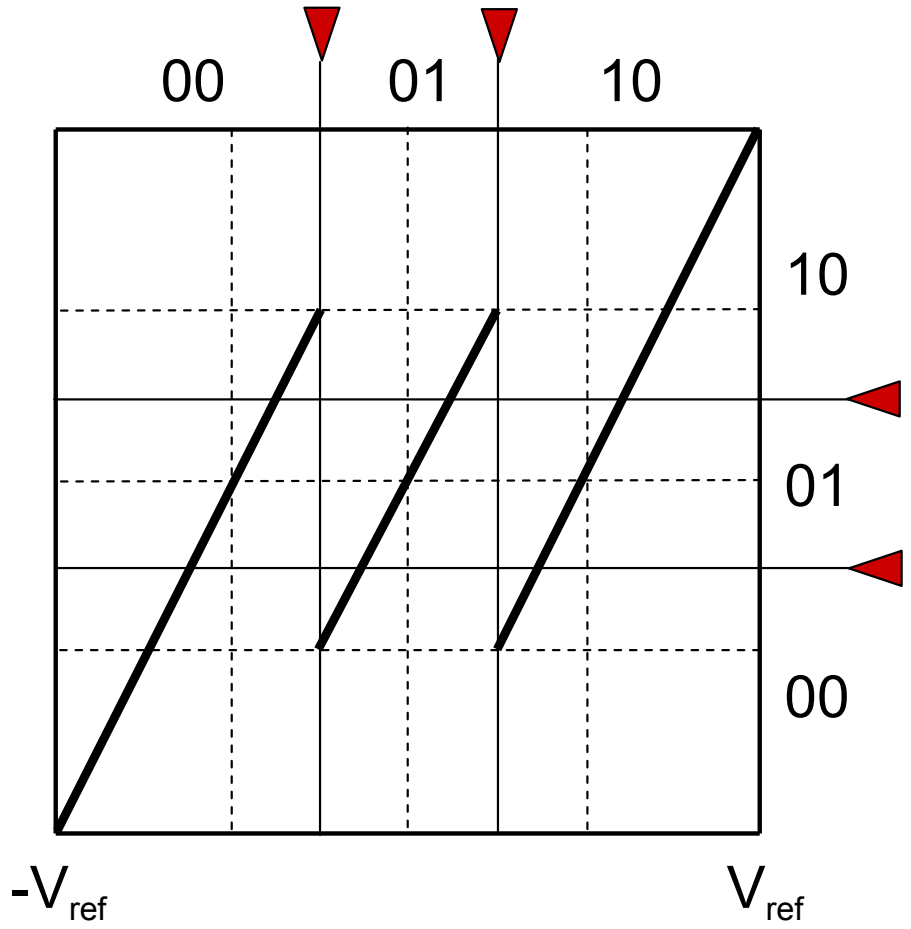




MDAC for Degenerate 1.5b Case

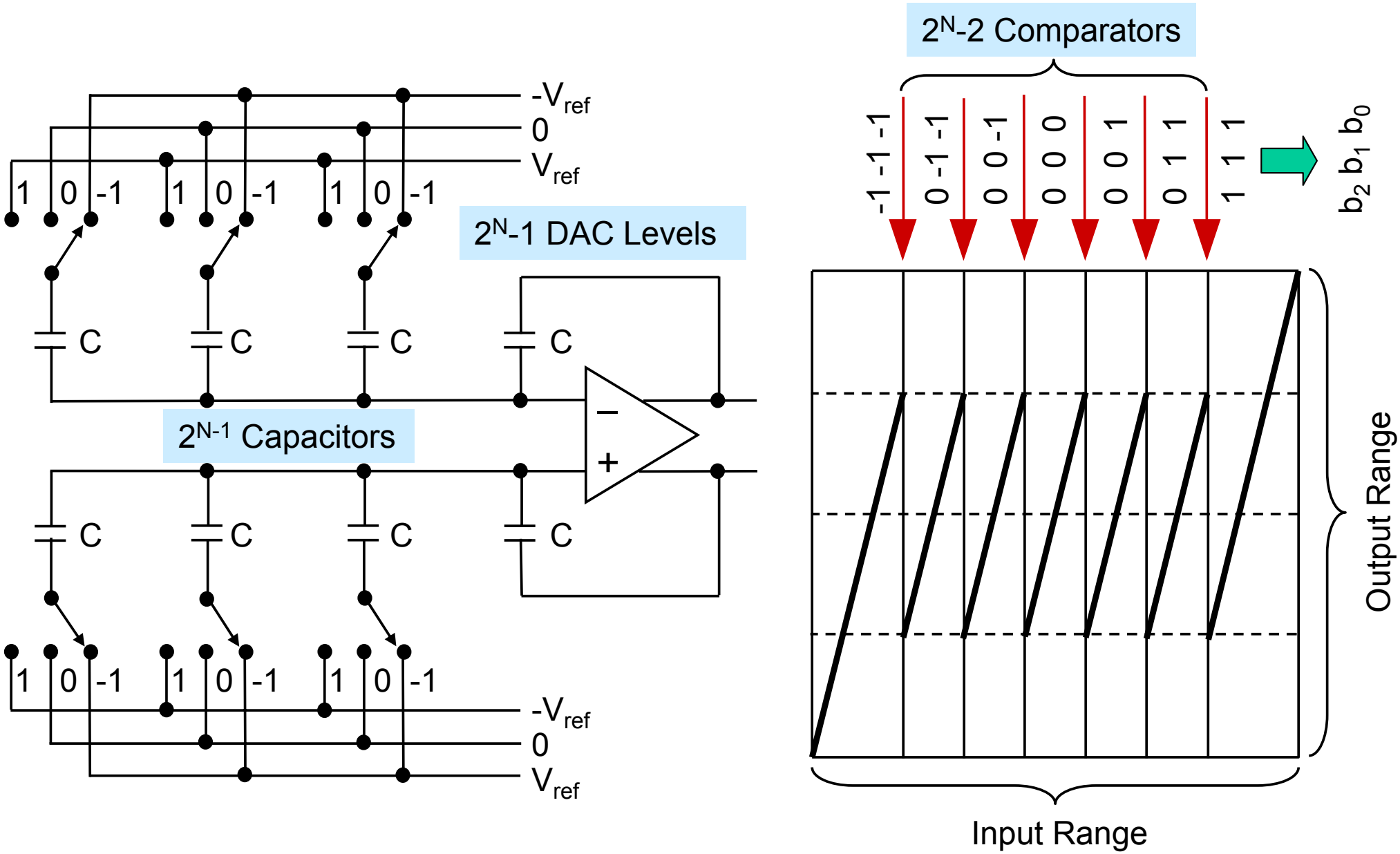


2 capacitors for MDAC.

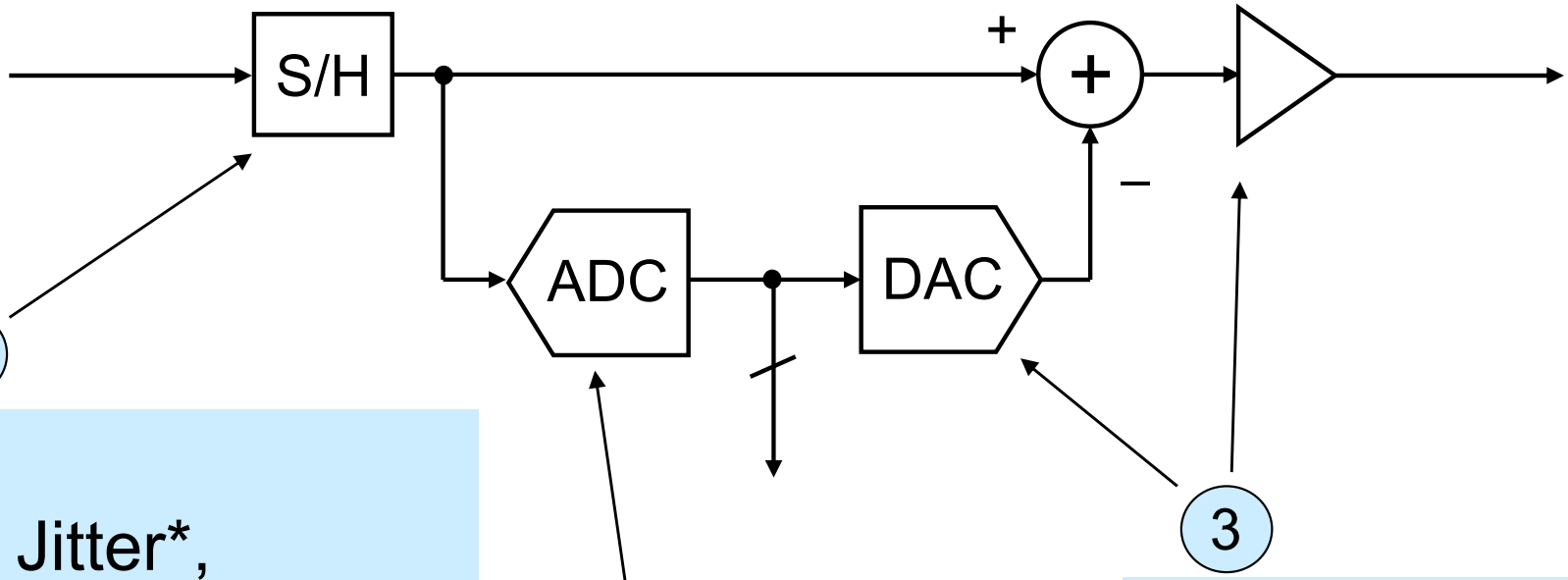


Multiply-by-2 ($2V_{in}$ –/+V_{ref}) circuit using 2 capacitors.

General Tri-Level MDAC Example



Issues in Pipelined ADC



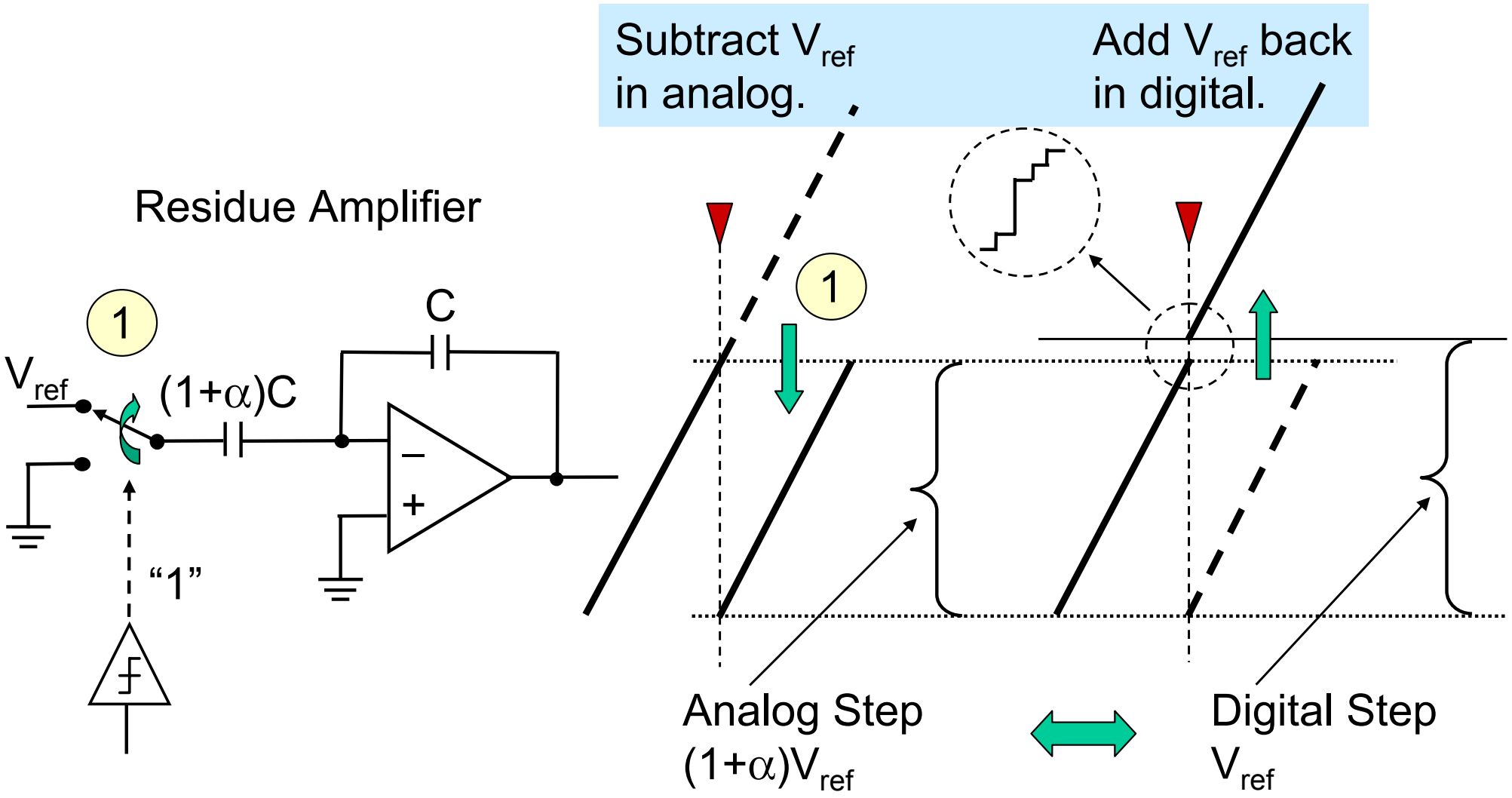
kT/C,
Clock Jitter*,
Switch Nonlinearity*,
Opamp Nonlinearity

* For input S/H only.

Metastability,
Latch Time,
Latch Hysteresis,
Preamp Offset

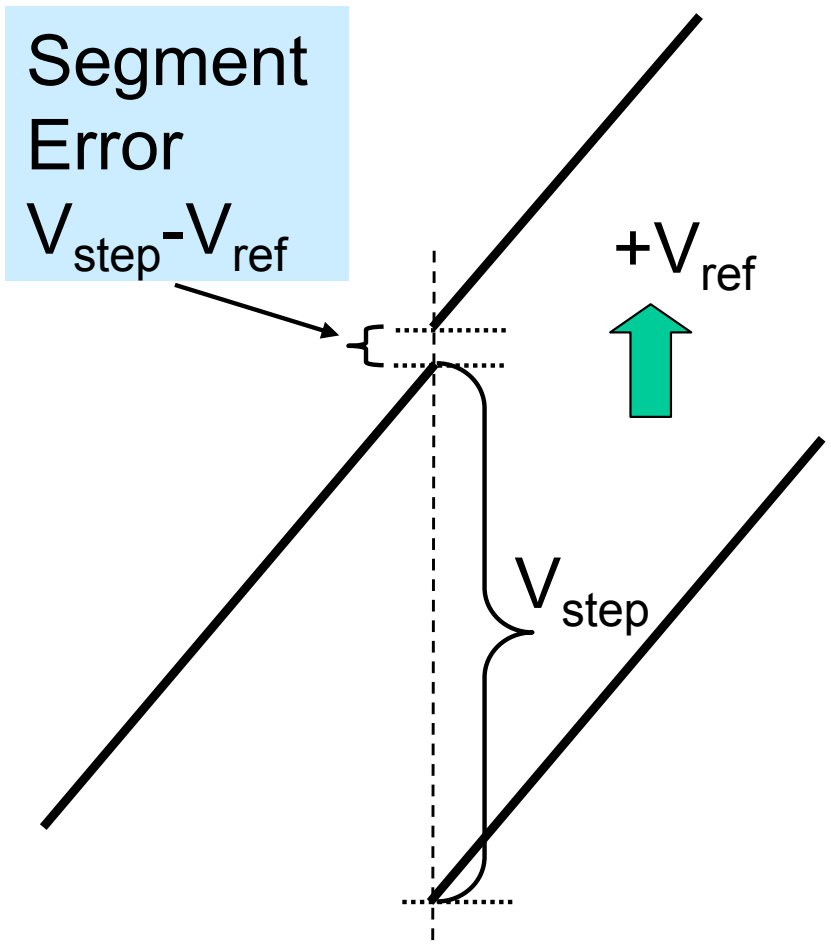
Capacitor Matching,
Opamp Settling,
Finite Opamp Gain,
Opamp Nonlinearity

Nonlinearity Error Source

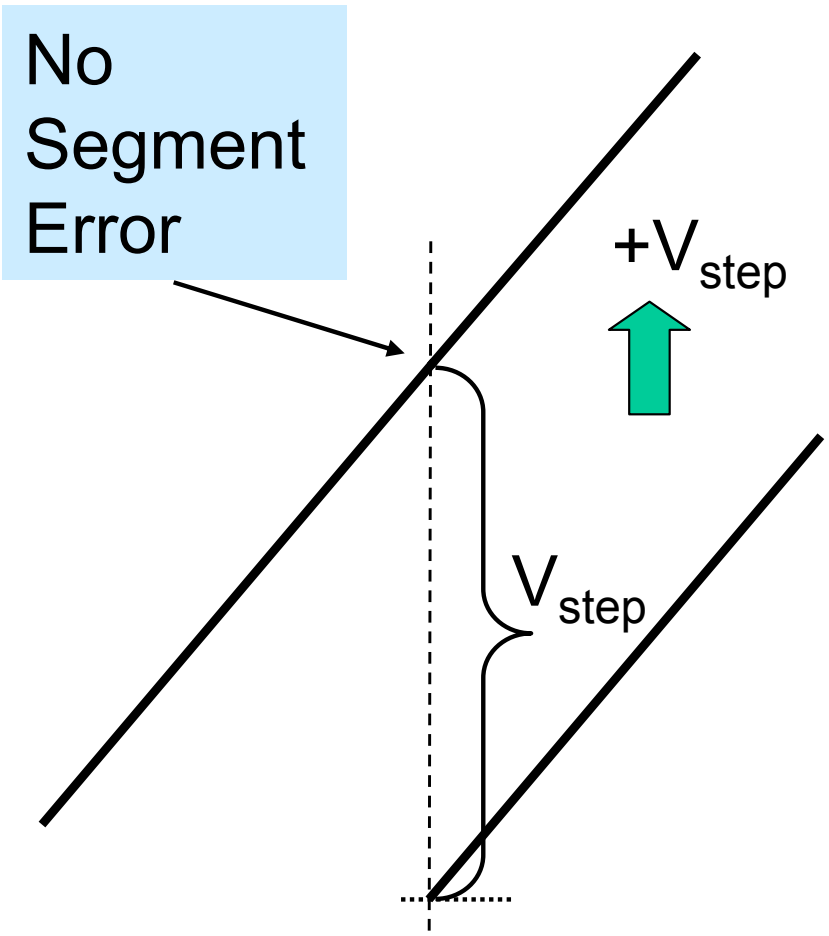


- Mismatch between analog and digital steps makes DNL.

Digital Correction vs. Calibration



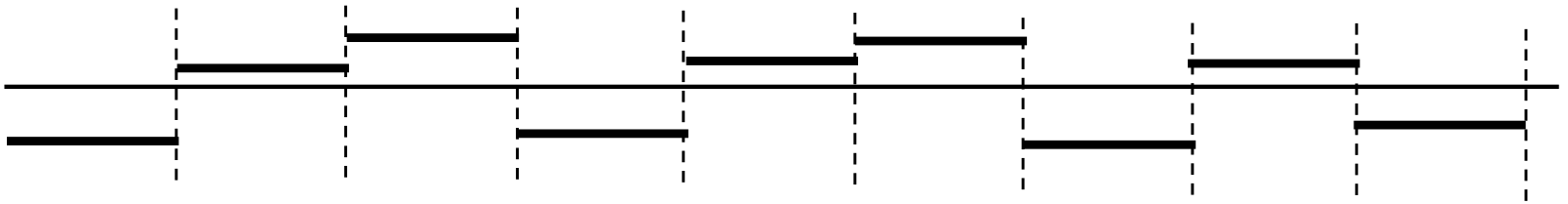
Digital Correction: Move segment up by V_{ref} digitally.



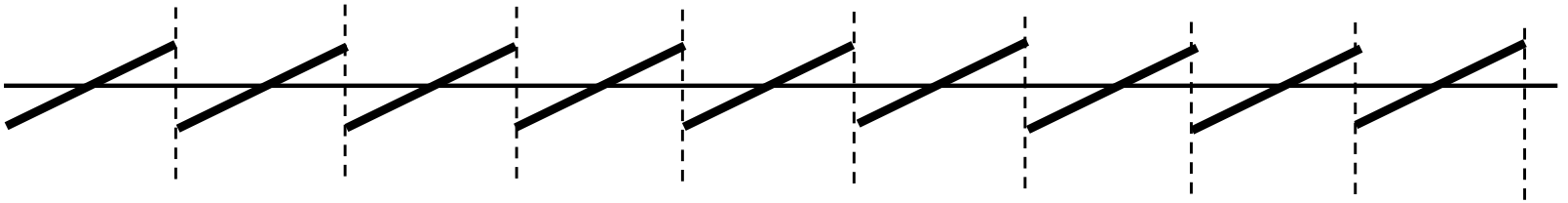
Digital Calibration: Move segment up by V_{step} digitally.

INL for Three Cases

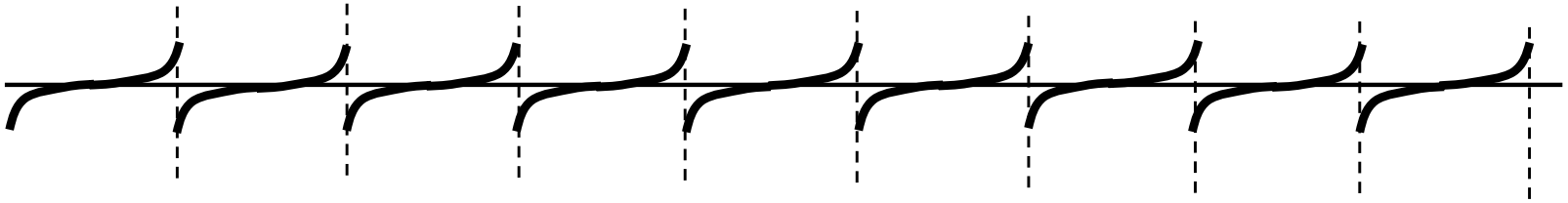
Capacitor Mismatch



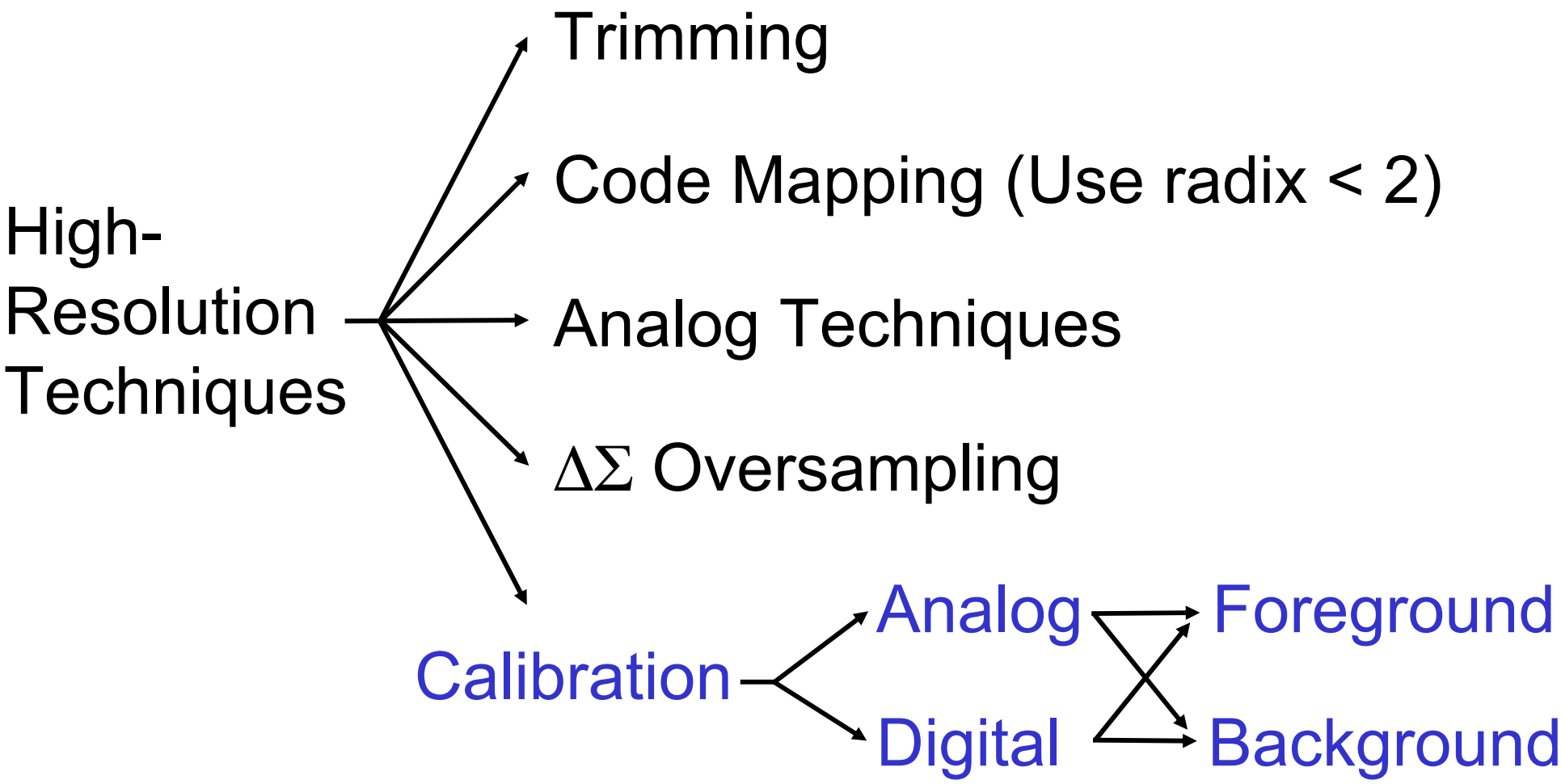
Low Opamp Gain



Opamp Gain Nonlinearity

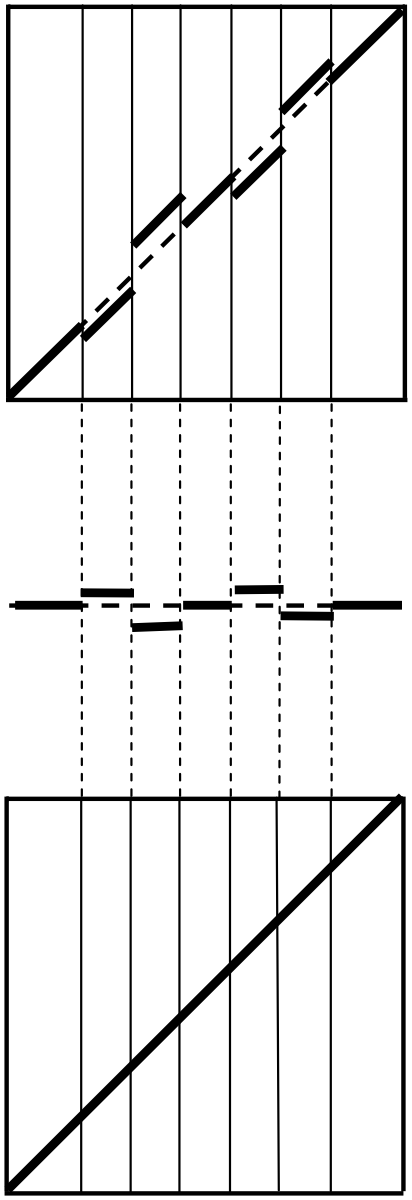


High-Resolution Techniques

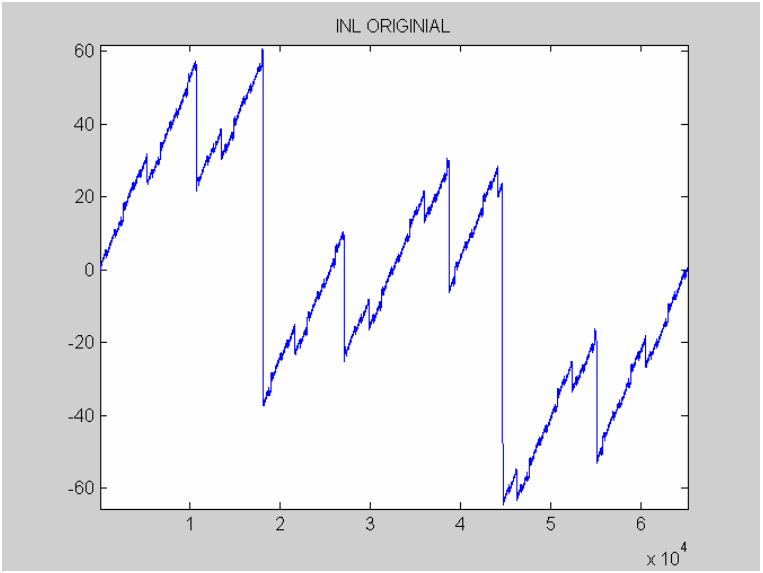


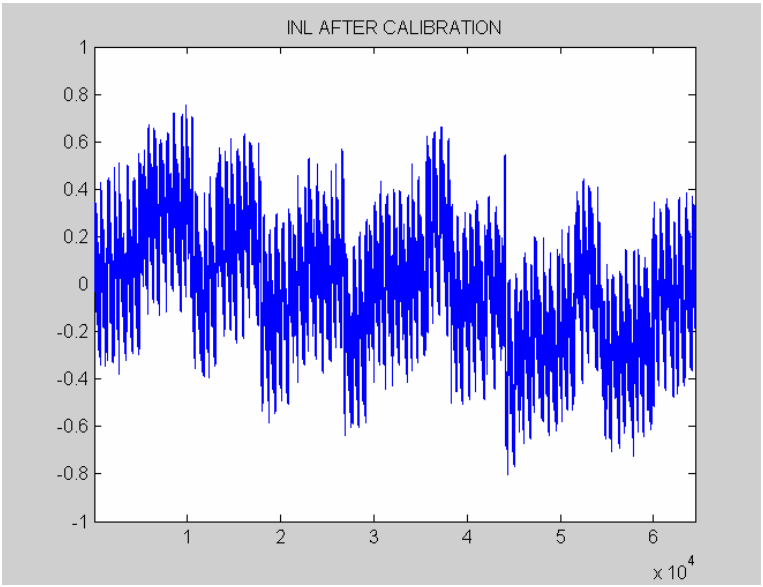
Digital Calibration Concept

(Lee, JSSC, Dec. 1992)



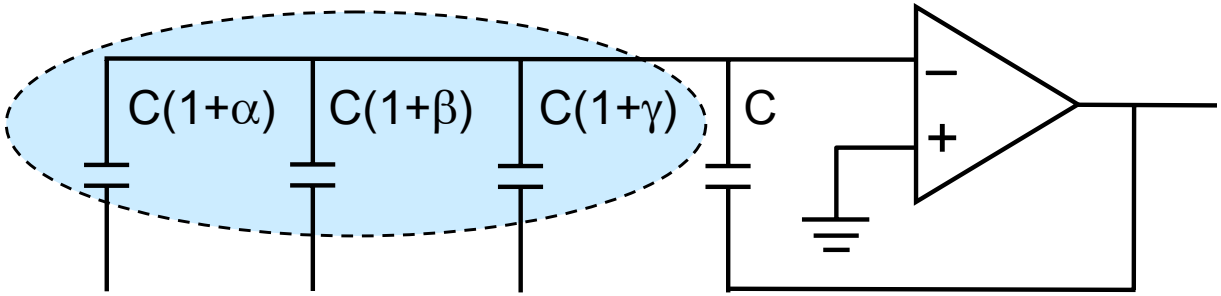
1. Measure segment errors.
2. Accumulate them for code errors.
3. Subtract errors digitally.





MDAC Capacitor Error

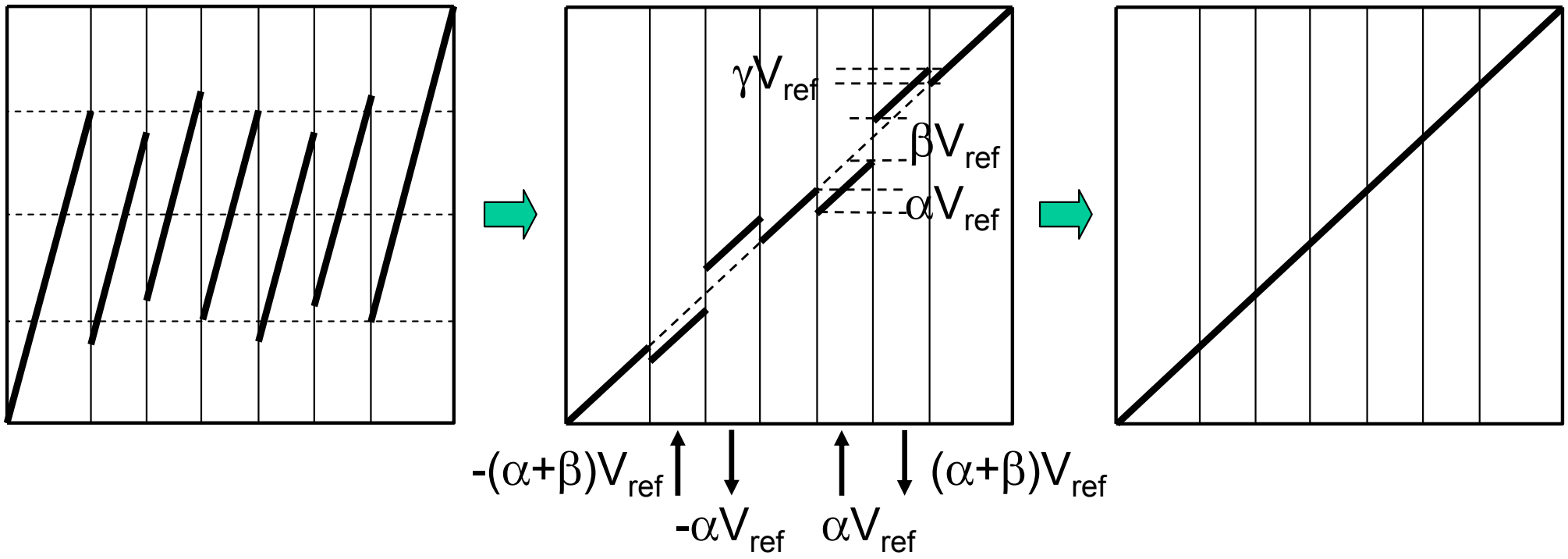
$\alpha+\beta+\gamma = 0$



Residue Output

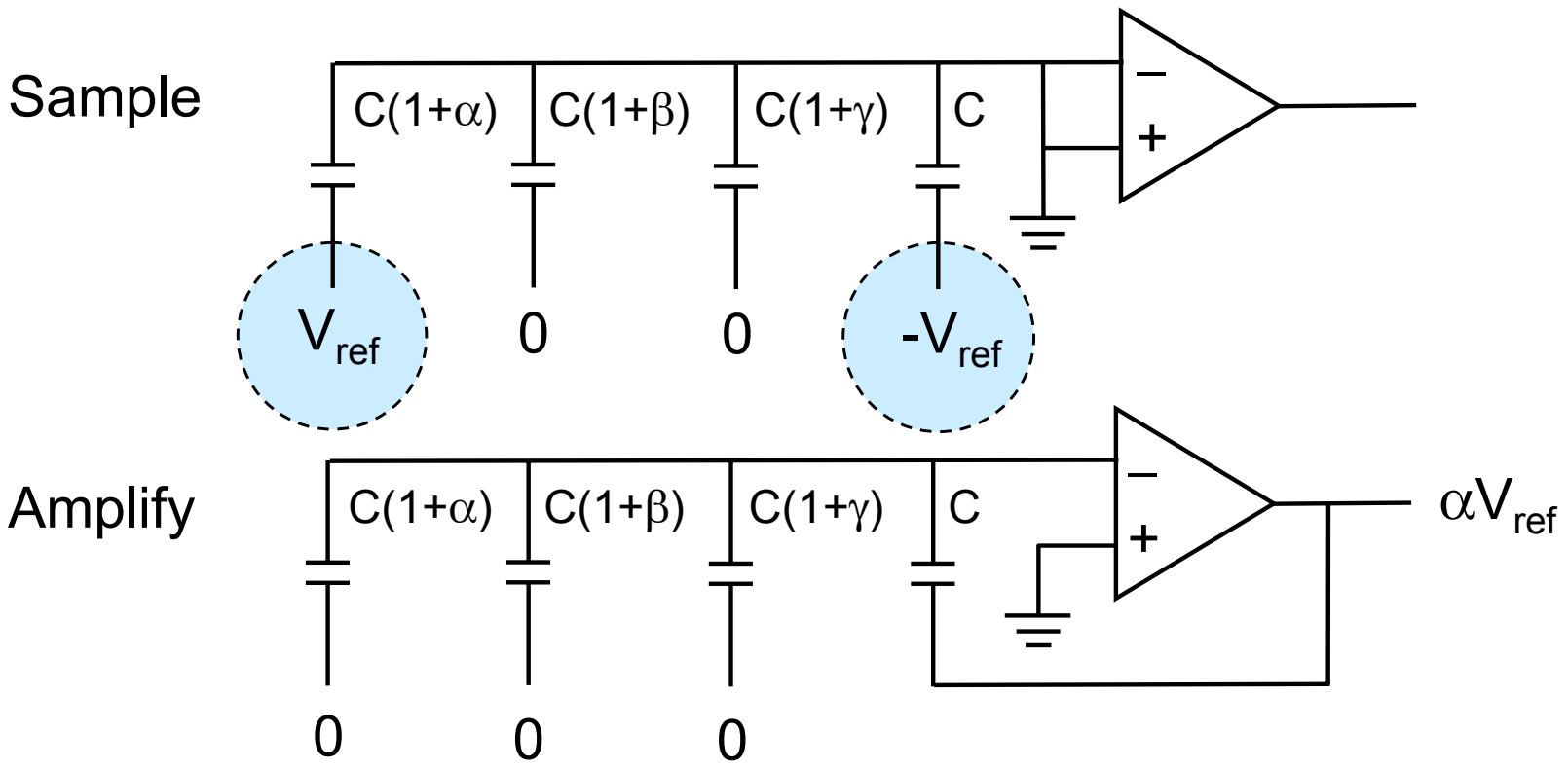
Transfer Function

After Calibration



- Move segments up or down by code error amounts.

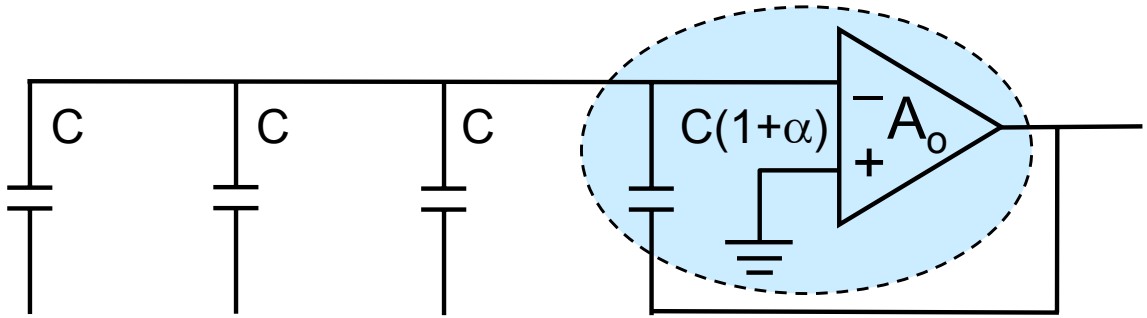
MDAC Capacitor Error Measurement



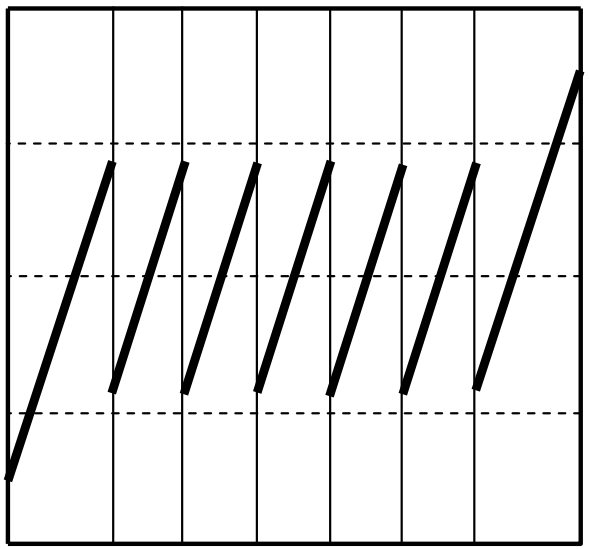
- Measure αV_{ref} , βV_{ref} , γV_{ref} by injecting V_{ref} into each caps.
- These are segment errors. Accumulate them to get code errors.

MDAC Gain Error

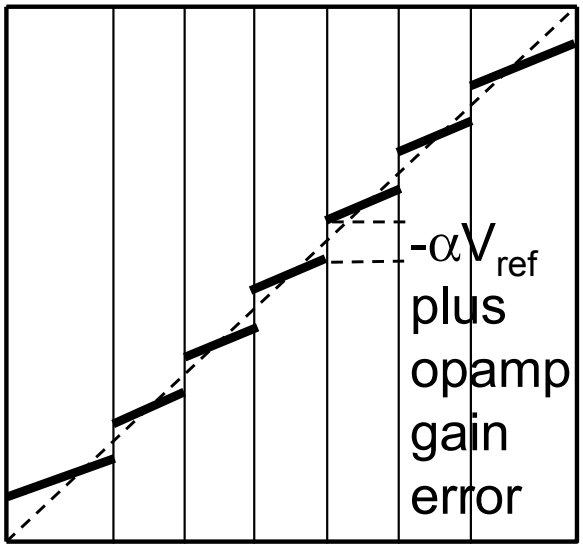
Mismatch α, and/or finite opamp gain.



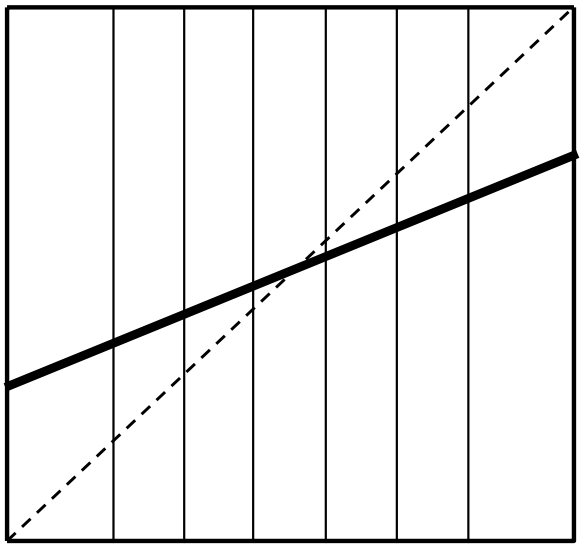
Residue Output



Transfer Function

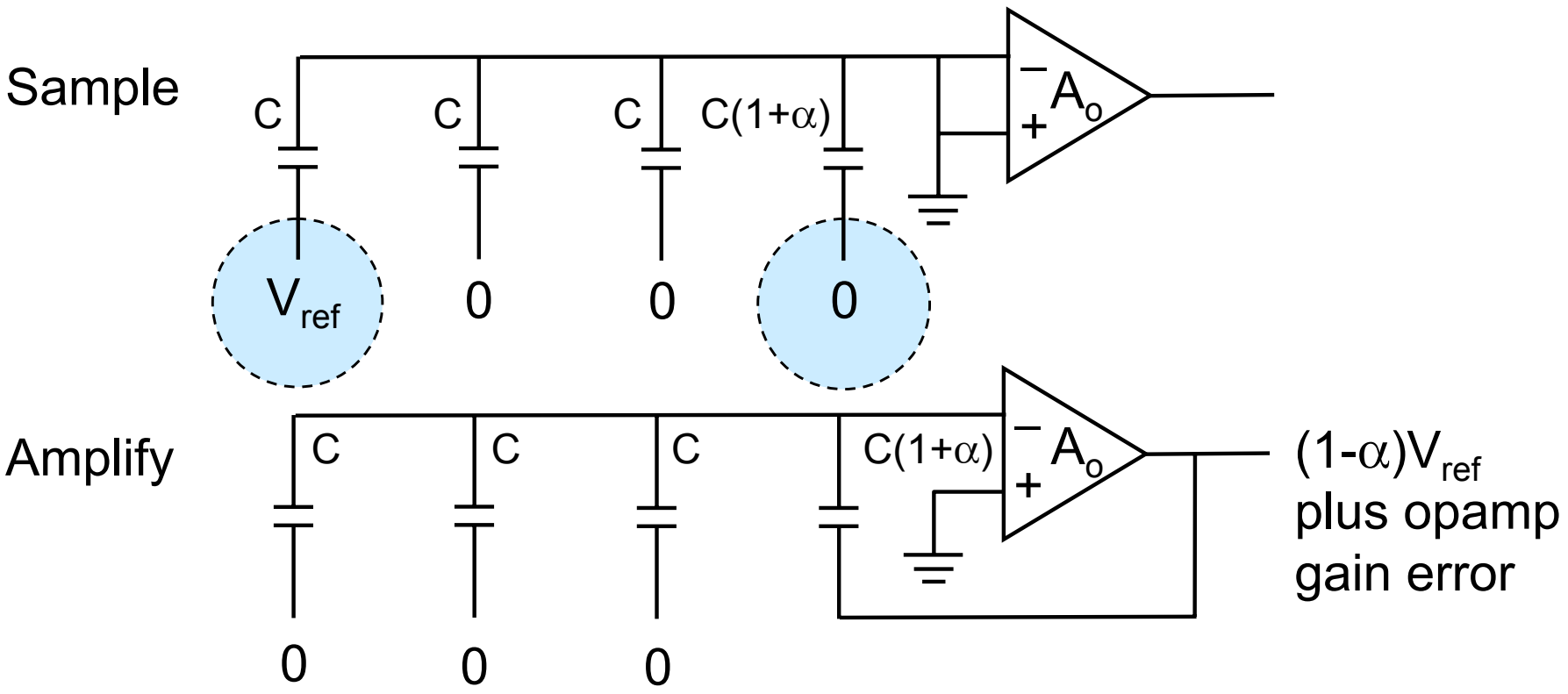


After Calibration



- Discontiuity is corrected by shifting segments up/down like capacitor error.

MDAC Gain Error Measurement



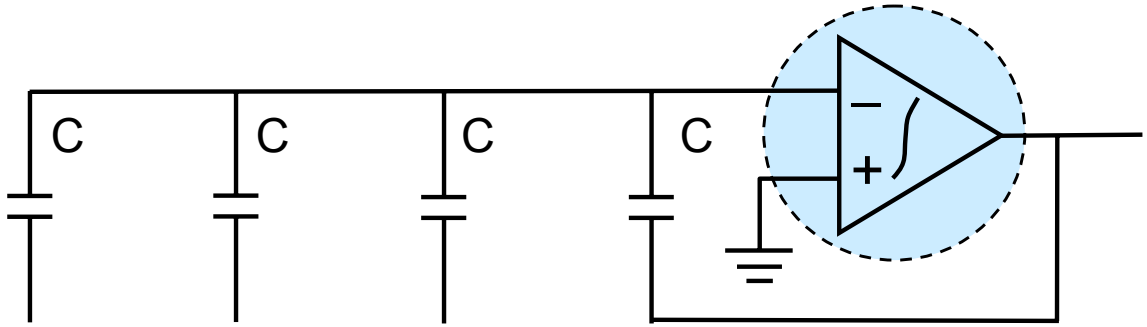
- Finite opamp gain A_o error can be measured together with capacitor mismatch error.
- Output may exceed V_{ref}.

What If Output Exceeds V_{ref}?

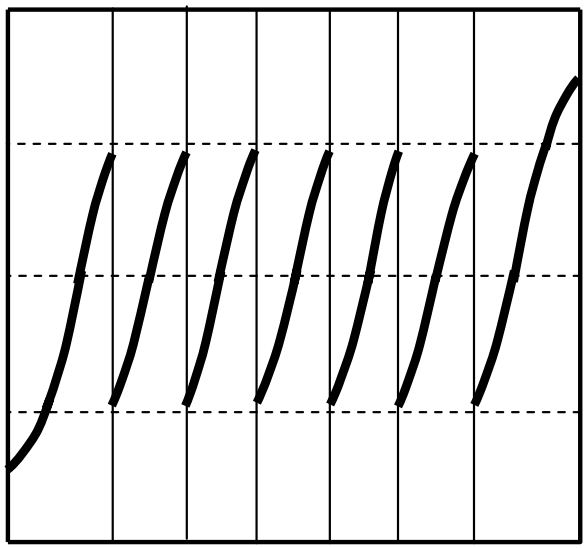
- Use a radix smaller than 2 to contain output within V_{ref}. (Karanicolas, JSSC, Dec. ’93)
- Split capacitors into two and limit output swing to $V_{ref}/2$, and add two half V_{ref} errors to get the whole V_{ref} error. (Moon, TCAS-II, Feb. ’97)
- Extend the output range to cover more than V_{ref}.
- Use V_{cal} which is $<V_{ref}$, and digitally subtract it, but need to know V_{cal} to a certain accuracy.
- Initialize with $-V_{cal}$, and measure $V_{ref} - V_{cal}$.

MDAC Gain Nonlinearity

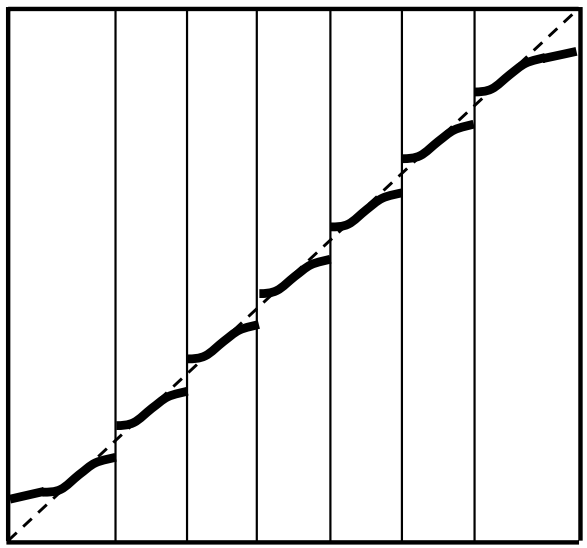
Nonlinear opamp gain.



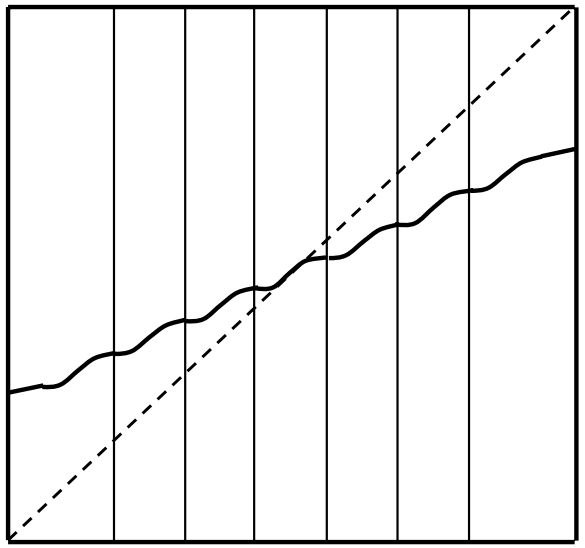
Residue Output



Transfer Function



After Calibration



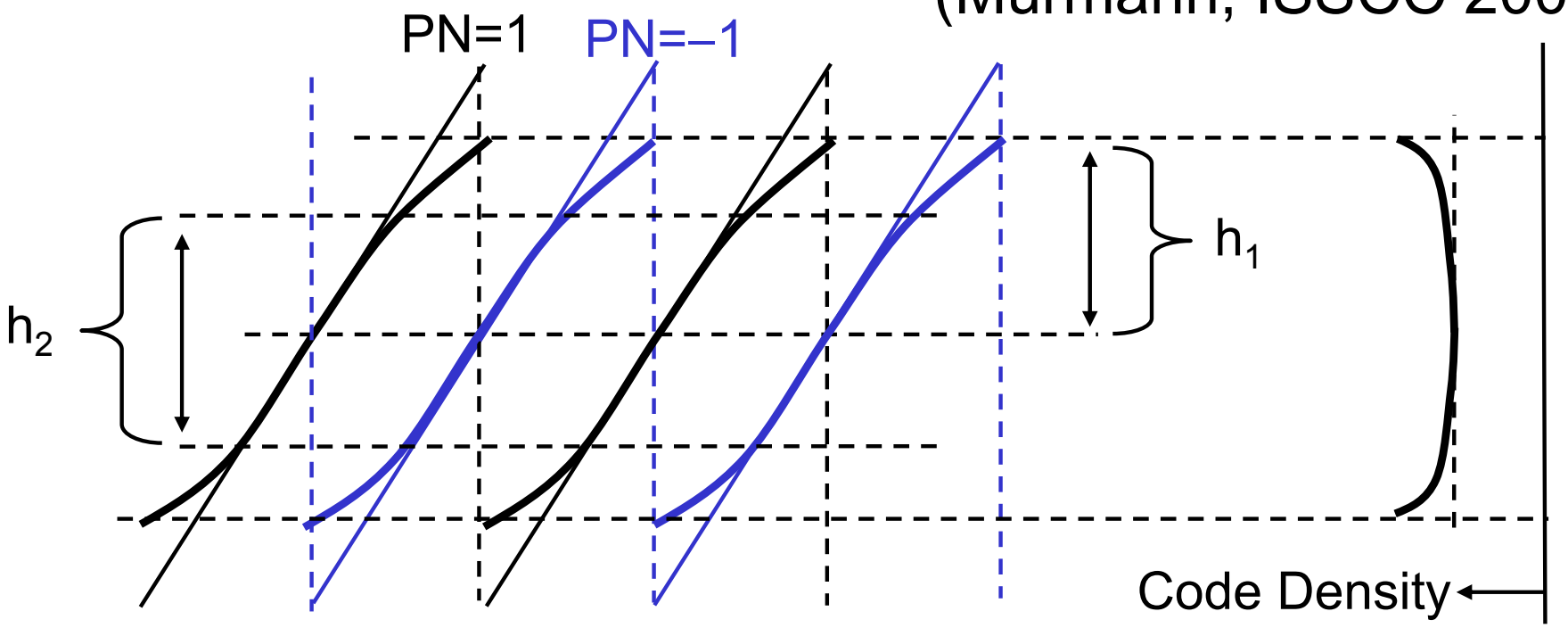
- Discontiuity is corrected like capacitor and gain errors,
  but residual nonlinearity remains.

Embedding Measurement in Background

- Retiring → Retire hardware for calibration.
  (Shouwenaars, JSSC, Dec. 1988, Ingino, JSSC, Dec. 1998,
  Choe, JSSC, Dec. 2000)
- Skip and Fill → Skip normal cycles randomly for error measurement and fill in missing data point by interpolation.
  (Moon, TCAS-II, Feb. 1997)
- Q-Based → Steal cycles for calibration by operating S/H faster than the normal operation. (Blecker, ESSIRC 2000)
- Code Density → Estimate errors from output code density.
  (Murmann, ISSCC 2003)
- Dithering or Shuffling → PN scrambling of errors and digital correlation and cancellation.
  (Ming, ISSCC 2000, Galton, TCAS-II, Mar. 2000)

Background Nonlinearity Measurement

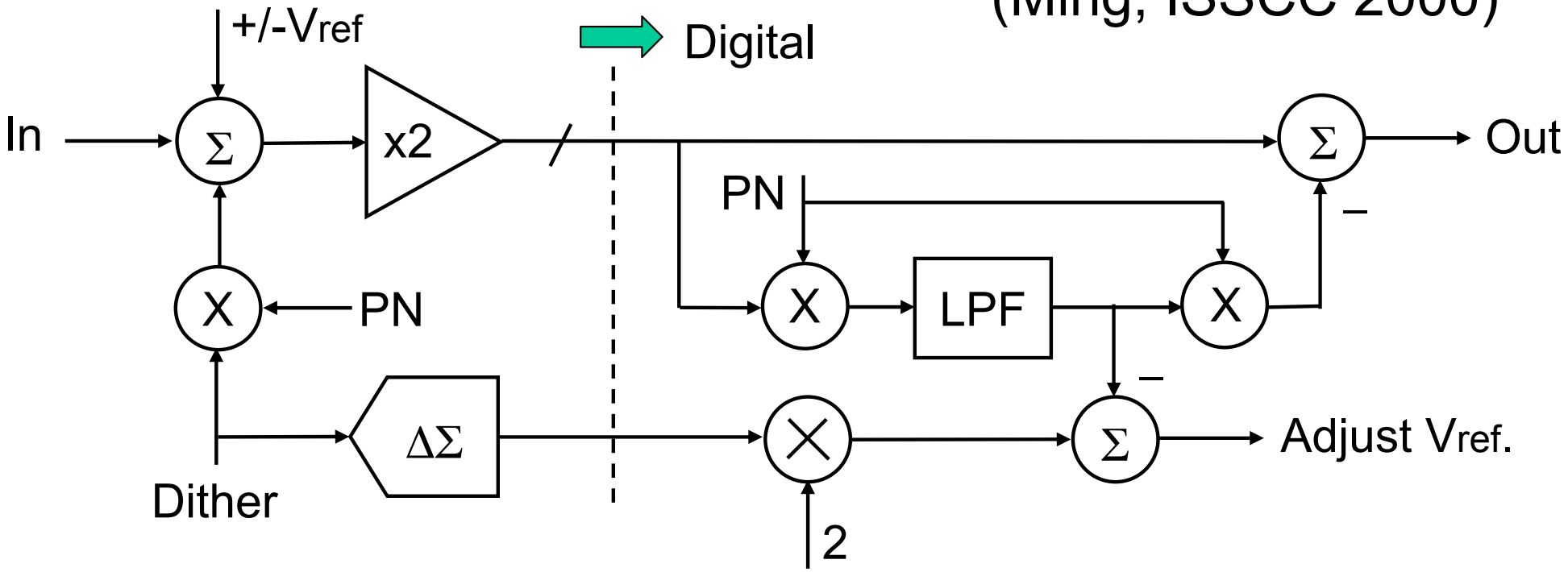
(Murmann, ISSCC 2003)



- Random comparator threshold jump generates two residue curves with constant vertical gap.
- Gain nonlinearity makes $h_1 < h_2$. The difference is measured by code density, and nonlinearity is fitted with a polynomial.

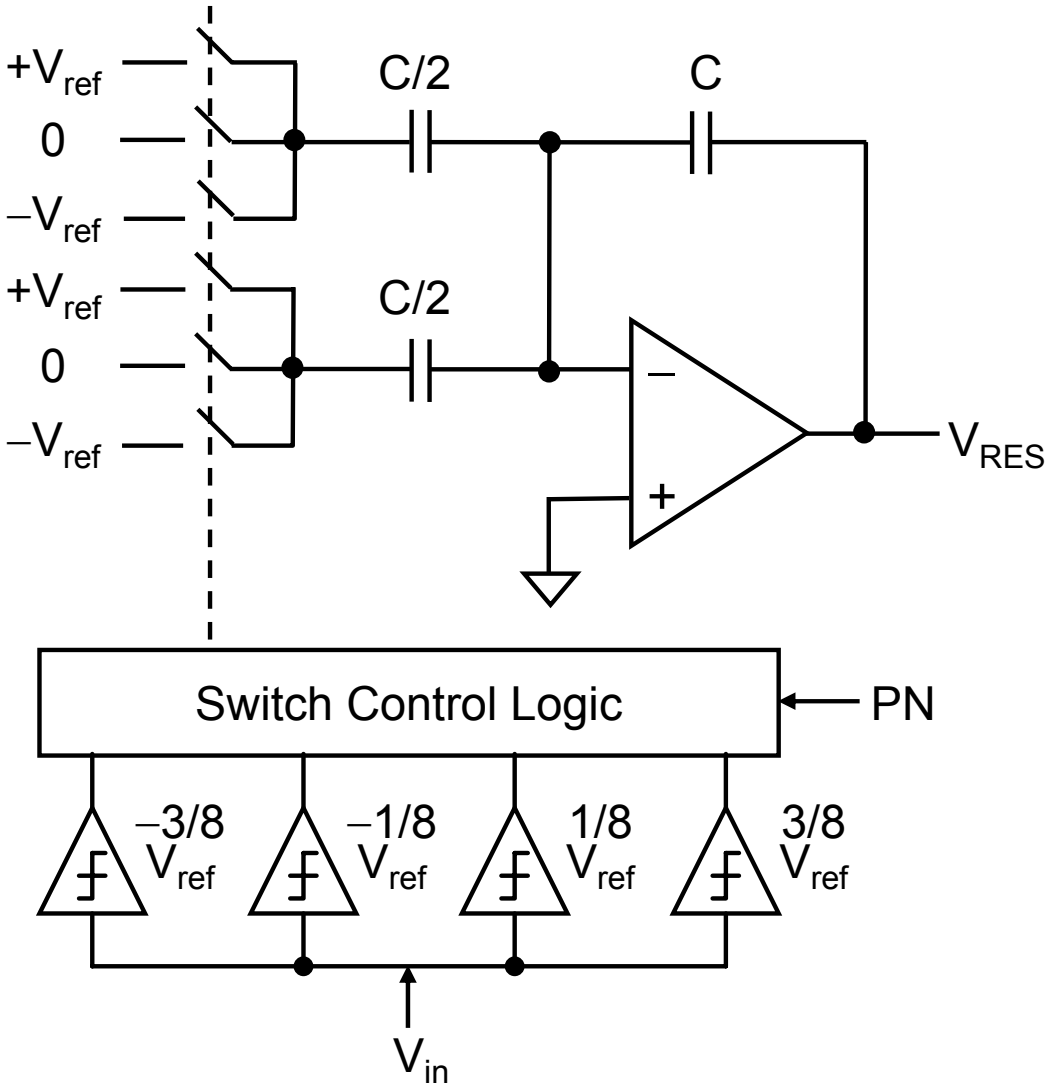
Background Calibration by Dithering

(Ming, ISSCC 2000)

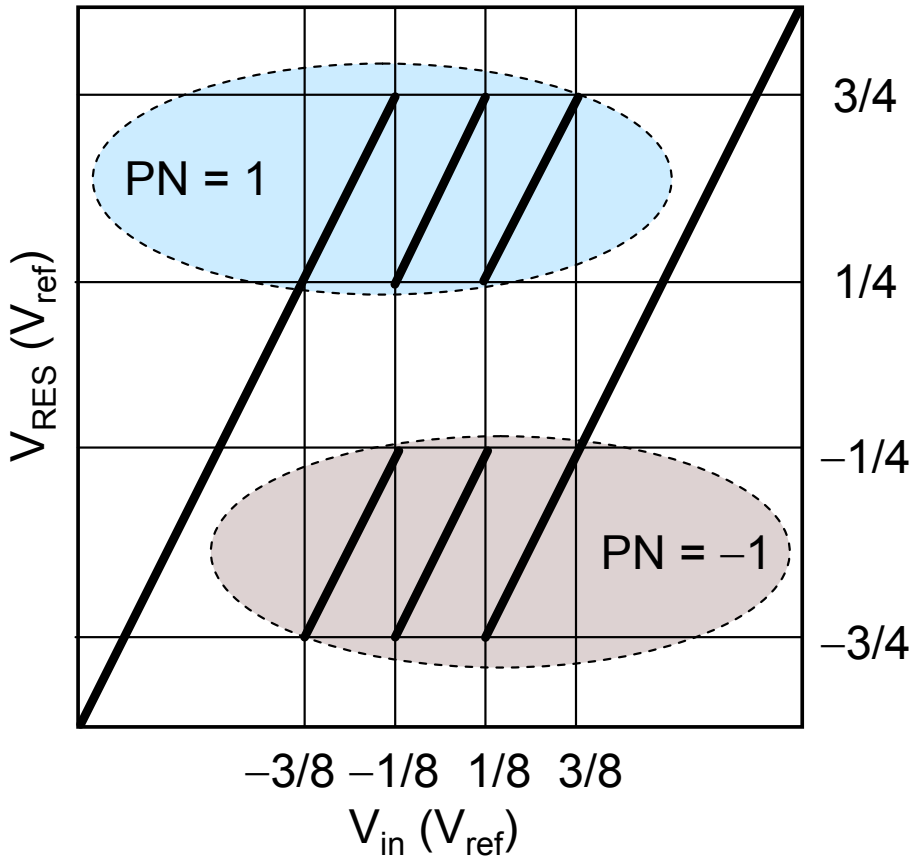


- Measure dither with slow but accurate ΔΣ ADC, and compare it with quantized dither to measure the gain error.
- Adjust V_{ref} to match with the subrange.
- Signal range is reduced for dithering.

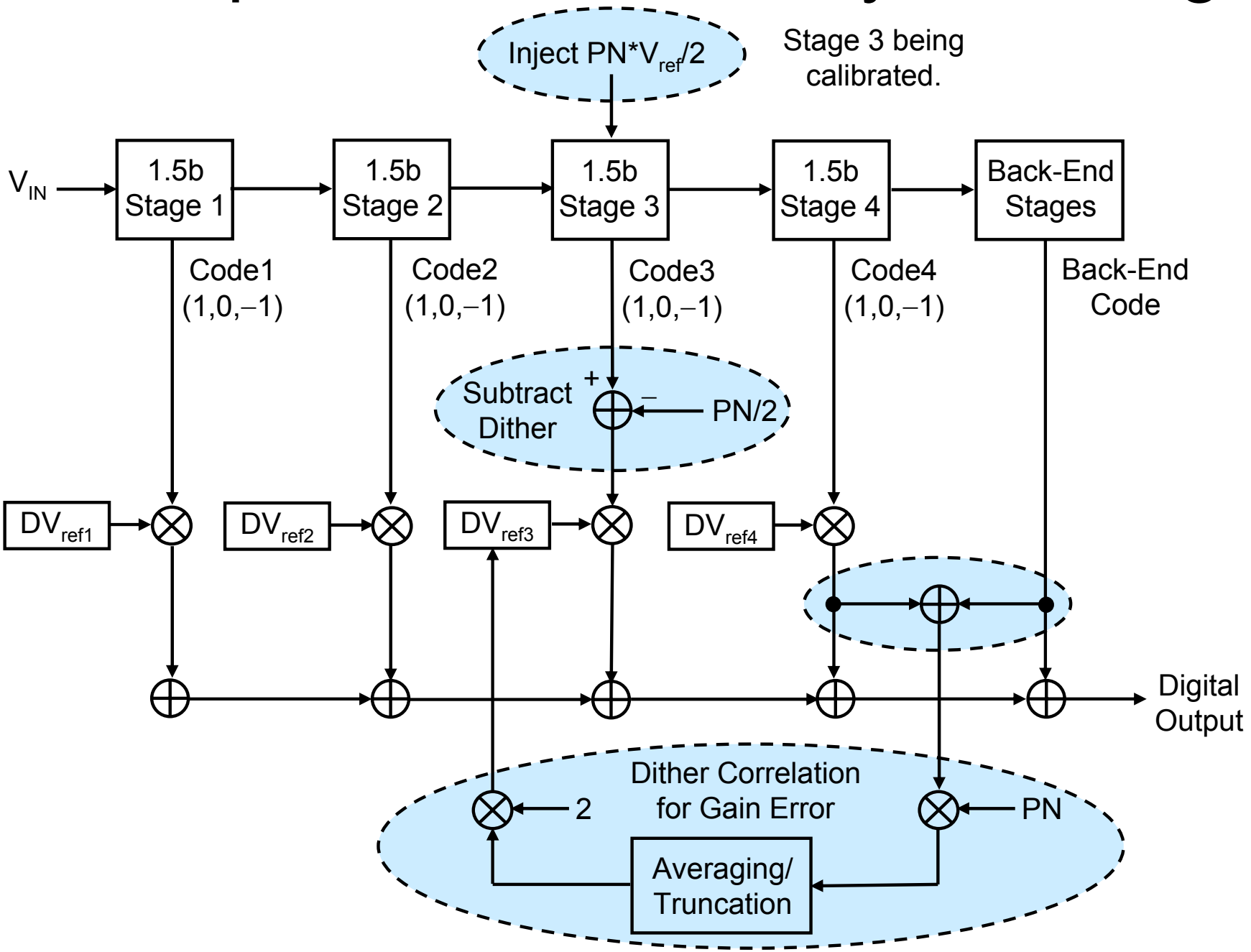
1.5b MDAC Stage Modified for Dithering



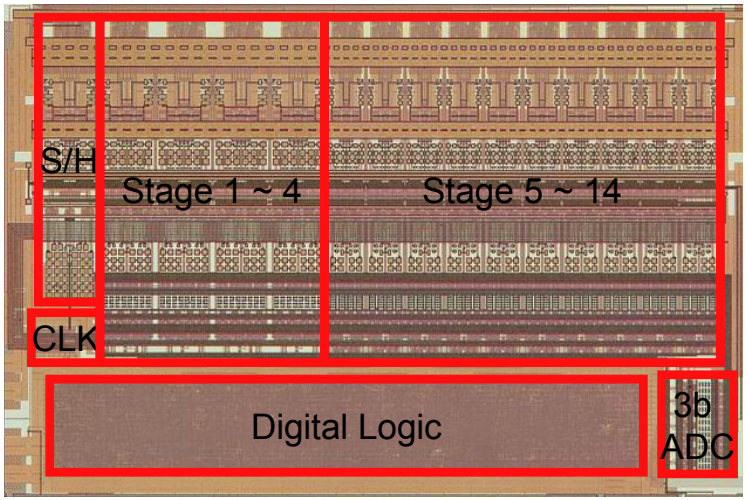
- Split reference injection to keep the signal range.

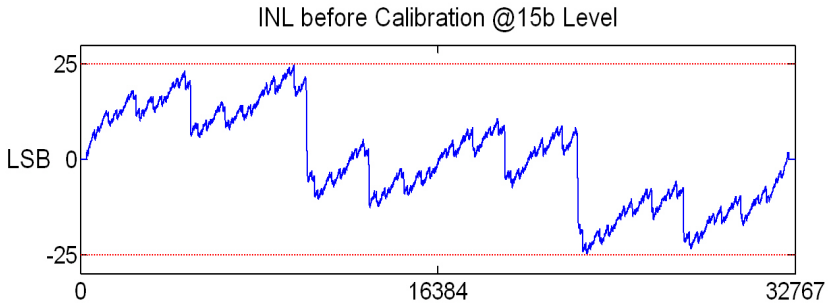


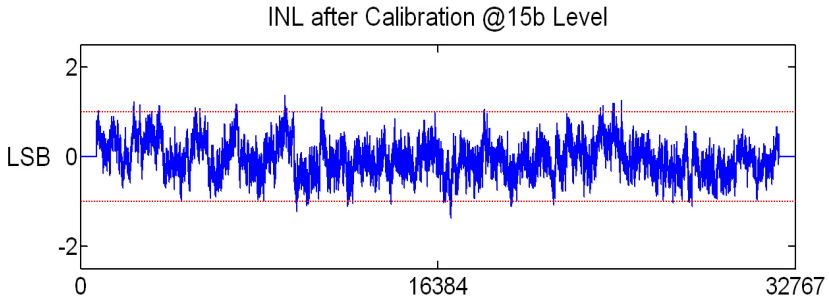
Example of Calibration by Dithering



1.5b/stage ADC Calibrated by Dithering

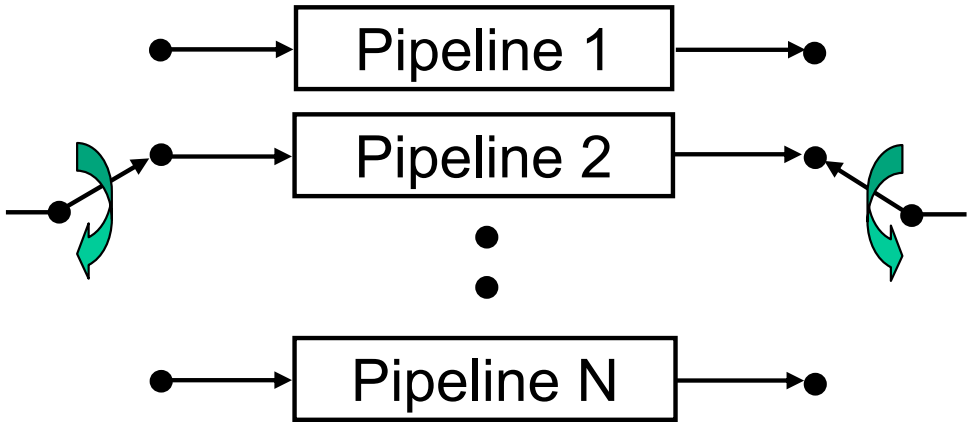


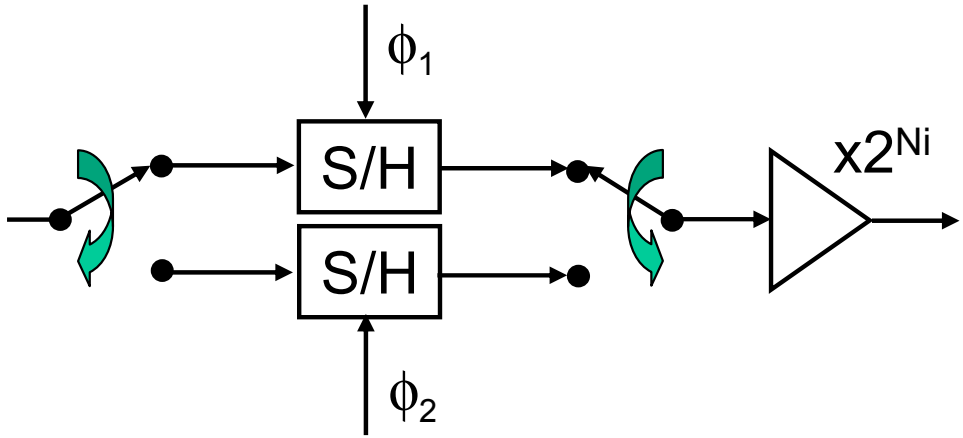




Technology	0.18μ CMOS
Resolution	15b
Speed	20MS/s
Supply	1.8V
Reference	1.4V/0.4V
DNL/INL	0.4LSB/1.3LSB
Peak SNDR	72.6dB
SFDR	98dB
THD	-92dB
Calibration	45sec
Active Area	2.3x1.7mm^2
Power	280mW (Analog)

Other Variations of Pipelined ADC





Time-interleaved N-path

Duplicate hardware for speed.

(Conroy, JSSC, April 1993)

Offset, gain, timing errors

One S/H for timing error.

May calibrate path offset and gain.

Still DNL errors show up

as time-varying spurious tones.

Opamp-sharing

Reuse hardware for low power.

(Nagaraj, JSSC, March 1997)

Opamp input is never reset.

Twice output worst-case settling.

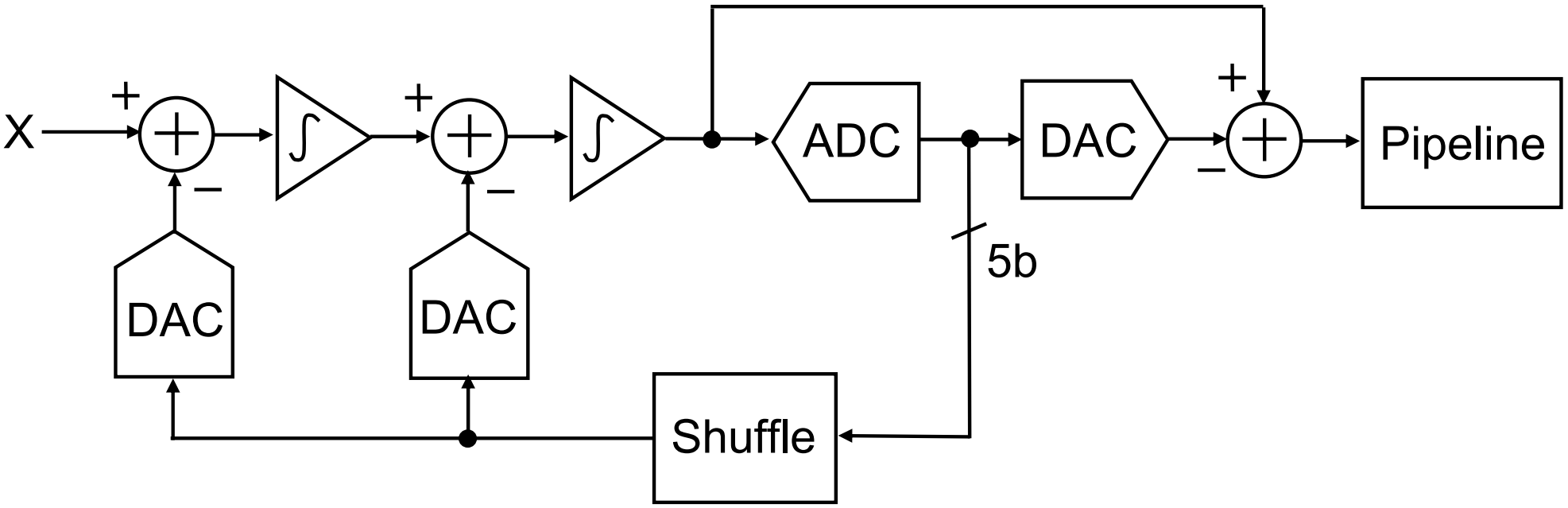
Time-varying input capacitance

Opamp input switching makes it

sensitive to supply noise.

Pipelined ADC with ΔΣ Front-End

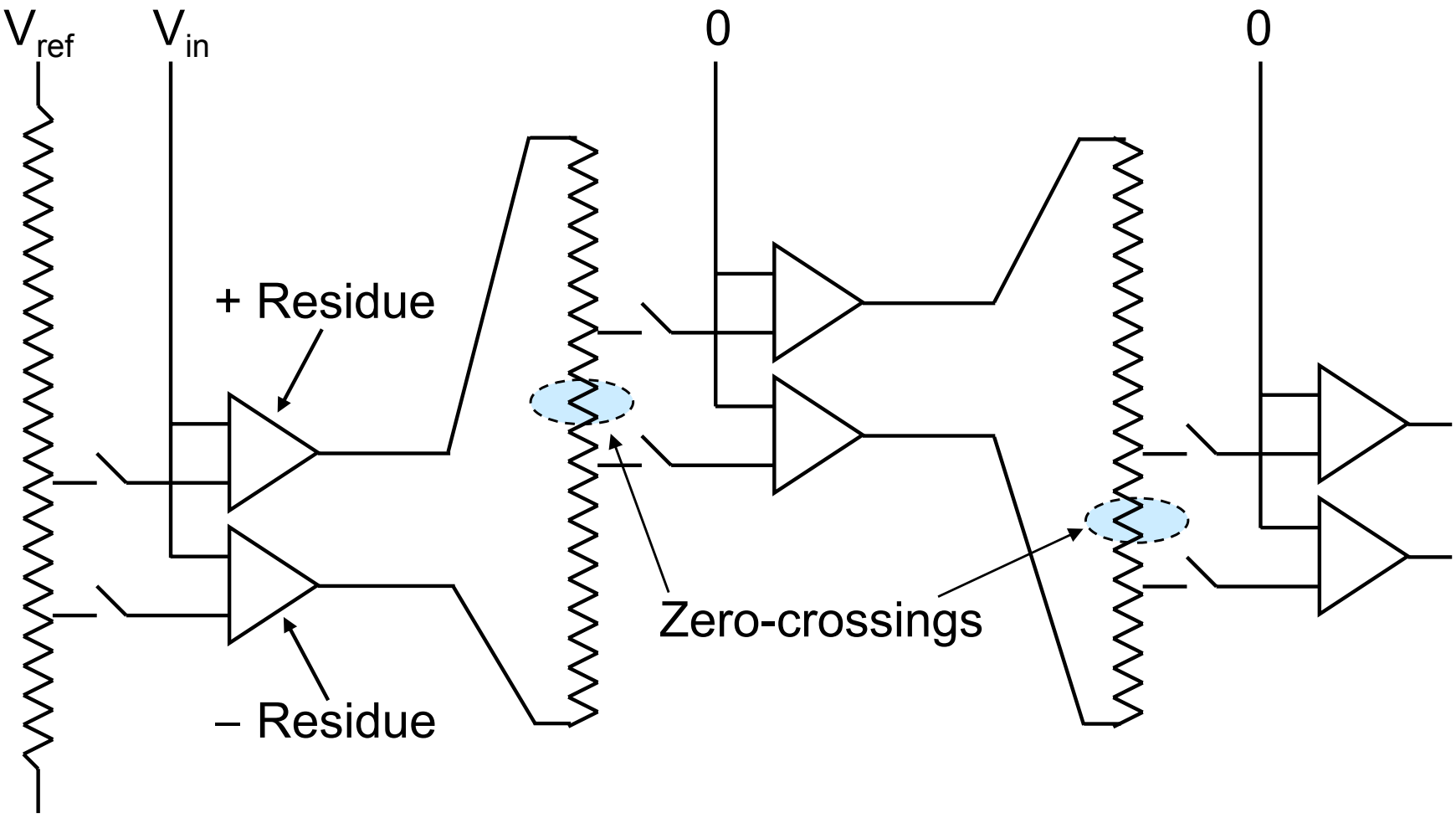
(Brooks, JSSC, Dec. 1997)



- ΔΣ modulator front-end coupled with pipeline rear-end.
- x8 oversampling, 89dB SNR @ 2.5MS/s.
- 0.6μ CMOS, 55mW @ 5V, 5.7 x 6.2mm².

Two-Residue Pipelined ADC

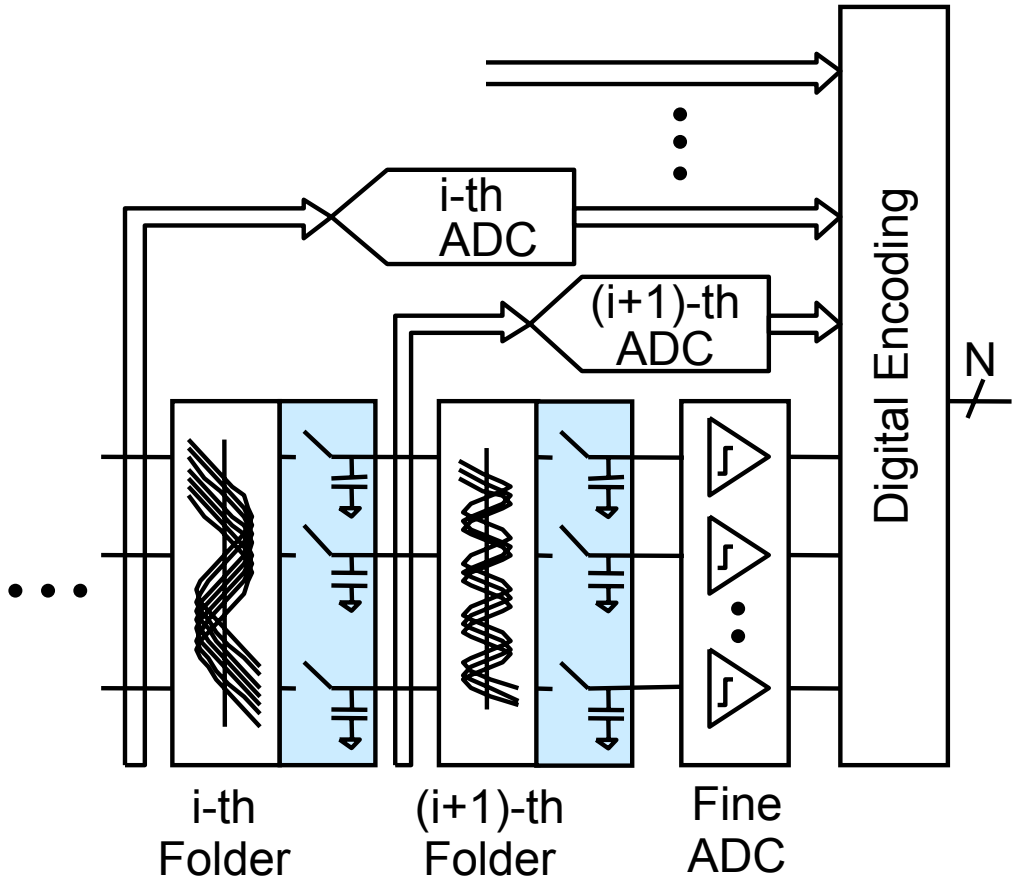
(Mangelsdorf, ISSCC, 1993)

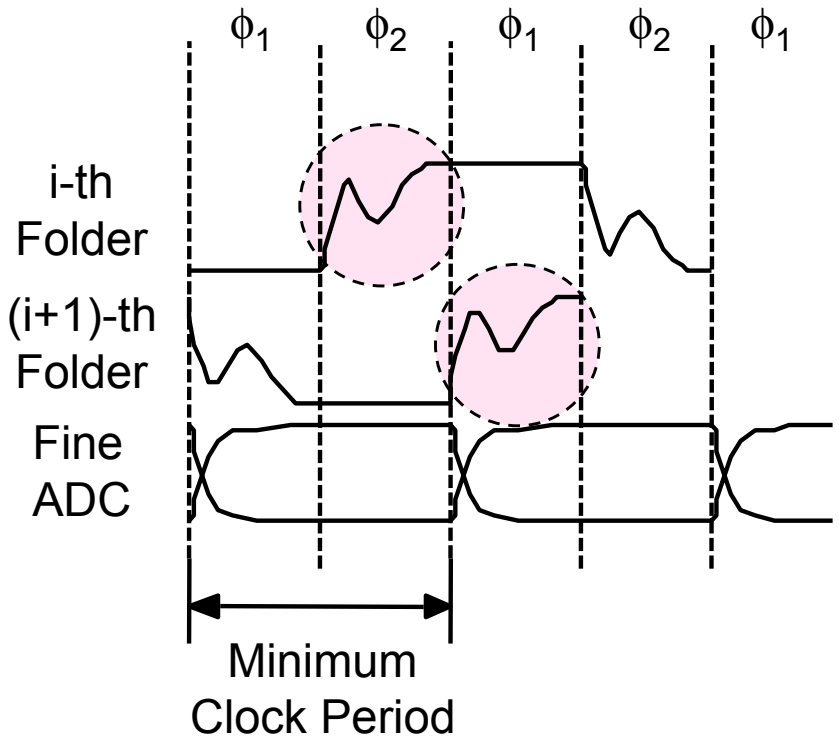


- Low gain, slow settling amplifier for zero crossings.
- Suffer from reference error, offset and gain matching.

Pipelined Folding ADC

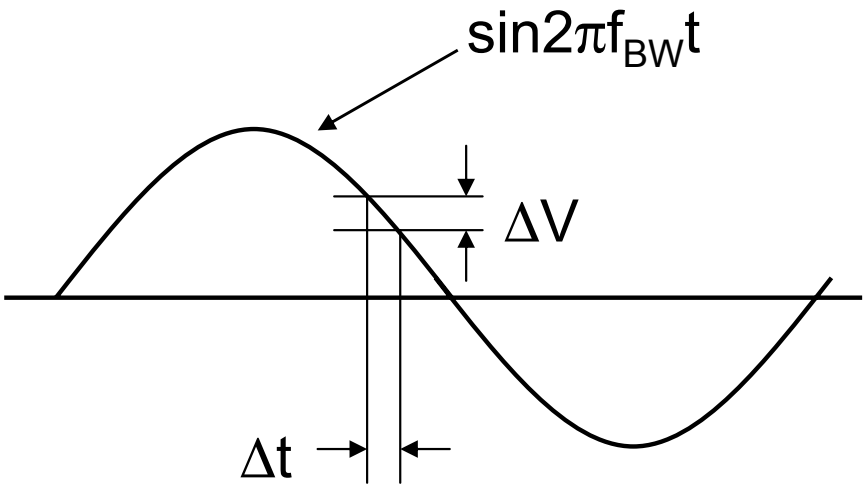
(Choe, JSSC, Dec. 2000)



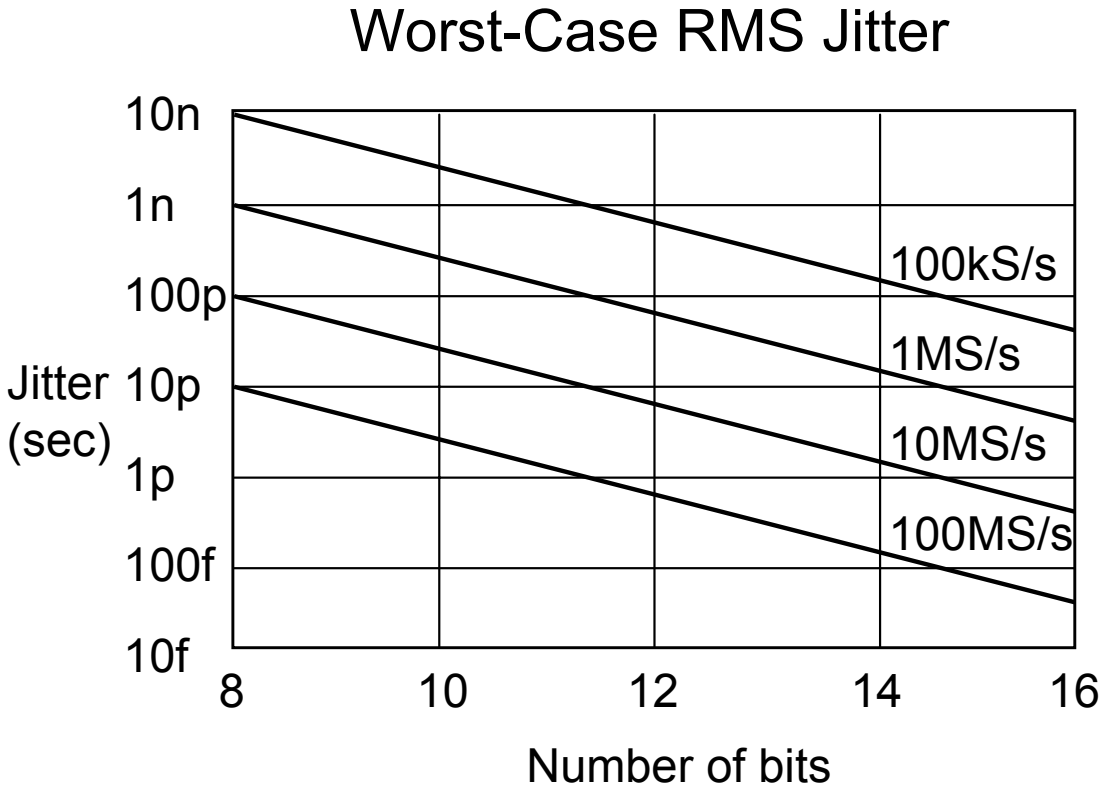


- Achieves high folding degree without speed constraint.
- Further reduction in the number of comparators.
- Less accurate distributed interstage sampling.

Sampling Clock Jitter



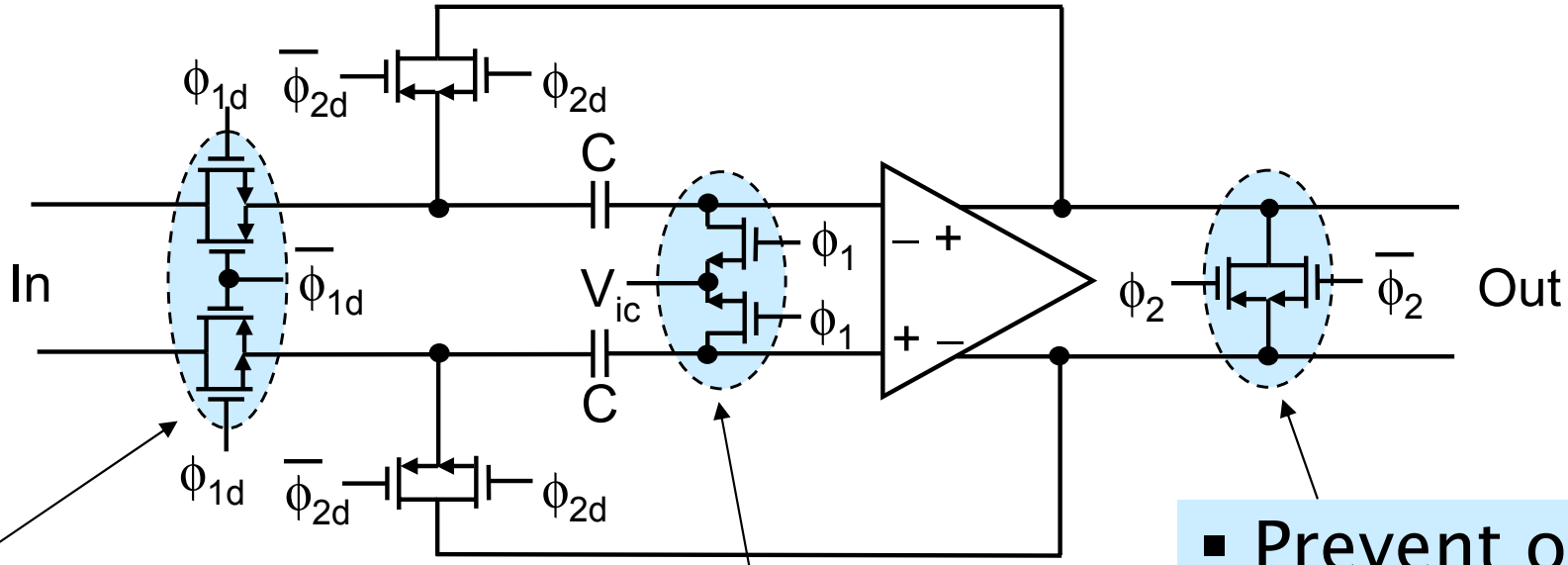
$$\Delta t_{rms} = \frac{1}{2\pi f_{BW} 2^N} \sqrt{\frac{2}{3}}$$



- Worst-case RMS jitter < Q noise.
- Right signal at wrong time = Wrong signal at right time.
- Worst-case jitter should be < 80fsec for 15b @100MS/s.

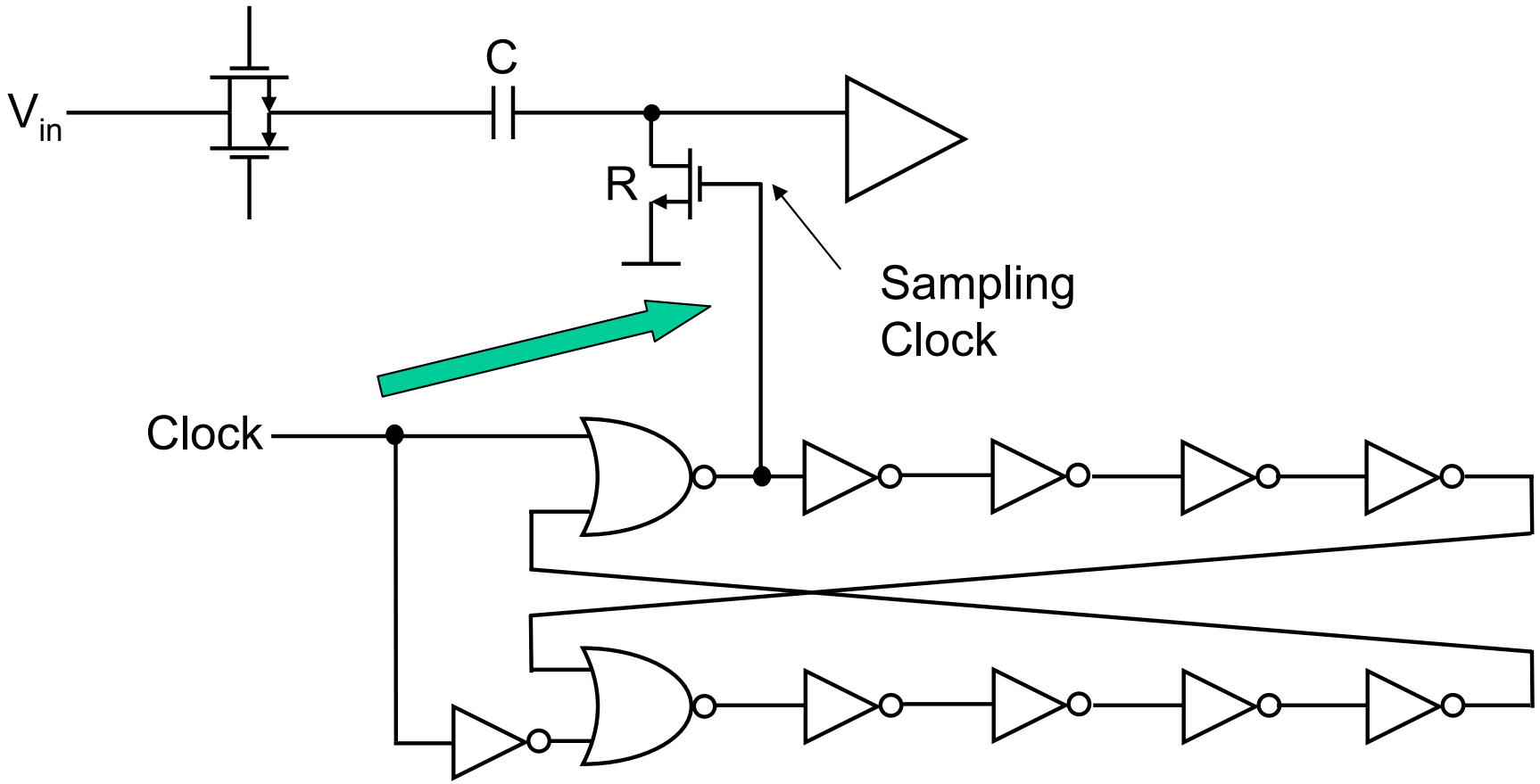
Bottom-Plate S/H Design

(Li, JSSC, Dec. 1984)



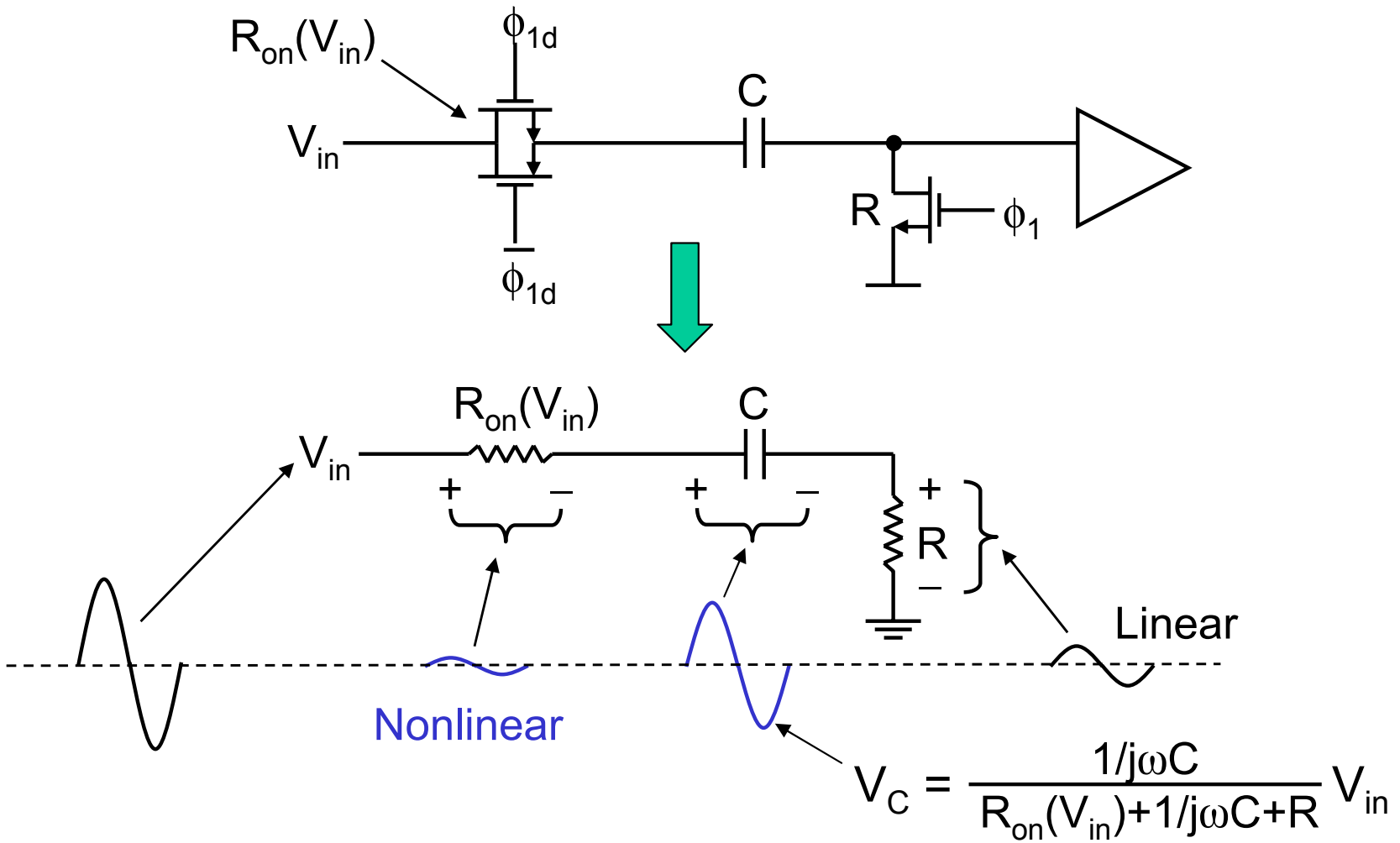
- Minimize bottom switch on-resistance and watch its nonlinearity.
- Turn off top switches early to reduce V_{th}-dependent nonlinear clock feed-through and fall time effect.
- Prevent output from wandering during sampling

Low-Jitter Sampling Clock



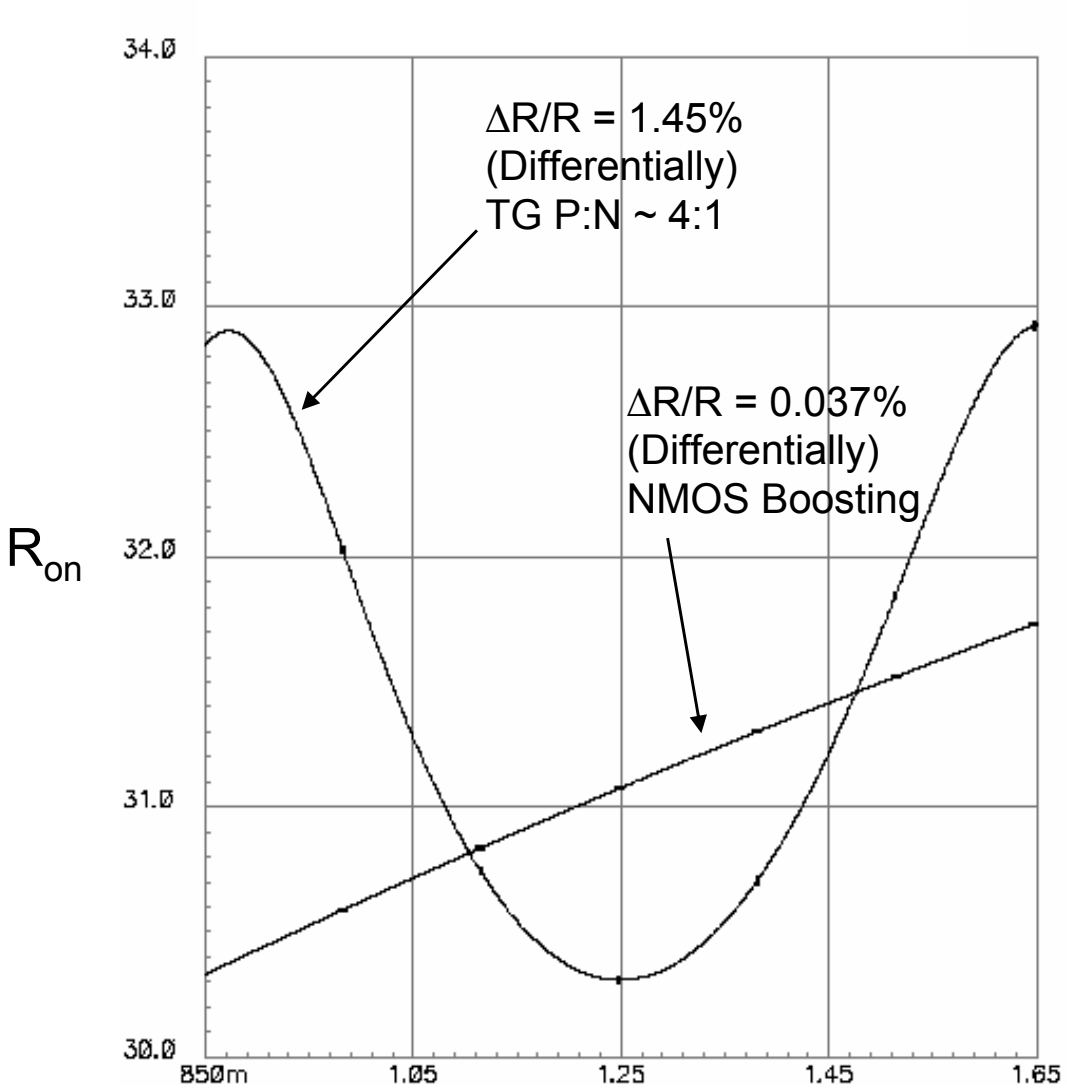
- Use a low-jitter clock source, and minimize the clock delay.
- Square-wave clock is difficult to match impedance at a board level. Use a crystal filter for sinusoidal clock.

Bottom-Plate Switch Nonlinearity



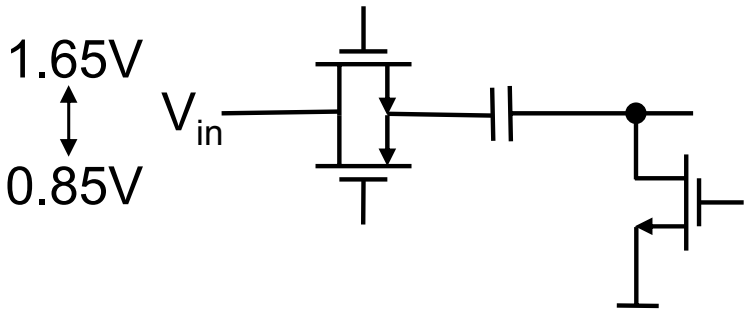
- R_{on} nonlinearity is dominant in sampling.
- Reduce voltage drop across R_{on}, and keep R_{on} constant.

Nonlinearity of Bottom Switch

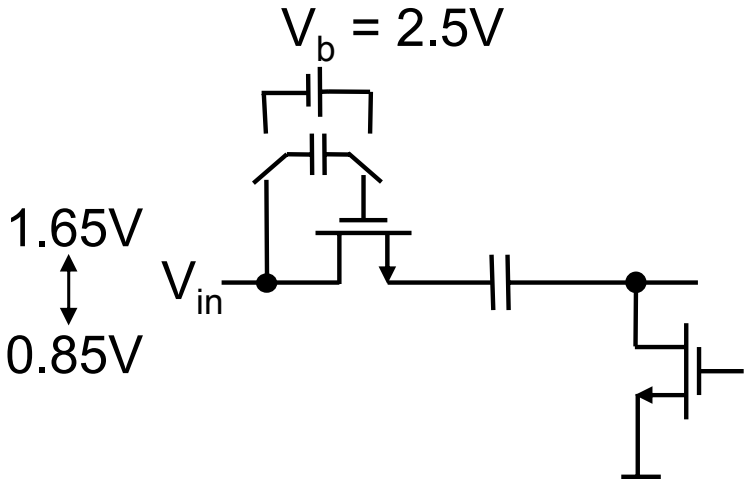


Single-Ended Input

Transmission Gate(TG)



NMOS Boosting



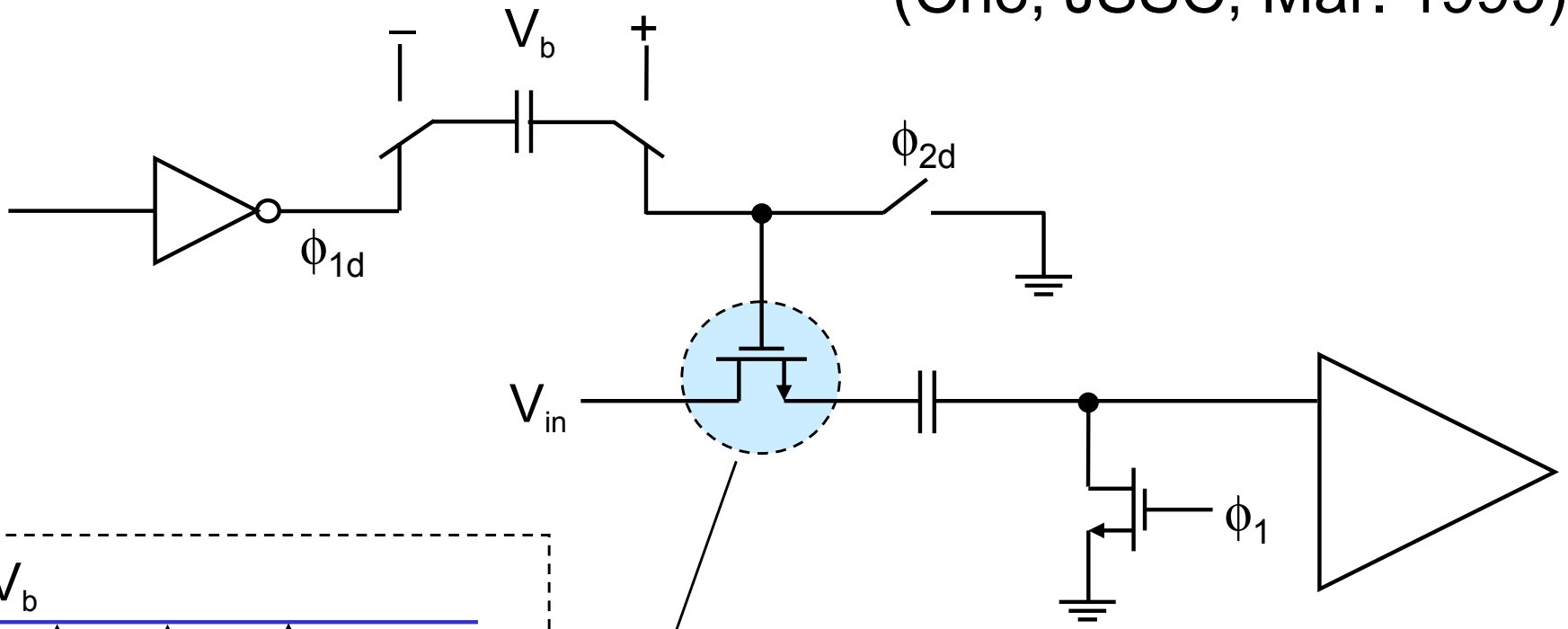
0.25μ process @2.5V

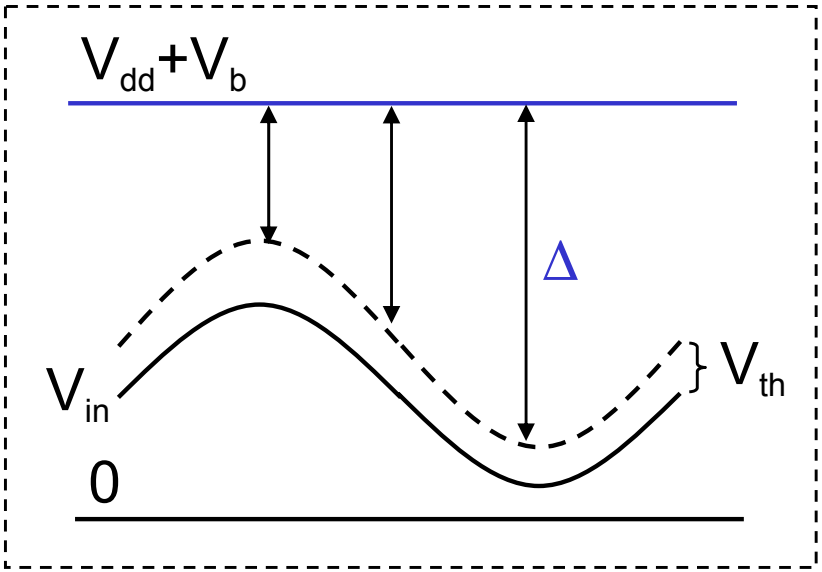
$15\tau = 15(R_{on}+R)C < T/2$

$R \approx 10R_{on}$, C = 0.5pF

Clock Boost for Low R_{on}

(Cho, JSSC, Mar. 1995)



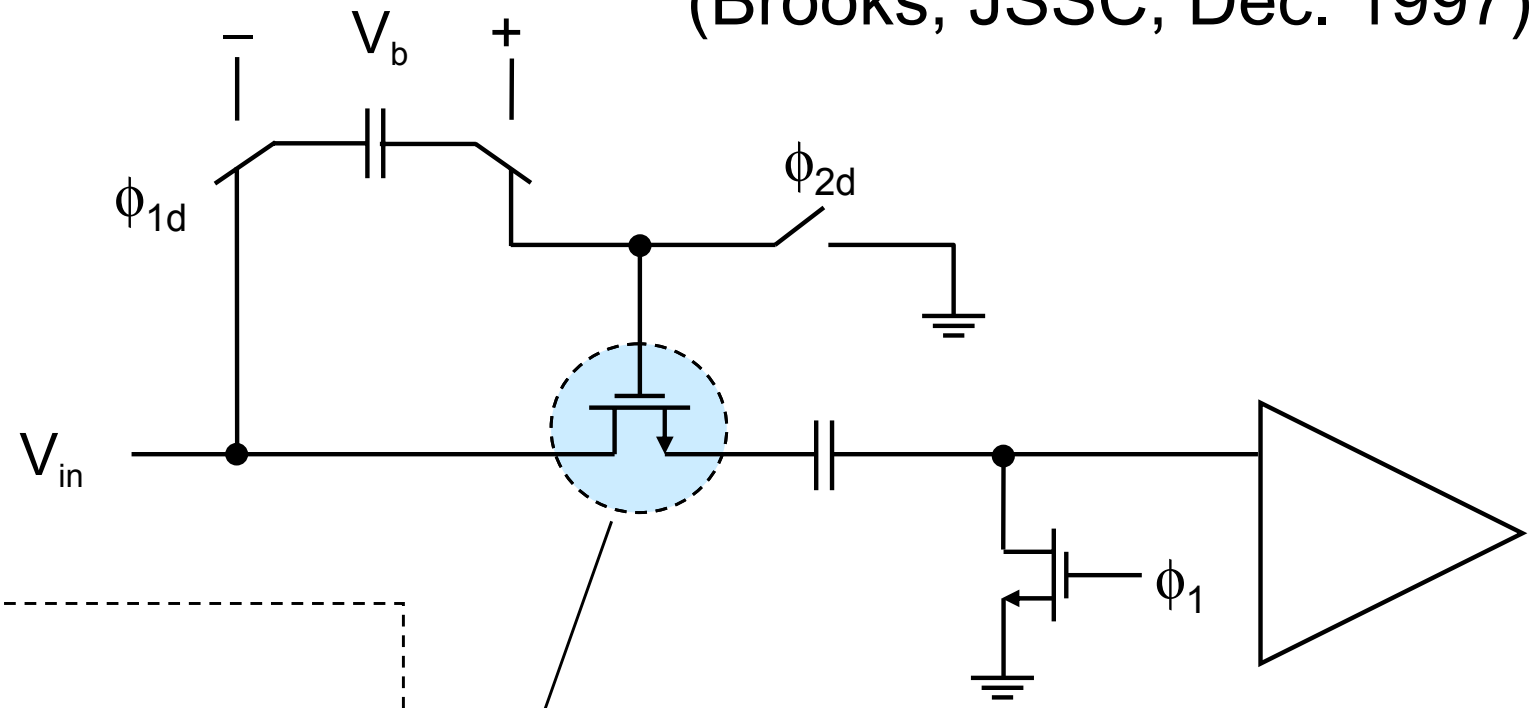


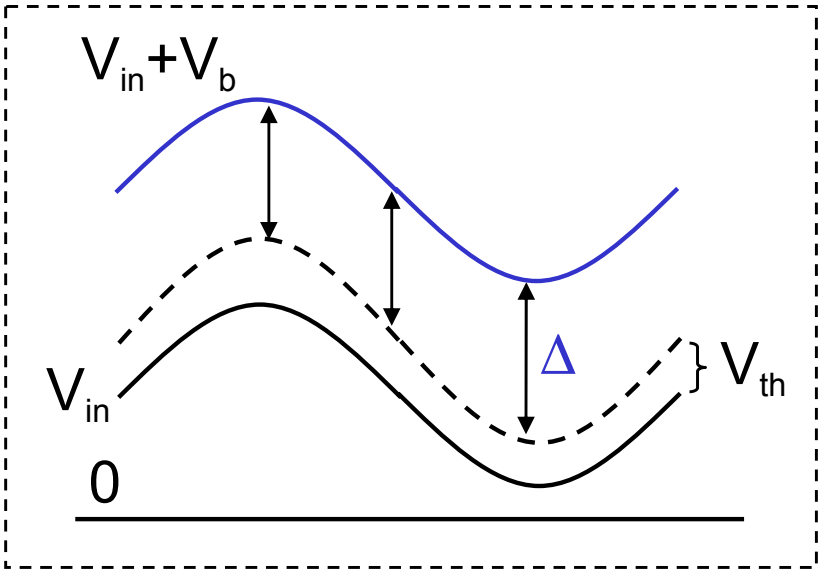
$$R_{on} = \frac{1}{\mu C_{ox}(W/L)\Delta}$$

- R_{on} is lower, but nonlinear.

Clock Boost for Constant R_{on}

(Brooks, JSSC, Dec. 1997)



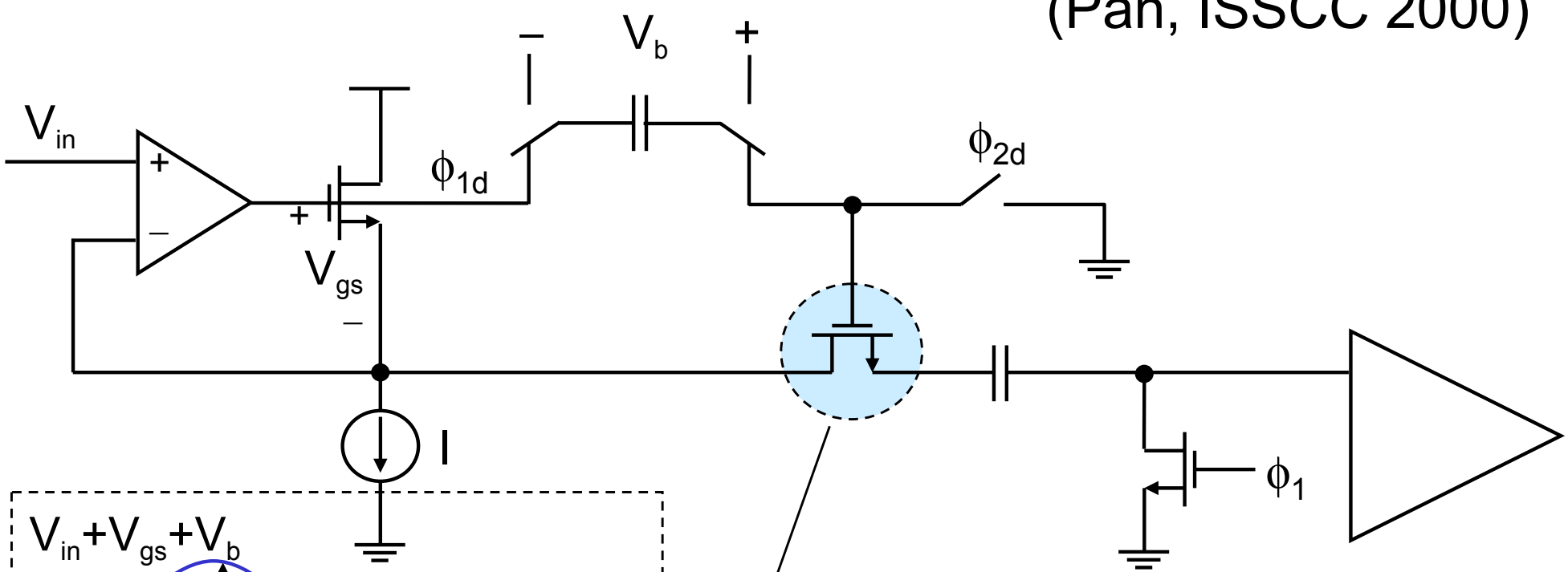


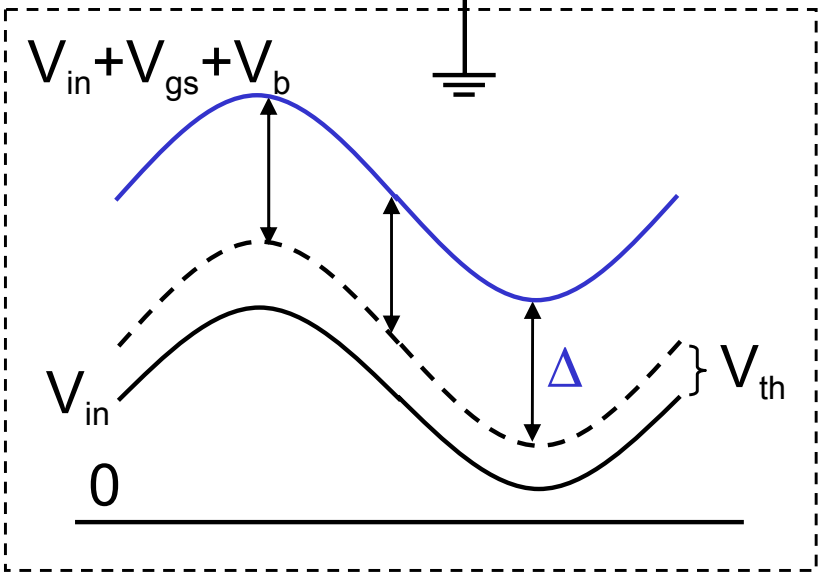
$$R_{on} = \frac{1}{\mu C_{ox}(W/L)\Delta}$$

- R_{on} is relatively constant, but V_{th} is nonlinear.

Clock Boost with Variable V_{th}

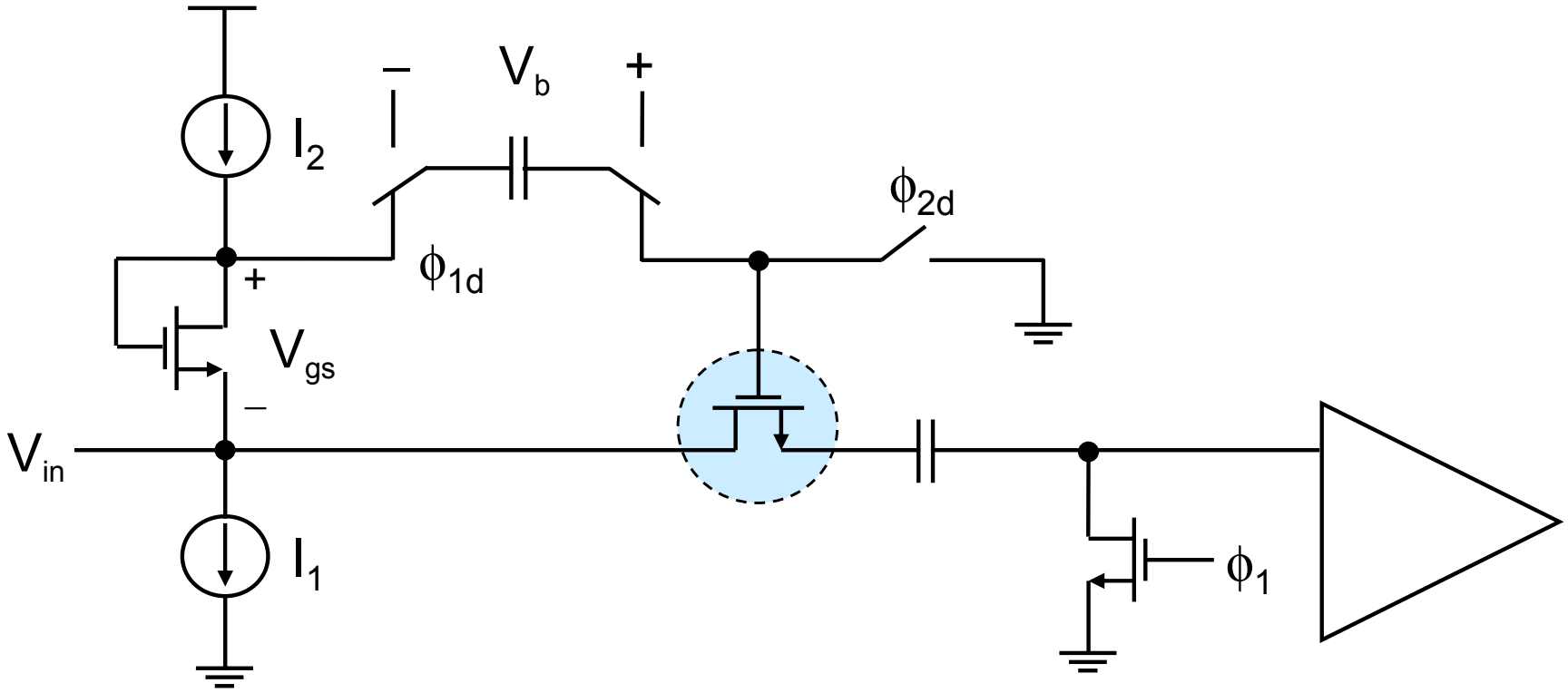
(Pan, ISSCC 2000)





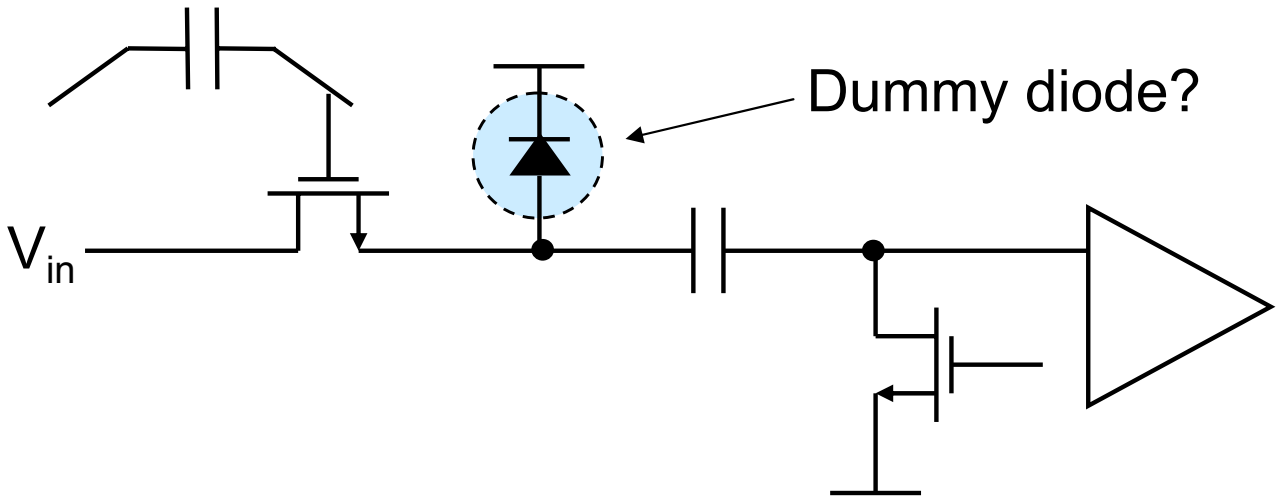
- R_{on} is constant, but opamp is slow.

Another Clock Boost with Variable V_{th}



- Diode provides a voltage drop of V_{gs}.
- V_{in} should be low-impedance source to drive $|I_1-I_2|$.

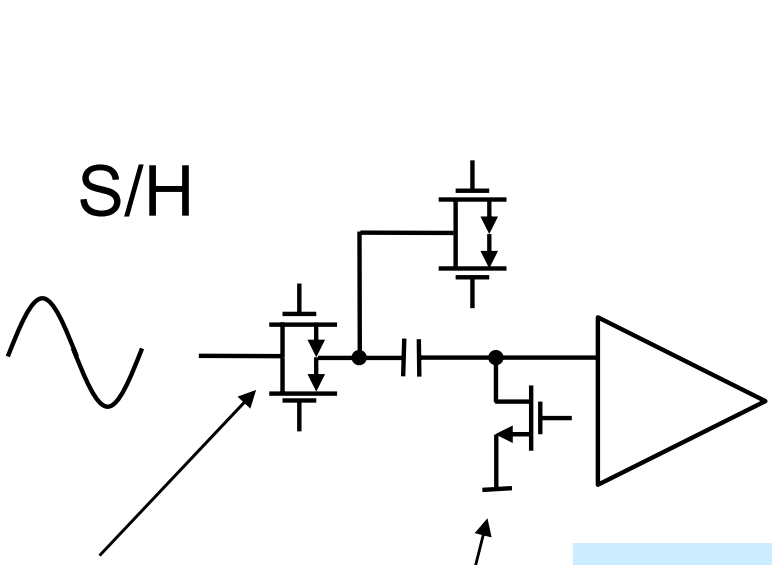
Considerations for Sampling

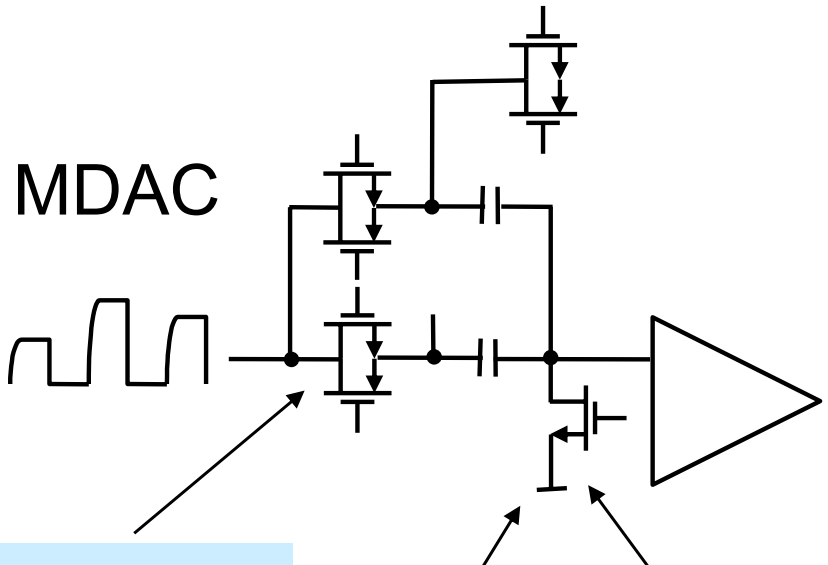


- kT/C and clock jitter
- >10% signal attenuation at Nyquist sampling if RC ~ $1/20f_s$.
- Finite CMRR: CMRR x ΔV_{cm}.
- Low opamp gain is acceptable if transfer function is linear.
- At HF, switches are large, and S/D junction capacitors are nonlinear.

  Dummy diode (?) may be effective to cancel nonlinearity.
- For reliability, limit V_{gs}, V_{gd}, and V_{ds} within V_{dd} (Abo, JSSC, May 1999).

Sampling in S/H and MDAC





R_{on} nonlinearity

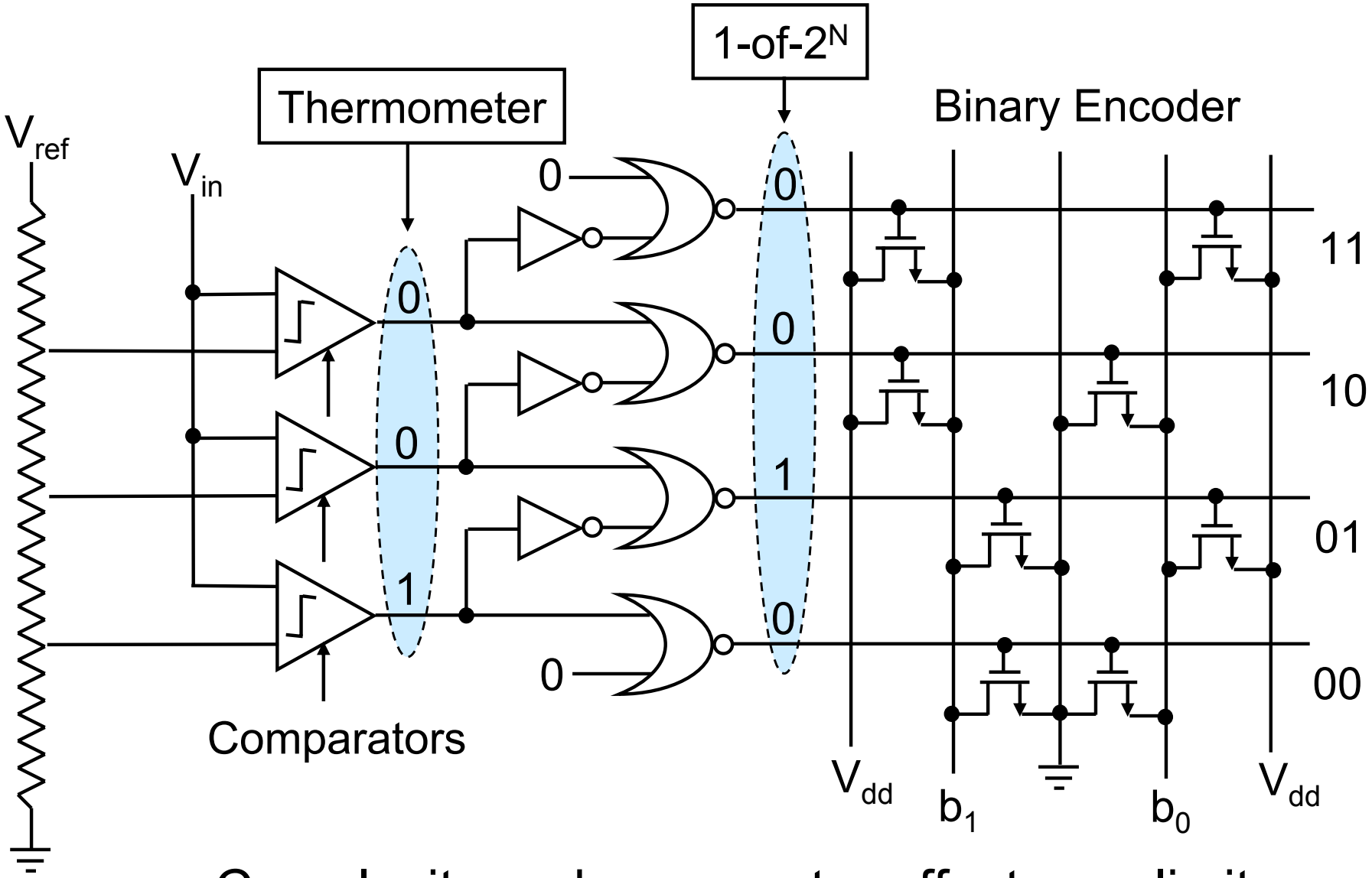
Gain and offset errors
(Ok if S/H is linear.)

No R_{on} nonlinearity

Offset error
(Ok if it is within digital correction range.)

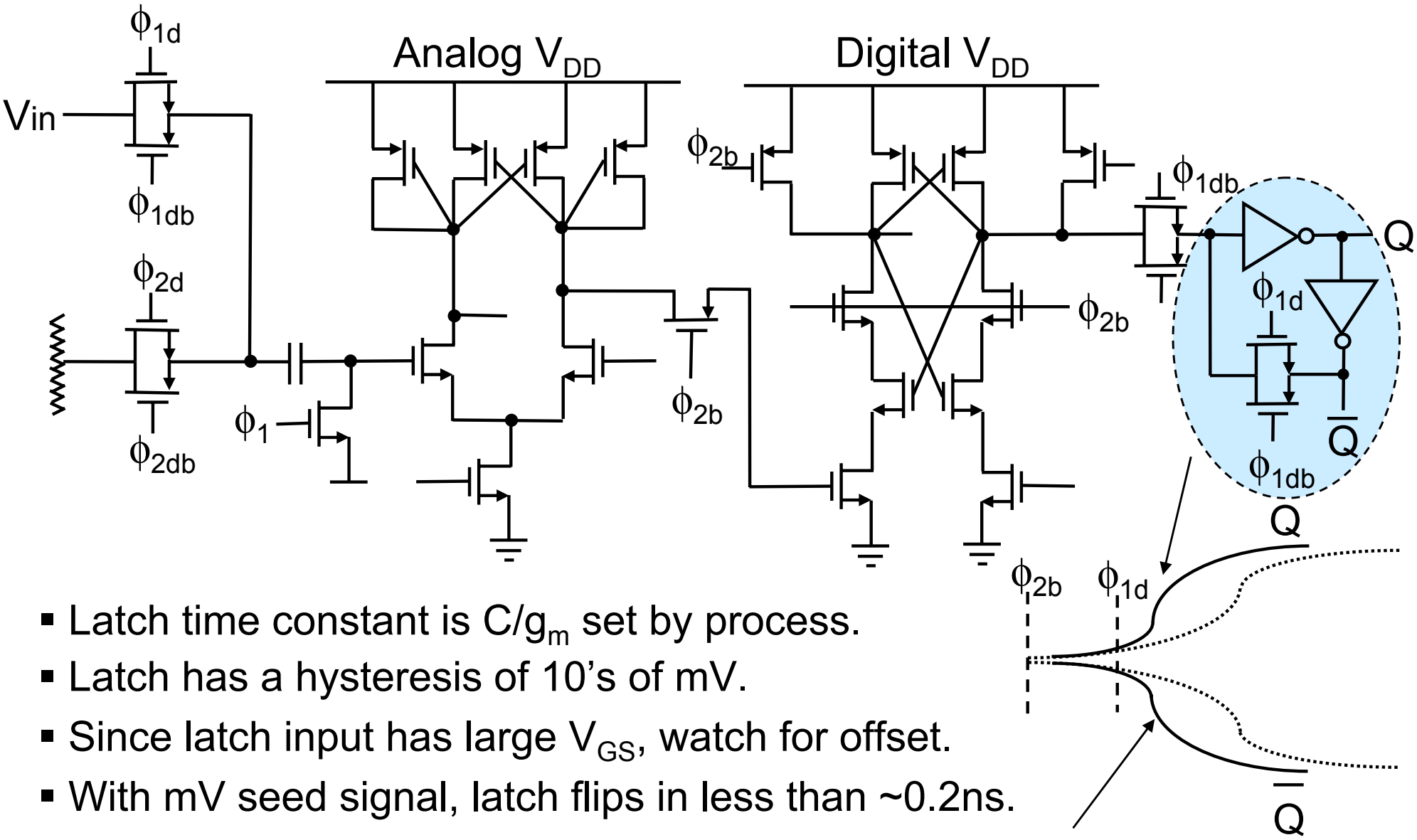
No gain error

Flash ADC for Sub-ADC (2b Case)



- Complexity and comparator offsets are limits.

Comparator with Double Latches

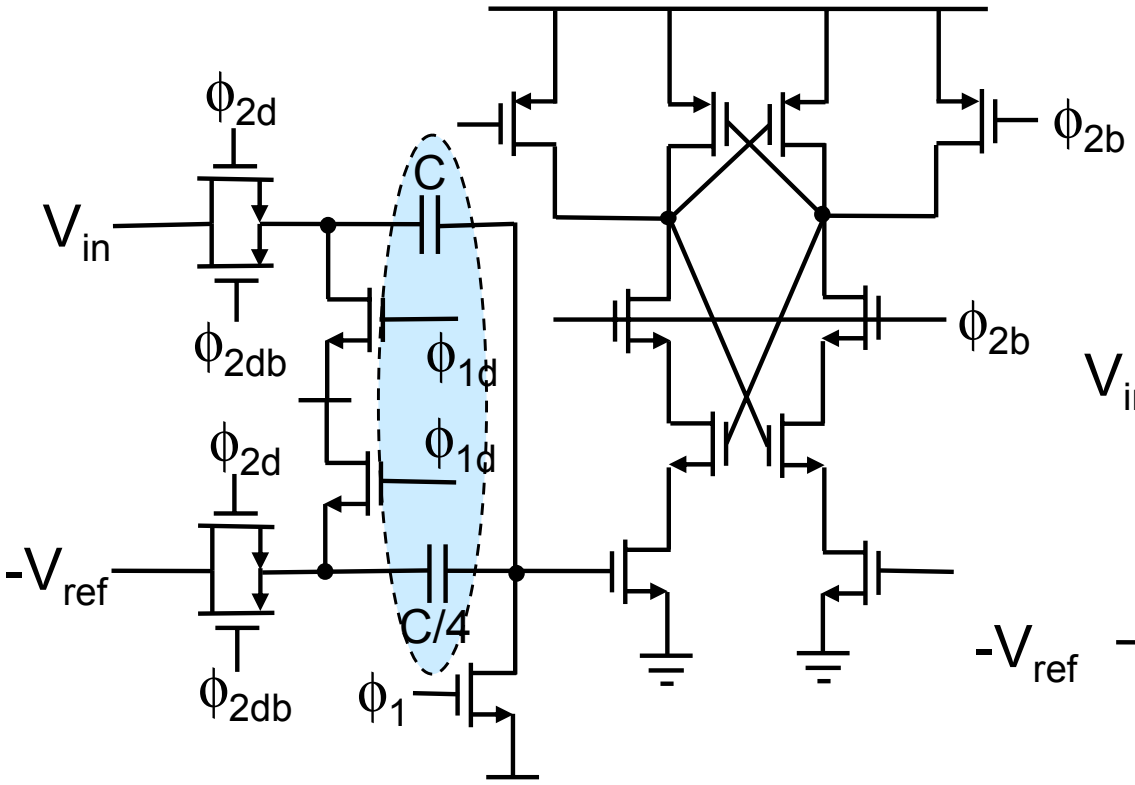


- Latch time constant is C/g_m set by process.
- Latch has a hysteresis of 10's of mV.
- Since latch input has large V_{GS}, watch for offset.
- With mV seed signal, latch flips in less than ~0.2ns.
- Additional digital latch is needed to avoid the meta-stable state.

Dynamic Comparator for 1.5b Case

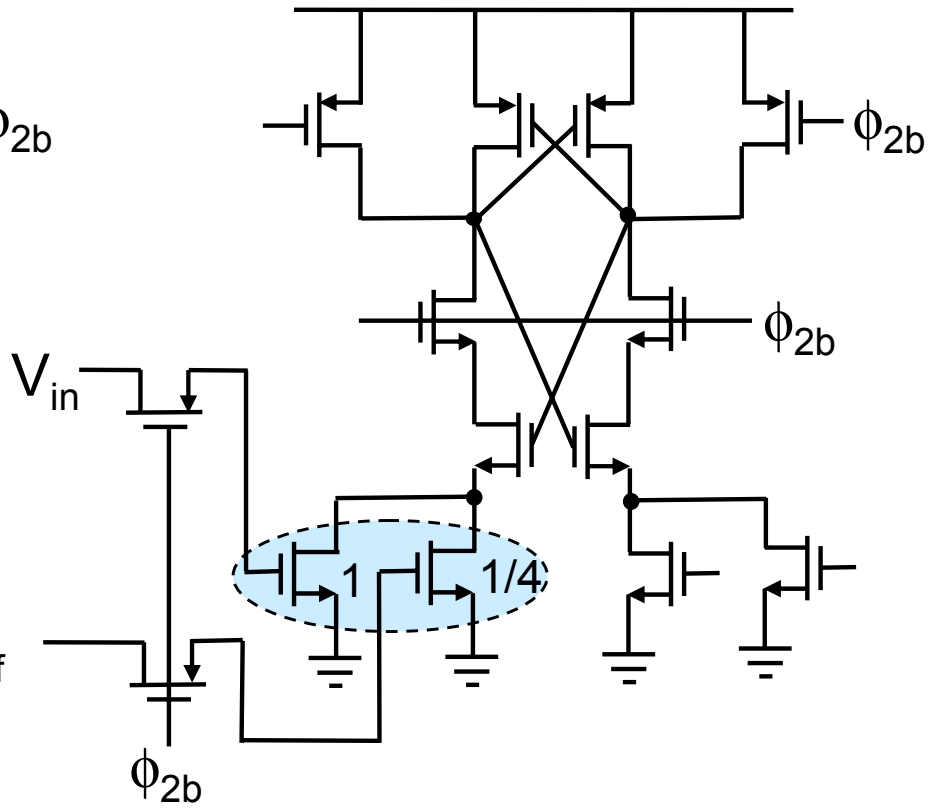
Capacitor Divider

(Song, JSSC, May 1995)



Current Divider

(Cho, JSSC, Mar. 1995)

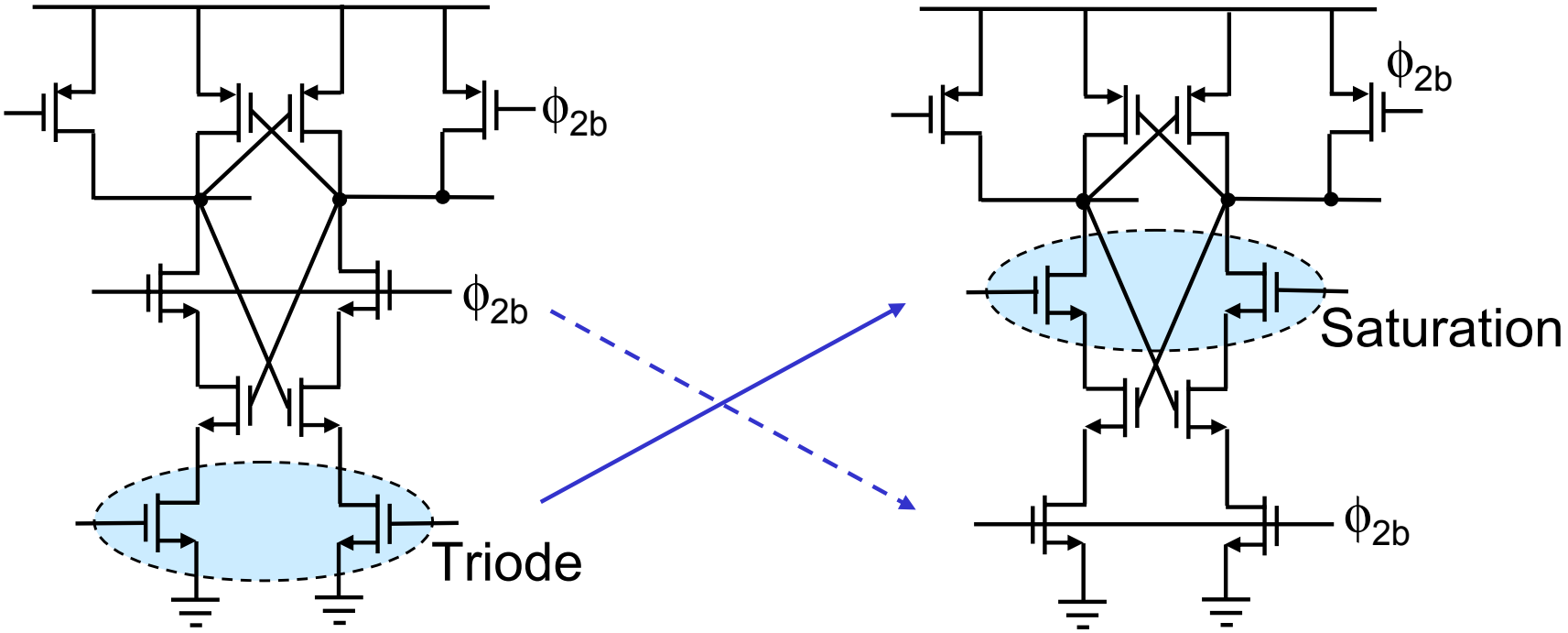


- For 1.5b comparator, no preamp is needed.
- No static power is consumed in dynamic latch.

Dynamic Latch Offset

Seed on Triode Input

Seed on Saturated Input

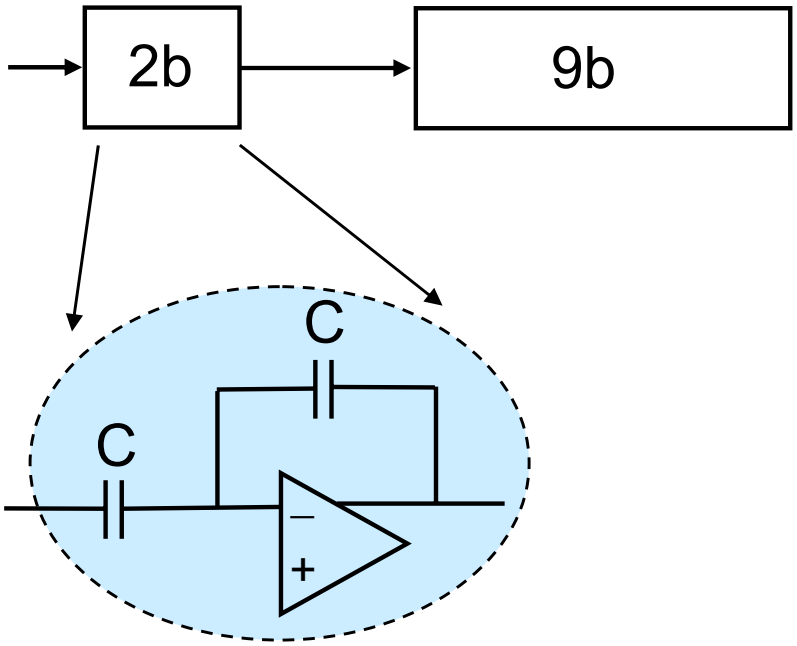


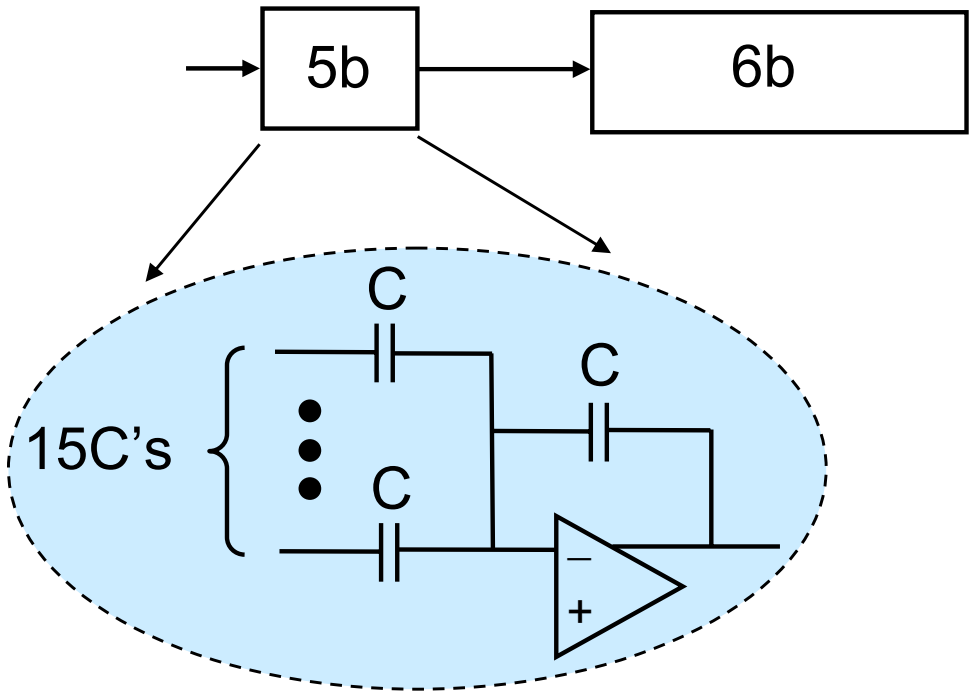
- Offset is large for triode input.
- By moving input pair to the middle, the input pair can be biased into saturation for lower offset.

Capacitor Matching Requirement

N bits/stage ⇨ Next stage can be (N-1) bits less accurate.

For example, to make 10b ADC;

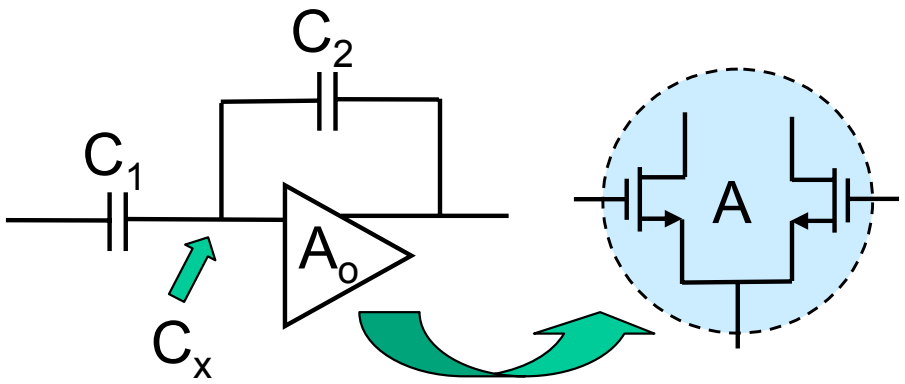




$$\sqrt{2} \times \frac{\Delta C}{C} < \frac{1}{2^9} \Rightarrow \frac{\Delta C}{C} < \frac{1}{\sqrt{2} \times 2^9}$$

$$\sqrt{16} \times \frac{\Delta C}{C} < \frac{1}{2^6} \Rightarrow \frac{\Delta C}{C} < \frac{1}{2^8}$$

Opamp Gain Requirement



$$\text{Loop Gain} = A_o f = A_o \times \frac{C_2}{C_1+C_2+C_x}$$

$$\text{Gain Error} = \frac{C_1+C_2+C_x}{C_2} \times \frac{1}{A_o}$$

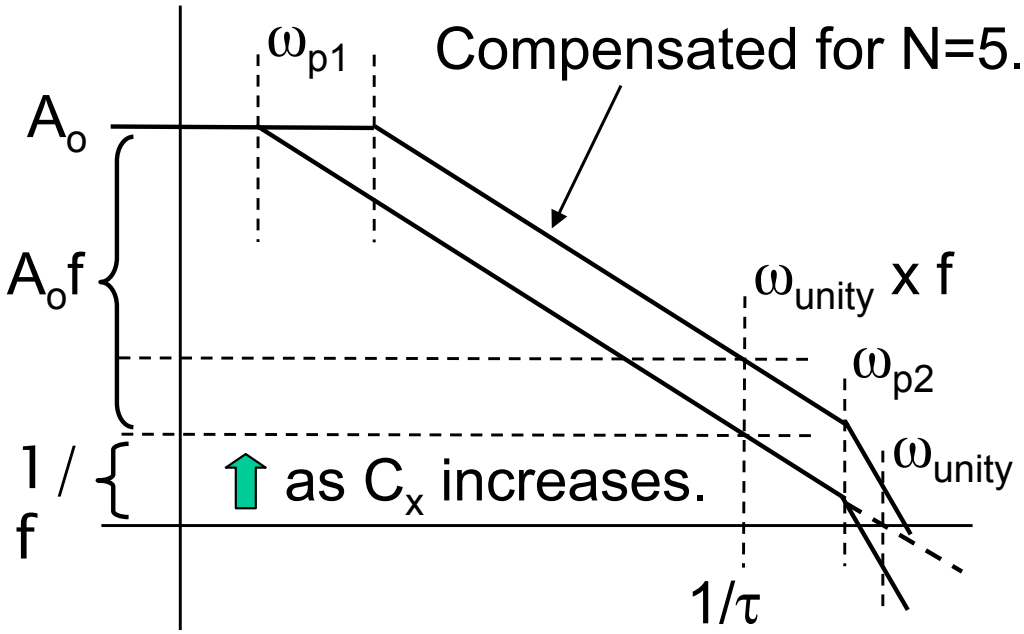
- $C_1 = 0$ in S/H.
- $C_x = C_p + C_{gs} + (1+A)\, C_{gd}$

$$\text{N=2:}\quad A_o > 2^9 \times \frac{C_1+C_2+C_x}{C_2} = 2^9 \left(2 + \frac{C_x}{C}\right) = 2^{10}\left(1 + \frac{C_x}{2C}\right)$$

$$\text{N=5:}\quad A_o > 2^6 \times \frac{C_1+C_2+C_x}{C_2} = 2^6 \left(16 + \frac{C_x}{C}\right) = 2^{10}\left(1 + \frac{C_x}{16C}\right)$$

➡ Gain requirement is less in the N=5 case.

Opamp Settling Requirement



$$f = \frac{C_2}{C_1+C_2+C_x}, \quad C_1 = 0 \text{ in S/H}$$

$$= \begin{cases} 1/(2 + \frac{C_x}{C}), \text{ if N=2.} \\ 1/(16 + \frac{C_x}{C}), \text{ if N=5.} \end{cases}$$

Compensated differently.

f factor of the N=2 case is more sensitive to the parasitics C_x.

Lower DC gain & Narrower BW.

$$A_o \text{ x } f > 2^{11-N},$$

$$e^{-T/2\tau} < \frac{1}{2^{11-N}},$$

$$\Phi_M = 90^o - \tan^{-1} \frac{\omega_{unity} \text{ x } f}{\omega_{p2}}$$
$$> 60^o.$$

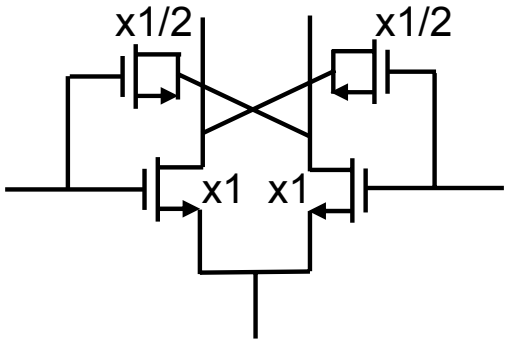
Then, settle with $\tau = \frac{1}{\omega_{unity} \text{ x } f}$

unless slew-limited.

How to Reduce Input Capacitance?

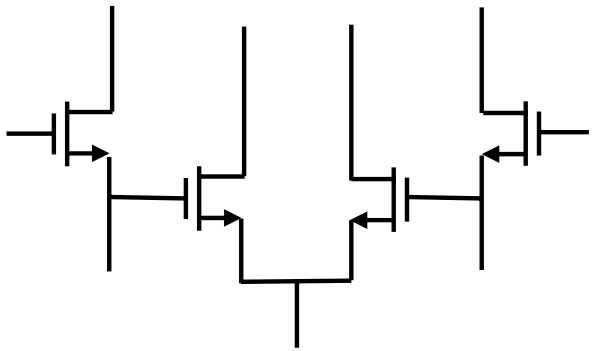
- High-speed design demands smaller sampling capacitance and larger input device for wider BW and faster settling.

Negative Cap.



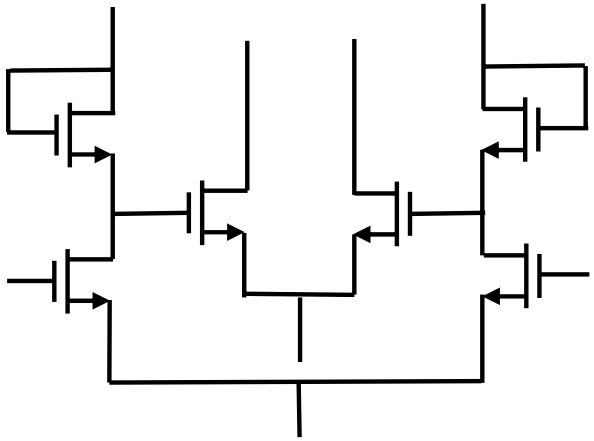
Normally-off 1/2 size dev. cancels input C_{gd} Miller cap.

Source Follower



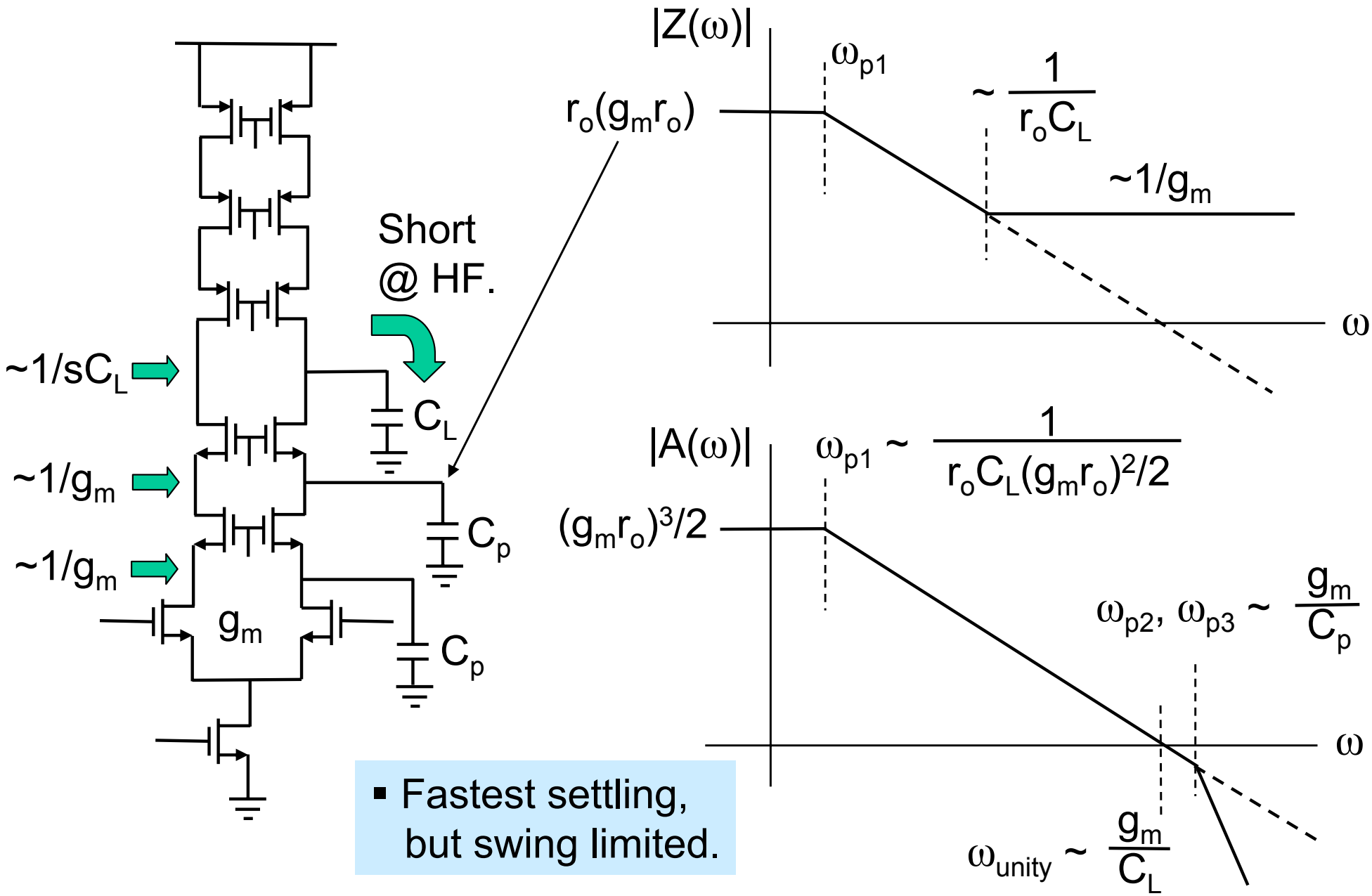
Input cap. is driven by low imp. ($1/g_m$) of the source follower.

Gain Stage



Low gain but wide BW amp makes up gain loss.

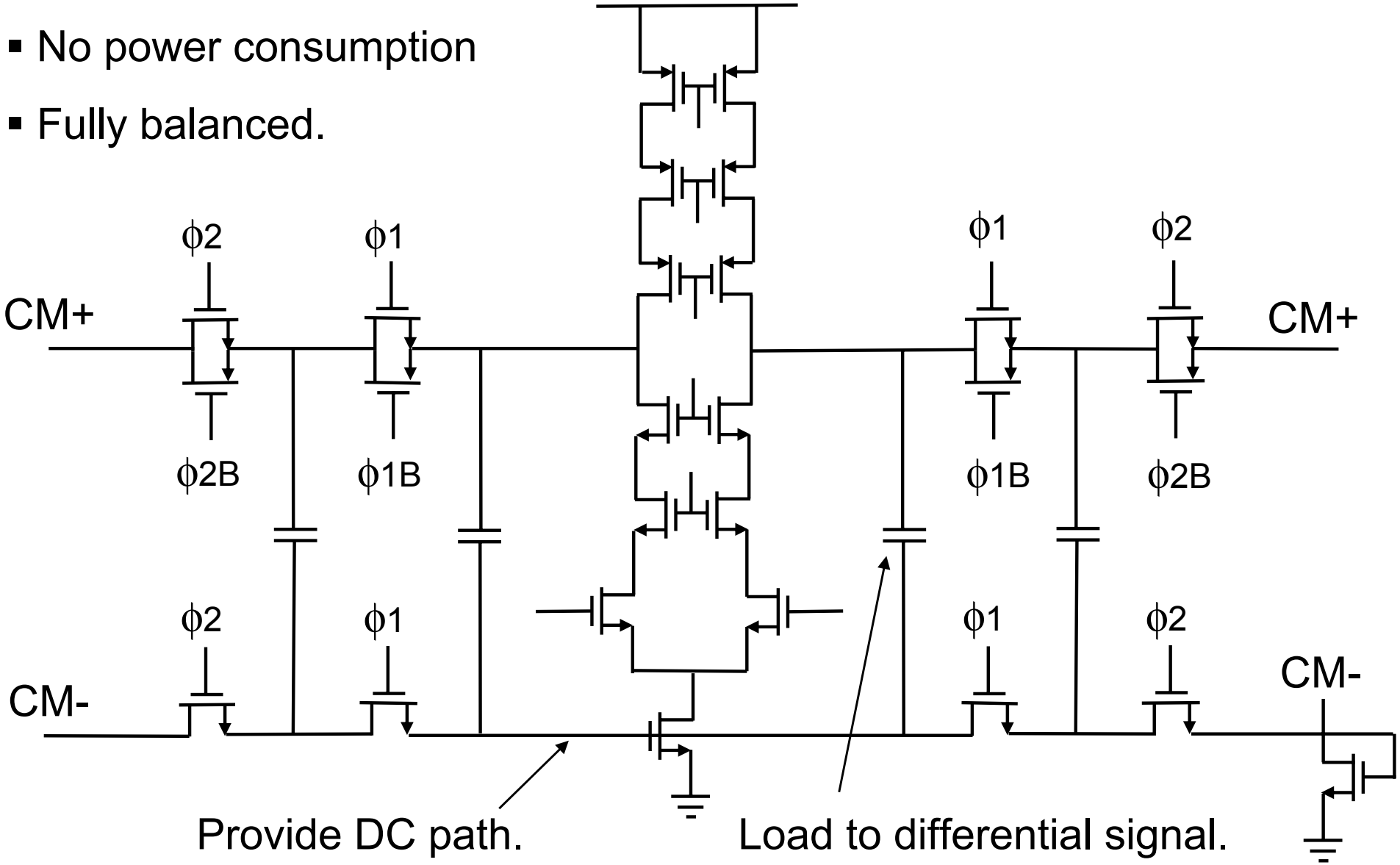
Triple-Cascode Opamp



- Fastest settling, but swing limited.

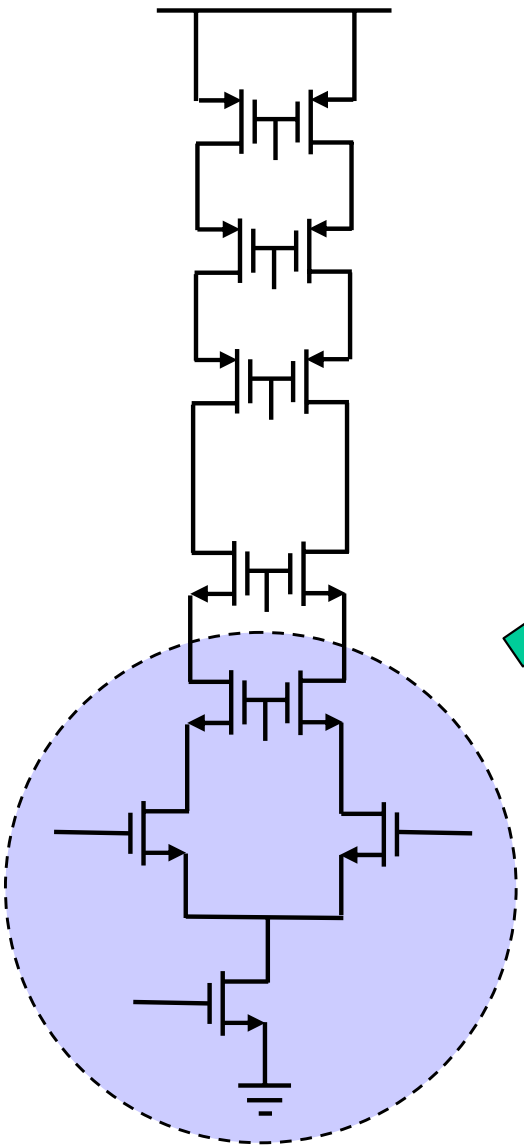
Capacitive CM Feedback

- No power consumption
- Fully balanced.

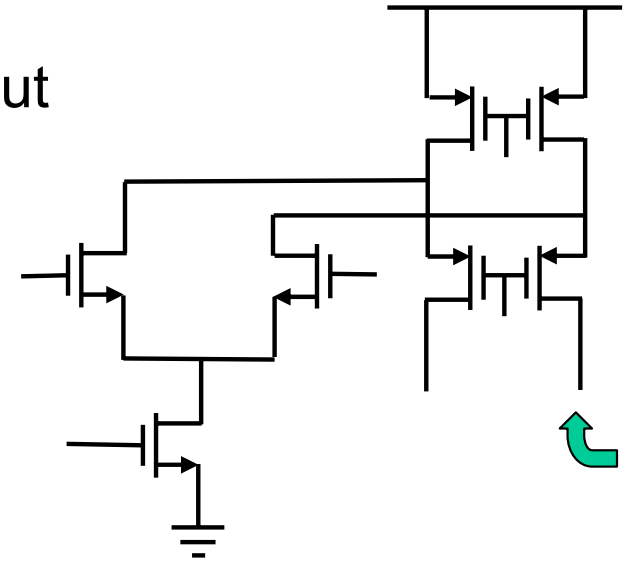


Folded-Cascode Opamp

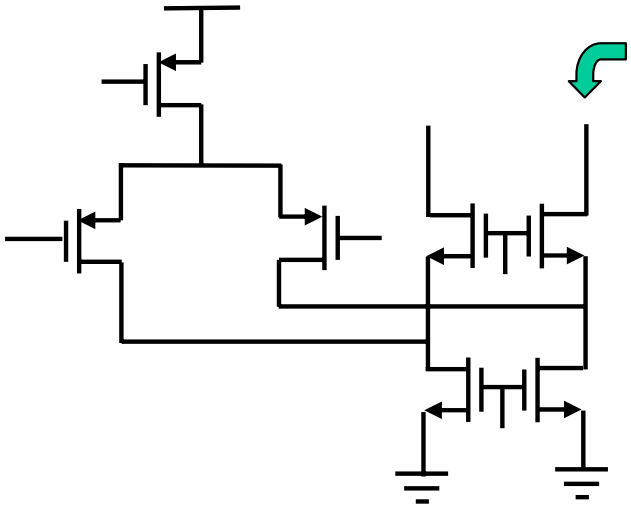
- Centered CM input voltage, but slightly lower gain.
- Also more parasitic at 1st cascode node.



NMOS Input

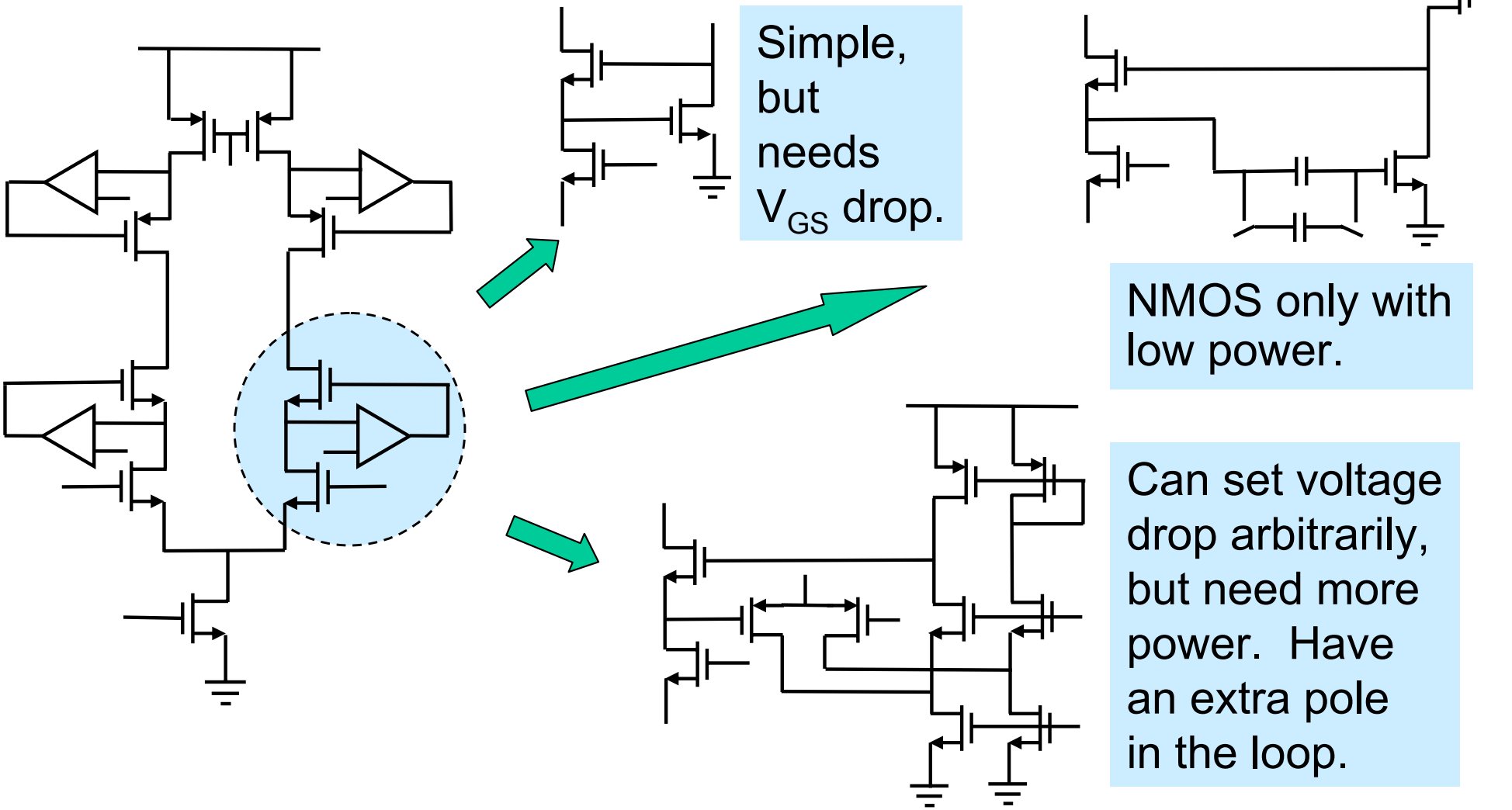


PMOS Input

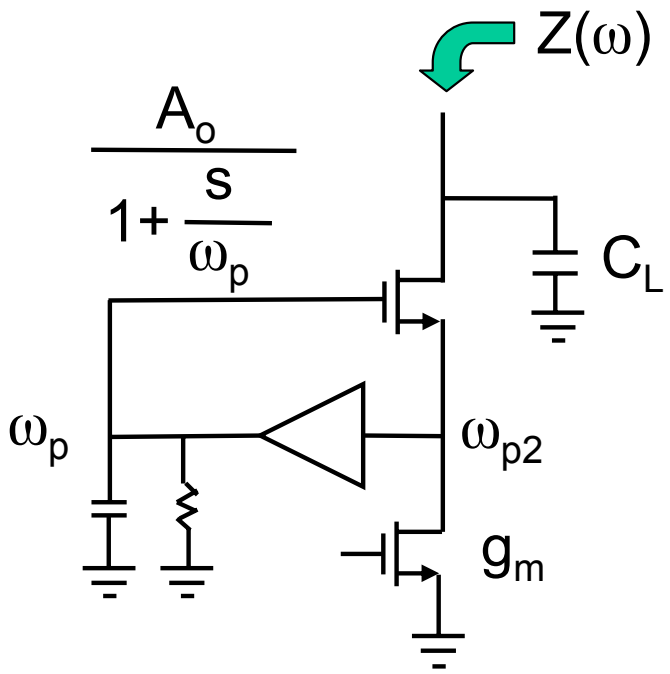


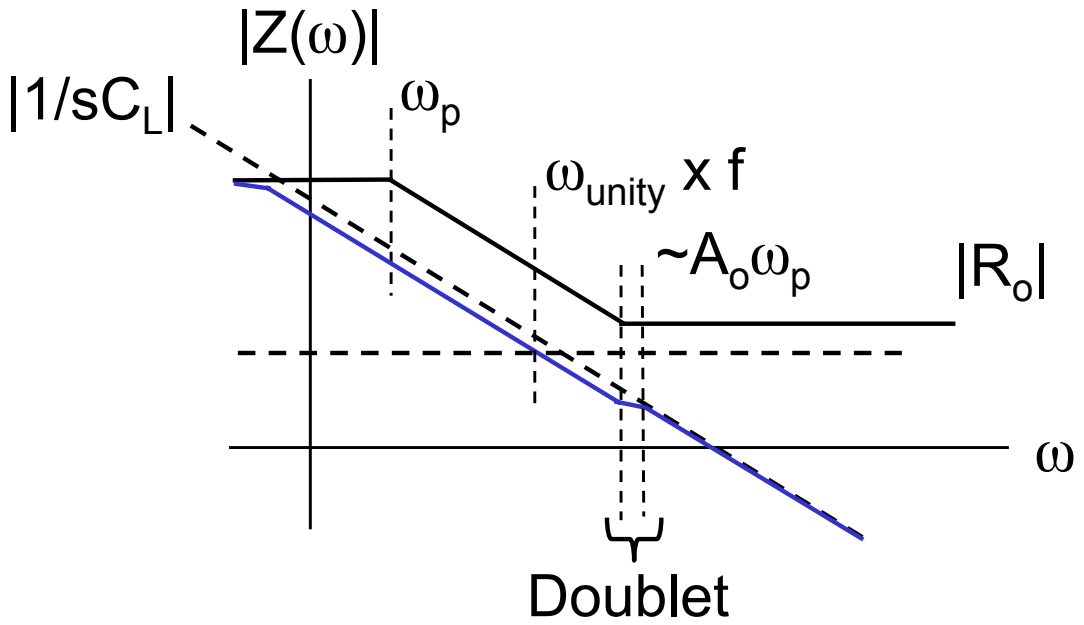
Gain-Boosted Cascode Opamp

- Cascode opamp settles fast, but has low gain.
  (Hosticka, JSSC, Dec. 1979, Bult, JSSC, Dec. 1990)



Gain-Boosted Opamp Stability



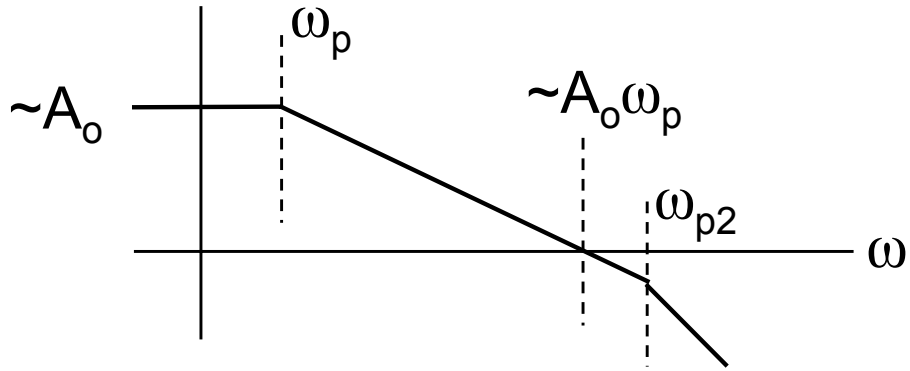


Doublet (pole-zero pair) slows down settling.

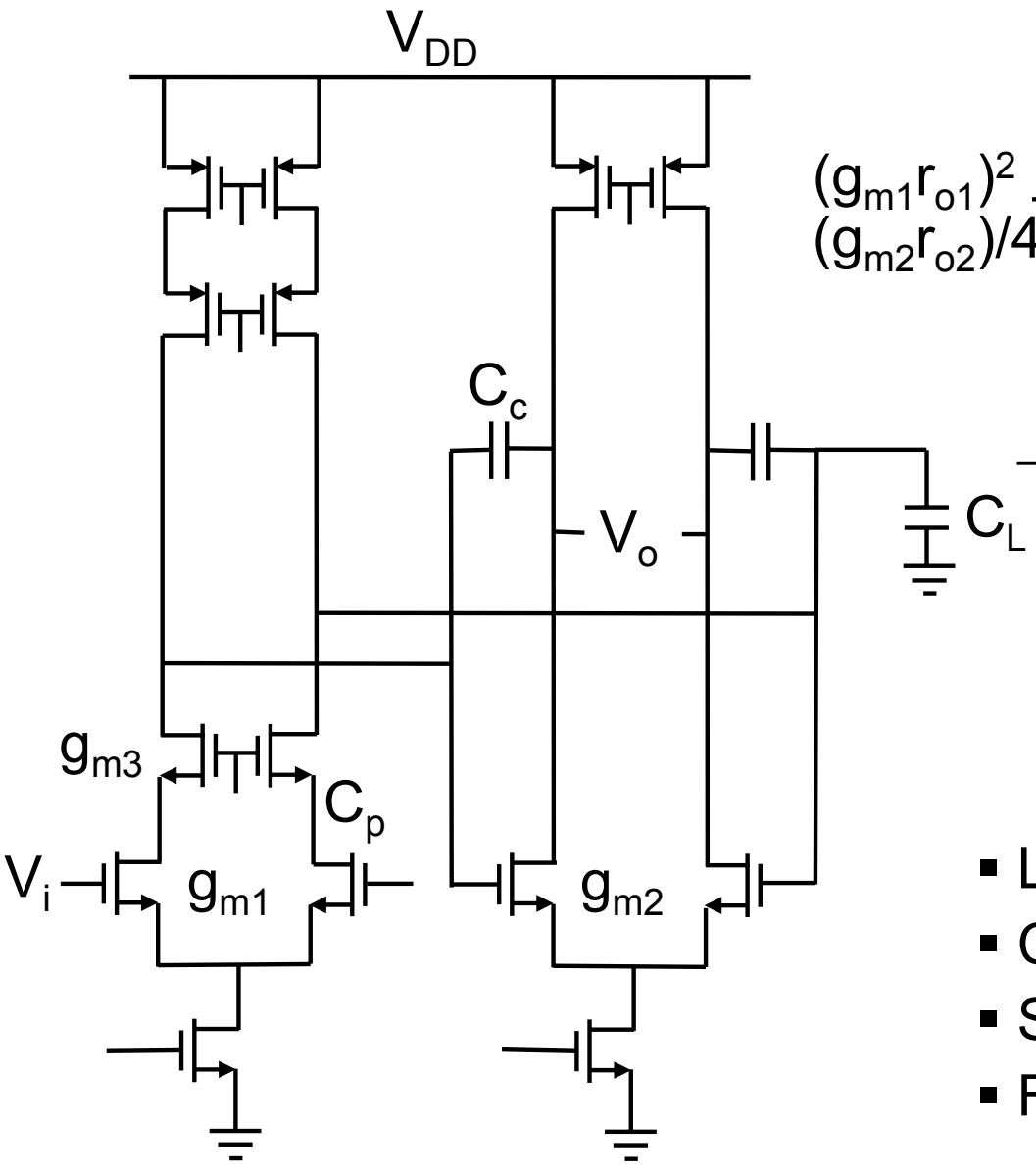
➡ $\omega_{unity} \times f < A_o\omega_p$

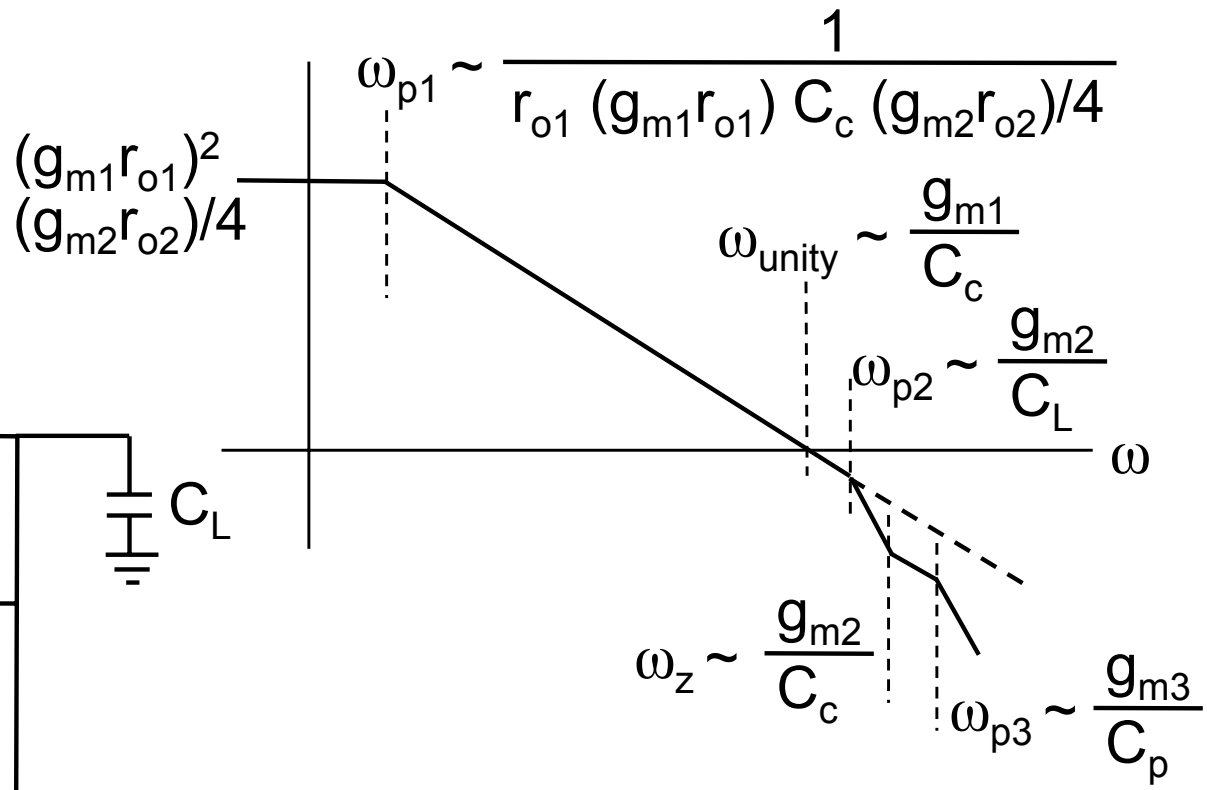
If non-dominant pole, ω_{p2}, is lower than the boost-loop unity-gain frequency, $\Phi_M < 45^o$.

➡ $A_o\omega_p < \omega_{p2}$



Two-Stage Opamp





- Larger signal swing than cascode.
- Cascode boosting can be used.
- Second pole is at g_{m2}/C_L.
- Right-half-plane zero at g_{m2}/C_c.

Design Considerations

N	2	3	4	5	6
Capacitor Matching			→	Less Accurate	
Opamp Gain			→	Low Gain	
Opamp Bandwidth			→	Narrow Bandwidth	
Comparator Resolution	Low Resolution		←		
Complexity	Less Complex		←		

Conclusions

- Minimize delay in the clock path for low jitter, and linearize bottom-plate switch for sampling.
- Optimize number of bits per stage to reduce capacitance matching and opamp gain requirement.
- Watch opamp gain, nonlinearity, input capacitance, and doublet effect in settling.
- Use tri-level thermometer-array capacitor MDAC, and shift comparator threshold by a half bit for minimum hardware.
- For higher resolution, use digital calibration.