

# Large Swing CMOS Power Amplifier

KEVIN E. BREHMER, MEMBER, IEEE, AND JAMES B. WIESER

**Abstract**—A CMOS class *AB* power amplifier is presented wherein supply-to-supply voltage swings across low impedance loads are efficiently and readily handled. The amplifier consists of a high gain input stage and a push-pull unity gain amplifier output stage. The amplifier dissipates only 7 mW of dc power and delivers 36 mW of ac power to a 300  $\Omega$  load, using standard power supplies of  $\pm 5.0$  V. Lower impedance loads can be driven to higher power levels, providing the internal current limiting level is not exceeded.

## I. INTRODUCTION

**D**URING the past few years, CMOS has emerged as an industry standard because of its low power dissipation. However, the implementation of analog functions in MOS has presented a challenge to many circuit designers. One area of MOS analog design where considerable work is taking place is the design of an efficient, large dynamic range power amplifier [1], [2].

Prior art MOS power amplifiers used output stage configurations that were subject to various limitations. Such limitations included the size of the output driver devices and the control of the dc bias current in these output drivers. In order to control the dc bias current in the output driver devices, previous designs used a source follower device and a controlled current sink as an output stage [1], [2]. This type of design has dynamic range limitations and requires large output driver device sizes. By replacing the source follower output driver with a bipolar emitter follower, transistor die area and dynamic range limitations can be reduced considerably. However, instabilities arise when using a bipolar emitter follower to drive high capacitive loads, thus limiting its application. Also, bipolar transistors are parasitic devices in a standard CMOS process which are not necessarily well controlled.

In order to obtain an efficient power amplifier with a large dynamic range capable of driving a low impedance load, a push-pull class *AB*, fully CMOS power amplifier is presented. This amplifier is designed to operate at voice-band frequencies for telecommunication and audio applications, and to be used in an inverting configuration so that users can design gain or attenuation into their systems.

## II. DESCRIPTION OF THE POWER AMPLIFIER

The complete power amplifier consists of a high gain input stage driving a unity gain push-pull output stage. The input stage is comprised of a differential amplifier and a common source amplifier. Compensation of this stage is achieved by a Miller multiplied feedback capacitor.

The output stage includes two unity gain amplifiers in push-pull configuration. Each amplifier contains a differential input stage whose output controls the gate of the output driver device. The drain of the output driver device is directly fed back to the noninverting input of the differential stage to form a noninverting unity gain amplifier, and one half of the push-pull configuration.

In the event of an offset between the two push-pull amplifiers, a feedback circuit controls the dc bias current in the output drivers. Fig. 1 shows a pseudo block diagram form of the power amplifier and the associated feedback circuitry required to stabilize the dc bias current in the output driver devices.

### A. Output Stage Analysis

From Fig. 1 we can see that amplifier *A1* and transistor *M6* form the unity gain amplifier for the positive half of the output voltage swing, and conversely amplifier *A2* and transistor *M6A* form the negative half cycle circuit. For the sake of simplicity, only the circuit referring to the positive half output swing of the output stage will be discussed. The operation of the negative half circuit is an inverted mirror image of that of the positive half swing circuit. Components performing similar functions in each circuit are designated with an additional letter "A" for the negative half circuit.

Shown in Fig. 2 is a detailed schematic of the positive unity gain amplifier. The differential amplifier input stage of the unity gain amplifier has a large positive common mode range (CMR), which allows transistor *M6* to source large amounts of current to the load, while still being of a reasonable physical size for incorporation into a monolithic circuit. Large current sourcing is provided by producing the highest possible gate drive on *M6*. The maximum gate-to-source voltage *M6* can have while still keeping *M1* and *M2* in the saturation region is given by

$$V_{GS6_{\max}} = -(V_{CC} - (V_{IN} - V_{GS1} + V_{DSAT1})) \quad (1)$$

Manuscript received July 11, 1983; revised July 26, 1983.

The authors are with the Telecom Group, National Semiconductor, Santa Clara, CA 95051.

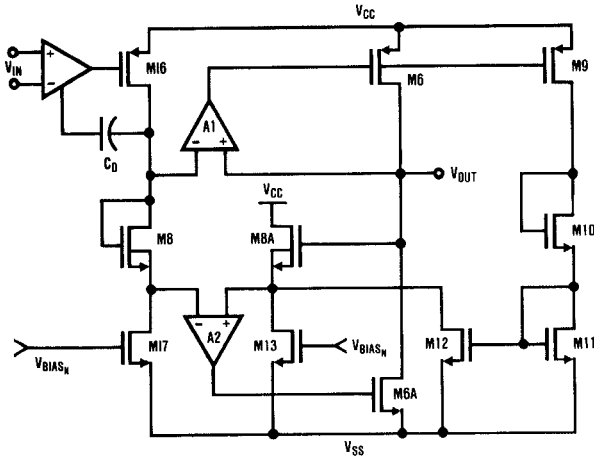


Fig. 1. Block diagram of power amplifier.

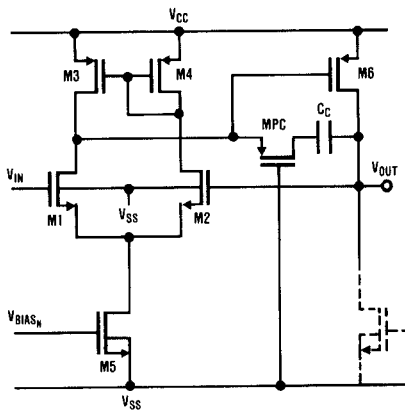


Fig. 2. Positive output stage unity gain amplifier.

It first appears that increasing  $V_{GS1}$  by increasing the overdrive voltage of  $M1$  and  $M2$  will increase the gate drive of  $M6$ . However, after substitution of the saturation equation (2) into the expression for  $V_{GS6max}$ , we see that this is not the case:

$$V_{DSAT} = V_{GS} - V_T \quad (2)$$

$$V_{GS6max} = -(V_{CC} - V_{IN} + V_{T1}). \quad (3)$$

From (3), maximum gate drive on  $M6$  is provided by increasing the threshold voltage (4) of  $M1$  and  $M2$ . One method of increasing the threshold voltage of  $M1$  and  $M2$  is to modify  $V_{T0}$  by a threshold implant. Implanting devices  $M1$  and  $M2$  to produce a higher  $V_{T0}$  pushes the common source voltage lower, allowing the gate of  $M6$  to drop more while still keeping  $M1$  and  $M2$  in saturation.

$$V_T = V_{T0} + \gamma \sqrt{V_{BS} - 2\phi_F}. \quad (4)$$

Further enhancement of the positive CMR is obtained by connecting the substrate of transistors  $M1$  and  $M2$  to

$V_{SS}$ , thereby modulating the source-substrate voltage of these transistors. The effect of this substrate modulation on the threshold voltage of  $M1$  and  $M2$  can be seen in (4). As the output swing increases, the common source voltage also increases, however, not by the same amount, since the threshold voltage of  $M1$  and  $M2$  has increased due to substrate modulation. The increased threshold voltage of  $M1$  and  $M2$  tends to reduce the common source mode voltage of the differential pair thus driving the gate of  $M6$  more negative while still keeping  $M1$  and  $M2$  in saturation.

The current in the output driver device  $M6$  is typically controlled by the current mirror developed in the differential amplifier of the positive unity gain amplifier and matches the current set in the negative output driver device  $M6A$  by the negative unity gain amplifier. If an offset occurs between amplifiers  $A1$  and  $A2$ , the current balance between output drivers  $M6$  and  $M6A$  no longer exists and either massive amounts of current or no current at all will flow through these devices. The feedback loop, shown in Fig. 1, consisting of transistors  $M8A$ – $M13$ , stabilizes the current through output drivers  $M6$  and  $M6A$  in the event of an offset between amplifiers  $A1$  and  $A2$ . The feedback loop operates as follows. Assume that amplifier  $A1$  has an offset such that transistor  $M6$  begins to source excessive amounts of current. The excessive current is sensed by transistor  $M9$  and is fed back to the source follower  $M8A$ – $M13$ . The increase of current provided to transistor  $M8A$  produces a greater voltage drop across the source follower  $M8A$ – $M13$  and more differential signal on the input of amplifier  $A2$ . The larger differential signal on amplifier  $A2$  results in lower gate drive on output driver  $M6A$ , thereby reducing the current in the output drivers  $M6$ – $M6A$ . The output voltage now has increased due to the fact that the positive swing amplifier  $A1$  attempts to keep both of its inputs at the same potential. The complete power amplifier is in a feedback loop, wherein amplifier feedback drops the voltage of the negative input of amplifier  $A1$  in attempting to keep the output of the complete power amplifier at 0 V in the dc bias condition. Transistor  $M8$  transfers this voltage drop to the negative input of amplifier  $A2$ , thus balancing offset of amplifier  $A2$ . The offset that was initially introduced by amplifier  $A1$  is absorbed by the source follower transistor  $M8A$ .

Because the output stage current feedback is not unity gain, some current variation in transistors  $M6$  and  $M6A$  occurs. Offsets between amplifiers  $A1$  and  $A2$  can produce a 2:1 variation in dc current over temperature and process variations. Equation (5) predicts the change in the output driver current assuming that  $V_{out}$  is at ground, and any offset between amplifiers  $A1$  and  $A2$  can be reflected as a difference between the inputs of amplifier  $A1$ . From this equation,  $V_{off1}$  must be zero for  $\Delta I_0$  to be zero.

$$\Delta I_0 = -gm_{6A}A_2 \left[ V_{off1} - \sqrt{\frac{2\beta_9\beta_{12}}{\beta_{8A}\beta_6\beta_{11}}} \left[ \sqrt{I_{B1} \left( \frac{\beta_6\beta_{11}}{\beta_9\beta_{12}} + \frac{1}{2} \frac{\beta_5\beta_6}{\beta_7\beta_3} \right) + \Delta I_0} - \sqrt{I_{B1} \left( \frac{\beta_6\beta_{11}}{\beta_9\beta_{12}} + \frac{1}{2} \frac{\beta_5\beta_6}{\beta_7\beta_3} \right)} \right] \right] \quad (5)$$

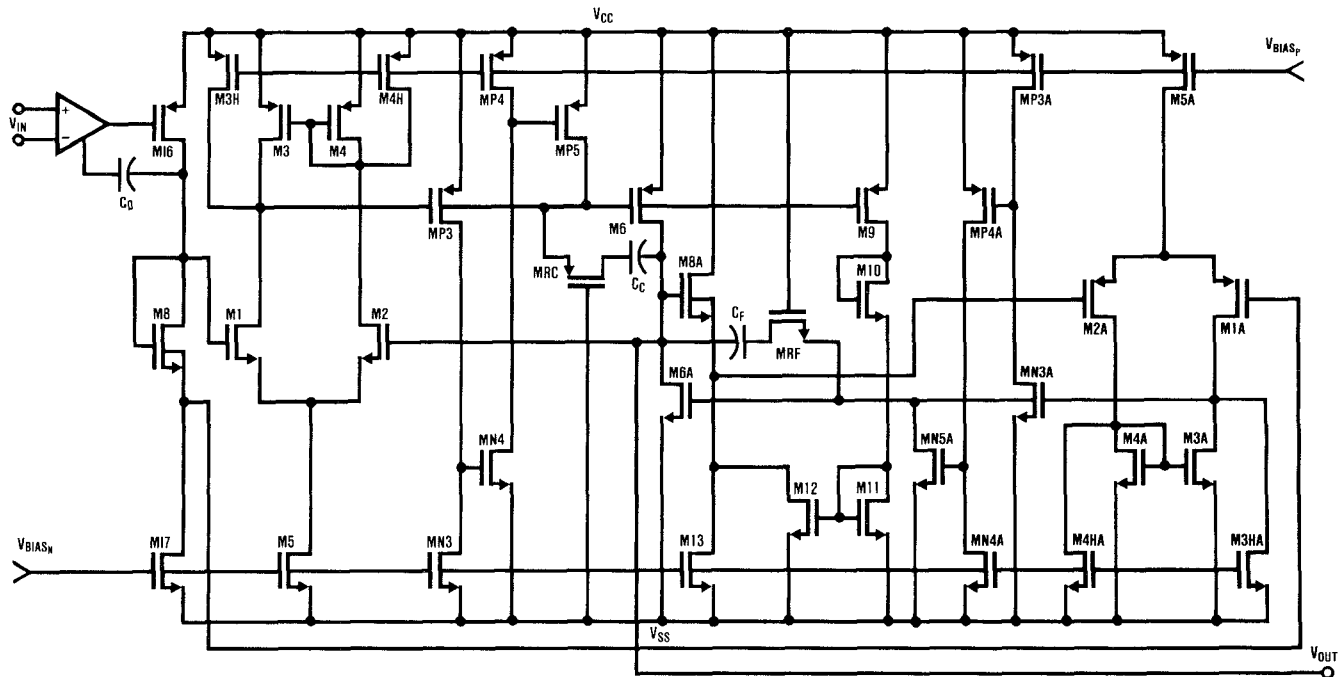


Fig. 3. Complete power amplifier schematic.

where

$$\beta = \frac{\mu_{\text{eff}} C_{\text{ox}}}{2} \left( \frac{W}{L} \right)_{\text{eff}} \text{ and } I_{B1} = I_{M17}.$$

Since transistor  $M6$  can supply large amounts of current, care must be taken to ensure that this transistor is off during the negative half cycle of the output voltage swing. For large negative swings, the drain of transistor  $M5$  pulls to  $V_{SS}$ , turning off the current source that biases the differential amplifier  $A1$ . As the bias is turned off, the gate of transistor  $M6$  floats and tends to pull towards  $V_{SS}$ , turning on transistor  $M6$ .

Shown in Fig. 3 is circuitry which ensures that transistor  $M6$  remains off for large negative voltage swings. As transistor  $M5$  turns off, transistors  $M3H$  and  $M4H$  pull up the drains of transistors  $M3$  and  $M4$ , respectively. As a result, transistor  $M6$  is turned off and any floating nodes in the differential amplifier are eliminated. Positive swing protection is provided for the negative half cycle circuit by transistors  $M3HA$  and  $M4HA$ , which operate in a manner similar to that described above for the negative swing protection circuit. The swing protection circuit does, however, degrade the step response of the power amplifier since the unity gain amplifier not in operation is completely turned off.

Short circuit protection is also included in the design of the amplifier. From Fig. 3, we can see that transistor  $MP3$  senses the output current through transistor  $M6$ , and in the event of excessively large output currents, the biased inverter formed by transistors  $MP3$  and  $MN3$  trips, thus enabling transistor  $MP5$ . Once transistor  $MP5$  is enabled, the gate of transistor  $M6$  is pulled up towards the positive

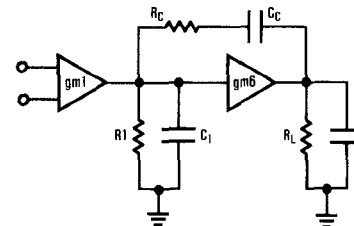


Fig. 4. RC compensation for the output stage unity gain amplifier.

supply  $V_{CC}$ , thus limiting the current transistor  $M6$  source to approximately 60 mA.

### B. AC Compensation of the Power Amplifier

AC stability of the complete power amplifier is achieved by providing a wide-band output stage and by using compensation at the input stage to produce the dominant pole. The dominant pole in the input stage is produced by the Miller multiplied capacitor  $C_D$ . The compensation of each unity gain amplifier in the output stage is achieved by a Miller multiplied capacitor and feedforward resistor. From Figs. 2 and 3, we can see that transistor  $MRC$  and capacitor  $C_C$  comprise the  $RC$  network for the positive unity gain amplifier and transistor  $MRF$  and  $C_F$  comprise the  $RC$  network for the negative unity gain amplifier. To simplify the calculation of the open loop transfer function of Fig. 2, a model as shown in Fig. 4 has been developed [1]. In this figure, the effective output impedance of the first stage is represented by resistor  $R_1$  and capacitor  $C_1$ , while the effective output impedance of the second stage is represented by resistor  $R_L$  and capacitor  $C_L$ . From this model, it can be shown that the poles and zero of each unity gain amplifier before closing the feedback loop are

$$P_1 \approx \frac{-1}{gm_2 R_L R_1 C_C}; \text{ for high } R_L$$

$$\approx \frac{-1}{gm_2 R_L R_1 C_C + R_1(C_1 + C_C)}; \text{ for low } R_L$$

$$P_2 \approx \frac{-gm_2 C_C}{C_L(C_1 + C_C) + C_1 C_C}; \text{ for high impedance load}$$

$$\approx \frac{-(gm_2 + g_2) C_C}{C_C(C_1 + C_C) + C_1 C_C}; \text{ for low impedance load}$$

$$P_3 \approx \frac{-1}{R_C C_1}$$

$$Z \approx \frac{-1}{R_C C_C - \frac{C_C}{gm_2}}$$

Note that the pole splitting between  $P_1$  and  $P_2$  is a function of the load resistance and load capacitance. For low resistive loads the open-loop gain of the positive swing amplifier drops, and  $P_1$  and  $P_2$  both move out in frequency. Since both  $P_1$  and  $P_2$  move out in frequency, phase degradation could occur depending on the location of  $P_3$ ; however, by bringing the zero shown above, into the left half plane, some phase shift that occurs can be cancelled. The zero placement also helps to cancel phase shift that will occur as a result of capacitive loading on the output. As the output capacitance increases,  $P_2$  decreases and phase margin degradation occurs; however, by careful placement of the zero, the reduction in the phase margin can be minimized.

The ac stability of the total output stage can be modeled, to a first order, as two independent amplifiers in parallel. Since the negative unity gain amplifier is an inverted mirror image of the positive unity gain amplifier with equal drive requirements, the dominant poles and zeros of each amplifier are approximately the same, and the complete output amplifier transfer function simplifies to that of a half cycle stage. The number and location of the poles and zeros of the complete output stage are identical to those in each of unity gain amplifiers; therefore, no additional compensation is required to stabilize the complete output stage.

The total amplifier circuit is capable of driving 300  $\Omega$  and 1000 pF to ground. The gain-bandwidth product is approximately 500 kHz and is limited by the output stage 1000 pF load requirement. The output stage bandwidth is approximately 1.0 MHz.

### III. EXPERIMENTAL RESULTS

The power amplifier presented was fabricated using National Semiconductor's proprietary  $P^2$ CMOS process. A die photo of the power amplifier is shown in Fig. 5. The total die area of the power amplifier is 1500 mils<sup>2</sup>.

Table I shows a comparison between the simulated and measured results of the power amplifier and Table II shows the device sizes that correspond to Fig. 3. Since the ampli-

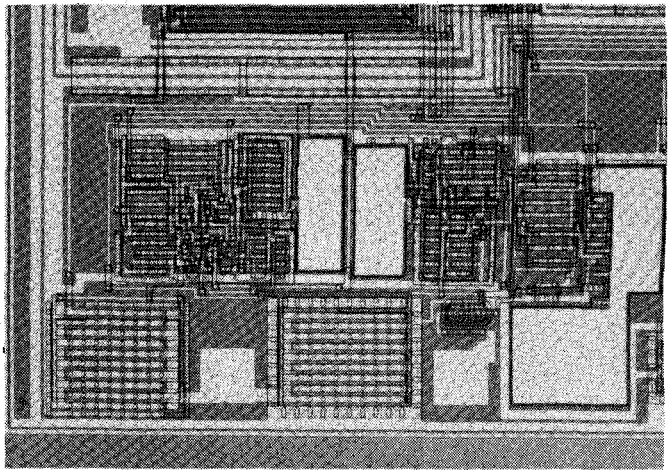


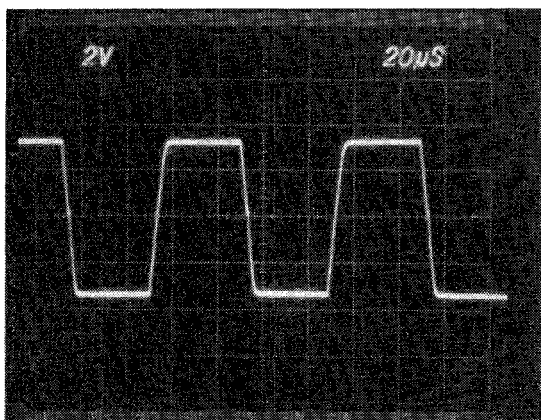
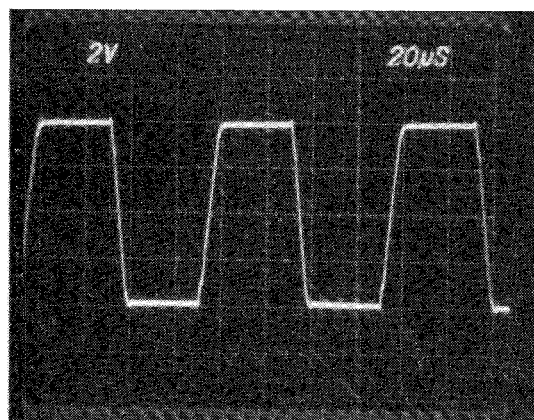
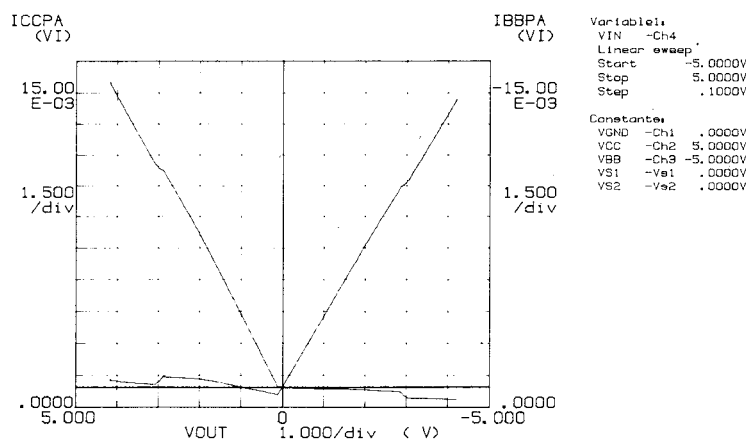
Fig. 5. Die photo of power amplifier.

TABLE I  
POWER AMPLIFIER PERFORMANCE

Parameter	Simulation	Measured Results
Power dissipation	7.0 mW	5.0 mW
$A_{vol}$	82 dB	83 dB
$F_u$	500 kHz	420 kHz
$V_{offset}$	0.4 mV	1 mV
PSRR+ (dc)	85 dB	86 dB
(1 kHz)	81 dB	80 dB
PSRR- (dc)	104 dB	106 dB
(1 kHz)	98 dB	98 dB
THD $V_{IN} = 3.3 V_p, R_L = 300 \Omega$	0.03%	0.13%(1 kHz)
$C_L = 1000 \text{ pF}$	0.08%	0.32%(4 kHz)
$V_{IN} = 4.0 V_p, R_L = 15K \Omega$	0.05%	0.13%(1 kHz)
$C_L = 200 \text{ pF}$	0.16%	0.20%(4 kHz)
$T_{settling} (0.1\%)$	3.0 $\mu\text{s}$	< 5.0 $\mu\text{s}$
Slew rate	0.8 V/ $\mu\text{s}$	0.6 V/ $\mu\text{s}$
1/f noise at 1 kHz	N/A	130 nV/Hz
Broad-band noise	N/A	49 nV/Hz
Die area		1500 mils <sup>2</sup>

TABLE II  
COMPONENT SIZES  
( $\mu\text{m}, \text{pF}$ )

M16	184/9	M8A	481/6
M17	66/12	M13	66/12
M8	184/6	M9	27/6
M1, M2	36/10	M10	6/22
M3, M4	194/6	M11	14/6
M3H, M4H	16/12	M12	140/6
M5	145/12	MP3	8/6
M6	2647/6	MN3	244/6
MRC	48/10	MP4	43/12
CC	11.0	MN4	12/6
M1A, M2A	88/12	MP5	6/6
M3A, M4A	196/6	MN3A	6/6
M3HA, M4HA	10/12	MP3A	337/6
M5A	229/12	MN4A	24/12
M6A	2420/6	MP4A	20/12
MRF	25/12	MN5A	6/6
CF	10.0		

Fig. 6. Output time response for a  $\pm 3.3 V_p$  input pulse.Fig. 7. Output time response for a  $\pm 4.0 V_p$  input pulse.Fig. 8. Power supply current versus output voltage level for  $R_L = 300 \Omega$ .

fier was designed to be used in an inverting configuration, the common-mode range and CMRR are not applicable op amp parameters.

Shown in Figs. 6 and 7 are step responses of  $\pm 3.3 V_p$  and  $\pm 4.0 V_p$  for loads of  $300 \Omega/1000 \text{ pF}$  and  $15 \text{ K} \Omega/200 \text{ pF}$ , respectively, using  $\pm 4.75 \text{ V}$  supplies. The slight cross-over distortion, as seen in Fig. 6, while slewing negatively, is a result of the delay caused by the offset feedback circuit when amplifier *A2* is required to drive large amounts of current to the load. This distortion is negligible in THD measurements for telecommunication and audio applications.

Fig. 8 shows the efficiency of the power amplifier as the output voltage swings from rail-to-rail. For this case the power supplies used were  $\pm 5.0 \text{ V}$ . The slight discontinuity in the supply current curves at approximately  $\pm 3.0 \text{ V}$  is a result of the opposite unity gain amplifier turning off in the output stage. This discontinuity in supply current has no effect on the distortion seen in the amplifier. The dc operating current at  $0 \text{ V}$  is the operating current for two power amplifiers since the application in which the power amplifiers is to be used requires a differential signal. The

dc operating current per amplifier is  $500 \mu\text{A}$ . The ICCPA current in the positive supply is greater due to the fact that the high current *M6* source is mirrored around to the source follower *M8A* by the output driver current offset feedback circuit.

Amplifier offset voltages of typically  $1 \text{ mV}$  were measured. These low offsets were a result of a good process and careful layout. From these data and the fact that amplifier feedback will reduce any offset between the output unity gain amplifiers, the dc current variation in the output driver devices should be very small.

#### IV. CONCLUSION

Presented was a fully CMOS class *AB* power amplifier wherein supply-to-supply voltage swings across low impedance loads are efficiently and readily handled. The amplifier dissipates only  $7 \text{ mW}$  of dc power and can deliver  $36 \text{ mW}$  of ac power to a  $300 \Omega$  load using  $\pm 5.0 \text{ V}$  power supplies. Other features of the design include typical offset voltages of  $1 \text{ mV}$  and THD of less than  $0.4$  percent.

## ACKNOWLEDGMENT

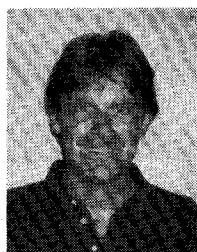
The authors gratefully acknowledge the contributions of C. Laber to the design of the presented power amplifier.

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**Kevin E. Brehmer** (S'79-M'80) received the B.S.E.E. degree from the University of Michigan, Ann Arbor, in 1980 and is currently working on the M.S.E.E. at the University of Santa Clara, Santa Clara, CA.

From 1980 to 1981 he was a Design Engineer involved in subscriber



loop products for the Telecommunications Group at Mostek, Carrollton, TX. In 1981 he joined the Telecom Group at National Semiconductor, Santa Clara, CA, as a Design Engineer, where he is involved in CMOS analog circuit design.

**James B. Wieser** was born in Detroit, MI, on June 23, 1955. He received the B.S. degree and M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1977 and 1978, respectively.

In 1978 he joined the Telecom Group at National Semiconductor, Santa Clara, CA. He has designed a wide variety of CMOS analog circuits including op amps, A/D converters, and switched-capacitor filters. He is the author of several pending patents. He is currently an En-

gineering Section Manager for the Telecom Group at National Semiconductor.

Mr. Wieser is a member of Tau Beta Pi.

# An Improved Frequency Compensation Technique for CMOS Operational Amplifiers

BHUPENDRA K. AHUJA

**Abstract**—The commonly used two-stage CMOS operational amplifier suffers from two basic performance limitations due to the RC compensation network around the second gain stage. First, this frequency compensation technique provides stable operation for limited range of capacitive loads, and second, the power supply rejection shows severe degradation above the open-loop pole frequency. The technique described here provides stable operation for a much larger range of capacitive loads, as well as much improved  $V_{BB}$  power supply rejection over very wide bandwidths for the same basic op amp circuit. This paper presents mathematical analysis of this new technique in terms of its frequency and noise characteristics followed by its implementation in all n-well CMOS process. Experimental results show 70 dB negative power supply rejection at 100 kHz and an input noise density of 58 nV/ $\sqrt{\text{Hz}}$  at 1 kHz.

## I. INTRODUCTION

**L**INEAR CMOS techniques have achieved significant progress over the last five years to provide high-performance low-power analog building blocks like opera-

tional amplifiers (op amp), comparators, buffers, etc. These circuits have demonstrated comparable performance to their bipolar counterparts at much less silicon area and power dissipation, thus enabling single chip implementations of complex filtering functions, A/D and D/A conversions with quite stringent specification. Due to relatively simple circuit configurations and flexibility of design, CMOS technology has an edge over NMOS technology and is gaining rapid acceptance as the future technology for linear analog integrated circuits, especially in the telecommunication field [1], [2]. The most important building block in any analog IC is the op amp of which numerous implementations have been reported in both the technologies [3], [6].

The most commonly used op amp configuration in CMOS has two gain stages, the first one being the differential input stage with single-ended output, and the second one being either class A or class AB inverting output stage. Each stage typically is designed to have gain in the range of 40 to 100. Fig. 1(a) shows the circuit configuration while