A 1.7mW 11b 250MS/s 2x Interleaved Fully Dynamic Pipelined SAR ADC in 40nm Digital CMOS

Bob Verbruggen[1], Masao Iriguchi[2], Jan Craninckx[1]

[1] imec, Leuven, Belgium

[2] Renesas Electronics, Kawasaki, Japan

© 2012 IEEE

Outline

- Motivation
- ADC channel implementation
  - Coarse SAR
  - Residue amplifier
  - Fine SAR
- Calibration and measurements
- Conclusion

Motivation: efficient ADC for high bandwidth wireless standards

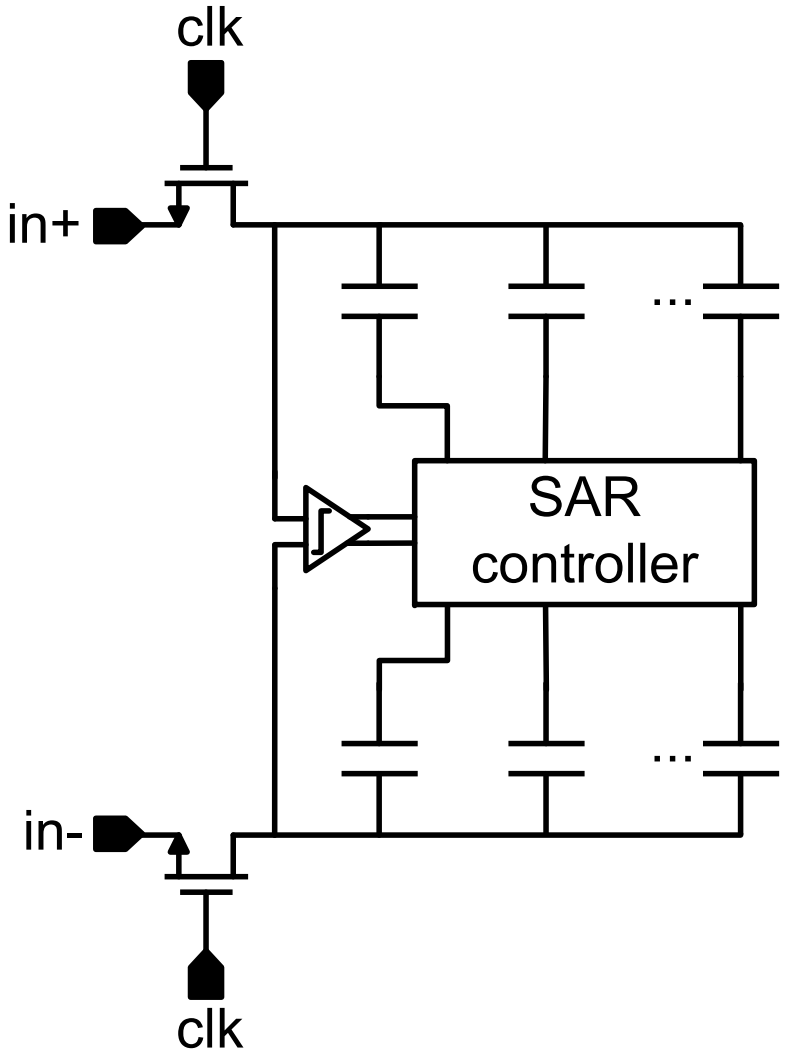
- LTE-Advanced uses up to 50 MHz I/Q BW

  ➔ 200 MS/s ADC w/ factor 2 oversampling

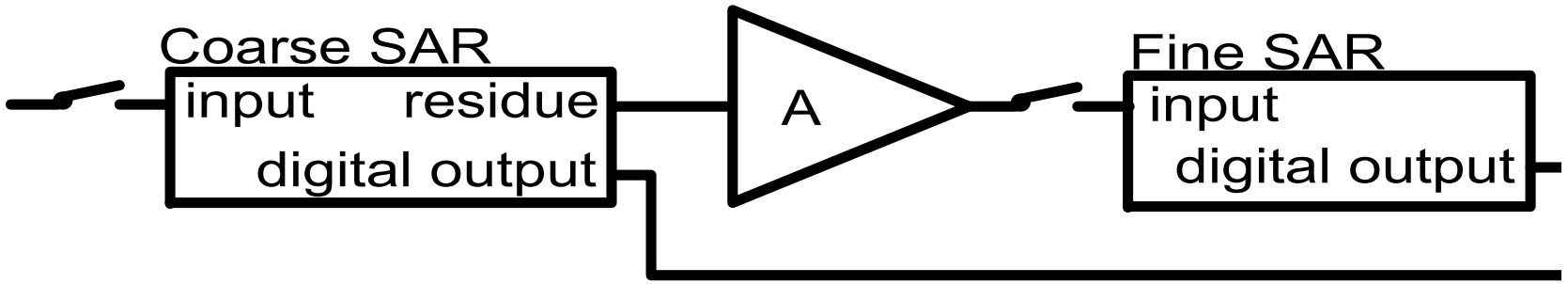
- A/D conversion is low power

  ➔ More oversampling eases analog signal conditioning

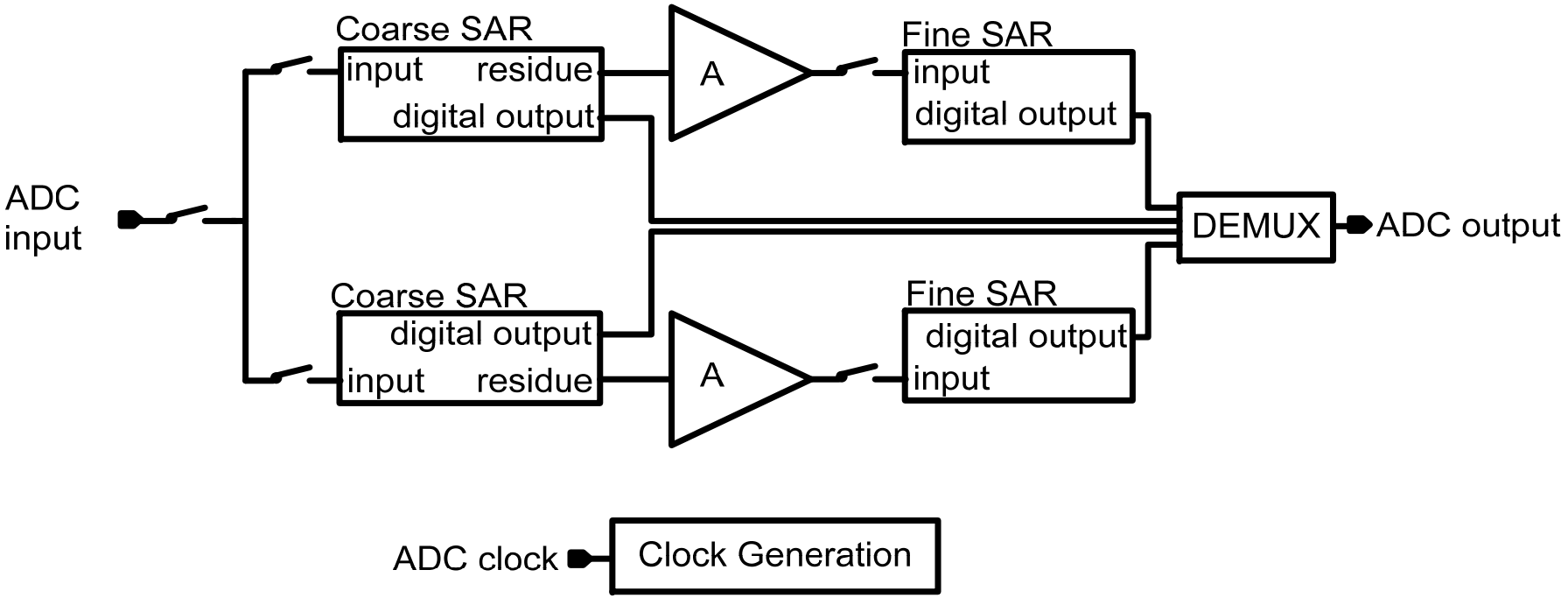
Proposed architecture: SAR ADC core for high efficiency



Proposed architecture: pipelining for increased speed



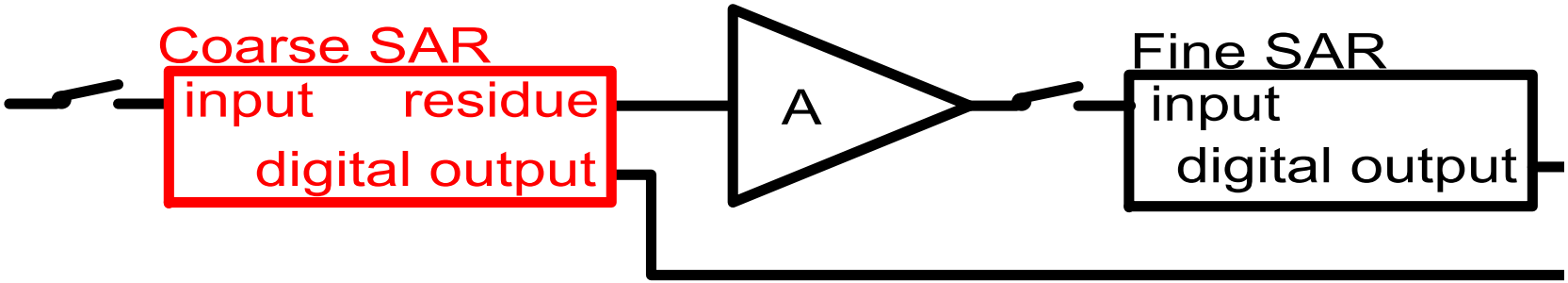
Proposed architecture: factor 2 interleaving for speed



Outline

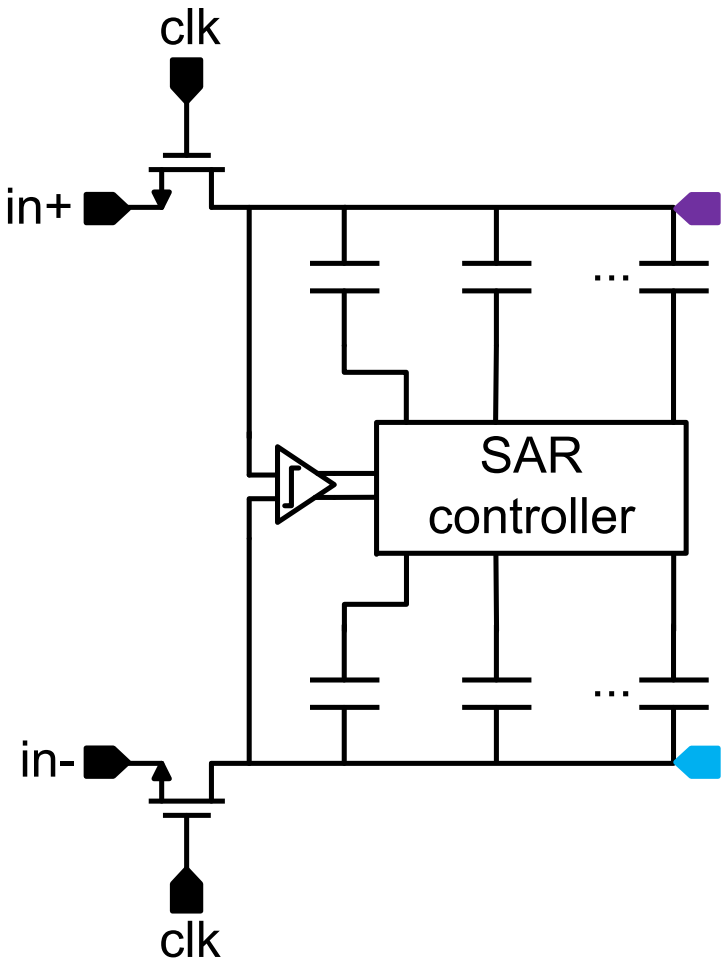
- Motivation
- ADC channel implementation
  - Coarse SAR
  - Residue amplifier
  - Fine SAR
- Calibration and measurements
- Conclusion

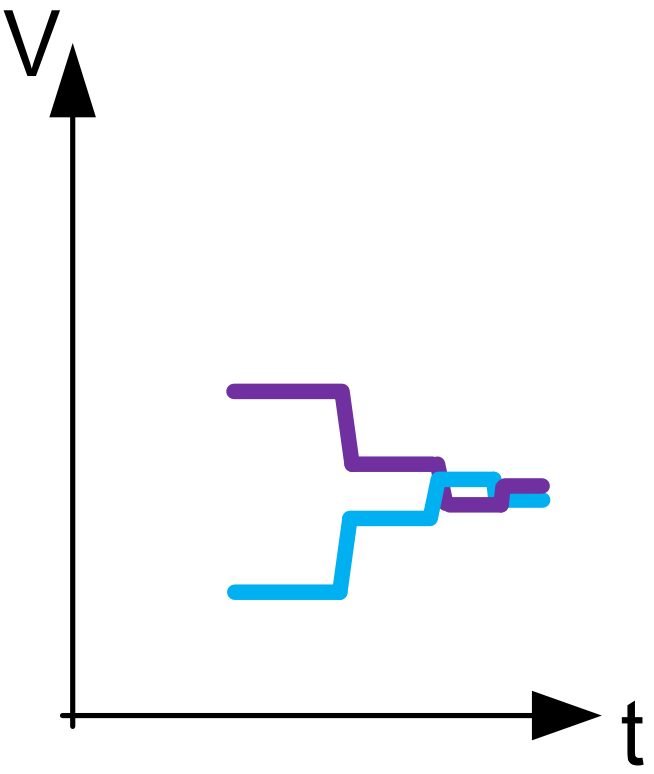
ADC channel (1): 6 cycle coarse SAR generates residue



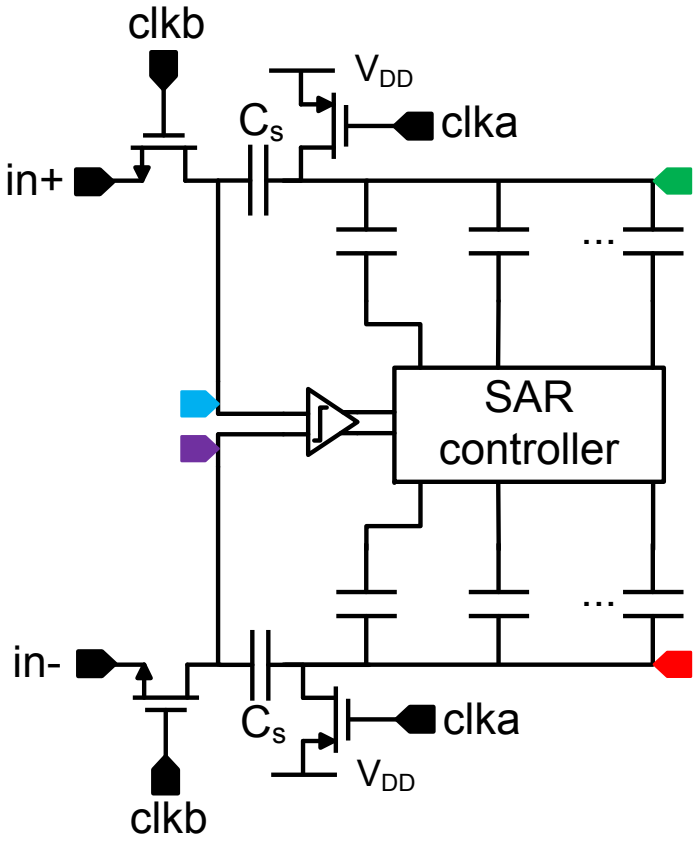
- Samples input signal
- Quantizes
- Generates ~ 20 mV residue
- Robust to comparator errors
  - ➔Low comparator accuracy requirement
  - ➔Low power

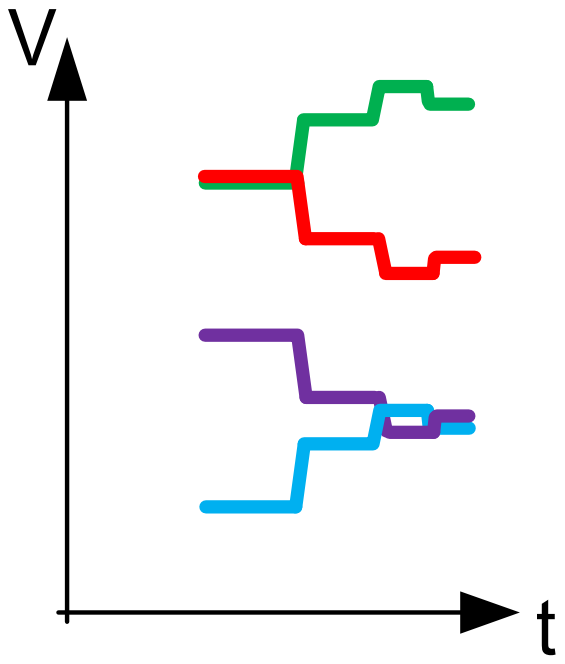
Conventional SAR implementation





Coarse SAR implementation: series sampling capacitance reduces input capacitance

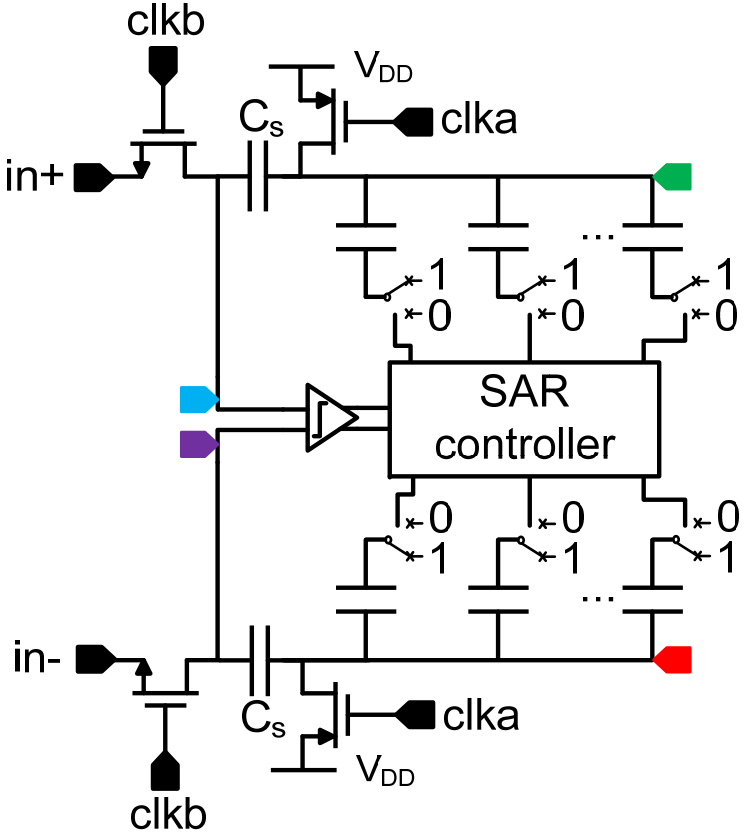


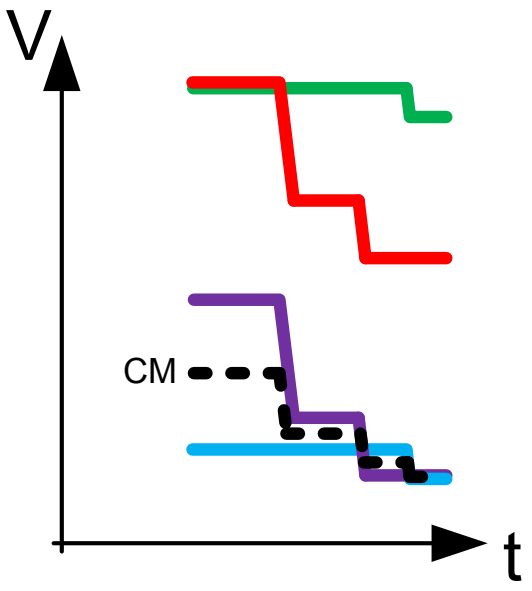


Input voltage tracked across C_s

C_s = 1 pF $T_{track} = T_{clk} / 4$

Coarse SAR implementation: single-ended DAC switching for fast settling



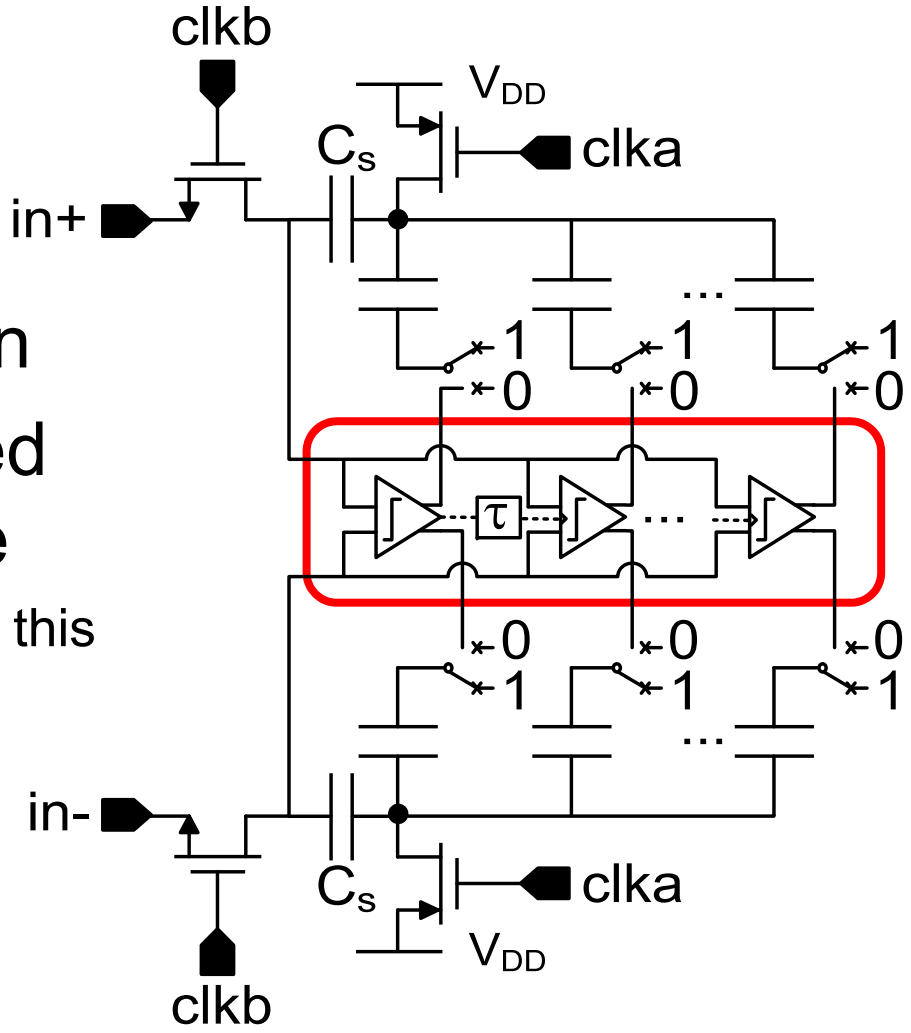


- Either positive or negative node discharged
  - Settling through NMOS with maximum overdrive
  - Common-mode changes each cycle
  - C_{MSB} = 2 x 1 pF

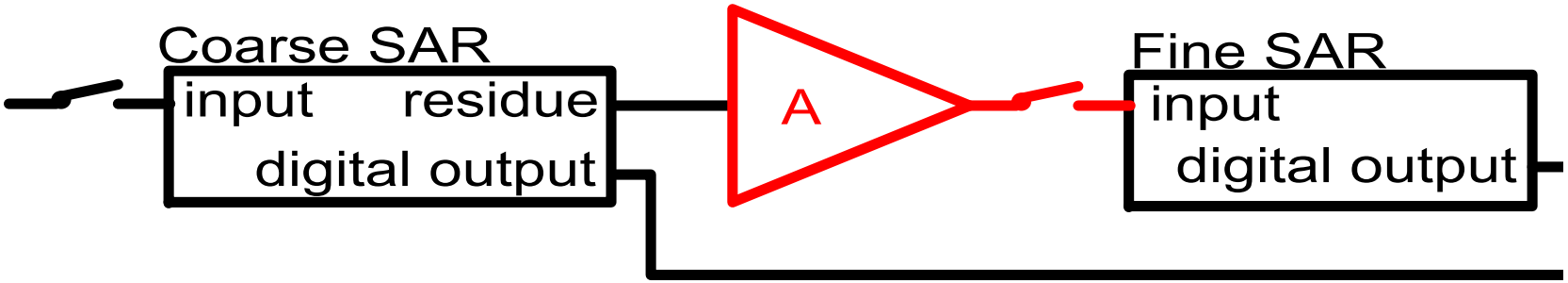
© 2012 IEEE

Coarse SAR implementation: Controller replaced by comparators + delays

- Lower power consumption
- Each comparator activated at specific common-mode
  - Comparator offsets calibrated at this common-mode



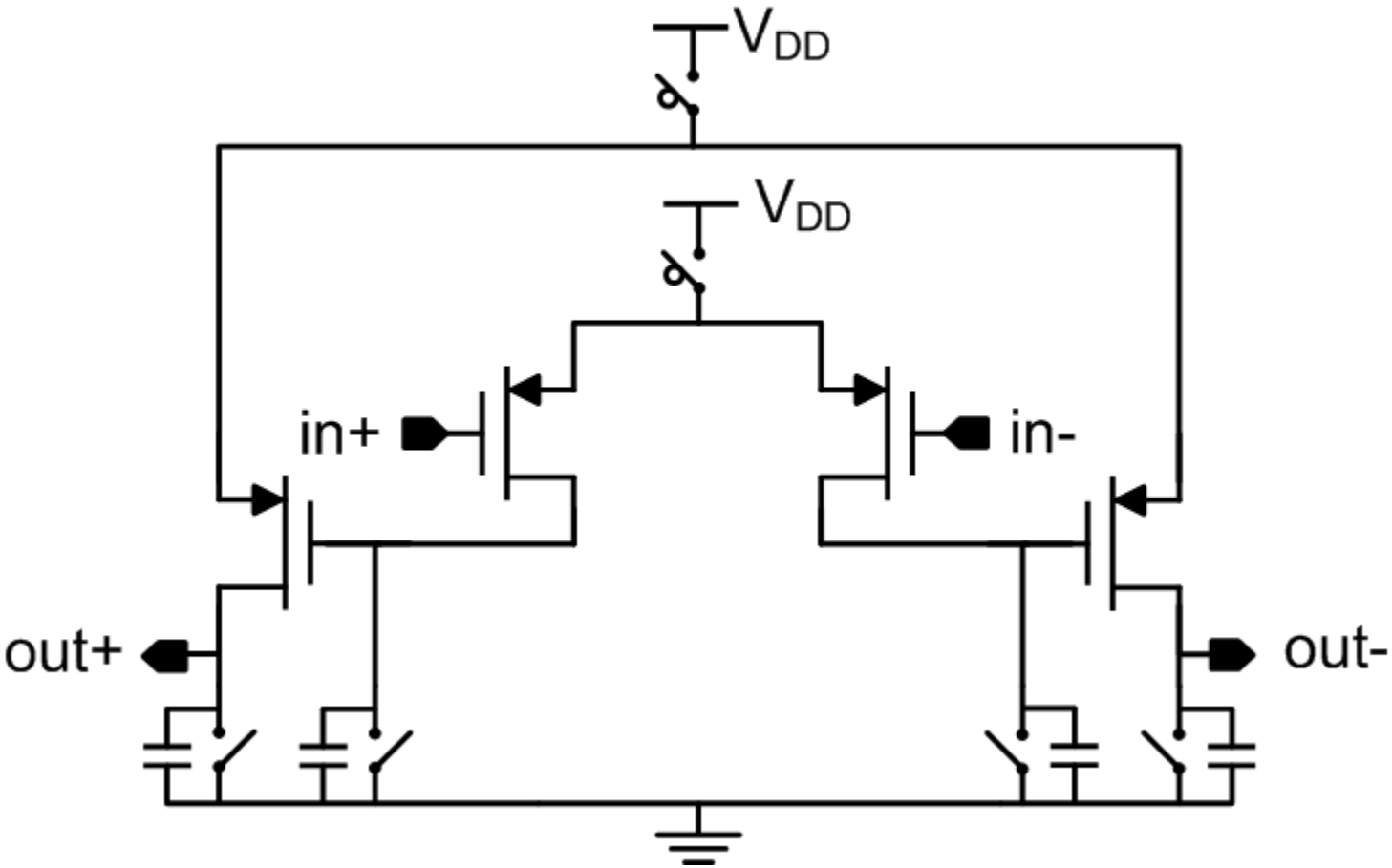
ADC channel (2): Dynamic residue amplification



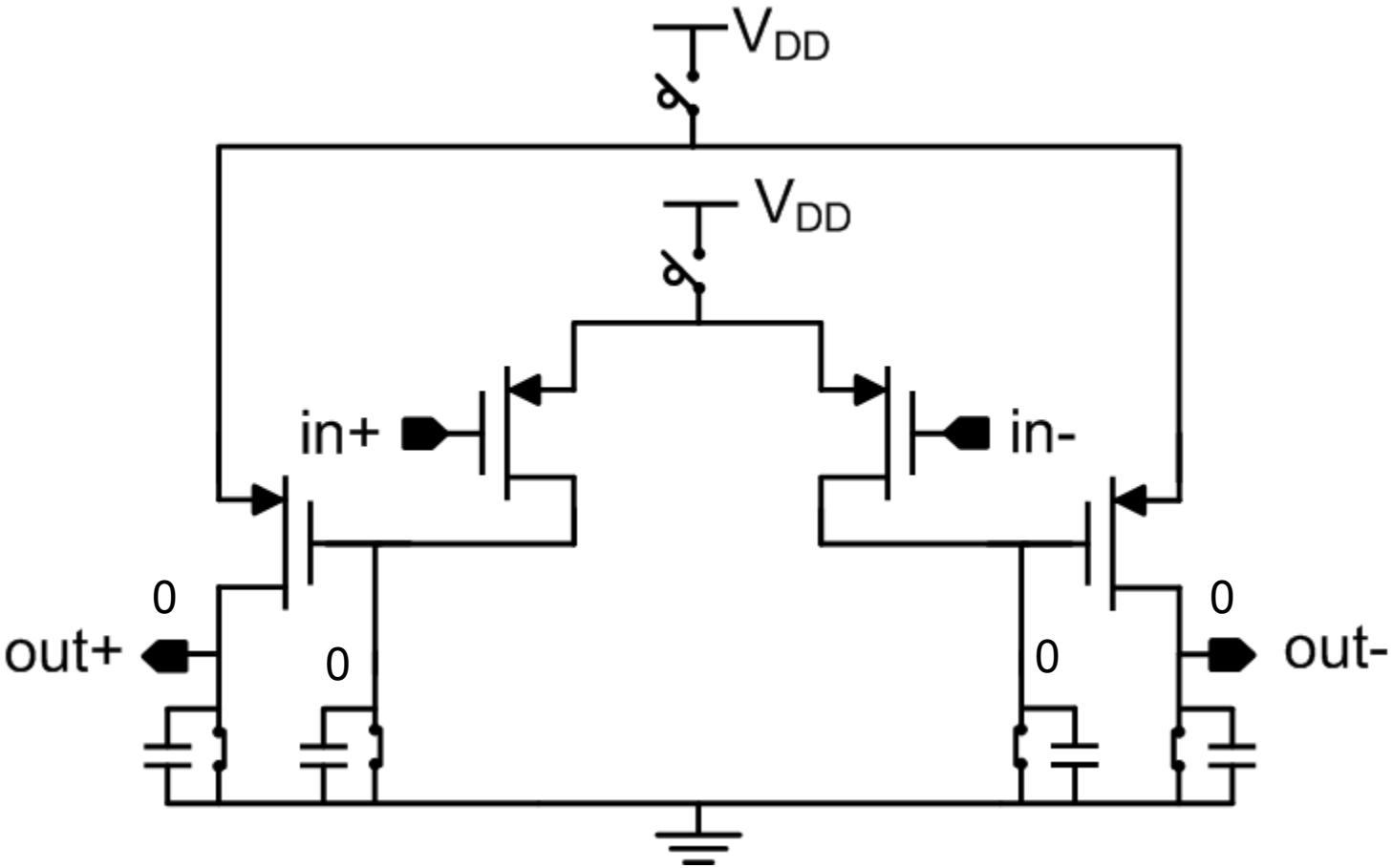
- Amplifies residue and samples
- Small output swing ➔ low linearity requirement
- Uncertain gain ➔ mixed signal calibration matches coarse LSB to fine MSB
- Fast settling time at low power

© 2012 IEEE

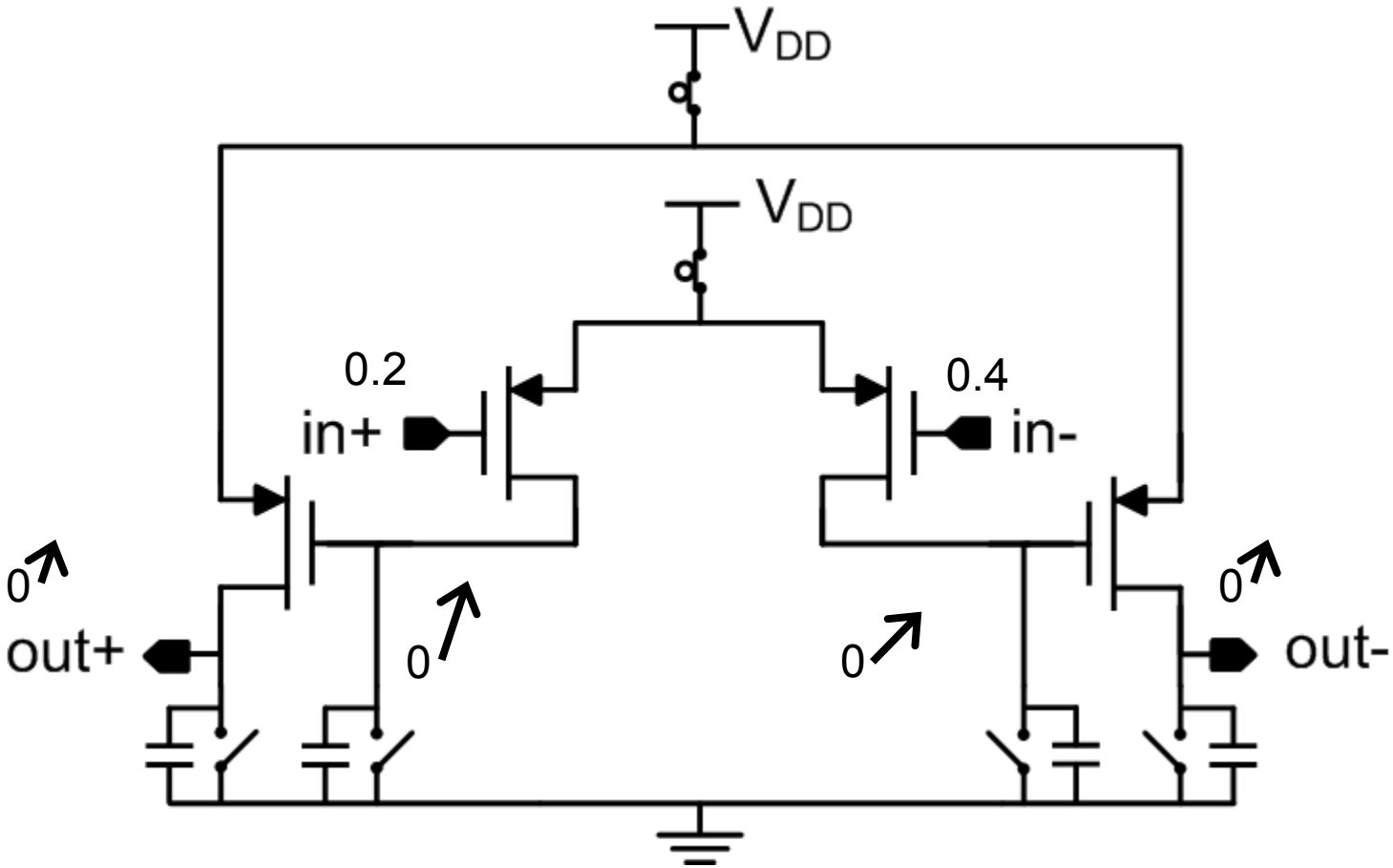
Dynamic amplifier (simplified)



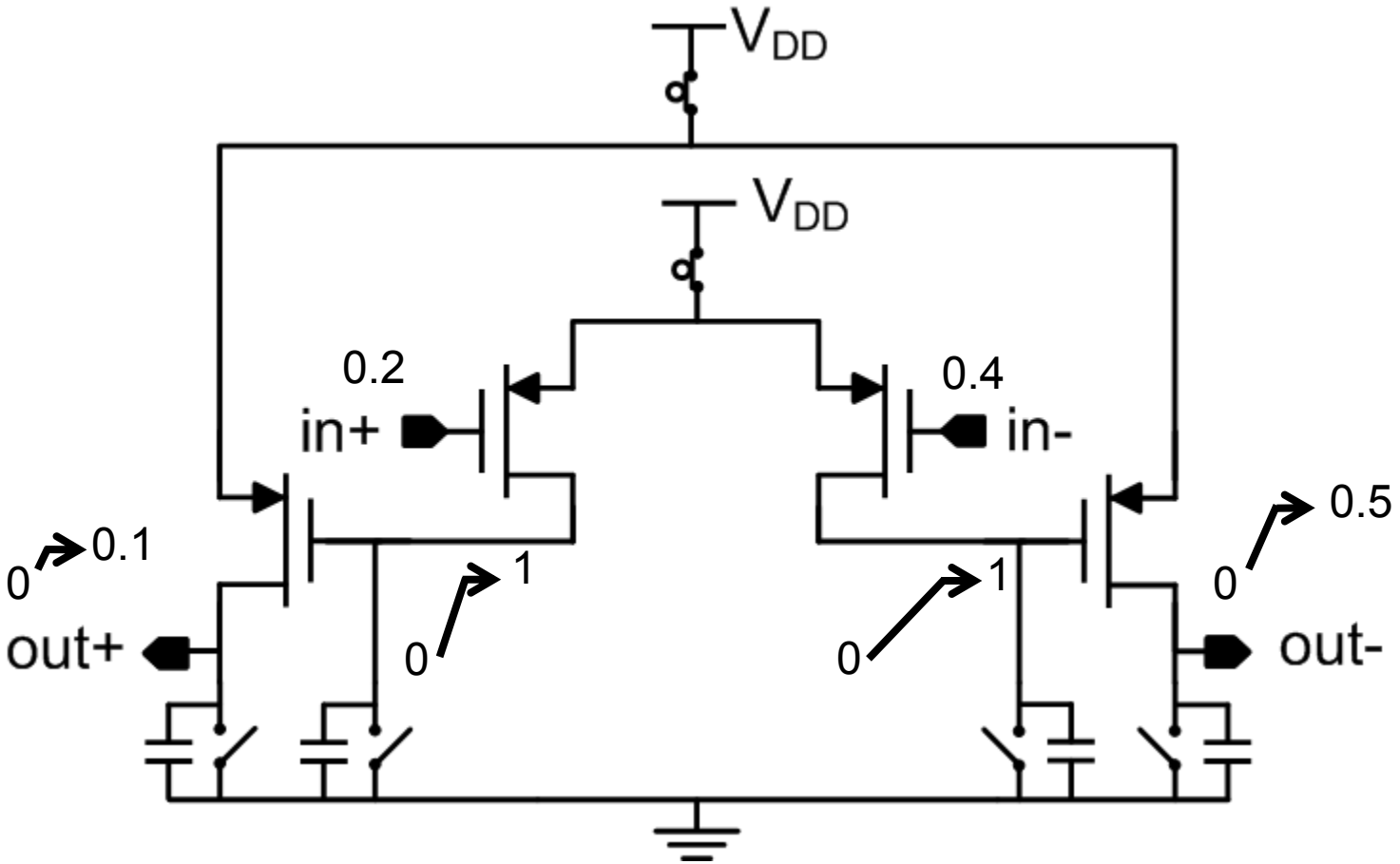
Amplifier outputs reset to ground: no static current



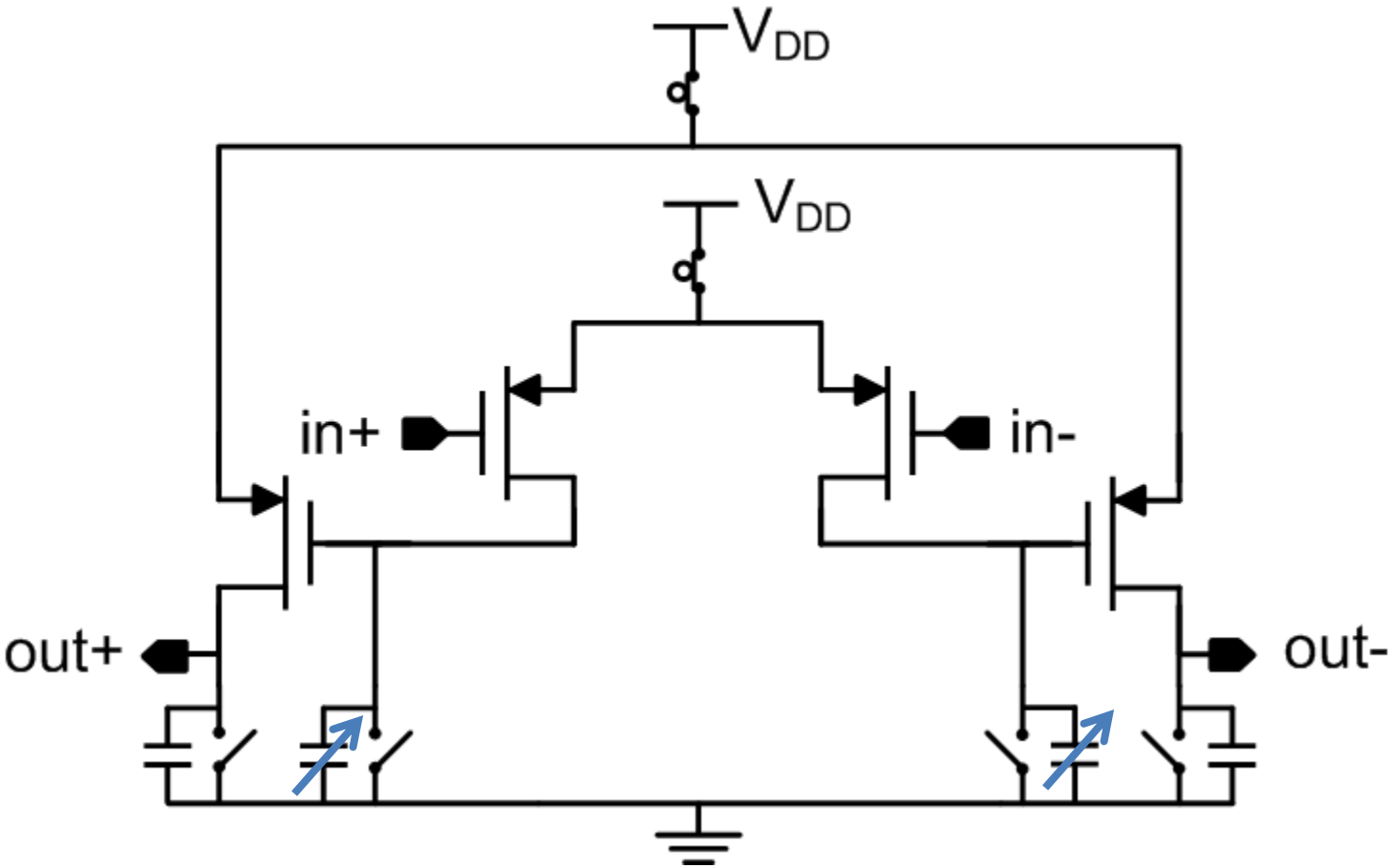
Amplifier converts voltage into charging time, current dumped into output



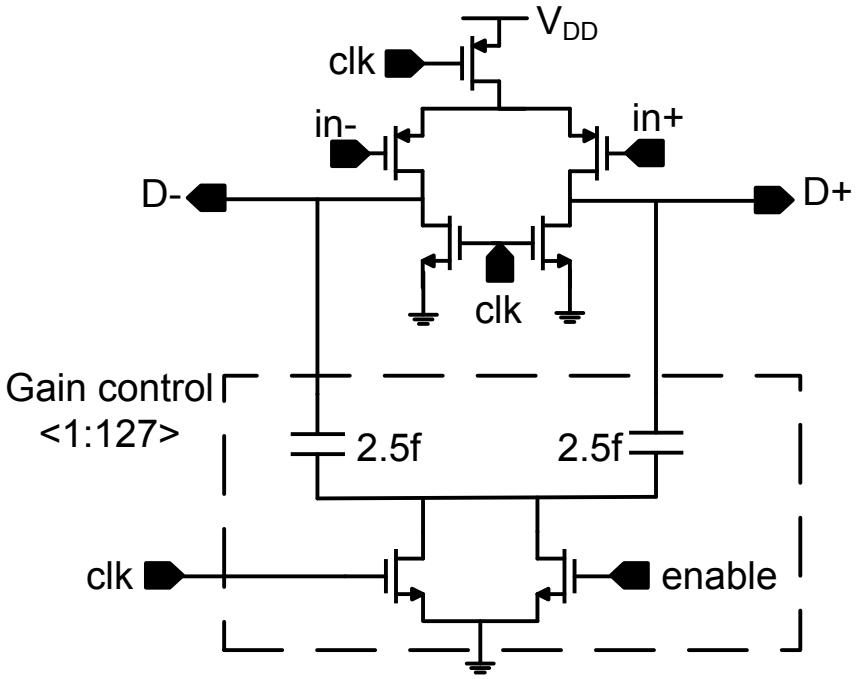
Input drain node turns off output transistor ➔ no static current, output fixed

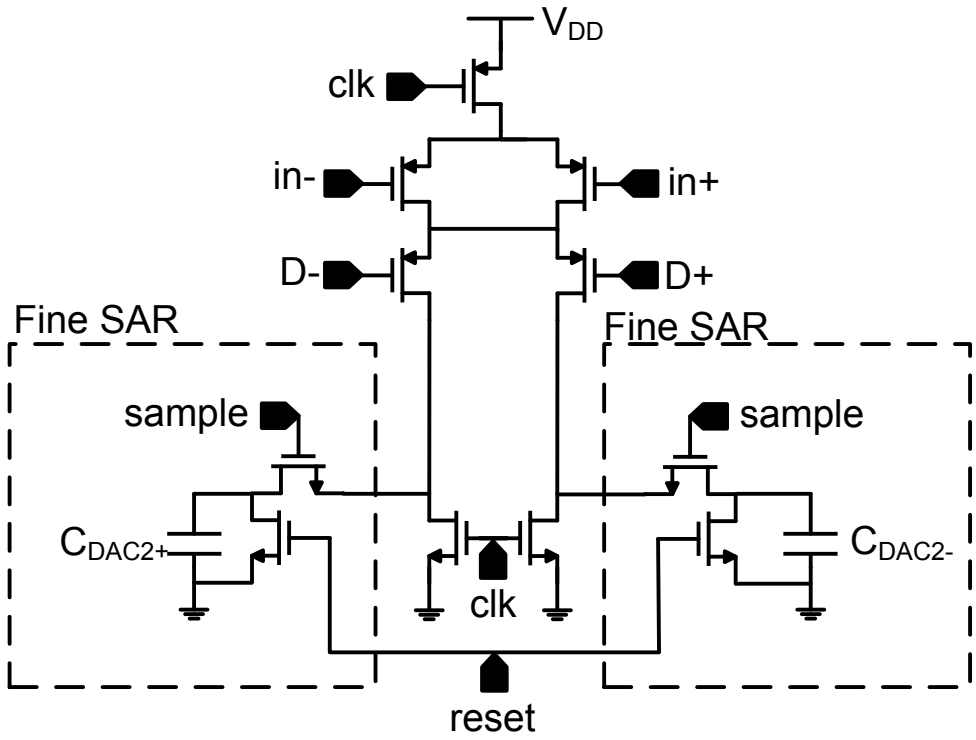


Amplifier gain controlled using switchable capacitance



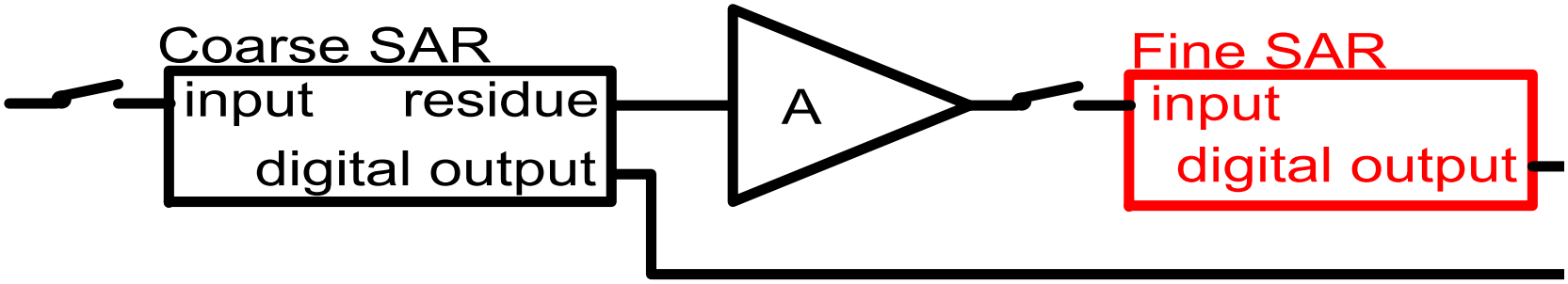
Dynamic amplifier (detailed)





P = 1.1 pJ/cycle	$V_{noise,i.r.}$ < 200 μV
$t_{settling}$ < 1.5 ns	THD < -40 dBFS
Gain control > 10dB	
Gain PVT sensitive: 8.5 dB ⇔ 14 dB	

ADC channel (3): 5+2 cycle fine SAR quantizes amplified residue

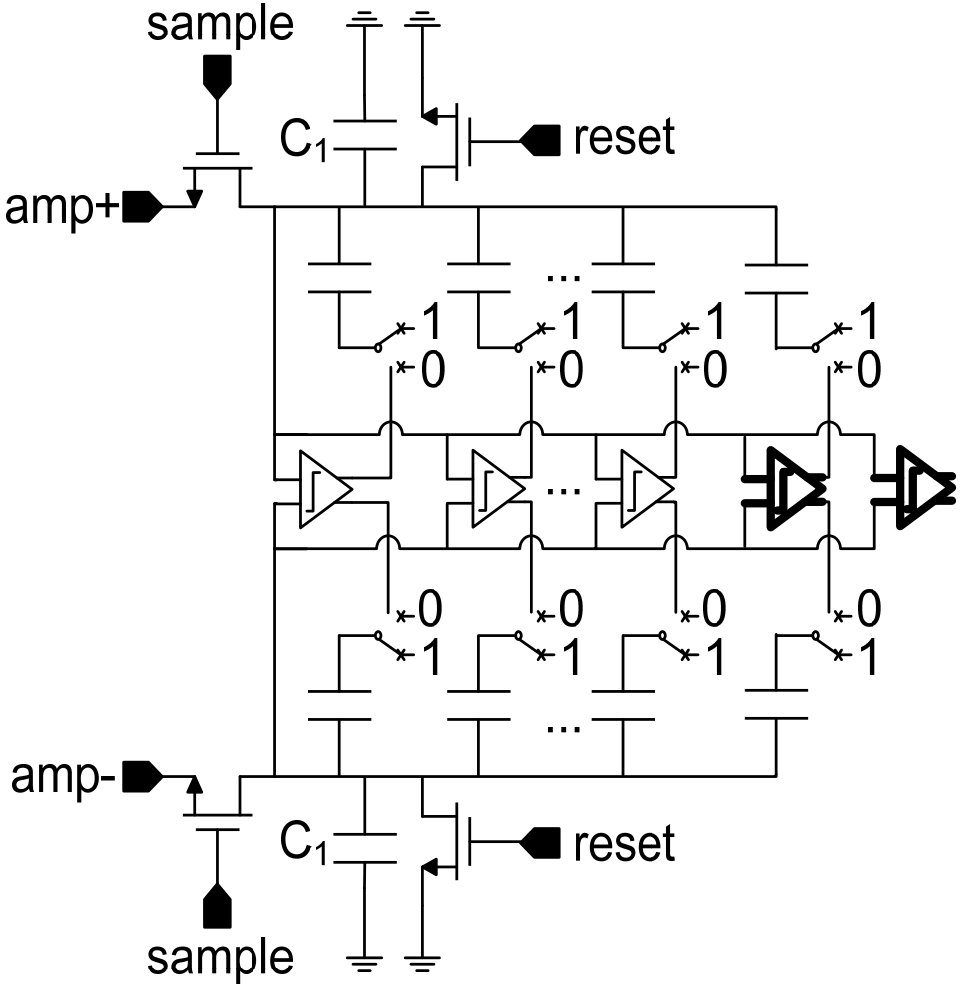


- 1b redundancy between coarse and fine
  - Comparator errors in coarse SAR corrected
- 1b redundancy between cycles 5 and 6
  - Comparator errors in cycles 1-5 corrected

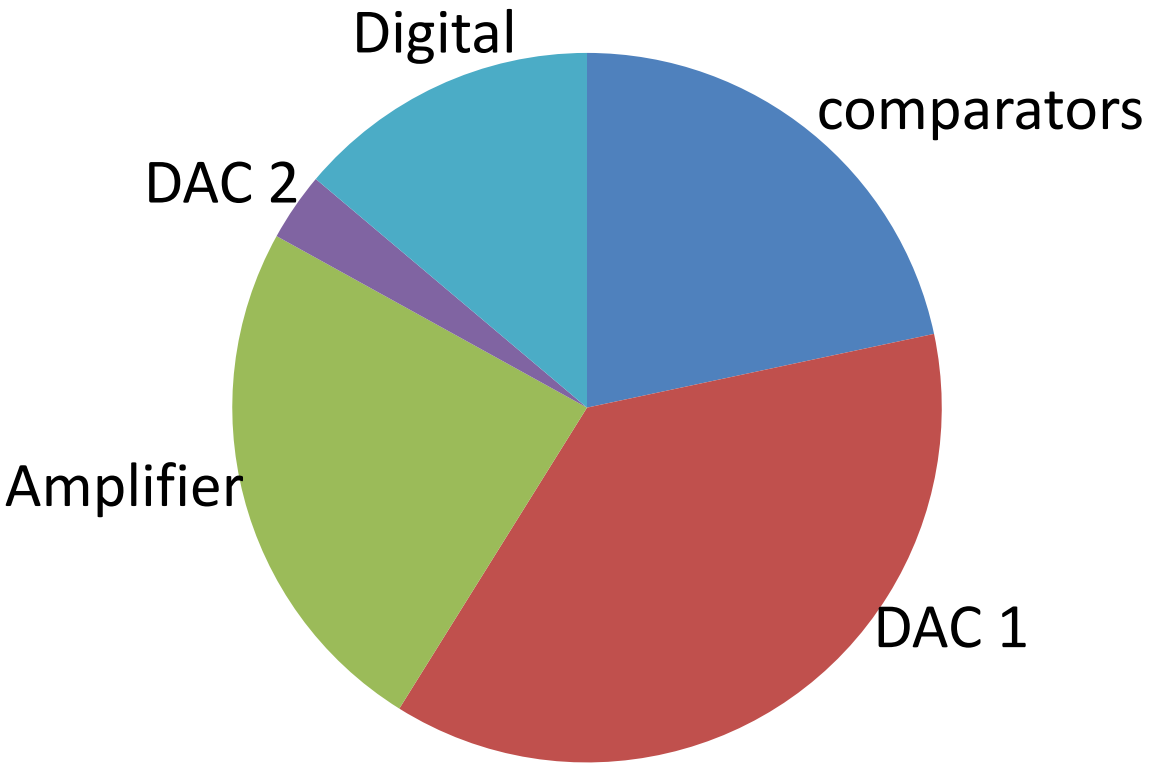
© 2012 IEEE

Fine SAR implementation

- Single-ended DAC switching
- Comparator controlled
  - Lower noise/speed in comparators 6-7
- No series sampling cap.
  - ← C_{MSB} = 31 fF (unit-limited)
- Added C_1= 600 fF to ground
  - ➔ Reduced range
  - ➔ Lowered kT/C noise

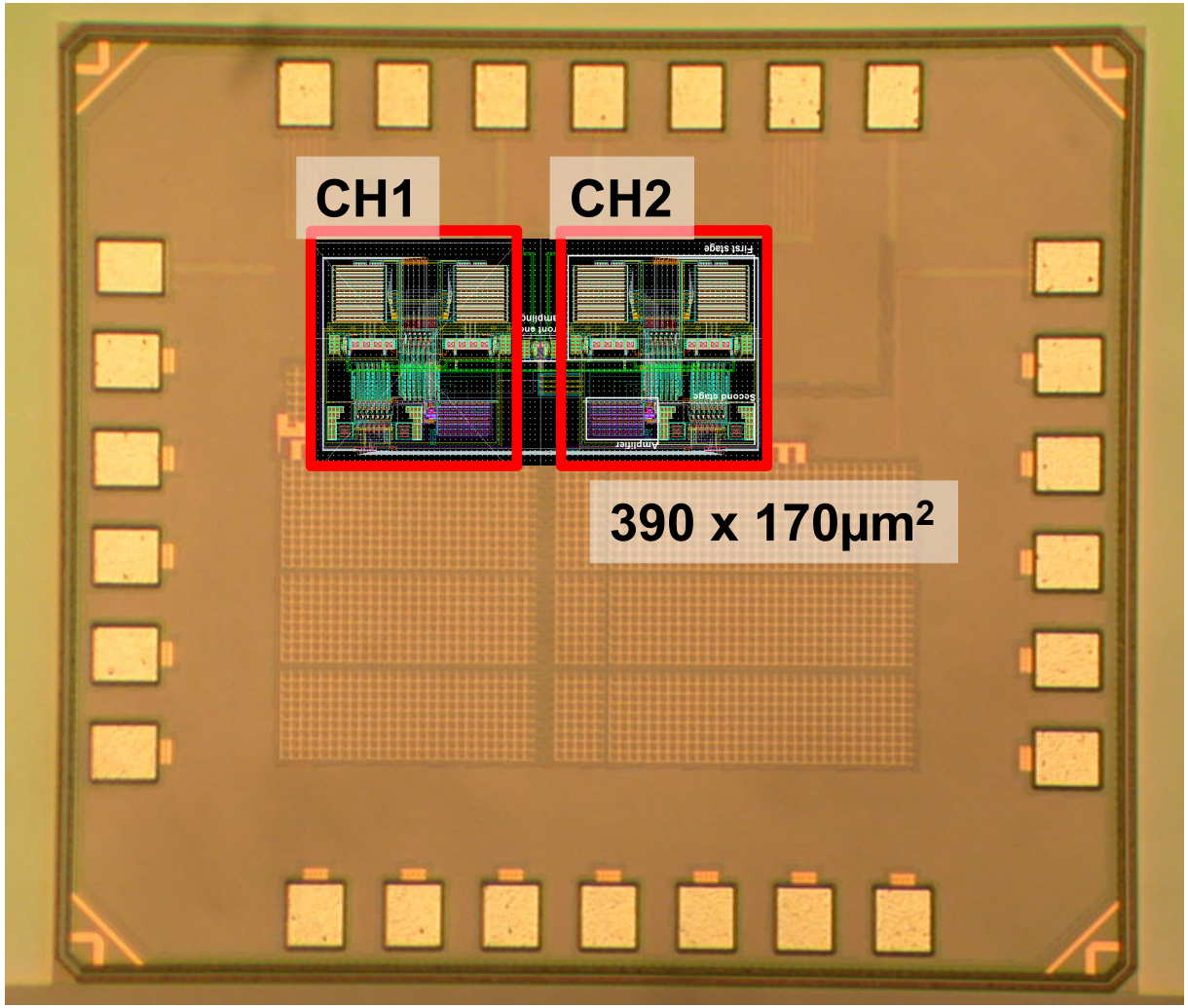


Simulated power breakdown



Total power = 6.9 pJ / conversion

Die photo



1.1 V 40nm LP Digital CMOS

Outline

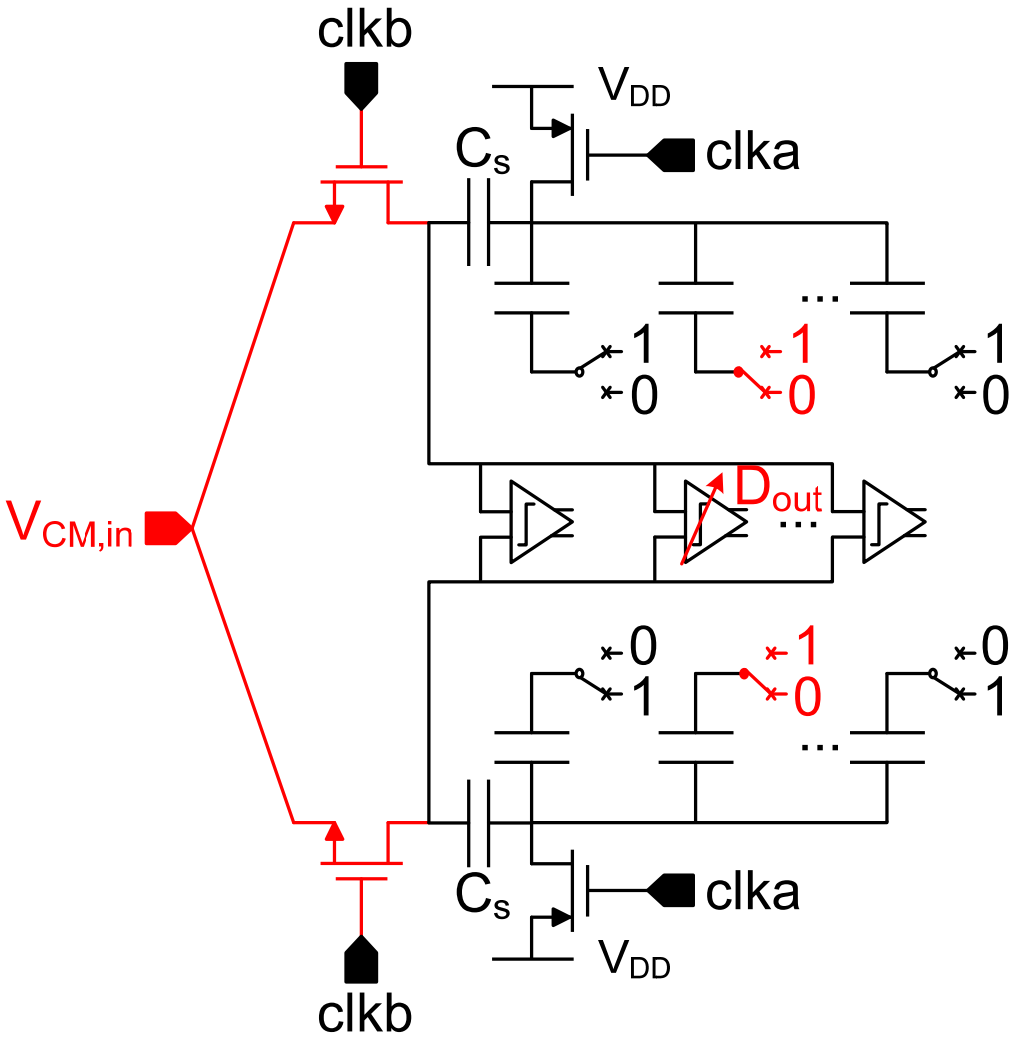
- Motivation
- ADC channel implementation
  - Coarse SAR
  - Residue amplifier
  - Fine SAR
- Calibration and measurements
- Conclusion

Off-line calibration corrects non-idealities

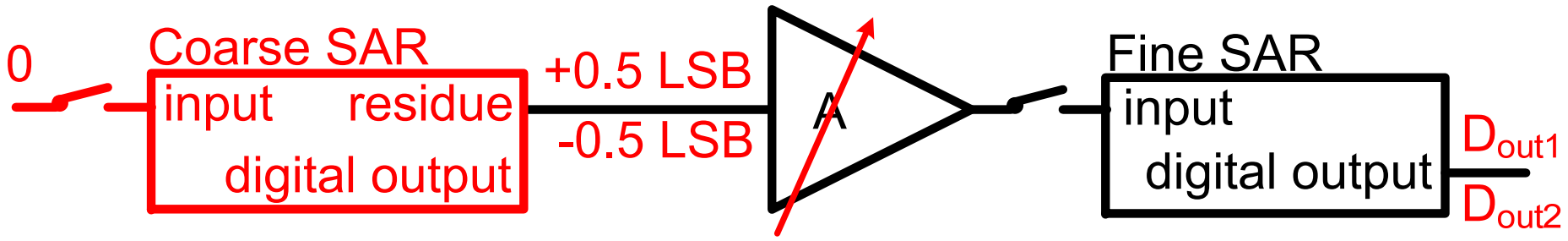
- Shorted input
  - ➔ No dedicated calibration DAC required
- Fully automatic, implemented off-chip
  - ➔ Easy to integrate in VHDL
- Partly sensitive to PVT
  - ➔ Recalibrate when voltage/temperature changes

Comparator offset calibration (1)

- Short ADC input
- Use DAC to generate correct common-mode
- Change comparator thresholds to average $D_{out} = 0.5$
- In second stage: Also cancels amplifier offset
- Sensitive to PVT

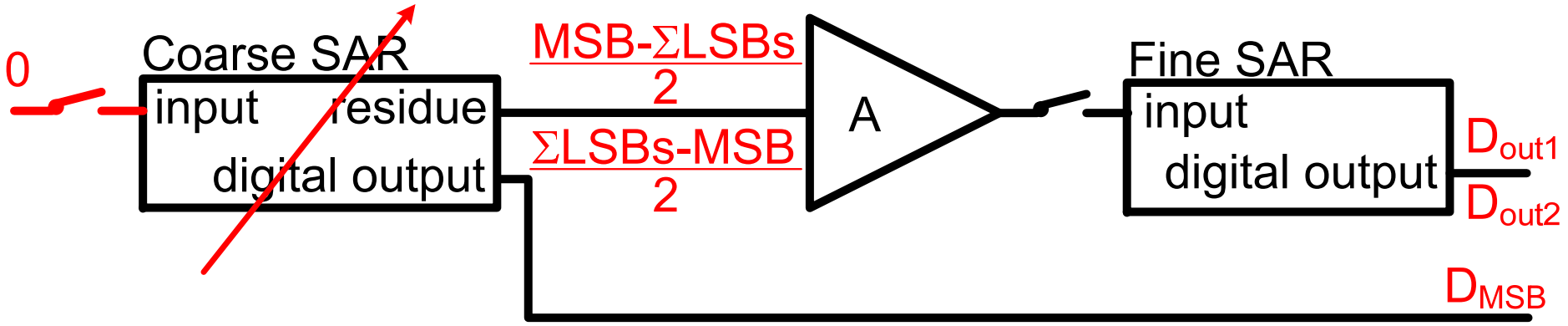


Inter-stage gain calibration



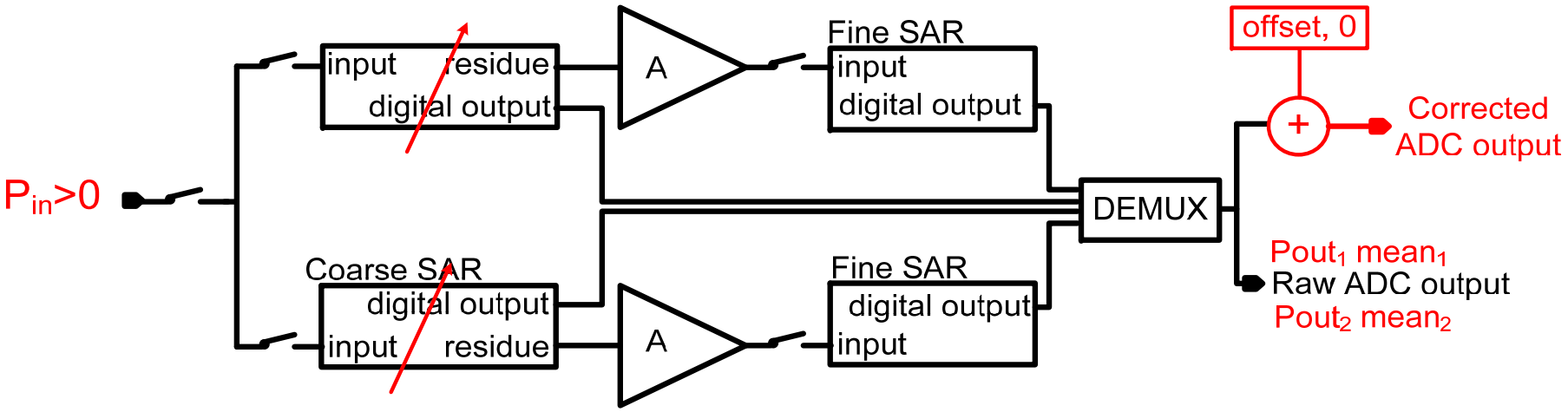
- Short ADC input
- Use coarse DAC to generate +0.5/-0.5 coarse LSB amplifier input
- Change gain to obtain D_{out1}-D_{out2} = 1 fine MSB
- Sensitive to PVT

MSB capacitance calibration



- Short ADC input
- MSB comparator noise ➔ 2 residue values
- Use second stage to measure MSB – Σ(LSBs)
- Change MSB size to obtain D_{out1}-D_{out2} = 1 fine MSB
- Insensitive to PVT

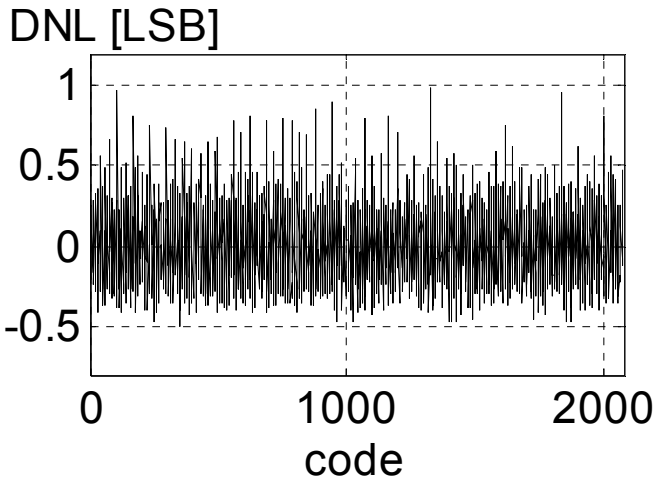
Inter-channel mismatch calibration

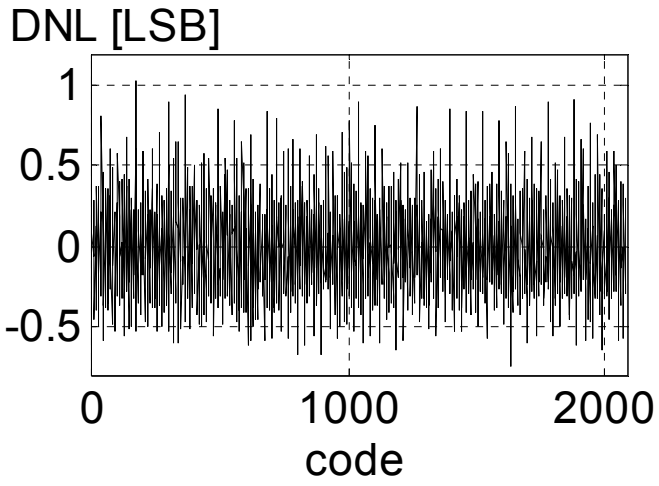


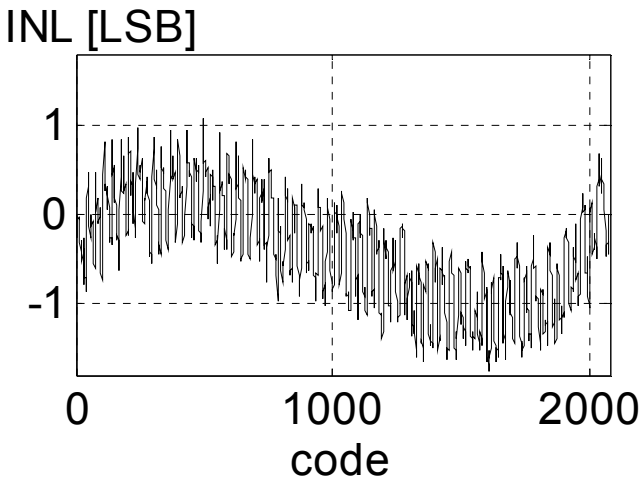
- Apply non-zero input signal
- Measure power & mean of both channel outputs
- Change capacitance on top plate of Coarse DAC to obtain equal power outputs
- Compensate offset digitally (off-chip)
- Gain: insensitive to PVT; offset: sensitive to PVT

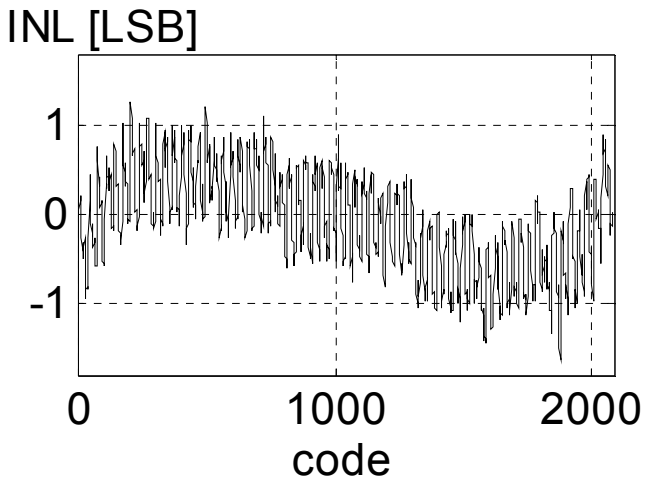
© 2012 IEEE

Static performance at 10 MS/s





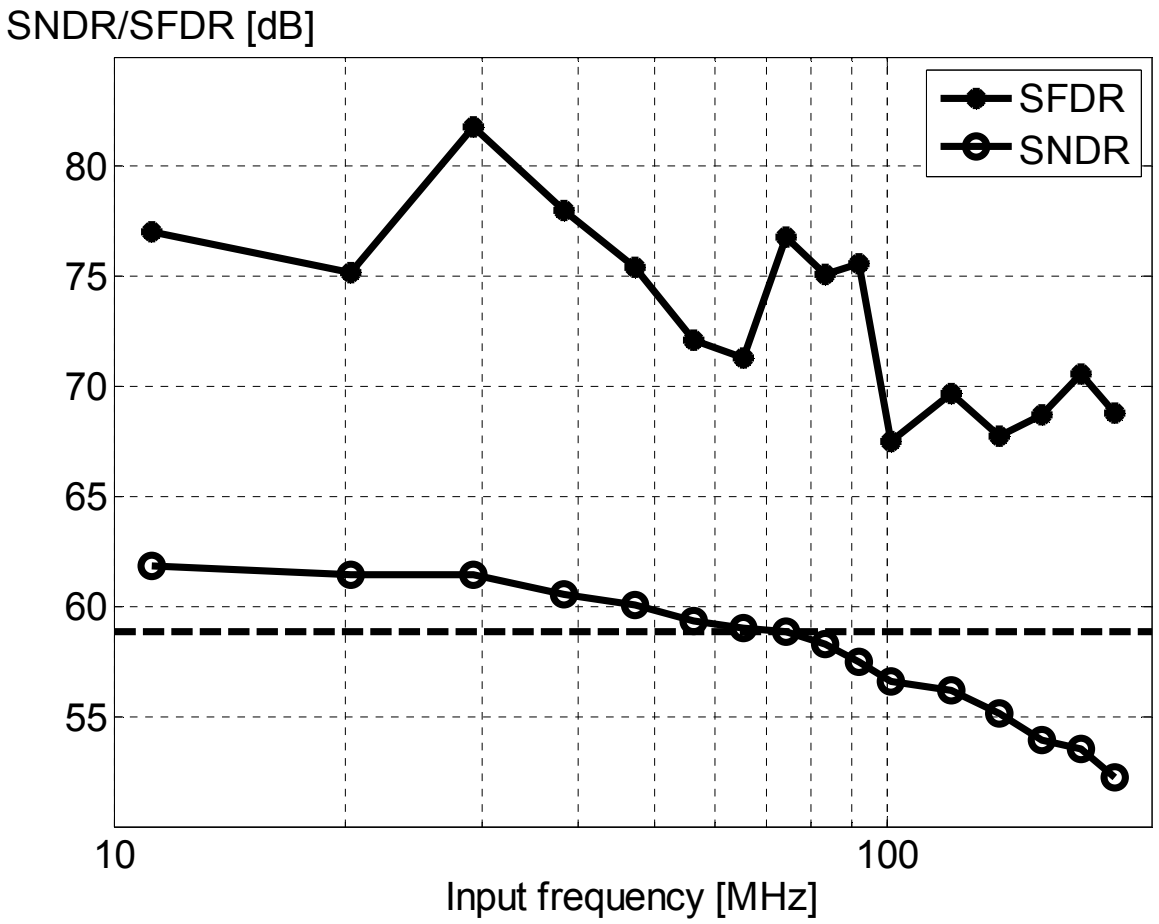




Channel 1

Channel 2

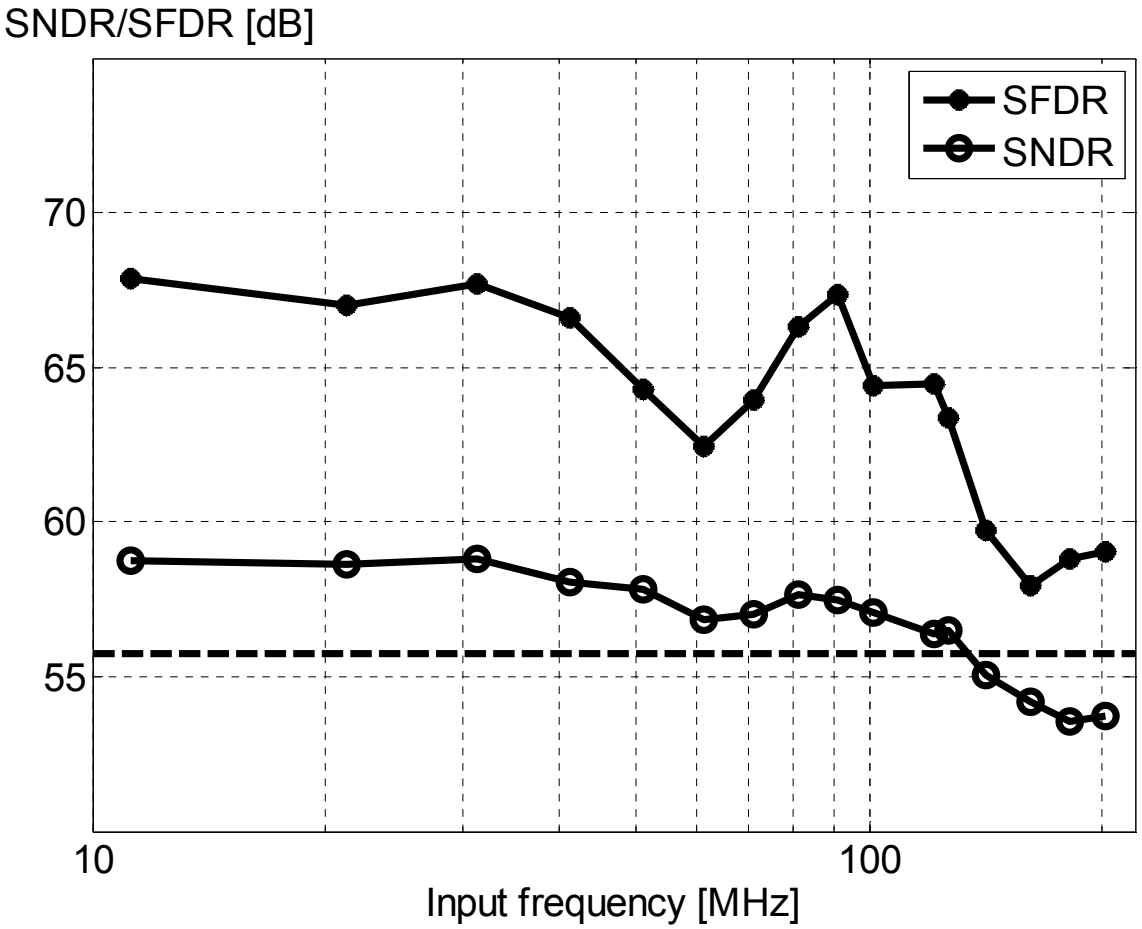
Dynamic performance at 10 MS/s



$SNDR_{max}$ = 62 dB ERBW = 65 MHz

P = 70 μW

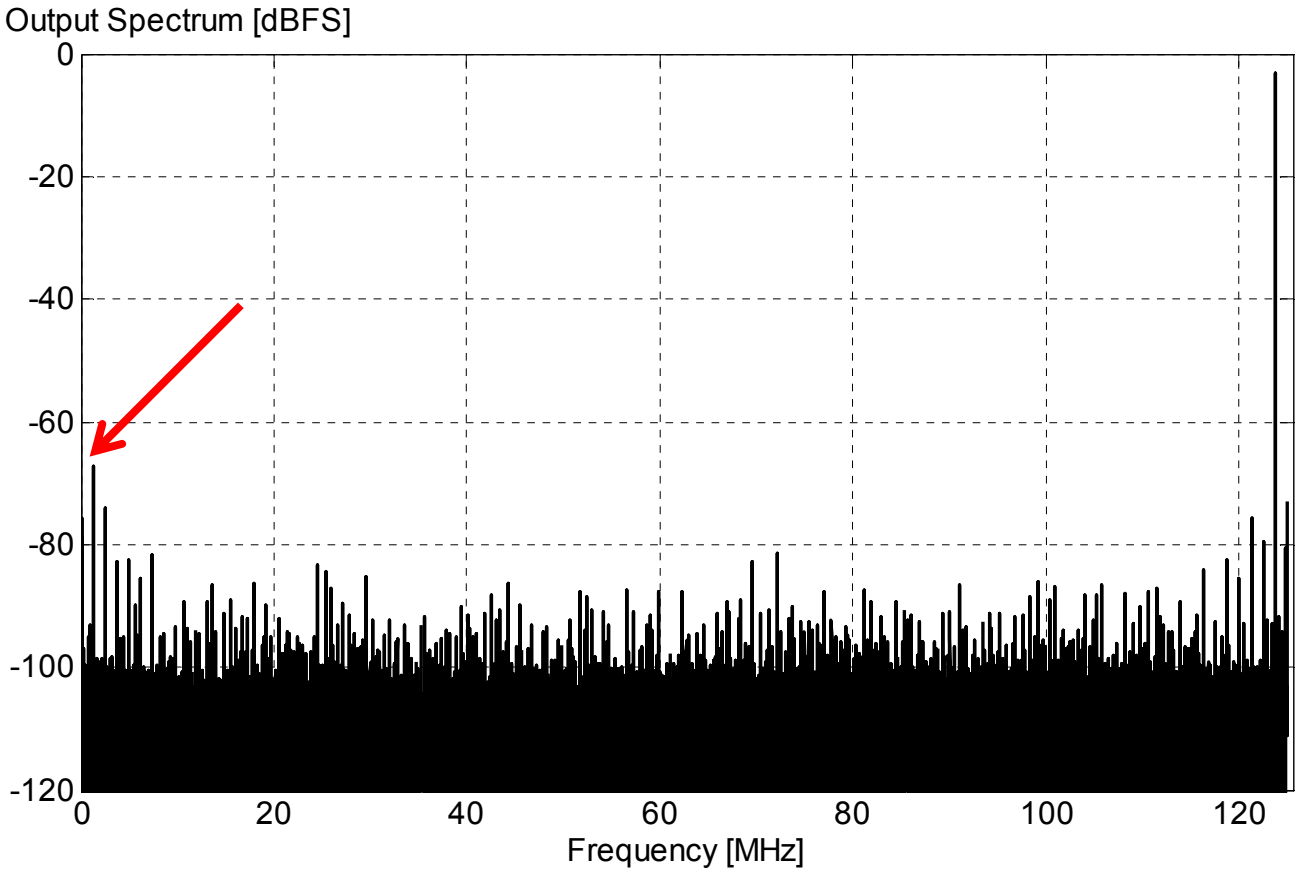
Dynamic performance at 250 MS/s



$SNDR_{max}$ = 59dB ERBW = 126 MHz

P = 1.7 mW

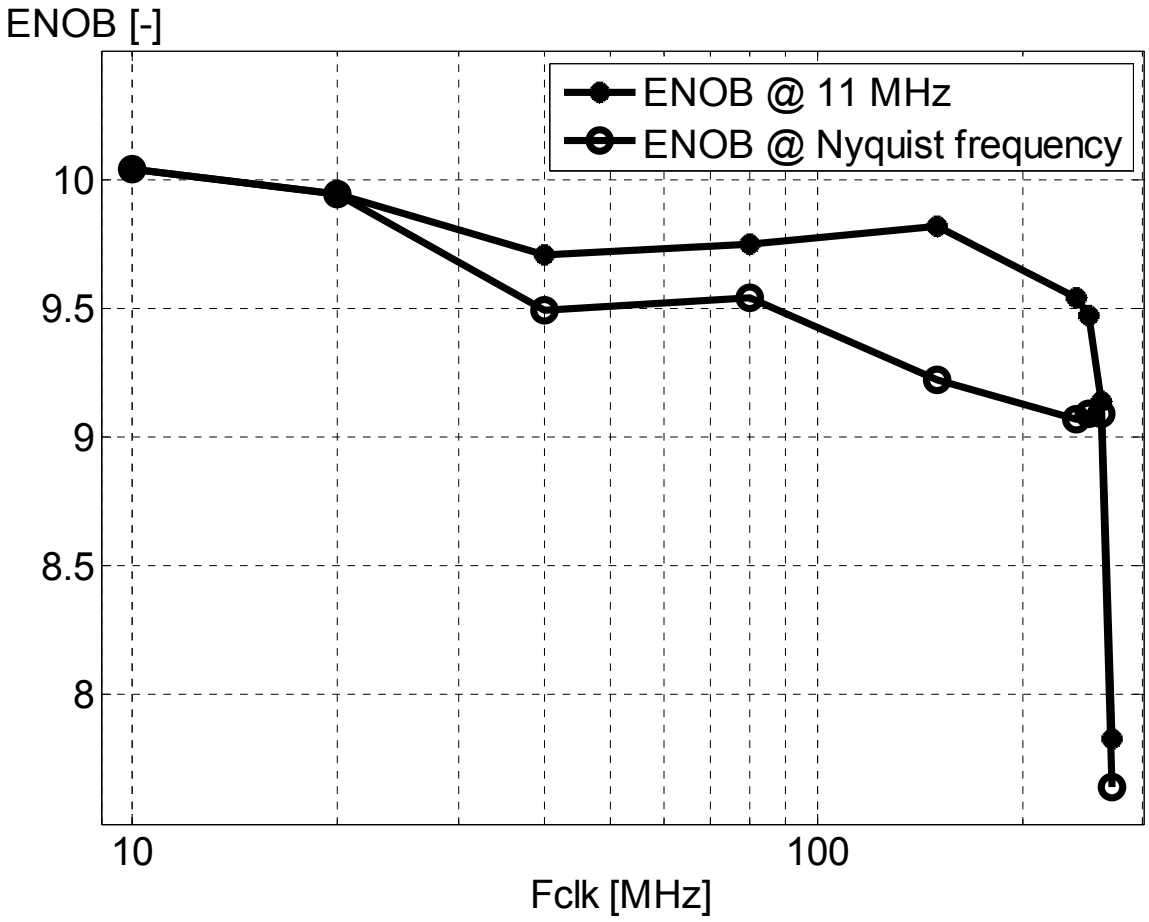
High frequency SFDR limited by time constant mismatch



Fclk = 250 MS/s Fin = 126 MHz

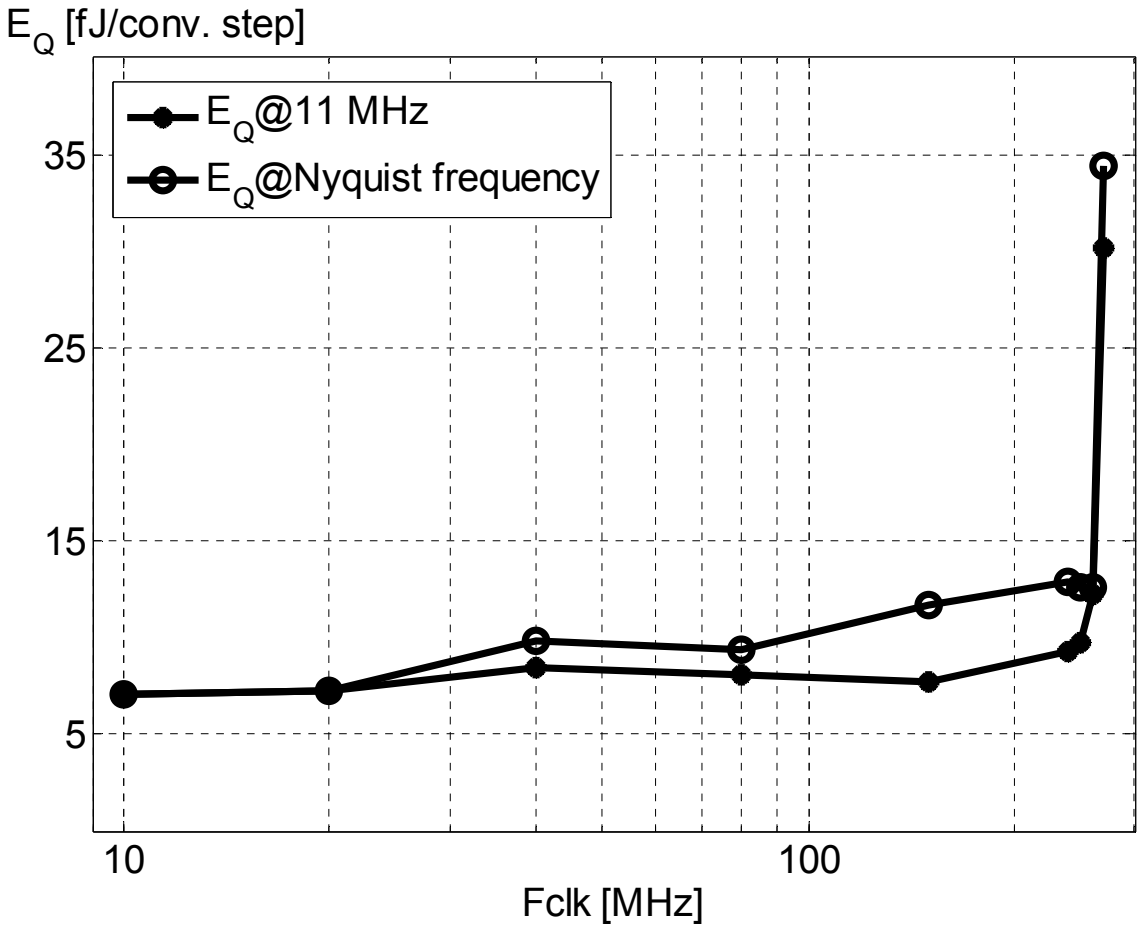
SNDR = 56.5 dB SFDR = 64.3 dB

ENOB vs. F_{clk}

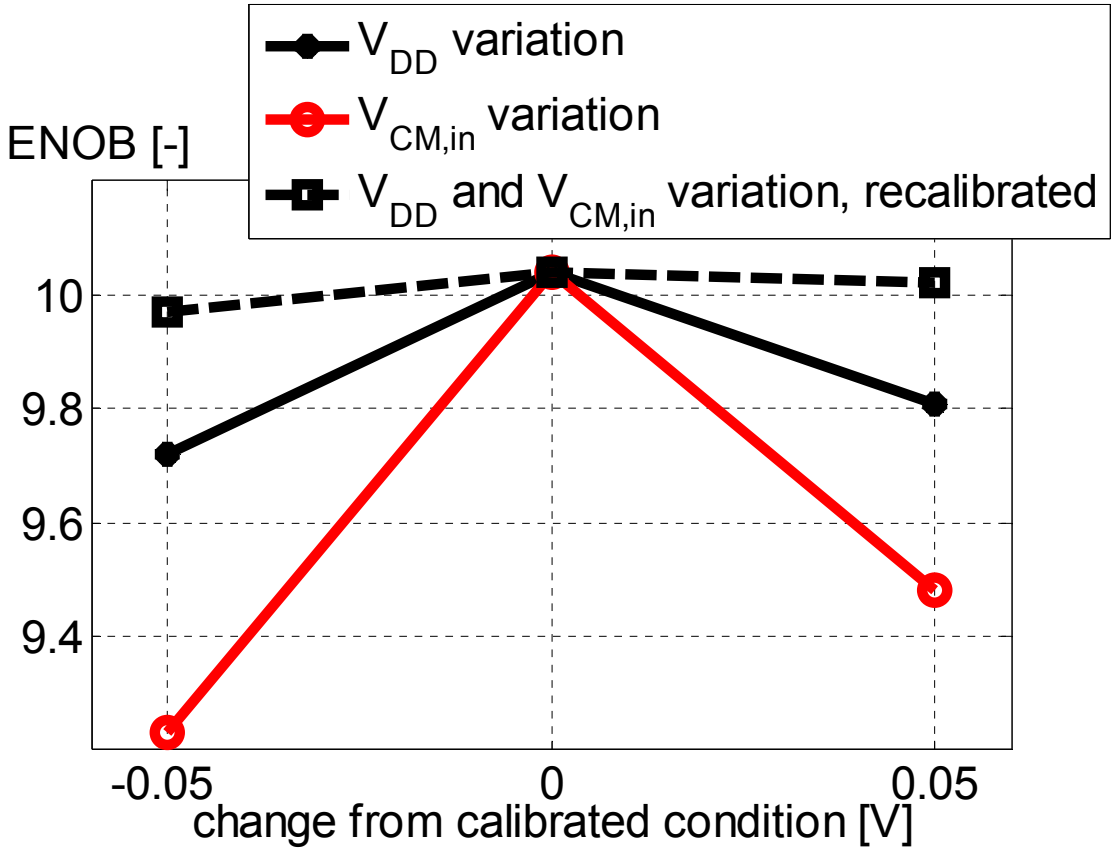


Dynamic power = 6.9 pJ/conversion

➔ E_Q < 13 fJ/c.s. @ Nyquist



Calibration sensitive to supply and common-mode input



Original calibration at V_{DD} = 1.1 V, $V_{CM,in}$ = 0.5 V

F_{clk} = 10 MHz F_{in} = 11 MHz

© 2012 IEEE

Performance summary

Technology	1.1 V 40nm LP CMOS	
Area	0.066 mm^2 (core) 0.78 mm^2 (incl. IO)	
Speed	10 MS/s	250 MS/s
$SNDR_{max}$	62 dB	58.8 dB
$SNDR^*_{min}$	62 dB	56.5 dB
ERBW	65 MHz	126 MHz
Power consumption	6.9 μW/MHz	
Input range	1.4 $V_{pp,diff}$	
Input capacitance	1 pF	

*in Nyquist bandwidth

State of the art comparison

Source	Speed (MS/s)	ENOB	Energy/c.s. (fJ)	Technology (nm)
Verma (ISSCC'09)	500	9	300	90
Liu (ISSCC'10)	100	9.5	15	65
Jeon (CICC'10)	204	8.9	95	65
Mulder (ISSCC'11)	800	9.5	180	40
This work	250	9.5	10	40

Conclusion

- Controller-less, step-down DAC SARs allow low power at high speed
- Dynamic amplifier achieves fast settling at low power with limited output range
- Shorted input calibration enables lower power consumption
- Measurements show state of the art performance