Comparative analysis of two operational amplifier topologies for a 40MS/s 12-bit pipelined ADC in 0.35μm CMOS

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***Abstract*— This paper describes a comparative analysis between two topologies of operational amplifiers to design a 40 MS/s 12-Bit pipeline analog to digital converter (ADC). The analysis includes AC and transient simulation to select the proper topology. This ADC is implemented in a 0.35μm AMS CMOS technology with 3.3V single power supply. The capacitors and selected operational amplifiers were scaled for low power dissipation. All analog components of this pipeline ADC are fully differential, as there are dynamic comparators, analog multiplexers and operational amplifiers with gain boosting.**

Index Terms digital: ADC, pipeline, CMOS, operational amplifier.

I. Introduction

Today, high performance analog to digital converters are a key element for the development of high performance mixed signal systems like image sensors. In the last years designers are developing analog to digital converters to achieve higher conversion speeds while reducing power consumption. This is special important for portable devices, a growing up sector in current user electronics. In fact the global performance of many integrated applications is limited by the performance of the ADC. Pipelined ADCs are a popular architecture for high-speed data conversion (10-100 MS/s) at medium to high resolution (8-14 bits). Within this architecture, residue amplifiers are known to dominate power dissipation due to the simultaneous demand for low noise, high speed, and precise linear amplification. This is especially true for the amplifiers in the first few-stages of the pipeline, which have the greatest impact on the ADCs overall performance. In this paper, we have compared two topologies of operational amplifier (Opamp) using transient and AC simulations. The topology that reached the best performances was used to design a 40 MS/s 12-Bit Pipelined ADC whose measured results are shown in the last section. Besides of this comparison, several techniques have been developed to reduce the power dissipation. Basic low-power design approaches include stage scaling [1] and optimization of the per-stage resolution [2] [3] and an optimal topology of the operational amplifier. The rest of the paper is organised as follows. In section II we explain the ADC architecture. A comparison between the opamps is described in section III. In section IV measurement results of the implemented ADC are shown. Finally we conclude in section V.

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II. ADC ARCHITECTURE

The topology of this pipeline ADC is based on a conversion of 1.5 effective bit per stage, whose diagram is shown in Fig. 1. Process and circuit non idealities affect the transfer characteristic which result in a conversion factor different from two. These non-idealities include capacitor mismatches, offsets, etc. There are two possibilities to circumvent this. The first is to set the factor A_V to a nominal value smaller than 2, and the second is to increase redundancy by choosing 1.5 bit/stage [4]. The pipeline consists of 11 stages. Each one of the first ten stages performs a 2 bit quantization.

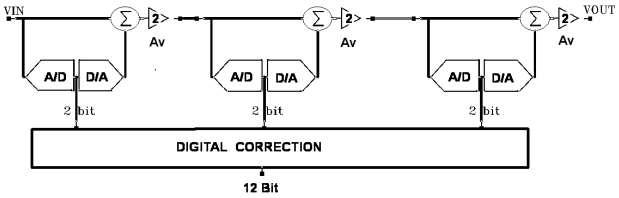

Fig. 1. Block diagram of the pipeline ADC.

A digital to analog conversion of the quantization result is done by a fully differential analog multiplexer with 3 levels of selection. Subtraction of the reference voltages and amplification of the residue by a factor of two completes the stage [5] [6]. In Fig. 2, the detailed configuration is shown. The output residue voltage is given by:

$$V_{OUT} = \begin{cases} 2V_{in} + V_{ref} & if \quad V_{in} < -V_{ref}/4 \\ 2V_{in} & if \quad (-V_{ref}/4 < V_{in} < V_{ref}/4) \\ 2V_{in} - V_{ref} & if \quad (V_{in} > -V_{ref}/4) \end{cases} \tag{1}$$

The converter works in two semicycles. In the first semicycle, the input signal is applied, the four capacitors are simultaneously charged to $VIN = (INP - INN)$. Comparators quantize the signal with two bits of resolution. The outputs of the comparators are connected to the inputs of the analog multiplexer which provide 3 voltage levels whose values used are $+V_{ref}$, 0, $-V_{ref}$.

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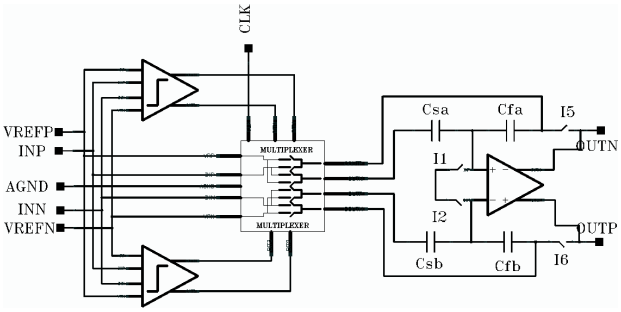

Fig. 2. Differential block diagram of a 1.5 bit converter stage.

In the second semicycle the subtraction is done by connecting the bottom plate of each capacitor to the output of analog multiplexer with the values $+V_{ref} = (V_{REFP} - V_{REFN})$, $0 = (AGND - AGND)$, $-V_{ref} = (V_{REFN} - V_{REFP})$ and the operational amplifier passes the residue to the next stage which amplifies with a factor of two. The transfer function is given by:

$$Vout = \left(1 + \frac{Csa}{Cfa}\right) VIN_{(Sampled)} + \frac{Csa}{Cfa} V_{ref} \qquad (2)$$

III. Comparative Analysis of Operational Amplifiers

The operational amplifier is the most design-challenging part of the ADC. We have compared two topologies of operational amplifiers, which are shown in Fig. 3:

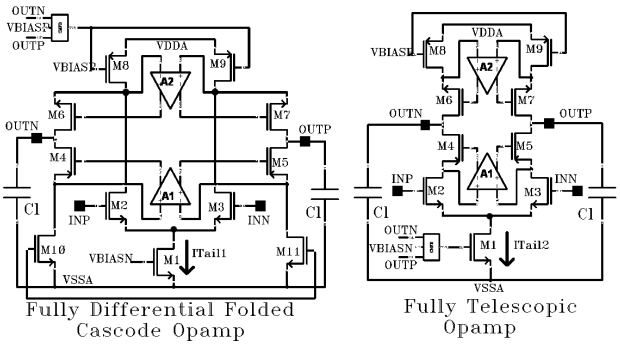

Fig. 3. Schematics of fully differential and telescopic opamps with gain boosting and common-mode feedback.

The topologies correspond to a fully differential telescopic [7] and a fully differential folded-cascode [8] opamp both with gain boosting. The performance and topology of the operational amplifier is defined by the required specifications for the first pipeline stage of the 40 MS/s 12 bit ADC. To achieve an amplification accuracy of less than 1/2 LSB it requires that the output settles to 0.012% in a semicycle (12.5 ns) [10]. To carry out the comparison among both operational amplifier topologies, they have been designed with identical power consumption and we have tried to maximize their performances separately. The architecture with the best results has been redesigned in the remaining stages according to the size of capacitors and the required resolution.

A. Fully Differential Telescopic with gain boosting and common-mode feedback switched capacitor circuit (CMFB)

The gain-enhanced telescopic topology was chosen because it shows a high DC-Gain [7], a high united gain bandwidth and a fast settling. However, the five levels of transistors from VDDA to VSSA reduce the output dynamic range, making the design of an ADC with a high dynamic differential input range of 1.5 Vpp Differential and 3.3 Voltage Supply critical. Transistor M_1 is used to set the tail current (I_{Tail2}) which is defined by the slew-rate (SR) and capacitance load C_L.The other parameters g_{mi} and r_{oi} are the device small-signal transconductance and output resistance respectively. The slew rate and output resistance (R_{out}) in small-signal of this operational amplifier are given by:

$$\text{SR} = \frac{I_{Tail2}}{C_l} \qquad (3)$$

$$R_{out} = A_1\ g_{m4}\ r_{o2}\ r_{o4} || A_2\ g_{m6}\ r_{o6}\ r_{o8} \qquad (4)$$

B. Fully Differential Folded-Cascode with gain boosting and common-mode feedback switched capacitor circuit (CMFB)

Although the dynamic behavior of the gain-enhanced folded-cascode topology is worse than the telescopic opamp [8] [9], the four levels transistors increase the output dynamic range and it could make the design more robust. In this case, the tail current (I_{Tail1}), SR, R_{OUT} depend on the following equations:

$$\text{SR} = \frac{I_{Tail1}}{C_l} \qquad (5)$$

$$R_{out} = A_1\ g_{m4}\ r_{o10}\ r_{o4} || A_2\ g_{m6}\ r_{o6}\ r_{o8} \qquad (6)$$

C. Simulation Results

Transient and AC simulations were done to compare performance of both topologies. Because of one of the opamps would be used in pipeline ADC, the test transient circuit has been adapted to the operation conditions of the opamps. Fig. 4 shows the test circuit used for transient simulations. In this configuration, the load of the operational amplifiers are switched capacitors circuits used in the ADC, where the value of each capacitors is 1.4 pF.

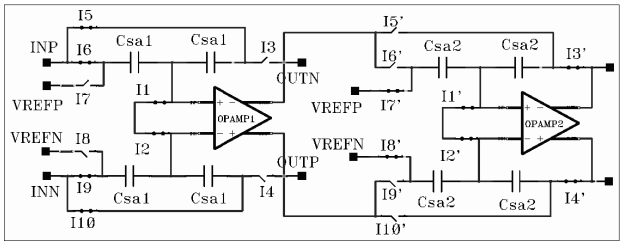

Fig. 4. Test circuit for transient simulation of the settling time in a pipeline stage for both OTAs.

The results of these simulations are shown in Fig. 5, where we can see the input signal (VIN), the output signal of the

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telescopic opamp (VOUT_T) and the folded cascode opamp (VOUT_F), as well as several clock signals (I7, I8, I3 and I4) to control the test circuit. The SR is clearly better when a telescopic opamp configuration is used although the circuit works at the maximum dynamic range (3 Vpp).

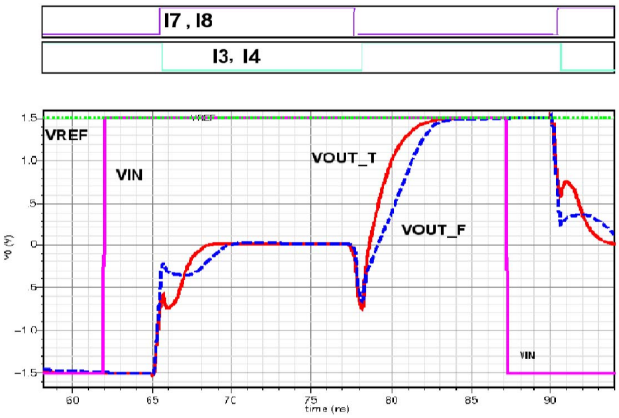

Fig. 5. Transient simulations.

Corner simulations (Fig. 6) were done to test the behavior of the output signal of the telescopic opamp (VOUT_T) using the recommended values of AustriaMicrosystem (AMS) for the technology C35B4.

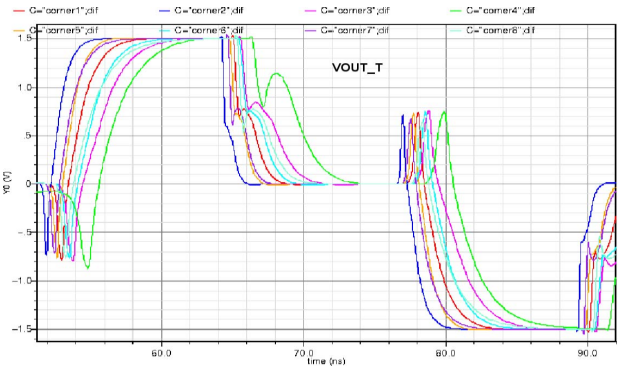

Fig. 6. Corner simulations.

The stability of the opamps, bandwidth and DC-Gain of these architectures are evaluated through AC Simulations. The frequency responses of both topologies are shown in Fig. 7. The telescopic topology reaches better results in phase margin and bandwidth than the folded cascode when an identical power and capacitance load (C_L) are used. Comparison results among both topologies are summarized in Table I.

We know that a 12-Bit ADC requires an opamp with a dc-gain $>$ 84.3 dB and unity gain frequency $>$ 114.73 MHz [10]. Both topologies exceed both specifications with similar power consumption. However, the telescopic topology reduces the required settling time to reach the specifications of the ADC. We can conclude that with a dynamic range of 1.5 Vpp Differential, telescopic topology allows to fit the specifications of the ADC with less power. Every stage of the pipeline converter has been designed using this topology but scaling the power dissipation according to the capacitance load and the required linearity. Other important design specifications are

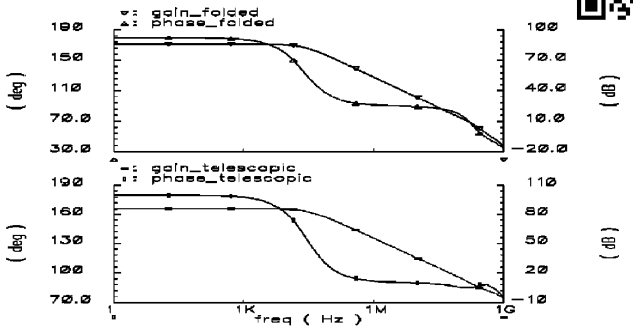

Fig. 7. Opamp frequency and phase response.

TABLE I
SIMULATION RESULTS

Opamp Specification	Telescopic	Folded-Cascoded
DC Gain (dB)	86.4	85.9
GBW (MHz)	570	350
PM (degree)	85.6	56
SR (V/us) Close Loop	832	472
C_l(pf)	1.4	1.4
0.012% Settling (ns)	8.6	14.3
Current (mA)	4.8	4.8
Input/Output Common Mode (V)	1.2 / 1.8	1.65 / 1.65
Power Supply (V)	3.3	3.3

the input and output dc-levels of the telescopic opamp. These dc-levels have been added to the reference voltage circuit to allow the correct working of the ADC.

IV. MEASUREMENTS AND RESULTS

A prototype of the ADC has been fabricated in a 350-nm 2-poly 3-metal AMS CMOS technology which occupies an active area of 2.54mm x 2.26mm (Fig. 8). This size is mainly due to the technology employed and to the high value of the capacitors used for the integrated voltage sources. The supply voltage is 3.3 V for all analog and digital circuits. The dynamic range of the ADC is 1.5 Vpp Differential and the DC voltage is 1.8V. All clock signals are internally generated by a timing circuit to implement the sycronization between digital and analog blocks.

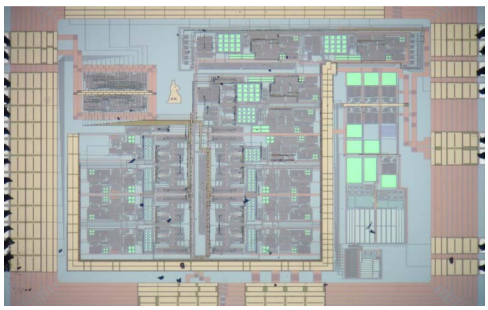

Fig. 8. Chip microphotograph of the ADC.

A discrete fourier transform (DFT) of ADC is shown in Fig. 9 for a sampling rate (f_s) of 40 MS/s and input frequency (f_{in})

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of 2.8 MHz.

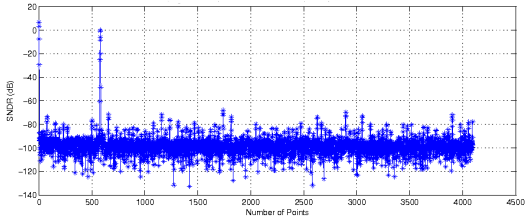

Fig. 9. DFT: Sampling Rate 40MS/s and Input Frequency 2.8MHz.

Fig. 10 shows the measured signal-to-noise and distortion ratio (SNDR) versus input frequency when f_s is 40 MS/s. Finally, SNDR versus sampling rate is shown in Fig. 11 for f_{in} of 1.4 MHz. The measured SNDR is 59.7 dB for a f_s of 40 MS/s and for a f_{in} of 2.8 MHz and the corresponding effective number of bits (ENOB) is 9.63 bits.

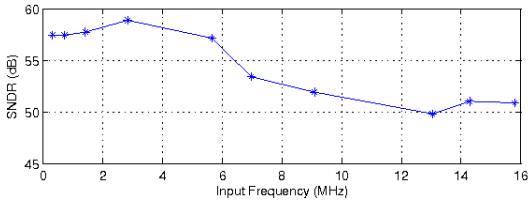

Fig. 10. SNDR vs Input Frequenct at Sampling Rate of 40MS/s.

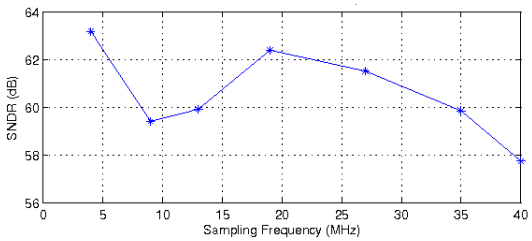

Fig. 11. SNR vs Sampling Rate at Input Frequency of 1.4MHz

The differential nonlinearity (DNL) and integral nonlinearity (INL) are within +1.2/-097 and +3.8/-4.8 LSB for a f_s of 40 MS/s and a f_{in} of 1.4 MHz. DNL and INL are represented in Fig. 12. Table II shows the values of SNR, total Harmonic Distortion (THD), analog power, DNL, INL, input common mode and area of this ADC.

V. Conclusions

This paper describes a comparative analisys of two opamps for a 12 bit, 40 MS/s, pipeline ADC. It was implemented in 0.35 μm CMOS technology. Because of the ADC has not Sample and Hold stage, SNDR is reduced when the input frequency is increased. However, if the input frequency is lower than $<$ 2 MHz, SNDR shows good results in a wide range of sampling rates. For this reason, in the next project phase new topologies of Sample and Hold will be tested to improve the bandwidth of ADC. Moreover an optimized analog pipeline block with opamp sharing topology will be

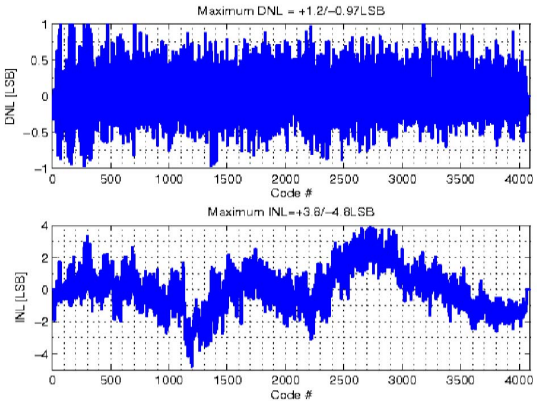

Fig. 12. DNL and INL at 40 MS/s and f_{in}=1.4 MHz.

tested to reduce the power keeping and improving SNDR values.

TABLE II
Measured Results

Process	CMOS C35B4 for 3.3V
SNDR(dB) at 40 MS/s	58
THD (dB) at 40 MS/s	-64.9
Analog Power(mW)	132
DNL(LSB)	+1.2/-0.97
INL(LSB)	+3.8/-4.8
Area(mm^2)	5.74
Input common mode(V)	1.8
Voltage Supply(V)	3.3

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