Gaetano Palumbo and
Domenico Pappalardo

Abstract

Due to the continuous power supply reduction, charge pumps circuits are widely used in integrated circuits (ICs) devoted to several kind of applications such as smart power, nonvolatile memories, switched capacitor circuits, operational amplifiers, voltage regulators, SRAMs, LCD drivers, piezoelectric actuators, RF antenna switch controllers, etc.

The main focus of this tutorial manuscript is to provide a deep understanding of the charge pumps behavior, to present useful models and key parameters and to organically and in details discuss the optimized design strategies. Finally, an overview of the main different topologies is also included.

Charge Pump Circuits: An Overview on Design Strategies and Topologies

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I. Introduction

A Charge Pump (CP) is an electronic circuit that converts the supply voltage V_{DD} to a DC output voltage V_{Out} that is several times higher than V_{DD} (i.e., it is a DC-DC converter whose input voltage is lower than the output one). Unlike the other traditional DC-DC converters, which employ inductors, CPs are only made of capacitors and switches (or diodes), thereby allowing integration on silicon [1]–[2]. CPs were originally used in smart power ICs [3]–[6] and nonvolatile memories [7]–[13] and, given the continuous scaling down of ICs power supplies, they have also been employed in a vast variety of integrated systems such as switched capacitor circuits, operational amplifiers, voltage regulators, SRAMs, LCD drivers, piezoelectric actuators, RF antenna switch controllers, etc. [14]–[24].

In this overview, after a brief introduction of the CP behavior reported in Section II (which also includes an original perspective that makes use of the CP nodes voltages), models, design strategies and CP topologies are discussed.

The CP parameters and analytical models, which are presented in Section III, represent the background to the optimized CP design strategies that follow.

In current applications, CPs may be either loaded by a simple capacitor (or equivalently the gate of a MOS transistor) or by complex electronic circuits. In the last case the CP load can be simply modeled by means of an equivalent capacitance and an equivalent current generator whose value is given by the load current. Thus, both design strategies considering a current load or a pure capacitive load are treated in Section IV and V, respectively. Note that a current generator can also be used to model a pure resistive load. Moreover, the discussed design strategies refer to the main CP topologies evolved from the Dickson CP [1] (the first used in an IC), but they are not suitable for series-parallel CPs or Fibonacci-like CP topologies.

Finally, the main CP topologies are briefly presented and critically discussed in Section VI.

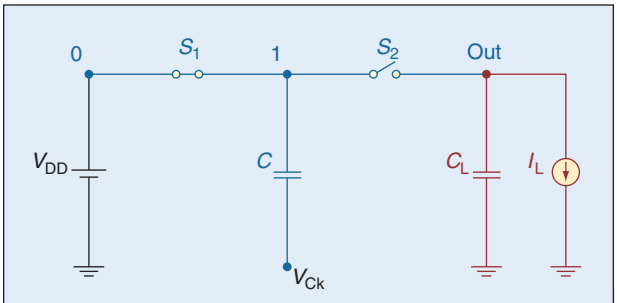

Figure 1. Ideal one-stage CP.

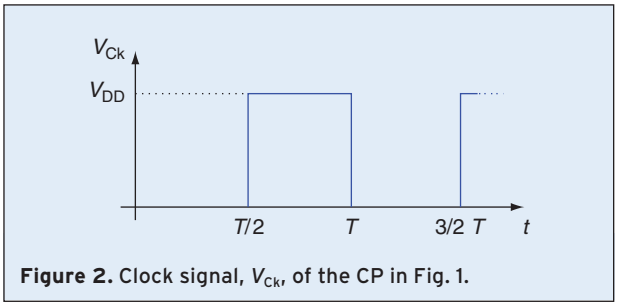

Figure 2. Clock signal, V_{Ck}, of the CP in Fig. 1.

II. Charge Pump Simplified Analysis

a) One-stage Charge Pump

To show the behavior of an ideal CP, let us consider the one-stage topology in Fig. 1, which comprises a single pumping capacitance, C, two switches, S_1 and S_2 (driven by two complementary phases), a clock signal whose amplitude is equal to the power supply V_{DD} (Fig. 2), and a load represented by a current generator I_L and a capacitor C_L (also referred to as the bulk capacitor).

During the first half period (0 to $T/2$), S_1 and S_2 are respectively closed and open and C, being connected to

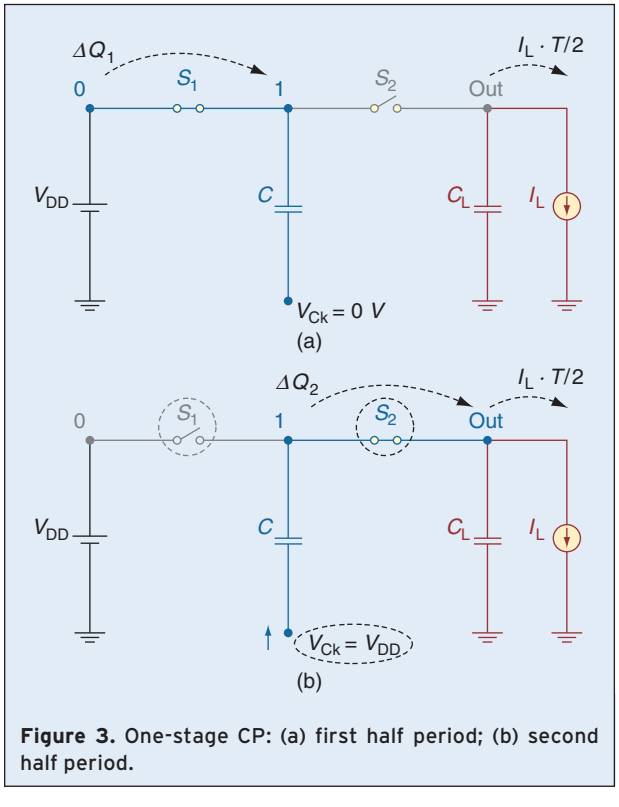

Figure 3. One-stage CP: (a) first half period; (b) second half period.

Gaetano Palumbo (IEEE Fellow) and Domenico Pappalardo are with Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi (DIEES), Universitá di Catania, Viale Andrea Doria 6, I-95125, Catania, Italy.

the power supply, is charged to V_{DD} (Fig. 3a), while the output node is discharged by the current load, I_L, which sinks a charge $I_L T/2$.

In the second half period ($T/2$ *to* T), the switches change their state (see Fig. 3b), the clock signal now equals V_{DD}, thus part of the charge stored in C is transferred both to the capacitive load, C_L, and, for an amount of $I_L T/2$, to the current load. Hence, as shown in the Appendix, at each cycle the output voltage will increase up to the final asymptotic value, equal to

$$V_{Out}|_{Steady\ State} = 2V_{DD} - \frac{I_L \cdot T}{C}. \qquad (1)$$

Several cycles are needed to approach the asymptotic value and, as shown in Fig. 4 where the output voltage of a one-stage charge pump is plotted, the step increment of the output voltage in each successive clock period becomes smaller. Indeed, the output voltage will steeply increase in the first part of the transient and will slowly tend to its final value.

In conclusion, according to its name, a CP takes charges from the power supply via the capacitor C, pumps these charges into the output load and, thanks to the output capacitor C_L, allows to increase the output voltage up to an ideal value that, except for the loss due to the current load, is twice the power supply.

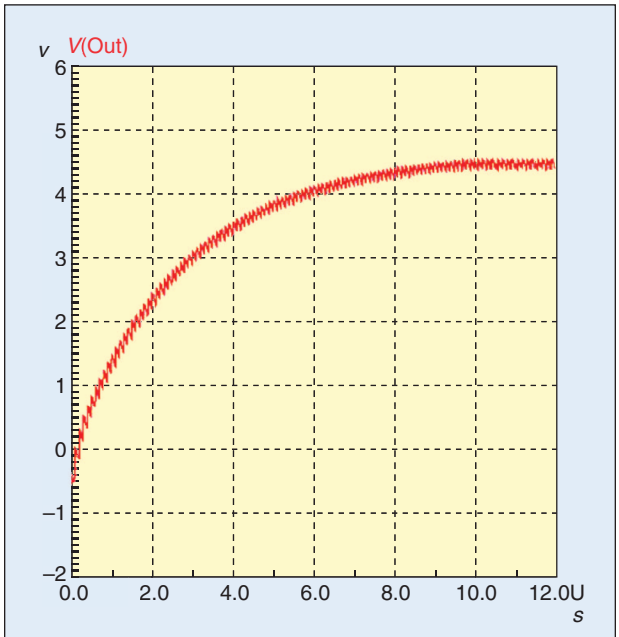

Figure 4. Output voltage of the one stage charge pump.

b) N-Stage Charge Pump

The one-stage CP topology can be generalized by including additional cascaded stages as shown in Fig. 5, where a generic N-stage CP is depicted. Each stage is made of a pumping capacitor C and a switch S_i. Moreover, the N-stage CP needs a two-phase clock and, to properly connect the output load to the final stage, switch S_{Out} is also required.

The behavior of the N-stage CP is similar to that of a one-stage CP. During the first half clock period, V_{Ck} is low and only the odd switches are closed. The first pumping capacitor is thus charged to V_{DD} and all the other pumping capacitors in the odd stages receive the charge from the capacitor of the previous stage (this happens also for the load capacitor if the number of stages is even).

During the subsequent half clock period, the signal V_{Ck} is equal to V_{DD} and only the even switches are closed. Now all the capacitors in the odd stages give the charge to the capacitor in the subsequent stage (the load capacitor is maintained separated from the CP if the number of stages is even, since the switch S_{Out} is open).

In summary, in a complete clock period, each CP capacitor receives an amount of charge from the capacitor at its left side and gives a part of this charge to the capacitor at its right side. Thus, in each period there is a charge transfer from the power supply to the output load. In particular, the amount of charge exchanged in each half period between two adjacent capacitors is equal to $I_L T$ (which can be assumed constant under a constant current load), given that, in the steady state, a CP has to provide such an amount of charge in each time period.

Consider for example a two-stage CP with a current load, as shown in Fig. 6. During the first half period (in the steady state), the first capacitor is connected to the power supply, and is recharged by ΔQ, which is the same amount of charge provided by the CP to the output (Fig. 6b). In the next half period, when the first and the second pumping capacitors are

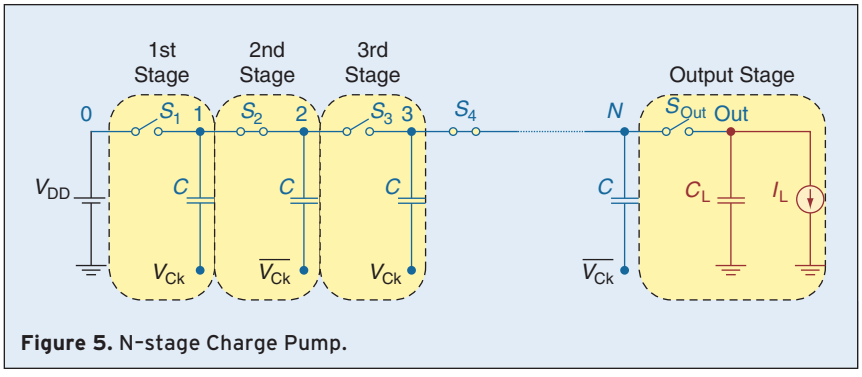

Figure 5. N-stage Charge Pump.

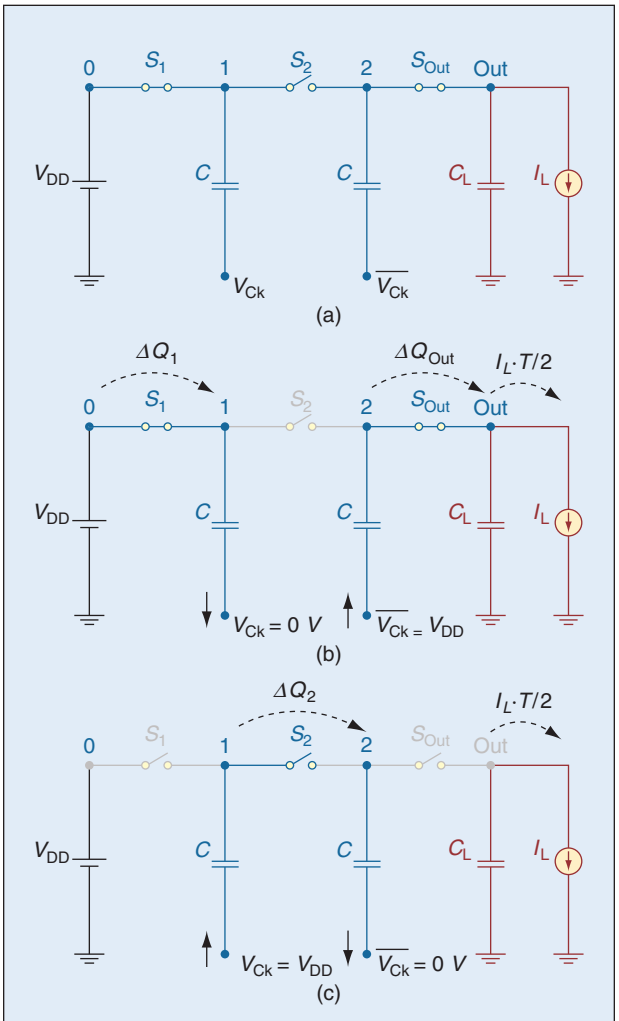

Figure 6. Two-stage CP: (a) topology; (b) first half period; (c) second half period.

connected together (Fig. 6c) since switch S_2 is closed, they exchange the same amount of charge, ΔQ, and the highest node voltage results to be

$$V_1|_{V_{Ck}=V_{DD}} = V_2|_{\overline{V_{Ck}}=0V} = V_1|_{V_{Ck}=0V} + V_{Ck} - \frac{I_L \cdot T}{C} = 2 \cdot V_{DD} - \frac{I_L \cdot T}{C}. \tag{2}$$

Finally, in the subsequent first half period, when the switches S_1 and S_{Out} are closed (Fig. 6b), the output voltage is

$$V_{Out} = V_2|_{\overline{V_{Ck}}=V_{DD}} = V_2|_{\overline{V_{Ck}}=0V} + V_{Ck} - \frac{I_L \cdot T}{C} = 3 \cdot V_{DD} - 2\frac{I_L \cdot T}{C}. \tag{3}$$

Extending the reasoning to an N-stage CP, we get the well known output voltage asymptotic value

$$V_{Out}|_{Steady\ State} = (N+1)V_{DD} - N\frac{I_L \cdot T}{C}. \tag{4}$$

It is worth noting that, when switches close, assuming them almost ideal the charge transfer occurs in a very short time (ideally zero). Thus, when S_{Out} closes, the output voltage suddenly reach its maximum value and then, due to the presence of the current load I_L, during all the time period it slightly decreases. This effect results in an output voltage ripple, V_r, which, assuming the charge pump capacitor C much smaller than the load capacitor, is equal to

$$V_r = \frac{I_L \cdot T}{C_L}. \tag{5}$$

c) Voltages in a Charge Pump Nodes

Since the voltages in the CP nodes are higher than the power supply, to evaluate the voltage stress on each CP component, it is useful to compute the voltage on each CP node and across each switch. At this purpose, let us consider the voltage at the generic node j and analyze its value at the beginning and at the end of each half period. Without loss of generality, we can assume that in the first half period the capacitor of the stage j (with the clock signal low) is connected with the previous stage through the closed switch S_j. Hence, during this half period, it receives a charge ΔQ from the capacitor in the stage $(j-1)$. Representing with ΔV the voltage variation on the charge pump capacitors due to the charge transfer ΔQ, the voltage at the beginning of this half period is

$$V_{i,start-left-sharing} = j(V_{DD} - \Delta V) \tag{6}$$

and at the end of the half period it is

$$V_{i,end-left-sharing} = j(V_{DD} - \Delta V) + \Delta V. \tag{7}$$

During the subsequent half period, when switch S_j is open and switch S_{j+1} is closed, the clock signal driving the stage j is high (i.e., there is a charge sharing with the capacitor in the stage $j+1$), and the voltage at the beginning of the half period is

$$V_{i,start-right-sharing} = j(V_{DD} - \Delta V) + \Delta V + V_{DD} \tag{8}$$

and at the end of the half period it is

$$V_{i,end-right-sharing} = j(V_{DD} - \Delta V) + V_{DD}. \tag{9}$$

Let us consider the switch S_j, which connects capacitors at nodes $j-1$ and j, and evaluate the voltage across it, $V_{j,j-1} = V_j - V_{j-1}$. This voltage behavior is plotted in Fig. 7.

At the end of the first half period S_j is closed and consequently the voltage across the switch is zero (point 2 in Fig. 7). At the beginning of the subsequent half period (S_j open) the clock signal changes and the voltages at nodes j and $j-1$ fall and rise, respectively, by the clock amplitude. Hence, the voltage across the switch results to be $V_{j,j-1} = 2V_{DD}$ (point 3 in Fig. 7). At the end of this half period, the capacitor at node $j\,(j-1)$ gives (receives) charge ΔQ. Thus, as seen from point 4 in Fig. 7, the voltage at node $j\,(j-1)$ reduces (increases) of ΔV and $V_{j,j-1} = 2V_{DD} - 2\Delta V$. Finally, when S_j is closed again and the charge transfer between capacitors at nodes $j-1$ and j begins, the clock signal changes, and the voltage across the switch is $V_{j,j-1} = -2\Delta V$ (point 1 in Fig. 7).

These voltage values are equal for all the CP switches, and are summarized in Table 1.

It is worth noting that the voltage across the switches depends on the clock amplitude (assumed, as usual, equal to the power supply) and on the voltage step, ΔV, which is given by

$$\Delta V = V_{DD} + \frac{V_{DD} - V_{Out}}{N}. \tag{10}$$

III. Charge Pump Parameters and Models

The most important design parameters of a CP are the number of stages, the silicon area occupation and the current consumption. Moreover, in the design of charge pumps with purely capacitive load, also the rise time and the charge consumption during the rise time are of importance. However, it is worth noting that even if the clock frequency may appear as a design parameter, it is usually set at the value of the clock used inside the system where the CP is used.

The **number of stages**, N, is strictly related to the required output voltage, V_{Out}, given by (4), which, in the case of a pure capacitive load, can be simplified into

$$V_{Out}\big|_{\text{Steady State}} = (N+1)\cdot V_{DD}. \tag{11}$$

To physically implement a CP, the required **total silicon area**, A_{Tot}, may be non negligible. Since this area occupation is mainly due to the capacitors, we can approximate A_{Tot} simply with the area required to implement the capacitors

$$A_{Tot} = k\cdot N\cdot C = k\cdot C_{Tot}, \tag{12}$$

where the parameter k depends on the process used to realize the capacitors and C_{Tot} is the sum of the pumping capacitors, $N\cdot C$.

Combining relationship (4) with (12), the area of CP in the case of a current load is given by

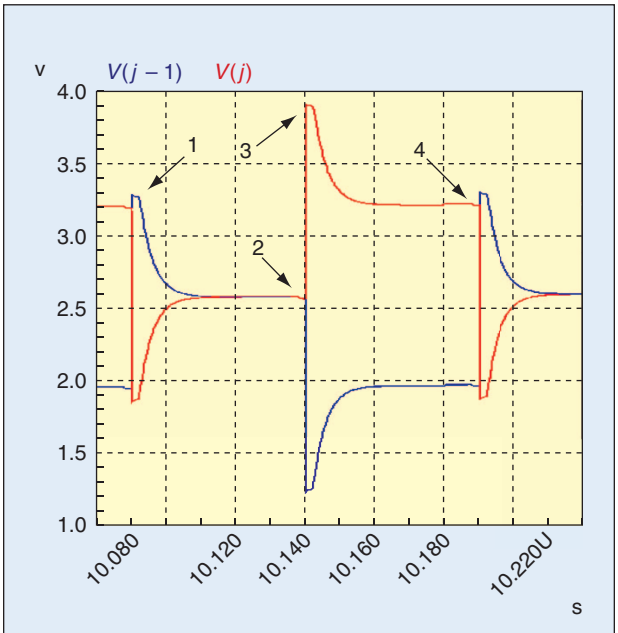

Figure 7. Voltage across switch S_j.

$$A_{Tot} = k\cdot\frac{N^2}{(N+1)\cdot V_{DD} - V_{Out}}\frac{I_L}{f}. \tag{13}$$

Thus, as expected, the CP area increases both increasing the load current and decreasing the CP frequency. Indeed, in both cases, to provide the required amount of charge, higher charge pump capacitors are needed. Moreover, as will be shown later when the optimum number of stages is evaluated, the CP area also increases with the increase of output voltage and with the reduction of the power supply. In particular, while a linear dependence on V_{Out} holds, a dependence $1/V_{DD}^2$ arises regarding the dependence on the power supply.

The **current consumption**, I_{VDD}, can be considered as constituted by two contributions [25]. A term due to the ideal CP behavior, I_{Id}, and a term that accounts for the parasitic effects, I_{Par}. Thus, we get

$$I_{VDD} = I_{Id} + I_{Par}. \tag{14}$$

Current I_{Id} can be evaluated by considering that the amount of charge, ΔQ, delivered to the load and provided

Table 1.
Switch voltages versus time.

Time	Switch Voltages $V_{j,j-1}$
Beginning S_j closed	$-2\Delta V$
End S_j closed	0 V
Beginning S_j open	$2V_{DD}$
End S_j open	$2V_{DD} - 2\Delta V$

by the power supply, is transferred in each period from one capacitor to another. Hence, I_{Id} results to

$$I_{Id} = (N+1)\cdot\frac{\Delta Q}{T} = (N+1)\cdot I_L. \tag{15}$$

The same result can be achieved by using the transformation factor of the CP. We amplify the power supply of an $N+1$ factor and, in an ideal case without energy waste (i.e., by transferring all the power taken from the power supply into the output load), the current sunk by the CP is $N+1$ times higher than the load current.

Since, in general, we can neglect the cross conduction currents that arise when two adjacent switches provide a conductive path during commutation, current I_{Par} is mainly due to the charge and discharge in each time period, T, of the total parasitic capacitance, C_P, i.e.

$$I_{Par} = N\frac{C_P V_{DD}}{T} = \alpha N C_{Tot} f V_{DD}, \tag{16}$$

where the bottom plate parasitic capacitance, C_P, is assumed proportional to the pumping capacitance C through a factor α.

Thus, from (15), (16) and using (4) to express the total pumping capacitance, the current consumption in the steady state is given by

$$I_{VDD} = \left[(N+1) + \alpha\cdot\frac{N^2}{(N+1)\cdot V_{DD} - V_{Out}}\cdot V_{DD}\right]\cdot I_L. \tag{17}$$

It is worth noting that the current consumption, and hence the power consumption, depends neither on the clock frequency nor on the total CP capacitance, but it is linearly related to the current load, I_L.

The **rise time**, t_r, which is the time required to achieve a defined output value $V_{Out}(t_r)$, is a parameter typically useful only for charge pump with purely capacitive load. Thus, by adopting the dynamic models of a CP with purely capacitive load developed in [26]–[29], the CP rise time can be approximated with the relationship

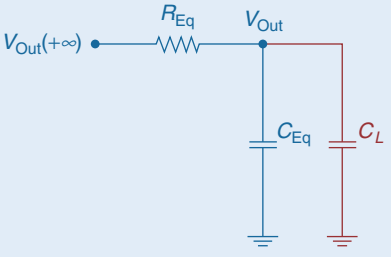

Figure 8. CP equivalent model.

$$t_r = T\cdot\left(N\frac{C_L}{C} + 0.3\,N + 0.6\right)\cdot\ln\left[\frac{(N+1)V_{DD} - V_{Out}(0)}{(N+1)V_{DD} - V_{Out}(t_r)}\right]. \tag{18}$$

Moreover, for N much higher than 1, and normalizing the output voltage to the power supply, i.e.

$$v_x = \frac{V_{Out}(t_r)}{V_{DD}} \tag{19}$$

$$v_{x0} = \frac{V_{Out}(0)}{V_{DD}} \tag{20}$$

we get

$$t_r = T\cdot N^2\cdot\frac{C_L + C_{Eq}}{C_{Tot}}\cdot\ln\left(\frac{N+1-v_{x0}}{N+1-v_x}\right), \tag{21}$$

where capacitance C_{Eq} is equal to $C_{Tot}/3$.

As expected, to reach the output steady state voltage, $(N+1)V_{DD}$, (21) anticipates an infinite rise time. Moreover, it is apparent that t_r is affected by the load capacitance and the total CP capacitance, C_{Tot}.

Since from (21) we can write

$$V_{Out}(t_r) = (N+1)V_{DD} - [(N+1)V_{DD} - V_{Out}(0)]\cdot e^{-\frac{t_r}{\frac{N(C_L+C_{Eq})}{Cf}}}, \tag{22}$$

the dynamic behavior of CP with purely capacitive load is equivalent to that of a simple RC circuit [27]. More specifically, the CP model is the RC circuit in Fig. 8 where

$$R_{Eq} = \frac{N}{C\cdot f} \tag{23}$$

and $V_{Out}(+\infty)$ is the output voltage in the steady state, given by (11).

Again, for CP with purely capacitive load, it may be useful to evaluate the **charge consumption**, which is only delivered by the power supply to the CP during its rise time, and can be divided into three main contributions

$$Q_T = Q_L + Q_{Pump} + Q_{Par}. \tag{24}$$

The charge Q_L is the contribution given to the load, the charge Q_{Pump} is required during the transient by the pumping capacitors, and the charge Q_{Par} is the contribution wasted in the parasitic elements shown in Fig. 9 (note that the parasitic capacitance at the bottom plate, C_P, is generally more than one order of magnitude higher than that of the other plate).

Taking into account the equivalent RC circuit in Fig. 8, we get

$$Q_L(t_r) + Q_{Pump}(t_r) = (N+1)\cdot(C_{Eq} + C_L)\cdot[V_{Out}(t_r) - V_{Out}(0)]. \tag{25}$$

During each clock period, the charge loss due to parasitic effects (required to charge and discharge the parasitic capacitances on the bottom plate of a pumping capacitor) can be modeled by NC_PV_{DD}, and the contribution during the rise time results to

$$Q_{Par} = NC_PV_{DD}\frac{t_r}{T} = \alpha C_{Tot}V_{DD}\frac{t_r}{T}, \quad (26)$$

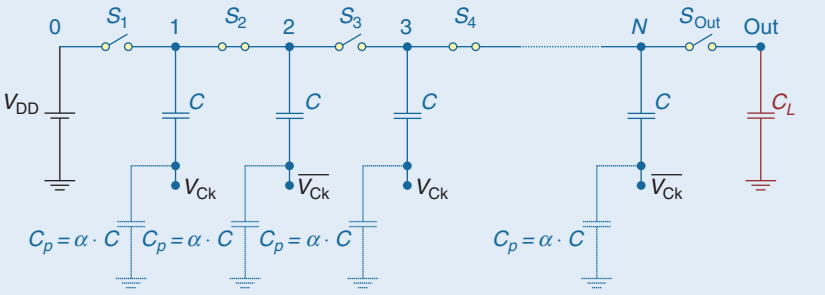

Figure 9. N-stage CP with parasitic effects.

where the bottom plate parasitic capacitance, C_P, is assumed proportional to the pumping capacitance C through a factor α.

Substituting each contribution into (24), we get the expression of the total charge sunk by the power supply up to the rise time

$$Q_T(t_r) = \left[(N+1)(v_x - v_{x0}) + \alpha N^2 \ln\frac{N+1-v_{x0}}{N+1-v_x}\right](C_{Eq}+C_L)\cdot V_{DD}. \quad (27)$$

IV. Charge Pump with a Current Load: Design Strategies

The design parameters involved in the design of a CP with a current load are summarized in Table 2. Among the unknown entries (highlighted in bold characters), two can be evaluated by using (13) and (17). We can start the CP design by finding parameter $N$and we can follow two possible strategies minimizing either the area or power consumption. Indeed, as shown in Fig. 10 (which exemplifies the case in which $V_{DD} = 1.35\ V$, $V_{Out} = 5\ V$, $f = 10$ MHz, $\alpha = 0.1$ and $I_L = 300\ \mu A$) area and current consumption are minimized for different values of N.

a) Area Occupation Minimization

To find the optimum N minimizing the silicon area, we must set to zero the derivative of (13) with respect to N. On the other hand, if we want to maximize the current provided to the load, we have to set to zero the derivative of current I_L evaluated from (4). In both cases, we get

$$\{2N\cdot[(N+1)\cdot V_{DD} - V_{Out}] - N^2\cdot V_{DD}\}\cdot\frac{I_L}{f} = 0, \quad (28)$$

which, solved for N, gives [30]

$$N_{Aopt} = 2\cdot\left(\frac{V_{Out}}{V_{DD}} - 1\right). \quad (29)$$

After solving (4) for C, one has

$$C = N\cdot\frac{I_L\cdot T}{(N+1)\cdot V_{DD} - V_{Out}} \quad (30)$$

and substituting N_{Aopt} in (30), we find the stage capacitor C.

b) Current (Power) Consumption Minimization

The optimum N that minimizes current consumption is obtained by setting to zero the derivative of (17) with respect to N

$$1 + \alpha\frac{N\cdot[(N+2)\cdot V_{DD} - 2\cdot V_{Out}]}{[(N+1)\cdot V_{DD} - V_{Out}]^2}\cdot V_{DD} = 0. \quad (31)$$

Hence, solving for N, we get [25]

$$N_{Iopt} = \left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right)\cdot\left(\frac{V_{Out}}{V_{DD}} - 1\right). \quad (32)$$

Finally, substituting the optimum value of (32) in (30), we get the required value of C for the optimized design.

c) Design Strategies Comparison

In order to compare the two considered design strategies, let us start evaluating the increase in area of the minimum power consumption design, compared to the minimum area design [25].

From (30) and using the values N_{Aop} and N_{Iop}, we obtain the CP total capacitance for minimization of area and power consumption, respectively

Table 2.
CP design parameters.

Parameter	Comment
V_{DD}	Technology dependent
I_{VDD}	**Not known a priori**
V_{Out}	Design constraint
I_{Out}	Design constraint
$f = 1/T$	System dependent
$C_{Tot} \propto A_{Tot}$	**Not known a priori**
N	**Not known a priori**
$\alpha = C_P/C$	Technology dependent

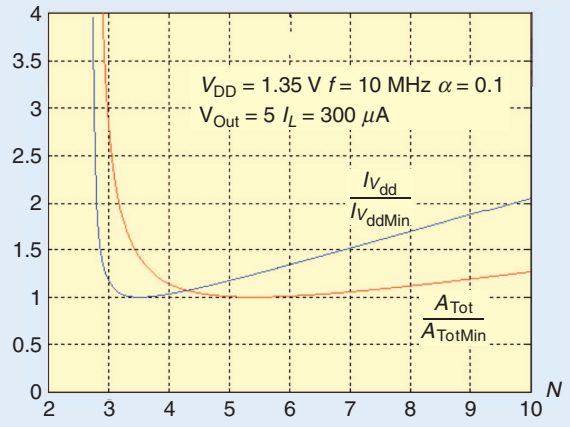

Figure 10. Current consumption and area normalized to their minimum values versus N.

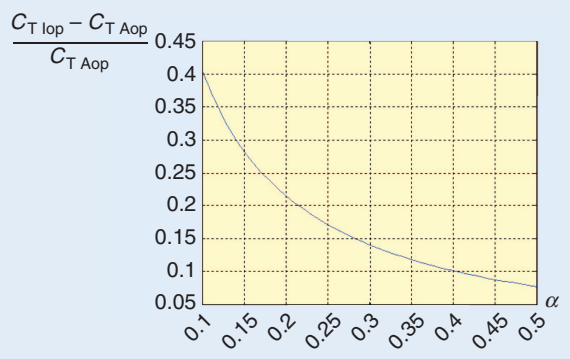

Figure 11. Increment of capacitance (i.e., area) in the case of power consumption optimization with respect the case of area minimization.

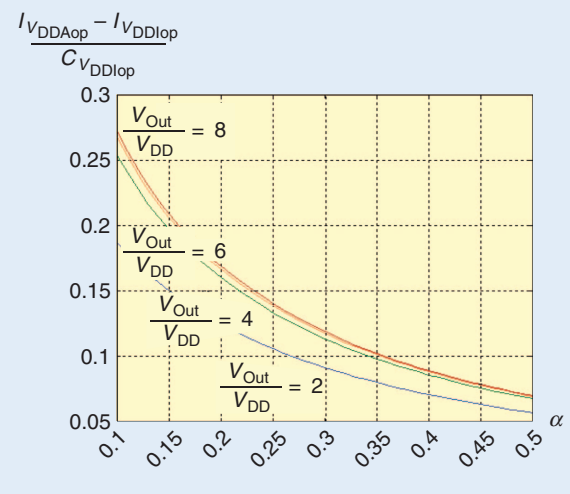

Figure 12. Increment of current consumption (i.e., power consumption) in the case of area minimization with respect the case of minimum current consumption.

$$C_{T,Aop} = 4\left(\frac{V_{Out}}{V_{DD}} - 1\right)\frac{I_L \cdot T}{V_{DD}} \tag{33}$$

$$C_{T,Iop} = \frac{\left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right)^2}{\sqrt{\frac{\alpha}{1+\alpha}}}\left(\frac{V_{Out}}{V_{DD}} - 1\right)\frac{I_L \cdot T}{V_{DD}} \tag{34}$$

from which the increase of area results to be

$$\frac{C_{T\,Iop} - C_{T\,Aop}}{C_{T\,Aop}} = \frac{\left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right)^2}{4\sqrt{\frac{\alpha}{1+\alpha}}} - 1. \tag{35}$$

Relationship (35), which is plotted in Fig. 11, is a decreasing function of α, and it is about equal to 0.4 and 0.2 (i.e., an area increase equal to 40% and 20%) for α equal to 0.1 and 0.2, respectively. For α much lower than 0.1 (not plotted), the minimum power consumption strategy requires a huge amount of silicon area.

Let us now evaluate the incurred increase in current consumption with the minimum area design. Substituting (29) or (32) into (17), we find the expression of I_{VDD} for the minimum area and minimum current design strategies

$$I_{VDD,\,Aop} = \left[2(1+2\alpha)\left(\frac{V_{Out}}{V_{DD}} - 1\right) + 1\right] \cdot I_L \tag{36}$$

$$I_{VDD,\,Iop} = \left\{\left[(1+2\alpha) + 2\sqrt{\alpha+\alpha^2}\right]\left(\frac{V_{Out}}{V_{DD}} - 1\right) + 1\right\} \cdot I_L. \tag{37}$$

The current increase is given by

$$\frac{I_{VDD,Aop} - I_{VDD,Iop}}{I_{VDD,Iop}} = \frac{\left[2(1+2\alpha)\left(\frac{V_{Out}}{V_{DD}} - 1\right) + 1\right]}{\left[(1+2\alpha) + 2\sqrt{\alpha+\alpha^2}\right]\left(\frac{V_{Out}}{V_{DD}} - 1\right) + 1} - 1. \tag{38}$$

By inspection of Fig. 12 where (38) is plotted, we see that the increment in I_{VDD} is a decreasing function of α and an increasing function of the ratio V_{Out}/V_{DD}. In particular, for an ideal one-stage CP, the current consumption increase is, for the optimum area design, not higher than 20%. On the other hand, for V_{Out}/V_{DD} higher than 4, the current consumption increase is higher than 20%, provided that α is lower than 0.15. Similar results that take into consideration CP efficiency instead of current consumption are found in [25].

V. Charge Pump with Purely Capacitive Load: Design Strategies

The design parameters involved in the design of a CP with purely capacitive load are summarized in Table 3 and can be obtained from relationships (12), (21) and (27). The first parameter to be set is the number of stages. However, even if (11) relates N and the steady state output voltage in a simple way, it cannot be really used since this value is ideally reached after an infinite time.

Again, as for the case of current load discussed above, we can follow different design strategies. Indeed, analyzing the plot in Fig. 13, where normalized (to their minimum values) Q_{Tot} and C_{Tot} are plotted versus N, two different minima appear. Hence, before starting the design procedure, we have to clearly identify the main design target, in order to use the design approach that allows the chosen performance to be optimized.

a) Area Occupation and Rise Time Minimization

To establish the optimum number of stages that minimizes the silicon area we must evaluate C_{Tot} through (21) and set to zero its derivative with respect to N. Similarly, the optimum N that minimizes the rise time is found by directly setting to zero the derivative of (21). In both cases we get

$$-2\ln\frac{(N+1)-v_x}{(N+1)-v_{x0}}+N\left[\frac{1}{(N+1)-v_{x0}}-\frac{1}{(N+1)-v_x}\right]=0. \tag{39}$$

The above expression can be simplified using the empirical approximation (very accurate for x ranging from 0.3 to 1 [28])

$$\ln(x)\approx\frac{2x^2-x-1}{3x}. \tag{40}$$

And, after some algebraic simplifications, (39) becomes

$$\frac{(v_x-v_{x0})[4v_x+2v_{x0}-3(N+2)]}{[(N+1)-v_x][(N+1)-v_{x0}]}=0 \tag{41}$$

from which, the optimum N minimizing both the total capacitance and rise time is

$$N_{Aop}=\frac{4}{3}v_x+\frac{2}{3}v_{x0}-2 \tag{42}$$

and, since v_{x0} is often equal to 1, we get

$$N_{Aop}=\frac{4}{3}(v_x-1). \tag{43}$$

Once N_{Aop} is defined, we can use the rise time constraint, given by (21), to evaluate the required total pumping capacitance and, hence, the value of C.

Table 3.
CP design parameters.

Parameter	Comment
V_{DD}	Technology dependent
Q_{Tot}	Not known a priori
$V_{Out}(t_r)$	Design constraint
t_r	Design constraint
$f = 1/T$	System dependent
$C_{Tot} \propto A_{Tot}$	Not known a priori
N	Not known a priori
$\alpha = C_P/C$	Technology dependent

b) Charge Consumption Minimization

To find the optimum number of stages that minimizes charge consumption, we take the derivative of (27) and set it to zero

$$(v_x-v_{x0})+2\alpha N\ln\frac{(N+1)-v_{x0}}{(N+1)-v_x}$$
$$-\alpha N^2\frac{v_x-v_{x0}}{[(N+1)-v_x][(N+1)-v_{x0}]}=0. \tag{44}$$

To solve (44), we again approximate the logarithmic term. We now use the linear approximation which minimizes the error in the range 0 to 1 [28]

$$\ln(x)\approx 2(x-1). \tag{45}$$

Thus (44) becomes

$$1+\frac{4\alpha N}{(N+1)-v_{x0}}-\frac{\alpha N^2}{[(N+1)-v_x][(N+1)-v_{x0}]}=0 \tag{46}$$

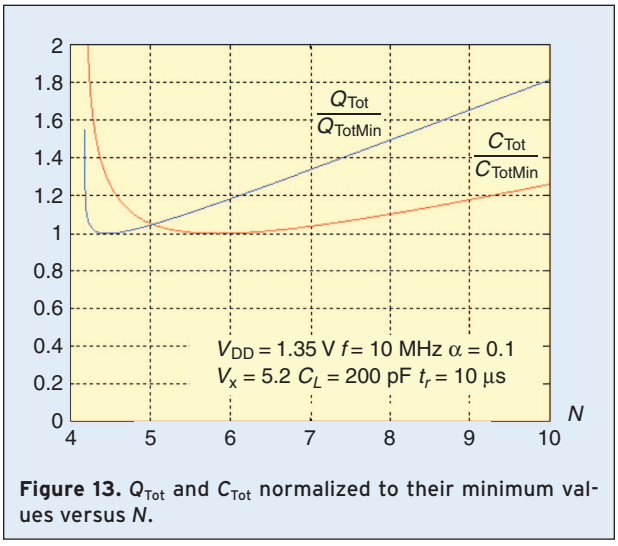

Figure 13. Q_{Tot} and C_{Tot} normalized to their minimum values versus N.

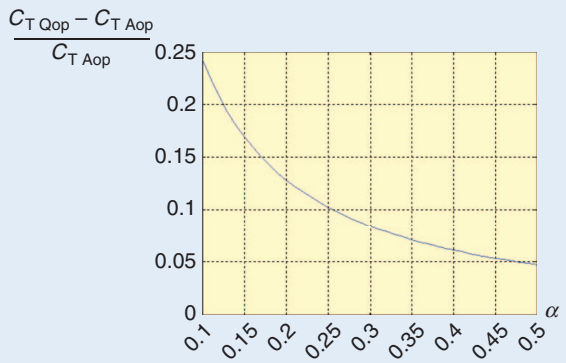

Figure 14. Increase on total CP capacitance (proportional to silicon area) of minimum power consumption design with respect to the minimum area design.

or equivalently

$$(1+3\alpha)N^2-[v_x+v_{x0}+4\alpha(v_x-1)-2]N+(v_x-1)(v_{x0}-1)=0. \tag{47}$$

Since v_{x0} is often equal to 1, the optimum number of stages minimizing charge consumption is expressed by

$$N_{Qop}=\frac{1+4\alpha}{1+3\alpha}(v_x-1). \tag{48}$$

Again, once N_{Qop} is calculated, we find the pumping capacitor, C, for the required rise time by using relationship (21).

c) Design Strategies Comparison

To perform a comparison of the design strategies discussed before, we evaluate the area overhead caused by the minimum power consumption design and the charge consumption overhead caused by the minimum silicon area design [28].

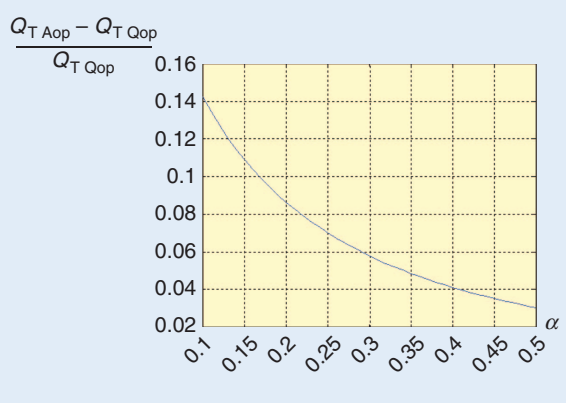

Figure 15. Increase on charge consumption (i.e. power consumption) of minimum area design with respect to minimum consumption design.

As already stated, the silicon area can be directly derived from the CP total capacitance, hence evaluating (21) for each design strategy, we get

$$t_{r,Aop}=T\frac{C_L+C_{Eq}}{C_{T,Aop}}\left[\frac{4}{3}(v_x-1)\right]^2\ln 4 \tag{49}$$

$$t_{r,Qop}=T\frac{C_L+C_{Eq}}{C_{T,Qop}}\left[\frac{1+4\alpha}{1+3\alpha}(v_x-1)\right]^2\ln\left(\frac{1}{\alpha}+4\right), \tag{50}$$

where $C_{T,\,Aop}$ and $C_{T,\,Qop}$ are the pumping total capacitances in the cases of area and charge consumption minimization, respectively. Assuming a given rise time to be achieved by both design strategies, by equating (49) and (50) we can evaluate the increased total CP capacitance for the optimized power consumption design with respect to the minimum area design. It results to be

$$\frac{C_{T,Qop}-C_{T,Aop}}{C_{T,Aop}}=\left(\frac{3}{4}\frac{1+4\alpha}{1+3\alpha}\right)^2\frac{\ln\left(\frac{1}{\alpha}+4\right)}{\ln 4}-1. \tag{51}$$

Relationship (51) is a decreasing function of α as can be seen from its plot in Fig. 14. It is apparent that the area increases by 25% to 5% for α ranging from 0.1 to 0.5.

To compare the charge consumption of the two design strategies, we substitute N from (43) and (48) into relationship (28) (assuming as usual v_{x0} equal to 1), we get

$$Q_{T,Aop}=\left[\frac{4}{3}(v_x-1)^2+\alpha\left(\frac{4}{3}\right)^2(v_x-1)^2\ln 4\right](C_L+C_{Eq})V_{DD} \tag{52}$$

for the area minimization design, and

$$Q_{T,Qop}=\left[\frac{1+4\alpha}{1+3\alpha}(v_x-1)^2+\alpha\left(\frac{1+4\alpha}{1+3\alpha}\right)^2(v_x-1)^2\ln\left(\frac{1}{\alpha}+4\right)\right]\times(C_L+C_{Eq})\cdot V_{DD}. \tag{53}$$

for the charge consumption minimization design. Hence, the increase of the charge consumption incurred by the minimum area design is given by

$$\frac{Q_{T,Aop}-Q_{T,Qop}}{Q_{T,Qop}}=\frac{\frac{4}{3}\left(1+\alpha\frac{4}{3}\ln 4\right)}{\frac{1+4\alpha}{1+3\alpha}\left[1+\alpha\frac{1+4\alpha}{1+3\alpha}\ln\left(\frac{1}{\alpha}+4\right)\right]}-1. \tag{54}$$

By inspection of Fig. 15 where relationship (54) is plotted, we can see that (54) is a decreasing function of α and is always lower than 15% for typical α values.

VI. Charge Pump Topologies

In the previous sections we have considered CP with ideal switches. However, real CPs differ substantially for the way switches are implemented.

a) The Dickson Charge Pump

The integrated realization of a CP was demonstrated for the first time by Dickson in 1976 [1]. Like previous CPs adopted in discrete implementations, such as the Crockcroft and Walton topology proposed in 1932 [31], the **Dickson CP** makes use of diodes instead of switches, as illustrated in Fig. 16. A CP topologically similar to the Dickson's one but implemented with MOS diodes, as shown in Fig. 17, was also implemented on silicon [2].

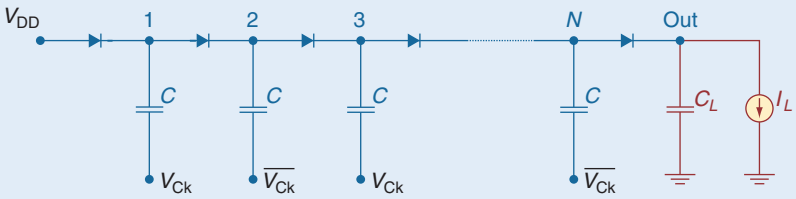

Figure 16. Dickson CP.

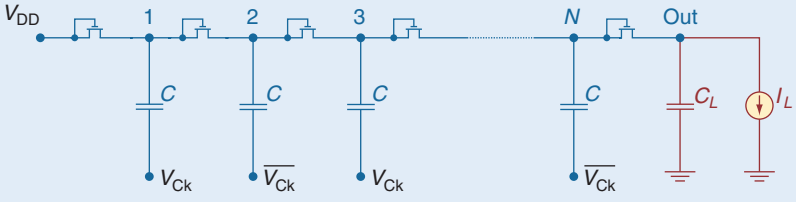

Figure 17. CP with MOS diodes.

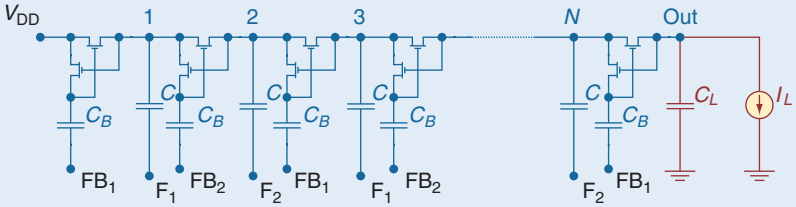

Figure 18. Bootstrap CP.

The main advantage provided by diodes is the absence of the switch control signals. The main drawback is the reduction of the CP output voltage. Indeed, when a diode is forward biased (i.e., when the corresponding switch must be closed), it causes a voltage loss equal to the diode threshold voltage, V_γ, which reduces the output voltage of a factor $(N+1)V_\gamma$.

This reduction is particularly critical under low power supplies, and determines also a loss in the CP efficiency. For this reason, the Dickson CP is not a practical topology for present applications.

b) The Bootstrap Charge Pump

An attractive and widely adopted implementation of the CP switches was presented in [8]–[9] and is called **bootstrap CP**. The associated CP topology is shown in Fig. 18, and the clock signals are plotted in Fig. 19.

Even if the implementation of a switch is conceptually simple (for example through a simple MOS transistor or a transmission gate), in a CP the voltage at the switch terminals are higher than the power supply. As a consequence, the MOS transistors used to implement the CP switches, have to be switched ON by applying suitable gate voltages higher than their source terminal voltages. Specifically, considering the CP in Fig. 18, the required high gate voltages are obtained for each stage thanks to a bootstrap circuit, which is realized by adding (for each stage) another capacitor and MOS transistor.

To understand the working principle of a bootstrap CP, let us analyze the generic stage (plus a capacitor) depicted in Fig. 20. During the half period in which there is no charge transfer (i.e., M_{PASS} is open), signal F_{B1} is low and the added transistor M_B is closed, since the voltage at its gate is higher of a threshold voltage ($V_{GS,MB} = 2V_{DD}$) than the other two nodes. The capacitor C_B is then charged up to a voltage equal to $V_{j-1} = (j-1)V_{DD} - (j-2)\Delta V$, see (38).

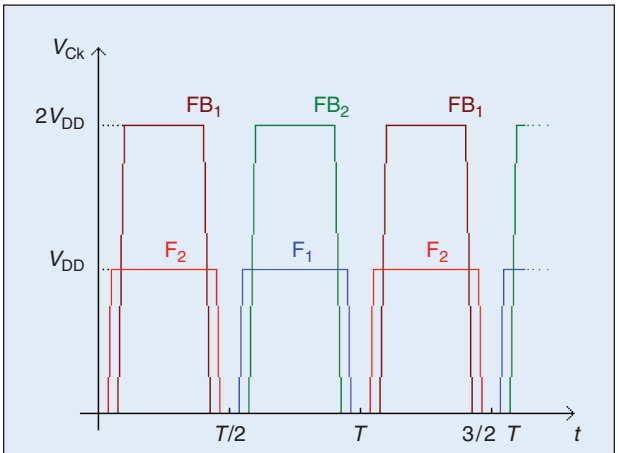

Figure 19. Bootstrap CP clock (F_i) and control (F_{Bi}) signals.

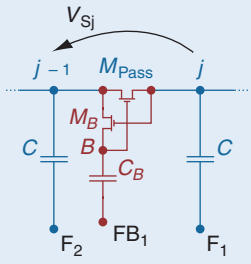

Figure 20. Generic stage (plus a capacitor) of a bootstrap CP.

During the subsequent half period, the clock signals F_1 and F_2 change their value, and, after another small time slot (see Fig. 19), F_{B1} goes high to 2 V_{DD}. Now the transistor M_B is open while the pass transistor M_{PASS} is closed. Indeed, the gate voltage of M_{PASS} is equal to $(j+1)V_{DD} - (j-2)\Delta V$, which is higher than the voltage at its source (i.e., the node j) by $V_{DD} + 2\Delta V$. Besides, during this half period, the gate-source of M_{PASS} is sufficiently high to keep this transistor closed (the gate-source voltage is always not lower than $V_{DD} + \Delta V$).

It is apparent that the ingenious behavior of this topology is obtained at the price of a more complex clocking and control section (requiring four phases and $2V_{DD}$ amplitude).

c) Double Charge Pumps

The *double CP* was conceived to reduce the output ripple by using the same total CP capacitance, C_T. As depicted in Fig. 21, each half part, which has a total capacitance $C_T/2$, feeds the load in a different half period [32]. Hence, the charge ΔQ pumped at the output is divided into two equal parts, each for half period. The output voltage is the same as the simple CP, but the ripple is now

$$V_r = \frac{1}{2}\frac{\Delta Q}{C_L} = \frac{I_L \cdot T}{2 \cdot C_L}. \tag{55}$$

Indeed, for this topology, the time interval between two charge transfer into C_L when the output voltage is reduced due to the current load I_L is now only $T/2$.

Of course, by properly implementing the switches, a *double Dickson CP* or a *double bootstrap CP* can be realized. The latter is shown in Fig. 22.

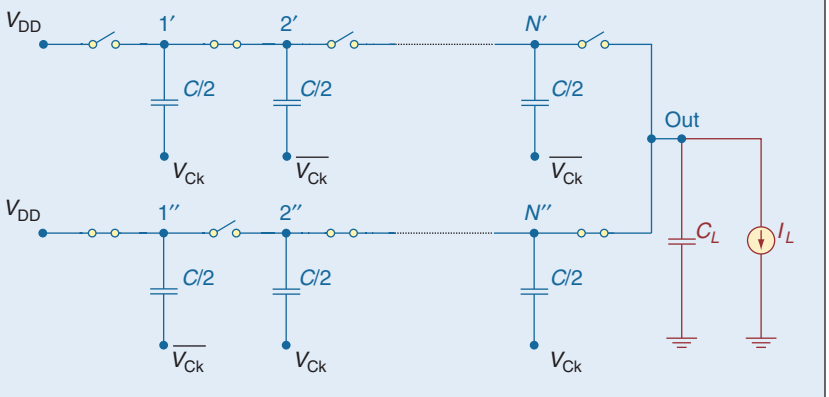

Figure 21. Simplified schematic of a double CP.

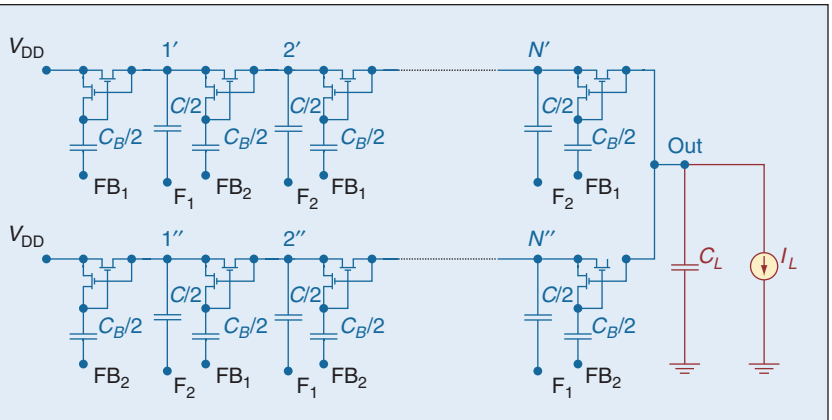

Figure 22. Double bootstrap CP.

A very interesting double CP that only recently is gaining popularity, was originally proposed in [5]–[6], and is shown in Fig. 23. This topology, often named *latched CP* since it includes a latch in each stage, is suitable for very high clock frequencies. Indeed, unlike the bootstrap CP, the latched CP needs only a two-phase clock.

d) Series-Parallel Charge Pumps

Another topology, which reminds those originally adopted for discrete implementations [31], is the *series-parallel CP*. It has been seldom used in IC implementations [17], since it was considered inefficient for this use. However, only recently, an in-depth analysis to evaluate its suitability for ICs has been carried out [33]–[34].

A two stage series-parallel CP is shown in Fig. 24. The peculiarity of this CP is the parallel charging of all the capacitors to the power supply, V_{DD}, during the first half period (i.e., when switches P_i and P_i' are closed and switches S_i

are open), and the series connection of all capacitors in the other half period (i.e., when switches P_i and P_i' are open and switches S_i are closed).

The main drawback of this topology is constituted by the parasitic capacitances which affect the behavior and performance more than the other topologies. Indeed, as demonstrated in [35], the reduction of the output voltage with respect to an ideal charge pump (i.e., without parasitic capacitances) strongly increases by increasing the number of stages. Moreover, another critical aspect concerns the switches implementation.

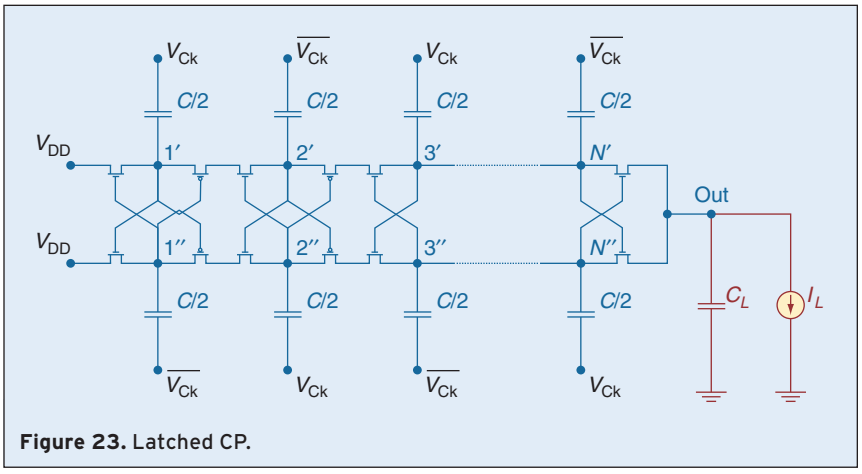

Figure 23. Latched CP.

e) Charge Pumps with Adaptive Number of Stages

In many IC applications more than one CP with different number of stages is required. Thus, when the CPs are used in non overlapping time periods, it can be useful to implement only one CP that dynamically adapts its number of stages. Examples of CPs with adaptive stages are shown in [36] and [13].

More specifically, a solution that switches from a two-stage to a four-stage topology is proposed in [36]. In [13], the number of stages is dynamically chosen by rearranging the whole set of capacitors so that the required output voltage could be reached by maximizing the CP's efficiency. Hence, for a defined number of stages, the whole CP capacitance (i.e., silicon area used by the CP) always remains equal.

A version of the topology proposed in [13], which adapts its number of stages from 1 to 3, is shown in Fig. 25. Without loss of generality, the topology uses diodes as switches, but changes can be simply implemented if switches instead of diodes are used.

It is worth noting that, in order to provide adaptability, each capacitor is connected through a diode both to the power supply (D_{Ai} and D_{Di}) and to the output node (D_{Ci} and D_{Ei}). Moreover, there are diodes that connect couple of capacitors (D_{Bi} and D_{Fi}).

To understand the behavior of the CP, let us consider each single case starting from the single-stage one. In this configuration, all the capacitors have to be connected in parallel to form a single capacitor. In other words, this means that all the capacitors have to be driven by the same phase signal and all the diodes connecting couple of capacitors (D_{Bi} and D_{Fi}) are always reverse biased.

In the case in which a two-stage topology is needed, the CP in Fig. 25 works like three parallel two-stage topologies. Hence, it can be simply inferred that the set of phases F_1, F_3 and F_5 must be complementary to the other set F_2, F_4 and F_6. Under this condition, the diodes D_{Fi} are always reverse biased. Moreover, since at steady state $V_{2i} > V_{DD}$ and $V_{2i+1} < V_{Out}$, the diodes D_{Di} and D_{Ei} are also reverse biased.

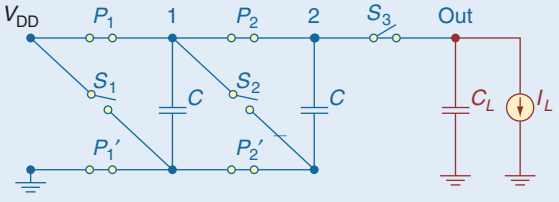

Figure 24. Series-parallel CP.

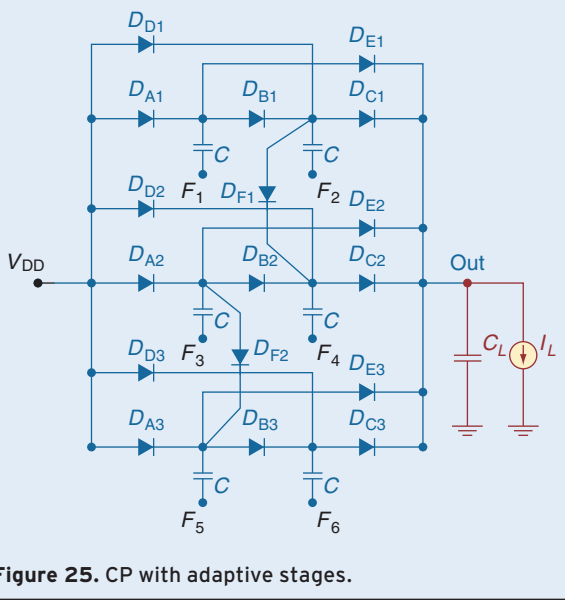

Figure 25. CP with adaptive stages.

Table 4.
Clock phases for the CP in Fig. 25.

	One-stage CP	Two-stage CP	Three-stage CP
FX	$F_1, F_2, F_3, F_4, F_5, F_6$	$F_1, F_3, F_5,$	$F_1, F_3, F_4, F_6,$
FN	–	$F_2, F_4, F_6,$	$F_2, F_5,$

Finally, a three-stage CP can be obtained by configuring the CP like two parallel three-stage CPs. This condition is obtained by driving the input phases F_1, F_3, F_4 and F_6 together, and the input phases F_2 and F_5 by the complementary phase. Thus, the two three-stage CPs have the two main paths constituted by internal nodes 1, 2 and 4 with the set of phases F_1, F_2 and F_4, and internal nodes 3, 5 and 6 with the set of phases F_3, F_5 and F_6. It can be simply verified that at the steady state the diodes D_{Di}, D_{Ei}, D_{C1}, D_{B2} and D_{A3} are reverse biased.

The phase arrangement for the three cases are summarized in Table 4.

VI. Appendix

Let us start by considering the CP in Fig. 3 without the current load. During the first half period (with S_1 closed and S_2 open) C is charged up to a voltage V_{DD}, while C_L holds its charge. In the second half period (with S_1 open and S_2 closed) there is a charge redistribution between C and C_L, and in a generic period j we get

$$V_{Out}(j) = V_2(j) = \frac{C \cdot 2V_{DD} + C_L \cdot V_{Out}(j-1)}{C + C_L}. \quad (56)$$

Assuming that in the initial state $V_{Out}(0) = V_{DD}$, we get

$$V_{Out}(1) = V_{DD} + \frac{C}{C + C_L} V_{DD} \quad (57)$$

$$V_{Out}(2) = V_{DD} + \frac{C}{C + C_L}\left(1 + \frac{C_L}{C + C_L}\right) V_{DD} \quad (58)$$

after one and two clock periods, respectively. Hence, relationship (56) can be rewritten as [36]–[37]

$$V_{Out}(j) = V_{DD} + \frac{C}{C + C_L} V_{DD} \sum_{i=0}^{j-1} \left(\frac{C_L}{C + C_L}\right)^i, \quad (59a)$$

which, by using the property of power series[1], becomes

$$V_{Out}(j) = V_{DD} + \left[1 - \left(\frac{C_L}{C + C_L}\right)^j\right] V_{DD}, \quad (60a)$$

whose limit for $j \to \infty$ is 2 V_{DD}.

If the CP has also a current load (as shown in Fig. 3) relationship (56) still holds. Indeed, with C_L much higher than C, the discharge due to I_L can be assumed equal in both the half periods. However, we have now a different initial condition, since (57) is now reduced by a factor $(I_L T)/C_L$. Thus, (59a) changes into

$$V_{Out}(j) = V_{DD} + \left(\frac{C}{C + C_L} V_{DD} - \frac{I_L T}{C_L}\right) \sum_{i=0}^{j-1} \left(\frac{C_L}{C + C_L}\right)^i, \quad (59b)$$

which is equivalent to

$$V_{Out}(j) = V_{DD} + \left[1 - \left(\frac{C_L}{C + C_L}\right)^j\right]\left[V_{DD} - \left(\frac{1}{C_L} + \frac{1}{C}\right)\right] I_L T, \quad (60b)$$

whose limit for $j \to \infty$ (with C_L much higher than C) is relationship (1).

Gaetano Palumbo was born in Catania, Italy, in 1964. He received the laurea degree in Electrical Engineering in 1988 and a Ph.D. degree from the University of Catania in 1993. Since 1993 he conducts courses on Electronic Devices, Electronics for Digital Systems and basic Electronics. In 1994 he joined the DEES (Dipartimento Elettrico Elettronico e Sistemistico), now DIEES (Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi), at the University of Catania as a researcher, subsequently becoming associate professor in 1998. Since 2000 he is a full professor in the same department.

His primary research interest has been analog circuits with particular emphasis on feedback circuits, compensation techniques, current-mode approach, low-voltage circuits. Then, his research has also embraced digital circuits with emphasis on bipolar and MOS current-mode digital circuits, adiabatic circuits, and high-performance building blocks focused on achieving optimum speed within the constraint of low power operation. In all these fields he is developing some the research activities in collaboration with STMicroelectronics of Catania.

He was the co-author of three books "CMOS Current Amplifiers" and "Feedback Amplifiers: theory and design" and "Model and Design of Bipolar and MOS Current-Mode Logic (CML, ECL and SCL Digital Circuits)" all by Kluwer Academic Publishers, in 1999, 2001 and 2005, respectively, and a textbook on electronic device in 2005. He is the author of 340 scientific papers on referred international journals (over 140) and in conferences. Moreover he is co-author of several patents.

Since June 1999 to the end of 2001 and since 2004 to 2005 he served as an Associated Editor of the *IEEE Transactions on Circuits and Systems part I* for the topic "Analog Circuits and Filters" and "digital circuits and

[1]Remember that, for $x < 1$, one has that $\sum_{i=0}^{j-1} x = 1 - x^j/1 - x$

systems", respectively. Since 2006 to 2007 he served as an Associated Editor of the *IEEE Transactions on Circuits and Systems part II*. Since 2008 he is serving as an Associated Editor of the *IEEE Transactions on Circuits and Systems part I*.

In 2005 he was one of the 12 panelists in the scientific-disciplinare area 09—industrial and information engineering of the CIVR (Committee for Evaluation of Italian Research), which has the aim to evaluate the Italian research in the above area for the period 2001–2003.

In 2003 he received the Darlington Award. Prof. Palumbo is an IEEE Fellow.

Domenico Pappalardo was born in Catania, Italy, in 1966. He received the Laurea degree in electronic engineering from the University of Catania in 2000.

Since then he has worked for ST Microelectronics, Catania, Italy. During this time he has worked on the design of non-volatile memory circuits. He is the author of some scientific papers on referred international journals and conferences. Moreover, he is also author of several patents.

In 2003 he received the Darlington Award for a paper published on TCAS-I dealing with charge pump circuits.

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