A Truly Low-Cost High-Efficiency ASK Demodulator Based on Self-Sampling Scheme for Bioimplantable Applications

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***Abstract*—In the fields of wireless bioelectronics implants and sensor network systems, amplitude shift keying (ASK) is one of the most commonly used schemes employed to modulate the baseband signal with reference to the intermediate or even the carrier frequency. In this study, a demodulator architecture capable of dealing with most of the previous limitations in an ASK-utilized medical implant, especially in want of being powered through wireless delivering, is proposed. It features the abilities of working on a very small modulation index and being provided without any R/C component(s) inside by means of a self-sampling scheme. The design has been implemented in an 18-μm CMOS process. The demodulator circuit occupies a die size of merely $32.3 \times 14.5\ \mu\text{m}^2$. Analytic results from both simulated gradation and fabricated chips show that the proposed circuit can operate at a carrier of 2 MHz and achieve a modulation rate of up to 50%. The results also demonstrate that the presented work can still perform a proper demodulation even with a modulation index beneath 5.5%. An average power of approximately 336 μW was confirmed in return for the remarkable advantages. All aspects regarding the design, including a review of the prior arts, system consideration, circuit description, and analyses from simulation phase to actual measurement, are presented in detail.**

***Index Terms*—Amplitude-shift keying (ASK) demodulator, artificial prostheses, bioimplantable systems, self-sampling.**

I. Introduction

SO FAR, the amplitude-shift keying (ASK) modulation/demodulation scheme has been widely utilized in many communication systems in virtue of its structural simplicity. Over the decades, numerous researchers dedicated their vigor to move such a technique to their special research demands in biomedical science. With regard to the medical applications in this way, ASK is generally involved in function electrical stimulation (FES) for implantable cardiac pacemakers, bladder control, neuromuscular stimulus, cochlear implants, and retinal prostheses [1]–[13]. In most cases, the FES systems are able to be simply summarized using a block diagram shown in Fig. 1.

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The extracorporeal part generates the stimulus patterns containing information of the excitation-induced current magnitudes and corresponding addresses for driving the internal stimulators performing electrical stimulation in right positions. These data will be subsequently encoded further and are modulated, power amplified, and finally transmitted through a transmitter coil. At the receiver side (i.e., the internal part), the presence of a portion of the energy transmitted via the transcutaneous link forms a voltage source, which will be rectified to obtain a coarse dc level and referred ground. The following regulator provides rest of the circuitry with a fine and stable dc supply. Meanwhile, the gathered envelope passes through a stepdown circuit serving as a voltage divider to obtain the signal needing to be demodulated at the next stage. The on-chip demodulator recovers the digital waveform a nonreturn-to-zero (NRZ) format after discriminating the lower amplitude (i.e., the modulated signal amplitude) from the higher one (i.e., the unmodulated signal amplitude). Finally, the signals for achieving a proper functional stimulation will be reconstructed as they predefined prior to transmission by means of a string of the postprocessing circuit submodules. These submodules have functions of: 1) clock regeneration and data recovery for specific coding format; 2) data registration and arrangement for regained parameters; 3) generation of the stimulus signals with respect to the indexed parameters; 4) control of analog front-end for neural stimulus.

One of the essential factors in proper action of the implant is the integrity of command bits governed by demodulation correctness. Most ASK demodulators (ASKDs) involved in such fields, however, carry out a purely envelope-based determination. The demodulation fashion not only results in limitations in implant space and data rate but also induces a huge expense for circuit amendment as a result of their insufficiency regarding the discriminable modulation index. A high modulation index makes the overall power efficiency of the systems a bit poor in case those ASKDs are put to use. Motivated by this, we present in this paper a versatile new ASKD aimed at overcoming foregoing problems. The proposed architecture is RC-less and can sustain correctly an ultralow-end demodulation. In order to demonstrate workability of the resulting circuit, fabrication of a proof-of-concept prototype has been enforced through the foundry. The results originate from both simulation and actual experiments have sufficiently shown its merit. Through the experiments, a comforting robustness has also been confirmed. All aspects regarding the efficiency of an implantable system are of our main concerns. This paper is organized as follows. Section II

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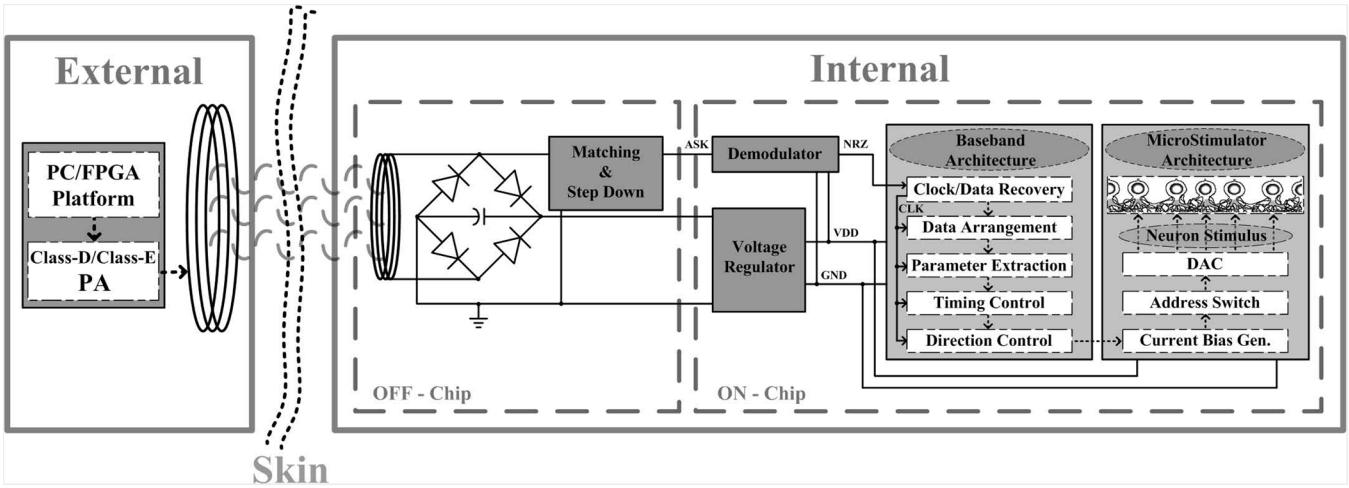

Fig. 1. Block diagram of a familiar FES system.

presents a general review for certain of the typical ASKD architectures. Section III describes issues and considerations for an ASK-modulated wirelessly powered implant. The overall design methodology for the proposed circuit is elaborated on in the same section. Results and analyses are discussed in depth in Section IV, followed by concluding remarks in Section V.

II. Overview of ASKD Families

Figs. 2–9 show some typical ASKDs which are, respectively, proposed or adopted by Gunnar *et al.* [1], Baru *et al.* [2], Yu *et al.* [3], Liu *et al.* [4], Chen *et al.* [6], Dong *et al.* [7], Lee *et al.* [8], and Djemouai *et al.* [9], [10]. We start the introduction with the Gunnar's architecture shown in Fig. 2.

In Gunnar *et al.*'s architecture, the ASK-modulated signal first passes through a preprocessing stage consisting of a simple voltage follower, a current-limited inverter (CLI), and a load driver to obtain a sharpened clock signal A corresponding to a valid logic HIGH. This signal is then utilized as a reference signal for recovering the system clock. In the meantime, it is also fed into a low-pass filter (LPF) stage. Owing to the prolonged charging period stemming from the capacitor of the LPF, the modulation rate is restricted. In addition, a ripple on the signal B also contributes a possible risk about which a jittering of the demodulated output may appear when the ripple sweeps the transition threshold of the following CLI persistently. It will lead to another possible limitation on erroneous judgement in the following stage while the modulation rate of this design becomes improvable.

Similar jitter phenomenon also occurs in the Baru's structure shown in Fig. 3. In this design, the fist stage amplifier serves as the comparator. Once the modulated signal is higher than the reference dc level, the P-transistor M turns on to retrieve the "1". On the other hand, "0" is decoded in the absence of carrier. The main feature of such a design is that the comparator was implemented in a cheaper large-size process. The long-channel weak inversin makes the comparator be provided with an ultralow-power efficiency. However, in order to obtain an enough gain and minimize the noise, such a weak inversion also contributes an incredible sizing in the differential pair as well as its

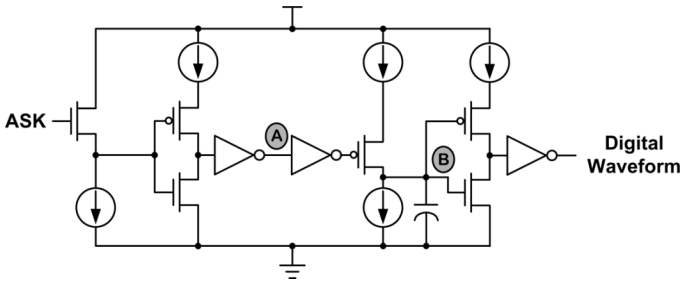

Fig. 2. Gunnar *et al.*'s architecture.

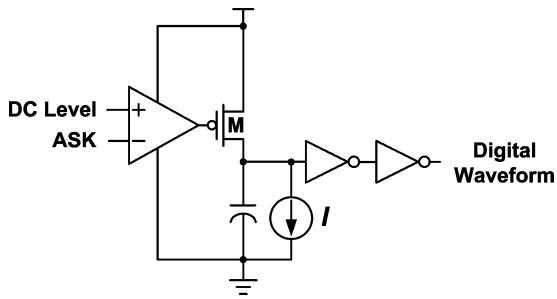

Fig. 3. Baru *et al.*'s architecture.

reference stage, resulting in a huge occupied silicon area. Also, the carrier frequency is limited to a band low enough, leading to only a few data rate available. In addition, the biased dc level of the modulated input and the reference level of the whole comparator should be kept letting the interference as small as possible to remain valid for the operation at the weak inversion region. It makes the design be confronted by a serious problem in robustness. Moreover, for a given amount of capacitor, there is still a tradeoff among driving ability on transistor M, discharge current I, data rate, and power consumption, which needs to be carefully considered.

Fig. 4 shows the design of Yu *et al.* where two LPFs with different timing constants are utilized. The two LPFs assist the succeeding cross-coupled comparator in sensing the difference between the modulated amplitudes from an envelope detector for recovering the digital command bits. Such a structure whose hysteresis is defined in advance is with the same principle as

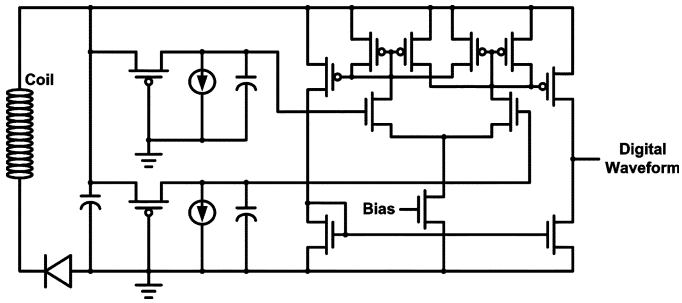

Fig. 4. Yu *et al.*'s architecture.

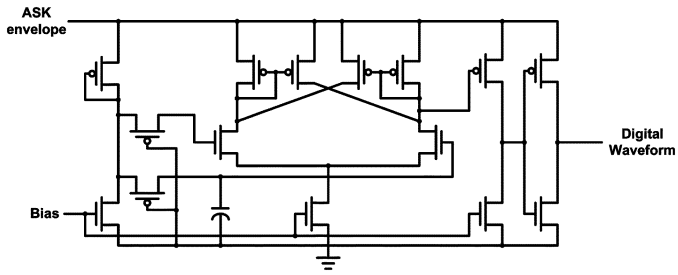

Fig. 5. Liu *et al.*'s architecture.

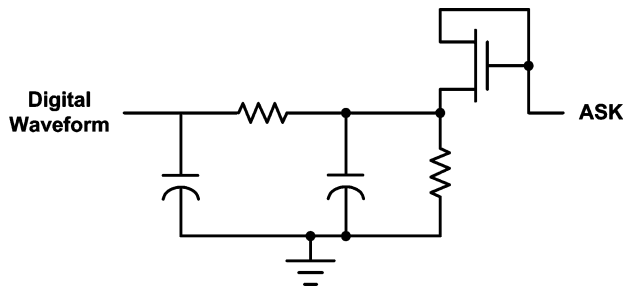

Fig. 6. Architecture adopted by Lin *et al.* and Chen *et al.*.

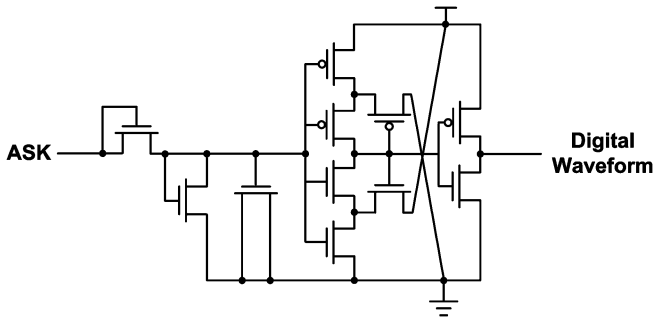

Fig. 7. Dong *et al.*'s architecture.

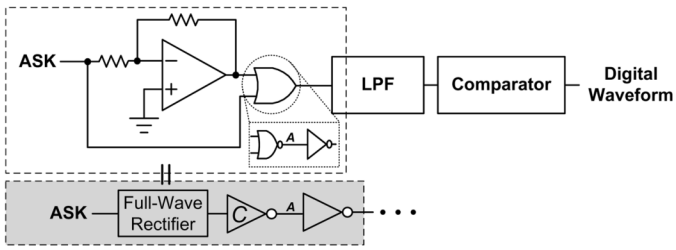

Fig. 8. Lee *et al.*'s architecture.

the Liu's architecture shown in Fig. 5 in which only one LPF is utilized. Their operation can be simply described as follows. After the received carrier has passed through the envelope detector, the resulting data-combined envelope flows to two signal paths and is subsequently fed into the comparator. One of the voltage levels of the signal paths serves as a reference, both of which are shifted within the input common-mode rage of the following comparator. Once the difference between the two signal levels has been amplified, the demodulation process is completed. Despite their simplicity, however, both the designs become sensitive if the modulation index is demanded to be small. It makes the adjustment of the timing constant of the LPF-formed signal path extremely difficult, resulting in a failed demodulation caused by the severe jittering on the demodulator output.

Referring to the architecture of Lin *et al.* and Chen *et al.* (Fig. 6), an envelope detector composed of a diode and two LPFs is employed to demodulate the amplified received signal first. The following data buffer (not shown) recovers a desirable voltage level. Such a configuration is based upon a common approach of the envelope detection except the second LPF close to the demodulated output. Despite the authors claim that the additional LPF can be utilized to cope with the tradeoff between the clipping time and carrier on the envelope and, hence, decreasing the capacitor dependency of the data rate, the modulation rate reported in [5], [6] is still unsatisfactory for a sufficient data capacity especially when only a lower carrier band is available. In addition to the architecture of Fig. 6, Dong *et al.* propose a similar structure shown in Fig. 7 in which the diode and *RC* circuit have been replaced with MOS transistors to expedite the on-chip integration. A Schmitt trigger is put in the output of the envelope detector to serve as the comparator so as to extract the binary data from the captured carrier signal at the reception side. However, despite the fully active benefit, this design has no additional LPF resembling the structure of Fig. 6. Therefore, the tradeoffs among the clipping time, the ripple on the envelope, and the choice of capacitor amount will impose a serious bottleneck on its circuit efficiency. In other words, the data rate and capacitor-related effects must be considered with carefulness.

Fig. 8 shows the work of Lee *et al.* It consists of a unit-gain amplifier, an OR gate (composed of a NOR and an inverter), an LPF, and a comparator. This structure is quite similar to most of the designs mentioned previously, adopting an envelope detection to recover the digital command bits. The first half of the structure is notable because it can be utilized to lighten the *RC* demand of the LPF. It is able to be explained by a simplified equivalent block brushed in gray. The full-wave rectification is the major cause for reducing the component size in the LPF. The inverter marked in C serves as a pre-comparator. The actual comparator in the circuit can also be considered as an inverter since its threshold has been defined as half of the supply [8]. The main limitation in the design is its high modulation index associated with the threshold of the NOR gate. When the index comes low, the increase of lower modulation level will cause the output of the NOR to be discharged, leading to a failed determination on comparator. In order to overcome such a problem, the transition threshold of the NOR must be sized to an extreme value, making

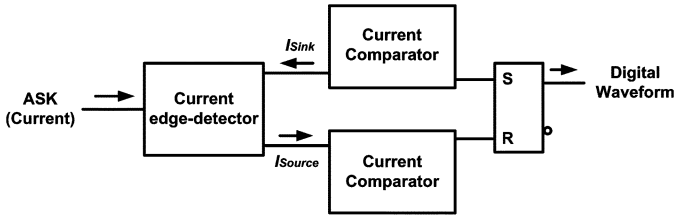

Fig. 9. Djemouai *et al.*'s architecture.

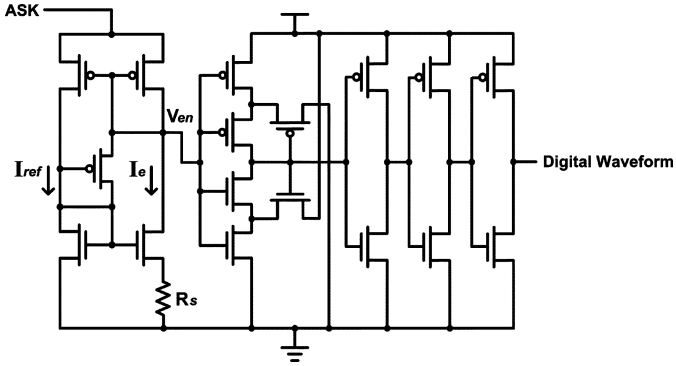

Fig. 10. Wang *et al.*'s architecture.

the design susceptible to noise. In addition, a dual-supply mechanism with dual-polar may be demanded for the OP to avoid operation in triode region, resulting in a higher processing cost.

A demodulator architecture, shown in Fig. 9 and proposed by Djemouai *et al.*, adopts a current-mode design methodology to process an input current whose levels are with very small modulation index. It is constructed of three stages named current edge-detector, current comparators, and SR latch. The current edge-detector detects the immediate input current transition. Once the current transition is detected, one of the current pulses, sink and source, associated with the aspect of transition is generated and then converted to voltage pulses through the comparators. These voltage pulses are utilized to control the latch stage for recovering carried information correctly. Such a design is with an improved version presented in [10] where a gain- and level-shifting stage is added into the edge-detector stage. Such a newly added stage amplifies the input current signal including the current difference at each transition and shifts it to the operation range of the comparators so that the noise tolerance of the demodulator can be strengthen. In addition, the amplification can also alleviate the demodulation difficulty as a result of the intensified source and sink pulses. Furthermore, two mirroring branches of the current paths of the comparators are forced into the *I–V* stages in front of the latch to eliminate the limiting factor of the comparator speed in demodulator performance. However, despite the authors' claim that it is able to be provided with less sensitive to the process variation in their latest version, the successful demodulation is relevant to the supply dependency on the gain and level shifting input stage of the edge detector. Once the supply is not stable enough (i.e., supply ripple is high enough), the demodulation fails. It implies that an extremely high-performance voltage regulator is demanded to make the circuit work properly. Also, the clear (ripple-free) input current as given in [9] and [10] is hard to extract from the receiver front-end in effect when the modulation index becomes small. Moreover, the modulation rate may also be restricted by the tradeoff between the asserted index and the stable input current.

The last reviewed structure, shown in Fig. 10, is proposed by Wang *et al.* [11]. It employs a supply-independent bias generator (SIBG) and the gate capacitor coming from the following Schmitt trigger to achieve the envelope detection. The Schmitt trigger serves as the threshold detector (i.e., comparator) to recover the digital waveform. Following cascaded inverters act as a buffer for driving the subsequent stages. This design has no passive capacitor inside and is highly praised for its simplicity. It seems to be a breakthrough in current ASKDs involved in the medical electronic implants. Despite its remarkable advantage, however, the passive resistor R_S here is quite pertinent to recovering correct binary sequence. This can be explained by referring to the equation

$$I_e = \frac{2}{\mu_n C_{\rm ox}\left(\frac{W}{L}\right)_{\rm nMOS}} \cdot \frac{1}{{R_S}^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \qquad (1)$$

where μ_n, $C_{\rm ox}$, and K are electron mobility, gate-oxide capacitance/per unit area, and ratio $I_e/I_{\rm ref}$, respectively. The output of SIBG (V_{en}) is dependent upon the current I_e. When the implemented resistor varies from the predefined value, the V_{en} changes and the designed threshold for the threshold detector loses efficacy, resulting in a demodulator malfunction. In addition, since the correct demodulation is in the same way dependent upon the threshold adjusted by the detector, this design suffers from a notable concern on demodulation performance yet in spite of R_S is accurate. When the supply variation occurs, the threshold varies, leading to a failed determination on V_{en}. A quantitative comparison in terms of the parameters for the aforementioned structures is tabulated in Table I. Summing up all of these architectures, there seems to be still no satisfactory demodulator type that is completely efficient in current and future FES as well as other medical-implant applications.

III. System Considerations and Circuit Design

A. ASKDs in Subminiature Wireless-Powering Devices

Prior to discussion of the proposed circuit, it will be instructive to briefly summarize the limitations of those reviewed structures and to introduce some specific considerations pertinent to the limitations. With regard to most previous ASKD designs, at least one capacitor or resistor (or both) is required to achieve a proper envelope detection. The choice of amount for such an *RC* circuit relies mainly on the available carrier band. This is particularly important because familiar implantable devices for FES are of special request in the temperature increase of body tissue caused by the absorption in higher carrier frequency. The selection of lower carrier band is usually considered reasonable. However, it leads to that the cost reduction in the *RC* circuit for a whole implant becomes less possible, especially when the component(s) is(are) constructed in passive element(s). Moreover,

TABLE I
COMPARISON OF PRIOR ARTS

Source	Modulation Index★	Operated Carrier (MHz)	Data Rate (Kbps)◆	Modulation Rate	Capacitor (C) or Resister (R)	ASK Core Size	Consumption	
							Power	Current Draw / Supply Voltage
Gunnar et al.[1]	100%	5	100	2%	1 pF	0.06 mm^2	—	30μA@3.3V
Barú et al.[2]	100%	0.027	0.68	2.52%	10 pF	0.29 mm^2	—	5μA@2V
Yu et al.[3]	—	—	—	—	2 C	0.035 mm^2	0.13 mW	—
Liu et al.[4]	7.14%	1~10	50~500	5%	10 pF	—	—	—
Lin et al.[5] Chen et al.[6]	100%	433	2000	0.46%	2 R, 2 C (11KΩ + 11pF)	0.0836*mm^2	1.36mW	@0.45V
		150	2000	1.33%			3.1mW	@0.5V
Dong et al.[7]	100%	10	1000	10%	1 C	—	—	—
Lee et al.[8]	63.64%	2	20	1%	2 R, 1 C	—	—	—
Djemouai et al.[9][10]	5.88%	—	500	—	1 R, 1 C	—	—	—
Wang et al.[11]	10.34% ~ 17.24%	2	20	1%	1 R	0.01274 mm^2	10.234mW**	—

— : Not available at demodulator side
* : Including other pre-processing and output driving circuits
** : Including output load
★ : Defined as $\frac{V_{usa}-V_{msa}}{V_{usa}+V_{msa}}\times 100\%$ [14] , where V_{usa} and V_{msa} can be referred to the definition of Fig. 11
◆ : Data rate has been calculated for only the demodulator side, without consideration to the added coding schemes involved

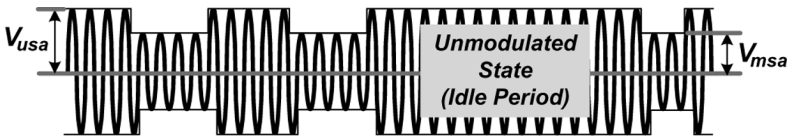

Fig. 11. Common inward ASK-modulated data-binding power link used in medical electronic implants. The term "inward" represents the information is carried from the external part to the internal side.

for those demodulators whose inputs are from an envelope detector, e.g., Yu *et al.*'s architecture, the modulation rate is greatly restricted by the load capacitance of the detector. When in the cases like the work of Gunnar *et al.* and Baru *et al.*, the internal LPFs also cause a capacitance dependency on modulation rate. This is how ASK can only be utilized in a low data-rate communication in general regardless of its feature of simplicity. Obviously, the bulk of the prior designs reveal a tradeoff between modulation rate and implant space.

However, in addition to the existent problems given above, the modulation index in an implantable system plays a notable role as well. It can be illustrated in detail with the common inward data-binding power envelope, which is presented at the receiver frond end across the FES implant, as shown in Fig. 11. The demodulation-used ASK input in this case is extracted from such a power envelope after the envelope is passed through a step-down (voltage-dividing) stage as depicted in Fig. 1. The comparatively longer period lying in the unmodulated signal amplitude V_{usa} is often adopted to achieve maximum power transfer periodically. For such a case, however, the minimum carrier level required by the system to generate stable dc supply is no more than V_{usa}, but may be higher than the modulated signal amplitude V_{msa}. ASK modulation during this idle state is usually undesirable to avoid the risk of losing system power. It makes the transmission speed in such protocols potentially insufficient and limits further the practicability of the ASK in an implantable system aspiring to high data-rate information exchange, e.g., the visual prostheses. When the modulation index increases, the load capacitance of an on-implant power recovery module will become a huge amount leading to a small possibility of on-chip full integration.

For a case that the minimally demanded carrier level is no more than V_{msa}, the system will be unable to malfunction no matter when the modulation occurs. Assuming that V_{msa} is exactly the minimum carrier level demanded of an implant, the amplitude of V_{usa} exceeds V_{msa} seems to become an unwanted dissipation source of the system power. As we knew the demodulation-used ASK input comes from the power carrier (envelope), the corresponding voltage differences for the same modulation index, seen by the receiver front-end and the demodulator side respectively, are quite different. The exceeding amplitude at the receiver front end is usually very large compared with the demodulator side in an implantable system adopting wireless (inductive) powering [15]. According to the report in [16], the minimally required carrier level for an implant functionality is able to be approximated as a linear scale factor (with a unit in ohms) multiplied by a product of coupling factor and current supplied by the power amplifier driving the primary coil if the equivalent resistance of a whole implant is modeled as a time-invariant value. It means that when data switch the exceeding amplitude at the receiver front end could result in an

extremely large unwanted switching current at the outside transmitter due to the nonideal switching, leading to further a huge power loss in spite of the fact that the linear scale factor has been optimized.

Notably, the power loss will become extraordinarily dramatic while the modulation rate is increased. Also, the above-mentioned assumption is considered somewhat impractical because the overwhelming majority of the external transmitters usually provide power levels much higher than the minimal requirements of the implants to ensure that they are able to work properly at all conditions even on a dreadful situation. The effect on the modulation index from such a practical standpoint will be of more critical importance since the higher the modulation index demanded for proper demodulation, the more the considerably exceeding voltage level across the receiver front end, implying a more significant reduction in the system power efficiency. In view of this, the index associated with the exceeding amplitudes governing the power efficiency of the whole system should be demanded as small as possible for such an inward ASK-modulated power link. Part of a recent paper [17] noted a similar notion of the efficiency, but the ASKD structure involved in that of the work is with the same envelope detection method as the majority mentioned before, which results in similar constraints.

Decreasing the index also brings about a benefit in increasing the modulation rate, while at the same time being with less requirement in lowering the system quality factor (Q), thereby making the high-data-rate transmission with good power efficiency become possible. When desiring to achieve data communication with a small modulation index and a satisfactory modulation rate, most of the existing ASKDs will malfunction, thereby causing considerable costs done on the circuit improvements.

B. Circuit Topology

The proposed demodulator is revealed in Fig. 12. This demodulator is mainly composed of four parts called pulse shaper (including ϕ and $\bar{\phi}$ generators), voltage scaler, level contraster, and self-sampler, respectively. The pulse shaper, constructed of a Schmitt trigger and a common inverter, shapes the ASK input into a pair of clear and regular sampling pulses ϕ and $\bar{\phi}$ representing the normal and the inverted clock signals, respectively. These clock signals will carry out a synchrony with the final self-sampler for data recovery. In order to keep the clock signals stable and to make the demodulator work correctly, the range of the demodulation-used input should be taken into account. Since the input will always go back to the referred ground of an implant where the level is given as 0 V, the peak of the ASK signal becomes our main concern, in particular for the peak level V_{ASKm} during modulation. V_{ASKm} should remain higher than a transition threshold $V_{L.B.}$ at which the output of the ϕ generator switches from high to low so that the sampling pulses do not be interrupted. In order to deduce the transition threshold $V_{L.B.}$, we make an assumption that the threshold has been set first. When the input risesto the threshold, transistor N2 enters the conduction mode, meaning that

$$V_{GS_{N2}} = V_{tn} \tag{2}$$

where V_{tn} is the nMOS threshold voltage. The source terminal voltage of N2 ($V_{S_{N2}}$) will be

$$V_{S_{N2}} = V_{L.B.} - V_{tn}. \tag{3}$$

Here, we neglect the body effect of N2. Because $V_{S_{N2}}$ is decided by transistors N1 and N3, these transistors are being operated at saturation region since

$$\begin{cases} V_{DS_{N1}} = V_{GS_{N1}} - V_{tn} = V_{L.B.} - V_{tn}; \\ V_{DS_{N3}} = V_{\mathrm{DD}} - V_{S_{N2}} > V_{GS_{N3}} - V_{tn}. \end{cases} \tag{4}$$

Therefore, we have

$$\beta_{N1}(V_{L.B.} - V_{tn})^2 = \beta_{N3}(V_{\mathrm{DD}} - V_{L.B.})^2 \tag{5}$$

where β_{N1} and β_{N3} represent the parameters of process and geometry ratio for the transistors N1 and N3, respectively. Thus, the transition threshold $V_{L.B.}$ can be obtained as

$$V_{L.B.} = \frac{V_{\mathrm{DD}} + V_{tn}\sqrt{\beta_n}}{1 + \sqrt{\beta_n}} \tag{6}$$

where β_n denotes $[((W/L)_{N1}/(W/L)_{N3})]_{\mathrm{effective}}$.

In the meantime the clock signals are being extracted, the second stage, called voltage scaler, made up of a common-source stage serves the post of an envelope detector. This stage can raise the ASK input to a specific minimum level, and reflect the peak difference between V_{ASKu} and V_{ASKm} by means of the disparities of their gains so that the amplitude change caused by the modulation can be judged by the next stage. The adoption of all p-transistor design enables the voltage scaler to be provided with less noise contribution than the counterpart, which is meaningful since the demodulation validity will be considerably affected by the noise for a very small modulation index and a given decision point from the next level contraster.

Before considering the operation of the voltage scaler, the policy of defining modulation index for the proposed circuit should be clarified. In our design, the index is concluded by a variable V_{ASKm} and a constant $V_{\mathrm{ASKu}}(V_{\mathrm{DD}})$ as a reference datum. By referring to the conceptual drawing of the signal flow as shown in Fig. 12, we can discover that V_{ASKm} in this case is still of our particular concern. As we knew, V_{ASKm} should be at least higher than $V_{L.B.}$, and it is also demanded as close to V_{ASKu} as possible to fulfill a low-end discrimination. The regions, we are interested in, at which the transistor P4 operate, will be starting at saturation and ending at the subthreshold region. On consideration of the subthreshold, conduction is due to the fact that P4 will not be immediately off while its effective source–gate voltage is smaller than the absolute value of its threshold voltage. This will be somewhat contributive to the decrease of the modulation index. However, it also affects the design of the next stage, and therefore should be considered with carefulness. By ignoring the channel-length modulation, the relationships of the output V_{VSM} of the voltage scaler, associated

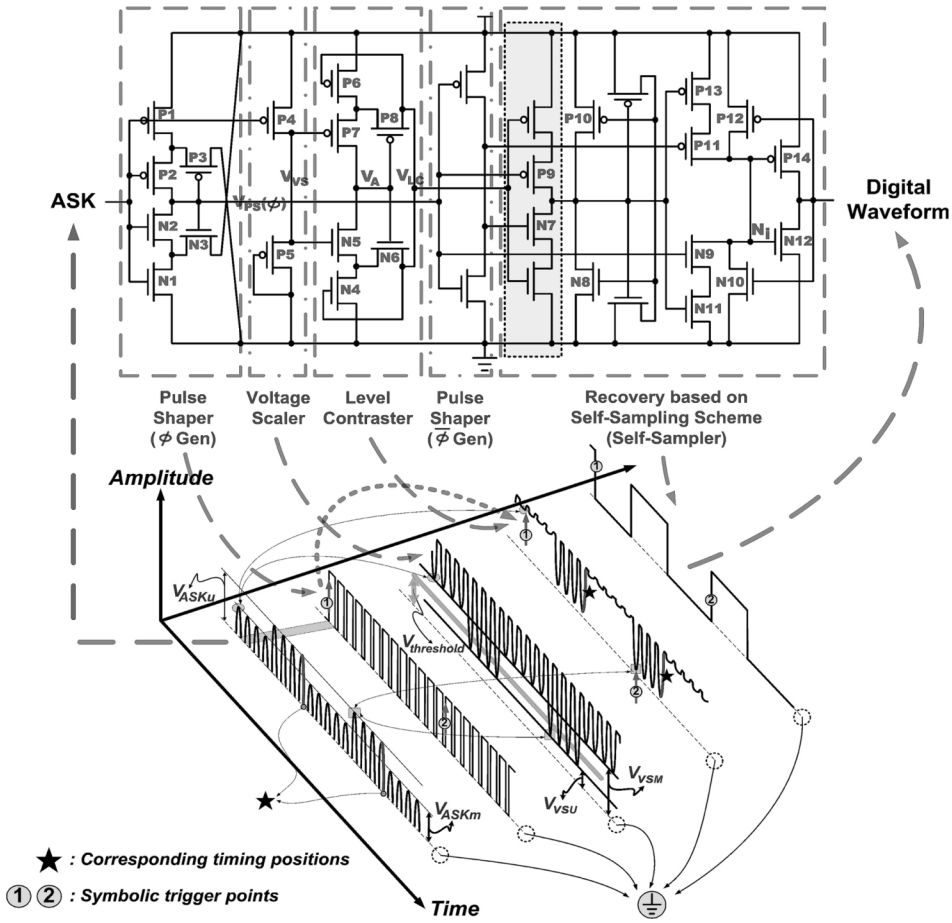

Fig. 12. Proposed demodulator and its conceptual drawing of signal flow.

with V_{ASKm}, can be given as

$$\begin{cases} \dfrac{\left(\frac{W}{L}\right)_{P4}(V_{\mathrm{DD}}-V_{\mathrm{ASKm}}-|V_{tp}|)^2}{\left(\frac{W}{L}\right)_{P5}(V_{\mathrm{VSM}}-|V_{tp}|)^2}=1, \\ \quad \text{for } V_{L.B.}<V_{\mathrm{ASKm}}\le V_{\mathrm{DD}}-|V_{tp}| \\ \dfrac{\left(\frac{W}{L}\right)_{P4}\cdot I_{D0}\cdot e^{(V_{\mathrm{DD}}-V_{\mathrm{ASKm}}/nV_T)}}{K_p\left(\frac{W}{L}\right)_{P5}(V_{\mathrm{VSM}}-|V_{tp}|)^2}=1, \\ \quad \text{for } V_{\mathrm{DD}}-|V_{tp}|<V_{\mathrm{ASKm}} \end{cases} \tag{7}$$

where V_{tp}, I_{D0}, n, V_T, and K_p are pMOS threshold voltage, current coefficient, process-dependent term affected by the depletion region characteristics, thermal voltage, and process parameter of the pMOS, respectively, while the subthreshold relation is cited according to [18]–[20]. Therefore, we obtain

$$\begin{cases} V_{\mathrm{VSM}}=-pV_{\mathrm{ASKm}}+[pV_{\mathrm{DD}}+|V_{tp}|(1-p)], \\ \quad \text{for } V_{L.B.}<V_{\mathrm{ASKm}}\le V_{\mathrm{DD}}-|V_{tp}| \\ V_{\mathrm{VSM}}=q\cdot e^{(V_{\mathrm{DD}}-V_{\mathrm{ASKm}}/2nV_T)}+|V_{tp}|, \\ \quad \text{for } V_{\mathrm{DD}}-|V_{tp}|<V_{\mathrm{ASKm}} \end{cases} \tag{8}$$

where p and q are $\sqrt{((W/L)_{P4}/(W/L)_{P5})}$ and $\sqrt{(I_{D0}\cdot(W/L)_{P4}/K_p\cdot(W/L)_{P5})}$, respectively. In order to connect the voltage scaler with the level contraster sufficiently, the V_{ASKu}-associated output level V_{VSU} of the voltage scaler should be calculated as well. This level, however, is able to be simply deduced by replacing the V_{ASKm} of the subthreshold relation in (8) with V_{DD}, introducing an appropriate relation given as

$$V_{\mathrm{VSU}}=\sqrt{\frac{I_{D0}\cdot\left(\frac{W}{L}\right)_{P4}}{K_p\cdot\left(\frac{W}{L}\right)_{P5}}}+|V_{tp}|. \tag{9}$$

It should be noted that, to make the circuit stable enough as expected, P4 and P5 were designed with a medium Vt , commonly available in many modern CMOS processes including TSMC 0.18-μm, in actual implementation. The low-Vt pMOS only has around 160 mV in the adopted process, which is even smaller than its low-Vt counterpart (250 mV), such that the designed ASKD can be endowed with a modulation index down to 4.35%. Notably, the area increase caused by the implant for the low-Vt pMOS can be omitted.

Following the above, we are now able to link up the voltage scaler with the level contraster more clearly by means of the signal flow illustrated in Fig. 12. Since V_{VSU} and V_{VSM} have been computed, $V_{\mathrm{threshold}}$ is what should be taken into account. As can be seen, the output of the voltage scaler is able to be further processed as the sampling target of the pulse shaper if $V_{\mathrm{threshold}}$ is properly decided to differentiate the modulation (V_{ASKm}) from the unmodulated state (V_{ASKu}). The level contraster serves as a comparator to obtain the required waveform in sampling by making use of a low-power structure proposed by Al-Sarawi [21]. Operation of this level contraster can be

explained as follows. Assuming that the output of the voltage scaler $V_{\rm VS}$ is initially LOW, transistors P7, N6, and P6 are turned on while N5 and P8 are off. N4 is situated at a subthreshold conduction and the drain voltage $V_{\rm LC}$ of P8 and N6 is eventually lower than that for V_{tn}. As $V_{\rm VS}$ approaches $2V_{tn}$, N5 is turned on and V_A decreases. However, the pull-down ability is significantly restricted by N4 since $V_{\rm LC}$ is still below one V_{tn}. After $V_{\rm VS}$ rises to a level that is sufficiently high (i.e., the transition threshold at which V_A switches from HIGH to LOW), V_A decreases to a level at which P8 is completely on. V_{LC} will be soon charged up while V_A drops off rapidly. The conduction relation between the transistors N5, P8, and N4 can reduce the short-circuit effect considerably so as to obtain a notable power efficiency. By symmetry, a similar reduction in the short-circuit current can also be observed when V_A switches from LOW to HIGH. $V_{\rm threshold}$ is thus capable of corresponding to the low-to-high transition threshold of V_A, yielding [21]

$$V_{\rm threshold} = \frac{V_{\rm DD}(R+1)R_p - V_{\rm th}\left[(2R-1)R_p - 1\right]}{(R+1)R_p + 1} \quad (10)$$

where R and R_p denote the ratios of $\sqrt{(g_{mN5}/g_{mP7})}$ and $\sqrt{(g_{mP6}/g_{mP7})}$, respectively (g_m represents the transconductance), while an assumption of $V_{\rm th} = V_{tn} = |V_{tp}|$ has been made to simplify the calculation, which is valid in our employed process since V_{tn} and $|V_{tp}|$ are around 538 and 512 mV, respectively. Hence, by connecting (10) with (8) and (9), one of the concrete design criteria can be determined as

$$V_{\rm VSU} < V_{\rm threshold} < V_{\rm VSM}. \quad (11)$$

For the other criteria, we can referred to the positions marked with asterisk in the conceptual drawing. These positions shown in the ASK signal indicate the occurrence of high-to-low transitions on the data stream. A bit "0" should be recovered after the self-sampler responses to such bit changes. However, for the corresponding timing positions, the level contraster is very likely to lose due to packet waveform as indicated on the depicted $V_{\rm LC}$ signal flow if $V_{\rm VS}$ cannot exceed a transition threshold at which V_A switches from HIGH to LOW. This will result in the proposed circuit failing in demodulation. In the presented design, the worst case timings related to the positions are approximated to when the ASK signal goes back to the system reference level. Therefore, the input level at the positions will enforce an operation of the triode region and an operation of the saturation region on P4 and P5 respectively, resulting in P

$$\frac{2\left(\frac{W}{L}\right)_{\rm P4}\left[(V_{\rm DD}-|V_{tp}|)(V_{\rm DD}-V_{\rm VS})-\frac{1}{2}(V_{\rm DD}-V_{\rm VS})^2\right]}{\left(\frac{W}{L}\right)_{\rm P5}(V_{\rm VS}-|V_{tp}|)^2} = 1. \quad (12)$$

Therefore, by solving (12) and combining the solution with the high-to-low threshold ($V_{\rm hl}$) calculation of V_A according to [21], the remaining criterion can be obtained as

$$V_{\rm VS} = |V_{tp}| + \sqrt{|V_{tp}|^2 - \frac{2(\beta_{\rm P5}|V_{tp}|^2 + 2\beta_{\rm P4}|V_{tp}|V_{\rm DD} - \beta_{\rm P4}V_{\rm DD}{}^2)}{\beta}} \quad (13)$$

$$> \frac{V_{\rm DD}(R_n+1) + V_{\rm th}\left[(2R-1)R_n - 1\right]}{(R+1)R_n + 1} = V_{\rm hl} \quad (14)$$

where $\beta_{\rm P4} = (W/L)_{\rm P4}$, $\beta_{\rm P5} = (W/L)_{\rm P5}$, $\beta = (2(W_{\rm P4}L_{\rm P5} + W_{\rm P5}L_{\rm P4})/L_{\rm P4}L_{\rm P5})$, $R = \sqrt{(g_{\rm mN5}/g_{\rm mP7})}$, and $R_n = \sqrt{(g_{\rm mN4}/g_{\rm mN5})}$ (g_m is the transconductance). Also, the assumption of $V_{\rm th} = V_{tn} = |V_{tp}|$ is still required for the validity of (14).

A final stage of the so-called the self-sampler, which is essentially built from an improved clocked CMOS D-flip-flop (C2MOSDFF), is in charge of the data recovery. It samples the change on the $V_{\rm LC}$ simultaneously whereby the data can be regained immediately by means of the positive-edge trigger of $V_{\rm PS}$. This self-sampler can also be designed with other DFF types. One of the merits of adopting such an architecture is that both its internal and output nodes are firmly clamped by the transistors P9, P11, N7, and N9 without being affected by the internal race caused by the skew between the $V_{\rm PS}$ and its complement. In addition, when the primary stage (brushed in gray) of the sampler is turned on, the internal node N_i of the secondary stage does not become floating and vice versa. It makes the design suitable for low-speed operation since the nodes originally susceptible to noise have been able to remain static by means of the feedback transistors P10, P12, N8, and N10. Both conventional transmission-gate-based DFF (TGDFF) and the proposed DFF are intrinsically lower power consumption than those of the true single-phase-clock (TSPC) -8T and -9T clocked storage elements by virtue of the absence of precharge [20], [22]–[24]. In our case, C2MOSDFF can have a power consumption even lower than the TG-based structure for the same test patterns if the transistors with respect to the feedback keepers can be sized appropriately. Such an improvement in power efficiency can be referred to the less internal switching nodes in C2MOSDFF. The evaluation was carefully conducted by constraining their size to be minimum for both DFFs. It is worthily mentioned that sampling the $V_{\rm LC}$ rather than the original output V_A of the contraster is better suited for our case utilizing C2MOSDFF in spite of the presence of the restricted swing on the $V_{\rm LC}$. When the fan-out ability of the proposed ASKD should be enhanced to satisfy subsequent implanted circuitry, sampling the $V_{\rm LC}$ can both maintain a recovery in-phase with the modulated information represented on the carrier envelope and fulfill the enhancement by just increasing the width of P14 and N12, neither buffering the output node with new cascaded inverters nor increasing the width of P12 and N10. As we knew the two transistors are inherently essential for our design, the space increase is able to be minimized.

Here, we consider the last issue with respect to the design. In the aforementioned discussion regarding the pulse shaper, we only place emphasis on how the essential clock signals can be properly extracted without interruption. However, the timing of occurrence of the positive edge on $V_{\rm PS}$ may also bring about a possible concern for correctly recovering a bit "1" as presented on the symbolic trigger points "2" of Fig. 12. The optimal sampling point can be decided by taking the relation between (10), (14), and the transition threshold $V_{\rm lh_{PS}}$ at which $V_{\rm PS}$ switches

from LOW to HIGH into account. More concretely, we assume that the timing points associated with $V_{\text{threshold}}$, V_{hl}, and $V_{\text{lh}_{\text{PS}}}$ are $T_{\text{threshold}}$, T_{hl}, and $T_{\text{lh}_{\text{PS}}}$ respectively. The design of sampling point determined by the $V_{\text{lh}_{\text{PS}}}$ should be strictly obeyed to the restriction formulated as

$$T_{\text{threshold}} < T_{\text{lh}_{\text{PS}}} < T_{\text{hl}} \tag{15}$$

$$T_{\text{lh}_{\text{PS}}} - T_{\text{threshold}} > T_{\text{setup}} \tag{16}$$

$$T_{\text{hl}} - T_{\text{lh}_{\text{PS}}} > T_{\text{hold}} \tag{17}$$

where T_{setup} and T_{hold} correspond to the setup time and hold time demanded for C2MOSDFF.

C. Simulation Analysis

As discussed in the previous section, owing to the requisites of longer penetration depth, less energy absorption in the human body, and giving immunity from interference of other medical instruments for the implants whose information and energy are wirelessly transmitted, a carrier frequency of 2 MHz is chosen for the current design. In order to demonstrate that the performance of the whole circuit is not drastically affected by temperature and process variations, an entire evaluation under different process corners for a selected temperature range and the set modulation indexes will be helpful for understanding the physical limitation of the demodulator. The temperature range between 35 °C and 41 °C is of general concern for a profound implant due to the constant temperature of the human body in nature. In addition, two worst case conditions are also included in the test to further consider its robustness. The evaluation results are depicted by means of a Shmoo plot shown in Fig. 13. The supposed environment used for this test includes 50-Ω matching resistance and 10-kΩ gate-protective bias resistance to emulate actual measurement interface. Some 5-nH inductors are also added between input signals (including supply) and corresponding nodes of the circuit to consider possible bounce effects. Such effects are associated with the mutual inductance, caused by the wire bonds from the I/O ports as well as from other signal wirings, in an actual chip. As can be seen, the proposed ASKD can accomplish a modulation index up to 4.35% as desired. Also, the modulation rate utilized to perform the test is set to be 50% (1 Mb/s) for each index. Although this modulation rate is considered a bit difficult to achieved in current implantable systems due to the high Q factor, it still provides a meaningful performance index for the demodulators. In addition, since a certain benefit in modulation speed may be derived from a low-end discrimination as discussed previously, it is possible to achieve a high modulation rate and to improve the system efficiency in practice by incorporating some techniques as reported in [25] in the presented ASKD, thereby giving the possibility to overcome the fact that ASK is traditionally less adequate for high data-rate communication.

Figs. 14 and 15 show steady-state performance and the waveforms with respect to circuit operation. The recovered data displayed in Fig. 15 are from the input with 5.89% modulation index for obtaining four corner waveforms. The upper panel shows cases of TT (35 °C) and TT (41 °C) while the lower one expresses the FF (0 °C) and the SS (100 °C). The data transitions V_{HL} and V_{LH}, caused by the sampling of V_{PS} to V_{LC}, can

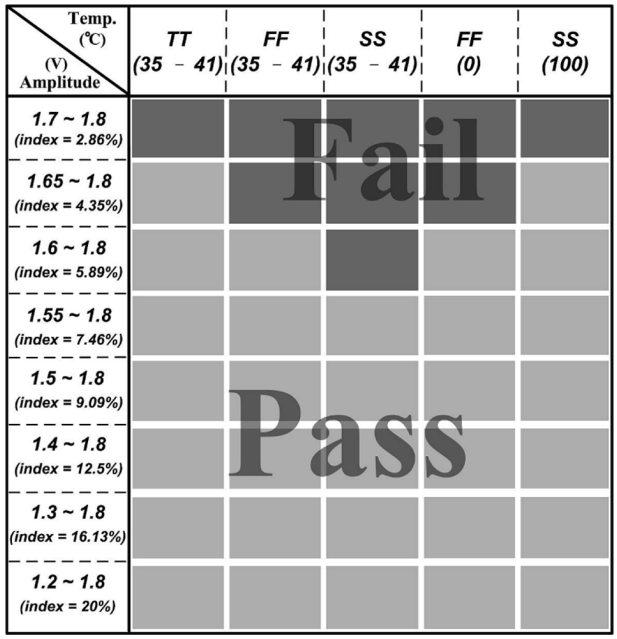

Fig. 13. Shmoo plot for the modulation input versus temperature variation under different process corners. (The terms TT, FF, and SS denote typical-typical, fast-fast, and slow-slow, respectively. The former of each term corresponds to nMOS while the latter corresponds to PMOS.).

be connected with the same transitions shown in the left plot of Fig. 14. The two subfigures in the right plot of Fig. 14 indicate the voltage variations corresponding to the same timing axis for Fig. 15. Maximum offset percentages for both the steady-state voltage level as well the data transition can be calculated according to

$$\frac{\text{Offset}(\max) \cdot -\text{TT}(35)}{\text{TT}(35)} \cdot 100\% \tag{18}$$

thus obtaining the performance parameters of 0.045% (V_{HL}), 0.02% (V_{LH}), and 23.125% (level LOW), while the offset in level HIGH can be almost ignored. Moreover, owing to the self-sampling characteristic, it can be observed from Fig. 15 that output latency of the proposed circuit is kept within one carrier cycle while the presence of data changes on the received carrier.

In addition to the analyses on corner and offset, what one may want to see is how efficient the circuit can perform a correct demodulation when it operates at an input coming from a received carrier carrying a certain noise level. As we have manifested that the discrimination limitation of the proposed ASKD is 4.35% from simulation, we have made the tests with and without adding a noise source to an ideal received carrier seen by the receiver front-end. In these tests, it is supposed that the 4.35% ASK is extracted from an ideal preprocessing stage. The resultant for the latter (with noise source) is a received carrier with 0.77 dB in signal-to-noise ratio (SNR). The simulation waveforms can be seen from Fig. 16 where the modulation-utilized pattern is a random bit stream. The top panel shows ASK obtained from a received carrier in an ideal case, i.e., noise-free. In this case, the corresponding demodulation waveform is error-free. However, the demodulation result, coming from the

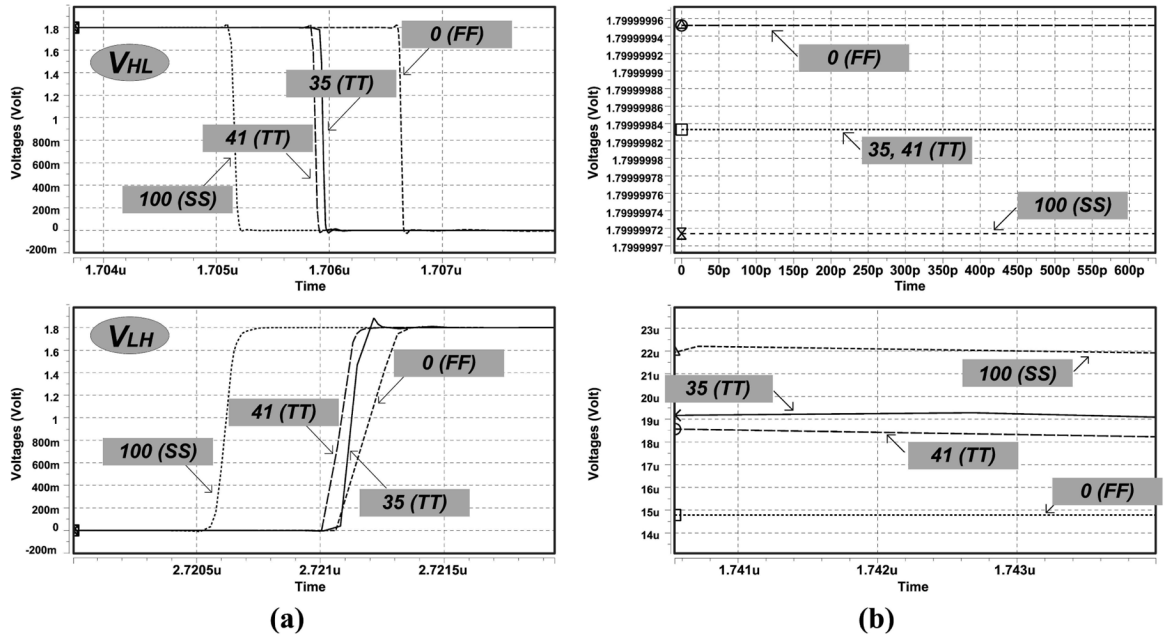

Fig. 14. (a) Data transitions corresponding to Fig. 15. (b) Simulated steady-state voltage variations. The upper subfigure shows the voltage levels with respect to demodulated bit "1" while the lower one shows the levels of bit "0."

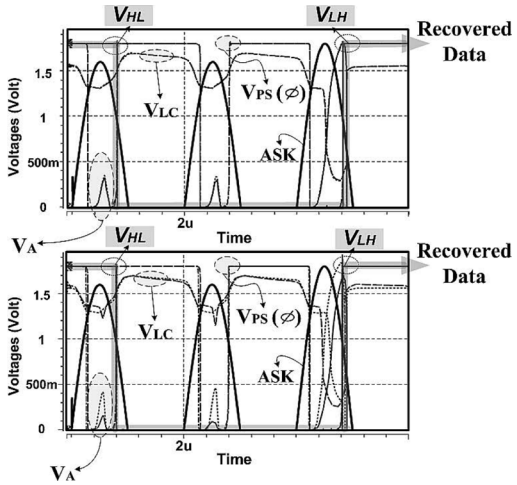

Fig. 15. Simulated demodulation waveforms obtained from HSPICE. The ASK is with a modulation index of 5.89%. The upper panel shows the waveforms of TT (35 °C) and TT (41 °C) while the lower panel are the FF (0 °C) and the SS (100 °C).

received carrier buried in noise, shown in the middle panel reveals that significant errors have occurred. The positions indicating occurrence of the errors can be obtained by comparing the two demodulation results immediately and are shown in the bottom panel, thereby deducing a rough bit error rate (BER) of 2.6×10^{-1} from the present cases (50 bit samples). This BER can be compared with a theoretical value of 1.9×10^{-1} calculated according to the error probability $(P_{B.E.})$ formula [27]

$$P_{B.E.} \cong \frac{1}{2}\left(1 + \frac{1}{\sqrt{\frac{2\pi E_b}{N_0}}}\right) e^{-(E_b/2N_0)} \qquad (19)$$

where $(E_b/2N_0)$ corresponds to the SNR here, resulting in an error percentage that is 36.8% higher than the theoretical calculation. A more realistic performance evaluation related to our design in accordance with the plots of SNR versus BER will be discussed in the following the section. It should be mentioned that (19) is derived from the noncoherent detection, namely, conventional demodulation with capacitors; therefore, it can be used as a comparison for our current design as the proposed ASKD makes the decision of binary digit single clock period long.

IV. Results and Discussion

The proposed self-sampling ASKD (SSASKD), shown in Fig. 17, was fabricated in a TSMC 0.18-μm CMOS technology. It has been integrated into a subminiature prosthetic device for our ongoing implant project. Eight prototypical chips were utilized to obtain the experimental data. An on-chip active N-type cross-coupled rectifier with oxide-enhanced (out of figure) allows a lossless rectification in a demodulation-used signal to support both system-level and stand-alone tests. This rectifier is also protected by an off-chip circuit while the whole chip is activated. Separate I/O pads and an analog multiplexer have also been introduced to not only connect the demodulator and the external supply but also switch off the system components except the implemented ASKD as well as the rectifier when the stand-alone test is enabled. The experiment setting is in agreement with the Shmoo test with the exception of the inductors to avoid input loss and to obtain a rail-to-rail output. The demodulator occupies only a silicon area of 32.3×14.5 (μm^2) without making use of any capacitor or resistor inside. Fig. 18 presents the measurement waveforms. In order to demonstrate its wide-range operation in modulation index and modulation rate, a signal generator instead of a real wireless link was

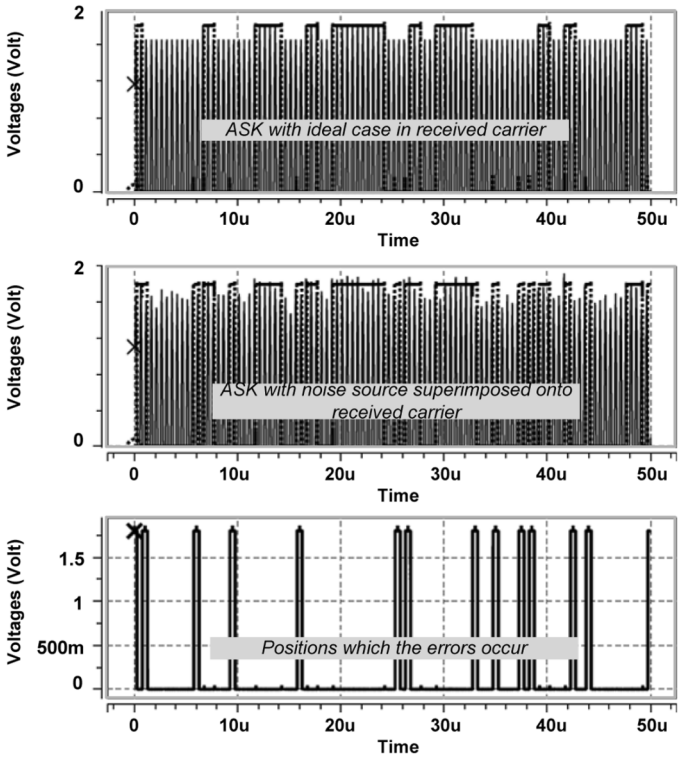

Fig. 16. Simulated comparison of demodulated patterns between ideal and noisy inputs. From the top the waveforms are the ideal ASK and the corresponding data, ASK with 0.77 dB at received carrier and the corresponding data, and the obtained bit error information respectively.

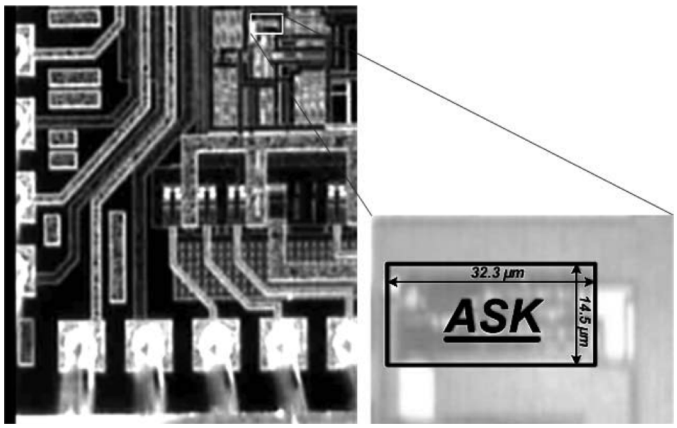

Fig. 17. Photomicrographs of SSASKD and the partial prosthetic chip.

adopted. Significant circuit nodes including the demodulated output have been buffered to drive the probes that may have loads up to 25 pF so that they could accompany the input. According to the measurements, a minimum of 5.26% modulation index is certified. A 4.35% index, which is originally manifested as the discrimination limitation according to the simulation, was however failed in all samples. The malfunction mainly comes from the level contraster. The reason may be due to the undesired parasitic effects caused by the process variation or the mobility difference between two types of the transistors.

The average power consumption and the SNR-BER curves for the SSASK demodulator at three selected modulation indexes are shown in Figs. 19 and 20, respectively. Each mark

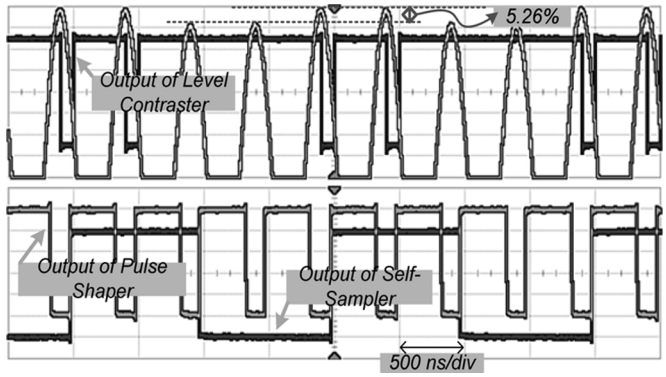

Fig. 18. Traces of demodulator at a 5.26%-index operating condition. The carrier frequency is 2 MHz while the modulation rate is 50%. The vertical scale is set to be 360 mV/div except for the ASK waveform ($V_{\mathrm{ASKu}} = 1.8$ V) for obtaining clear discrimination.

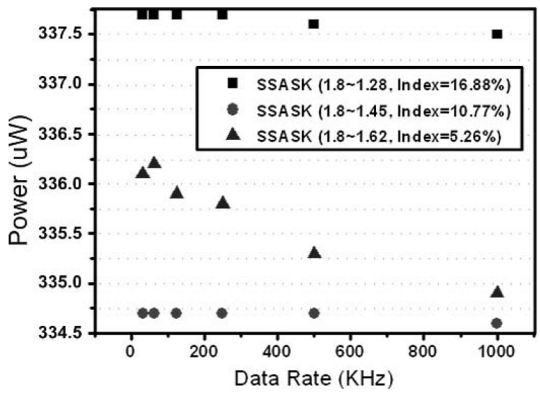

Fig. 19. Measured power consumption under selected indexes.

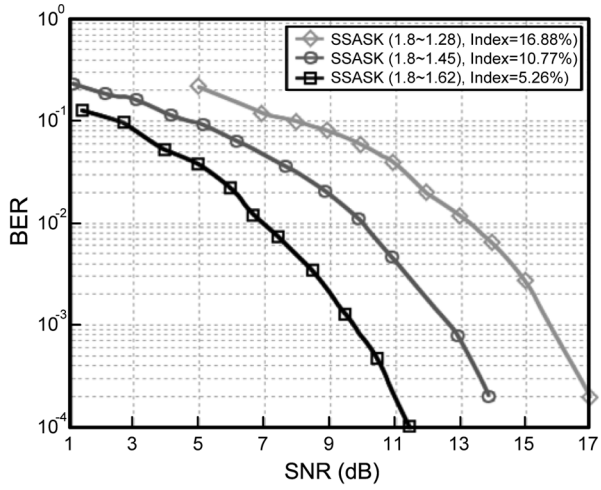

Fig. 20. BER characteristics of the SSASKD.

shown in Fig. 19 is an average obtained from all eight samples. In addition, each test pattern involved in the power estimation is with equal switch probability of "0" and "1." The plots of SNR versus BER presented in Fig. 20 were obtained through comparing the original bit stream with the demodulated pattern. Notably, owing to the random error characteristics, every symbol marked in the plots was calculated from eight-time tests to make

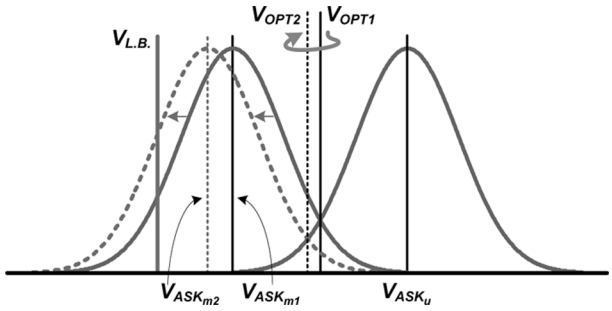

Fig. 21. Error probability distribution curves of the SSASKD.

the statistics comparatively authentic. Interestingly, we can observe from the curves that the demodulation performance is inversely proportional to the modulation index, neither as anticipated beforehand nor as seen in general. This can be explained by using the curves as shown in Fig. 21. These curves show error probability distributions for the ASK signal with Gaussian noise in terms of two cases of modulation index. As the general situation which can be seen in textbooks, the overlapped area, caused by $V_{\mathrm{ASK_{m1}}}$ and $V_{\mathrm{ASK_u}}$, symmetrical to one of the optimal decision thresholds (V_{OPT1}) shows the initial decision error probability for binary data transmission. Particularly, the area below $V_{L.B.}$ (formed with solid lines) denotes the error probability resulted from the malfunction of the pulse shaper in generating ϕ and $\bar{\phi}$ when $V_{\mathrm{ASK_m}}$ is less than $V_{L.B.}$. As $V_{\mathrm{ASK_{m1}}}$ moves to $V_{\mathrm{ASK_{m2}}}$ (i.e., the modulation index increases) while V_{OPT1} migrates to V_{OPT2}, it is obvious that the decrease of the overlapped area around the optimal decision thresholds is less than the increase caused by the malfunction of the pulse shaper. This is the reason that the BER performance of lower modulation index is superior to that of the higher one. When $V_{L.B.}$ is put to a position having long distance to $V_{\mathrm{ASK_m}}$, the effect caused by such a transition threshold of the pulse shaper for BER performance is minimized. The SSASKD will be consistent with the general case that the modulation index is inversely proportional to the BER. Furthermore, the SNR-BER plots in Fig. 20 have more than 1-dB loss compared with the simulated prediction, utilizing the inputs constructed from high-resolution (i.e., large points) piesewise-linear data, as a result of the noise contribution on the on-chip rectifier and the signal paths.

In order to overcome the dependency on $V_{L.B.}$, two feasible approaches are presented. One is to feed the pulse shaper with the input directly obtained from the middle stage of the step down instead of the predefined ASK. In this case a gate-oxide overstress should be seriously taken into account as the pulse shaper will have frequently an input voltage higher than its supply, implying the oxide-enhanced masking must be applied to this stage, and the readjustments on the transition thresholds of the pulse shaper should be done with carefulness to meet the criteria. The other is to put a simple preamplifier in front of the pulse shaper to meet the $V_{L.B.}$ and other conditions demanded of the design. It is envisaged that what one may want to know is that whether the demodulation efficiency is sufficient for a realistic application. As observed from Table I, ASK in medical electronic implants usually has a low modulation rate. Assuming that the rate is just 10% for the intended carrier

TABLE II
PERFORMANCE SUMMARY OF THE DEMODULATOR

Process / Supply	*0.18-μm 1P6M CMOS / 1.8 V*
Core Size	*32.3 μm x 14.5 μm*
R/C Component(s) Inside	*None*
Operation Carrier / Modulation Rate Available	*2 MHz / up to 50% (i.e. 1Mb/s)*
Duty Cycle Offset (Max.)	*0.8 ns (sim.)*
Static Level Variation (Max.)	*4.45 μV (sim.)*
Power Consumption (Avg.)	*336 μW (meas.)*
Discrimination Limitation / Index	*1.8 V ~ 1.65 V (sim.) / 4.35%* *1.8 V ~ 1.62 V (meas.) / 5.26%*
Tolerance in Supply Variation	*+11.67% ~ -11.39% (meas.)* *(0.21V) (0.205V)*

frequency and the case of 5.26% index, which is adequate for most FES implants in terms of the data rate (200 kb/s). In order to obtain a BER lower than 10^{-6}, a predicted SNR of 15 dB should be addressed in accordance with the measured curve, signifying that overall in-band root-mean-square (rms) noise must not exceed 16 mV. This requirement would be achievable for an implant powered and communicating through inductive coupling according to [28] and [29].

The performance of the SSASKD is summarized in Table II. The bottom item indicates that the proposed circuit has a sufficient immunity on supply fluctuation. The supply ripples at the FES implants are usually suppressed within a significantly low amount $(\leq 200\,\mathrm{mV})$ by an on-chip regulator [3], [8], [11], [16], thereby providing the SSASKD with adequate robustness. To sum up, our design not only satisfies the practical requirements of most current electronic implantable devices but also states that it is quite suitable for the applications demanding low cost, low modulation index, and high demodulation performance.

V. CONCLUSION

In this paper, numerous aspects pertinent to designing a novel ASKD have been discussed. The motivation related to the design is to create the possibility of increasing the efficiency of an implantable system powered wirelessly by way of the demodulation technique. The proposed architecture is *RC*-less whereby it can reduce the implant space and consequently advance the fully integrated possibility. Experimental results from both simulation phase and fabricated chips are with good agreement on the modulation index; thereupon the design offers the implantable systems an ultralow-end demodulation so as to improve their efficiency as a whole. In addition, because the ASKD conquers the capacitance dependency of those prior arts by means of the self-sampling, it cannot only be utilized to realize a high-data-rate communication without incurring notable loss caused by the Q reduction in power efficiency, but can also be easily applied to other microsystems such as radio-frequency identification (RFID) transponders and wireless sensor network systems having similar requirements in efficiency. The first edition proof-of-concept prototype is currently serving in our new-generation FES chips to regain requisite command information. Future work will be on the

investigation of practicability of operating the demodulator in an actual wirelessly powered receiver for the implants.

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REFERENCES

[1] G. Gunnar, E. Bruun, and H. Morten, "A chip for an implantable neural stimulator," *J. Analog Integr. Circuits Signal Process.*, vol. 22, pp. 81–89, 1999.

[2] M. Barú, H. Valdenegro, C. Rossi, and F. Silveira, "An ask demodulator in CMOS technology," in *Proc. IV Iberchip Workshop*, Mar del Plata, Argentina, 1998, pp. 37–42.

[3] H. Yu and K. Najafi, "Circuitry for a wireless microsystem for neural recording microprobes," in *Proc. 23rd IEEE-EMBS*, 2001, vol. 1, pp. 761–764.

[4] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. D. Juan, J. D. Weiland, and R. Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1487–1497, Oct. 2000.

[5] Y. T. Lin, T. Wang, S. S. Lu, and G. W. Huang, "A 0.5 V 3.1 mW fully monolithic OOK receiver for wireless local area sensor network," in *Proc. IEEE Int. Asian Solid-State Circuit Conf.*, Hsin-Chu, Taiwan, R.O.C., Nov. 2005, pp. 373–376.

[6] C.-H. Chen, R.-Z. Hwang, L.-S. H. S. Lin, H.-C. Chen, Y.-C. Yang, Y.-T. Lin, S.-A. Yu, Y.-H. Wang, N.-K. Chou, and S.-S. Lu, "A wireless bio-MEMS sensor for C-reactive protein detection based on nanomechanics," in *Proc. IEEE ISSCC*, San Francisco, CA, Feb. 2006, pp. 2298–2307.

[7] M. Dong, C. Zhang, Z. Wang, and Li Dongmei, "A neuro-stimulus chip with telemetry unit for cochlear implant," in *Proc. IEEE Int. Workshop Biomed. Circuits Syst.*, Dec. 2004, pp. S1/3/INV–S1/39.

[8] S.-Y. Lee and S.-C. Lee, "An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2526–2538, Dec. 2005.

[9] A. Djemouai and M. Sawan, "Integrated ask demodulator dedicated to implantable electronic devices," in *Proc. 46th IEEE Midwest Symp. Circuits Syst.*, 2003, pp. 80–83.

[10] A. Djemouai and M. Sawan, "New CMOS current-mode amplitude shift keying demodulator (ASKD) dedicated for implantable electronic devices," in *Proc. Int. Symp. Circuits Syst.*, May 23–26, 2004, vol. 1, pp. I-441–4.

[11] C.-C. Wang, Y.-H. Hsueh, U. F. Chio, and Y.-T. Hsiao, "A C-less ask demodulator for implantable neural interfacing chips," in *Proc. Int. Symp. Circuits Syst.*, May 2004, vol. 4, pp. IV-57–60.

[12] K. Arabi and M. A. Sawan, "Electronic design of a multichannel programmable implant for neuromuscular electrical stimulation," *IEEE Trans. Rehab. Eng.*, vol. 7, no. 2, pp. 204–214, Jun. 1999.

[13] G. J. Suaning and N. H. Lovell, "CMOS neurostimulation ASIC with 100 channels, scaleable output, and bidirectional radio-frequency telemetry," *IEEE Trans. Biomed. Eng.*, vol. 48, no. 2, pp. 248–260, Feb. 2001.

[14] *Understanding the Requirements of ISO/IEC 14443 for Type B Proximity Contactless Identification Card*, , Nov. 2005 [Online]. Available: http://www.atmel.com/dyn/resources/prod_documents/doc2056.pdf

[15] J. P. I. Piella, *Energy Management, Wireless and System Solutions for Highly Integrated Implantable*. Barcelona, Spain: La Universitat Autónoma de Barcelona, 2001.

[16] C. Sauer, M. Stanacevic, G. Cauwenberghs, and N. Thakor, "Power harvesting and telemetry in CMOS for implanted devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2605–2613, Dec. 2005.

[17] H. Yu and R. Bashirullah, "A low power ask clock and data recovery circuit for wireless implantable electronics," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2006, pp. 249–252.

[18] D. J. Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 1, pp. 8–14, Jan. 2004.

[19] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. , NY: McGraw-Hill, 2000.

[20] N. H. E. Weste and D. Harris, *CMOS VLSI Design—A Circuits and Systems Perspective*, 3rd ed. Reading, MA: Addison-Wesley, 2005.

[21] S. F. Al-Sarawi, "Low power Schmitt trigger circuit," *Electron. Lett.*, vol. 38, no. 18, pp. 1009–1010, Aug. 2002.

[22] M. Afghahi and C. Svensson, "A unified single-phase clocking scheme for VLSI systems," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 225–233, Feb. 1990.

[23] J.-S. Wang, P.-H. Yang, and D. Sheng, "Design of a 3-V 300-MHz low-power 8-b8-b pipelined multiplier using pulse-triggered TSPC flip-flops," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 583–592, Apr. 2000.

[24] P. Nilsson and M. Torkelson, "A monolithic digital clock-generator for on-chip clocking of custom DSP's," *IEEE J. Solid-State Circuits*, vol. 31, no. 5, pp. 700–706, May 1996.

[25] P. R. Troyk and M. Edgington, "Inductive links and drivers for remotely-powered telemetry systems," in *Proc. IEEE Antennas Propag. Soc. Int. Symp.*, 2000, pp. 60–62.

[26] A. M. Shams and M. A. Bayoumi, "A novel high-performance CMOS 1-bit full-adder cell," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 5, pp. 478–481, May 2000.

[27] B. P. Lathi, *Modern Digital and Analog Communication Systems*, 3rd ed. New York: Oxford Univ. Press, 1998.

[28] Y. Hu and M. Sawan, "A fully integrated low-power BPSK demodulator for implantable medical devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2552–2562, Dec. 2005.

[29] G. Gudnason and E. Bruun, *CMOS Circuit Design for RF Sensors*, 1st ed. Amsterdam, The Netherlands: Springer, 2002.

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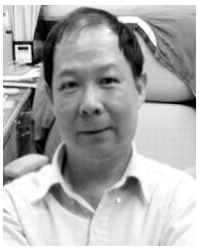

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